

Letter

# Crosstalk Analysis of a CMOS Single Membrane Thermopile Detector Array

Ying Dai <sup>1,\*</sup>,<sup>†</sup> , Syed Zeeshan Ali <sup>2</sup>, Richard Hopper <sup>1</sup>, Claudio Falco <sup>2</sup>, Prakash Pandey <sup>3</sup>, Chris Oxley <sup>3</sup>, Daniel Popa <sup>1</sup>  and Florin Udrea <sup>1</sup>

<sup>1</sup> Department of Engineering, University of Cambridge, Cambridge CB3 0FA, UK; rhh39@cam.ac.uk (R.H.); dp387@cam.ac.uk (D.P.); fu10000@cam.ac.uk (F.U.)

<sup>2</sup> Flusso Limited, Cambridge CB4 0DL, UK; zeeshan.ali@flussold.com (S.Z.A.); claudio.falco@flussold.com (C.F.)

<sup>3</sup> Faculty of Computing, Engineering and Media, De Montfort University, Leicester LE1 9BH, UK; prakash.pandey@dmu.ac.uk (P.P.); choxley0@gmail.com (C.O.)

\* Correspondence: yd283@cam.ac.uk; Tel.: +44-(0)-1223-748311

† Current address: Department of Engineering, University of Cambridge, Cambridge CB3 0FA, UK.

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**Abstract:** We present a new experimental technique to characterise the crosstalk of a thermopile-based thermal imager, based on bi-directional electrical heating of thermopile elements. The new technique provides a significantly simpler and more reliable method to determine the crosstalk, compared to a more complex experimental setup with a laser source. The technique is used to characterise a novel single-chip array, fabricated on a single dielectric membrane. We propose a theoretical model to simulate the crosstalk, which shows good agreement with the experimental results. Our results allow a better understanding of the thermal effects in these devices, which are at the center of a rising market of industrial and consumer applications.

**Keywords:** infrared sensor; thermopile; CMOS; MEMS; seebeck effect; crosstalk

## 1. Introduction

Low-cost and low-power consumption thermal infrared (IR) focal plane arrays (FPAs) are increasingly important for many applications [1–4]. These consist of two-dimensional arrays of imaging pixels (typically bolometers [5], thermopiles [6] or pyroelectric detectors [7]), found within the Internet of Things (IoT) environment [8], and/or consumer electronics [9] applications, including, e.g., activity recognition for care services [10] and presence detection for security [11]; applications which require high volume device manufacturability and battery powered operation [9]. Currently, bolometers [1,5,12] and thermopiles [5,6,13–15] dominate the low-cost IR-FPA market [4]. Bolometers detect temperature induced changes in resistance ( $R$ ), created when the detector element is heated by incident IR radiation. A voltage signal ( $V_B$ ) is obtained by providing a suitable biasing current to the detector element [16]. Compared to bolometers, which often require specialist fabrication and packaging [1,12], IR-FPAs based on thermopiles are easier to manufacture using standard low-cost Complementary Metal–Oxide–Semiconductor (CMOS) fabrication processes [13,14]. In addition, they detect temperature induced changes in electromotive force (i.e., the thermoelectric voltage ( $V_T$ ) generated due to the Seebeck effect [17]), and thus do not require a biasing current, thereby simplifying the interface circuitry [13,14].

Thermopiles are typically made of a series of thermocouples [18], each comprising two conductors (e.g.,  $p^+/n^+$  doped polysilicon [14,19,20], or silicon [13,20]) with dissimilar Seebeck coefficients (typically  $\sim 300 \mu\text{V}/\text{K}$  [20]), where one “hot junction” can be heated while the opposite “cold

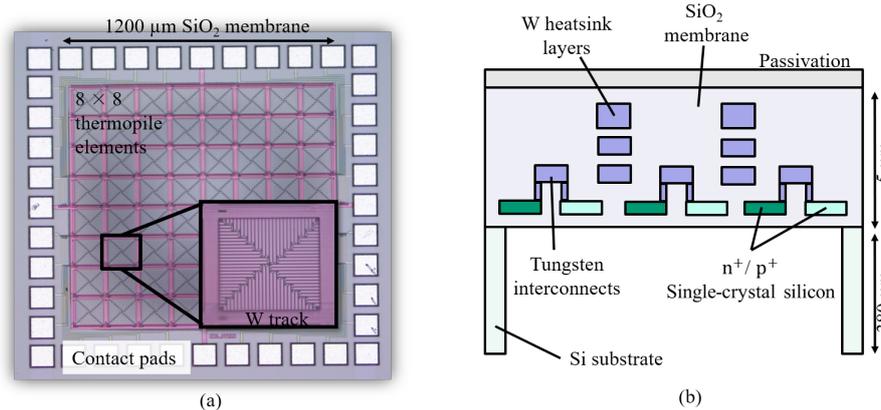
junction" is thermally bonded to a heat-sinking substrate [21]. The thermocouple generates a voltage  $V_T = \alpha\Delta T$  [18] when a temperature gradient  $\Delta T$  is present across its junctions, where  $\alpha$  is the Seebeck coefficient (a measure of the material's efficiency to thermally generate a voltage [17]). Thermopile-based FPAs are composed of an array of thermopile-based pixels located at the focal plane of a lens [4], and produce a thermal image by detecting  $\Delta T$ s between pixel elements. The hot junctions of each pixel's thermocouples are typically thermally isolated by a thin dielectric membrane [21,22]. A voltage  $V_T = N\alpha\Delta T$  (proportional to the number of thermocouples  $N$ ), is generated when the membrane is IR irradiated [18]. We recently demonstrated a low-cost (<1\$) and low-power-consumption ( $\sim$ mW) CMOS-based thermopile FPA fabricated on a single dielectric membrane, employing standard CMOS tungsten (W) metallization layers for heat-sinking of the thermopile cold junctions, and exemplified its potential by applying it to gesture recognition and people-counting [13].

An important figure of merit of a FPA is the pixel-to-pixel crosstalk ( $C$ ) (i.e., the unwanted transfer of signals between pixels [23]), which can affect the spatial resolution of the detector and thus complicate the reconstruction of the desired image [24]. For a thermopile array,  $C$  is defined as the ratio between the  $V_T$  signal generated by an optically irradiated pixel ( $V_{T1}$ ) and that of an adjacent non-irradiated pixel ( $V_{T2}$ ), i.e.,  $C = V_{T2}/V_{T1}$  [6]. In thermal FPAs,  $C$  is dependent on inter-pixel heat diffusion [6], and is typically measured by optically irradiating (e.g., by a laser source [6]) a pixel and comparing its  $V_T$  signal to that of adjacent pixels [6,19]. However, imperfections in the laser focusing can lead to optical leakage from the laser spot, which can be challenging to control and/or quantify [6,19]. A different approach for  $C$ -measurement is to use an on-chip heater for thermal excitation [6]. However, this additional structure increases the fabrication complexity and may compromise the thermal performance of the device.

Here we introduce a novel approach for measuring the crosstalk of a thermopile-based FPA without using a laser source, or an on-chip heater. Our approach uses bi-directional electrical biasing of the thermopile elements themselves to obtain the thermoelectric voltages needed for crosstalk calculations. Moreover, we propose a numerical model to simulate the crosstalk of a single membrane thermopile array design, which we use to better understand the crosstalk formation of these devices.

## 2. Device Fabrication

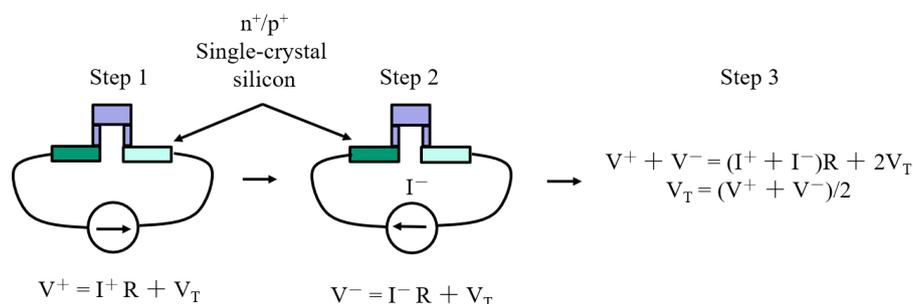
The thermopile detector array is fabricated on a single membrane using a commercial 1  $\mu\text{m}$  silicon on insulator (SOI)-CMOS process on 6 inch Si wafers. The pixels are formed by highly doped  $p^+$  and  $n^+$  single-crystal Si layers formed within the SOI layer. The interconnection between the  $p^+$  and  $n^+$  elements, and the heatsinking tracks between the pixels are formed by three W interconnect layers, with 20  $\mu\text{m}$  track widths, and  $\sim$ 1  $\mu\text{m}$  total thickness. W is an interconnect metal which can be employed in standard high-temperature CMOS processes [25] and it is implemented for heatsinking due to its much higher thermal conductivity ( $\sim$ 80 W/mK) when compared to that of silicon dioxide ( $\text{SiO}_2$ ,  $\sim$ 0.8 W/mK) which forms the membrane of our device. Figure 1a shows the optical image of our device, with the inset showing the zoomed-in structure of a single pixel. The  $\text{SiO}_2$  membrane is  $\sim$ 5  $\mu\text{m}$  thick and has an area of 1200  $\mu\text{m} \times 1200 \mu\text{m}$  (150  $\mu\text{m} \times 150 \mu\text{m}$  for a single pixel), see Figure 1b. The layers are grown on a 380  $\mu\text{m}$  thick Si substrate, back-etched using deep reactive ion etching (DRIE) to form the membrane, with the first  $\text{SiO}_2$  layer acting as an etch stop. A device, with array sizes of 8  $\times$  8 pixels, is fabricated as a proof-of-concept. Each pixel consists of a thermopile with 52 thermocouple pairs. The thermopiles have their cold junctions placed adjacent to the surrounding heatsinking tracks, formed by the three W layers.



**Figure 1.** (a) Optical image of the thermopile array with a magnified image (colour-shifted) of an individual pixel. Chip size = 1.76 mm × 1.76 mm. (b) Cross-sectional view of the numerical model (not to scale) showing the single-crystal Si  $p^+/n^+$  elements and tungsten (W) layers of the thermopile array.

### 3. Experimental Results

To evaluate the crosstalk, we use a bi-directional electrical biasing approach to obtain the voltage  $V_T$  generated by a thermopile (pixel) under thermal stress, as shown in Figure 2. The pixel is thermally stressed by Joule heating [26], i.e., by applying a range of biasing currents (from  $I \sim 10 \mu\text{A}$  to  $200 \mu\text{A}$  in our case) to the thermopile elements, resulting in a heat load ( $RI^2$ ) proportional to the track resistance ( $R$ ). This gives rise to a  $\Delta T$  across its thermocouple's junctions and thus a  $V_T$ . To extract  $V_T$ , we apply a current in both negative and positive directions, as shown in Figure 2. When the  $p^+$  and  $n^+$  Si elements of the pixel are  $I$ -biased, the total generated voltage will then contain an ohmic drop ( $V = IR$ ) contribution, caused by the thermocouple track's  $R$ , added to  $V_T$ . The measured respective voltages, for the applied positive ( $I^+$ ) and negative ( $I^-$ ) electrical currents, will therefore be  $V^+ = I^+R + V_T$  (step 1) and  $V^- = I^-R + V_T$  (step 2), as shown in Figure 2. When added, the voltage due to the electrical resistance (created by the opposing current flows) cancels out, resulting in  $V_T = (V^+ + V^-)/2$  (step 3). The  $V_T$  generated by an adjacent pixel is then directly measured and finally the crosstalk is calculated as the ratio between the two. Three chips were tested to check consistency, with the results presented in Table 1 (measurements with current source), showing  $\sim 2.69\%$  crosstalk. These values are comparable to current state-of-the-art thermopile FPAs [6,13,14], with our novel method being significantly simpler to apply. A comparison with the simulation results, also shown in Table 1, is discussed in the next section.



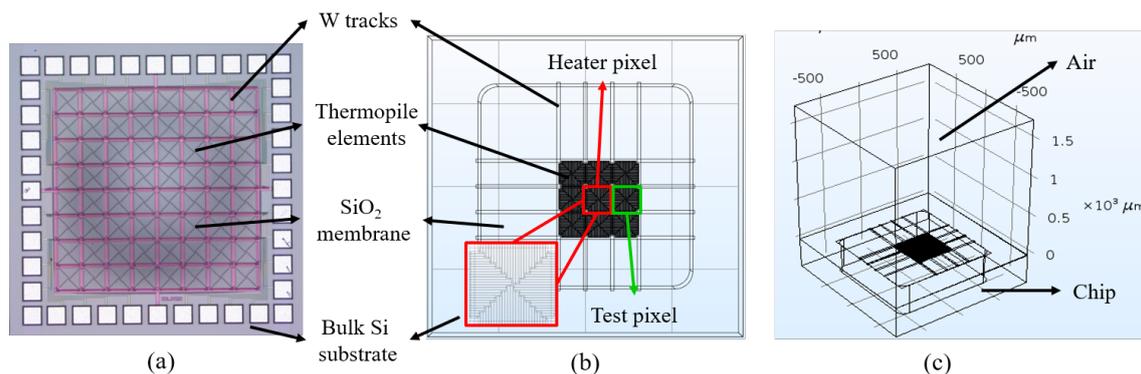
**Figure 2.** Schematic diagram showing the bi-directional electrical biasing measurement method.

**Table 1.** Comparison between experimental and simulation results. Numerical simulations were implemented using both a current source and an uniform heat source across the thermopile elements.

Results	Pixel Resistance (k $\Omega$ )	Crosstalk (%)	Responsivity (V/W)
Measurements with current source	76.07	2.69	73.10
Simulations with current source	76.21	2.70	72.76
Simulations with uniform power source	76.21	3.02	63.05

#### 4. Numerical Simulations

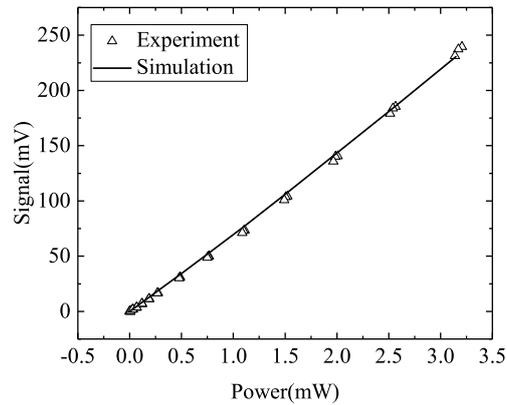
To better understand the thermal behaviour of our device, we perform numerical simulations based on a finite elements method (FEM) model. For a comprehensive depiction of the thermopile's behaviour, we use the heat transfer module, and the electric current module of the commercial software package COMSOL Multiphysics [27]. We reduce the complexity of our model by making the following two simplifications (a comparison between the structure of the real chip and that of our model is shown in Figure 3): we remove the metal pin pads around the membrane (Figure 3a,b), considering their negligible effect on both the electrical and thermal behaviour of the chip [20]; and, we simulate only 9 pixels at the centre of the membrane, and the metal tracks surrounding them (Figure 3b), considering the device contains 64 identical thermopiles (thus reducing the computation time). The 3-dimensional (3D) view of our model (Figure 3c), shows an air cube placed on top of the chip to account for heat losses in the air.



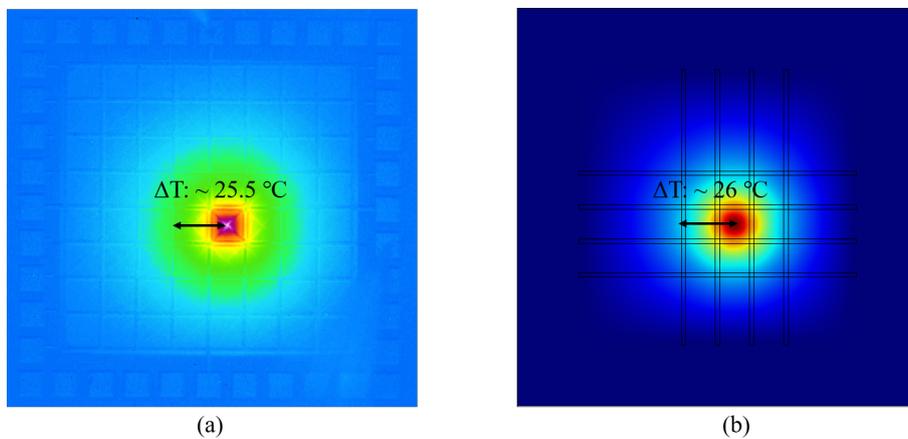
**Figure 3.** (a) Optical image of the thermopile array. Numerical model (b) top view and (c) 3D view.

We compare the simulation and experimental results in Figure 4, showing good agreement for  $V_T$  generated by a pixel as a function of input power. The corresponding crosstalks are 2.7% and 2.69% respectively for the simulations and experiments. We also compare the simulated temperature distribution ( $\Delta T$ ) across the heated pixel, to that measured using an IR thermal microscope, both obtained with a heating  $I \sim 200 \mu\text{A}$  (Figure 5). The respective  $26 \text{ }^\circ\text{C}$  (simulations) and  $25.5 \text{ }^\circ\text{C}$  (experiment)  $\Delta T$ s show good agreement. It is expected that  $T$ -induced changes in the thermal properties of the materials, which would cause any distortion [16], will be limited here as  $T$  changes due to electrical heating are limited.

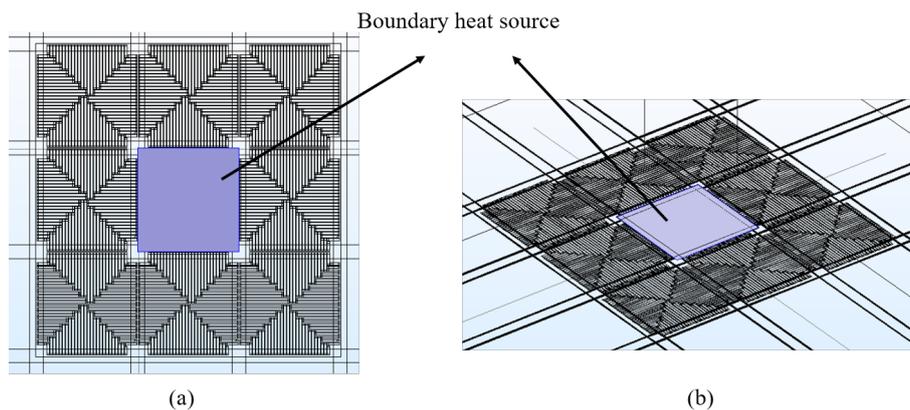
We then consider the effect of a uniform heat source across the pixel, as shown in Figure 6. We thus replace the current biasing with a boundary heat source, across the pixel, to define a constant power dissipation per unit area (a scenario mimicking a laser source illuminating a single pixel). In this case, the pixel is solely heated by the uniform boundary heat source (no current being applied); with the heating power being equivalent to that for the Joule heating scenario. Table 1 shows a comparison of simulated crosstalk values obtained for both heating approaches. The pixel's responsivity, defined as the change in voltage response due to incident optical power [16], is also included.



**Figure 4.** Comparison between simulated and experimentally generated thermoelectric voltages, by a heated pixel at electrical powers from 0 to 3.5 mW.



**Figure 5.** (a) Infrared image of the thermopile detector array chip measured using an IR thermal microscope. (b) Temperature distribution across the chip obtained from the simulations.



**Figure 6.** (a) Top view of the boundary heat source area. (b) 3D view of the boundary heat source area.

The crosstalk simulated with the uniform heat source (3.02%) is slightly higher than that simulated with Joule heating (2.7%), while the responsivity shows an opposite trend, i.e., 13% lower. This is expected, as a non-uniform heat distribution across the pixel enhances  $\Delta T$ , while inter-pixel heat diffusion is limited by the localised thermopile tracks.

## 5. Conclusions

In conclusion, we report a bi-directional electrical biasing method for crosstalk measurements of a thermopile-based IR detector array fabricated on a single dielectric membrane. The use of the thermopile itself as a heater, significantly simplifies the experimental setup, compared to the use of a laser source. We propose a theoretical model to further investigate crosstalk effects in these devices, which shows good agreement with the experimental results. Our results open new perspectives for these novel thermal devices.

**Author Contributions:** Conceptualization, S.Z.A., Y.D., R.H., D.P. and F.U.; investigation, Y.D., S.Z.A., R.H., C.F., D.P. and F.U.; resources, D.P., F.U., P.P. and C.O.; writing, Y.D., R.H. and D.P.; project administration and funding acquisition, D.P. and F.U. All authors have read and agreed to the published version of the manuscript.

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**Conflicts of Interest:** The authors declare no conflict of interest.

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