Modelling of Large Area Trench IGBTs: The Effect of Birds-Beak

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***Abstract*— Three-dimensional modelling is becoming an increasingly prevalent technique to model more complex device structures. However, this alone is insufficient to accurately model large area devices. This study images the birds-beak in a commercial Insulated Gate Bipolar Transistor (IGBT) and highlights how this processing uncertainty, which impacts the channel properties, has a strong effect on the accuracy of TCAD simulations; resulting in the designer struggling to validate models and underappreciating the true behaviour of the device. It has been demonstrated that the birds-beak effect can be accounted for by a simple two-device model which allows for small-scale and large-scale device behaviours to be matched while limiting the computational effort for designers. The practical effects of birds-beaking on device performance has also been considered, and it has been shown that the variation in threshold voltage across the chip area results in a 32% reduction in short-circuit endurance time for the device. To overcome this, an alternative n+ emitter implantation is proposed, using a combination of arsenic and phosphorus, so that the device threshold is unaffected by the presence of birds-beaking and its variation during processing.**

***Index Terms*— Insulated Gate Bipolar Transistor (IGBT), Birds-Beak, Three-dimensional Technology Computer Aided Design modelling (3D TCAD), Endurance Time, Power devices, Power electronics**

I. Introduction

The Insulated Gate Bipolar Transistor (IGBT) has become the dominant power device in the 600V to 4.5kV range [1], with the introduction of the trench technology and the soft punch through (SPT) design. The trench design was first reported in 1986 [2] and demonstrated in 1989 [3] with the intention of increasing the MOS channel density and reducing latch-up susceptibility. Theoretically, a 30-40% overall loss advantage with no serious penalties in safe operating area SOA can be achieved [4]–[6], and advanced trench structures have been developed by numerous manufacturers [7]–[10]. Fabrication of the trench is, however, complex and defects such as birds-beak at the top of the trench occur due to processing variations [11], [12]. The SPT [13], fieldstop (FS) [14] or light punch-through (LPT) [15] designs offer a compromise between the punch through (PT) and non-punch through (NPT) IGBT structures, providing an initial fast turn-off typical of NPT but eliminating the long tail [13], [16]. Compared to the PT design, the SPT has a soft turn-off behaviour reducing noise, overshoot and electromagnetic interference (EMI) issues [13] and a positive coefficient of temperature with resistance, making it suitable for paralleling devices for use in higher power applications [13], [16]. With these benefits, the Trench SPT IGBT is the leading IGBT design.

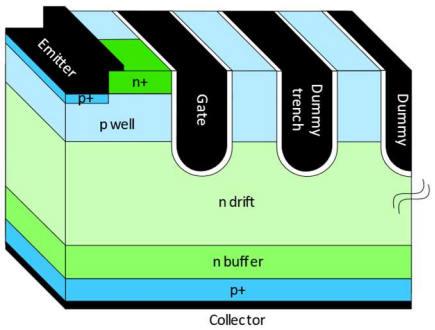

Fig. 1. 3D TCAD model of IGBT

Development of new IGBT designs are becoming increasingly reliant on simulation tools which allow for rapid device development that could not be achieved by manufacturing prototypes due to the cost and time of fabrication. However, to ensure that the device when manufactured performs as expected, it is critical that models are accurate. Three-dimensional (3D) models enable designers to emulate more complex and realistic structures. 3D modelling is becoming increasingly prevalent as processing power becomes more readily available, however, the high computational demands means that designers are restricted to model only a very small proportion of the total device active area. In the case of large area high power devices, processing variations across the chip can become significant, particularly for trench designs, and the simulation model becomes inaccurate as these deviations from the ideal structure are difficult to account for.

This study develops a 3D Sentaurus TCAD model to simulate the behaviour of a 1.7kV 150A Trench IGBT. The effect of process variations across the chip area on the device characteristics are investigated, and simulation techniques to account for this are proposed. The practical implications on device performance as a result of these processing defects are also demonstrated and to minimise their effects, a new n+ emitter implantation design is given.

II. Device Structure

Fig. 1 is a schematic representation of the 3D TCAD IGBT

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model developed in Sentaurus. A 3D model was necessary since the n+ doped region under the emitter was not continuous throughout the whole depth of the device. A 2D variant with modified area scaling factor was explored in Section IV but was found to be inaccurate. The simulation cell was equivalent to 0.000166% of the device active area and represents the smallest possible replicating structure. As such, an area scaling factor is applied to the simulation results so that the output emulates the behaviour of the whole chip. Doping profiles were taken from spreading resistance profiling (SRP) plots and the parameter file for silicon used default values provided by Sentaurus. Both simulation and experimental measurements were conducted at 298K. Experimental data was collected in accordance with IEC standard 60747-9:2007 [17].

III. Development of 3D Model

The device threshold (V_{th}) was matched as shown in Fig. 2, by adjusting the fixed gate oxide charge. The simulation provided excellent sub-threshold matching but the injection of carriers was too high as the gate voltage increased. 10mA corresponds approximately to 8mA/cm^2 where the excess charge in the device is lower than the n-drift doping and therefore, at this low collector current, this discrepancy cannot be attributed to the IGBT pnp transistor gain. The simulated device shows very poor on-state matching, both in terms of the gradient of the I_cV_{ce} curve in the linear region and the saturation current (Fig. 3), with the saturation current exceeding the experimental results by over 5 times (V_g = 9V).

The IGBT saturation current ($I_{C(sat)}$) can be defined as a function of the channel length (L_{ch}), inversion layer mobility (μ_{ni}), the specific capacitance of the gate oxide (C_{ox}), the length of the IGBT channel in the z plane (Z) and the gain of the pnp structure within the IGBT (α_{pnp}) [18];

$$I_{C(sat)} = \frac{\mu_{ni} C_{ox} Z}{2L_{ch}\left(1-\alpha_{pnp}\right)}\left(V_g - V_{th}\right)^2 \qquad (1)$$

Typically the bipolar action of the IGBT [$(1-\alpha_{pnp})^{-1}$] increases the saturation current for a given gate voltage by a factor of 1.6 compared to a MOSFET of the same geometry, and therefore the discrepancy in Fig. 3 cannot be attributed to the hole injection efficiency alone. Fig. 2 showed acceptable agreement with the threshold, and the experimental measurement was taken in a quasistationary state such that there was no gate current when the collector current was recorded. These together indicate that V_g and V_{th} are not the source of the issue. Both Z and L_{ch}, which are dependent solely on the device geometry, were known to be correct in this instance (the area scaling factor can account for, at most, a 15% discrepancy which is insufficient to account for this error). The gate oxide capacitance is fixed by the material (silicon dioxide), the geometry and thickness of the gate oxide trench. The change in saturation current for small variations in thickness is minimal: increasing thickness by 0.01µm only decreases the saturation current by 9%, partly due to the dependence of gate oxide capacitance on the device threshold voltage.

Mobility models were modified, particularly since the threshold measurement indicated the mobility of majority carriers within the channel was slightly high. The High Field Saturation model (when the drift velocity of carriers is no longer proportional to the electric field) was instead calculated parallel to the closest semiconductor–insulator interface, which has been shown to be a more accurate model to represent the MOSFET channel behaviour [19]. The old model for Slotboom bandgap narrowing was also used since it has been shown to be more physically realistic [20]. Specific silicon parameter values based upon crystallographic lattice orientations were used, rather than the default Sentaurus general silicon values. These more specific silicon values were taken from the standard Sentaurus parameter file. Using these models resulted in a 43% reduction in saturation current. The gradient of the I_cV_{ce} curve in the linear region, particularly at higher gate voltages, also had much improved matching to the experimental results. However, the saturation current still exceeded the experimental values by over 200% and, particularly at lower gate voltages, the collector current-collector voltage trace shape still differed significantly from the experimental results.

The effect of emitter shorting the dummy p-well regions (p-well adjacent to the dummy trenches in Fig. 1) was also considered, which in previous simulations was left floating. These dummy p-well regions provide a secondary avenue for hole extraction and therefore reduce the number of electrons injected at the emitter and reduce plasma formation at the top of the device. This emitter shorted device had a 34% decrease in the gradient of the I_cV_{ce} curve in the linear region compared an equivalent device with floating dummy p-well regions, but the saturation

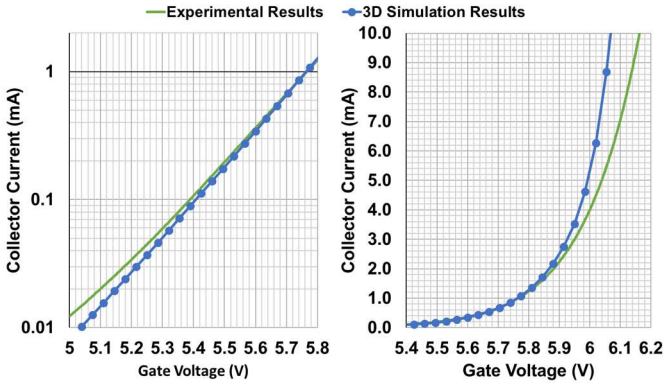


Fig. 2. Gate threshold measurement of original 3D model, Collector-Emitter Voltage (V_{ce})=1V, ambient temperature 298K (a) sub-threshold (b) at threshold, experimental V_{th}=6.04V, simulation V_{th}=5.99V at I_c=5mA

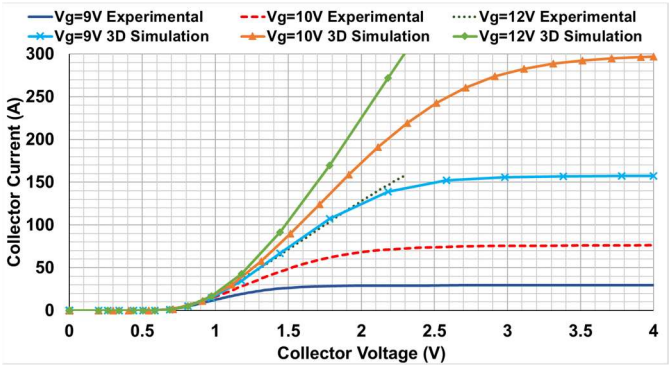
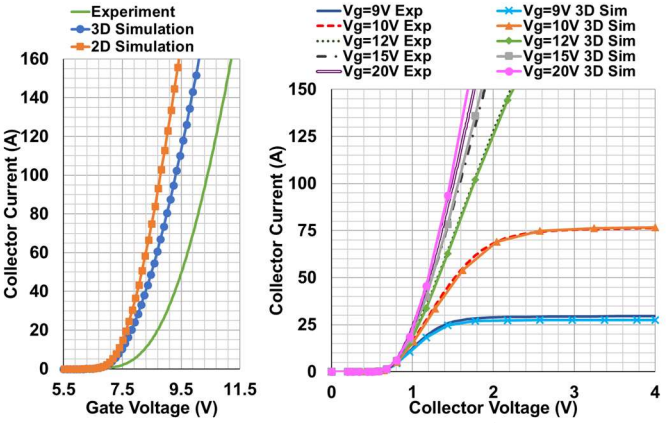


Fig. 3. On-state characteristics, original 3D model, ambient temperature 298K

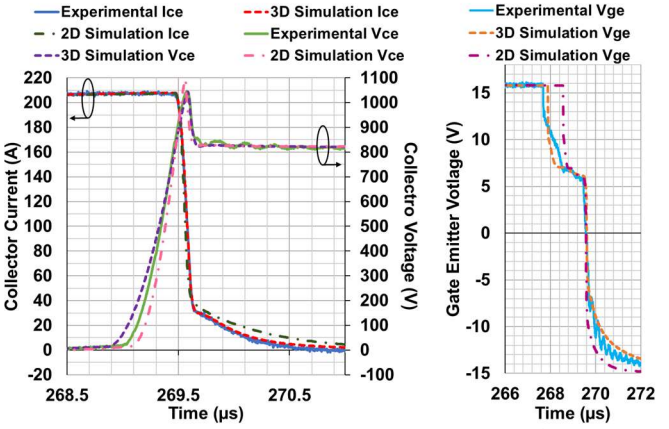
current remained unchanged. This therefore indicates that the MOSFET channel is dominating the error in the saturation current shown in Fig. 3. As a result, self-heating effects were investigated since significant self-heating in the channel region would reduce mobility and therefore reduce the saturation current. Simulations were conducted assuming only the backside of the wafer provided an avenue for thermal extraction (the thermal resistance of this contact was derived from the device datasheet). There are, however, competing effects within the device as threshold voltage decreases with temperature and saturation current is proportional to $(V_g - V_{th})^2$ as shown in (1). Overall, the saturation current only increased by 0.5% compared to the non-thermal model and although this is more realistic of the device conditions, to include lattice heating the computational time increased by over 5 times. Therefore, self-heating effects were not considered in subsequent simulations of on-state or transient switching behaviour.

Fig. 4 (a) shows the relationship between saturation current and gate voltage of the device, using the modified mobility model. The overall shape of the curve for the 3D simulation results matched the experimental curve well, which indicates that the multiplying terms of (1) are correct, however, the simulated results are 0.85V too close to the y axis. Consequently, it can be concluded that either the applied gate voltage or the device threshold in the simulation model is incorrect; but since the measurement was taken at zero gate current, the discrepancy is therefore with the device threshold voltage. Increasing the threshold voltage of the simulated device by 0.85V produces the on-state characteristics shown in Fig. 4 (b). This simplistic modification to the simulation model results in good matching for large currents, however is physically unrealistic as the simulation model turns on at a much higher gate voltage than experimental results have shown and further investigation was required.



(a) (b)

Fig. 4. (a) Saturation current with gate voltage, V_{ce}=4V, ambient temperature 298K for 3D and 2D simulation models with same mobility model and parameters (b) On-state with 3D simulation model threshold voltage increased by 0.85V, ambient temperature 298K



(a) (b)

Fig. 5. Transient measurement comparing simulation results with both models' threshold voltage increased by 0.85V: 2D with doping dependent Masetti model and 3D model from section III, ambient temperature 298K (a) collector-emitter voltage and current (b) gate-emitter voltage

IV. 2D Simulation v 3D Simulation

A 2D simulation model, using the same doping, gate charge and mobility models was also run for comparison. The 2D model still suffered from the same voltage offset as seen for the 3D model (Fig. 4 (a)), providing further evidence that this offset is not a modelling issue. As a result, the threshold voltage of the 2D model also had to be increased by 0.85V for the on-state current to match. Fig. 4 (a) shows that for the 2D model the gradient of the curve is too steep; the 2D model does not account for fringing effects at the n+/p-well boundary along the gate and therefore an error in Z is expected. The 3D simulation output shows that fringing increases the length of the IGBT channel in the z plane by 2.5%, which, if included in the 2D model, would increase the saturation current further. As it stands, there is a 35% discrepancy between the gradient of the 2D results and the experimental curve. This indicates that the 2D model does not fully account for the carrier mobility nor the gain of the bipolar element of the IGBT.

Improved matching could be achieved for the 2D model by replacing the Philips unified mobility model used in the 3D simulation with the doping dependent Masetti model. Both models account for doping-dependent scattering in the device, but the Philips unified mobility model also accounts for other effects such as electron-hole scattering [19]. Implementing this more simplistic Masetti model in the 2D simulation results in the saturation current having only a 2.5% error in the on-state, which can be attributed to the unaccounted fringing effects. It also has a good on-state curve matching. Yet despite this improvement in the on-state matching, when a transient simulation was run with the same conditions (Fig. 5), the 2D simulation with the Masetti doping dependent mobility had too large a tail current compared to both the 3D model and the experimental data (indicating that plasma formation within the device is too high). The gate charge was also much reduced resulting in a significantly shorter Miller plateau time (39% reduction compared to equivalent 3D model), signifying that the gate-collector Miller capacitance is too low in the case of the 2D model. By reintroducing the Philips unified mobility model improvements in the transient output were seen, however the 2D model output was still a significantly worse match to the experimental data compared to the 3D output. Given the 2D model could not provide consistent matching for all of the measurements for a given set of mobility models, it demonstrates the need for a 3D model in this instance. The 2D

model (excluding fringing effects) assumes that all holes are extracted via the p+ under the emitter contact, but the 3D model accounts for a small amount of hole extraction via the p-well emitter contact (behind n+ region in z plane). The three-dimensional effect impacts the behaviour of the device and as a result, a full 3D IGBT model is required to accurately model the device behaviour.

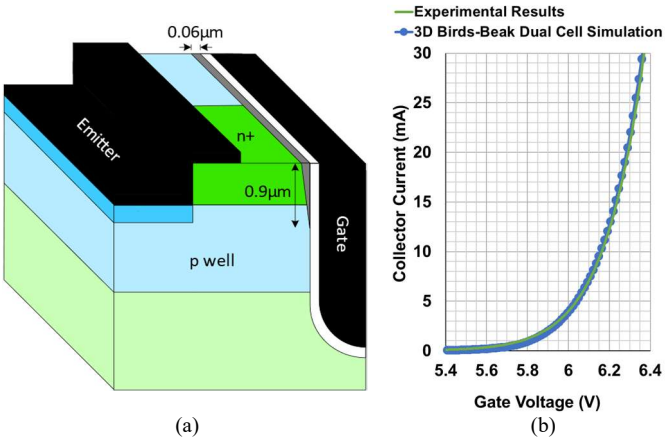
V. Emulating Processing Variations

Using the relationship in (1), for a threshold voltage of 6.04V (collector current 5mA, in agreement with device datasheet values) and the other defined device parameters, the theoretical saturation current is significantly higher than the experimentally measured values. Therefore, to explain this behaviour, it is postulated that a processing defect across the chip area results in a small proportion of the IGBT active area having a threshold voltage of 6.04V and the remainder of the device's active area having a higher threshold voltage. The proportion of the chip area that turns on at higher gate voltages dominates the large current measurements and thus the theoretical relationship described in (1) is still observed.

The most likely cause of this threshold variation across the device is a birds-beak effect. Birds-beak is a defect that is difficult to control in device processing, and the presence of the birds-beak structure affects the point at which strong inversion occurs within the device. The deep trench oxide structure of this device is prone to the birds-beak effect as the oxide width does not remain constant due to processing variations [11], [12]. The device used for this investigation also has an arsenic implanted n+ source: arsenic implants are much higher doped compared to phosphorous, resulting in a shallower implant, but lower contact resistance, which is beneficial for the on-state performance. Typically, birds-beaking can be neglected as it is assumed the oxide width is constant over the depth of the implant; but the combination of trench technology, shallow arsenic implants and large device area brings this effect into consideration.

To test this hypothesis, a new simulation model was developed to account for this birds-beak effect, shown in Fig. 6 (a). It is likely that a range of birds-beak sizes will be present across the device active area, however, to reduce the computational effort, the device was modelled as two structures in parallel: one 3D model which turned on at 6.04V (collector current 5mA) and represented 8% of the total active area, and the remaining active area by a 3D model which had a birds-beak applied at the channel. The applied birds-beak was modelled as a triangular structure, which extended 0.06µm into the channel, and was 0.9µm deep. The threshold of the birds-beak model was set at 6.62V (collector current 5mA).

Fig. 6 (b) shows the threshold model output from the dual birds-beak 3D model, which now has good agreement to the experimental results, compared to the original 3D model in Fig. 2. This measurement is dominated by the behaviour of the 8% device area model cell (no birds-beak), and the reduced active area turning on at this gate voltage diminishes the number of injected carriers, resulting in good matching to the experimental data. Fig. 7 shows the on-state characteristics which are



(a) (b)

Fig. 6. (a) Zoom of 3D TCAD model at the gate with birds-beak structure highlighted in grey (b) Gate threshold measurement of dual device 3D model with birds-beak, V_{cc}=1V, ambient temperature 298K, experimental V_{th}=6.04V, simulation V_{th}=6.04V at I_c=5mA

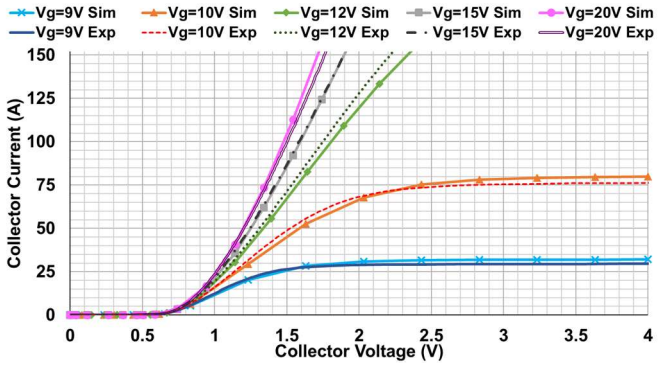
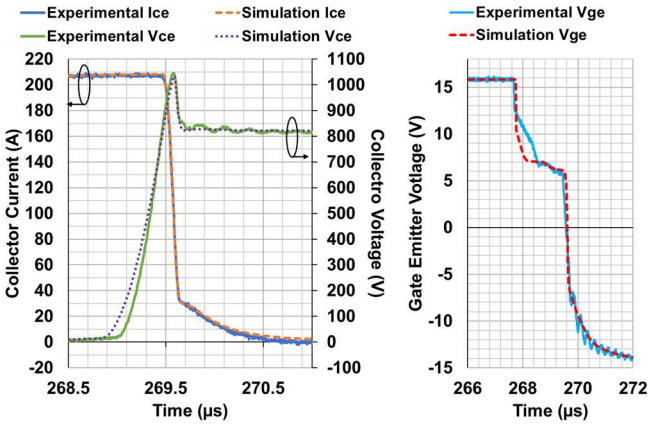


Fig. 7. On-state characteristics of dual device 3D model with birds-beak, ambient temperature 298K



(a) (b)

Fig. 8. Transient measurement of dual device 3D model with birds-beak, ambient temperature 298K (a) collector-emitter voltage and current (b) gate-emitter voltage

dominated by the behaviour of the birds-beak model cell. These results are slightly worse than those provided in Fig. 4 (b), but still in good agreement compared to the original device models (4.4% error in the saturation current at V_g=10V). Introducing the birds-beak structure significantly reduced the saturation current but the gradient of the I_cV_{ce} curve in the linear region decreased as the injection efficiency for the channel worsened. Increasing the IGBT pnp transistor gain (by slightly increasing the p+ collector doping) could counteract this without effecting the saturation current but resulted in too large a tail current

during turn-off. The simulation model could be made more accurate by modelling a range of birds-beak structures to account for more of the process variation across the chip area, however, the computational effort would be significant.

The transient characteristics of this dual model are given in Fig. 8 which show excellent matching. The model does not consider parasitics such as bond wires and busbars, which account for the small variations in V_{ce} and V_{ge}. The Miller plateau voltage does, however, match well indicating that the saturation current of this model accurately replicates the real device. The tail current matches particularly well which signifies that the plasma formation within the IGBT is correct. The turn-off plots demonstrate that this dual cell modelling technique is a reliable method for a device designer to use.

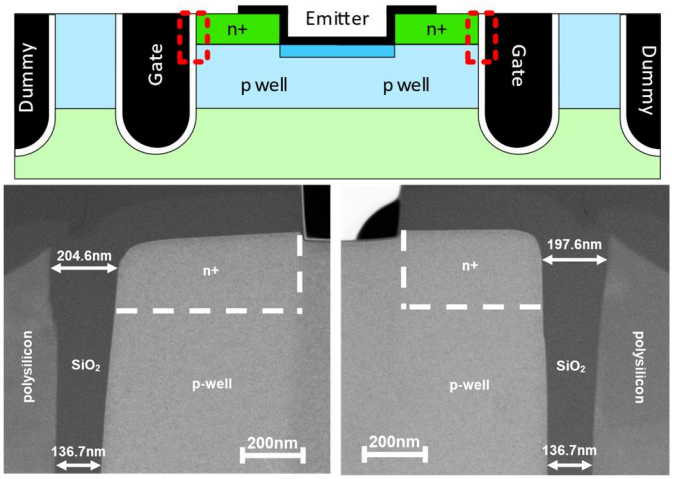
To confirm the presence of birds-beak, the emitter region was observed in cross-section by high angle annular dark field scanning transmission electron microscopy (HAADF-STEM) in a FEI Tecnai Osiris microscope operated at 200 kV. The sample was prepared by focused ion beam. The image in Fig. 9 shows two adjacent gate trenches either side of the emitter contact. Not only is birds-beaking present in the sample, but the amount of birds-beaking varies significantly between the two trenches. For this device, the n+ emitter implantation extends ~0.25µm into the silicon area, which coincides with the thicker oxide regions in the images and the increase in thickness of the oxide is also in line with that included in the simulation model with birds-beak (Fig. 6 (a)). This confirms that birds-beak is the cause of the threshold variation seen in the device behaviour.

VI. Implications of Birds-Beak on Device Performance

The effect of the birds-beak on the device endurance time was investigated using the dual threshold model developed in section V. Self-heating effects were included in this simulation assuming only the backside of the wafer provided an avenue for thermal extraction; a heat loss of 0.6K/W was included at the collector in accordance with the manufacturer's recommended heatsink (0.2K/W thermal resistance of junction to module package, 0.1K/W thermal resistance module package to heatsink, 0.3K/W thermal resistance of heatsink).

A summary of the simulation results are given in Table I. Under short circuit conditions the dual 3D model exhibited an endurance time of 21.36µs; the current density of the lower threshold model (non-birds beak cell with 8% active area) was 0.179mA/cm^2 and the higher threshold model (birds-beak applied) was 0.143mA/cm^2. As a result, thermal breakdown occurs in the region with the lower threshold due to this higher current density. Comparing this result to a single 3D simulation model with the birds-beak applied across the whole of the device active area increased the endurance time by 21.8%. Therefore, it can be concluded that the lower threshold regions are causing local hotspot formation across the chip area which will reduce reliability and ultimately cause premature failure of the device.

This dual model, however, is a simplification of the device heating as, in reality, the lower threshold regions are dispersed across the device active area and are adjacent to other active regions which contain birds-beak. It is expected that there will be an interaction within the silicon bulk for these two regions, which is not considered in the current two cell simulation



(a) (b)

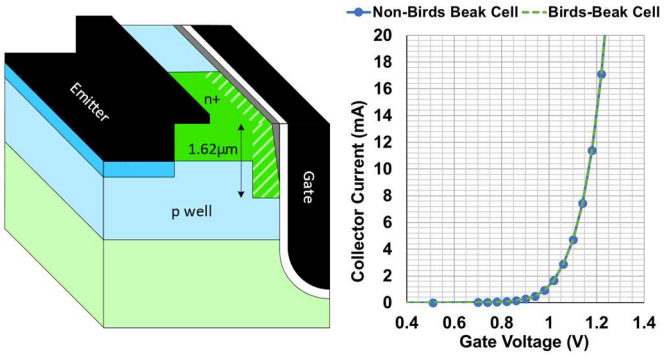
Fig. 9. Cross-sectional HAADF-STEM images of the gate regions showing the presence of birds-beak; (a) and (b) are taken from the regions indicated by the rectangles in the schematic image at the top.

TABLE I
Summary of Endurance Time for 3D Simulation Models Including Lattice Heating and Heatsink at Collector (heat loss of 0.6K/W)

Model Description	Endurance Time
Single model (birds-beak higher threshold cell only)	26.02µs
Dual model (non-birds beak lower threshold 8% active area, paralleled with birds-beak cell)	21.36µs
Dual model (non-birds beak and birds-beak in same silicon bulk, 16% active area, paralleled with birds-beak cell)	17.71µs

model. To address this, a further simulation model was developed where a non-birds-beak cell was situated adjacent to a birds-beak cell with a common collector as one model (similar to the layout in Fig. 9). This accounts for 16% of the active area and the remaining active area is formed from another cell with birds-beak, connected in parallel as before. This more complex model exhibited an endurance time of 17.71µs; a further 17% reduction from the original dual model simulation result. Despite the IGBT having a positive temperature coefficient of resistance which will cause a redistribution of the charge away from the hotter non-birds beak channel region to the birds beak channel region, the interaction in the silicon bulk means that the overall temperature of both channel regions will be slightly higher than in the original dual model, thus causing a faster rate of heating and a lower endurance time than was previously accounted for.

To overcome this reduction in endurance time, an additional phosphorus n+ emitter implant is proposed, shown in Fig. 10 (a). A shallow, highly doped arsenic implant is often preferred in power devices as it provides a low contact resistance to the emitter metal which reduces the on-state losses of the device and susceptibility to thyristor latch up compared to a deeper traditional phosphorus implant. The study has demonstrated, however, that in trench devices the arsenic implant is susceptible to the effects of birds-beaking. As a result, an arsenic phosphorus co-implantation is proposed; a technique commonly implemented in CMOS design [21]. By combining the arsenic and phosphorus implants to form the n+ emitter, a low contact resistance can be achieved while removing the threshold variation across the chip induced by the birds-beaking. The phosphorus implant was applied locally along the gate to the simulation model. The same gaussian implant was applied to the cells with and without the birds-beak, with a peak



(a) (b)

Fig. 10. (a) Zoom of 3D TCAD model at the gate with birds-beak structure highlighted in grey and the additional phosphorus co-implant for n+ source shown in striped green. (b) Threshold measurement of TCAD model with additional phosphorus co-implantation, comparing cells with and without birds-beak for same active area, V_{ce}=1V, ambient temperature 298K

concentration of 1e20cm^{-3} at the emitter metal and the implantation extending to a depth of 1.62µm. Fig. 10 (b) shows the threshold voltages of the two simulated cells, demonstrating that this co-implantation strategy removes the effect of the birds-beak entirely. The threshold of the device is reduced compared to the original model as the p-well doping is lower at the n+ emitter/p-well interface, but designers can compensate for this by increasing the p-well doping concentration, which also helps prevent thyristor latch-up and punch-though under breakdown conditions.

VII. Conclusion

This study presents the importance of accounting for birds-beak process variations in large-area devices, and that 3D modelling techniques alone do not guarantee an accurate device model. The birds-beak phenomenon has been successfully imaged and it has been demonstrated that this effect can be accommodated by a simple two-device simulation model to account for the variation in threshold voltages across the chip area. This two-model technique reduces computational effort for designers while producing accurate results. The birds-beak phenomenon has been shown to reduce the short-circuit endurance time of the chip by 31.9% as the areas of lower threshold conduct 25.2% higher current density compared to regions of the device which suffer from birds-beak. To overcome this, an arsenic phosphorus co-implantation technique was demonstrated in simulation where it was shown that there was no variation in device threshold even with the presence of the birds-beak and/or variations across the area.

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