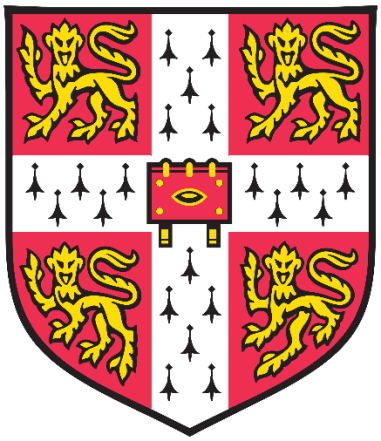
Pico-grid: Multiple Multitype Energy Harvesting System



A thesis submitted for the degree of Doctor of Philosophy

by

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Abstract

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PICO-GRID: MULTIPLE MULTITYPE ENERGY HARVESTING SYSTEM

This thesis focuses on the development of a low power energy harvesting system specifically targeted for wireless sensor nodes (WSN) and wireless body area network (WBAN) applications. The idea for the system is derived from the operation of a micro-grid and therefore is termed as a pico-grid and it is capable of simultaneously delivering power from multiple and multitype energy harvesters to the load at the same time, through the proposed parallel load sharing mechanism achieved by a voltage droop control method. Solar panels and thermoelectric generator (TEG) are demonstrated as the main energy harvesters for the system.

Since the magnitude of the output power of the harvesters is time-varying, the droop gain in the droop feedback circuitry should be designed to be dynamic and self-adjusted according to this variation. This ensures that the maximum power is capable to be delivered to the load at all times. To achieve this, the droop gain is integrated with a light dependent resistor (LDR) and thermistor whose resistance varies with the magnitude of the source of energy for the solar panel and TEG, respectively. The experimental results demonstrate a successful variation droop mechanism and all connected sources are able to share equal load demands between them, with a maximum load sharing error of 5 %. The same mechanism is also demonstrated to work for maximum power point tracking (MPPT) functionality. This concept can potentially be extended to any other types of energy harvester.

The integration of energy storage elements becomes a necessity in the pico-grid, in order to support the intermittent and sporadic nature of the output power for the harvesters. A rechargeable battery and supercapacitor are integrated in the system, and each is accurately designed to be charged when the loading in the system is low and discharged when the loading in the system is high. The dc bus voltage which indicates the magnitude of the loading in the system is utilised as the signal for the desired mode of operation. The constructed system demonstrates a successful operation of charging and discharging at specific levels of loading in the system.

The system is then integrated and the first wearable prototype of the pico-grid is built and tested. A successful operation of the prototype is demonstrated and the load demand is shared equally between the source converters and energy storage. Furthermore, the pico-grid is shown

to possess an inherent plug-and-play capability for the source and load converters. Few recommendations are presented in order to further improve the feasibility and reliability of the prototype for real world applications.

Next, due to the opportunity of working with a new semiconductor compound and accessibility to the fabrication facilities, a ZnON thin film diode is fabricated and intended to be implemented as a flexible rectifier circuit. The fabrication process can be done at low temperature, hence opening up the possibility of depositing the device on a flexible substrate. From the temperature dependent I-V measurements, a novel method of extracting important parameters such as ideality factor, barrier height, and series resistance of the diode based on a curve fitting method is proposed. It is determined that the ideality factor of the fabricated diode is high (> 2 at RT), due to the existence of other transport mechanism apart from thermionic emission that dominates the conduction process at lower temperature. It is concluded that the high series resistance of the fabricated diode (3.8 kΩ at RT) would mainly hinder the performance of the diode in a rectifier circuit.

Declaration

This thesis is a collection of work completed by the author whilst pursuing his doctorate at the Department of Engineering, University of Cambridge. The work is entirely original except where due reference has been made. No contents from this thesis have been submitted at this institution or elsewhere for the application of another degree or qualification.

This thesis is comprised of 44672 words and 94 figures and tables. These do not exceed the limits set by the Department of Engineering.

Mohamad Hazwan bin Mohd Daut

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List of Abbreviations

ac	alternating Current
CC-CV	constant current-constant voltage
CMOS	complementary metal-oxide-semiconductor
COTS	commercial-off-the-shelf
dc	direct current
EDLC	electric double layer capacitor
EM	electromagnetic
ESR	equivalent series resistance
GPS	global positioning system
HEV	hybrid electric vehicle
IC	integrated circuit
IoT	Internet-of-Things
I-T-V	current-temperature-voltage
I-V	current-voltage
JST	Japan solderless terminal
LDO	low-dropout
LDR	light dependent resistor
MIS	metal-insulator-semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
MPP	maximum power point
MPPT	maximum power point tracking
MS	metal-semiconductor
NTC	negative temperature coefficient
OCV	open circuit voltage
PCB	printed circuit board
PCE	power conversion efficiency
PnP	plug-and-play
PTC	positive temperature coefficient
P.U	per unit

P-V	power-voltage
RB	rechargeable battery
SBD	Schottky barrier diode
SC	supercapacitor
SEM	scanning electron microscope
SG	specific gravity
SOC	state of charge
SP1	solar panel 1
SP2	solar panel 2
TCO	transparent conductive oxide
TEG	thermoelectric generator
TFT	thin film transistor
UVLO	undervoltage-lockout
V-I	voltage-current
WBAN	wireless body area network
WSN	wireless sensor nodes
ZnO	zinc oxide
ZnON	zinc oxynitride

List of Publications

Publications related to this thesis

M. H. B. Mohd Daut, A. Nathan, "Self-Adjusted Voltage Droop Load Sharing Mechanism for Paralleling Multiple Low Power DC-DC Converters for Energy Harvesting Applications", IEEE Transactions on Industrial Electronics, 2018 (submitted – under review).

M. H. B. Mohd Daut, D. G. Hasko, A. Nathan, "Picogrid: An Integrated Multiple Harvesters, Energy Storage and Loads System for WSN and WBAN", IEEE Transactions on Industrial Electronics, 2018 (ready to be submitted).

M. H. B. Mohd Daut, John F. Wager, A. Nathan, "ZnON MIS Diodes", IEEE Journal of Electron Devices Society, 2018 (submitted – under review).

Publication not related to this thesis

M. Y. Fan, **M. H. B. Mohd Daut**, "Unity Power Factor, Voltage Step-Up/Down Conversion Pulse-Width Modulated Switching Rectification for Wireless Power Transfer Receiver", IEEE Transactions on Power Electronics, 2018 (accepted – to appear).

Conferences

M. H. B. Mohd Daut, Guangyu Yao, Hanbin Ma, Arokia Nathan, "Fabrication and Electrical Characterisations of ZnON MIS Diode", TCM 2016, Greece (oral presentation).

M. H. B. Mohd Daut, Arokia Nathan, "Energy harvesting system for wearables", Robinson College Graduate Conference 2016, United Kingdom (oral presentation).

Chapter 1

Introduction

1.1 Background and Motivation

Wearable devices are one of the emerging technological applications with a market share that has steadily increased from an estimated $25 billion (USD) in 2015 to $35 billion (USD) in 2018. It is forecasted to grow further to $150 billion (USD) in 2026 [1]. Immense interest particularly in health related devices has flourished and attracted multiple investments and resulted in the birth of many start-up companies focusing on this area. Whilst the first generation devices mostly serve as a complement to smartphones, the second generation and latest trend tends to move towards ‘embrace devices’, which are autonomous devices capable of carrying out specific tasks and functionality without the assistance of smartphones and capable of communicating with other devices through the emerging concept of ‘Internet-of-Things’. With the current trend, it is expected that in the future, many wearable devices will be worn by a single person, each carrying out a different and specific set of functions, and autonomously functioning with or without communications between them, as illustrated in Figure 1.1.

The nature of wearable devices which should be small, light, and compact would limit the battery size, and as a result, many of these devices are designed to have a very low power consumption to prevent the need of frequent recharging or battery replacement (typically from nW to mW). Moreover, most wearable devices are related to monitoring (body temperature,

glucose level, blood pressure *etc.*) or manually activated functionality (GPS, running timer *etc.*), which means that these devices mostly spend their time in 'sleeping' or 'standby' mode, which consume a very low quiescent power. In this aspect, there is an opportunity to power up these devices directly from the energy harvested from the human body. In recent years, the concept of energy harvesting has sparked an interest throughout the industry, and the number of publications related to this field has increased dramatically. Ever since its first proposal in a scientific publication by Starner in 1996 [2], the concept of harvesting energy from the human body is becoming more realistic now than it was 20 years ago as there has been an increase in the introduction of the energy harvesters or transducers that are capable of offering good efficiency, supported by the decreasing power consumption of most electrical and electronic devices. The interest to integrate energy harvesting mechanism into wearable devices arises due to few advantages. These include the reduction of system cost, less impact to the environment, less maintenance, and the possibility to further scale down the devices.

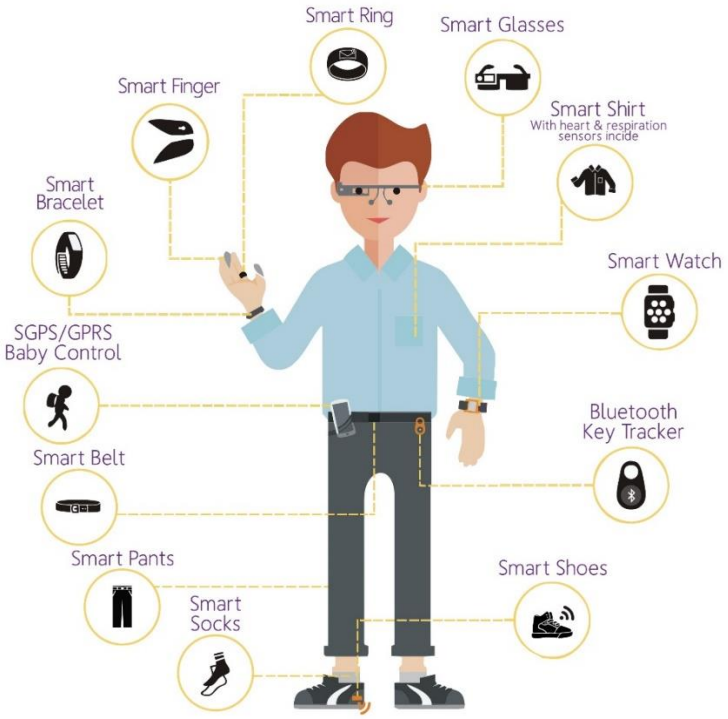


Figure 1.1: Wearables on a person in the future. Image taken from RoweBots [3].

The human body is an abundant energy generator, however with a low mechanical efficiency of around 15 -30 % which results in a lot of energy available to be harvested via various mechanisms. To put this into perspective, the daily amount of energy used by a human body is approximately 10 MJ (equivalent to 800 typical AA batteries or 0.2 kg of body fat), and based

on the metabolic efficiency alone, a significant amount of energy is released into the surroundings, mainly in the form of heat [4]. There are two main types of mechanism to harvest this energy; thermoelectric and through motion and vibration. Another possibility is to harvest energy from the surroundings through wearable harvesters or transducers, such as the concept of wearable solar panel and wearable electromagnetic wave rectenna.

Thermal energy from the human body can be harvested to produce electrical energy by means of thermoelectric devices. These devices contain thermoelectric material which can generate electrical voltage from temperature differences (Seebeck effect). Since the human body is continuously regulated to be at 36 °C, a significant amount of heat (up to 100 W [5]) is released to the surroundings. By placing thermoelectric generators on the human body, energy can be harvested from the difference between the body temperature and the surrounding temperature. The amount of harvested energy mainly depends on the magnitude of temperature difference and the surface area of the thermoelectric generator. Using this method, typically around few µW to mW can be harvested from a single thermoelectric generator placed on the human body.

Three main transducers are used to harvest energy from the motion and vibration of the human body. These are piezoelectric transducer (utilises piezoelectric material which can generate voltage when it vibrates), electromagnetic induction (utilises magnetic material to generate voltage from motion based on Faraday's law), and electrostatic transducer (varying capacitance under constant charge or constant voltage condition). Unlike thermal energy, motion and vibration energy is not continuously available to be harvested except when the human body is in motion. Generally, the amount that can be harvested from this method is in the µW range.

Apart from harvesting energy directly from the human body, it can also be used as a transducer to harvest energy from the surroundings. This is the case for electromagnetic wave (EM), in which the human body can act as an antenna to pick up this signal. Human tissues have a very high dielectric constant and can be easily coupled with a low frequency EM wave. This will then generate electricity in the human body, due to its conductive property. However, the amount of energy that can be harvested from this method is very low (approximately 50 µW from [6]). Finally, by placing a wearable solar panel on human body, a significant amount of energy can be harvested from the surrounding illumination. For example, an integrated jacket with 16 solar panels has been demonstrated capable of generating 0.5 W of power during sunny day [7]. The method of harvesting energy from the human body and surrounding is presented in Figure 1.2.

Figure 1.2: Mechanism to harvest energy from the human body and surroundings to generate power for wearable devices. Images taken from their respective publications in [7]–[14].

Wearable devices will require a steady dc supply voltage in order to operate reliably. In order to power up wearable devices from the energy harvested from the human body, a power converter is needed as the front-end interface (rectifier or DC-DC converter). This power converter needs to be a low power converter. Furthermore, energy buffer/storage is also needed in order the support the intermittent nature of the energy harvester. The full system of wearable devices with energy powered from the human body would comprise all of these elements; energy harvester, power converter, energy storage, and wearables as shown in Figure 1.3.

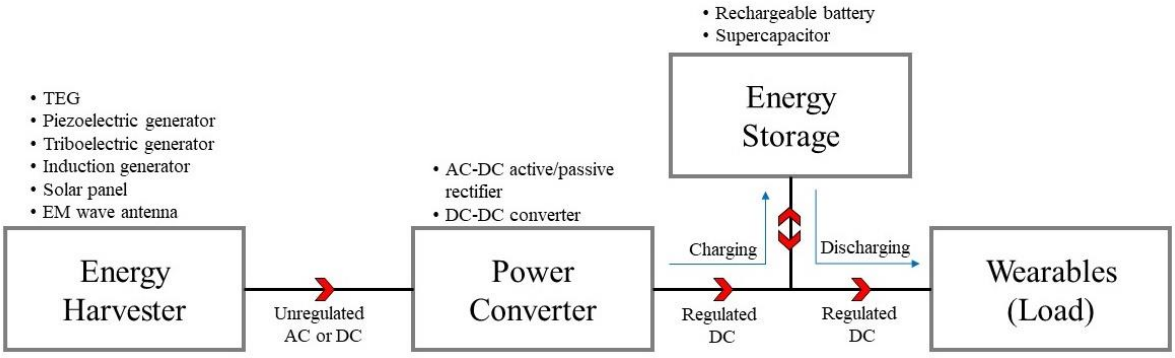


Figure 1.3: System architecture of a wearables with its own energy harvester and energy storage.

From this, a major problem could potentially arise and subsequently an opportunity presents itself. In the future, it is forecasted that a human body would have a lot of wearable devices, and if each system were to be integrated with an individual dedicated energy harvester, then there would be multiple harvesters and multiple energy storage on a human body, which is an inefficient approach. Moreover, some energy harvesters are needed to be placed on a specific location on the human body for maximum efficiency but wearable devices may be worn on other parts of the body. There exist an opportunity for the harvesters and storage system for all of the wearable devices to be tied together to a single unit, reducing the size and weight of the whole system. If we can imagine that a human body is like a big city with multiple localised power plants (energy harvester and storage), multiple residential houses and industrial areas which consume power (wearable devices), and a big overhead cable connecting them together (conductive fibre through clothing), then we can imagine that the whole system can be modelled as the electricity grid system. From this, the concept of pico-grid, which is a low power grid system designed specifically to harvest energy from human body and distribute this energy to power up wearable devices is proposed, designed, and discussed.

1.2 Aim and Objectives

The main aim of this PhD project is to demonstrate a working prototype of a multiple energy harvesters system designed to power up multiple low power loads through a single link system. The introduction of the system itself which is named as a pico-grid, since it is possibly the smallest possible scale of the grid system, is the main contribution of this PhD. The main focus of the PhD is therefore to design an integrated system of these multiple sub-systems, and to ensure a seamless operation of the integrated system.

In order to achieve the main aim, the objectives that need to be completed include:

- Define the operation modes and parameters of the proposed pico-grid system, such as system architecture, power flow control, and voltage range.
- Design each sub-system independently within the set operation in order to ensure that each system can work independently before integrating them together.
- Determine and design an efficient load sharing mechanism among connected energy harvesters. In the system, the power consumed by all of the wearables will be jointly provided by multiple harvesters at the same time and therefore, a load sharing mechanism is needed to achieve this.
- Determine and design energy buffer and storage charging and discharging mechanism in the pico-grid. Energy storage is a requisite in the system and acts not only as buffer or storage for the harvested energy, but also as a back-up power supply in the case when energy is unavailable from the harvesters. In that sense, this sub-system serves either as a load or power source, depending on the power level in the system bus.
- Design a cut-off mechanism and load shedding operation in order to ensure the safety and reliability of the pico-grid system.
- Demonstrate the integration of each sub-system and a final working prototype of the pico-grid system. The performance of the system will be analysed to ensure it meets the specifications set for the application requirements.

It should be noted that the pico-grid system is a system that comprises many sub-systems, and whilst each sub-system can potentially be further optimised to suit the overall operation of the integrated system, the main focus of this PhD project however is not to design and optimise each system but rather focus on introducing the system itself and to demonstrate an approach of systematic integration of each sub-system in order to achieve a working pico-grid prototype.

1.3 Pico-grid

One of the most important innovations that has driven industrial and technological revolutions and enabled the development of a modernised world is the grid system. This system has enabled power to be delivered to any remote area from far away sources. Grid system is an autonomous interconnected system comprised of multiple energy sources and multiple loads connected via overhead cables (national grid).

The concept of a grid can be scaled down and applied exclusively on human body to power up wearable devices as shown in Figure 1.4, and is called 'pico-grid'. In this, a system of energy harvesters and multiple wearable devices are connected through a single bus, where the power flow takes place.

Since most wearable devices require a dc supply voltage, and since some energy harvesters generate dc voltage, the link which connects all of the elements together is proposed to be operated in dc. Plus, energy storage such as rechargeable battery and supercapacitor are also in dc, therefore by using a dc link bus, the need for any rectifier or inverter is eliminated and thus increases the efficiency of the system. This is unlike the typical grid system, which is mostly operated in ac. However, there is an emerging concept of a dc micro-grid, which is a small scale localised grid system connected to the main grid system and capable of providing and generating power on their own.

The pico-grid is proposed to be operated at 2.2 V, since this voltage is an intermediate level between a typical li-ion rechargeable battery (3.7 to 4.2 V) and the expected voltage produced by the energy harvesters (in the range from few mV to 1.5 V). Furthermore, most wearable devices require a dc supply voltage in the 5 V vicinity, which makes 2.2 V a good choice for the bus voltage. The voltage cannot be too low or too high from this range as the DC-DC converter would be pushed to the limit in order to provide a higher step-up or step-down ratio, which in turn would generate high losses and reduce the efficiency of the entire system.

The system architecture of the pico-grid is shown in Figure 1.5. There are two main operations, determined by the control system, and defined by the amount of available power and load demand:

- Condition 1 – power produced by energy harvesters is the same or higher than the load demand, in this case, the excess available power is used to charge the storage system.

- Condition 2 – power produced by energy harvesters is lower than the load demand, in this case, the storage system will discharge to support the load demand. If the demand is still not met, then load shedding process will start based on the priority of the loads.

Finally, since pico-grid is used to supply power for wearable devices, the plug-and-play functionality is one of the required features in the system. The pico-grid will be designed to enable plug-and-play functionality not just for the wearable devices, but also for the energy harvesters.

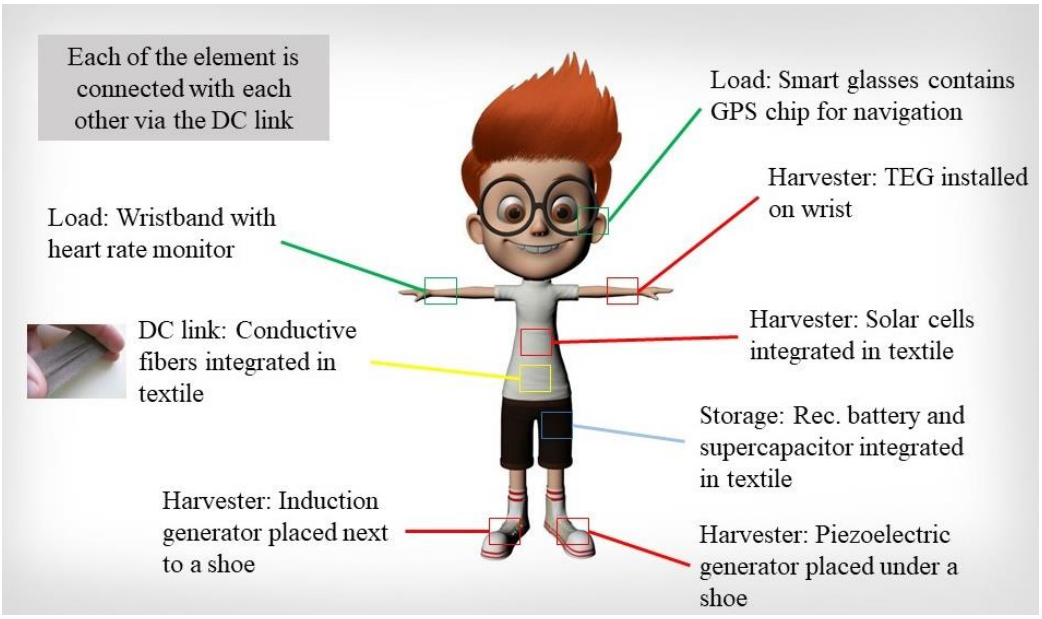


Figure 1.4: The final prototype proposed for the pico-grid system on human body.

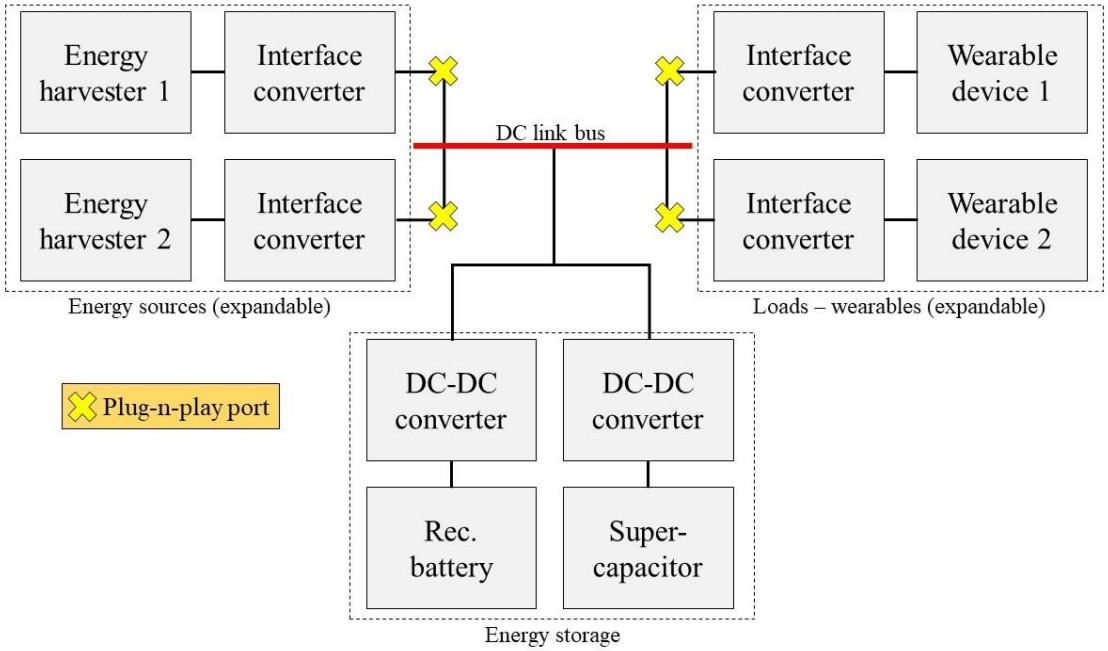


Figure 1.5: System architecture for pico-grid system.

1.4 Thesis Outline

The contents of this thesis encompass the design, construction, testing, and evaluation of each sub-system related to the pico-grid system. After each sub-system has been designed and tested to ensure individual successful operation, all sub-systems are integrated together to form the full working system prototype, which is then tested and evaluated.

Chapter 2 provides an overview and overall design for the control system for the harvester converters to ensure successful parallel load sharing operation. The theory for load sharing is presented and discussed at the beginning of the chapter, and then the control design based on the proposed droop mechanism is presented, simulated, and discussed. Solar panel and thermoelectric generator (TEG) are selected to be the main energy harvesters. As the nature of the output power for these harvesters is time-varying, the droop mechanism needs to be designed to follow the variation of this power, to ensure maximum power is capable to be delivered to the load. Finally, the construction of multiple source converters for these harvesters with the proposed self-adjusted droop control system is presented and the performance is evaluated.

Chapter 3 presents the power flow operation for the power converters for the storage system which serves as the backbone for the pico-grid operation. A supercapacitor and rechargeable battery are selected as the main energy storage element. The mode select circuit to control the power flow for charging and discharging mechanism is presented and tested. Several important operations such as start-up operation are presented and evaluated. The proposed mechanism for load shedding is also presented and discussed. Experiments and tests are carried out to test the feasibility of the proposed mechanism and the performance is presented and discussed.

Chapter 4 which is the most important chapter presents the integration steps of the whole sub-systems and discusses and evaluates the performance of the entire system. The first wearable prototype is built from the integrated system and the performance is evaluated. Few recommendations for improving the first prototype in order to be implemented in real world applications are outlined by the end of the chapter.

Chapter 5 presents an additional side project during the PhD involving fabrication and electrical characterisation of ZnON thin film diode in MIS structure which could potentially be deposited on a flexible substrate. This diode is initially intended to be implemented as a rectifier circuit

for energy harvesting applications. The results for the fabrication and subsequent temperature dependent I-V and C-V characterisations are presented and discussed.

Finally, the conclusions and future work are presented in Chapter 6.

Chapter 2

Parallel Load Sharing – Theory and Demonstration

2.1 Foreword

In this chapter, the concept of simultaneously extracting energy from multiple harvesters is proposed, discussed, simulated, and demonstrated. This operation of load sharing among harvesters is a very important feature of the pico-grid system (multiple sources multiple loads), which differentiates it from the typical single source single load or single source multiple loads systems. The control method to achieve a seamless load sharing operation is presented and discussed. This method which relies on the concept of voltage droop regulation is further improved by integrating a self-adjusted feature to ensure that the variation of input power is considered. Finally, a multiple sources multiple loads system is built from commercial-off-the-shelf (COTS) components and the functionality of the load sharing concept is demonstrated.

2.2 Background and Theory

2.2.1 The Need for Multiple Multitype Energy Harvesters

Recently, the concept of WBAN has surfaced and attracted significant attention throughout the wearables industry [15]. In this system, a network of wirelessly interconnected sensors on human body work together to sense and monitor certain parameters of the body, which are mostly health-related, and send the signals to the processing centre, normally to a mobile phone, to alert the user on any fore coming health issues. This concept is very similar to the

WSN, in which a network of multiple sensors works autonomously and send signals to the central processor. These concepts are all related to the emerging concept of Internet-of-Things (IoT), in which multiple sensors, devices, appliances, and almost any product, are wirelessly connected and capable of exchanging data, sending instructions and commands, enabling wireless integration of almost every aspect of electronics devices. For WBAN and WSN, since most of the networks comprise sensors, therefore the power consumption of each node is very low. Traditionally, this is powered by a rechargeable battery. However, major drawbacks associated with a rechargeable battery such as a frequent charging requirement, performance degradation over time, operation sensitivity over a specific temperature range, and eventually the need for a replacement have made the integration of energy harvesting mechanism into these systems a more logical and realistic approach. Furthermore, multiple researchers have introduced efficient energy harvesters that can harvest and scavenge enough energy to sustain the operation of these wireless nodes. Multiple standalone sensor node systems powered by a single energy harvester have been introduced in the publications [16]–[19]. However, the intermittent and sporadic nature of the power output of most energy harvesters means that integration of energy storage is still a requisite requirement in these systems. This means that the nature of the harvester itself defeats the purpose of having the harvester in the system to replace the rechargeable battery. To counter this particular issue, the use of multiple and multitype energy harvesters in the system is introduced. Multiple harvesters with different energy harvesting or scavenging mechanisms (hence multitype) are needed to ensure a higher opportunity for a continuous supply of power, hence capable of sustaining the operation of these systems.

To reduce the overall footprints of the multiple energy harvesters, a single cell comprising multiple and multitype harvesters has been proposed. For example, recently Guo *et al.* [20] have introduced a hybrid triboelectric-electromagnetic generator capable of harvesting mechanical energy from harsh environments. The weakness with their generator is the harvesting mechanism solely relies on surrounding mechanical energy, and when this one type of energy is unavailable, then the amount of harvested power depletes to zero. A better solution to this type of hybrid energy harvester is a generator that can harvest multiple surrounding energy at once, such as the one demonstrated by Wu *et al.* [21], which is capable of harvesting mechanical, solar, and chemical energy at the same time. Other examples are demonstrated by Zheng *et al.* [22] and Lee *et al.* [23]. However, these papers do not outline another challenging

aspect associated with multiple and multitype harvesting system, which is how to extract and deliver the energy from all of these sources simultaneously to the target load.

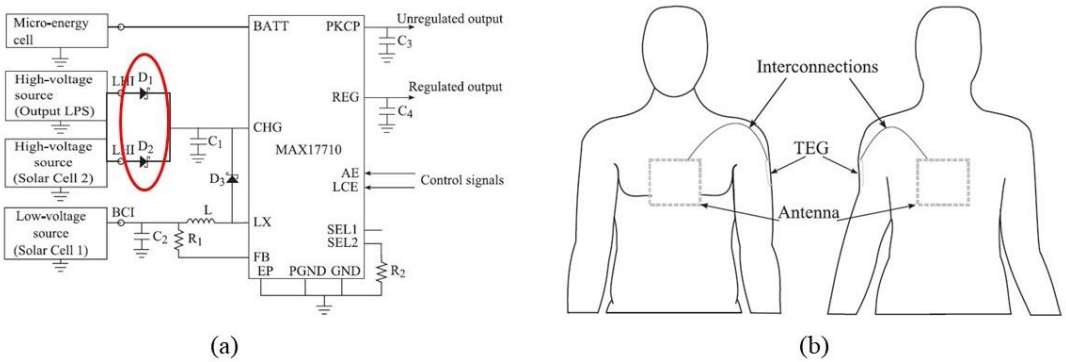


Figure 2.1: (a) shows a multiple multitype energy harvesting system proposed by Lemey *et al*. [24]. The red oval shows the OR-ing diode configuration. (b) shows the actual depictions of the system on the human body. Images taken from [24].

Multiple methods have been proposed in the literature in relation to the power flow management and connectivity between multiple and multitype energy harvesters in a single system. The most common method of connecting two or more energy sources is through the power OR-ing method, in which every source is connected in parallel to a common link through a passive diode or a transistor in diode configuration. This diode serves to prevent each harvester to be perceived as a load by other harvesters, thereby preventing the power to flow to the harvester. Although this method ensures that the power is always delivered to the load if at least one of the sources is generating power, it suffers from energy wastage if two or more sources are generating power, since only the source with the highest voltage will be connected to the load. If the sources are energy harvesters, then the energy harvested by only one harvester with the highest voltage will be delivered to the load, regardless of the availability of another harvester with a higher power. For example, Lemey *et al.* [24] have demonstrated a system in which the large area around the antenna integrated in smart fabric interactive textile (SFIT) for WBAN is utilised for a multiple energy harvesting system. In their system, they used TEGs and solar panels with OR-ing diodes connected between them to supply COTS chip MAX 17710 to deliver regulated power to the load and charging battery at the same time. The main issue with their system is the OR-ing diodes which prevent the power to be extracted from both harvesters at the same time. However, this work is probably the closest concept to a pico-grid system, in which multiple harvesters are integrated together on human body in a single system

as shown in Figure 2.1. The same direct connection with the OR-ing mechanism is also presented by Tan *et al.* [25], Romani *et al.* [26], and Carli *et al.* [27] as shown in Figure 2.2.

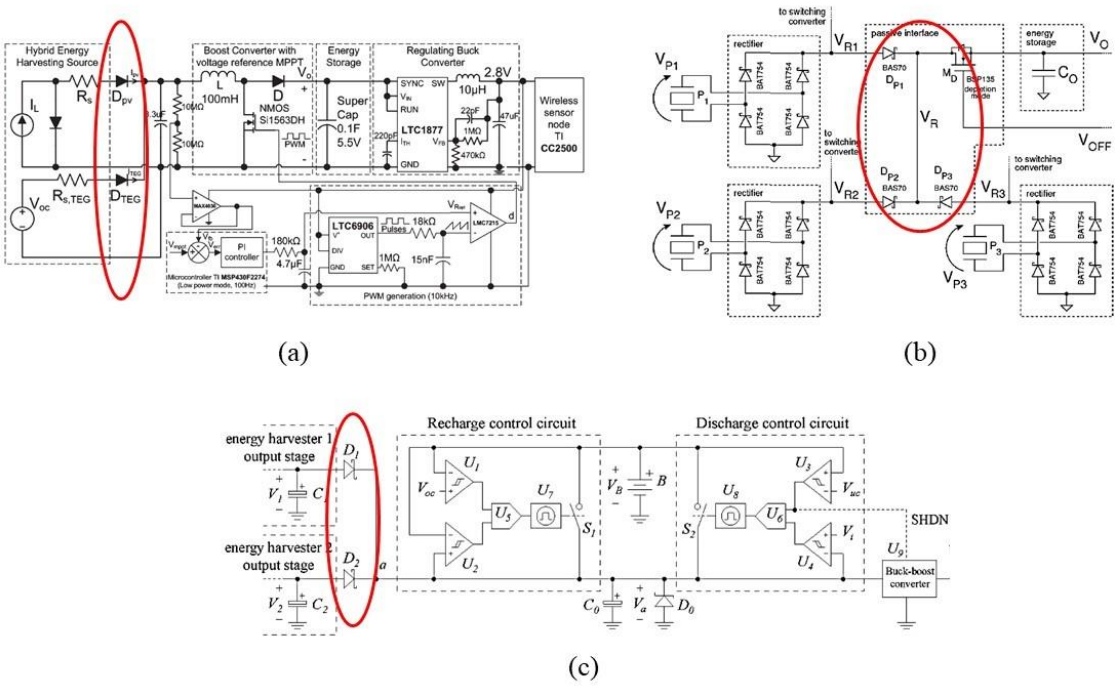


Figure 2.2: Multiple multitype energy harvesting systems using OR-ing method reported in publications; (a) from [25], (b) from [26], (c) from [27]. Red ovals show the OR-ing configuration.

In the previous OR-ing configuration, one of the criteria that must be met by the energy harvesters in order to ensure successful delivery of power to the load is that the voltage produced by the harvesters must exceed the diode turn-on voltage, which is around 0.7 V for COTS silicon p-n diode, 0.3 V for COTS Schottky diode, and the threshold voltage of the COTS transistor for passive diode configured from a transistor. This means that some high power low voltage energy harvesters such as TEG would have difficulty to get its power transferred to the load. Furthermore, even for those harvesters that generate enough voltage to barely exceed this turn-on voltage, power loss incurred in terms of voltage drop across the diode would be enormous, further reducing the magnitude of power delivered to the loads. To counter this problem, the voltage of the harvesters is stepped up by the means of a power converter before the OR-ing diode as demonstrated by Magno *et al.* [28]. Another method of using a low drop-out (LDO) voltage regulator to replace OR-ing diode, hence increasing the overall power transfer efficiency was also demonstrated by Farrarons *et al.* [29]. However, the main issue associated with the power OR-ing method, in which only one harvester will be

connected to the load regardless of the availability of other harvesters still exists. Moreover, the power consumption of the power converter itself must be taken into consideration when evaluating the performance of the whole system.

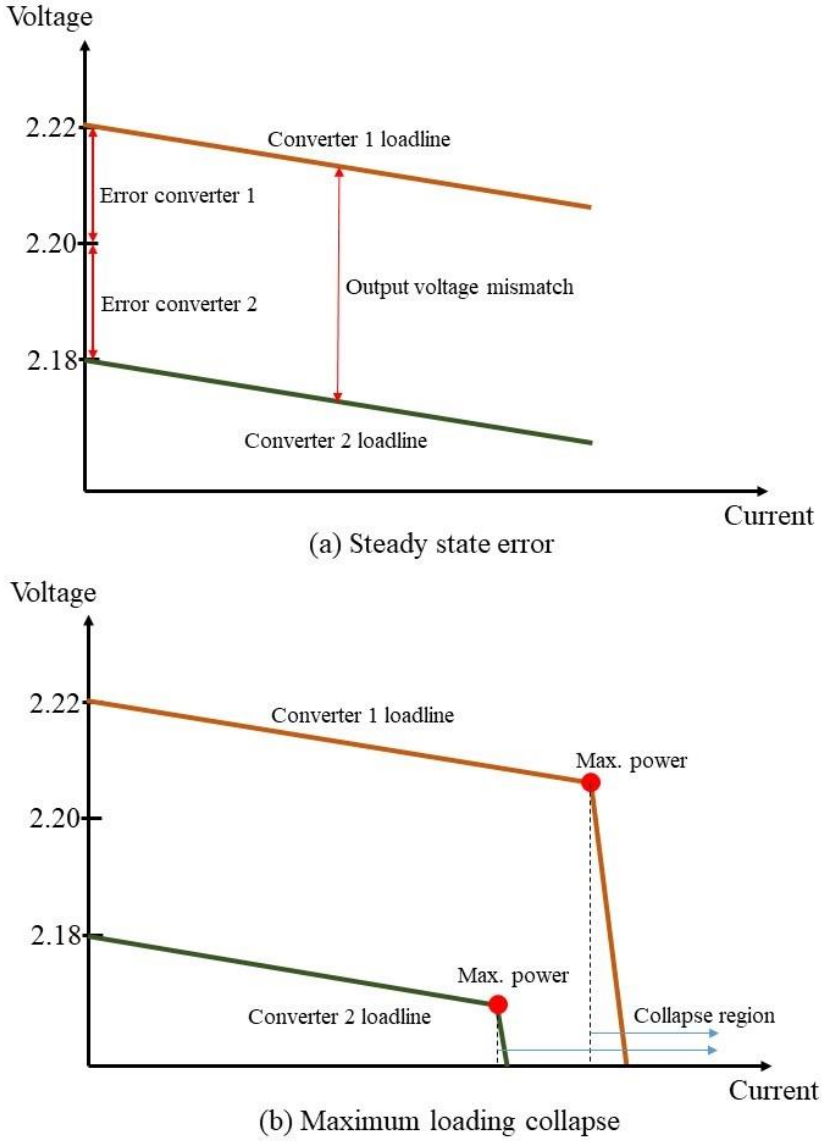
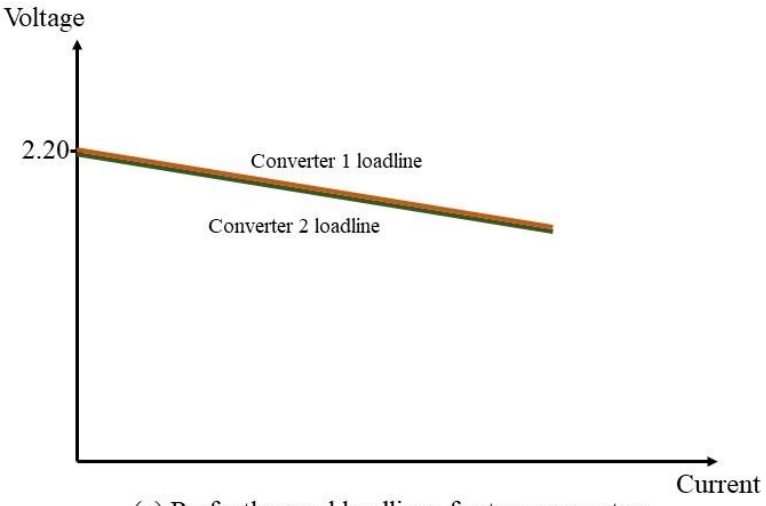


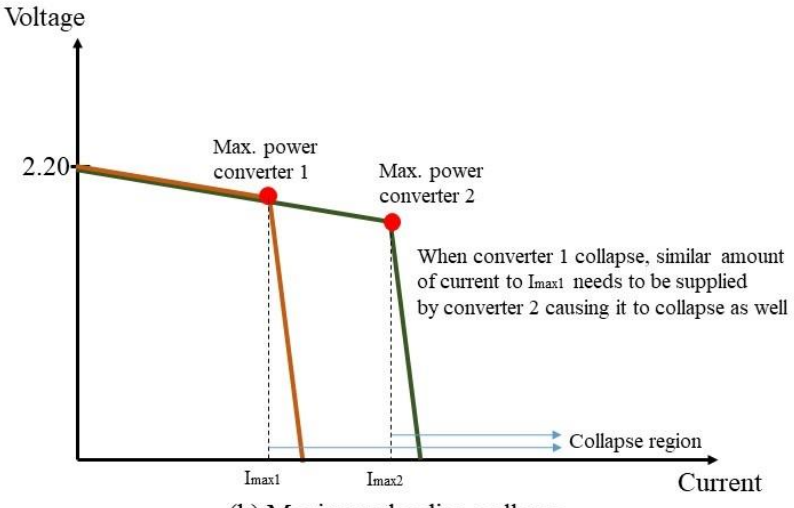
Figure 2.3: Difficulty in OR-ing configuration due to the output voltage mismatch.

It can be argued that in the OR-ing configuration, if the output of each parallel-connected converter is tuned to produce a similar level of voltage, all converters will be able to deliver current to the load at all times. However, this is very difficult to achieve and may even lead to the collapse of the system due to two main reasons. The first reason is the difficulty to achieve a perfectly equal output voltage for all converters with the presence of steady state error in the output voltage. This can be further explained in Figure 2.3. In Figure 2.3 (a), assuming both converter 1 and 2 are tuned to produce 2.2 V, and if converter 1 outputs 2.22 V and converter 2 outputs 2.18 V under no load condition due to their steady state error, only converter 1 will

be connected to the load. Converter 2 will be connected to the load if the voltage level in converter 1 drops to its actual output voltage; 2.18 V due to the internal droop in converter 1. However, if the power rating in converter 1 is low and could collapse before the output voltage reaches 2.18 V, then it would collapse first even before converter 2 is connected to the load, as shown in Figure 2.3 (b). The second reason is the different in power rating between parallel connected converters. This is further illustrated in Figure 2.4. In Figure 2.4 (a), assuming that two converters are connected in parallel and are able to output a perfectly equal output voltage and possess a similar amount of internal droop, if converter 1 has a lower power rating than converter 2, then as the magnitude of drawn current increases, it would collapse and the loading for converter 2 will tremendously increase due to sudden unavailability of converter 1. If the amount of drawn current exceed the power rating of converter 2, then converter 2 will also collapse, and the overall operation of the system will collapse.



(a) Perfectly equal loadlines for two converters



(b) Maximum loading collapse

Figure 2.4: Difficulty in OR-ing configuration due to the different power ratings.

To further improve on this energy harvesting issue, a rapid charge/discharge energy storage such as a supercapacitor that can capture intermittent power is integrated into the system to ensure that all power from the harvesters can be stored first before being transferred to the load, still via a direct parallel connection. In this configuration, typically each harvester has its own dedicated power converter and supercapacitor, and the voltage of the supercapacitor is used as the indication of its storage status and when the energy should be transferred to the load. By using this buffer storage system, the energy from all harvesters can be captured at the same time, thereby eliminating the problem associated with the direct OR-ing configuration. Furthermore, since the load is effectively disconnected from the harvester and power converter during the charging process, the power converter can be easily integrated with MPPT function, further increasing the efficiency of the energy extraction process. This method was utilised by Ambimax [30], which is probably the most cited published work in multiple multitype energy harvesting system. Ambimax was built from COTS components and is capable of harvesting energy from multiple energy harvesters at the same time by integrating a dedicated supercapacitor for each of the harvesters, and when the voltage of the supercapacitor reaches a pre-set threshold voltage, then the node from that supercapacitor is short circuited to the load, thus enabling the power transfer. Another example is Kang *et al.* [31] who have demonstrated a system with an almost similar mechanism, however in an integrated package. Their proposed system is shown in Figure 2.5. The same concept was also demonstrated by Srujana *et al.* [32] and Morais *et al.* [33]. Although the efficiency of energy extraction is increased by effectively harvesting every available energy, the system is incapable of delivering all of the harvested energy at the same time to the load, especially when the power demand from the load is higher than what each single harvester could produce.

Some other methods have also been proposed. Dini *et al.* [34] have proposed a multiple multitype energy harvesting system based on a priority based queuing. In this system, a similar approach of using dedicated supercapacitor and MPPT was used, however instead of using the voltage of the supercapacitor as the connection switching parameter, a set of priority based mechanisms are proposed to transfer the power to the load. The pre-set queue places the harvester with the highest expected power output on the highest priority and when the circuit detects that the supercapacitor associated with this harvester has low power level, the queue will move to the second prioritised harvester, and so on. On the other hand, Shi *et al.* [35] have proposed a timely slot queue mechanism, in which each harvester is allocated a specific time slot to transfer power to the load. In determining the slot queue selection process, the harvesters

with output voltage lower than a pre-set threshold voltage are disabled. Finally, a well-designed system with plug-and-play capability was proposed by Weddell *et al.* [36], utilising a multiplexing method to select the power to be delivered to the load. Their complex system consists of a microprocessor used to store electronics datasheet of each of the elements in the system, and works together with the multiplexer to consistently determine the energy available in each node and transfer this energy to the load depending on the demand from the load.

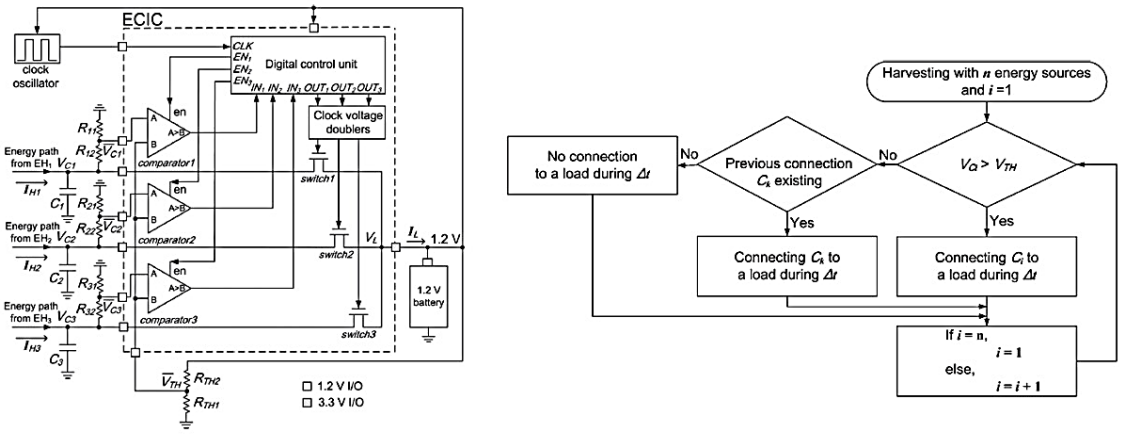


Figure 2.5: Proposed system by Kang *et al.* [31]. Left shows the circuitry architecture of the energy combiner system and the flowchart of the combiner operation is shown on the right.

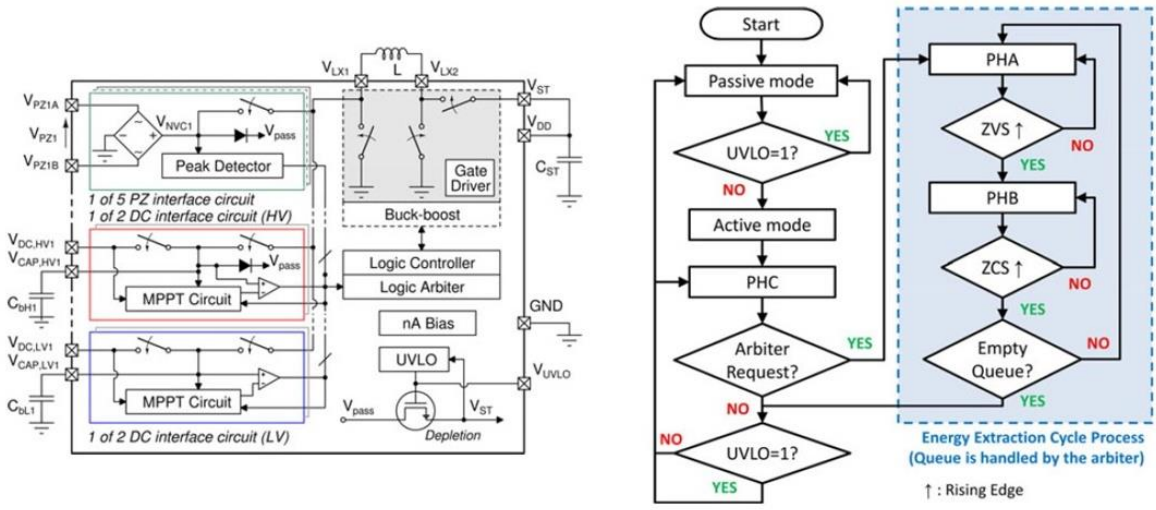


Figure 2.6: Multiple energy harvesting system utilising priority based queueing method proposed by Dini *et al.* [34] The system architecture is shown on the left and the operation flowchart is shown on the right.

In all of these reported systems, although the issue of harvesting every available energy simultaneously has been solved, none are capable of delivering power to the load directly and

simultaneously from all energy harvesters at any given time. This will become a major problem especially when the system is used to power up heavy load. In that sense, all of the reported work serve to improve the redundancy of the power by integrating them together to sustain the operation of the system, instead of integrating multiple harvesters to boost the power output capability. Apart from a few, most of the systems do not possess plug-and-play functionality for the harvesters. Furthermore, for systems that rely on a supercapacitor to store energy, between the period in which the supercapacitor is fully charged and the supercapacitor is connected to the load, the energy harvested during this period will not be extracted. It will be shown in the next section by using the method proposed in this work, all of these issues can be solved altogether concurrently.

2.2.2 Voltage Droop Current Sharing Mechanism

The proposed pico-grid system would comprise multiple energy harvesters, each equipped with a dedicated power converter to regulate the output voltage of the harvesters to meet the input requirements of the DC bus. The purpose of integrating multiple sources in this system is to improve redundancy, reliability, and loading capacity of the output power. Improvement in redundancy and reliability is achieved when a continuous supply of power to the load can be sustained via the introduction of multitype harvesters, which has been accomplished via multiple methods that have been reported in the literature presented in the previous section. On the other hand, improvements in loading capacity involves combining and transferring harvested power to the load altogether simultaneously, which has not been reported elsewhere. To achieve both of these objectives, a method capable of delivering power simultaneously to the load; voltage droop is explored. Voltage droop is defined as an intentional voltage drop of the output of a power converter when its output current is increased. As will be shown later, the introduction of this ‘virtual impedance’ at the output of a power converter not only would enable multiple power converters connected in parallel to simultaneously deliver power to the load, but can also be utilised to set each converter to share the same magnitude of current in terms of its generation capacity, or per unit (P.U).

When power converters are connected in parallel, there should be a cross regulation between them to enable current sharing. The concept of paralleling multiple power converters has been discussed in great details in publications, such as by Huang *et al.* [37]. In high power systems, this can be achieved through master-slave configuration, in which one master power converter is set to be operated in voltage controlled mode and the other power converters are set to be

operated in current source mode. In this configuration, the voltage is effectively determined by the master controller. Furthermore, in a few cases, the communication link between the controllers of these converters is required, further complicates the overall system architecture. However, in a low power system, this method is not feasible since the configuration consumes a significant amount of power. In this case, a simpler control mechanism is required.

Generally, a DC-DC power converter is designed to output a constant voltage regardless of the output current. However, the presence of parasitic resistance between the output node of the converter and the input node of the load causes the drop of this voltage as seen by the input node. The higher the current drawn from the converter, the higher this voltage drop would be. The idea of voltage droop was derived from this phenomenon, in which an intentional voltage drop can be integrated in the output of the power converter by the introduction of virtual impedance, to shape the V-I loadline of the power converter, as shown in Figure 2.7 (a). This virtual impedance can be integrated in the control loop of the power converter, as will be shown in the latter section. The original loadline of a typical DC-DC converter is shown as a blue line. The voltage collapse region marked as a red dot indicates the collapse of the converter operation when the drawn current exceeds its output power capability. By integrating a virtual impedance, this loadline can be shaped to the steeper green line, enabling higher current to be drawn at lower voltages (same amount of output power).

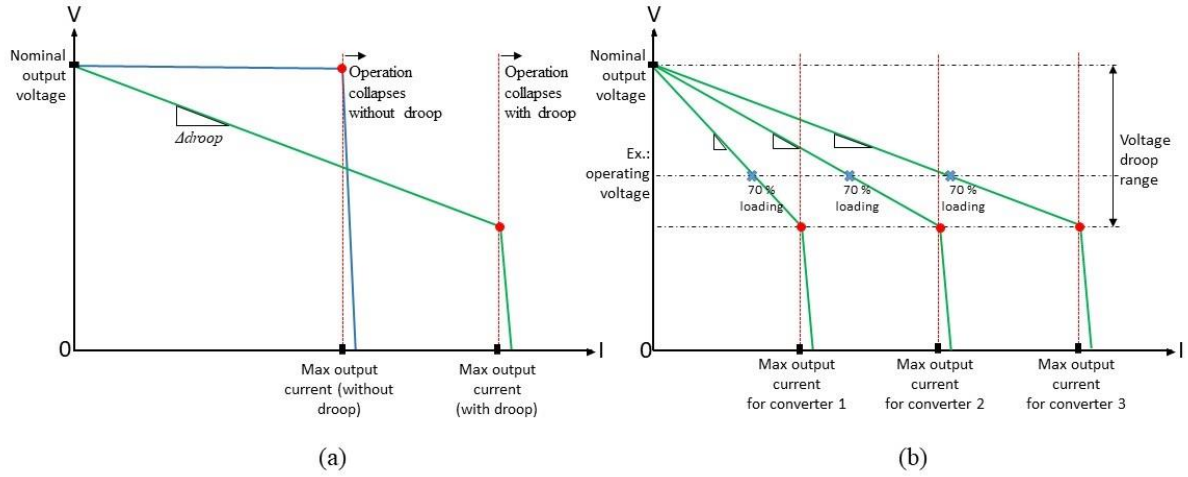


Figure 2.7: (a) shows the typical loadline of DC-DC converter (in blue) and the modified loadline with droop (in green). (b) shows the connection of three power converters with different rated power connected in parallel.

If the maximum expected output powers for multiple converters are known, then each converter can be designed to have the same nominal output voltage at no load and at maximum load

conditions, as shown in Figure 2.7 (b). When these converters are connected in parallel, each converter can supply current simultaneously to the load. Furthermore, current sharing in terms of their generation capacity is automatically achieved. For example, if the power demand from the connected load causing the operating voltage to droop as shown in Figure 2.7 (b), then each converter will supply a different magnitude of current according to their loadline characteristic, however their percentage of the loading is equal (70 % or 0.7 P.U in this case).

2.2.3 P.U Equal Load Sharing and Simulation

In order to demonstrate an equal load sharing mechanism achieved via the voltage droop method, a case study and full simulation is presented in this section. In the simulation presented, three energy sources; source 1 with 1 V 0.1 W output, source 2 with 0.8 V 0.5 W output, and source 3 with 3 V 0.25 W output are connected to a common bus, each via a dedicated power converter. For simplicity, it was assumed that the energy sources produce a consistent voltage and are capable of generating maximum power during the whole period of simulation. The load comprises a 70 Ω resistor, 1 µF capacitor, and a 40 mA constant current sink, all connected in parallel. The nominal voltage of the bus was set at 2.0 V for 50 % loading of the system. The droop voltage range of 0.4 V was set from 2.2 V (0 % loading) to 1.8 V (90 % loading).

To determine the magnitude of the droop for each converter, the maximum output current of each power converter, $I_{max\ loading}$ was determined according to the following relation:

$$I_{(\text{max.loading},\ \ 90\%\ \text{loading})} = \frac{0.9 \times \eta_{\text{converter}} \times P_{\text{harvester}}}{V_{(\text{max.loading},\ \ 90\%\ \text{loading})}}$$

Here $\eta_{converter}$ is the efficiency of the power converter at maximum loading, $P_{harvester}$ is the maximum output power of the energy harvester, and $V_{max\ loading}$ is the set output voltage of the power converter at 90 % loading (1.8 V for this case). The efficiency of each converter was assumed to be 90 % for the buck converter and 85 % for the boost converter. The value of 0.9 represents the set maximum loading of the converter in P.U in order to prevent the converter from approaching its full loading, which could possibly collapse the operation of the power converter. From this, the magnitude of the required voltage droop, Δdroop was determined from the following relation:

$$\Delta\text{Droop} = \frac{V_{(\text{no load},\ \ 0\%\ \text{loading})} - V_{(\text{max.loading},\ \ 90\%\ \text{loading})}}{I_{(\text{max.loading},\ \ 90\%\ \text{loading})}}$$

Here $V_{no\ load}$ represents the output voltage of the power converter at no load (open circuit) condition (2.2 V). From this, the droop regulation and subsequent V-I output loadline of each converter was determined and the results are shown in Figure 2.8. As can be observed from the figure, power converter 1 which outputs regulated voltage from energy source 1 possesses the highest droop due to its lowest power capability, and vice versa. The loadlines for all converters in P.U are shown in the inset figure. The loadlines in P.U are regulated to output the same P.U output current at a specific bus voltage, indicating that all converters share the loading equally between them.

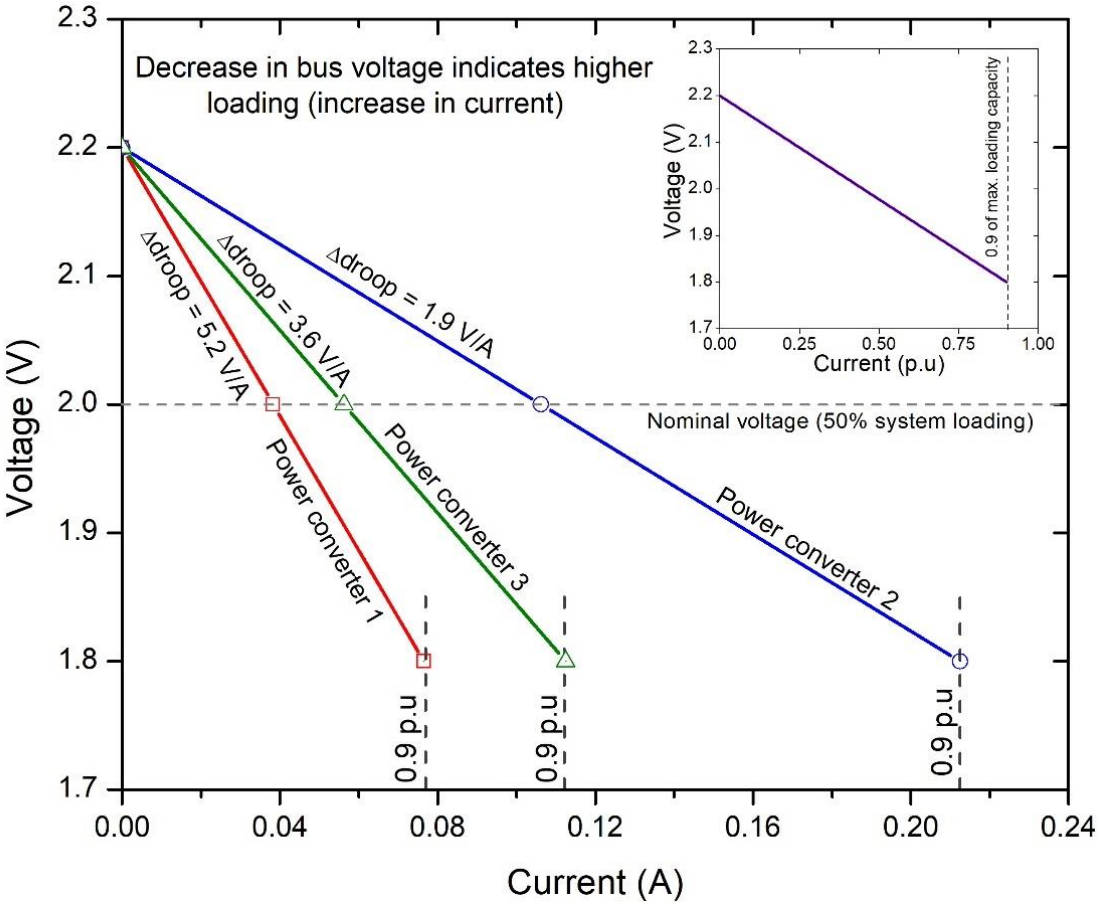


Figure 2.8: V-I loadlines of all power converters and their respective voltage droop. The inset figure shows the loadlines of all power converters in P.U. The loadlines shown here represent the steady state value of the power converter.

The simulation layout in Simulink is shown in Figure 2.9. The simulation was run for 5 seconds and the readings for the output current for all sources, bus voltage, and load current were recorded and are shown in Figure 2.10.

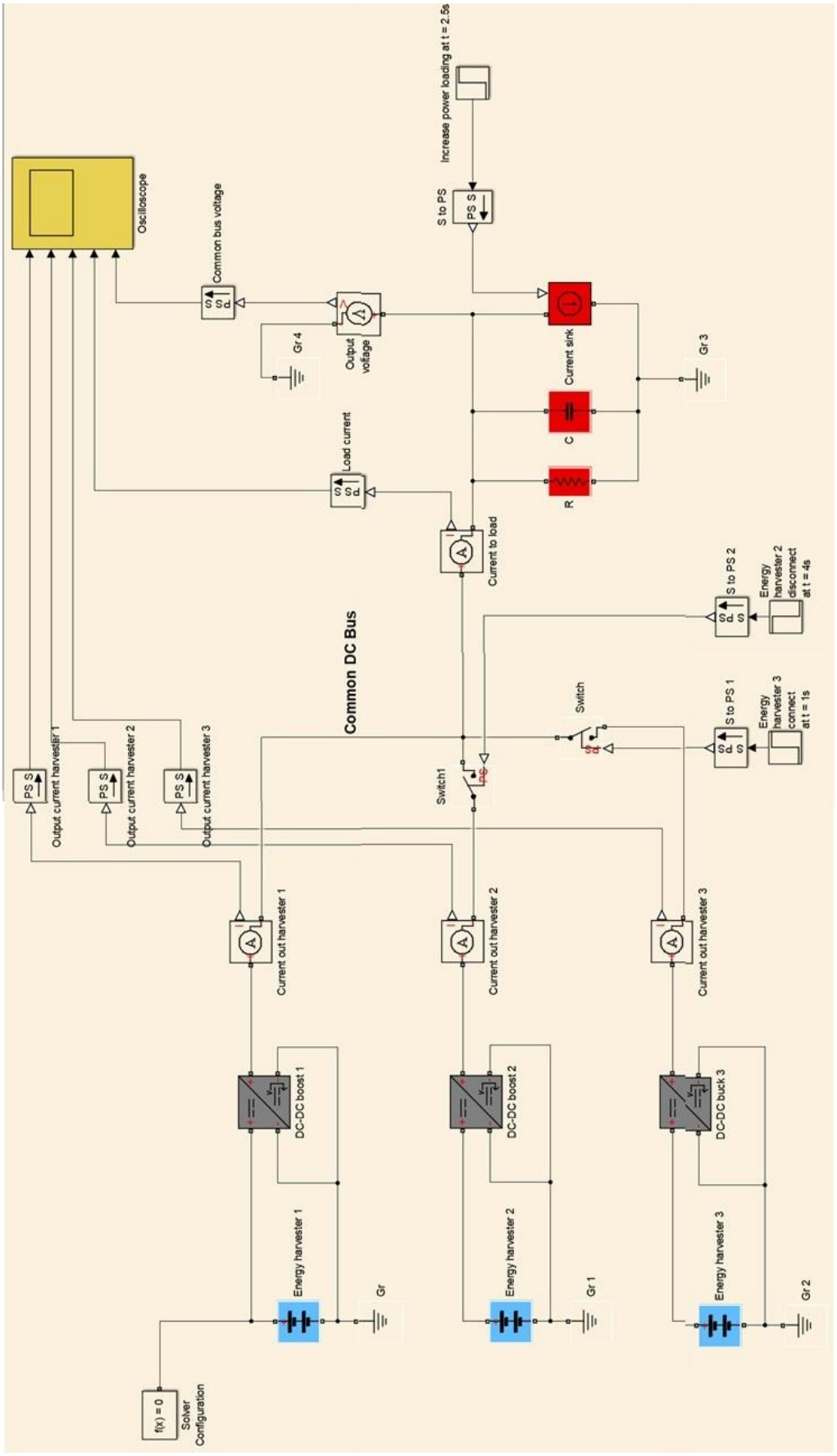


Figure 2.9: Simulation layout in Matlab Simulink.

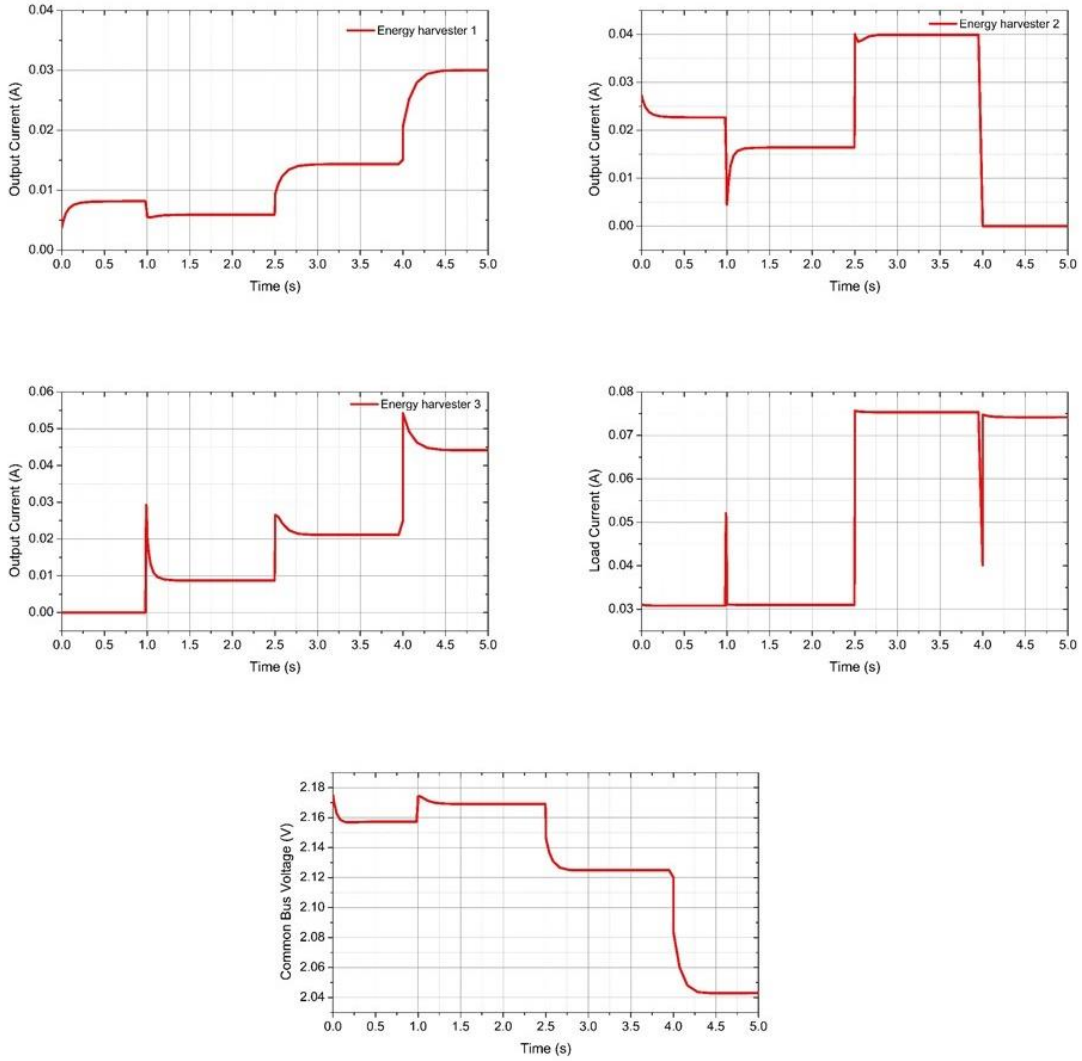


Figure 2.10: Results from the simulation.

The chronology of the simulation and results are discussed as follows:

1) At t = 0, power converter 1 (for energy source 1) and power converter 2 (for energy source 2) are both connected to the load of 70 Ω resistor and 1 µF connected in parallel. Power converter 3 (for energy source 3) and 40 mA constant current sink are not connected in the system. It can be observed from the waveforms that both power converter 1 and power converter 2 deliver an output current simultaneously to the load. It can be determined from the bus voltage (2.16 V) that the loading of the system is less than 50 %. The output current from both converters are consistent with the designed loadlines as shown in Figure 2.8 before.
2) At t = 1, power converter 3 is connected, increasing the available power of the system. As a result, the bus voltage rises indicating that the loading of the system is reduced, and both

output current from power converter 1 and power converter 2 decrease as the load is now shared with power converter 3.

3) At t = 2.5, 40 mA constant current sink is connected, increasing the load in the system. All power converters respond to this sudden change in load by increasing their output current, and the bus voltage drops due to the higher loading.
4) At t = 4, power converter 2 is disconnected, decreasing the available power in the system. As a result, the load is now shared between power converter 1 and power converter 3. The output current from both of these converters increase to balance out the absence of output current from power converter 2. The bus voltage decreases due to the higher loading in the system. In these simulations, it was observed that the steady state values of the converters agree with the designed loadlines.

This simple simulation shows that the operation of parallel power converters can be easily regulated via the introduction of this voltage droop mechanism. The observations and conclusion drawn from this simulation include:

1) Voltage droop enables all connected power converters to simultaneously deliver current, hence power to the load. This means that the system could be used to power up heavy load that could not be powered by a single energy harvester, hence increasing the loading capability of the energy harvesting system.
2) The system is capable in reliably responding to the connection and disconnection of any power converters and loads, and provided the generation capacity is higher than the power demand from the load, the system will not collapse. The response time is determined by the time constant of each converter connected to the system. This means that in the actual system, the plug-and-play feature is easily achievable.
3) Apart from a pre-set design value, there is no communication between power converters to regulate the sharing mechanism, hence there is no need to establish a communication link for the converters. The bus voltage is used by all converters as the main regulation parameter.
4) Load burden is shared equally by all connected power converter in terms of their generation capacity.
5) The bus voltage can be used to determine the loading in the system, hence more features such as load shedding can be integrated based on the magnitude of the bus voltage.

In the next section, the implementation of this voltage droop mechanism in actual control circuitry of the power converter is investigated. Furthermore, as energy harvesters possess

time-varying output power, the droop needs to be regularly tuned to match this variation and the solution for this issue will be presented.

2.3 Droop Demonstration

In this section, the implementation of voltage droop mechanism in presented. Although the general concept has been outlined in the previous section, the implementation aspect in actual circuits has neither been presented nor discussed yet. Moreover, the droop magnitude presented in the previous section is fixed and static, however since the amount of output power from the energy harvester will vary over time, the magnitude of the droop needs to be able to follow this variation. The method to achieve this droop variation with rated power for the energy harvester proposed here has not been reported elsewhere and is the main contribution from this chapter. This section investigates the implementation and presents the results of this variable droop mechanism in the feedback circuitry of a power converter.

2.3.1 I-V Characterisation for Harvesters

The first step to demonstrate the droop mechanism is to investigate the characteristics and performance of energy harvesters/transducers that will be used in the system. In this aspect, two types of harvester are proposed; solar panel and thermoelectric generator (TEG). Each of these harvesters was put under controlled environment conditions and the magnitude of harvested power that will be fed to the system is determined.

a. Solar Panel

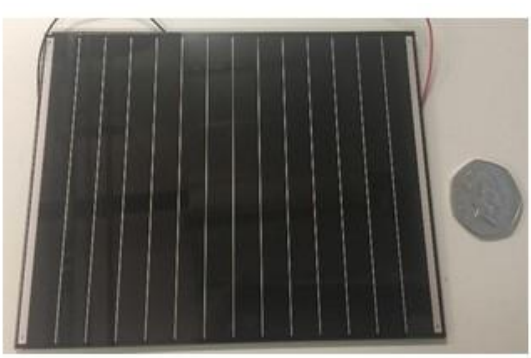
The characteristics and equivalent circuit models of solar panel have been proposed, presented, and discussed in great details in the literature. Under any illumination, a typical solar panel possesses a standard and recognisable shape of current voltage (I-V) and power voltage (P-V) characteristics. Additionally, since solar panel possesses parasitic series and shunt resistance, there is a point in the P-V curve where the solar panel outputs the maximum available power to the load. This point is commonly known as maximum power point (MPP). This point typically occurs when the output voltage of the solar panel is at 80 % of its open circuit voltage (V_{OC}). Most power converters are equipped with MPP tracking (MPPT) functionality designed to adjust the input impedance to ensure that the solar panel is always operating in the region around this MPP voltage (V_{MPP}).

The solar panel used in this thesis is an amorphous silicon (a-Si) AM-7E04CAR manufactured by Sanyo as shown in Figure 2.11 (a). In order to obtain the I-V characteristic of this panel, it

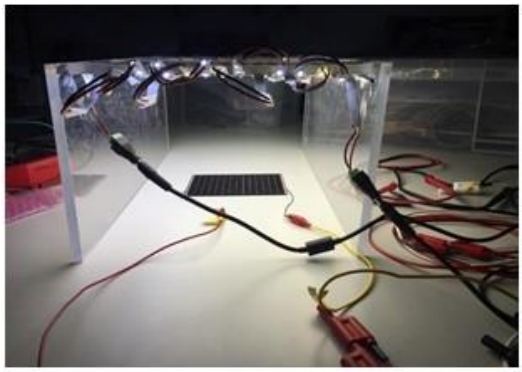
was put under four different illuminations as described in Table 2.1 and the I-V curve was extracted for each illumination by drawing a set current from the panel by using Keithley Sourcemeter 2604B as shown in Figure 2.11 (b). Figure 2.11 (c) shows the extracted I-V and calculated P-V curves of the solar panel under these different illuminations. Figure 2.11 (d) presents the plot of output voltage of the panel when the MPP occurs (V_{MPP}) against open circuit voltage (V_{OC}). All the relevant results are tabulated in Table 2.2.

Table 2.1: Illumination level

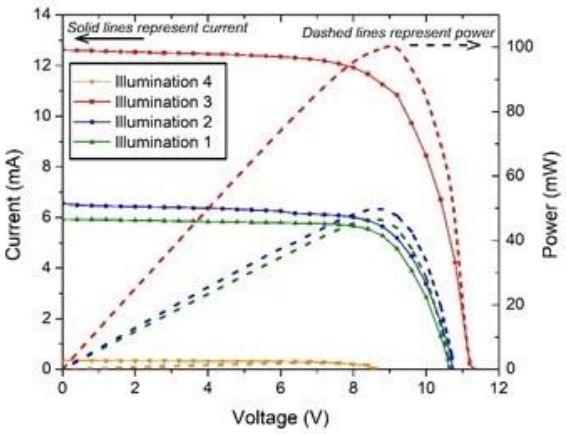
Illumination	LED	Lux (lx)
Illumination 1	White (cool white)	500
Illumination 2	Yellow (warm white)	600
Illumination 3	Both white and yellow	1100
Illumination 4	Typical fluorescent indoor light	120



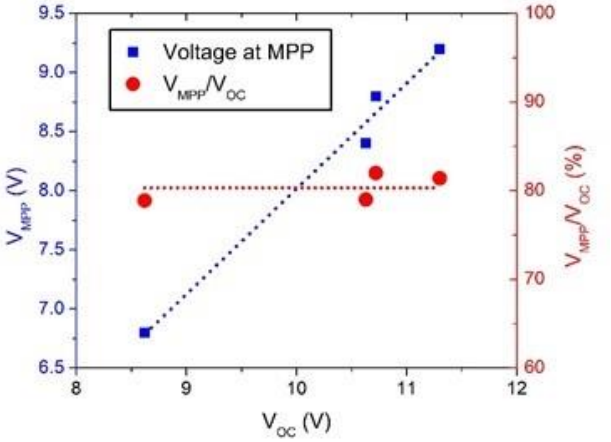
(a) AM-7E04CAR



(b) Experiment setup



(c) I-V and P-V characteristics



(d) V_{MPP} vs. V_{OC}

Figure 2.11: Experimental setup and characterisation results from the solar panel.

From the I-V curve, it can be observed that the short circuit current (I_{SC}), V_{OC}, and extracted MPP vary strongly with illumination. The highest MPP of 100 mW was extracted when the solar panel was illuminated through a combination of warm and cool LEDs. Under a typical indoor fluorescent light illumination, 2 mW of MPP was able to be extracted. Finally, from the V_{MPP}/V_{OC} ratio, it can be observed that the MPP occurs at approximately 80 % of V_{OC}, which agrees with the expected behaviour of any typical solar panel.

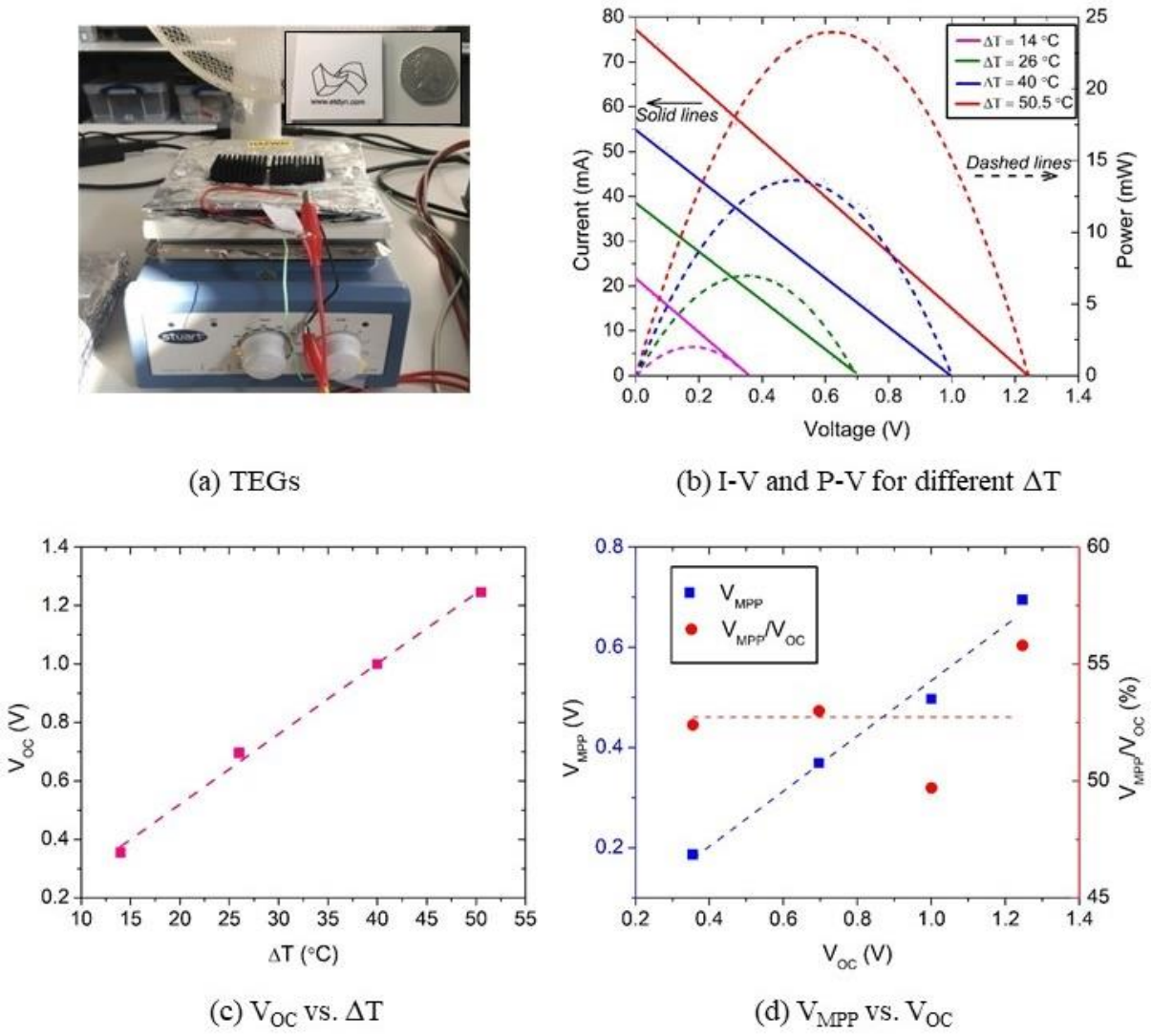
Table 2.2: Parameters for the solar panel for all illuminations

Illumination	V_{OC} (V)	I_{SC} (mA)	V_{MPP} (V)	MPP (mW)
4	8.62	0.35	6.8	2.04
3	11.30	12.62	9.2	99.09
2	10.72	6.55	8.8	49.72
1	10.63	5.93	8.4	46.62

b. Thermoelectric Generator (TEG)

The TEG is able to convert the difference in temperature, ΔT between its two exposed surfaces to a useful electrical voltage (Seebeck effect), which can be used to power up an external low power load. Generally, its equivalent circuit is simply a voltage source in series with an internal resistance. The magnitude of the output voltage varies linearly with the temperature difference. When the current flows through the TEG (when connected to the load), a reversible effect known as the Peltier effect can be observed; the applied voltage across the TEG created the temperature difference between its two surfaces. This causes the temperature of the hot side surface of the TEG to drop and vice versa, reducing the output voltage from the Seebeck effect and hence the output power of the TEG. Due to this unavoidable phenomenon, it is extremely important to maintain ΔT between the two exposed surfaces in TEG to ensure a stable output power.

The TEG used in this thesis is Seebeck Effect Module GM250-241-10-12 manufactured by European Thermodynamics. Since the TEG possesses a very low output voltage, two similar TEGs exposed to the same temperature on each side are connected in series to boost the total output voltage. Insulating foam was placed in between the hot side and cold side. The surface of the hot side is directly exposed but heatsinks (PGA, 9.8 K/W, 36 x 36 x 12.3 mm) were attached to the surface of the cold side using a thermal interface (polyamide, 0.37 W/mK 0.127 mm) to provide a better heat dissipation. The constructed TEGs system is shown in Figure 2.12 (a). The small inset picture in the same figure shows the TEG module used in the system.



(a) TEGs (b) I-V and P-V for different ΔT

(c) V_{OC} vs. ΔT (d) V_{MPP} vs. V_{OC}

Figure 2.12: Pictures showing the TEG harvester and experiment setup together with the characterisation results.

To extract the I-V characteristics under a different ΔT, a setup with a hotplate (Stuart UC152) and a digital thermometer (Omega HH501BJK) with a K type thermocouple were used. The hot side was placed directly on a hotplate and the heatsinks on the cold side were exposed to air with a fan facing towards it to assist the heat dissipation process. The hotplate temperature was controlled to heat up the hot side of the TEGs. In order to accurately monitor the surface temperature, K type thermocouples were placed on both sides. The temperature of the hotplate was varied and the ΔT and respective I-V characteristic were extracted by sinking the current to Keithley Sourcemeter 2604B. The setup was left for 30 minutes between each measurement to ensure that the temperature was stabilised for both sides. The experimental setup is shown in Figure 2.12 (a). Figure 2.12 (b) shows the extracted I-V characteristics for multiple ΔT. At ΔT = 50.5 °C, a maximum power of 24.5 mW was extracted from the TEGs. At ΔT = 14 °C

which is the typical ΔT expected when the hot side is equal to the body temperature (≈ 36 °C) and the cold side is equal to the room temperature (≈ 22 °C), maximum power of approximately 2 mW was extracted. It can be observed that the I-V curves have a strong dependency on ΔT. Figure 2.12 (c) shows this dependency by plotting V_{OC} against ΔT. This plot reveals a strong agreement with the expected linear characteristics between these two parameters. Since TEG has a parasitic series resistance, similar to a solar panel, there will be a point where MPP will occur. Figure 2.12 (d) shows the plot of V_{MPP} vs. V_{OC} for the TEGs used in this thesis. From this, it can be concluded that the V_{MPP} occurs at approximately 50 % of V_{OC}. These findings agree with the typical characteristic of TEG as reported in the literature. All results are tabulated in Table 2.3.

Table 2.3: Extracted parameters for the TEGs under different temperature differences, ΔT.

ΔT (°C)	Hot side temp. (°C)	Cold side temp. (°C)	V_{OC} (V)	I_{SC} (mA)	V_{MPP} (V)	MPP (mW)
14.0	39.6	25.6	0.36	22	0.19	2.05
26.0	56.3	30.3	0.69	37	0.37	7.01
40.0	74.0	34.0	1.00	56	0.49	13.92
50.5	87.5	37.0	1.25	78	0.69	24.33

2.3.2 Calculating Required Droop from Converter V-I Loadline

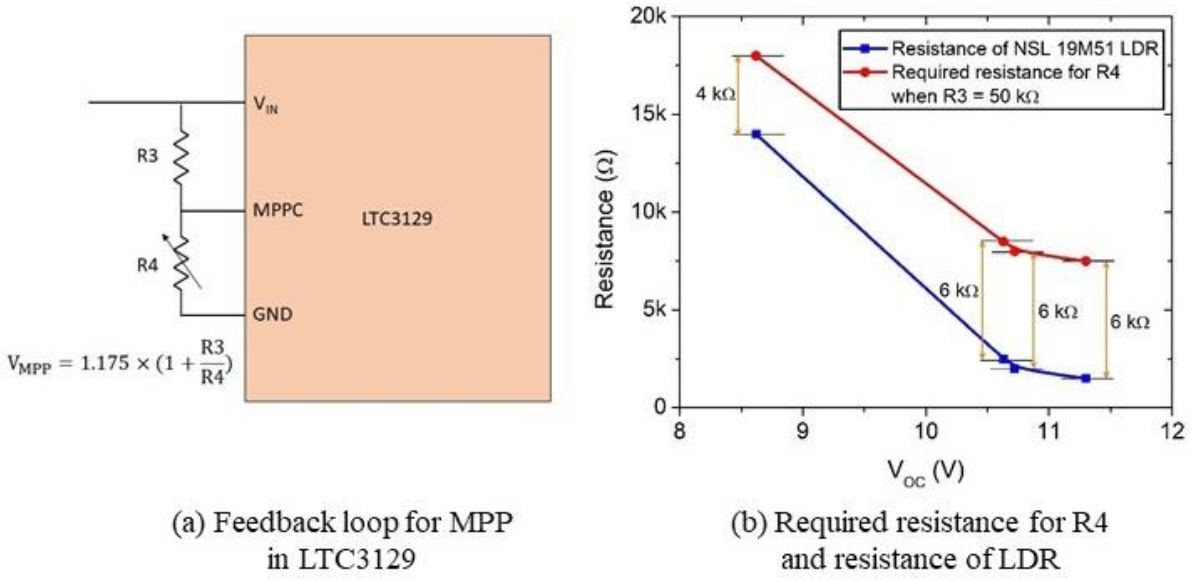
After the expected range for input voltage and power from the harvesters have been obtained, the interface circuitry can be designed to output the regulated voltage with a droop mechanism. In this thesis, COTS DC-DC converter integrated circuits (IC) suitable for the input and output specifications for both harvesters are used. As will be shown later, a simple addition to these ICs enable simple yet accurate droop mechanism to be seamlessly integrated. Unless otherwise stated, only steady state conditions/values are used in all analyses in the following sections. In order to determine the output voltage of the required power converters and subsequently to calculate the magnitude of the required droop, the droop parameters are presented in Table 2.4.

Table 2.4: Parameters for droop voltage and full load.

Parameter	**Magnitude**
No load output voltage (0 mA)	2.2 V
Full load output voltage	1.8 V
Percentage of full load from rated power	90 %

a. LTC-3129 for Solar Panel

The output voltage for the solar panel used is relatively high (> 8 V). Due to this, a buck converter is necessary to step down the DC voltage to the required 2.2 V. For this purpose, a synchronous buck-boost DC-DC converter IC LTC-3129 manufactured by Linear Technology was selected. This input voltage range for this IC is within the expected output voltage range of the solar panel (1.92 to 15 V) and the quiescent current of the IC is typically around 1.3 µA. Since the magnitude of the down conversion of the voltage is low, the duty cycle of the converter would be placed to the extreme low edge, which could degrade the power conversion efficiency (PCE) and introduce significant noise in the system. To counter this issue, this IC comes with a burst mode, in which the PWM will automatically skip its switching cycle if the output voltage is still within a tolerable pre-set value. Furthermore, this IC has a feedback loop in the input side to programme the V_{MPP} to ensure MPP can be extracted from the solar panel. This MPP programmed function ensures that the voltage of the solar panel is always kept above a pre-set V_{MPP}, regardless of the loading condition. Since the programmed voltage is fixed depending on the resistor network divider ratio in the input feedback loop, a resistor with its resistance varies with the illumination in the same magnitude as the variation of the solar panel V_{OC} with illumination is needed. This will ensure that the programmed V_{MPP} follows the variation of V_{OC} of the solar panel for any illumination level. To achieve this, a LDR whose resistance decreases with illumination is used.



(a) Feedback loop for MPP in LTC3129

(b) Required resistance for R4 and resistance of LDR

Figure 2.13: The programmed MPP function and the resistance of the LDR compared with the required resistance to ensure a reliable MPP functionality.

Figure 2.13 shows the variation of resistance value needed on the bottom side of the resistor network and subsequently the variation of resistance of NSL 19M51 LDR manufactured by Advanced Photonix, both against the V_{OC} of the solar cell which corresponds to the different level of illumination. It is shown that by connecting this LDR in series with a 6 kΩ resistor, an almost similar illumination response with the solar cell was obtained and hence this can be used in the MPP feedback loop. However, as will be discussed next, the significantly low total resistance in this loop (< 70 kΩ) would cause a significant amount of current to flow in this loop especially when the voltage of the solar panel is high, and this can degrade the efficiency of the system. Figure 2.14 shows the circuit layout for the converter.

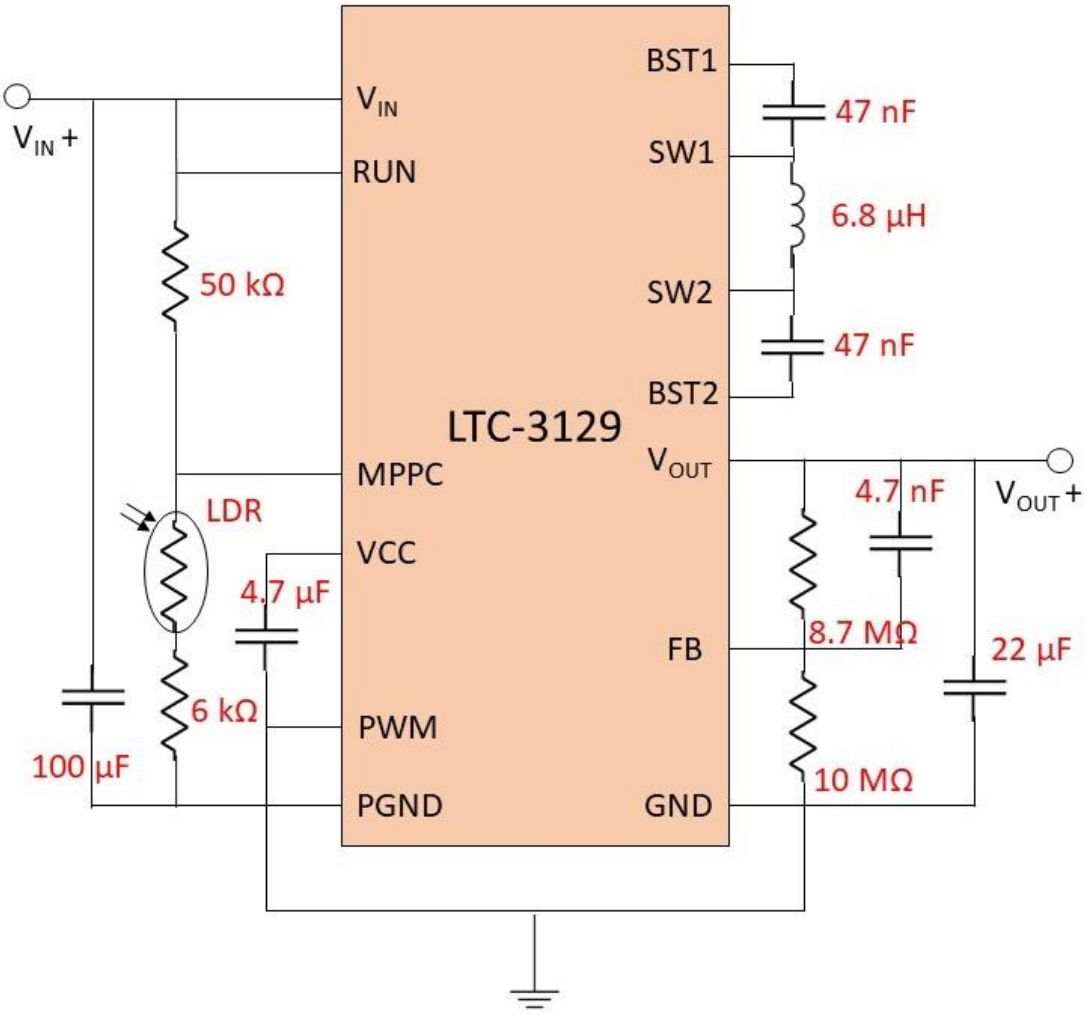
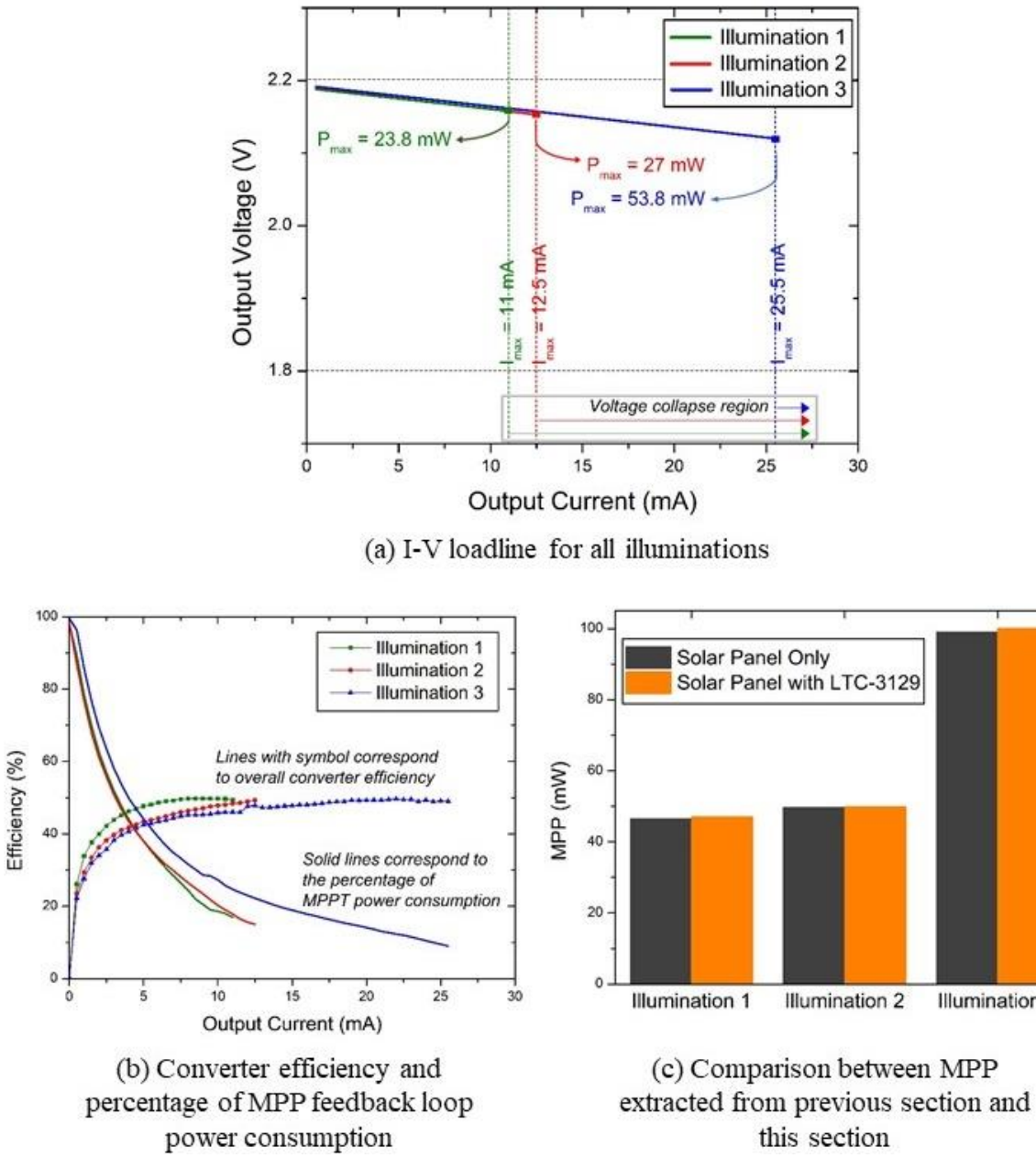


Figure 2.14: LTC-3129 circuit configuration for solar panel used in this thesis.

The constructed circuit was then tested under three different illuminations as presented in the previous section. The output of the converter was connected to Keithley Sourcemeter 2604B to sink set current and subsequently the output voltage was recorded. The sink current was slowly increased until the converter could no longer regulate the output voltage, signifying an

overloaded condition and the collapse of the operation. The V-I loadline was plotted to determine the internal droop of the converter due to the parasitic resistance. At the same time, the input voltage and current were also recorded. This enables an accurate determination of the overall efficiency of the converter. The results are shown in Figure 2.15.



(a) I-V loadline for all illuminations

(b) Converter efficiency and percentage of MPP feedback loop power consumption

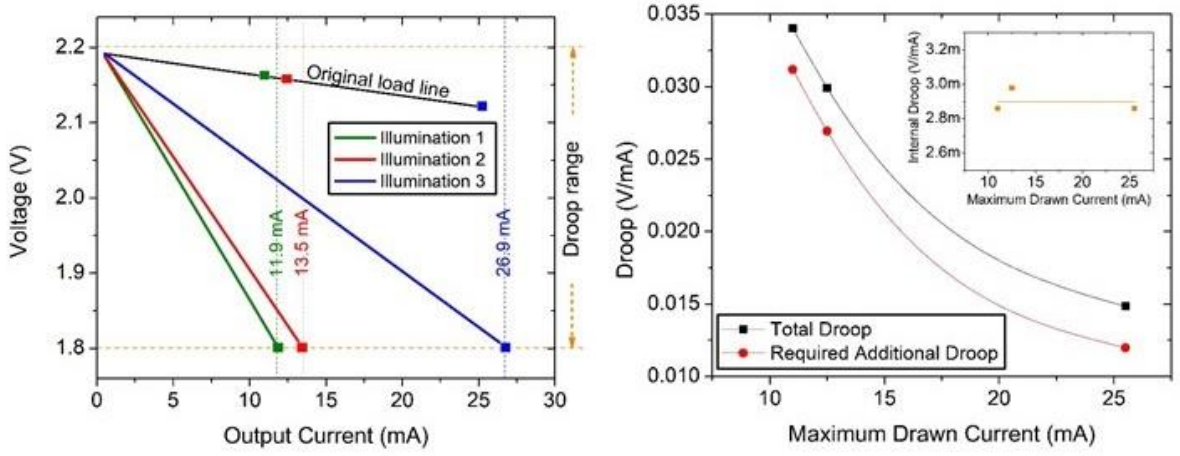
(c) Comparison between MPP extracted from previous section and this section

Figure 2.15: Results from the constructed circuit.

As shown in Figure 2.15 (a), the loadline for the converter possesses a linear characteristic, signifying the effect of internal series resistance in the output side of the converter. This resistance of 2.9 Ω can be determined from the slope of the loadline. It should be noted that this high value of resistance also includes the resistance of the cable connecting the setup to

the sourcemeter, which is around 1.5 Ω. From the input and output power determined from the recorded current and voltage on both the input and output sides, the efficiency for each of the illuminations was calculated and shown as the lines with symbols in Figure 2.15 (b). The peak efficiency was around 50 % for all illuminations and is significantly lower than the expected efficiency as stated in the datasheet (≈ 65 %). The main reason is the significant amount of current flowing into the MPP feedback loop due to the low total resistance in this leg. The ratio of power flowing into this loop per input power was calculated and it is shown in the same figure as the solid lines. It can be observed that minimum reduction of 10 % in the overall efficiency was contributed from the feedback loop. Aside from that, the dynamic power consumption and parasitic resistance losses also cause further reduction on the overall efficiency.

Another observation is the dependency of the maximum current hence power with the illumination level. The relationship between maximum power and illumination agrees with the previous I-V characterisations of the solar panel. Figure 2.15 (c) shows a comparison between extracted MPP from the solar panel in this section and previous section. The almost similar magnitude of MPP in all illuminations validates the functionality of the LDR based MPPT.



(a) Original loadline and new calculated loadlines for all illuminations

(b) Calculated droop and required additional droop against current to meet design requirements

Figure 2.16: Droop calculations.

Since the maximum available power from the converter varies with illumination, the droop required for each illumination is also different in magnitude to ensure reliable equal load sharing in the final system. Similarly, as before, the total droop required for each illumination is calculated as follows:

$$\Delta\text{Droop}_{\text{total}} = \frac{V_{(\text{no load, } 0\% \text{ loading})} - V_{(\text{max.loading, } 90\% \text{ loading})}}{0.9 \times \frac{P_{(\text{max})}}{V_{(\text{max. loading, } 90\% \text{ loading})}}} = \frac{2.2 - 1.8}{0.9 \times \frac{P_{\text{max}}}{1.8}} = \frac{0.8}{P_{\text{max}}} \quad \ldots \text{ eq. (2.1)}$$

Figure 2.16 (a) illustrates the desired new loadlines based on the calculated droops. It can be observed from the equation that since P_{max} is a function of illumination, therefore the droop value is also a function of illumination. From the calculated total droops, the required additional droops needed to be introduced in the system can be determined:

$$\Delta\text{Droop}_{\text{required}} = \Delta\text{Droop}_{\text{total}} - \Delta\text{Droop}_{\text{internal}} \ldots \text{eq. (2.2)}$$

Here, the internal droop is the droop as a result from the internal resistance of the converter. From this, the additional required droops were calculated and shown in Figure 2.16 (b). The design of the circuit to introduce these droops which vary with illumination level will be presented in the next section.

b. LTC-3105 for TEG

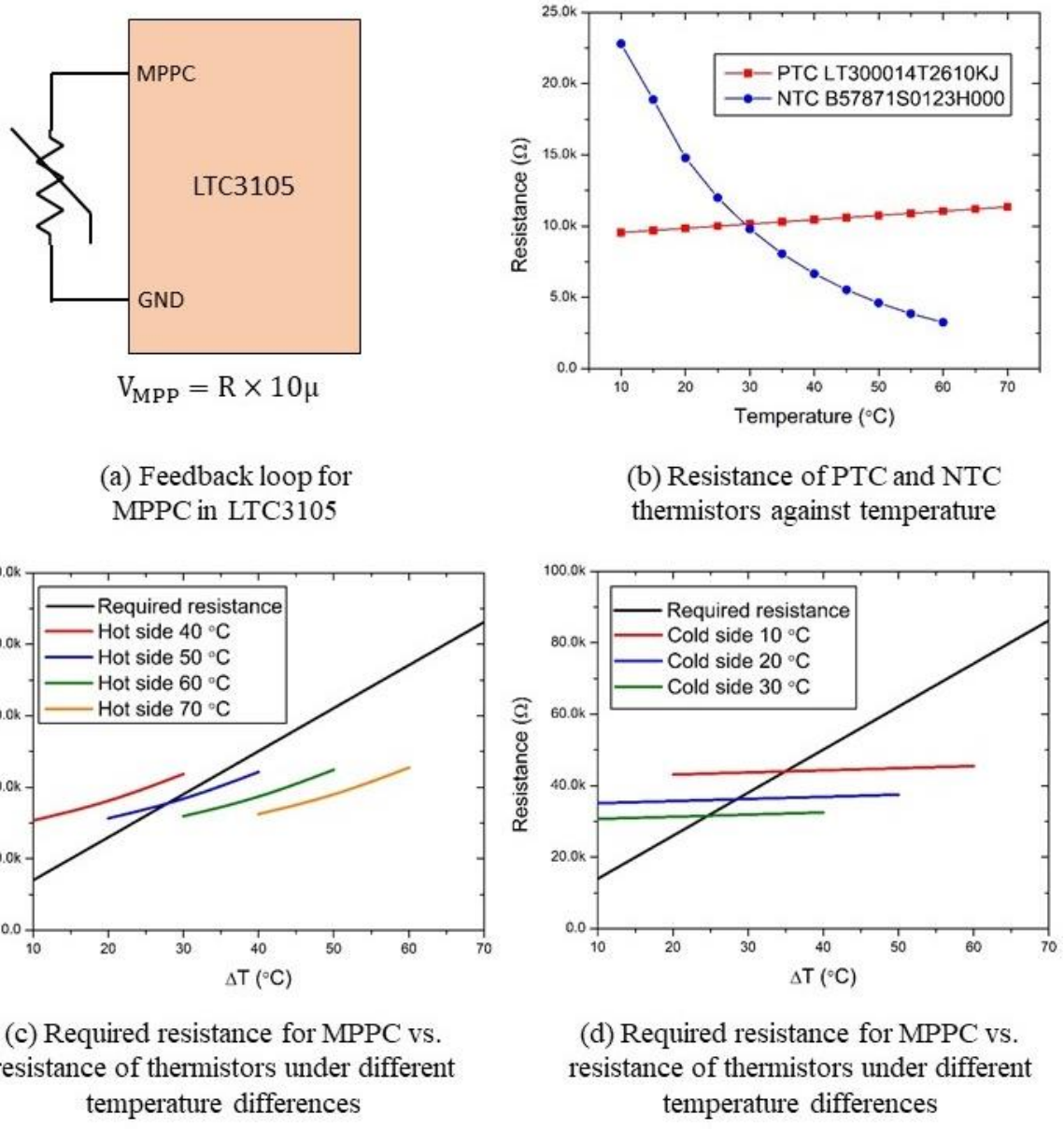
The output voltage for the TEGs harvesting system is low (1 V) and the voltage is expected to always be lower than the required output voltage of the converter (2.2 V). For this reason, a low voltage step-up converter is required and for this purpose, an IC manufactured by Linear Technology LTC-3105 specifically designed to harvest energy from a low input voltage high impedance source is selected. This IC has a minimum start-up voltage of 250 mV and is capable of stepping up the voltage to 5.25 V, configurable by the feedback loop configuration. This IC typically consumes as low as 24 µA of quiescent current during full operation to provide better efficiency. Furthermore, as before, this IC also has a programmable V_{MPP} function to programme the output voltage of the TEGs in the region of around 50 % of its V_{OC} to ensure maximum power extraction. However, this maximum power point controller (MPPC) function depends solely on the value of resistance in its loop without any direct feedback from the input side. In case of static resistance value, the V_{MPP} is set at a fixed value regardless of the temperature difference, hence TEGs V_{OC} variation. To counter this issue, a resistor whose resistance varies with temperature, thermistor is used. Figure 2.17 (a) shows the MPPC configuration of this IC. Since the magnitude of the temperature difference depends on the temperature of two different surfaces, a minimum of two thermistors are needed, one for each surface. The thermistor on the hot side should have a positive temperature coefficient (PTC) and the thermistor on the cold side should have a negative temperature coefficient (NTC) to ensure the weightage for both sides is considered in determining the temperature difference. Figure 2.17 (b) shows the resistance of a PTC thermistor LT300014T2610KJ and an NTC

thermistor B57871S0123H000 against the operating temperature. The expected ranges of temperature for the hot side and both sides in the final system are 40 – 70 °C and 10 – 30 °C, respectively. Assuming the temperature of the PTC thermistor is equal to the temperature of the hot side and vice versa, and by fixing the hot side temperature within the expected range in 10 °C intervals, the total resistance of both NTC and two PTC thermistors connected in series was determined and is shown in Figure 2.17 (c). The required programmed resistance value based on the formula given in Figure 2.17 (a) is also shown as the thick black line in the same figure. As can be seen, the blue line corresponds to the hot side temperature of 50 °C yields the closest value to the required resistance value. Deviations from the required resistance value can be observed for other temperatures, however based on the availability of an NTC and PTC thermistor available in the market, this combination of thermistors produces the closest value to the required resistance. Similarly, by fixing the temperature of the cold side, the comparison was drawn between the resistance of the thermistors and the required resistance value and is shown in Figure 2.17 (d). Similar to before, small deviations from the required value can be observed at around $\Delta T = 30$ °C, however, significant deviations can be observed whilst moving away from this value. The final circuit is shown in Figure 2.18.

The circuit was then tested under four different ΔT and the output of the converter was connected to Keithley Sourcemeter 2604B to sink set current and subsequently the output voltage was recorded. Similar to before, the sink current was slowly increased until the converter could no longer regulate the output voltage, signifying the collapse of the operation. The V-I loadline was plotted to determine the internal droop of the converter due to the parasitic resistance. At the same time, the input voltage and current were also recorded. This enables an accurate determination of the efficiency of the converter. The results are shown in Figure 2.19.

As shown in Figure 2.19 (a), initially, the loadline for the converter possesses a linear characteristic, signifying the effect of internal series resistance in the output side of the converter. A steep drop from the linear characteristic can be observed after certain current magnitudes indicating the converter has lost its voltage regulation capability due to the limited input power. From the slope in the linear region, the internal series resistance was determined to be 4 Ω (including 1.5 Ω from cable resistance of the Keithley Sourcemeter). From the input and output power determined from the recorded current and voltage on both the input and output sides, the efficiency was calculated and it is shown in Figure 2.19 (b). The peak efficiency was around 65 % when $\Delta T = 39$ °C, and overall efficiency of > 50 % was obtained, which agrees with the expected efficiency obtained from the datasheet. The efficiency curve

shows a typical increase trend when the current is initially increased. This is due to the ratio of the dynamic power consumed by the IC to operate to the output power of the converter is slowly reduced. After reaching the peak value, the efficiency starts to drop due to the increasingly parasitic resistance loss due to the increase in current. When the converter has lost its voltage regulation capability, the input power starts to drop however the efficiency shows a slight increase, due to the decreasing voltage on the output side of the converter.



(a) Feedback loop for MPPC in LTC3105

(b) Resistance of PTC and NTC thermistors against temperature

(c) Required resistance for MPPC vs. resistance of thermistors under different temperature differences

(d) Required resistance for MPPC vs. resistance of thermistors under different temperature differences

Figure 2.17: The MPPC function, the resistance of the PTC and NTC thermistors, and the usage of these thermistors in simulated situations when compared to the required resistance to ensure a reliable MPPC functionality.

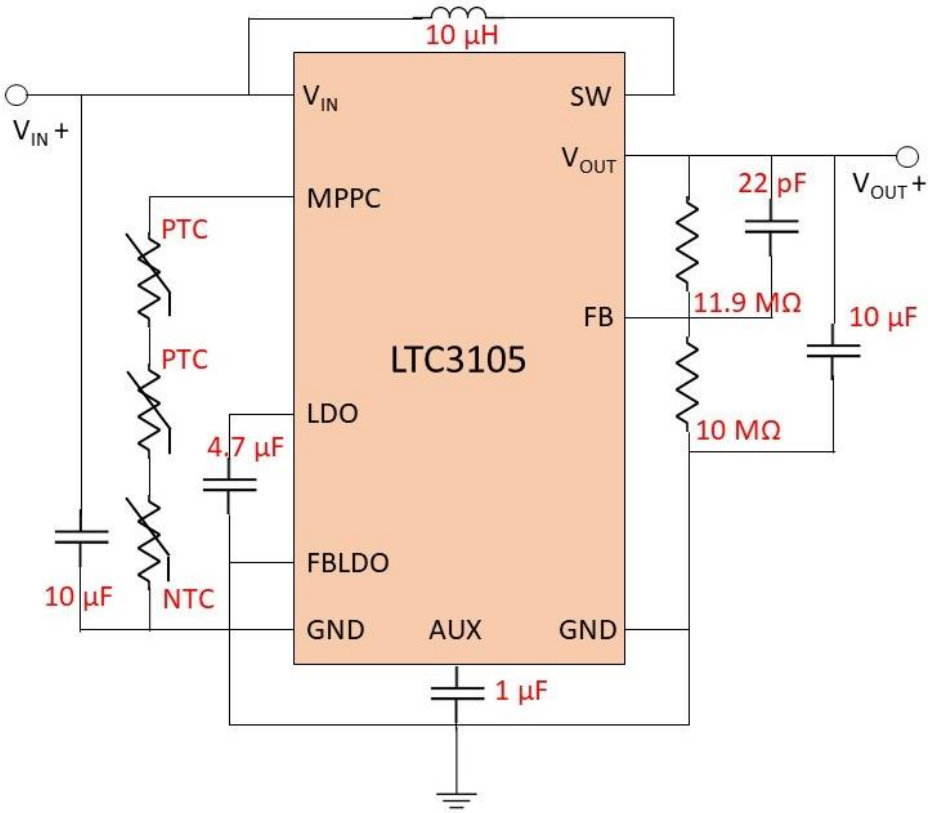
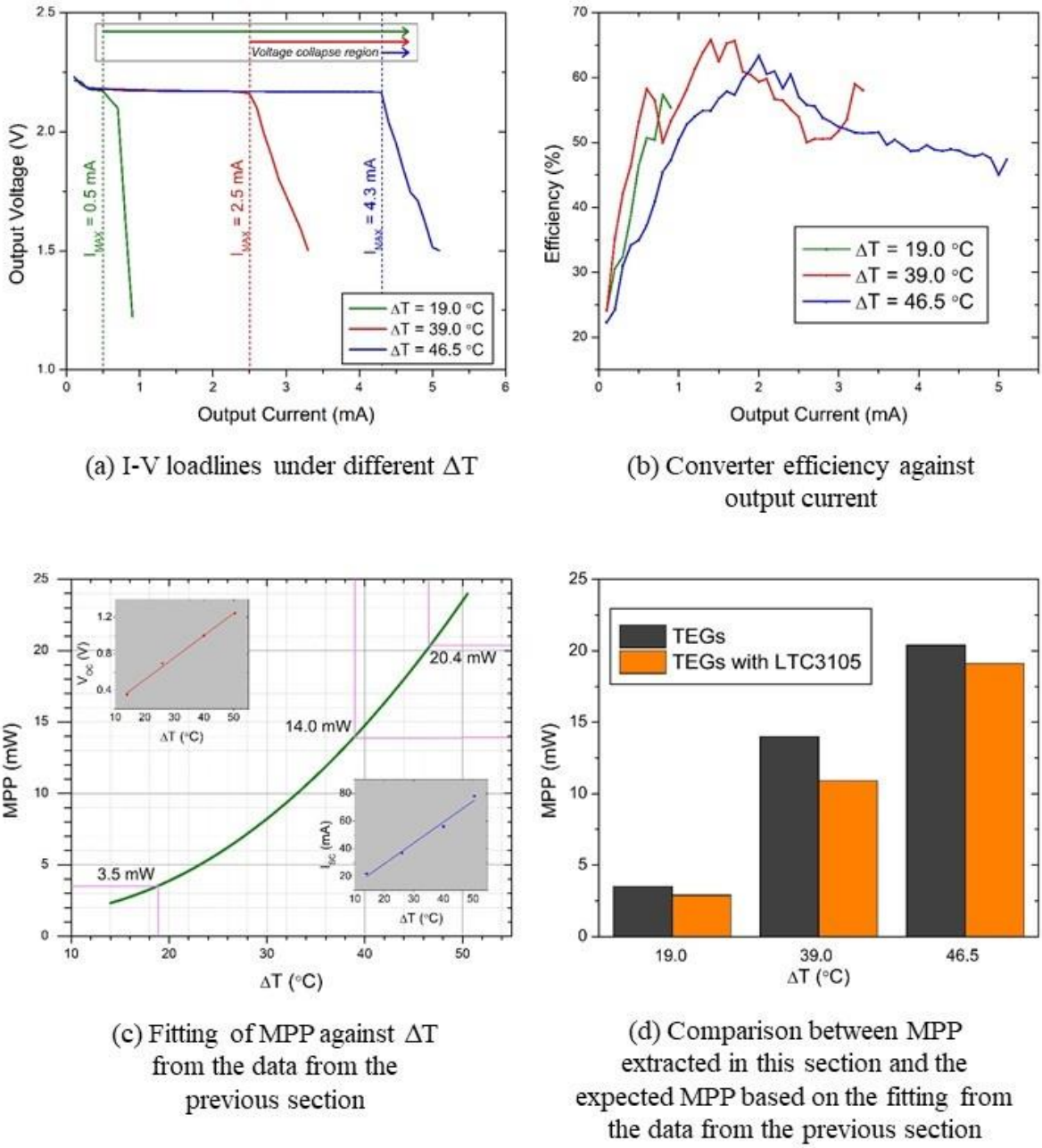


Figure 2.18: LTC-3105 circuit configuration for TEGs used in this thesis.

The trend from Figure 2.19 (a) also indicates a strong dependency of the maximum output current (when the converter still retains its voltage regulation) with ΔT. In order to verify the functionality of the thermistor based MPPT integrated in the IC, a comparison was drawn from the MPP extracted from the TEGs when connected to the IC with the expected MPP obtained from the characterisation in the previous section. Before that, due to the limited controllability over ΔT in the setup, the expected MPP from the TEGs needs to be determined since ΔT data in this section are different from the previous section. From the previous characterisation, both V_{OC} and short circuit current (I_{SC}) are determined to possess a linear dependency with ΔT, as shown in the insets in Figure 2.19 (c). By assuming that the V_{MPP} and the current at which MPP occurs (I_{MPP}) vary linearly with V_{OC} and I_{SC}, respectively, then the MPP can be assumed to vary quadratically with ΔT. Based on the MPP data obtained from the previous section, a best fit polynomial curve (to the power of 2) of MPP against ΔT was obtained and is shown in Figure 2.19 (c). From this, the expected MPP for all ΔT can be approximated and a comparison was drawn between the expected MPP with the extracted MPP by the IC for all ΔT in this section and is shown in Figure 2.19 (d). The extracted MPPs are slightly lower than the expected MPP, mainly due to inaccuracy of the thermistor resistance value compared to the

required resistance value in the loop. However, an overall satisfying performance of MPPT was demonstrated.



(a) I-V loadlines under different ΔT

(b) Converter efficiency against output current

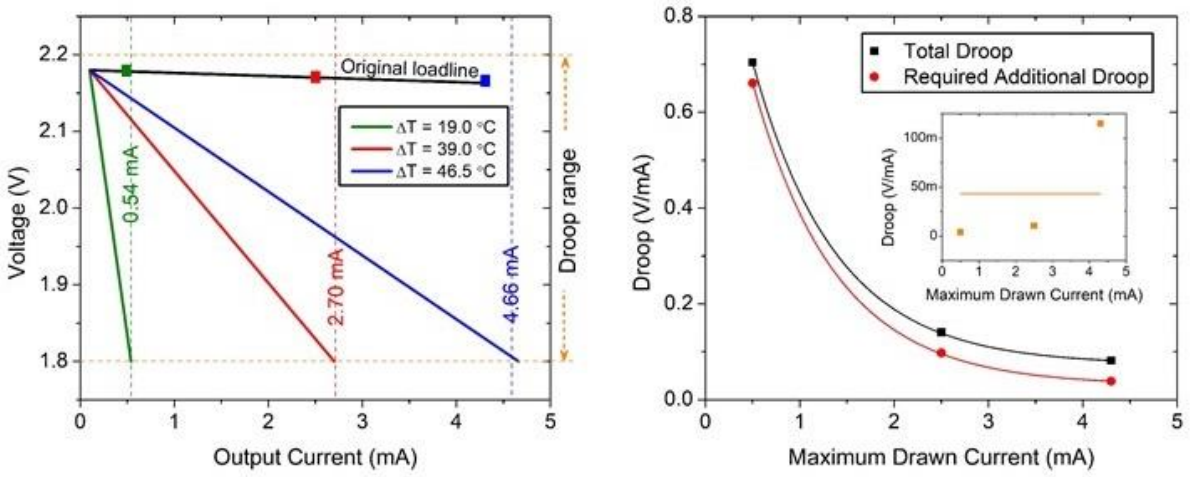
(c) Fitting of MPP against ΔT from the data from the previous section

(d) Comparison between MPP extracted in this section and the expected MPP based on the fitting from the data from the previous section

Figure 2.19: Results from the constructed circuit.

Since the maximum available current hence power available from the converter varies with ΔT, the droop required for each ΔT is also different in magnitude to ensure reliable equal load sharing in the final system. The droop was calculated in the similar manner as the previous section and the new desired loadlines for different ΔT are shown in Figure 2.20 (a). From this, the magnitude of total droop and the required additional droop against maximum drawn current

is plotted and is shown in Figure 2.20 (b). The design of the circuit to introduce these droops which vary with ΔT will be presented in the following section.



(a) Original loadline and new calculated loadlines for different ΔT

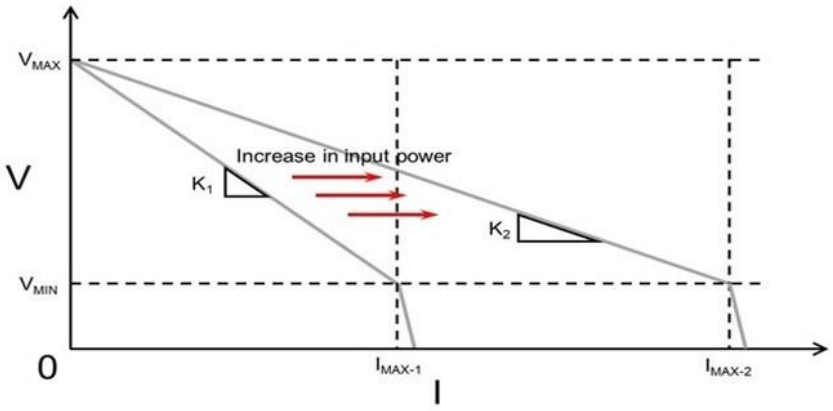
(b) Calculated droop and required additional droop against maximum current to meet design requirements

Figure 2.20: Droop calculations.

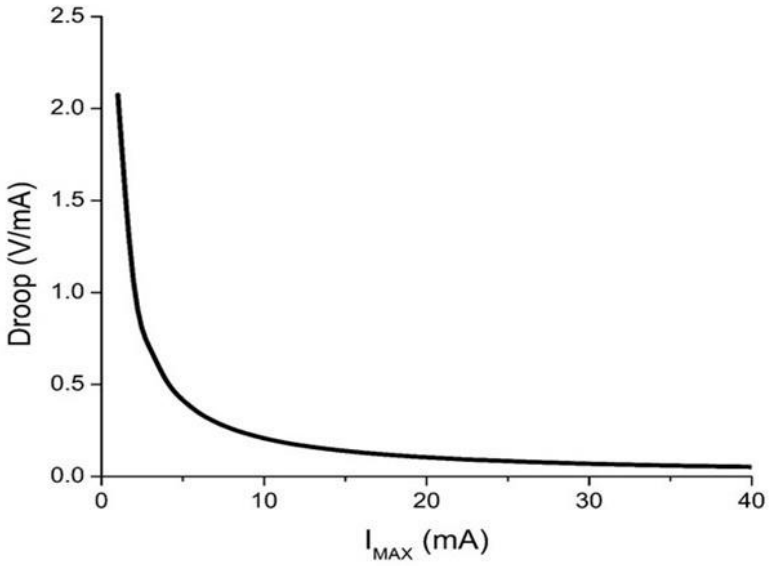
2.3.3 Variable Droop Demonstration

In the literature, static droop (voltage droop which does not vary with time) regulation for load sharing has been widely demonstrated. Whilst this idea has been implemented in high power applications, two major challenges exist for low power energy harvesting applications. The first challenge is associated with the power consumption of the control feedback circuitry, which could become significant if the power level in the system is too low, hence degrading the overall efficiency or even worse, is higher than the power generated by the source. The second challenge is related to the frequent variation of input power which would cause the variation of the rated output power of the converter. This in turn would require that the amount of voltage droop to follow this variation. In most systems however, the amount of voltage droop is designed to be fixed or stiff, and even if it is not fixed, an additional circuitry (example: perturb and observe method) is needed hence further increasing the power consumption. This can be further explained by referring to Figure 2.21. When the harvester output power is increased, the rated output power of the converter will increase. For the same converter voltage (minimum after full droop) as shown in the Figure 2.21 (a), the maximum output current will increase. Hence the magnitude of the droop which is equal to the gradient of the loadline needs to change to cater for this variation to ensure that maximum amount of power is available from

each converter to the load. For example, by defining that V_{MAX} = 2.2 V and V_{MIN} = 1.8 V, the variation of the required droop against maximum output current is shown in Figure 2.21 (b).



(a) The value of different gain is needed when the power rating is increased for a converter



(b) The variation of the droop gain required against maximum current for an example case of V_{MAX} = *2.2 V* and V_{MIN} = *1.8 V*

Figure 2.21: The need for variable droop gain.

The typical configuration for a static voltage droop regulation is shown in Figure 2.22. In this, the voltage droop is integrated in the voltage feedback loop of the power converter to modify the reference required output voltage to achieve regulation. The R_D shown in the figure which is the gain for the output current corresponds to the magnitude of the voltage droop. The most outer droop loop has a slower response than the output voltage loop and the inner current loop (if the converter is in current mode controlled), thus the dynamic behaviour of the converter can be effectively decoupled from the droop loop. Therefore, the behaviour of the system can

be accurately modelled by assuming that the new reference voltage introduced to the system after deduction by the required droop as a constant while analysing the response of the converter.

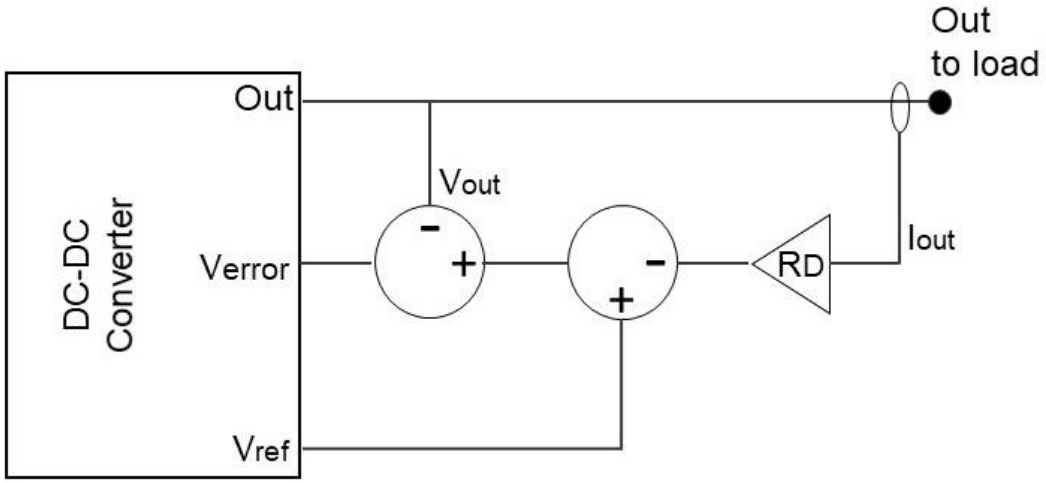


Figure 2.22: Droop integrated in the voltage feedback loop of a DC-DC converter.

Since the magnitudes of current for both solar panel and TEGs are very low, therefore the typical Hall Effect current sensor is not suitable to be used in this system. A more sensitive current sensor is needed and the most suitable solution for this is to use a current shunt monitor. A current shunt monitor works by sensing a differential voltage across a very small sense resistor placed in series with the conduction path from the output of the converter to the load, which will be multiplied with the set gain to output a voltage which is linearly related to the magnitude of the current that flows in this path. The proposed circuitry for the droop configuration used in this thesis is presented in Figure 2.23 (a). Figure 2.23 (b) shows the non-inverting summing amplifier used in the loops. In this configuration, the scaled voltage in the droop loop is summed with the scaled voltage in the feedback loop and then fed to the feedback input of the previous ICs. By selecting an appropriate gain for both loops, they can be seamlessly integrated with the ICs whilst maintaining the same level of reliable operation throughout the range of expected output voltage and voltage droop.

From Figure 2.23 (a), the value of differential voltage V_{SENSE} is:

$$V_{SENSE} = I_{OUT}R_{SENSE}$$

The output voltage for the current shunt monitor is magnified by a constant, β, and is connected in series with variable resistance R_5 and R_6. The voltage across R_5 and R_6 is equal to:

$$V_{R5+R6} = \beta V_{SENSE} = \beta I_{OUT}R_{SENSE}$$

The resistance R_5 and R_6 are variable resistors whose values can be programmed to vary with the input power to ensure proper droop at all input power level. The voltage across R_6 is fed to the input of the non-inverting summing amplifier:

$$V_{R6} = \alpha\beta V_{SENSE} = \alpha\beta I_{OUT} R_{SENSE}$$

where α is:

$$\alpha = \frac{R_6}{R_5 + R_6} \dots \text{eq (2.3)}$$

Another input of the non-inverting summing amplifier is the voltage across R_2 which is a scaled voltage of the converter output voltage responsible for the voltage regulation loop of the converter:

$$V_{R2} = \gamma V_{OUT} \dots \text{eq (2.4)}$$

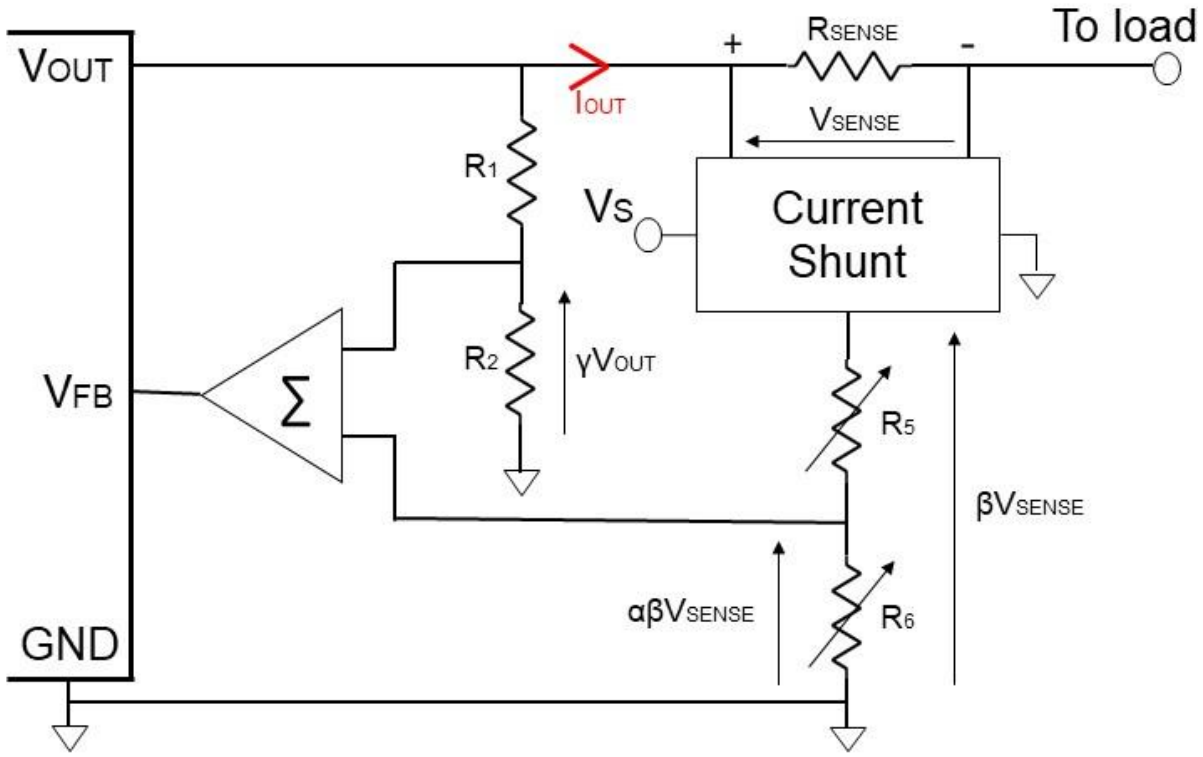
where γ is:

$$\gamma = \frac{R_2}{R_1 + R_2}$$

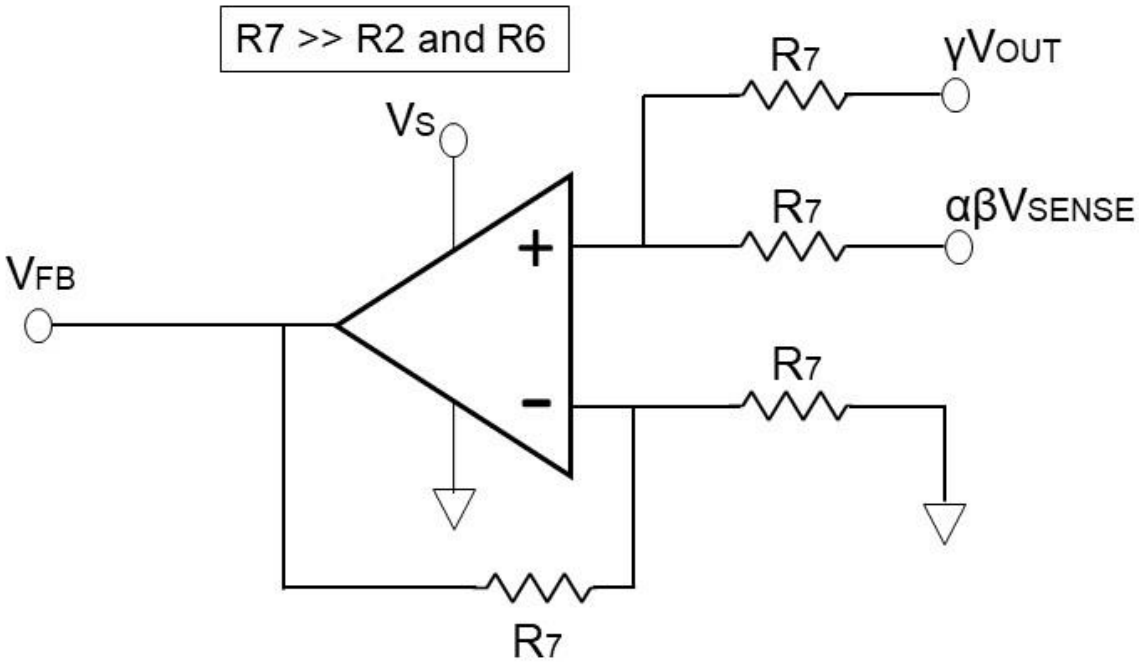
From Figure 2.23 (b), the transfer function of the non-inverting summing amplifier is:

$$V_{FB} = \left(1 + \frac{R_7}{R_7}\right)\left(\frac{R_7}{R_7 + R_7}\alpha k V_{SENSE} + \frac{R_7}{R_7 + R_7}\beta V_{OUT}\right) = \alpha\beta V_{SENSE} + \gamma V_{OUT}$$

In this configuration, R_7 needs to be significantly larger than R_2 and R_6 in order to ensure that there is no significant proportional amount of current to flow through R_7 in both loops, hence ensuring the accuracy of the programmed voltage ratio. The current shunt monitor used in this thesis is a Texas Instruments INA283AID, with a fixed gain of 200 V/V. The minimum supply voltage for this IC is 2.7 V. This level of voltage is not available in the circuit therefore an external source is required. In this thesis, this IC is directly powered by a Panasonic CR2032 3V Lithium Manganese Dioxide Coin Button Battery. However, by ensuring that the power consumption of this IC is much lower than the power transferred to the load when the power converter is online, positive power gain can still be maintained in the system. In order to ensure accurate determination of output current, R_{SENSE} cannot be too small otherwise noise will dominate the voltage across it. However, large R_{SENSE} contributes to more losses. Moreover, with the 3 V supply to the current shunt monitor, the maximum V_{SENSE} to ensure that the voltage is still within the gain range without saturating is 15 mV. The expected maximum current for each harvester needs to be considered whilst deciding the magnitude for R_{SENSE}.



(a) Droop loop implementation



(b) Non-inverting summing amplifier

Figure 2.23: Droop loop implementation and non-inverting summing amplifier configuration.

R_5 and R_6 are resistors whose values vary with the input power to ensure proper droop variation. In case of solar panel, an LDR will be used and in case of TEGs, both PTC and NTC thermistors will be used. This will be discussed in the following sections. The ratio of R_1 and R_2 should follow the datasheet of the power converter IC. The op-amp used in this thesis is a STMicroelectronics TSV632IDT. This low power op-amp requires a minimum supply voltage of 1.5 V. Similar as before, this op-amp will be directly powered by a Panasonic CR2032 3V Lithium Manganese Dioxide Coin Button Battery. It should be noted that throughout the entire experiments, the power consumption of these two ICs are monitored and considered in evaluating the efficiency of the whole system.

a. Variable Droop for Solar Cell

For the LTC-3129 power converter used for the solar cell, the internally generated reference voltage for the feedback loop is 1.175 V. When no current is flowing to the load, only the scaled voltage from the output voltage feedback loop will be compared with this reference voltage, therefore the selection of the resistance values for R_1 and R_2 will follow the datasheet. However, when the current starts to flow to the load, the summation of the voltage from the output voltage feedback loop with the droop feedback loop will be compared together with the reference voltage. In order to design an accurate droop regulation, in steady state, the summation of these two voltages should be equal to 1.175 V at the full range of the expected output voltage.

The first step of the design process is to define the value of R_{SENSE}. Based on the output characteristics of the converter obtained from Section 2.3.2, the maximum current expected from this converter when powered by the solar panel is around 30 mA. From this maximum current, the value for R_{SENSE} was selected to be 0.5 Ω. By using this resistance value, and by considering the maximum input voltage from the coin battery (3 V) and also the fixed gain of the current shunt monitor (200), a full range of output current of 30 mA can be accurately sensed by the current shunt monitor before it saturates.

The plot of the output voltage of the shunt current monitor against the output current for the theoretical and experimental values are shown in Figure 2.24 (a). It can be observed that a good agreement was obtained from these two values. Next, the droops need to be recalculated since the insertion of the R_{SENSE} in the path of the output current will add an internal droop of 0.5 mV/mA to the converter:

$$\text{Internal droop } \left(\frac{\text{mV}}{\text{mA}}\right) = \text{R}_{\text{OUT}} + \text{R}_{\text{SENSE}} = \text{R}_{\text{OUT}} + 0.5$$

Here R_{OUT} is the existing internal droop before the addition of the droop feedback circuitry. The calculations follow the steps presented in eq. (2.1) and eq. (2.2) before. The plot for the calculated required droop is shown in Figure 2.24 (b) together with the total and internal droops against the full range of output current. By using the value of internal droop in the figure, the converter output voltage (without external droop mechanism) can be determined. Due to the presence of this internal droop, the new minimum voltage at full load that should be directly outputted from the converter is no longer 1.8 V, however it is higher and depending on the I_{MAX} as shown in Figure 2.24 (c), since the internal drop varies with I_{MAX}. By placing the voltage feedback loop (resistor divided network R_1 and R_2) as close as possible to the V_{OUT} pin of the converter, the voltage across resistor R_2 (V_{R2}) can be determined based on eq. (2.4) presented before for each I_{MAX} and is shown in Figure 2.24 (d). At the steady state operation of the converter, the summation of V_{R2} with the feedback from the droop loop (voltage across R_6, V_{R6}) needs to be equal to the internally generated reference voltage of the converter (1.175 V for LTC3129). Thus, the required magnitude of V_{R6} was calculated and shown in the same figure:

$$\text{V}_{\text{R6}}(\text{at I}_{\text{MAX}}) = 1.175 - \text{V}_{\text{R2}}(\text{at I}_{\text{MAX}})$$

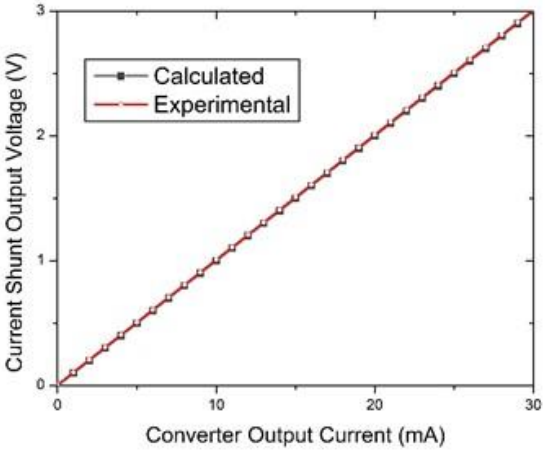
The droop feedback loop needs to be accurately tuned to produce this level of V_{R6} for different I_{MAX}. From the required V_{R6}, the resistor divider network ratio for R_5 and R_6 can be calculated from eq. (2.3) and is shown in Figure 2.24 (e). At a low current edge, the required ratio is negative due to the level of current shunt output voltage which is less than what is required from V_{R6}. In other words, V_{R6} will not be able to reach the required value. In turn, the magnitude of the droop in this region will be below the required value, hence the operation of the converter could potentially collapse before V_{MAX} is reached, due to the insufficient amount of input power available. Thus it is important that this operating region is avoided.

From the required ratio, the calculated resistance value needed for R_6 with the variation of I_{MAX} for a fixed value of R_5 of 44 kΩ is shown in Figure 2.24 (f). The three I_{MAX} shown in the figure correspond to the calculated I_{MAX} from P_{MAX} of the converter for three different illuminations as obtained in the previous section. In the same figure, the resistance of N5AC501085 LDR subjected to the same illuminations is shown. An almost perfect match for this LDR resistance with the required resistance value for R_6 was obtained for illumination 1 and 2, whereas a deviation can be observed for illumination 3. However, since the resistance of the LDR for this

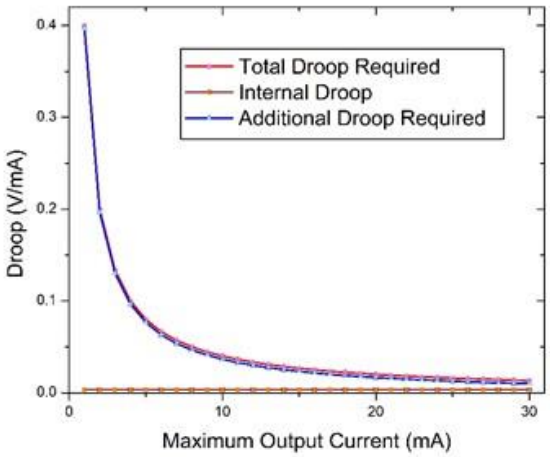
illumination is higher than the required value, it would not jeopardize the operation of the converter, since a similar or higher resistance value is needed to prevent the operation from collapsing due to overloading condition. This LDR was then used as R_6 and the circuit was tested. Both solar panel and LDRs for MPPT functionality and droop voltage regulation were subjected to the same level of illumination throughout the test. Figure 2.25 shows examples of a scope view of the output voltage of the converter subjected to illumination 2 and 3 after the droop feedback mechanism has been integrated. The output voltage shows a dependent on the output current (output voltage decreases with the increase in output current) hence validates the function of the droop feedback loop. However, a steady state error for a no load condition (0 mA) can be observed. This is suspected mainly due to the small error of the resistance of the resistors used and also the non-unity gain of the summing amplifier due to this error.

In order to provide an accurate assessment on the variable droop of the converter, the results were further analysed and are shown in Figure 2.26. Figure 2.26 (a) provides a comparison between actual (solid lines) and required (dashed lines) V-I loadlines of the converter for these 3 different illuminations. An almost perfect match was obtained for illumination 1 and 2, however the I_{MAX} in the actual loadline for illumination 3 was less than the required I_{MAX}. This agrees with the deviation of LDR resistance from the required resistance for R_6 when subjected to illumination 3. Figure 2.26 (b) shows the output power of the converter against output current. The blue region corresponds to the power consumption of the droop feedback loop which was powered by an external battery. A power gain in the system is obtained when the output power of the converter is higher than 2 mW. Figure 2.26 (c) shows the efficiency of the converter against output current for each illumination. Compared to the converter with no presence of droop feedback loop, a reduction of around 10 %, 8 %, and 6 % was observed for illumination 1, 2, and 3 during I_{MAX}, respectively. This reduction is fully attributed to the power consumption of the droop feedback loop. This shows that it is possible to design a reliable droop mechanism for any low power converter. Figure 2.26 (d) shows a comparison for maximum power at V_{MIN} (1.8 V) between actual and desired condition. Similar as before, an almost perfect match was obtained for illumination 1 and 2, however the actual power for illumination 3 was less than the desired power, which means that there will be a presence of unutilised power from the converter when the system is under illumination 3. This error is suspected to become even larger when the illumination level is further increased. Hence, it is important for the LDR resistance to be chosen to match the expected illumination level in the

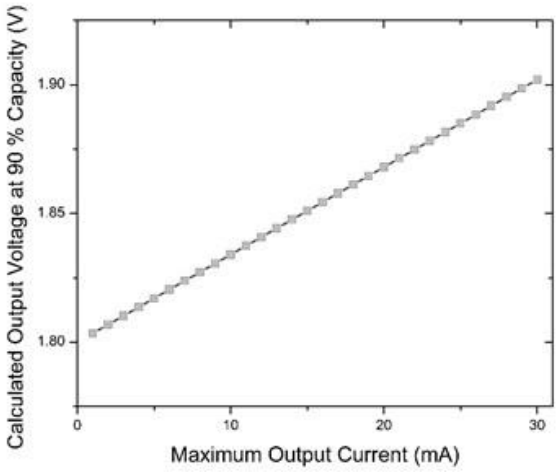
system. Overall, it was shown that the droop feedback loop is capable of reliably self-adjusting the droop gain to account for the variation of input power.



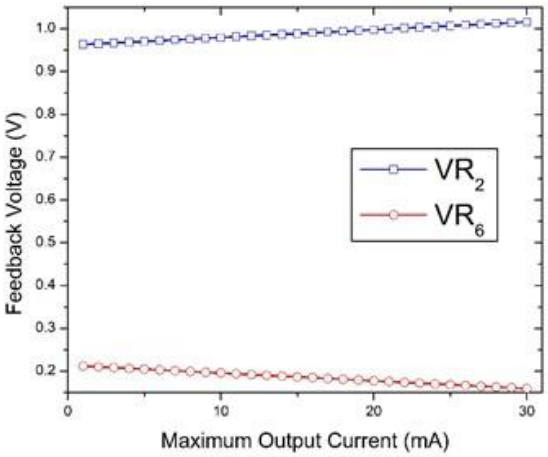
(a) Current shunt output voltage *vs.* output current



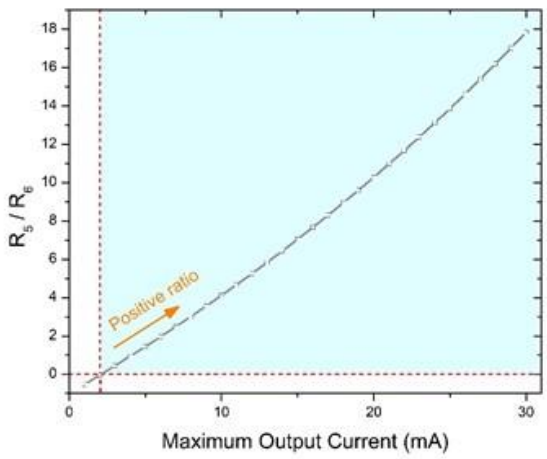
(b) Calculated droops *vs.* output current



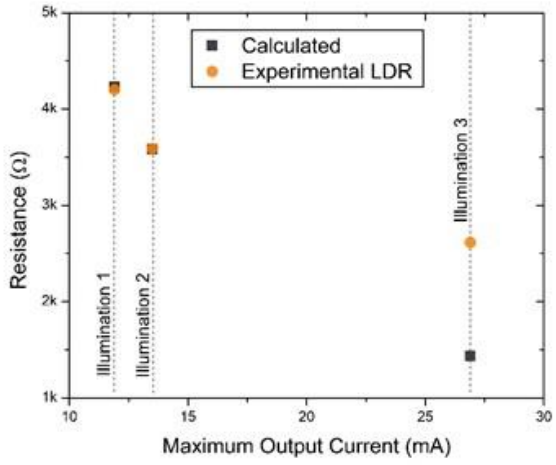
(c) Calculated output voltage at 90 % cap. *vs.* output current



(d) Feedback voltage (VR_2 and VR_6) *vs.* max. output current

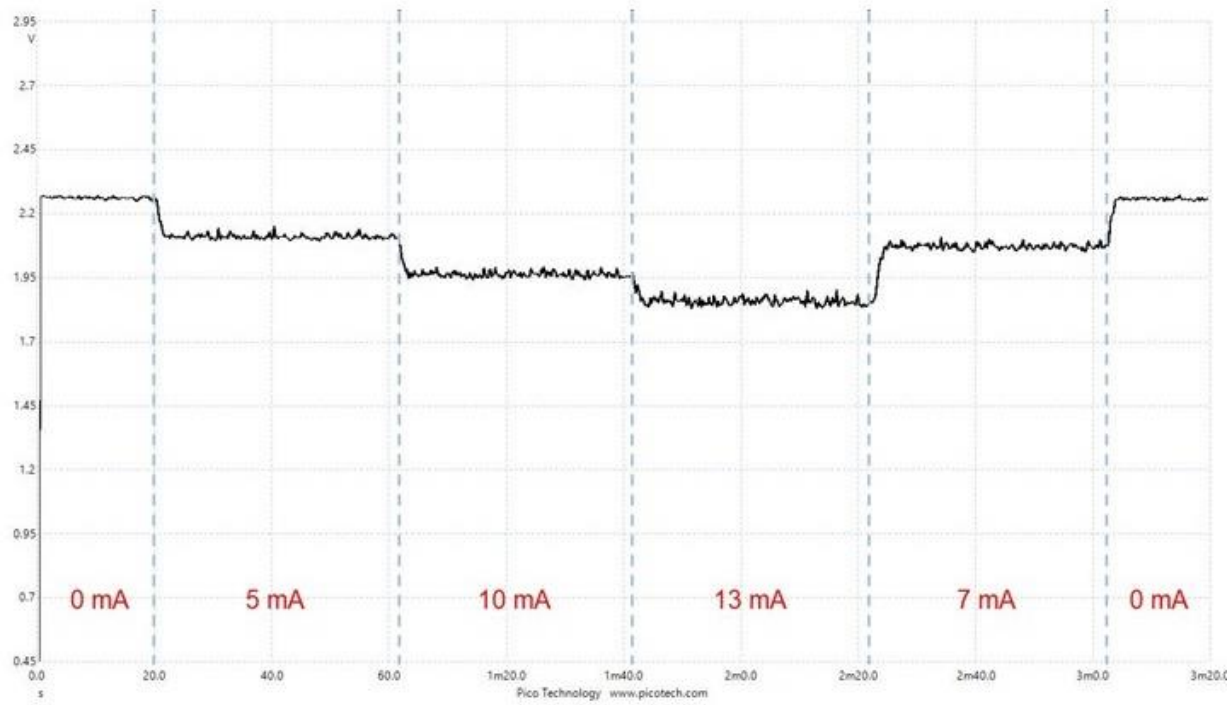


(e) R_5/R_6 ratio *vs.* output current

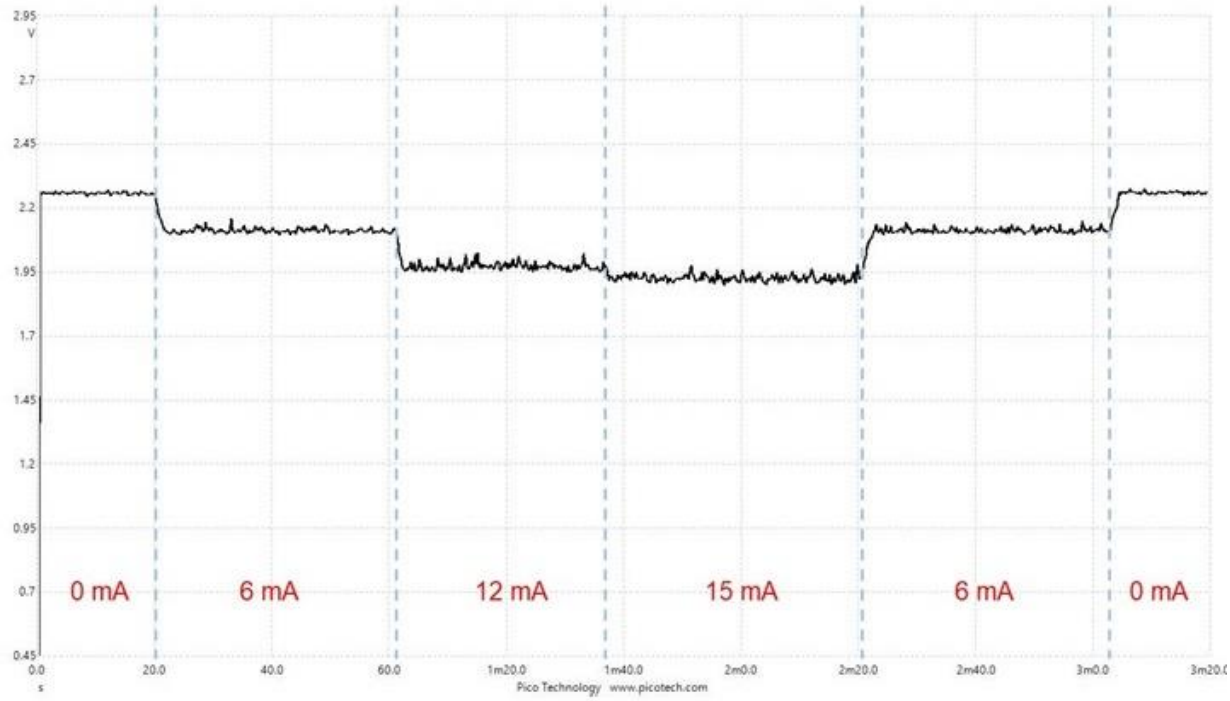


(f) Comparison between calculated and experimental R_6

Figure 2.24: Voltage droop feedback calculations for the LTC-3129 (solar panel).

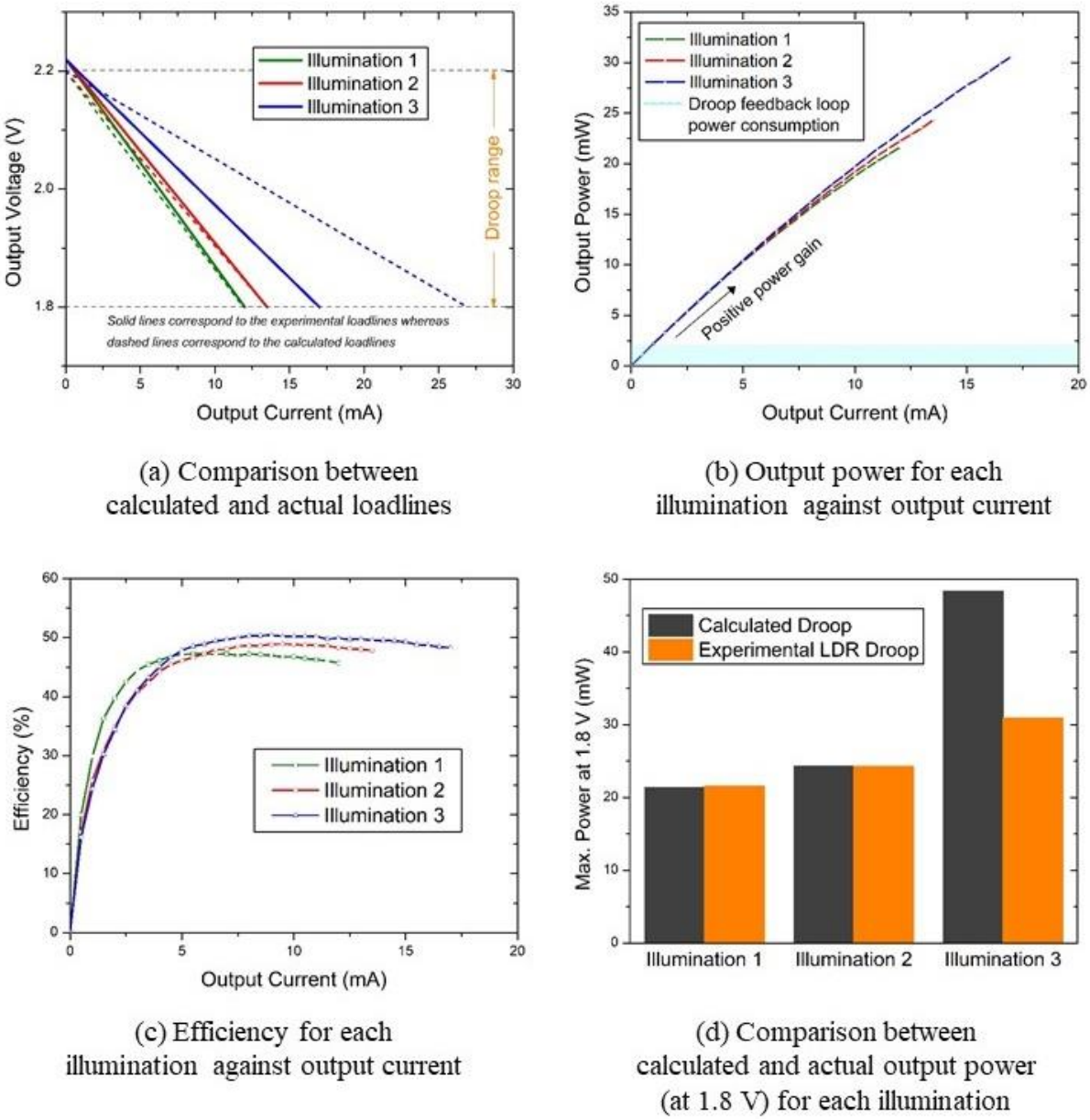


(a) Scope view of V_{OUT} against time when I_{OUT} is varied for illumination 2



(b) Scope view of V_{OUT} against time when I_{OUT} is varied for illumination 3

Figure 2.25: Scope waveform results for the droop test for the LTC-3129 (solar panel).



(a) Comparison between calculated and actual loadlines

(b) Output power for each illumination against output current

(c) Efficiency for each illumination against output current

(d) Comparison between calculated and actual output power (at 1.8 V) for each illumination

Figure 2.26: Analyses for voltage droop performance for the LTC-3129 (solar panel).

b. Variable Droop for TEGs

For TEG, the maximum expected range of the converter output current is 10 mA. Considering this, a 1.5 Ω precision resistor was used as R_{SENSE}. The output voltage for the current shunt monitor against the current through R_{SENSE} is shown in Figure 2.27 (a). The same method was applied for the droop feedback loop for the TEG. However, instead of comparing all parameters with the converter output current, they were compared with ΔT in order to provide a more accurate representation of the variation of input power. For a solar panel, this cannot be done since the illumination level cannot be quantified and only the output current of the converter

information is available based on the original V-I loadlines. In order to estimate the output power hence current of the converter for different ΔT, the following expression was used:

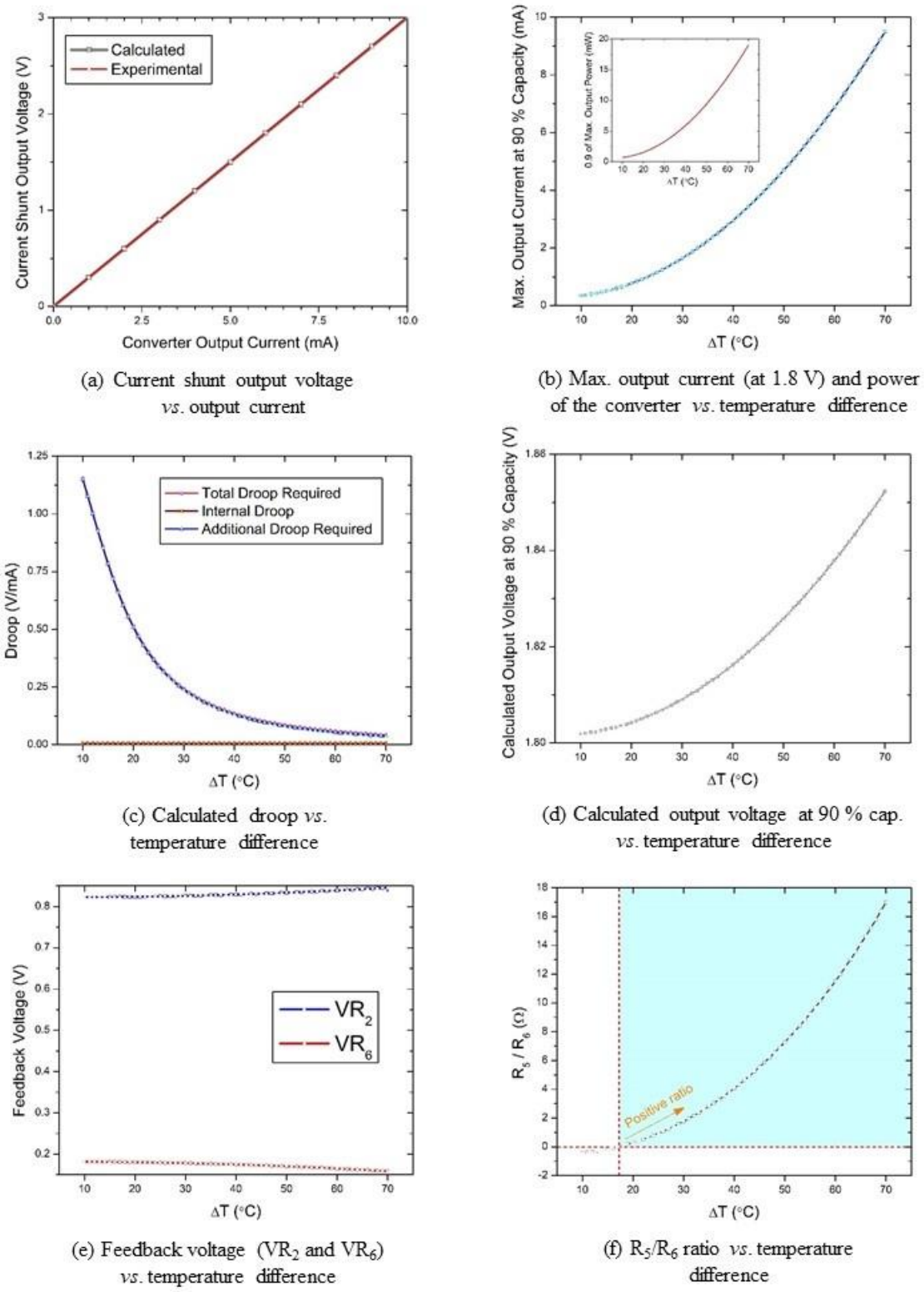
$$P_{MAX\ converter}(\Delta T) = \eta_{MPPT} \times \eta_{converter} \times P_{MPP\ TEG}(\Delta T)$$

Where η_{MPPT} is the efficiency of MPPT based on the thermistors configuration presented in the previous section (≈ 80 %) and $\eta_{converter}$ is the efficiency of the converter (≈ 60 %). The MPP of the TEG was obtained from Figure 2.19 (c). From this, the estimated maximum output power for the converter against ΔT is shown in Figure 2.27 (b). Following the same steps as before, the calculated droops, the new minimum voltage of the converter taking into account the additional and internal droops, feedback voltage (V_{R2} and V_{R6}), and R_5/R_6 ratio, all against ΔT, are shown in Figure 2.27 (c), (d), (e), and (f), respectively. The only different for this IC is the internally generated reference voltage which is at 1.004 V.

Unlike solar panels whose output power depends only on one factor (illumination), TEG output power depends on ΔT which in turn depends on two factors; the temperature for hot and cold sides. For this, the thermistors configuration is more complicated than the LDR configuration. From the required R_5/R_6 ratio, the magnitude of each R_5 and R_6 when the other is being set to 1 Ω was determined and is shown in Figure 2.28 (a). By setting the coupling of R_5 with cold side and R_6 with the hot side, the trend of the required resistance against temperature can be determined. From this, it was deduced that both thermistors need to possess NTC characteristics.

Figure 2.28 (b) shows the resistance value for three NTC thermistors against temperature. Based on these values, it was determined that there are two possible combinations to satisfactorily meet the design requirements for the thermistors configuration. The first configuration is 1 unit of ND03U00105J thermistor coupled to the hot side and 2 units of B57861S0503H040 thermistor coupled to the cold side and the second configuration is 1 unit of B57861S0503H040 thermistor coupled to the hot side and 2 units of B57871S0123H000 thermistor coupled to the cold side. For the first configuration, the value of the actual and required resistance for R_6 is shown in Figure 2.28 (c) for each of the value of R_5/temperature of the cold side. Although not a perfect match was obtained, it was preferable to maintain the actual value of R_6 to be higher than the required value to prevent the converter operation from collapsing due to excessive loading at I_{MAX}/V_{MIN}. In this configuration, this criteria is met when ΔT is greater than 20 °C. Similarly, for the second configuration, the comparison between actual and required resistance value is shown in Figure 2.28 (d). For this configuration, actual

R_6 is higher than the required R_6 when ΔT is greater than 30 °C. However, it can be observed that the value of actual R_6 for this configuration has a better matching with the required R_6 compared to the first configuration. By considering the presence of a guard factor in determining I_{MAX}, the second configuration was selected.



(a) Current shunt output voltage *vs*. output current

(b) Max. output current (at 1.8 V) and power of the converter *vs*. temperature difference

(c) Calculated droop *vs*. temperature difference

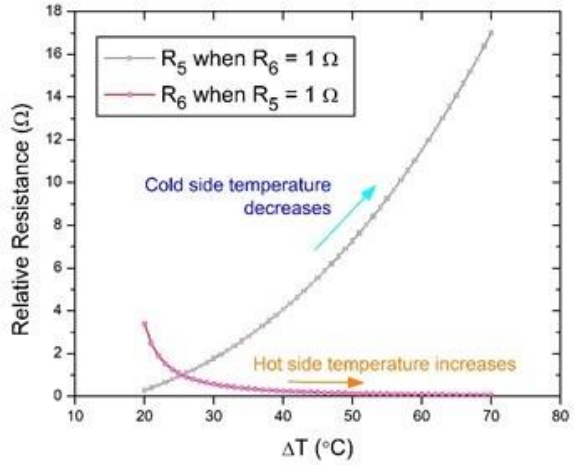
(d) Calculated output voltage at 90 % cap. *vs*. temperature difference

(e) Feedback voltage (VR_2 and VR_6) *vs*. temperature difference

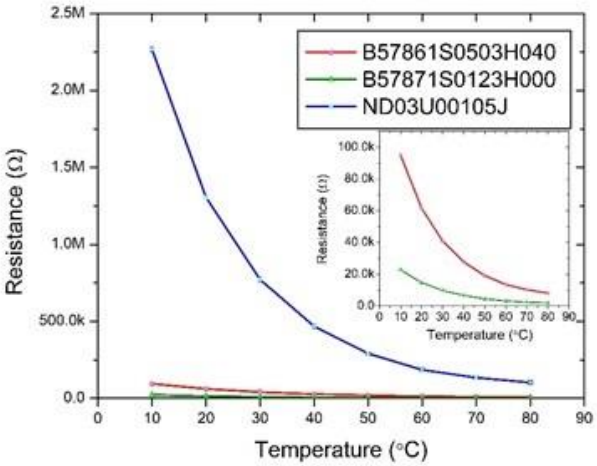
(f) R_5/R_6 ratio *vs*. temperature difference

Figure 2.27: Voltage droop feedback calculations for the LTC-3105 (TEG).

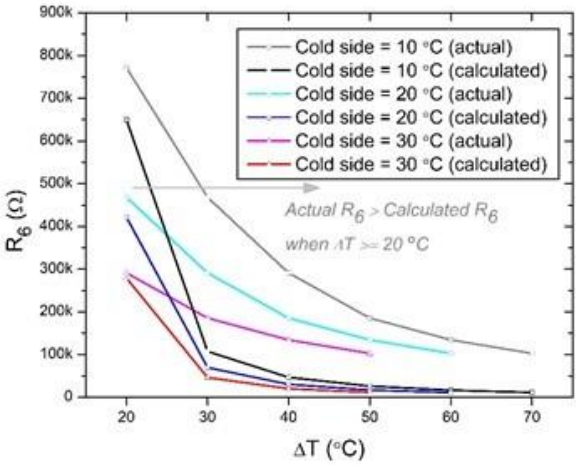
The circuit was then tested and the actual view of the scope for the converter output voltage for ΔT = 39 °C is shown in Figure 2.29. The voltage shows a dependent on the output current hence validates the function of the droop feedback loop. However, a steady state error for no load condition (0 mA) can be observed. Similar as before, this is suspected mainly due to the small error of the resistance of the resistors used and also the non-unity gain of the summing amplifier due to this error.



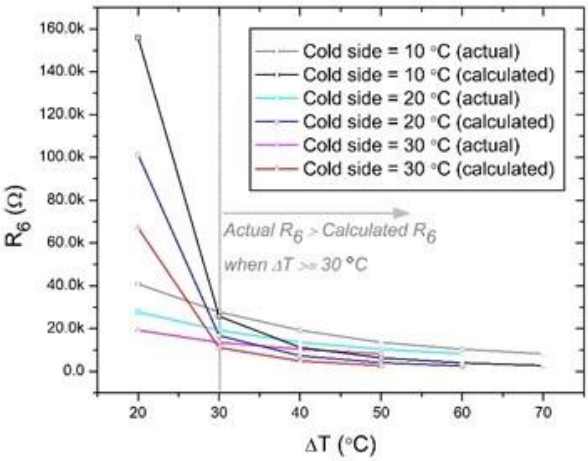
(a) Relative resistance for R_5 and R_6 *vs.* temperature difference



(b) Resistance of three NTC thermistors *vs.* temperature



(c) Actual and calculated resistance for R_6 (NTC thermistor on hot side) for each R_5 (corresponding to resistance of NTC thermistor on cold side) (Configuration = 1 ND03U00105J on hot side and 2 B57861S0503H040 on cold side)



(d) Actual and calculated resistance for R_6 (NTC thermistor on hot side) for each R_5 (corresponding to resistance of NTC thermistor on cold side) (Configuration = 1 B57861S0503H040 on hot side and 2 B57871S0123H000 on cold side)

Figure 2.28: Thermistors configurations for the LTC-3105 to self-track input power variation for TEG.

The results were further analysed and the actual V-I loadlines for multiple ΔT were compared with the required/desired loadlines. This is shown in Figure 2.30 (a). The actual loadlines for

all ΔT have the magnitude of I_{MAX} less than the required value, however the matching between the actual and required loadlines is better at lower ΔT. This agrees with the expected trend due to the actual value of R_6 which has a better matching with the required value at lower ΔT. Figure 2.30 (b) shows the output power of the converter against output current. Similar as before, the blue region corresponds to the power consumption of the droop feedback loop which was powered by an external battery. A power gain in the system is obtained when the output power of the converter is higher than 1.3 mW. Figure 2.30 (c) shows the efficiency of the converter against the output current for each ΔT. When compared to the converter with no presence of droop feedback loop, a reduction of generally around 20 % of the efficiency was observed for all ΔT during I_{MAX}. This is higher than the value reported previously for the solar panel due to the higher proportion of droop feedback power consumption from the lower power capability of the TEG. Figure 2.30 (d) shows a comparison for maximum power at V_{MIN} (1.8 V) between the actual and desired condition. Generally, the actual power was lower than the desired power, which means that there will be a presence of unutilised power when the droop feedback loop is operated. Overall, similar to before, it was shown that the droop feedback loop is capable of reliably self-adjusting the droop gain to account for the variation of input power.

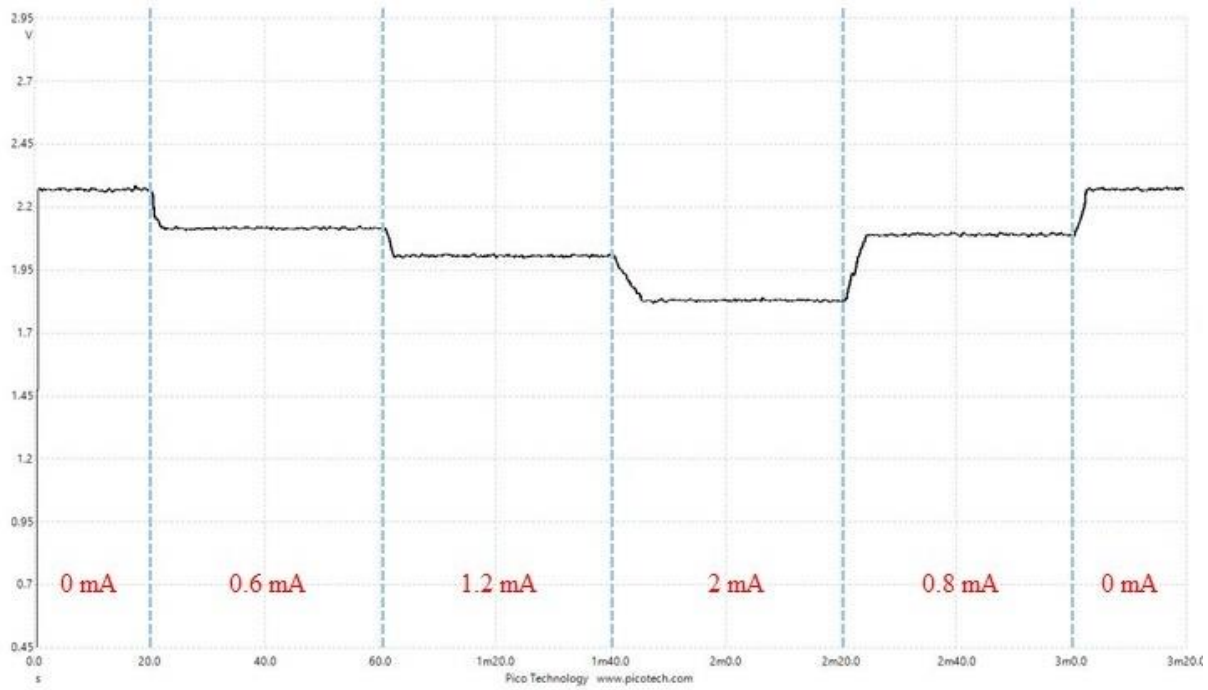
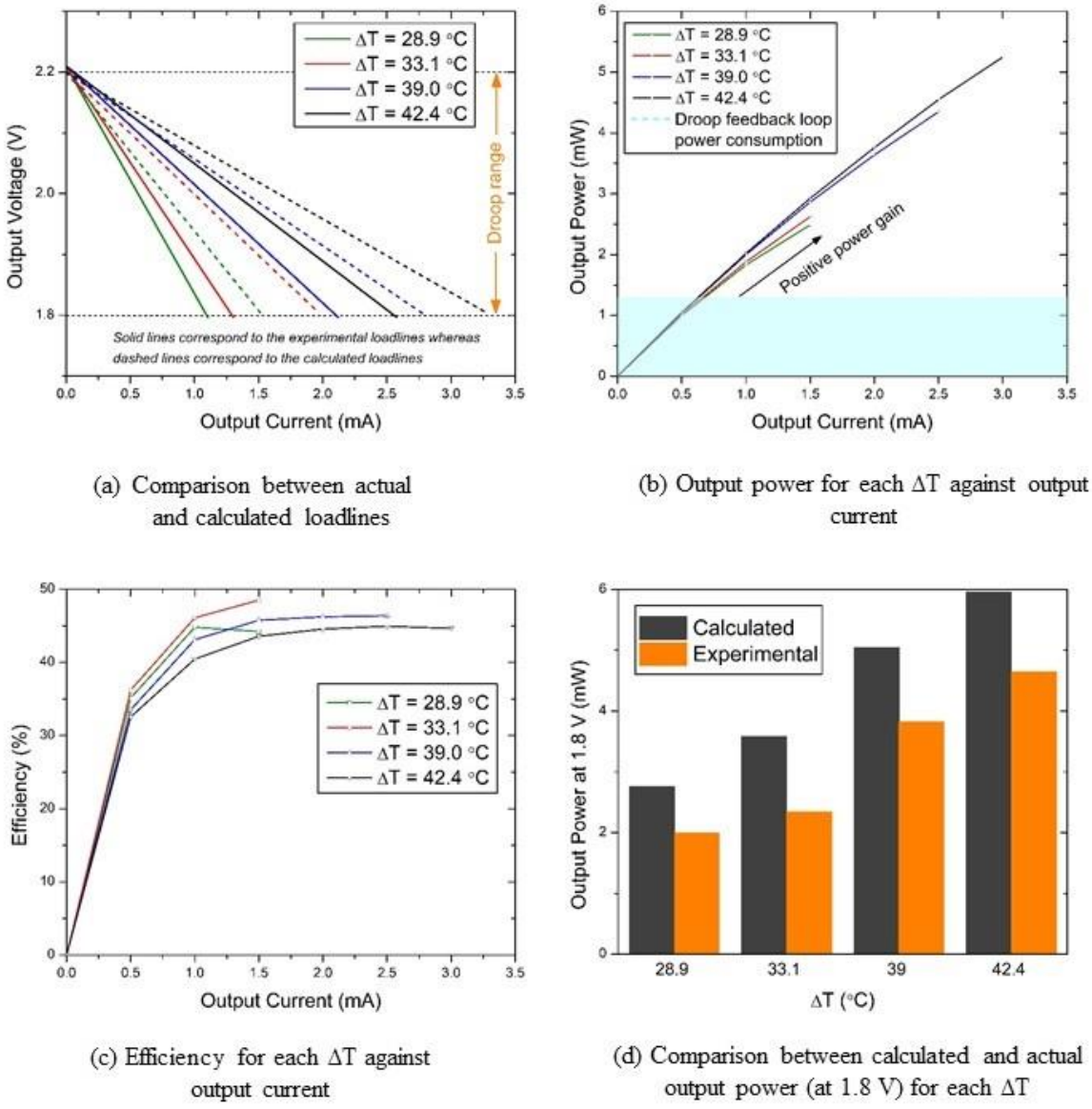


Figure 2.29: Scope waveform results for the droop test for the LTC-3105 (TEG).

This section has demonstrated that by using the right combination resistance value for LDR and thermistor, a reliable MPPT and variation in droop gain functionality can be achieved. The

same concept can be extended to any other converter or even other types of harvesters, provided that some resistance or reference voltage in the system can vary with the magnitude of harvested power. In the next section, the load sharing results for the solar panel and TEG when connected in a single system will be presented.



(a) Comparison between actual and calculated loadlines

(b) Output power for each ΔT against output current

(c) Efficiency for each ΔT against output current

(d) Comparison between calculated and actual output power (at 1.8 V) for each ΔT

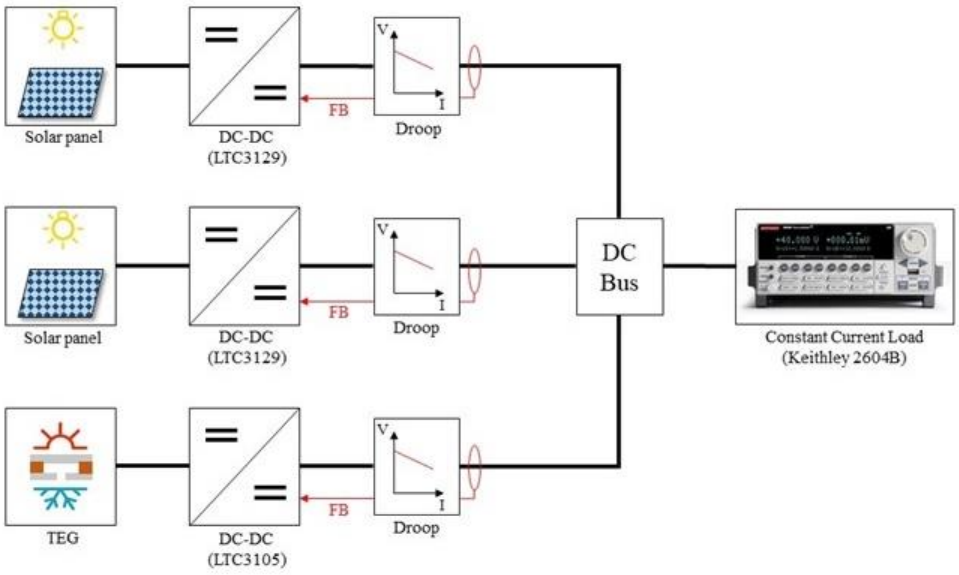
Figure 2.30: Analyses for voltage droop performance for the LTC-3105 (TEG).

2.4 Load Sharing Demonstration

After the self-adjusted droop mechanism has been successfully demonstrated for both solar panel and TEG applications, the circuits need to be connected together to validate the reliable parallel and load sharing operation of these multiple converters. In this section, this parallel system of multiple and multitype converters was constructed and subsequently the results

obtained from the constructed system are presented and the general performance of the system is discussed.

2.4.1 System Layout



(a) System layout

(b) Test rig

Figure 2.31: System layout and test rig used to validate the load sharing experiments.

In order to demonstrate the proposed system, a test rig was constructed and the layout is shown in Figure 2.31 (a). Two similar circuits for the solar panel were constructed and connected with

a single TEG. There were switches between the converter output and DC bus to demonstrate the plug-and-play action. The actual test rig is shown in Figure 2.31 (b). Two cases are presented.

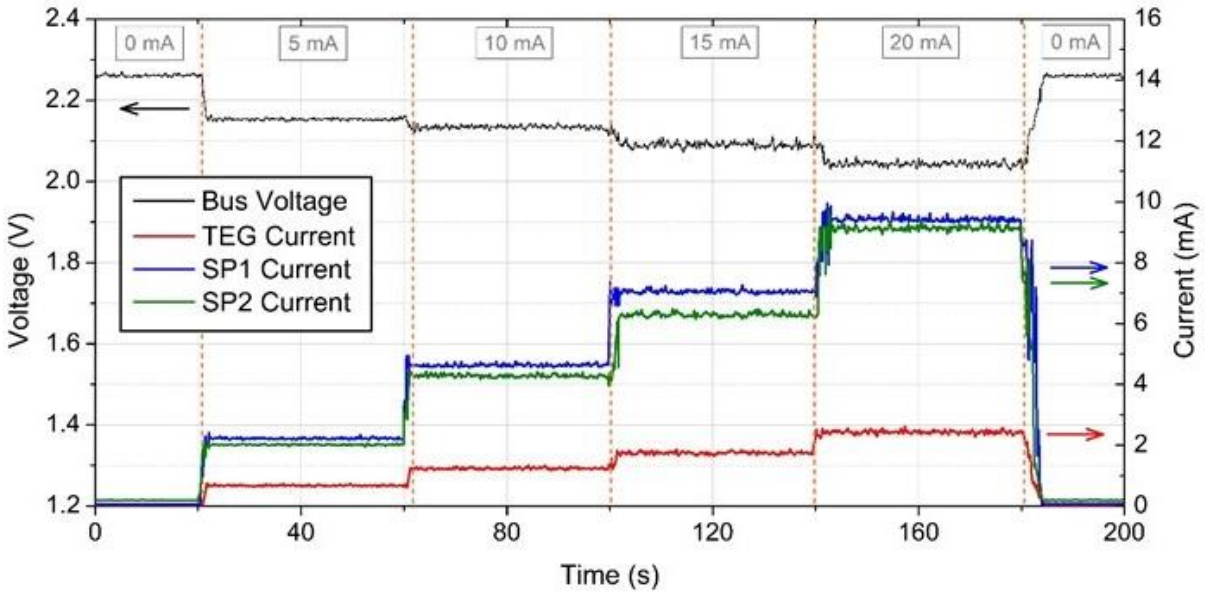
2.4.2 Case 1: Parallel Load Sharing Demonstration

In case 1, all converters were connected to the DC bus at all times. The current demand from the constant current load mimicked by the Keithley Sourcemeter was varied (also indicating plug-and-play action for load) and for each of this variation, the bus voltage and the current from each converter (obtained indirectly from the output of the shunt current monitor) were recorded. This situation is to assess the ability of the system to share the load equally between each of the harvesters, in terms of their generation capacity. The TEG was put under $\Delta T = 60$ °C and both solar panels were subjected to illumination 3. The load current was varied as follows:

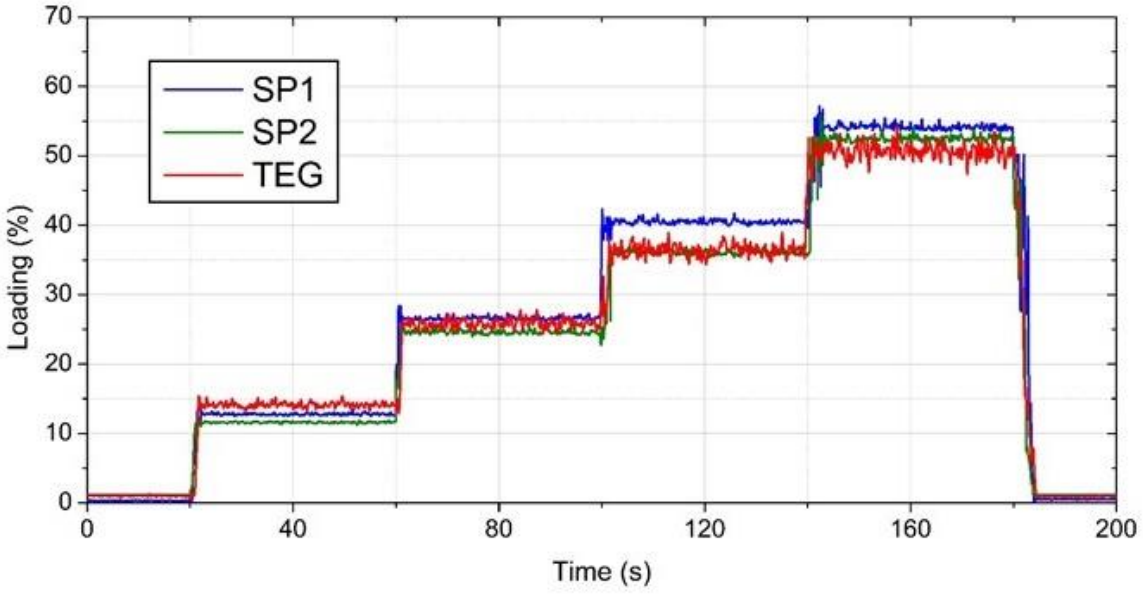
1. From T = 0, the load current is set to 0 mA (no load condition).
2. At T = 20 s, the load current is increased to 5 mA.
3. At T = 60 s, the load current is increased to 10 mA.
4. At T = 100 s, the load current is increased to 15 mA.
5. At T = 140 s, the load current is increased to 20 mA.
6. At T = 180 s, the load current is reduced to 0 mA (no load condition).

The results for the bus voltage, current from TEG, current from solar panel 1 (SP1), and current from solar panel 2 (SP2) are shown in Figure 2.32 (a). As can be seen, at all times when there was a current flowing to the load, all converters simultaneously worked together to supply this current. This is the main feature that differentiates this system with the typical OR-ing configuration implemented in most of the parallel converters system discussed at the beginning of this chapter. Although the total current from all converters was a bit higher, it was almost equal to the magnitude of the current flowing to the load. Similar to the previous tests, a steady state error can be observed in a no load condition. In order to accurately determine the loading of the converter for each of these conditions, the loading factor in terms of percentage of current from the maximum current for each converter is shown in Figure 2.32 (b). The loading almost matches perfectly for all converters, with a maximum sharing error of 5 %. The small deviations, even for the same two solar panel systems, can be attributed to the presence of parasitic resistance, capacitance, and inductance in the constructed circuits. In this experiment, the circuit was constructed on a stripboard and each connection was soldered manually. The

inconsistency arises from the layout of the circuits and soldered connections give rise to the variation of different parasitic factors which contributed to these variations. Furthermore, the error could be contributed from the error in the output of the current shunt monitor. Overall, this test validates the ability of load sharing in terms of generation capacity of the harvesters. The DC bus voltage was also determined to match the loading of the system, ≈ 2 V at 50 % loading.



(a) Magnitude of bus voltage and current for each converter with the variation of load current

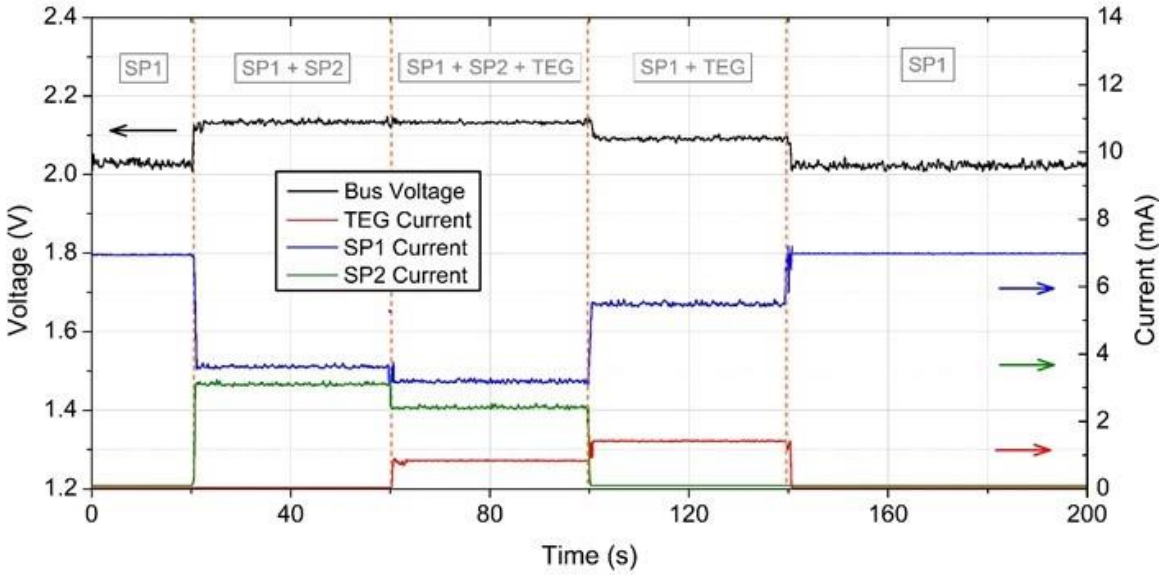


(b) Loading for each converter with the variation of load current

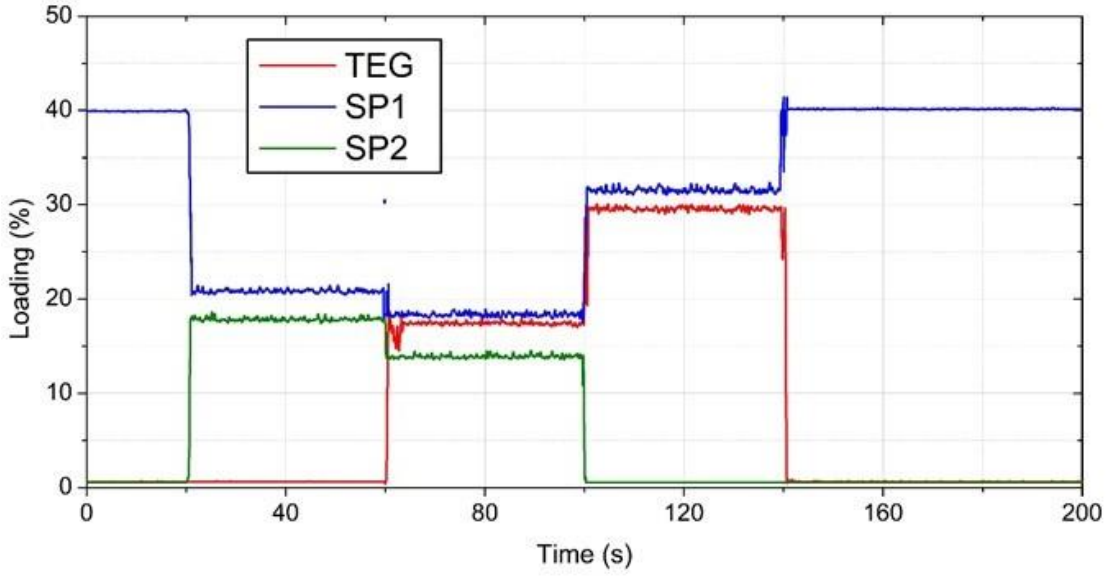
Figure 2.32: Results from the test in case 1.

2.4.3 Case 2: Plug-and-play (PnP) Demonstration

In case 2, SP1 was always connected to the load however SP2 and TEG were switched on and off to mimic the action of plug-and-play-ing whilst the current demand was maintained at 7 mA. This situation is to assess the plug-and-play capability for the source converters in the system. The TEG was put under ΔT = 60 °C and both solar panels were subjected to illumination 3.



(a) Magnitude of bus voltage and current for each converter with the variation of on/off status for each source converter



(b) Loading for each converter with the variation of on/off status for each source converter

Figure 2.33: Results from the test in case 2.

The connection was varied as follows:

1. From T = 0, only SP1 was switched on.
2. At T = 20 s, SP2 was switched on.
3. At T = 60 s, TEG was switched on.
4. At T = 100 s, SP2 was switched off.
5. At T = 140 s, TEG was switched off.

The results for the bus voltage, current from TEG, current from solar panel 1 (SP1), and current from solar panel 2 (SP2) are shown in Figure 2.33 (a). As can be seen, whenever a converter was switched on, the load current was automatically shared between the switched converter and also the existing converter. When a converter was switched off, the current from all the online converters in the system increased to cover the sudden dip in the current level. Similar as before, the loading factor in terms of percentage of current from the maximum current for each converter was determined and is shown in Figure 2.33 (b). The loading almost matches perfectly (with a maximum error of approximately 5 %) for all converters hence validating the ability of load sharing in terms of generation capacity of the harvesters and also the plug-and-play capability.

A few important observations from these two cases include:

- The system can ensure that the load is shared equally between the source converters. With the variable droop, this means that the load is shared equally in terms of the generation capacity/rated power of the harvesters. The sharing accuracy relies on the accuracy of the voltage droop to follow the variation of the input power, *i.e* the accuracy of the resistance of the LDR and thermistor.
- Plug-and-play capability for the source (increase/decrease in power sourcing capacity) and load (increase/decrease in power sinking demand) is achieved. At any time, the system possesses an automatic response to the increase/decrease in the system input/output power.
- Bus voltage can be used to determine the loading magnitude in the system. This means that energy storage can be integrated in the system and it can be set to charge and recharge at certain set bus voltage to prevent the system from losing its regulation hence collapsing. For example, when the loading is less than 20 % (bus voltage > 2.12 V), the energy storage can be set to charging mode and when the loading is greater than 80 % (bus voltage < 1.88 V), the energy storage can be set to discharging mode. This means that the bus voltage can be used as an indirect communication channel between all converters in the system, hence

eliminating the need for a complicated communication link for determining the power level in the system.

- However, the bus voltage is not constant due to the droop mechanism, hence there is probably a need for another interface converter for the load side. This will reduce the PCE of the overall system.
- The droop feedback loop is still operated even when there is only a single converter in the system and there is no need for a load sharing mechanism. In this sense, a cut-off function is needed for the droop feedback loop. However, as will be shown in the next chapter, this feature is required to regulate the charging/discharging mechanism for the energy storage.
- The droop feedback loop is still operated when the power produced by the harvester is less than the power consumed by the droop feedback loop. Similarly, a cut-off function is needed for this.

2.5 Summary

In this chapter, the concept of load sharing among power converters for multiple and multitype energy harvesters was discussed and the voltage droop method was proposed to be utilised as the load sharing mechanism for the parallel operation for these DC-DC converters. This method does not rely on the typical master-slave configuration and does not require any communication links between the control circuitry for each converter, hence the system configuration is simplified and therefore is suitable for low power applications.

From the characterisations of the solar panel and TEG used in this thesis, the expected output power, voltage, and current were determined and power converter COTS ICs were selected to provide the required regulation. Since these ICs possess an input feedback loop based on a pre-set resistance value for the MPP regulation, a resistor value whose resistance vary with the input power needs to be used. For this, LDRs were used for solar panel and thermistors were used for TEG. It was demonstrated that by using the correct variable resistors, a satisfactorily MPP extraction performance was obtained from the feedback regulation loop.

The same concept was further utilised to provide a variable droop regulation for each converter. Since the magnitude of the droop needs to be varied with the variation of input power to ensure that a maximum possible power is capable to be delivered to the load, this variable droop was accomplished through the usage of variable resistors in the droop feedback loop. It was demonstrated that the voltage droop mechanism has been successfully integrated and a satisfactory performance of the variable voltage droop was achieved.

Finally, the circuits were arranged to form a parallel system and the load sharing performance was tested, presented, and discussed. It was shown that the proposed method enables the connected converters to share the load equally between them (in terms of each converter rated power), within 5 % sharing error. Furthermore, the proposed method was also shown to possess plug-and-play capability for both source converter and load. Overall, it was demonstrated in this chapter that this variable voltage droop regulation based on variable resistors does not have high power consumption hence is suitable for low power applications and with the right selection of these variable resistors, a reliable parallel load sharing operation is possible to be achieved. The method presented in this chapter was used as the load sharing mechanism in the proposed pico-grid system.

Chapter 3

Energy Storage and System Operation

3.1 Foreword

In this chapter, the integration of energy storage elements in the pico-grid is investigated, presented, and discussed. Since the nature of the output power of the energy harvesters is sporadic and intermittent, the integration of energy storage elements is a requisite in the system to ensure that a continuous supply of power is available at all times to the load. However, these energy storage elements need to be regulated to allow charging when the power level in the system is high and to allow discharging when the power level in the system is low or depleted to zero. The method to set the charging and discharging mode of these storage elements is presented, tested, and discussed in this chapter. Finally, the overall operation of the pico-grid including start-up, no source and no load condition, and load shedding are discussed.

3.2 Energy Storage Integration

In this section, some background and theoretical aspects of different types of rechargeable battery and supercapacitor are presented. Then, the charging and discharging circuits are constructed based on COTS ICs specifically designed for energy harvesting applications. The performance of these circuits is then presented and discussed. Finally, the method to control and activate the power flow from the DC bus into the storage charging circuit and from the storage discharging circuit to the DC bus based on the power level of the system is proposed and demonstrated.

3.2.1 Rechargeable Battery and Supercapacitor

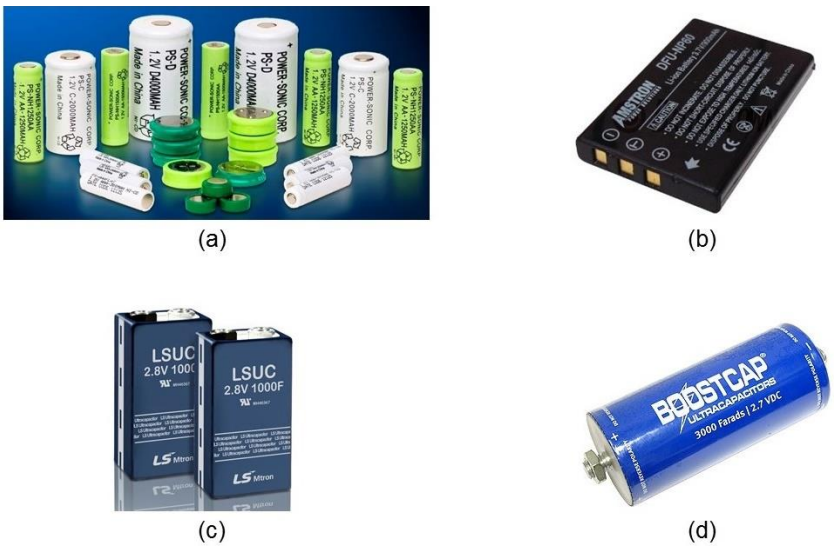


Figure 3.1: (a) Family of Ni-MH battery family. (b) Li-ion battery. (c) 1000F rectangular supercapacitor. (d) 3000F cylindrical supercapacitor. All images were taken from [38]–[41] respectively.

Energy storage is a mandatory element or an ‘enabler’ in the pico-grid system to serve as an energy buffer to continuously meet the power demand of the system load and also to store excess power produced by the energy harvester. A portable and wearable energy storage system is needed, and in most energy harvesting system, a rechargeable battery (RB) is used as an energy buffer. Recently, the use of a supercapacitor (SC) has also been proposed, since a supercapacitor has a faster response to the load variation and will be able to meet the occasional peak power demand of the load, especially the transient power demand when a new load is connected to the system.

RB which can be found in almost all of electronics equipment can be considered as a relatively matured technology, although ongoing researches are still being conducted to further improve the reaction mechanism, structure, and also to explore the possibility of using new chemical substances. Among the most common RBs are Ni-Cd (nickel cadmium), Ni-MH (nickel metal hydride), and li-ion (lithium ion). There are several other types of RB, such as lead acid however they are not suitable to be used in the pico-grid system due to the issues such as excessive weight and low energy density.

- **Ni-Cd** – One of the earliest RBs, therefore is a matured technology and inexpensive. They also possess a very low equivalent series resistance (ESR) that normally limits the current. Considered a ‘tough battery’, they perform well under heavy working condition, and among

other advantages, have a longer lifetime (high charge/discharge cycle) and can be 'slow' (trickle) charged without the presence of a charge termination circuit, provided the charging current falls within the acceptable value. One of the most claimed advantages of Ni-Cd is their flat discharge curve, therefore they act like an ideal voltage source [42]. They offer the best cost *vs.* performance among all of the available RBs. However, they have the lowest energy density and also contain cadmium, which is a toxic substance. Furthermore, they have a high self-discharge rate and high memory effect, thus maintenance/cleaning of the electrode is required after several operations.

- **Ni-MH** - An improvement from the Ni-Cd version, particularly to eliminate the use of toxic substance. Similar to Ni-Cd, they are relatively inexpensive and possess a low ESR. They are also capable of being trickle charged, however their current tolerance is much lower. They have a slightly higher energy density, however it is much lower when compared to the li-ion battery. Their discharge curve is also almost flat. The major disadvantages include high self-discharge and a required maintenance. Overall, they offer almost the same features as Ni-Cd battery, however in an environmentally friendly package.
- **Li-ion** – Often claimed as the most superior RB, they offer improvements on almost all features of Ni-Cd and Ni-MH battery, in particular a much higher energy density, lightweight, no memory effects, and a higher voltage. However, they also have some inherent major disadvantages, such as short lifetime, high ESR, and have a steep discharge curve. The most cited problem with li-ion batteries is that they are very fragile, therefore they require a safety cut off function during charging, to prevent overheating or even exploding [43]. A variation of the li-ion battery, li-ion polymer RB has also been proposed, which offer improvements from the current li-ion battery, particularly being much safer and less fragile.

Overall, in most portable electronics applications, li-ion battery is the preferred option since the most important factors are being lightweight and having a high energy density. Although the safety aspect is the main concern, this can be eliminated by integrating a safety cut-off function in the charging circuit. This cut-off function can be triggered by the voltage or temperature of the battery.

In a system where variation of power demand is expected to happen regularly, the usage of a battery will be a major disadvantage since battery 'likes' to work in a constant power environment, and putting battery in a very rigorous fluctuating environment will shorten its lifetime [44]. In order to counter this problem, an SC is proposed to enter the system and supply

the load first, and the RB is only used to supply the load when the power from the SC is not capable to supply the full load demand. Since SC stores its energy in the form of electrical charge, its stored power can be released in a short time. Furthermore, as with discharging, SC is also able to charge from any impulse power, thus making them suitable to capture even a short impulse of current for storage, although this feature will be hindered by the charging circuit. Moreover, SC also possesses an almost infinite charging-discharging cycle, and unlike battery, theoretically they can perform for eternity. These features make them a perfect complement for RB to be implemented in the pico-grid system. Among other advantages are very low ESR, small in size, have a high charging efficiency, and are environmentally friendly. However, they suffer from high self-discharge rate and have a linear discharge voltage profile [45]. Due to this linear discharge profile, the integration of a power converter to regulate the output voltage from the SC is needed. Different types of SC exist such as electrochemical double layer capacitor (EDLC) and pseudo capacitor [46]. Appendix 2 summarises the characteristics of different types of RB and SC.

A system that incorporates both RB and SC is not new, in fact most hybrid electrical vehicles (HEV) utilise this storage system, in order to provide a storage mechanism that is capable to capture impulse power from the regenerative braking and to provide intermittent power support. These are presented in numerous publications, for example Lerman *et. al.*[47] and Sefik *et. al.* [48] have proposed and presented a battery-supercapacitor energy source system for HEV. In energy harvesting applications, Jia *et. al.* [49] for example have proposed the same system to be implemented in a renewable energy application to prolong the battery life and to also capture as much power as possible.

(b) ENIX Energies 3.7V 1840mAh Rechargeable Lithium Battery Pack

(b) Vishay 15F Supercapacitor EDLC 196 HVC Series 4.2V dc Through Hole

Figure 3.2: Rechargeable battery and supercapacitor used in this thesis.

In this thesis, the RB used is a 3.7 V rechargeable li-ion battery pack manufactured by Enix Energies with a capacity of 1840 mAh. This battery pack can be charged at a maximum current of 2 A and has its own built-in circuit protection. The SC pack used comprises three units of

15 F 4.2 V EDLC supercapacitor manufactured by Vishay Electronics connected in parallel to boost the storage capacity.

3.2.2 Charging and Discharging Mechanism

The RB and SC each require a dedicated charging circuitry to ensure that they are being charged with the correct magnitude of current and voltage, below the maximum values as specified by the manufacturer in order to ensure that the quality of the storage elements is not compromised or deteriorated. On top of that, this charging circuitry should also be able to stop the charging process when the storage elements have been fully charged to prevent overcharging. Since the output voltage of these storage elements are varying and not necessarily equal to the required input voltage for the load, the addition of a voltage regulation circuit on the output side of these storage elements becomes necessary for the discharging condition. In this section, the interface circuitries for these purposes are presented, tested, and the performance is discussed.

a. BQ25504 for Battery Charging

The main challenge with a li-ion battery is it cannot tolerate overcharging, otherwise the safety aspect will be compromised. State-of-charge (SOC) of a li-ion battery is defined as the available amount of energy in a battery expressed in a percentage (0 % is fully discharged/empty and 100 % is fully charged/full). Several methods are used to estimate the SOC of a li-ion battery, with the open circuit voltage (OCV) being the most common indicator of SOC used in portable electronics applications. This method is very simple yet reliable. However, this method also possesses some drawbacks, such as a strong dependent factor of the OCV on the temperature, discharge rate, and the age of the battery [50]. Several other methods have also been proposed to determine SOC, such as specific gravity (SG) measurement and internal impedance measurement [50], however the complexity of the measurement circuits outweighs the benefit of the improved estimation accuracy. With an accurate SOC estimation based on OCV sampling, the charging mechanism can be safely designed to prevent the battery of being overcharged. This method is particularly preferred in low power applications since only a single voltage feedback loop is required for the charging cut-off function, hence reducing the complexity and power consumption of the control circuitry.

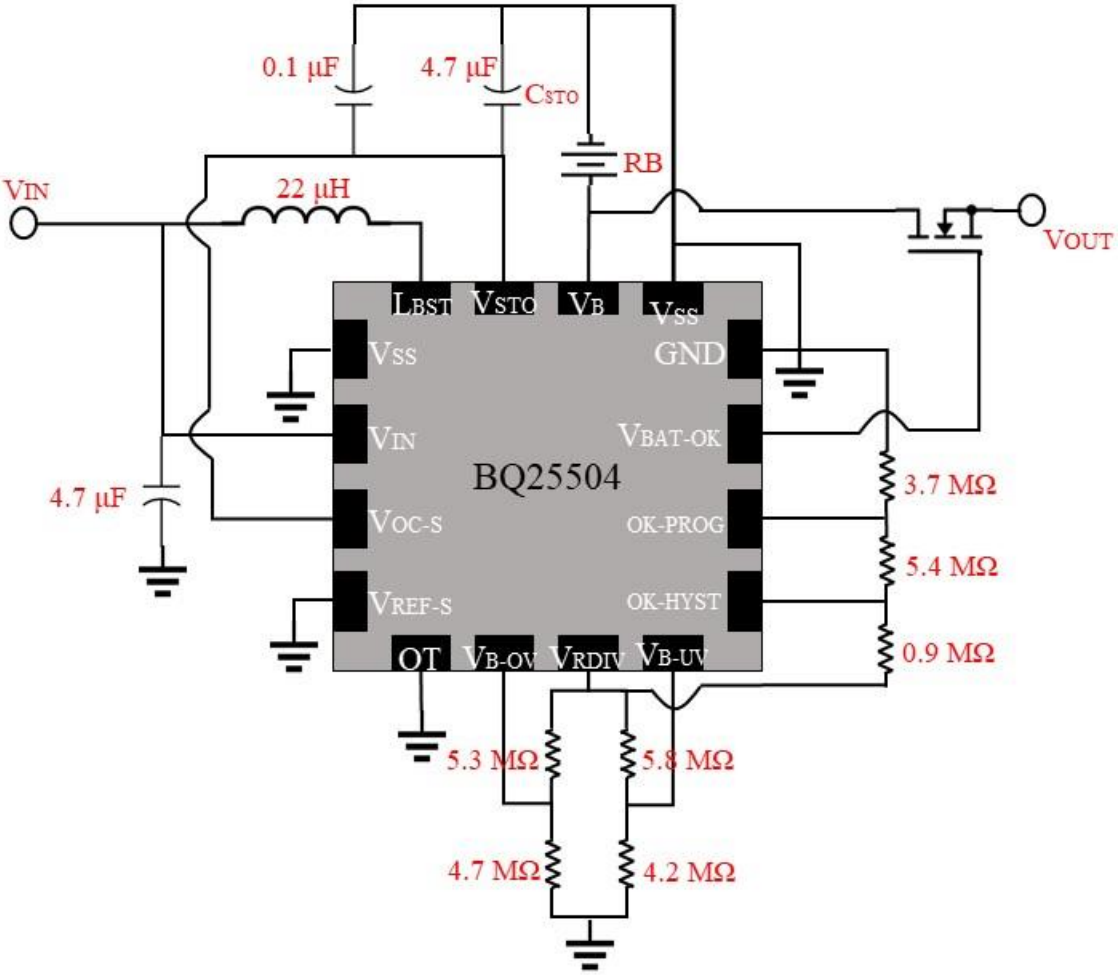
The most common way to charge a li-ion battery is the constant current constant voltage (CC-CV) method. In this method, there are two main stages of the charging process, the first stage is to charge the battery at a constant high current and wait until the voltage of the battery reaches a pre-determined voltage, and the second stage is to charge at a constant voltage and wait until

the current decreases to a certain pre-determined level, where the charging process will be terminated [51]. To prevent the battery being discharged over time when not in use, the battery will be trickle charged with a very low current. In low power applications with irregular charging rate and unavailability of high current source such as in energy harvesting applications, Buchmann [52] suggested that the battery can be charged at a varying current until the voltage of the battery reaches a pre-determined value (essentially similar to first stage of the CC-CV charging) and the charging process can be cut off (normally SOC is at 85 %). He suggested that this method, which is known as charge and run, will prolong the lifetime of the battery. It is also important to prevent a li-ion battery from reaching 0 % SOC, since this will significantly degrade its performance. To prevent this, in most applications there is a cut off mechanism when the voltage of the battery reduces to a pre-determined low threshold limit.

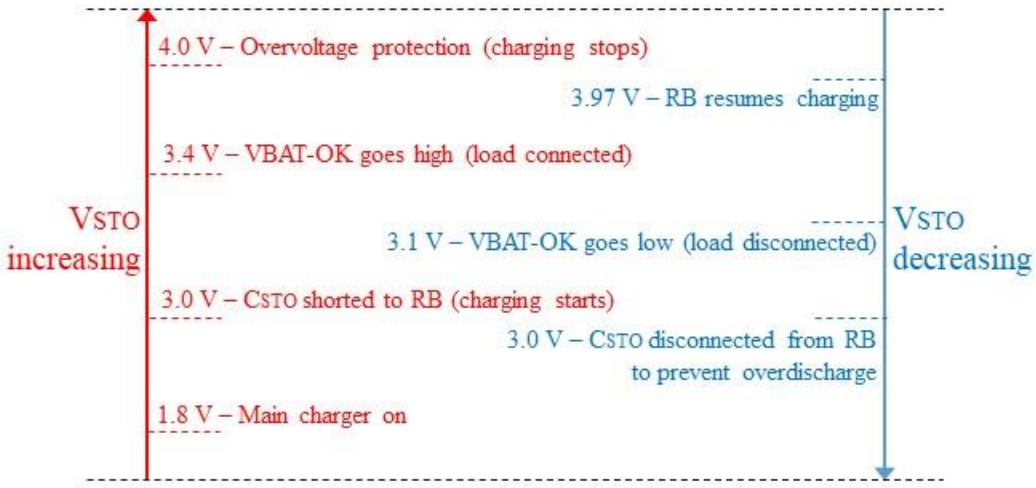
Considering all these factors, a low power battery charger and battery management IC specifically targeted for energy harvesting applications manufactured by Texas Instruments; BQ25504 was selected. This IC is capable of starting-up from an input voltage as low as 330 mV and has a very low consumption quiescent current (< 330 nA). The constructed circuit is shown in Figure 3.3 (a). By referring to this figure, the operation of the IC is explained; initially when the IC is connected to a source with an input voltage greater than 330 mV, an internal low efficiency hysteretic boost converter is cold started to charge the C_{STO} to 1.8 V. When the voltage of C_{STO} reaches 1.8 V, the main boost charger circuit is on and when the voltage of C_{STO} reaches the minimum set voltage (the minimum voltage of the battery to prevent overdischarge) of the RB, the C_{STO} is shorted to V_B to start the charging process. When V_B reaches the pre-set voltage value higher than the minimum RB voltage, the VBAT-OK signal is turned high, shorting the RB to the load. If V_B keeps increasing and reaching the maximum set voltage (the maximum voltage of the battery to prevent overcharge), C_{STO} is disconnected from V_B to stop the charging process. If V_B decreases to the pre-set voltage value, then the VBAT-OK signal is turned low, disconnecting the RB from the load. The operation of the IC is further summarised in Figure 3.3 (b) with the selected voltage level.

The circuit was then tested to evaluate its performance. The input side is connected to a constant 2 V voltage source mimicked by a Keithley Sourcemeter. The charging process ran for 4000 seconds and the charging current and RB voltage were recorded. These are shown in Figure 3.4. From this figure, it can be observed that there is a small increase in the RB voltage from 3.81 V to 3.82 V from the start to the end of the charging process. A constant charging current

of approximately 18.7 mA was continuously supplied to the RB, and is suspected to be limited by the IC itself, the internal resistance of the RB, and the connection from the IC to the RB.



(a) Charger circuit based on BQ25504



(b) Voltage programmed level

Figure 3.3: Circuit configuration and voltage programmed level for BQ25504.

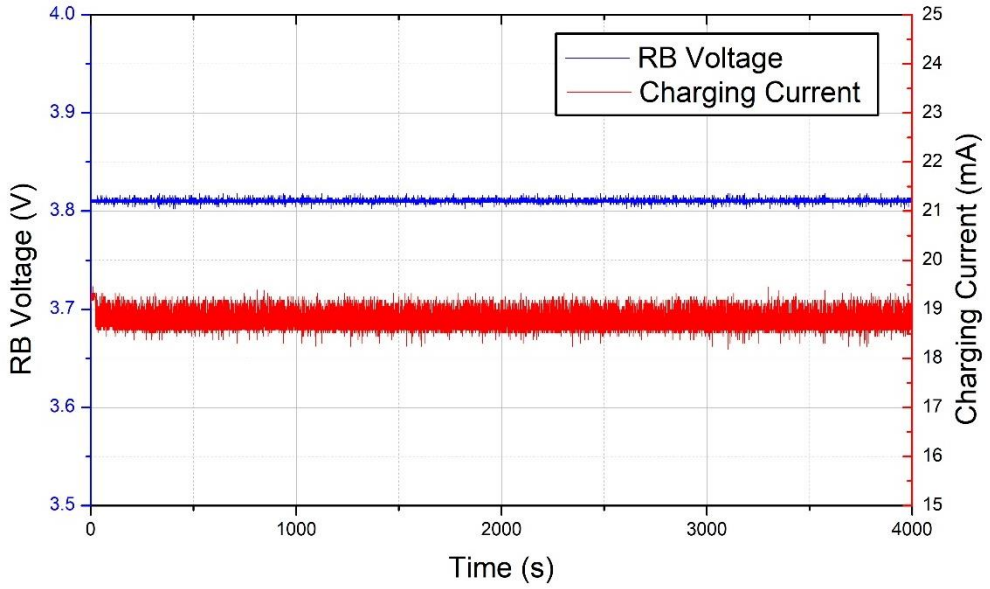


Figure 3.4: Charging profile of the constructed circuit.

The charging process and the RB voltage was rising extremely slowly due to the low level of the charging current and the high capacity of the RB (1840 mAh). The charging current was extracted from a current sensor constructed from a current shunt monitor with a very small precision resistor (0.2 Ω) and it can be observed that the data obtained from this sensor is quite noisy due to this low resistance value. From the voltage and current data from the input and output sides, the efficiency of the converter during the charging process was determined to be 84 %, which is the expected value from the datasheet.

b. LTC3105 for Supercapacitor Charging

Unlike RB, the SC charging process is simpler and as long as the SC is not being charged at a voltage greater than its rated voltage, then the charging process is safe. This means that if the SC is being charged by a voltage source, the voltage source needs to have an output voltage that is lower than the SC rated voltage. If the SC is being charged by a current source, then the SC voltage needs to be monitored for the charging process to be terminated.

The same DC-DC converter IC used for TEG in the previous chapter was used as the charging circuit for the SC. The output voltage was set (4 V) to be slightly below the rated voltage of the SC (4.2 V) as a safety margin. The circuit constructed is shown in Figure 3.5. The limiting resistor (R_{LIMIT}) was put in series with the SC to limit the charging current of the SC, which could go be incredibly high during the charging process. The R_{LIMIT} value was chosen to be 22 Ω. Similar as before, the IC was then supplied from a constant 2 V voltage source mimicked by a Keithley Sourcemeter and the charging process was run for 2000 seconds.

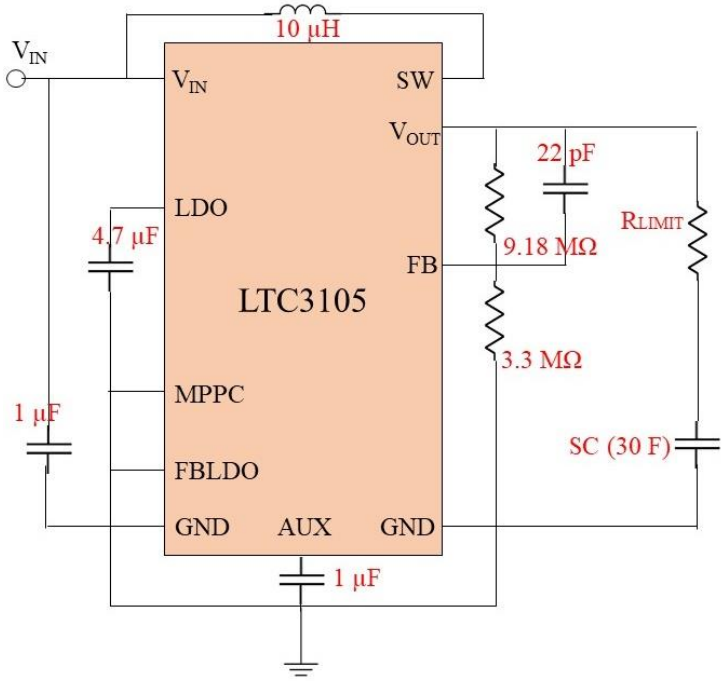


Figure 3.5: Charging circuit for SC.

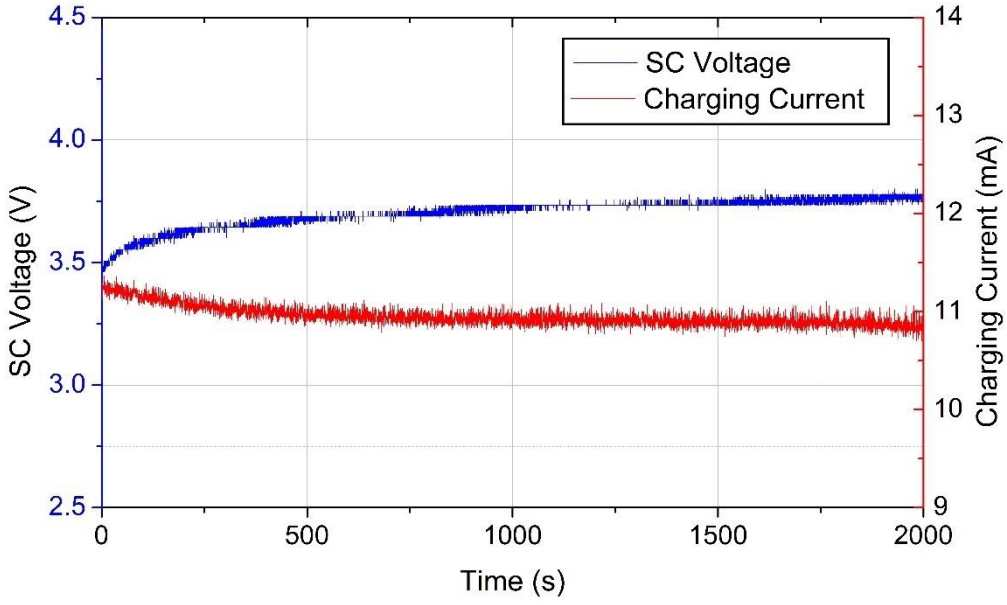
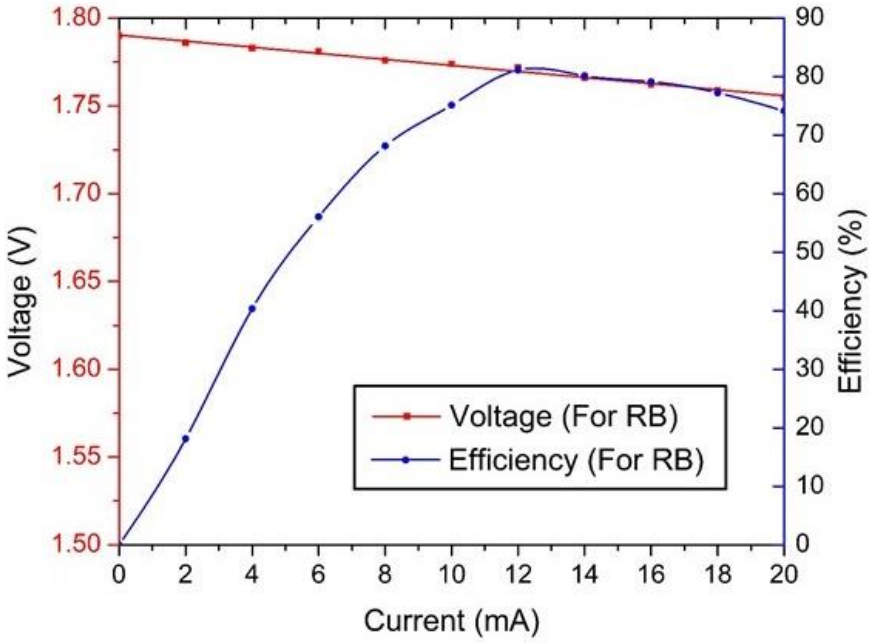


Figure 3.6: Charging profile for SC.

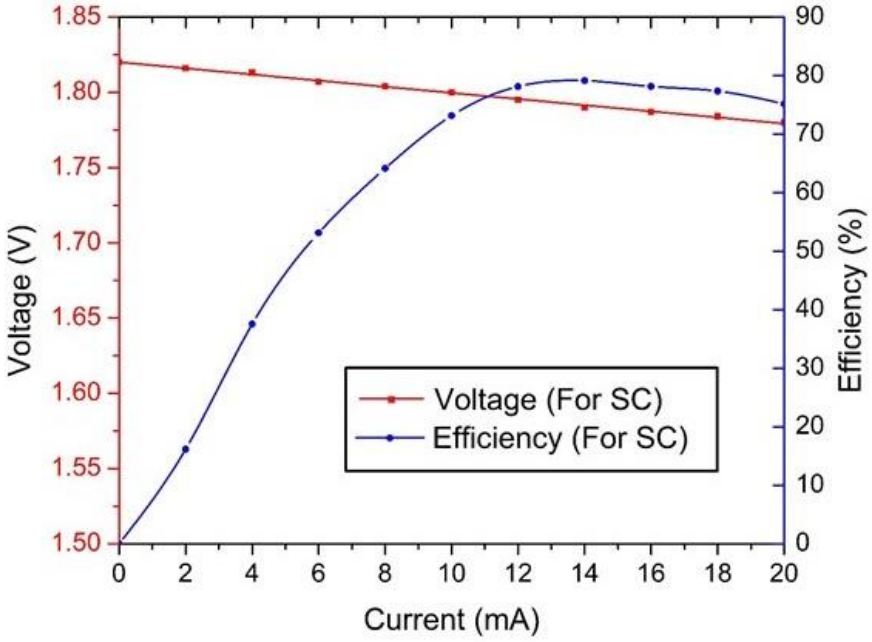
The charging profile for the SC is shown in Figure 3.6. It can be observed that the voltage of the SC is increasing during the charging process from 3.48 V to 3.75 V, signifying a successful charging operation. During the charging process, the current was decreasing progressively before becoming almost constant (10.8 mA). This is mainly due to the presence of the R_{LIMIT} which limits the magnitude of the charging current. From the voltage and current data from the input and output sides, the efficiency of the converter during the charging process was determined to be at 76 %.

c. LTC3105 for Storage Discharging

The discharging circuits for providing output voltage regulation for both RB and SC were constructed using LTC-3105 IC. The output voltage for SC discharging circuit was set to output a voltage that is slightly higher (1.82 V) than RB discharging circuit (1.79 V). The main reason behind this will be discussed in the next section.



(a) V-I loadline and efficiency for RB discharging circuit



(b) V-I loadline and efficiency for SC discharging circuit

Figure 3.7: Converter loadline and efficiency for both discharging circuits.

Figure 3.7 shows the converter V-I loadline and efficiency for the discharging circuits for both of the storage elements. For the RB discharging circuit, it can be observed that the no load output voltage is equal to the required value (1.79 V) but the voltage begins to droop as the load current increases due to the presence of parasitic output resistance. The efficiency increases in line with increased load current until it reaches a peak before it decreases again due to the significant effect of parasitic resistance loss which would dominate at a high current. The same trends can be observed for the discharging circuit for SC.

3.2.3 Demonstration of Bus Voltage Dependent Mechanism (Mode Select)

As demonstrated in the previous chapter, the bus voltage can be utilised as an indirect indication of the loading magnitude in the pico-grid system. The lower the bus voltage, the higher the load current in the system, hence the higher the loading of the system. Since the charging of the storage elements should only be activated when the load demand is low, and vice versa, the bus voltage can be utilised as the signal to trigger the activation of the charging/discharging mechanism. The proposed voltage level for each mode is shown in Figure 3.8 below.

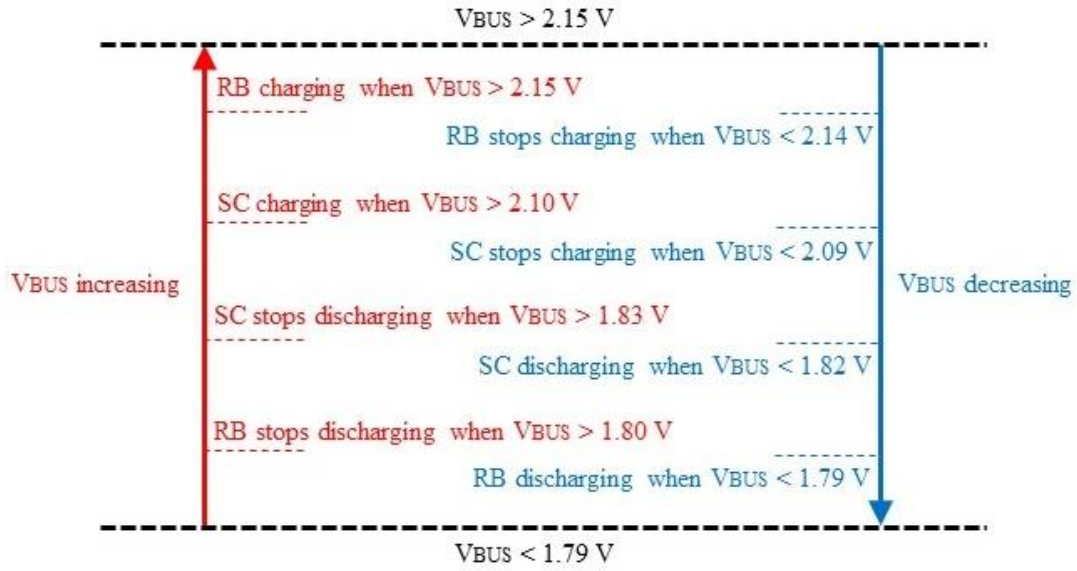
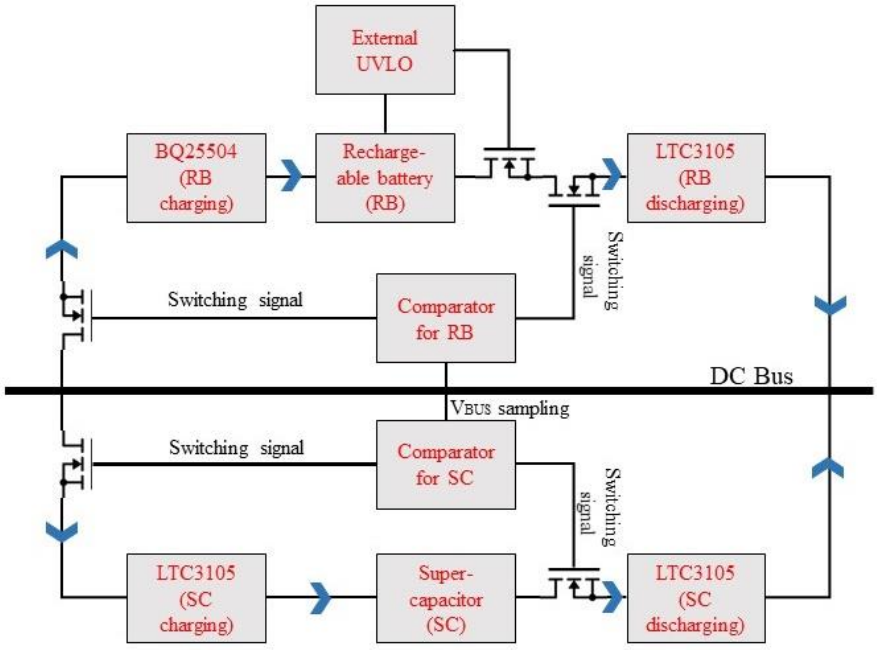


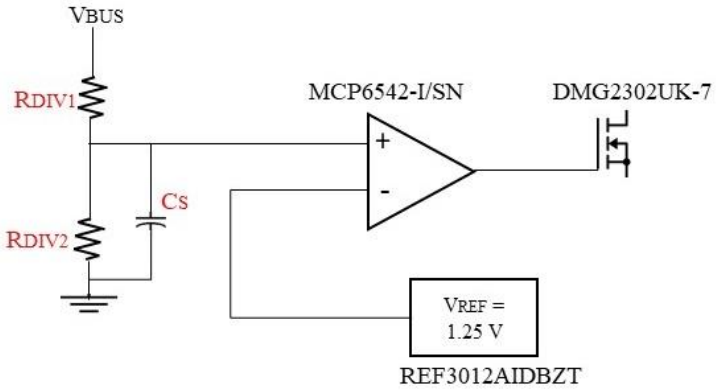
Figure 3.8: Operating mode at each bus voltage level.

For discharging, the SC was set to start discharging when the bus voltage drops below 1.82 V (approximately 95 % loading). Due to this, the output voltage of the discharging circuit of the SC was previously designed to output a voltage of 1.82 V. Since the RB acts as the final power back-up, it should only be discharged when the system reaches a full loading capacity and was therefore set to start discharging when the bus voltage drops below 1.79 V (> 100 % loading, to prevent the bus voltage from collapsing). Similarly, due to this, the output voltage of the

discharging circuit of the RB was previously designed to output 1.79 V. For charging, since the SC was placed at a higher priority for discharging, and to ensure that the power in SC is readily available for discharging, the threshold voltage for the SC charging to stop was put at a higher level than the RB.



(a) System configuration for bus voltage dependent mode



(b) Comparator configuration. R_{DIV1} and R_{DIV2} were selected appropriately for specific voltage. This configuration is for driving switches for storage charging. For discharging circuit, the connections for inverted and non-inverted input pins were interchanged.

Figure 3.9: Configuration for the bus voltage dependent mechanism and the comparator.

In order to integrate this voltage dependent mode mechanism in the pico-grid, the power flow from the bus voltage to the charging circuit and from the storage element to the discharging circuit needs to be regulated. To achieve this, an extremely low resistance n-channel enhancement mode MOSFET was put in this path to act as a switch. The gate of this MOSFET

is driven by an ultra-low power comparator whose one of the inputs is a fixed voltage reference. The other input should be a scale version of the bus voltage (achieved through a proper selection of resistors in the voltage divider circuit). Table 3.1 provides the values for these resistors. A small ceramic capacitor was placed in the input side of the comparator with the voltage divider network to filter any noise and prevent any unnecessary output trigger. Furthermore, the comparators used in this thesis have a built-in hysteresis of 10 mV to prevent any low level noise around the threshold voltage to trigger the output continuously, hence contributing to energy loss. This configuration is shown in Figure 3.9 (a) and the connections for the comparator are shown in Figure 3.9 (b). An additional undervoltage-lockout (UVLO) circuit for the RB was integrated in the output path of the RB. Referring to the charger IC BQ25504 for the RB presented previously, due to the dependence of the VBAT-OK on the V_{STO} and not on V_B, an external UVLO is required to replace the VBAT-OK signal to ensure that the RB is cut-off from the discharging path when its voltage drops below the under voltage threshold limit (3 V), regardless of the value for V_{STO}. This UVLO is not needed for the SC since SC energy can be fully depleted to zero without compromising its storage integrity.

Table 3.1: Value of resistors in the voltage divider network.

Mode	Connection for voltage divider	R_{DIV1} (Ω)	R_{DIV2} (Ω)
UVLO for RB	Non inverting	1.4 M	1 M
RB Charging	Non inverting	720 k	1 M
RB Discharging	Inverting	680 k	1 M
SC Charging	Non inverting	464 k	1 M
SC Discharging	Inverting	440 k	1 M

The power for the mode select circuitry which comprises the comparators and voltage reference was provided directly from the RB (after the UVLO connection). Only one voltage reference IC was used for all comparators. Similar to the discharging path, the power for this circuitry will be cut-off once the voltage of the RB falls below 3 V. It was determined from a quick test that the peak power consumption of the mode select circuitry is at 0.1 mW. The power for the UVLO circuit which is comprised of a comparator and a voltage reference IC was provided by an external coin battery. The system will cease to function if the power of this battery depletes to zero, therefore this can be used as an indirect indication on when to replace this coin battery. The peak power consumption of this UVLO circuit was determined during testing to be at 0.07 mW.

Each of the mode select configuration was individually tested first to ensure that they are switching at the right voltage level. Then, the mode select system for the energy storage system was tested by connecting the common DC bus to a voltage source mimicked by a Keithley Sourcemeter. The voltage source level was varied and the current level for each of the charging and discharging paths was recorded. Figure 3.10 below shows the results from this testing.

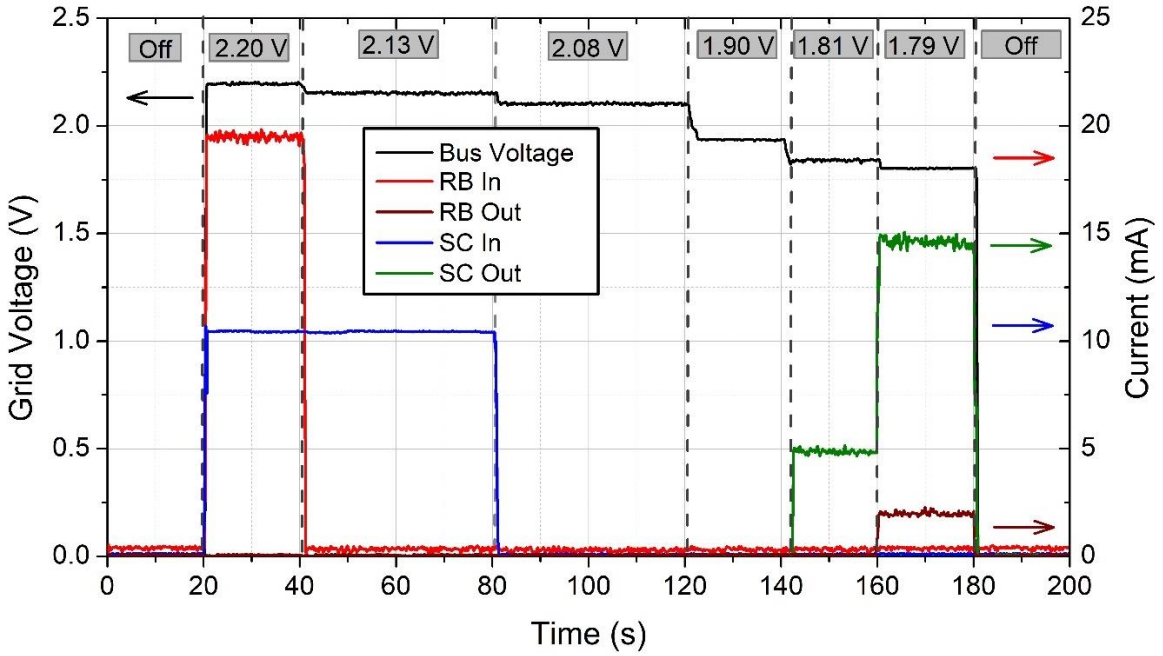


Figure 3.10: Results from the bus voltage dependent mechanism configuration.

As shown in the figure above, when the voltage source level was initially set at 2.20 V, both of the charging circuits automatically switched on to enable charging for the storage elements. When the voltage source level was dropped to 2.13 V, the charging circuit for the RB switched off since the bus voltage level was lower than the threshold voltage set for the charging circuit. When the bus voltage was further reduced to 2.08 V, the charging circuit for the SC switched off. At 1.81 V, it was observed that the discharging circuit for the SC was activated and the current started to flow from the discharging circuit into the DC bus. Finally, at 1.79 V, the discharging circuit for the RB was activated and both the SC and RB were discharging to the DC bus. In addition, it was also observed that the levels of the discharging current for both SC and RB are in good agreement with the converter loadline obtained in Figure 3.7. This also indicates that in real applications, the maximum current for the SC discharging converter is approximately 12 mA (approximated from Figure 3.7) before the converter voltage drops to 1.79 V, hence activating the RB discharging circuit. Overall, from this test, it can be concluded that the voltage dependent mode for the charging and discharging mechanism was successfully demonstrated and a satisfactory performance was achieved.

3.3 System Operation

In this final section, various operating modes of the pico-grid corresponding to various situations are presented and discussed. When the first prototype is constructed, it is important to ensure that the operation of the pico-grid runs smoothly and in order to achieve this, some of the important operations such as start-up, no source (energy harvester) condition, and no load (0 A load current) condition are first explored and discussed. Additionally, the load shedding mechanism which is important to prevent the operation of the pico-grid from collapsing due to excessive loading is also investigated.

3.3.1 Start-Up

Although the sources and load in the pico-grid are expected to possess a plug-and-play capability, the energy storage circuitry comprises the RB and SC as presented previously is always expected to be connected to the system. However, extra energy storage elements with a similar mode select operation can be further integrated in the system through the same plug-and-play port. Due to this, the start-up procedure for the pico-grid involves the switching of the storage circuitry, before any load or sources are connected to the system. Figure 3.11 below shows the start-up profile for the pico-grid.

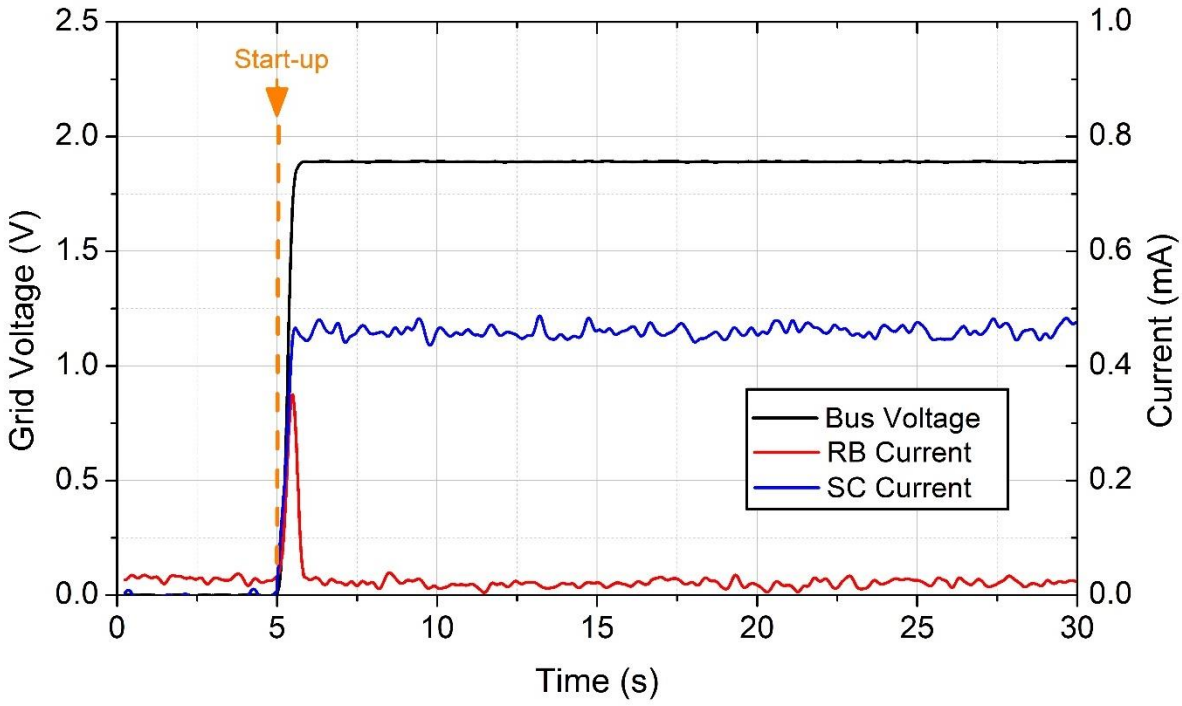


Figure 3.11: Start-up profile for the pico-grid.

As observed from the figure, at t = 5s, the energy storage circuitry was switched on. The circuitry was switched on by switching on the power supply from the coin battery to the UVLO circuit for the RB. If the voltage of the RB is above the minimum threshold limit, then the power supply for the mode select circuit will be automatically switched on. If the voltage is below the minimum threshold limit, then the RB is needed to be externally recharged before the system can resume its operation. If the system still fails to start and the RB voltage is above the threshold minimum, then this means that the power from the coin battery is fully depleted and a replacement is needed. After the UVLO has been switched on and the power was supplied to the mode select circuit, since at this moment, the bus voltage was at 0 V (no sources or load connected to the system), both of the discharging circuits were activated. Due to the output voltage of the SC discharging circuit which was set at a higher voltage than the RB, the bus voltage settled down at this voltage level (1.82 V). The SC would then have a very small discharging current, mainly due to the bus voltage sampling circuit (for the voltage divider network) and also parasitic resistance along the DC bus. The RB discharging circuit was then deactivated since the bus voltage was greater than its designed threshold limit.

3.3.2 No Source Condition

After a successful start-up operation, the system was further tested in a no source condition. In this situation, no source was connected to the system and the load current from the DC bus was increased. The storage elements then acted as the power source to meet the demand of the load current, as shown in Figure 3.12.

Referring to the same figure, it can be observed that the bus voltage was initially at 1.82 V, indicating a successful start-up operation. Then the load current was increased (sinking by the Keithley Sourcemeter) slowly at t = 10s and at 15 mA, the output voltage of the SC discharging circuit dropped to 1.79 V due to the internal droop, hence activating the RB discharging circuit. When the load current was further increased, both SC and RB discharged their current simultaneously to meet the load demand. After careful inspection, it was observed that the output V-I loadline for both discharging circuits is almost consistent with the one obtained in Figure 3.7. The total current from both circuits were greater than the load current, due to the current flow to the voltage sampling circuit. One possible explanation for this is the steady state error introduced by the current sensor used to measure the discharge current in the output path of both converters.

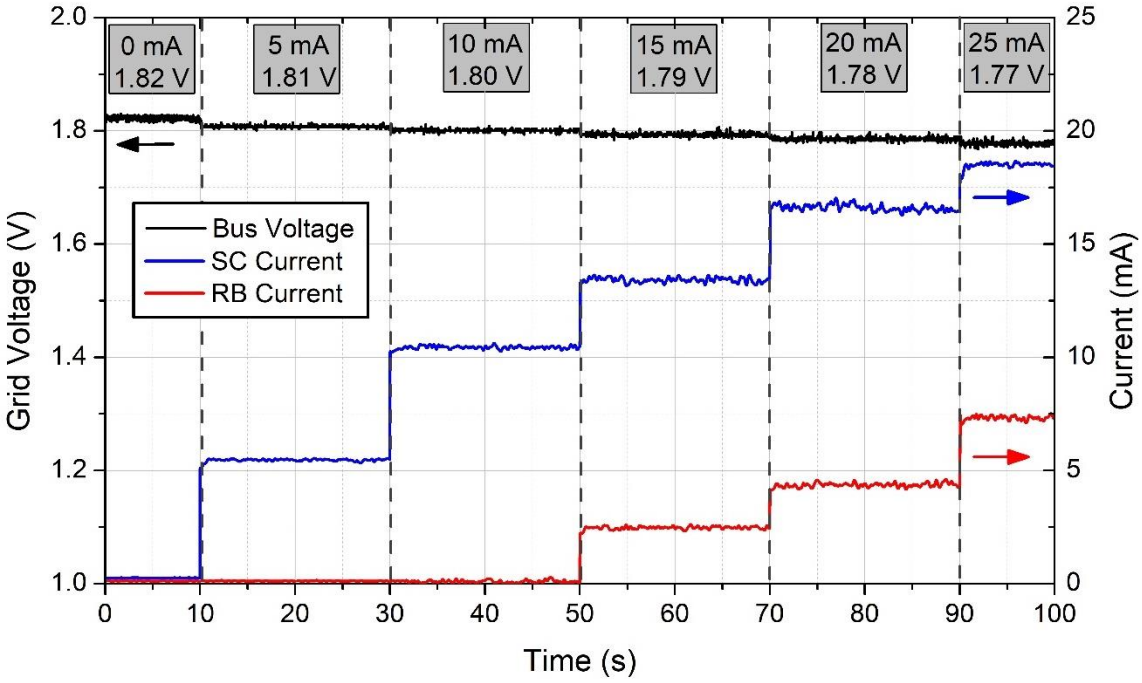


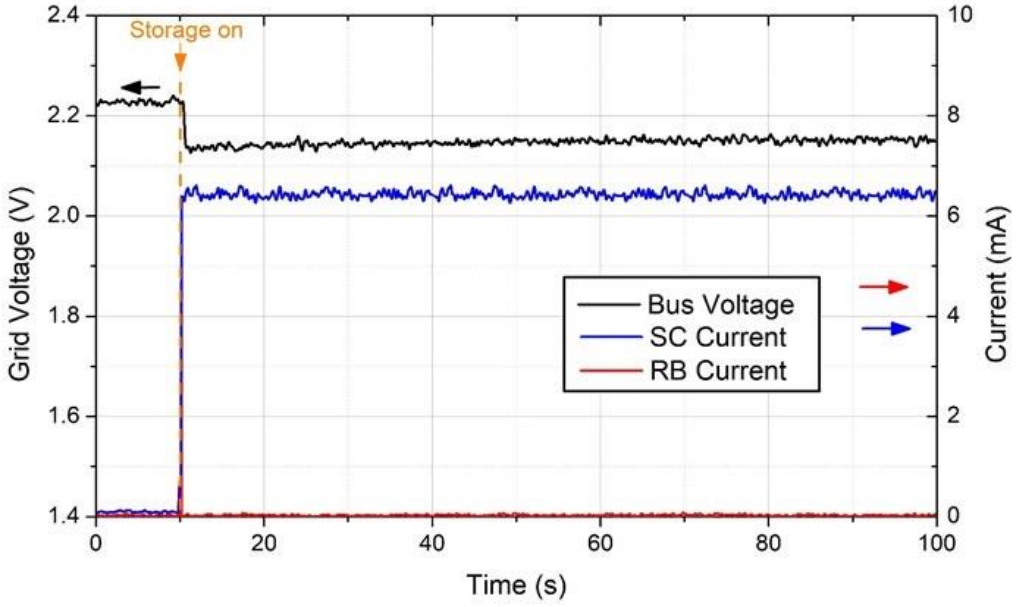
Figure 3.12: No source condition whilst load is connected to the system.

3.3.3 No Load Condition

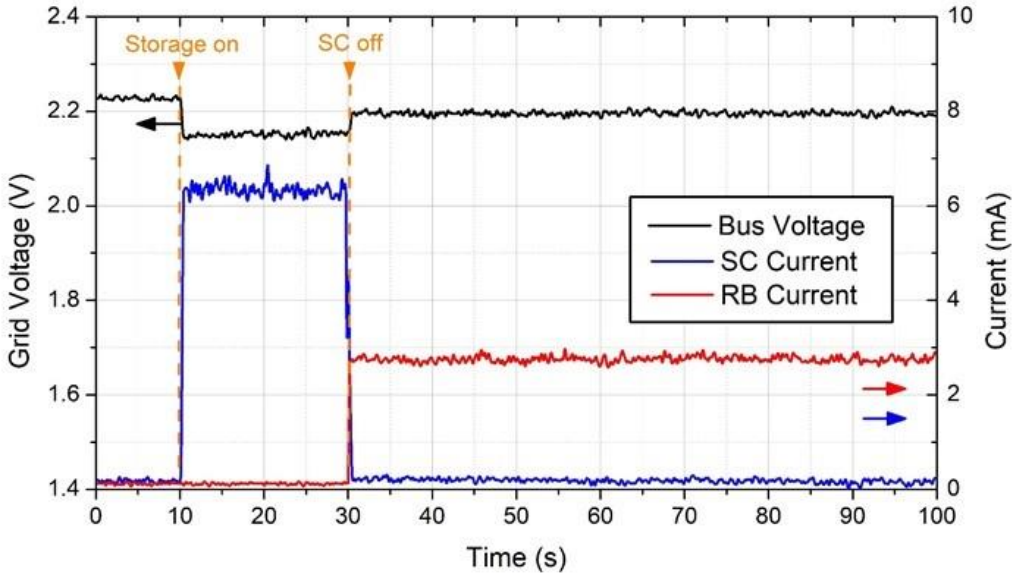
If an energy source is connected to the DC bus after a successful start-up operation (no load), then the mode select circuit will enter a charging mode. To mimic this condition, both SP1 and SP2 were connected to the DC bus. Both panels were subjected to illumination 1. Since the output voltage of the solar panel circuits was both set at 2.20 V (no load), then the bus voltage will be at this level (plus a steady state error). For the sake of data collection, the energy storage circuitry was initially disconnected from the DC bus. Since the charging current previously obtained for both RB and SC were too high, the value of R_{LIMIT} for SC was further increased to 44 Ω and a new R_{LIMIT} of 33 Ω was installed in series with the RB, both to limit the charging current to ensure that the current is within the rated power capability of the energy sources.

Figure 3.13 shows the results from this test. In Figure 3.13 (a), at t = 10s, the energy storage circuitry was connected to the system. It can observed that initially, the charging currents for both SC and RB increased, however after the bus voltage dropped below the threshold voltage for RB charging, the charging current for RB dropped to 0 mA. In order to demonstrate the RB charging mechanism in no load condition, in Figure 3.13 (b), the same test was repeated but at t = 30s, the SC charging circuit was disconnected from the system. During this period, the RB charging mechanism was activated and a small charging current of approximately 3 mA flows to the RB. From this, it can be deduced that it is important for the right value of R_{LIMIT} to be

selected to match the expected rated power from the energy harvesters. In order to further improve the system, it is possible to integrate a mechanism that switches off/alter the voltage droop mechanism in the source converters during a no load condition, in order to maximise the amount of power to charge the storage elements. However, this option is not explored in this thesis.



(a) No load condition and both RB and SC are connected to the system.



(b) No load condition and the SC is disconnected from the bus voltage at $t = 30\ s$.

Figure 3.13: No load condition whilst SP1 and SP2 are connected to the DC bus.

3.3.4 Maximum Load Condition and Load Disconnect (Shedding)

If the loading of the pico-grid is excessively increased beyond the power capability of the energy sources and energy storage, then the bus voltage will drop and then collapse, and the pico-grid will no longer be able to maintain its regulating operation. In order to avoid this, it is important that a load shedding mechanism is integrated in the system, which functions to progressively cut-off the load according to the load priority precedence before the voltage falls below a threshold value. From a test, it was discovered that the energy storage converters will fail to maintain the bus voltage regulation when the bus voltage falls below 1.62 V. This is the absolute maximum loading, therefore the load shedding process needs to start above this voltage level.

The proposed voltage level for the load shedding process to be first triggered is 1.80 V (100 % loading for harvesters). When the bus voltage reaches this level, the least priority load needs to be cut-off from the system. If the bus voltage keeps dropping after the first load has been cut-off, then the second least priority load will be cut-off and so on. The bus voltage should not be allowed to fall below 1.72 V, therefore a main cut-off function is needed to switch off all loads at this voltage level (maximum loading).

The implementation of this load shedding mechanism can be conducted in the same way as the mode select mechanism. A MOSFET can be used to switch the load on/off. Since for this purpose, a normally-on MOSFET is preferred to provide a cut-off mechanism, a depletion mode MOSFET can be used. The implementation aspect is not explored in this thesis.

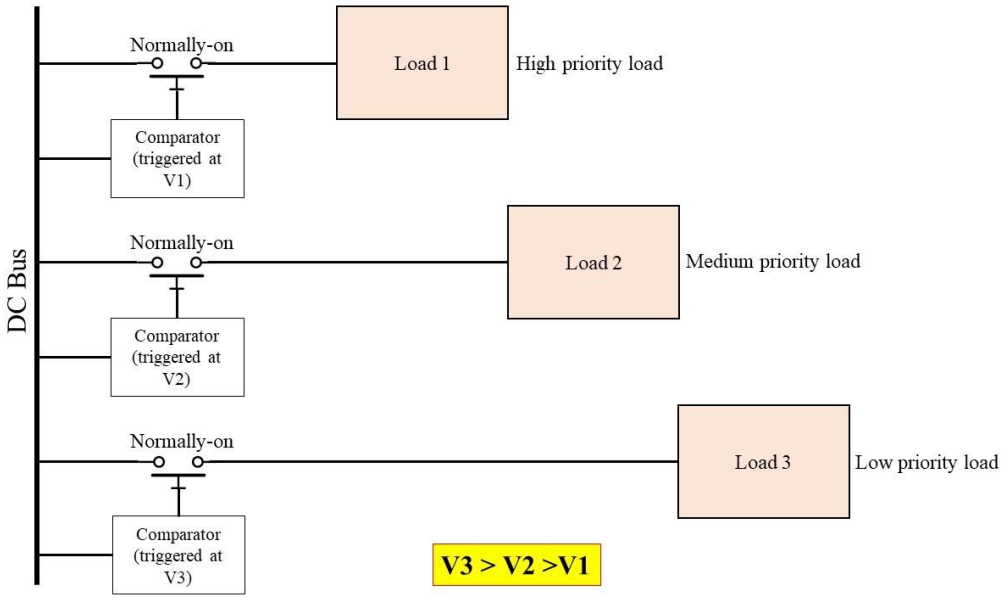


Figure 3.14: Proposed load shedding mechanism.

3.4 Summary

In this chapter, the integration of energy storage elements (rechargeable battery and supercapacitor) in the pico-grid was presented and demonstrated. Since the power from the energy harvesters is not necessarily available at all times, the need for energy storage becomes eminent to support the continuous load demand.

The charging and discharging circuits for these storage elements were presented, tested, and discussed. These circuits which were built from COTS ICs are demonstrated to perform reliably. The mechanism to switch on/off these circuits was also proposed based on a comparator configuration. The comparator was used to compare the bus voltage (loading indication in the system) with a fixed reference voltage and to provide a switching signal to a MOSFET. It was demonstrated that the power consumption of this mode select circuit is very low, hence suitable to be implemented in the pico-grid system. The proposed system was built and the performance was tested. It was demonstrated that a successful mode select operation was achieved.

Finally, to ensure a successful operation of the pico-grid prototype, several operating conditions corresponding to several different scenarios were demonstrated and discussed. It was demonstrated that a successful start-up procedure, no source, and no load conditions were able to be accomplished. A load shedding mechanism to prevent the pico-grid from overloading was also proposed and discussed.

Chapter 4

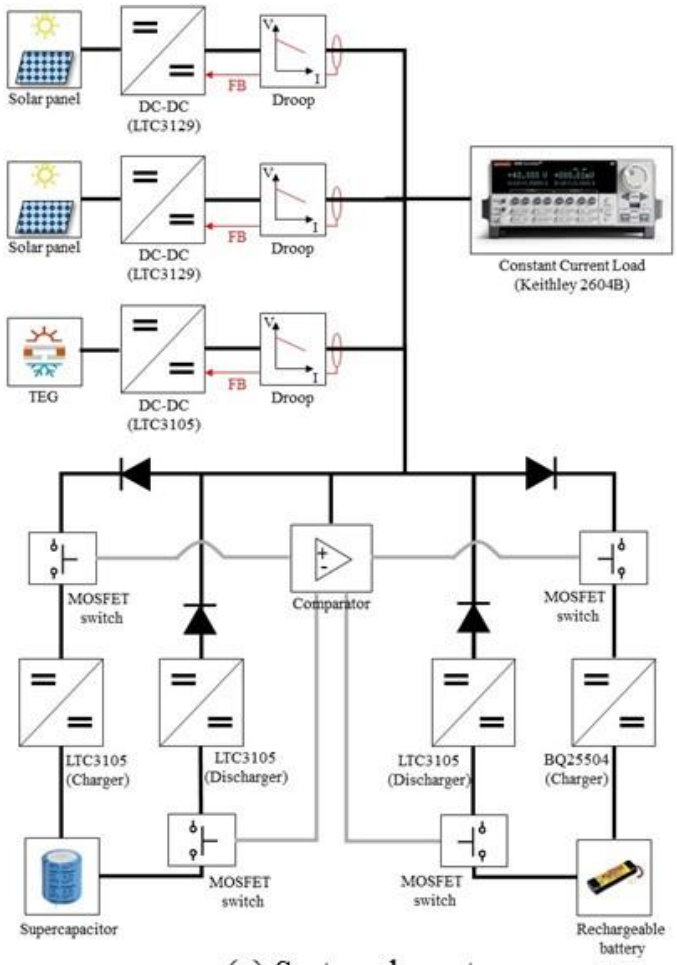
System Integration

4.1 Foreword

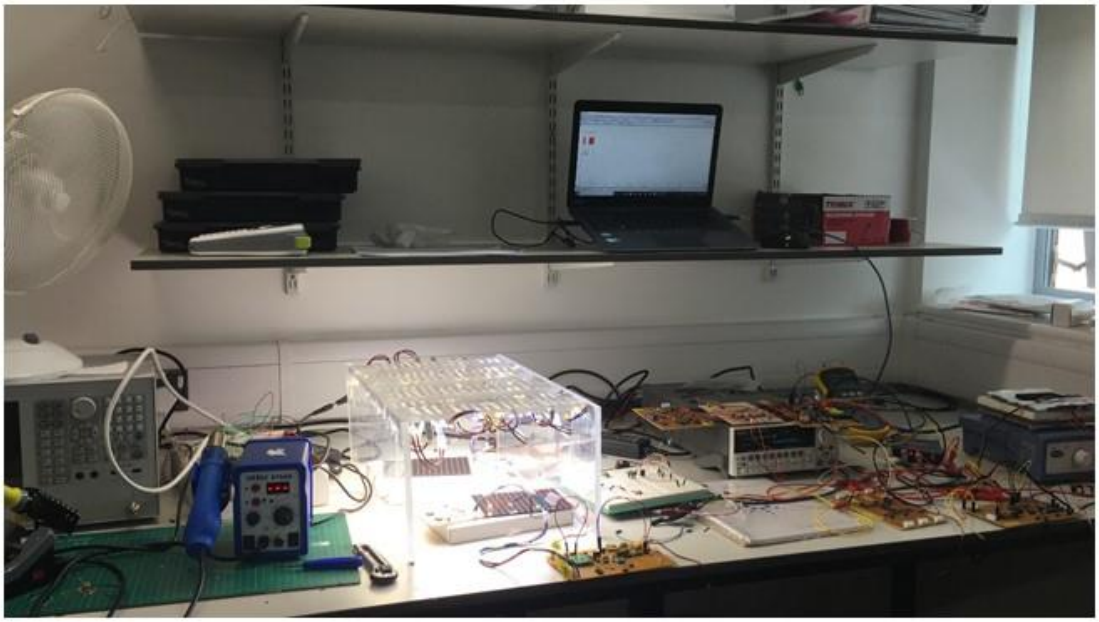
In this chapter, a full system integration is presented and its performance is presented and discussed. The first wearable prototype of the pico-grid is built and the features of the prototype are outlined in this chapter. This prototype is not fully optimised for real world applications hence some recommendations for improvement are presented at the end of this chapter.

4.2 System Integration

The full system layout for the pico-grid is shown in Figure 4.1 (a). The UVLO circuitry for the RB is not shown in the figure. Similar to the previous tests, the load for the pico-grid is a constant current sink mimicked by the Keithley Sourcemeter. The configuration for each of the connected subsystems is similar to the previous chapters, with the exception of the voltage droop circuitry for all of the source converters, in which the power is now directly supplied from the RB, through the same path as the supply power for the mode select circuit. This eliminates the need for a coin battery to power up each of these circuits as presented in Chapter 2. A three pin JST connector was used for all of the plug-and-play ports to the common DC bus; each one is for the DC bus, ground, and power supply for the voltage droop circuity for the source converter (this connection is present however not needed for the load). The test rig for the built pico-grid is shown in Figure 4.1 (b).



(a) System layout



(b) Test rig for the integrated system

Figure 4.1: System layout and test rig for the final system.

4.2.1 Plug-and-play Demonstration

The first test for the integrated pico-grid system is to demonstrate its full plug-and-play capability. In this test, the converters for the SP1 and TEG were disconnected and reconnected to the DC bus and the performance of the system was evaluated. Both SP1 and SP2 were subjected to illumination 2 and ΔT = 50 °C for the TEG. Similarly, the load current absorbed by the Keithley Sourcemeter was varied to simulate the action of plugging and unplugging of load to the system. The sequence of the test carried out is described as follows:

1. At t = 0 s, the start-up procedure commences.
2. At t = 50 s, all energy sources (SP1, SP2, and TEG) are connected to the system.
3. At t = 100 s, the loading for the system (Keithley Sourcemeter) is set to 1 mA.
4. At t = 150 s, the loading is further increased to 5 mA.
5. At t = 200 s, TEG is disconnected from the system.
6. At t = 250 s, SP1 is disconnected from the system.
7. At t = 300 s, the loading is further increased to 10 mA.
8. At t = 350 s, SP1 is reconnected back to the system.
9. At t = 400 s, the loading is further increased to 30 mA.
10. At t = 450 s, the loading is further increased to 50 mA.

The results from the test are shown in Figure 4.2. Each ‘Q’ in the diagram corresponds to the different sequence of the test. The data from the test is also tabulated in Table 4.1.

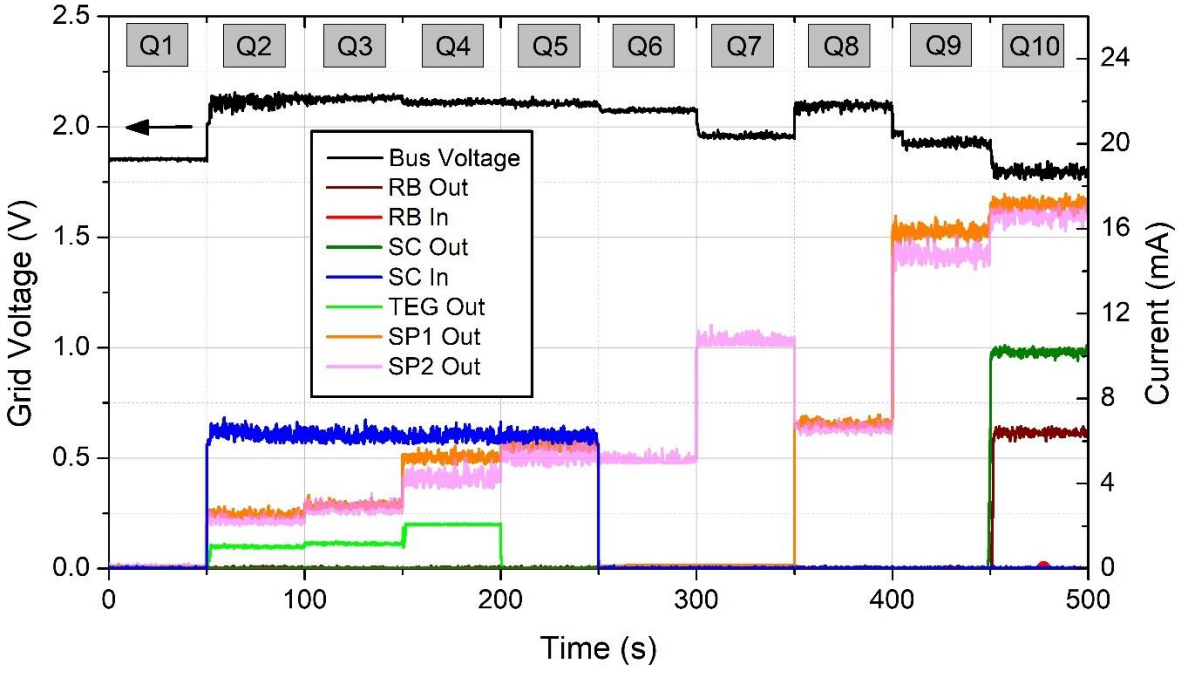


Figure 4.2: Results from the plug-and-play test.

Table 4.1: Data from the plug-and-play test.

Sequence	Status	Bus Voltage (V)	RB Out (mA)	RB In (mA)	SC Out (mA)	SC In (mA)	TEG (mA)	SP1 (mA)	SP2 (mA)
Q1	Storage on	1.82	0	0	0.1	0	0	0	0
Q2	SP1 + SP2 + TEG on	2.14	0	0	0	6.1	1.0	2.7	2.5
Q3	1 mA loading	2.13	0	0	0	6.1	1.3	3.2	2.8
Q4	5 mA loading	2.10	0	0	0	6.1	2.0	5.1	4.2
Q5	TEG off	2.09	0	0	0	6.1	0	5.9	5.2
Q6	SP1 off	2.07	0	0	0	0	0	0	5.4
Q7	10 mA loading	1.94	0	0	0	0	0	0	10.4
Q8	SP1 on	2.09	0	0	0	0	0	5.4	5.0
Q9	30 mA loading	1.86	0	0	0	0	0	15.7	14.9
Q10	50 mA loading	1.77	6.2	0	10.2	0	0	17.1	16.7

A few important observations from this test include:

- Generally, the pico-grid performed as expected. The bus voltage decreased when the loading was increased or the rated input power was reduced, and vice versa. The mode select operation was successfully demonstrated. The system can also perform under several variations of input and output power in the test, indicating a successful plug-and-play demonstration.
- At any point, the total current flowing into the DC bus (from source converters + discharging circuits) was slightly higher than the total current flowing out from the DC bus (to charging circuits + current sink). This slight difference can be attributed to the current flowing into

the voltage divider network for bus voltage sampling. Since the magnitudes of the current were obtained from the output voltage of the current shunt monitor, the slight difference can also be attributed to the steady state error of the current sensor, the inaccuracy of the resistance value used to sample the small voltage drop across the current path, or some noise in the output side of the current sensor. This is further supported by the significant presence of noise in the current waveforms in Figure 4.2.

- From the test, the maximum loading for the source converters (subjected to the test condition) without activating the discharging circuits for energy storage was approximated by the data to be around 40 mA.
- A small discrepancy can be observed between the output current of SP1 and SP2, although the circuit configuration for both of the converters were similar. This could be due to the small discrepancy of the value of resistance for the LDR used in the droop voltage mechanism or the different in the value of resistance in the voltage feedback loop. Also, the illumination incident angle for the solar panel and LDR for each of the converter might not be accurately similar.
- The charging circuit for RB was never activated due to the high threshold voltage set for this mode. Improvements that can be done to ensure the RB is charged include lowering down the threshold voltage or by increasing the R_{LIMIT} for the SC.
- Generally, the measurements data was quite noisy. This could be due to the environmental noise factors or the noise that was present in the oscilloscope or the probe. In all of the tests carried out in this thesis, due to the portability issue, a portable oscilloscope which has a lower quality compared to the typical bench oscilloscope was used. Nevertheless, it was shown that the mode select operation was successfully activated without any issue (in particular with the 10 mV hysteresis, no flickering or oscillation in the output signal of the comparator was observed) hence this confirms that the noisy measurement was mainly due to the equipment issues and not the system itself. The magnitude for each of the data presented in Table 4.1 for each of the sectors was obtained by taking the average of the low pass filtered value (with a cut-off frequency of 1 Hz) of the measured signals.

Overall, a successful plug-and-play operation was accomplished with the pico-grid system. An equal load sharing (with 5 % error) was achieved between each of the source converters in terms of their rated power and it was demonstrated that at full loading, the energy storage was successfully discharged to support the load demand of the system.

4.2.2 Full System Evaluation

After a successful plug-and-play operation has been demonstrated, the next step is to conduct a final test on the performance of the full system when every subsystem is connected to the DC bus. In this test, both SP1 and SP2 were subjected to illumination 3 and ΔT = 38 °C for TEG. The R_{LIMIT} for both RB and SC charging circuits were increased to 47 Ω and 68 Ω, respectively. This was done to reduce the magnitude of the charging currents to better match the rated power rating in the system. The sequence of the final test carried out is as follows:

11. At t = 0 s, all subsystems are connected to the DC bus. The load is set to 0 mA.
12. At t = 50 s, the loading for the system (Keithley Sourcemeter) is set at 5 mA.
13. At t = 100 s, the loading is increased to 10 mA.
14. At t = 150 s, the loading is increased to 15 mA.
15. At t = 200 s, the loading is increased to 20 mA.
16. At t = 250 s, the loading is increased to 25 mA.
17. At t = 300 s, the loading is increased to 30 mA.
18. At t = 350 s, the loading is increased to 35 mA.
19. At t = 400 s, the loading is increased to 40 mA.
20. At t = 450 s, the loading is increased to 45 mA.

The results from the test is shown in Figure 4.3. Each 'Q' in the diagram corresponds to the different sequence of the test. The data from the test is also tabulated in Table 4.2.

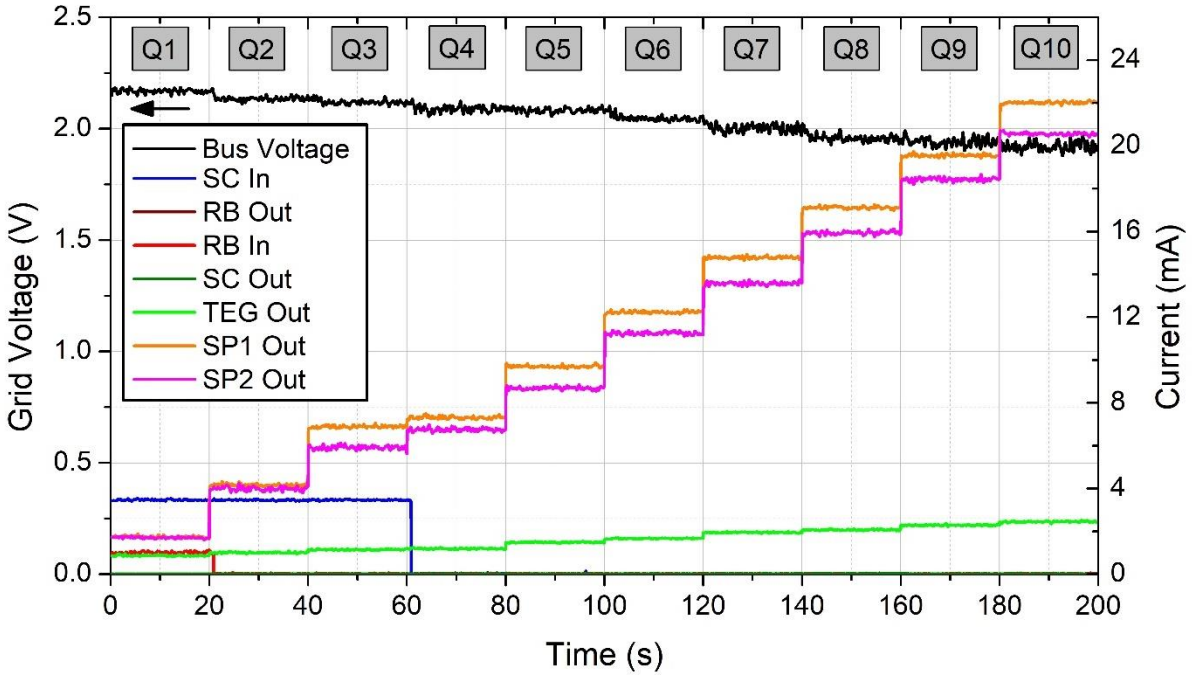


Figure 4.3: Results from load variation test.

Table 4.2: Data from load variation test.

Sector	Status	Grid Voltage (V)	RB Out (mA)	RB In (mA)	SC Out (mA)	SC In (mA)	TEG (mA)	SP1 (mA)	SP2 (mA)
Q1	All on	2.17	0	1.1	0	3.3	0.9	1.8	1.7
Q2	5 mA loading	2.14	0	0	0	3.3	1.0	4.2	3.9
Q3	10 mA loading	2.11	0	0	0	3.3	1.2	6.8	6.1
Q4	15 mA loading	2.09	0	0	0	0	1.2	7.3	6.6
Q5	20 mA loading	2.07	0	0	0	0	1.4	9.9	8.7
Q6	25 mA loading	2.04	0	0	0	0	1.6	12.0	11.4
Q7	30 mA loading	2.02	0	0	0	0	1.9	14.8	13.5
Q8	35 mA loading	1.99	0	0	0	0	2.1	17.1	15.9
Q9	40 mA loading	1.96	0	0	0	0	2.2	19.5	18.3
Q10	45 mA loading	1.92	0	0	0	0	2.4	21.8	20.9

A few important observations from this test include:

- Generally, the pico-grid performed as expected. At each sink current increment, the bus voltage decreased, and the current from each of the source converters increased.
- At any point, the total current flowing into the DC bus (from source converters + discharging circuits) was slightly higher than the total current flowing out from the DC bus (to charging circuits + current sink). This slight difference can be attributed to the same reasons as stated in the previous section.
- With the increase of the R_{LIMIT} for SC and RB, both storages were charged at the start of the test, when the loading of the system was still below the threshold limit set for both charging

circuits. From this, it was demonstrated that the value of R_{LIMIT} needs to be accurately tuned to match the expected rated power of the system. Similarly, the magnitude of threshold voltage for the charging could also be tuned to match the rated power. If this was not done correctly, then there would be a high possibility that the storage would not be charged at all. If the charging current is too high, even in a no load condition, the mode select circuit for the charging converters would be oscillated between on and off.

- From the test, it was observed that at 45 mA, the system still has not reached the full loading capacity. At 1.92 V, the discharging circuits were still not activated. The higher rated power from this test compared to the previous test was due to the higher available power from the solar panels due to the higher illumination level. This confirms the successful operation for the variable droop mechanism as presented in Chapter 2.
- Similar to before, a small discrepancy can be observed between the output current of SP1 and SP2, although the circuit configuration for both of the converters were similar.
- Similar to before, the measurements data was noisy, although in this instance the magnitude of the noise was less severe.
- For this test, the input and output voltage and current for each converter were recorded and from these values, the efficiency of each of the subsystems was calculated. The results are shown in Figure 4.4. The power consumption for the droop feedback/mode select circuitry was considered in the calculations. The efficiency for the charging and discharging circuits are all above 75 %. The efficiency for the source converters are lower, due to the higher power consumption of the droop feedback circuitry. It was determined from this that the power consumption for the current shunt monitor dominates the total power consumption of this circuitry. Generally, the average power consumption for the droop feedback circuitry is 20 times greater than the power consumption of the mode select circuitry (average 2 mW *vs*. 0.1 mW). Furthermore, the presence of a precision resistor across the output current path in each of the source converters for output current sampling also contributed to a higher loss in these converters. Other reasons for the lower efficiency of these source converters have been presented in Chapter 2.

Overall, a successful operation of the pico-grid was demonstrated. From the two tests that were carried out, it was determined that the pico-grid system was ready to be built into the first wearable prototype. The construction and the performance of this first prototype will be presented and discussed in the following section.

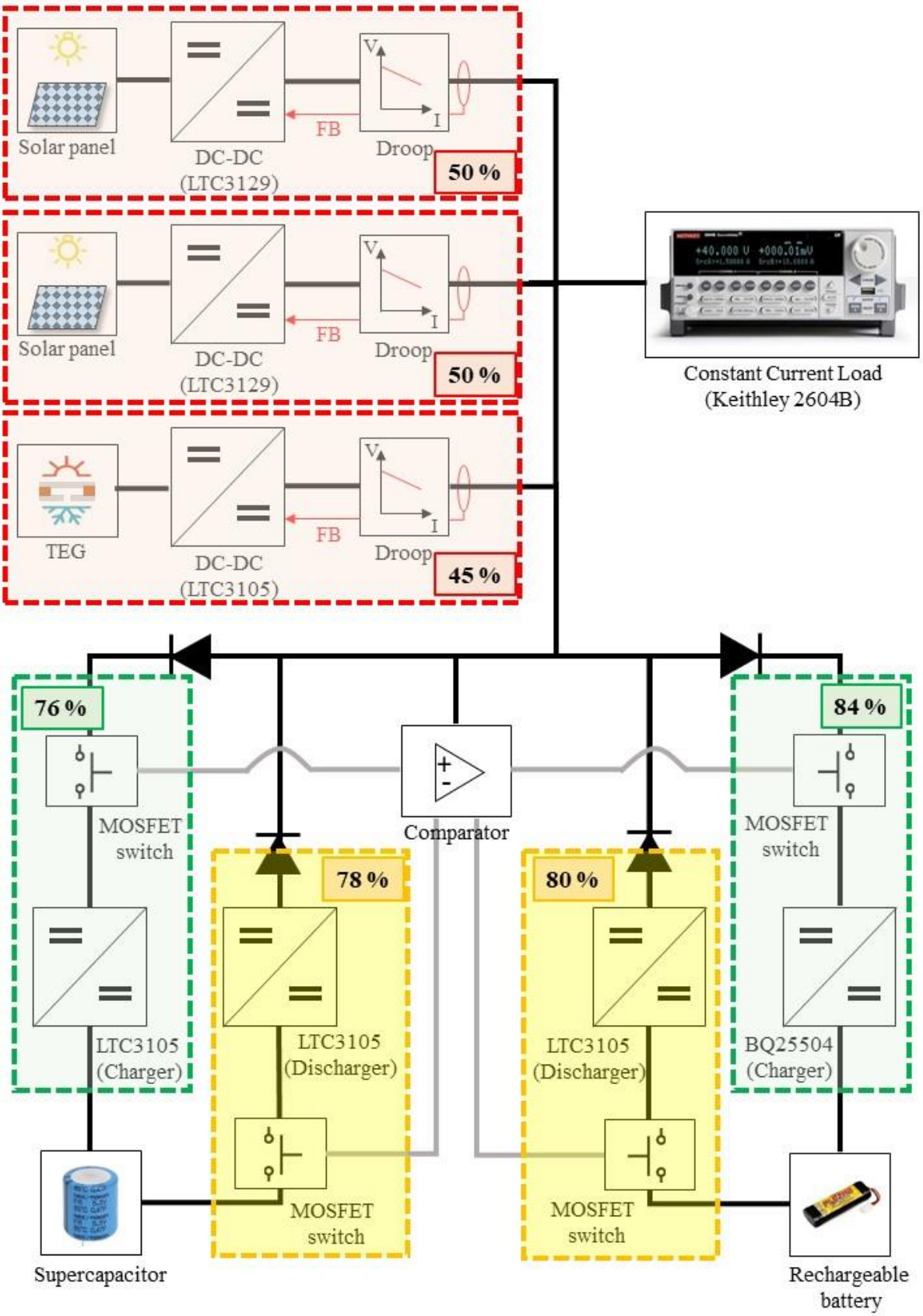


Figure 4.4: Efficiency of each of the subsystems. The efficiency presented here has taken into account the power consumption of the droop/mode select circuitry.

4.3 Wearable Prototype

In this section, the construction of the first wearable prototype is presented and the performance is discussed. Since the first prototype was not optimised for real life applications due to a number of limitations related to the research funding and time constraints, some recommendations for improvement are presented by the end of this section. Although the prototype is still not suitable for real world applications, the aim of this section is mainly to demonstrate the proof-of-concept and the possibility and feasibility for the pico-grid to function in a wearable or portable mode, since the target applications for this system are mainly for WSN and WBAN.

4.3.1 Prototype Construction

Each subsystem circuitry was placed in an enclosure made from acrylonitrile butadiene styrene (ABS) as shown in Figure 4.5. The main purpose for this is to provide an electrical insulation for the circuitry. This is to prevent an excessive electrostatic discharge from destroying the ICs, which are prone to occur when the circuit is attached to a jacket and subjected to the continuous friction between the jacket and the human body. Furthermore, these enclosures also serve as a platform for the circuitry to be attached to a jacket.

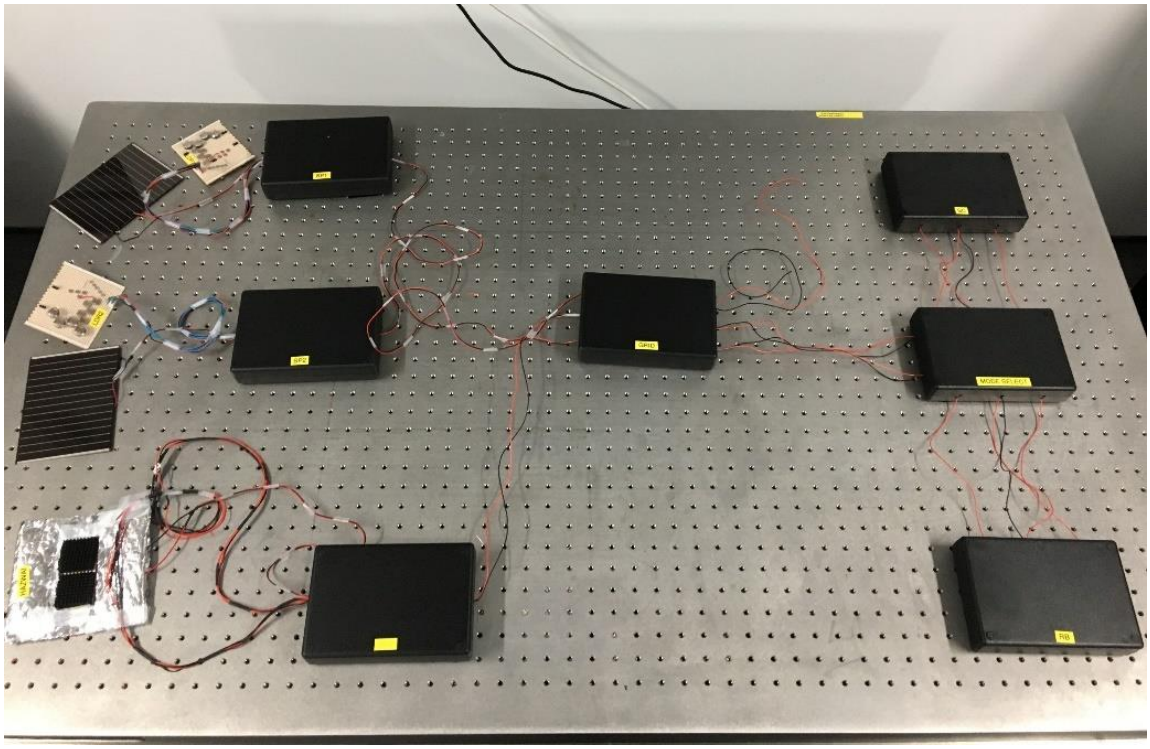


Figure 4.5: The prototype. Each enclosure contains a full circuitry for each subsystem.

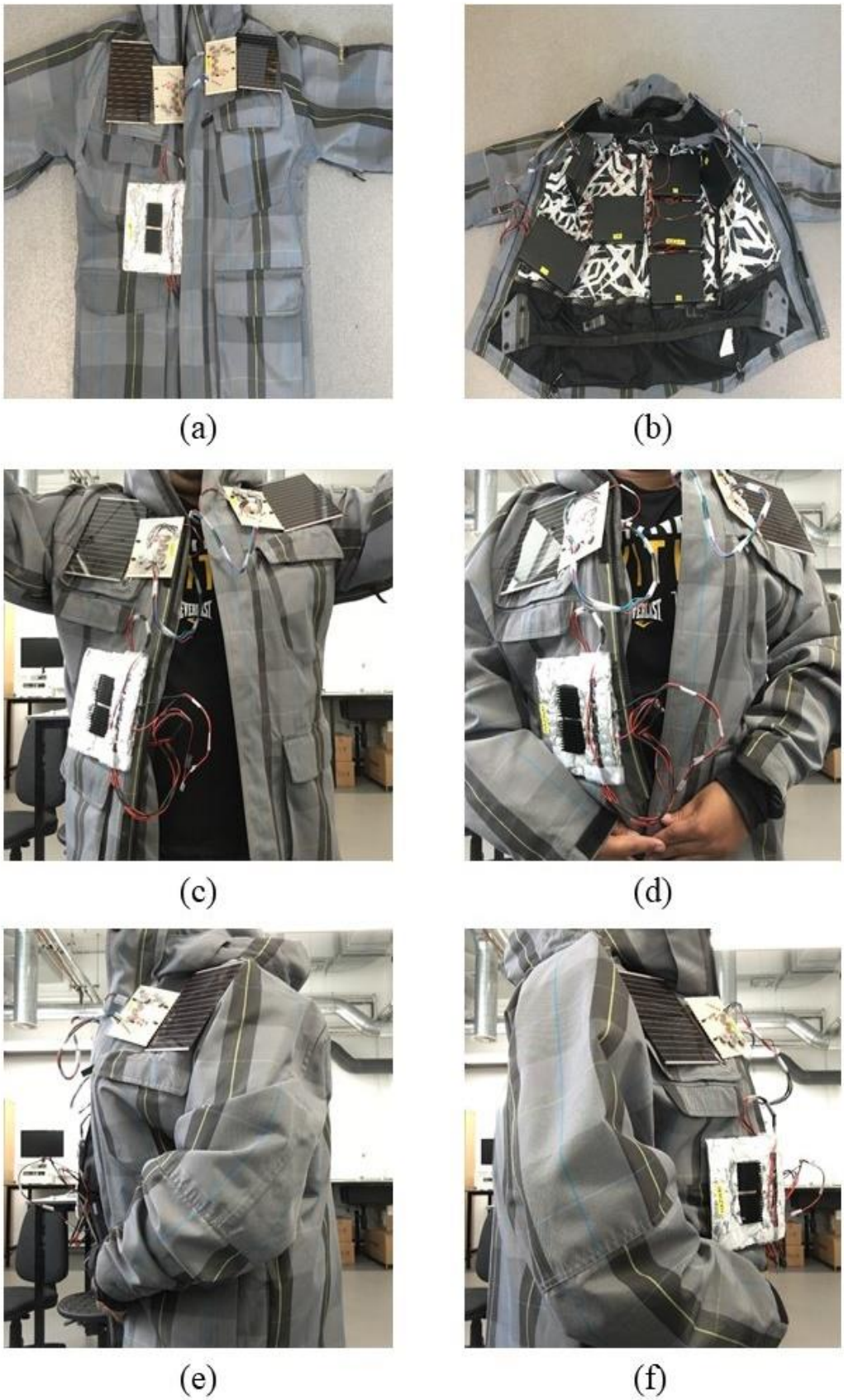


Figure 4.6: The prototype when attached to a jacket.

Each of the enclosures was attached to the inner part of the jacket through a Velcro™ tape. This tape provides a detachable platform for the enclosure, hence supporting the expandability feature of the system. The pictures of the jacket is shown in Figure 4.6. The solar panels and LDRs were placed on the shoulder area, where these elements have a higher chances of receiving maximum amount of light from the surroundings. A hole is made in the jacket to accommodate the TEG and to provide a good coupling between the hot side and the wearer's body. The first prototype needs some aesthetic development, which should be further improved for real life applications. The weight of the prototype was measured and the data is tabulated in Table 4.3 below. The system total weight is 2.08 kg, which is approximately equal to carrying 12 iPhone Xs (each iPhone X weights 174 g). Most of the total weight was contributed from the weight of the enclosures (≈ 54 %). Based on multiple tests, it was determined that the size of the enclosure that contributes the most to the degradation of the overall comfortability of the prototype. The weight although can be further reduced, was determined to be at an acceptable level without sacrificing much comfort to the wearer.

Table 4.3: Weight of each subsystem in the prototype.

System	Subsystem	Subsystem weight (g)	System weight (g)
SP1	Solar panel	65	355
	LDR + circuit board	40	
	Converter circuitry + circuit board	90	
	Enclosure box	160	
SP2	Solar panel	65	355
	LDR + circuit board	40	
	Converter circuitry + circuit board	90	
	Enclosure box	160	
TEG	Thermoelectric generator + thermistors setup	95	320
	Converter circuitry + board	65	
	Enclosure box	160	
Mode Select	Mode select circuitry + circuit board	90	250
	Enclosure box	160	
RB	Battery + circuitry + circuit board	166	326
	Enclosure box	160	
SC	Supercap. + circuitry + circuit board	80	240
	Enclosure box	160	
Voltage Bus	Circuitry + circuit board	75	235
	Enclosure box	160	
		Total weight (kg)	**2.08**

4.3.2 Prototype Performance

The prototype was tested in a typical summer outdoor environment and the performance data was collected. Due to the difficulty in measuring the current in the prototype, only the data for the bus voltage was able to be collected and analysed. Figure 4.7 below shows the scope view taken directly from the portable oscilloscope for the bus voltage when the sources converters were connected to the system and the load current was varied.

Figure 4.7: Scope view for the bus voltage of the wearable prototype.

Initially when the start-up procedure was performed, the bus voltage was recorded to be at the expected level of 1.83 V. At Q3, the source converters were connected to the system. The DC bus was recorded to be at 2.13 V, and it was expected that the SC was being charged during this period. The loading was then progressively increased and the DC bus voltage was recorded to be progressively reduced during this time, which is the expected behaviour. At Q6 and Q7, the discharging circuits for both storages were activated to support the high load current demand. At Q7, there was a sudden voltage peak due to the unexpected movement of the wearer during the test, which may have temporarily disconnected/disturbed the DC bus connection to the Keithley Sourcemeter. After the movement, the DC bus had levelled off at a slightly lower magnitude, possibly due to the difference in illumination level received by the solar panels and LDRs compared to the conditions before the movement, hence demonstrating the variable droop operation. It was postulated that during the full period of the test, the TEG did not

contribute any (or very low) power to the system, since the surroundings temperature was quite high (≈ 26 °C). At Q8, the load current demand was reduced to 7 mA, and the DC bus voltage level rose again. Whilst maintaining the same level of load current, at Q9, all of the source converters were disconnected from the system. The bus voltage was recorded to be at 1.80 V, which is at the expected level by considering the loadline of the SC discharging circuit as obtained in Figure 3.7. At this level, the RB discharging circuit was not activated.

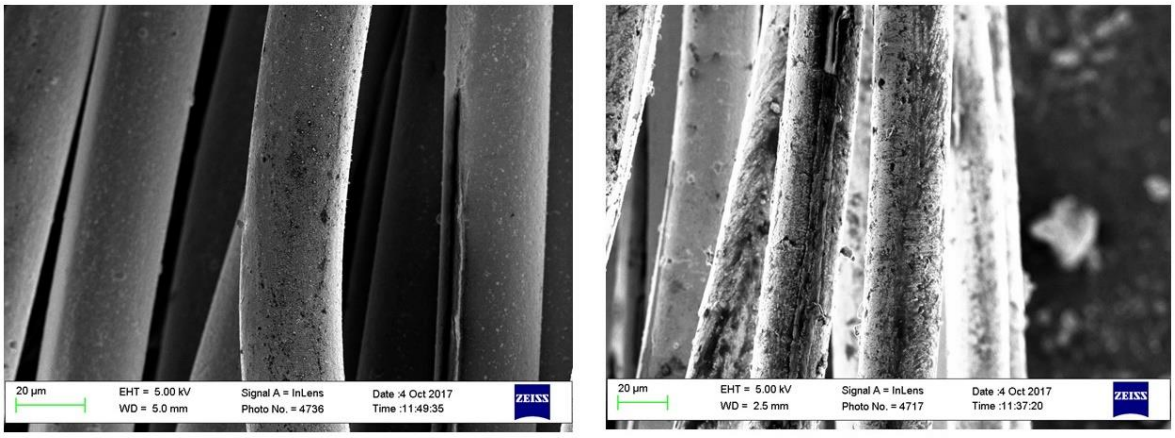
Overall, from this test, a successful operation for the prototype was demonstrated. This prototype proves the feasibility and reliability of the system to be implemented in real world applications.

4.3.3 Recommendations for Improvement

Some recommendations for the improvement of the first prototype are:

- The circuitry should be built and soldered on a flexible printed circuit board (PCB). This was initially in the scope of this PhD, however due to some unforeseen issues, this work was not completed. By using flexible PCBs, the size and weight of the overall circuit can be greatly reduced (approximately 60 % reduction). Currently, each circuit was built on a strip board. Furthermore, by using flexible PCBs, the circuit can be safely placed on the area where the circuit is expected to experience bending, and this will provide a better comfort to the wearer. The flexible PCB can be laminated to provide electrical insulation for the circuit.
- The solar panel and TEG are preferred to be flexible. With the availability of semiconductor materials and devices that can be deposited at low temperatures (< 200 °C), the fabrication of thin film devices on a flexible substrate that can match the performance of silicon based devices have been reported in recent years [53]–[57]. Among these, some flexible solar panels and TEGs have also been reported [58]–[62]. The integration of flexible solar panels and TEGs is not only able to improve the comfort of the system, but also opening up the possibility of direct integration with the clothing itself. Furthermore, to improve the variable droop accuracy for the solar panel and TEG, the same materials used to fabricate these devices can be further used to fabricate the LDR and thermistor. This ensures that both the energy harvester and the variable resistor have the same response towards the variation of the energy source.
- The connection wires are a hindrance to the overall comfortability of the system, and also make the system look less appealing. The wires can be hidden in the linings of the jacket,

however a better solution is to integrate silver fibres in the clothing to serve as a conductive thread to deliver power across any area on the jacket. Few preliminary works have been conducted (to support the work carried out by other students/postdoctoral associates under 1D-Neon project) on this, particularly extracting the electrical parameters such as resistance of the silver fibres. It was determined that the resistance of the thread is as low as the resistance of the typical copper wire with the same thickness, however the resistance will deteriorate (increase) after the thread was subjected to multiple stretching. This was due to the multiple cracks formed on the fibre after it was stretched, as shown in the scanning electron microscope (SEM) images in Figure 4.8. More work is required on this and if this issue can be solved, then the fibres have a huge potential to be implemented in the pico-grid system.



(a) Before stretching (b) After stretching

Figure 4.8: SEM images show each yarn in the silver fibre in a good and new condition (left) and after multiple stretching (right). The samples used for both images are different.

- Since the circuitry is preferred to be built on a flexible PCB, the passive components could be potentially fabricated/printed in thin film package to similarly possess the same flexibility feature. This ensures that the PCB is fully flexible and can bend in the same degree as the components placed on it. Since it is difficult to build a fully flexible thin film power circuit that can match the performance of a CMOS based power circuit, the usage of CMOS IC cannot be avoided. However, generally the size of these ICs is small and the size of the passive components will dominate the area on the board. Therefore, to ensure that the PCB is fully flexible, it is important to ensure that these passive components are flexible as well.
- Similarly, a flexible and thin film supercapacitor and rechargeable battery could be used as the energy storage and integrated in the system.

- The built prototype only utilises solar panel and TEG as the main source of energy. Several other energy sources such as piezoelectric generator, electromagnetic induction generator, triboelectric generator, and even wireless power (near field charger) all have potential to be integrated in the system. The method to track the variation of input power for each of these harvesters need to be explored and investigated in order to design the variable droop mechanism for the system. Furthermore, since the nature of these harvesters are in ac, the integration of a rectifier circuit, preferably flexible, is needed. Some preliminary work to fabricate and characterise a thin film diode that can be deposited at low temperature hence can be fabricated on a flexible substrate has been completed and will be presented in the following chapters.

4.4 Summary

In this chapter, the system integration for the pico-grid was presented and discussed. The integrated system was tested in two different ways; the first was aimed to demonstrate the plug-and-play capability of the source converters and load, and the other was aimed to demonstrate the general performance and to extract the efficiency of the system. Both tests were successfully carried out, and the performance expected from the pico-grid was successfully accomplished. It was determined that the efficiency of the source converters is significantly lower than the efficiency of the charging and discharging circuits (< 50 % *vs*. > 75 %), mainly due to the high power consumption of the droop feedback circuitry, which was dominated by the power consumption of the current shunt monitor. The first wearable prototype for the pico-grid was then constructed and the performance of the prototype was presented and discussed. Overall, a successful operation was achieved. Since the first prototype was not optimised for real world applications, some suggestions and recommendations for improvement were presented.

In conclusion, the proof-of-concept operation of the pico-grid has been successfully demonstrated and achieved, through both on-bench and wearable prototypes. Several important operations to improve the reliability, efficiency, and feasibility of the pico-grid such as variable mode select mechanism and plug-and-play operation were successfully demonstrated. In the following chapters, due to the opportunity of working with new semiconductor compound and accessibility to the fabrication facilities, some preliminary work on thin film diode fabrication for the purpose of fabricating a fully flexible rectifier circuit are presented.

Chapter 5

ZnON Thin Film Diode – Fabrication and Characterisation

5.1 Foreword

This chapter presents the fabrication and characterisation results for the zinc oxynitride (ZnON) thin film diode. After the operation of the pico-grid has been successfully demonstrated, there is a huge opportunity to further improve the overall system performance and to increase the feasibility of the operation by improving each sub-system. One of the possible areas is the power circuit.

In order to integrate any ac energy harvesting mechanism such as piezoelectric and electrostatic transducer in the pico-grid system, an AC-DC rectification stage is required to convert the ac voltage from these sources to a useful dc voltage. This is shown in Figure 5.1. In order to achieve this, a device with a blocking capability is needed and in most cases, Schottky diode is preferred due to its low forward voltage drop. Furthermore, since the targeted applications for the pico-grid are mainly on WBAN systems, flexible circuit is a favourable feature since this feature will enable a seamless integration of the circuit with the conductive textiles. In order to achieve this, the low temperature fabrication of a Schottky diode is investigated and presented in this chapter. The Schottky barrier diode performance fabricated from the selected semiconductor material is then evaluated and discussed.

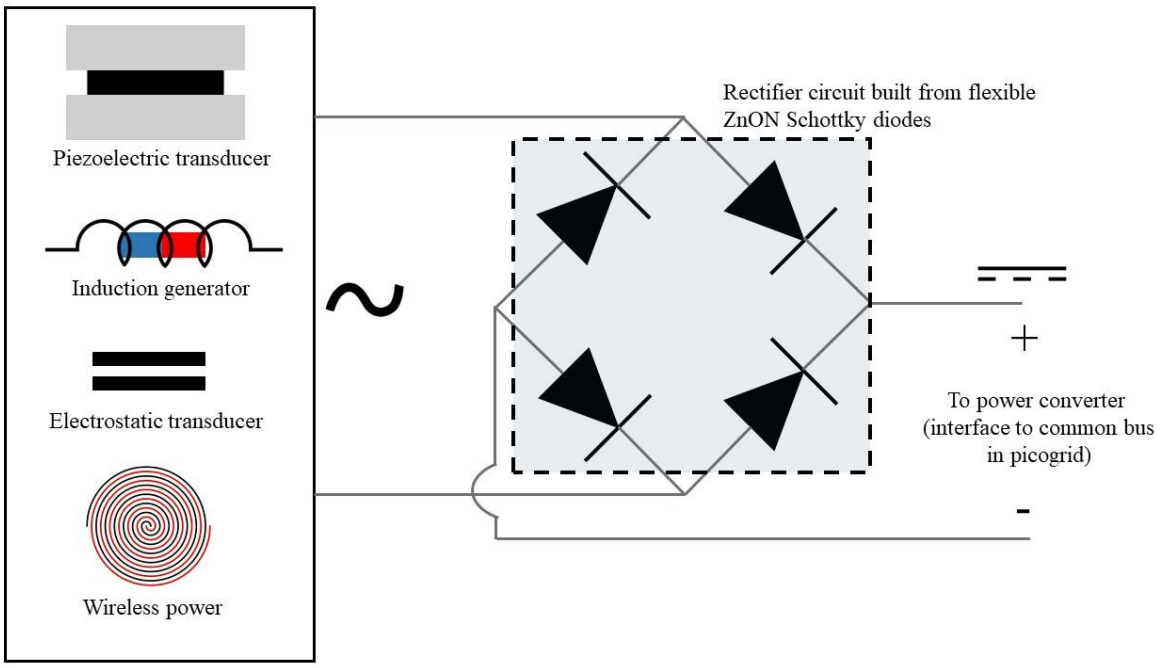


Figure 5.1: The need for a flexible diode for AC-DC rectification for AC energy harvesting mechanisms in WSN or WBAN applications.

5.2 Background

This section provides an overview on the selection of the semiconductor material and also the structure of the fabricated diode.

5.2.1 ZnON Semiconductor

Metal oxides semiconductors have garnered huge interest in recent years due to its superior performance. Among other advantages, low cost, possibility of low temperature deposition, and flexibility of integration with other organic and inorganic compounds are key attributes. In the application of thin film transistor (TFT), this type of semiconductor is preferred when compared to the conventional amorphous silicon due to its higher mobility. One of the most extensively studied semiconductor in this group is perhaps zinc oxide (ZnO). ZnO is an intrinsically n-type transparent conductive oxide (TCO) and was once used by multiple research groups as a TFT channel material [63]–[66]. However, the polycrystalline structure of ZnO means it suffers from a few instability issues. In particular, the traps in the dense grain boundaries of the crystalline structure and the grain nucleation issue has made it hard to control the fabrication process and produce a TFT with consistent performance. In order to improve this, a cation and anion control strategy has been implemented and investigated. Metal cation control is able to reduce the grain boundaries hence reducing the potential barrier and

increasing the mobility. However, this method is not as effective in amorphous metal oxides since the interaction of different metal cations can result in additional potential barriers. In this sense, the anion control strategy which can suppress potential barrier resulted from grain boundaries and at the same time eliminate the interaction of different metal cations is preferred. Examples of semiconductor materials utilising these methods include InGaZnO and InZnO for metal cation control and ZnON for anion control. Among these, ZnON has a huge potential since it can be fabricated at low temperature, and possesses high mobility and high illumination stability. However, ZnON is not to be confused and mixed with ZnO:N, which suffers from instability issue, which will be discussed next.

Perhaps the first paper related to nitrogen doped ZnO can be traced back to 1998 when Futsuhara *et al*. [67] doped ZnO with nitrogen through sputtering method by using ZnO target with argon and nitrogen gas flowed into the chamber. The purpose of most of the initial work was mainly to reduce the bandgap of the ZnO by introducing impurity dopants. Later in 2006, Yao *et al*. [68] published a paper outlining the change in conductive behaviour of ZnO film doped with nitrogen through reactive sputtering process, in which the film could change from p-type to n-type under different circumstances, and vice versa. In this sense, the instability issue is apparent in nitrogen doped zinc oxide, or ZnO:N. Due to this conductive behaviour instability, this material is not suitable to be used as the semiconductor material in thin film diode.

However, three years later in 2009, Ye *et al*. [69] was the first to publish a paper outlining the method of reactive sputtering process which promotes competitive reaction between nitrogen and oxygen with zinc (using Zn target), resulting in a rather amorphous ZnON structure, which upon annealing at 400 °C, was able to produce a high mobility n-type semiconductor exceeding 100 $cm^2 V^{-1} s^{-1}$ and most importantly is stable. The main difference from previous publications is that they used a Zn target with oxygen, nitrogen, and argon gases (ZnON) instead of ZnO target with nitrogen and argon gases (ZnO:N). The competitive reactions between zinc and oxygen (which produces hexagonal ZnO) and zinc and nitrogen (which produces cubic Zn_3N_2) are the main reasons that promote the amorphous structure of this film. Lee *et al*. [70] reported that the properties of ZnON can be adjusted based on the nitrogen flow rate in the reactive sputtering process. In their publication, it was found that the carrier mobility and bandgap are both highly dependent on the nitrogen content as shown in Figure 5.2. This feature is sometimes desired due to the different requirements of semiconductor material in different applications.

Since 2009, many different groups have managed to fabricate a good TFT from ZnON film [71][72].

However, degradation in the performance of ZnON has been observed in the deposited film since oxygen which possesses higher reactivity with zinc compared to nitrogen, can react with ZnON and change the chemical composition of the film. Two main treatments have been used to counter this issue; thermal annealing and argon plasma treatment. Thermal annealing has been shown to enhance the electron concentration from the increase in nitrogen vacancies of Zn_xN_y bonds in the ZnON film [73]. Argon plasma treatment assists the film to redistribute its atomic structure, hence leading to a more energetically stable configuration [74]. In both cases, degradation in performance has been significantly reduced, resulting in a longer shelf life of the ZnON film.

As a result of its superior performance in TFT especially stability and simple low temperature fabrication technique, ZnON was chosen as the semiconductor material to fabricate the diode. Furthermore, it would be much easier to integrate the same semiconductor material for both diode and TFT on the same substrate to make a working power circuit.

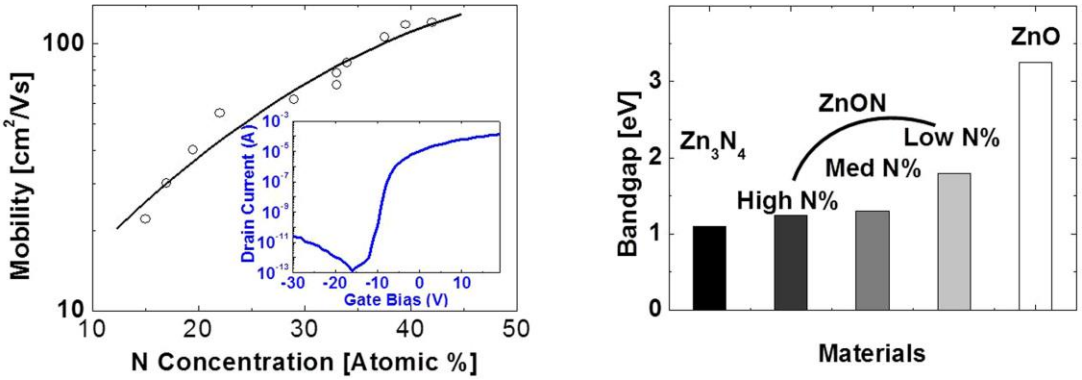


Figure 5.2: The variation of mobility and bandgap of ZnON film with nitrogen content taken from [70].

5.2.2 Schottky MIS Diode

The selection of the diode structure needs to consider the available fabrication method and also the requirements of the application. Since only the deposition of ZnON film which is an intrinsically n-type semiconductor is possible for the semiconductor material, therefore the p-n or p-i-n junction diode structures are not possible to be fabricated. The Schottky diode structure has been selected since it only requires metal contact depositions apart from the semiconductor deposition, which makes the entire process relatively simple.

The Schottky diode is a metal-semiconductor (MS) diode whose transport is solely based on a majority carrier, resulting in a fast switching action. MS contact can result in two different operations; ohmic or rectifying. Theoretically, the operation of the contact is dictated by the difference of the metal work function and electron affinity of the semiconductor. For an n-type semiconductor, if the metal work function is higher than the electron affinity of the semiconductor, then the MS contact is expected to behave as a rectifying contact, and vice versa. This property is outlined in the Schottky-Mott rule and is shown in Figure 5.3.

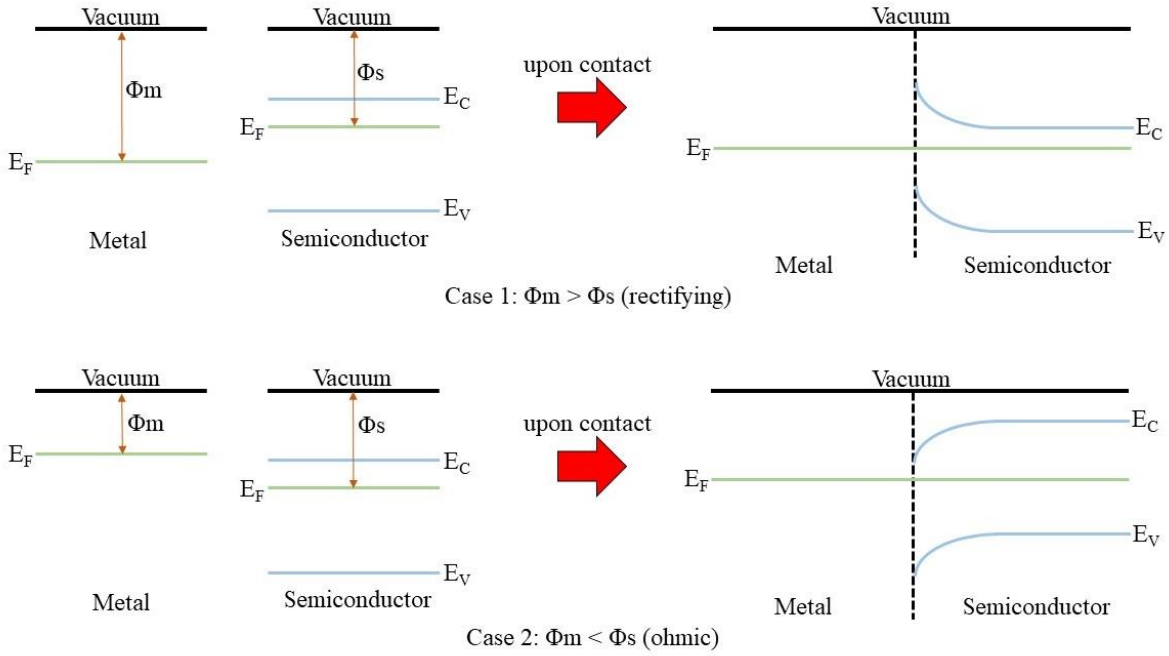


Figure 5.3: Energy band diagram of MS contact at thermal equilibrium. The metal work function and semiconductor electron affinity both would define the operation of the contact.

However, in reality, the behaviour of the contact is not solely governed by the metal work function, but also the interface quality between the metal and semiconductor. In an ideal case, both the metal and semiconductor are considered pure and there is no interfacial layer or reaction between them. Interface states and defects, intrinsic surface states, dangling bonds, and chemical reaction and diffusion could also occur from the metal to the semiconductor side, thus altering the interface properties and preventing the MS contact from behaving according to the expected Schottky-Mott rule. Generally, it is difficult to define the expected behaviour of an MS contact without testing the conductive behaviour of the actual fabricated contact.

The Schottky diode has been well known to have a fast switching property, small forward voltage drop, but with a high leakage current. These properties are mainly due to the single carrier transport mechanism for this diode. The conduction property of the diode is shown in

Figure 5.4. The built-in potential is defined as the amount of potential energy that must be acquired by a single electron to move from the semiconductor conduction band to the metal side. The external bias can be applied to either reduce or increase this potential, resulting in a higher or lower probability of electrons to have enough energy to overcome the barrier. When the external bias is positively applied to the metal side with respect to the n-type semiconductor side, then this potential will be reduced, thereby the current can easily flow. This is called forward bias. In reverse bias, the external bias is negatively applied to the metal with respect to the n-type semiconductor side, effectively increasing this potential causing only a very small current to flow.

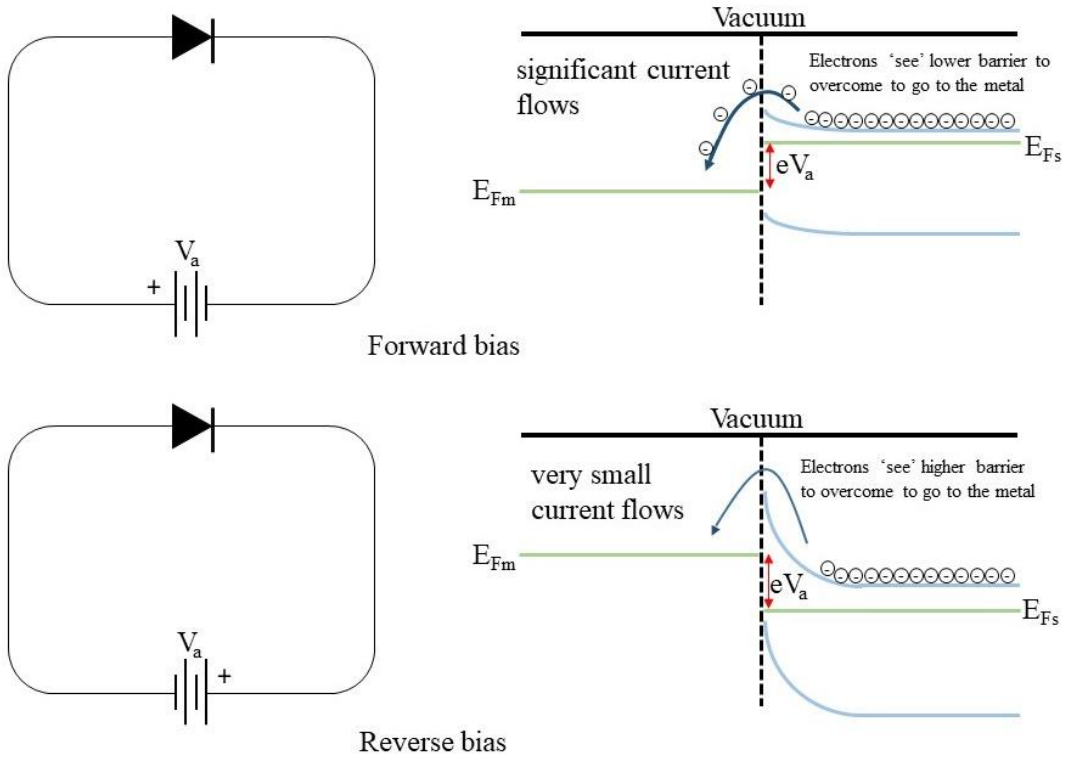


Figure 5.4: Energy band diagram for a Schottky diode under forward and reverse bias condition.

A very thin insulating layer (in the range of few nm) is normally intentionally deposited in between the metal and semiconductor surfaces. Aside from preventing the reaction and diffusion between the metal and semiconductor, this layer serves to enhance the performance of the diode, in particular it is capable of reducing interface states and preventing Fermi level pinning [75][76]. Fermi level pinning is a common phenomenon which occurs in the MS interface, where the degree of band bending in the semiconductor near the interface is independent of the metal work function variation, causing the alteration of the actual barrier height. Fermi level pinning is a very undesirable feature in MS contact since it can degrade the

performance of the diode by introducing higher parasitic resistance to the flow of electrons. Furthermore, the presence of a thin insulating layer could also potentially reduce the leakage current of the diode [77]. It has been shown that the insertion of the thin insulating layer would not significantly affect the transport mechanism of the diode, since this layer is so thin that electrons can easily tunnel through it [76]. However, the insulator must be of high quality since a low quality insulator can introduce interface states, thus further deteriorating the performance of the diode.

Due to the availability of the fabrication process to deposit high quality insulator with great controllability over the thickness, the MIS structure was selected as the diode structure.

5.3 Fabrication and Characterisation Results

This section presents the fabrication method and subsequently characterisation results of the ZnON MIS diode.

5.3.1 Fabrication and Characterisation Method

a. Fabrication Method

The structure of the fabricated diode is shown in Figure 5.5. The diode was fabricated on top of a 1 mm thick Corning 70059 glass substrate measuring 20 mm by 10 mm (cut from 20 mm by 20 mm). The substrate was cleaned properly by first rinsing it with deionised (DI) water and then ultrasonicating it in acetone and then isopropyl alcohol solution, each for 10 minutes. It was then dry blown with nitrogen gas and baked at 120 °C for 30 minutes to remove any possible moisture. Molybdenum is used as the bottom contact since it provides good ohmic contact with the ZnON film with a very low contact resistance. Nickel was used as the top contact since this metal is the only available metal that produces rectifying contact with ZnON film. Some other metals and TCO tested apart from nickel were chrome, aluminium, and indium tin oxide (ITO), however no definite and consistent rectifying property could be obtained. The depositions for both bottom and top metal contact were done at room temperature in the custom built-in metal sputter coater machine. The thickness for both layer was 100 nm. The depositions for the ZnON semiconductor and Al_2O_3 insulating layer were done by using a cluster tool multi deposition system manufactured by MVSystems, as shown in Figure 5.6. This deposition tool is an integrated deposition system capable of carrying out a few different deposition processes in multiple chambers; plasma enhanced chemical vapour deposition

(PECVD), atomic layer deposition (ALD), and reactive magnetron sputtering, with a vacuum isolation and transfer zone between each chamber to ensure no contamination to the samples.

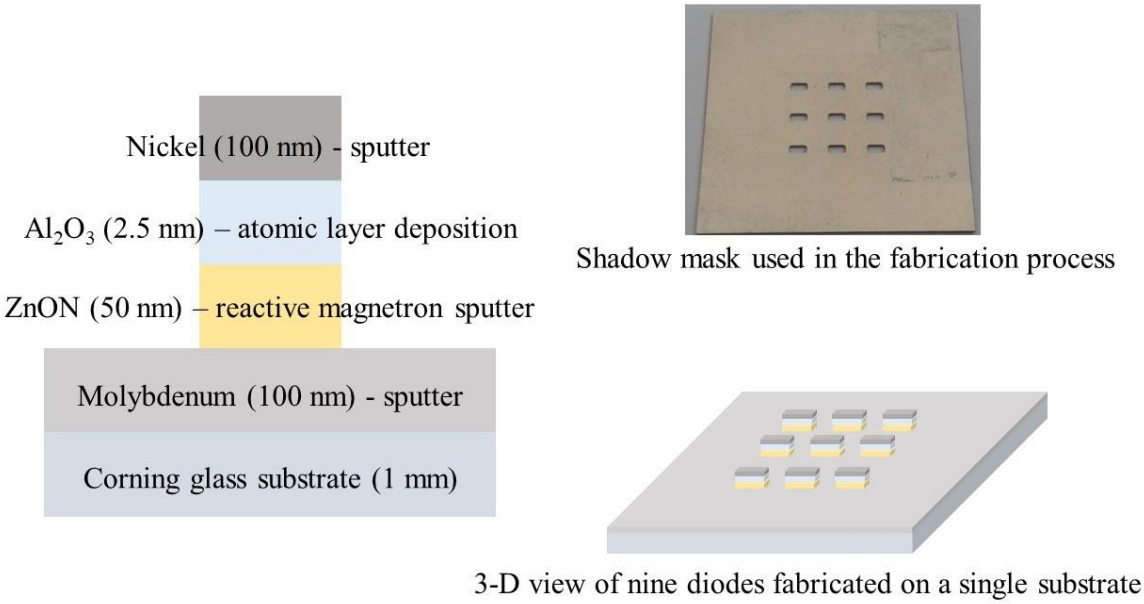


Figure 5.5: Structure and 3-D view of the fabricated diode. The shadow mask used in the fabrication is also shown here.

Figure 5.6: MVSystems cluster tool deposition system used in the fabrication process.

Reactive magnetron sputtering for ZnON layer

The ZnON film was deposited through a reactive magnetron process to produce a 50 nm layer. Zn target was used with argon, oxygen, and nitrogen gases flowed into the chamber at specific flow rate. Both the target and gases have 99.99 % purity. The optimisation process for the fabrication conditions was done by varying the flow rate of the gases into the sputtering chamber. Whilst keeping a constant flow rate of argon (4 sccm), the flow rates of nitrogen and oxygen were varied and after each fabrication, the characterisations were carried out on the fabricated film to get the optical bandgap (from UV-VIS measurement) and hall mobility and carrier concentration (from hall effect measurements). At each condition, the chamber pressure was set to be almost vacuum (<15 mTorr). The RF power was maintained at 250 W throughout all fabrication conditions.

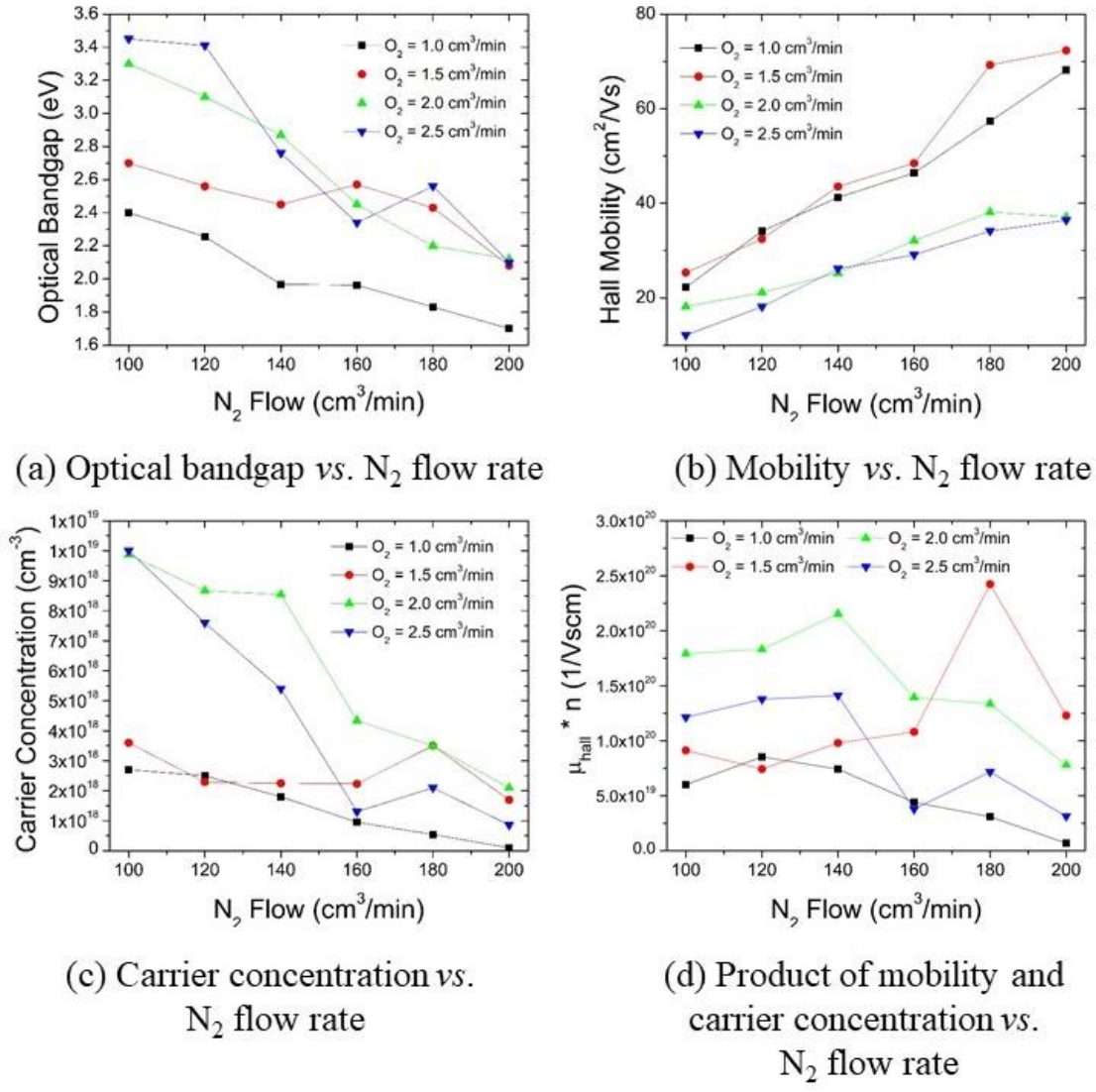


Figure 5.7: Characterisations for different fabrication conditions for ZnON film.

The results from the characterisations are shown in Figure 5.7. From Figure 5.7 (a), it can be seen that the optical bandgap decreases as the ratio of N_2/O_2 increases. This can be elucidated by considering the bandgap of ZnO (3.2 eV) and Zn_2N_3 (1.1 eV). As the ratio of N_2/O_2 increases, the optical bandgap will reduce due to the lower concentration of ZnO and higher concentration of Zn_2N_3 and nitrogen rich ZnON in the film. Figures 5.7 (b) and 5.7 (c) present the extracted hall mobility and carrier concentration for the film under different N_2/O_2 ratio. As the ratio of N_2/O_2 increases, the mobility increases but the carrier concentration decreases. This finding is consistent with some of the reported works in the literature [69][78]. Further characterisations involving XPS measurement are needed in order to provide a possible explanation for this phenomenon, and this was not carried out in this thesis. Nevertheless, in order to provide a figure of merit for the best fabrication condition, the product of mobility with carrier concentration was computed and is shown in Figure 5.7 (d). From this, it was determined the highest magnitude of this figure of merit was obtained from the following flow rate; N_2 = 180 sccm and O_2 = 1.5 sccm. This condition was then used throughout the fabrication of the diode in this thesis.

Atomic layer deposition (ALD) for Al_2O_3 layer

The Al_2O_3 layer was deposited through an ALD process to produce a 2.5 nm layer. The fabrication condition used in this thesis was optimised and provided by MVSystems. Hence, no optimisation process was done to further improve the fabrication condition. Trimethylaluminum (TMA) and water were used as the main precursors and each cycle of the ALD process was determined to produce almost a consistent thickness of 0.1 nm. The thickness of the film as obtained from the profilometer against the number of cycles used is shown in Figure 5.8.

The deposition conditions for both processes are tabulated in Table 5.1. A single shadow mask with an area of 0.66 mm^2 was used to pattern the semiconductor, insulator, and top metal contact layer. It is worth mentioning that another insulator, silicon nitride (SiN_x) was attempted to be used as the insulator, however, the degree for thickness controllability is poor, thus consistent film thickness was very hard to be reproduced. Plus, the deposition also requires a high substrate temperature (around 370 °C). Apart from the Al_2O_3 insulating layer, all other layers are deposited at room temperature. The overall thickness of the diode excluding the substrate is 252.5 nm.

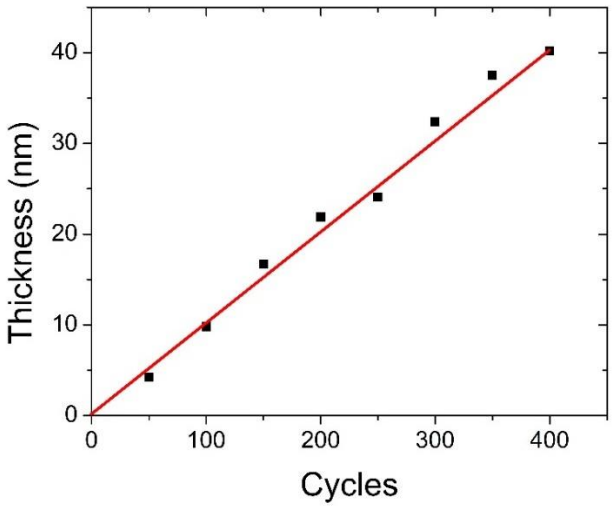


Figure 5.8: Thickness of Al_2O_3 film deposited from the ALD process obtained from the profilometer as a function of number of cycles.

Table 5.1: Deposition process parameters for ZnON and Al_2O_3.

Parameter	**Reactive magnetron sputtering (ZnON)**	**Atomic layer deposition (Al_2O_3)**
Pressure	12.5 mTorr	80 mTorr
Temperature	Room temperature	250 °C
RF power	250 W	N/A
Target / Precursor	Zinc (99.99 %)	TMA (99.99 %) Water (H_2O)
Gas flow rate	Ar – 4 sccm	N/A
	O_2 – 1.5 sccm	
	N_2 – 180 sccm	
Cycle	N/A	25

b. Characterisation Method

The I-V and C-V measurements were carried out by using a Keithley 4200 Semiconductor Characterisation System (4200-SCS). The sample was put inside the LakeShore probe station and the temperature was controlled by a Lakeshore 336 Temperature Controller. Temperature dependent measurements were conducted inside a vacuum chamber. All measurements were carried out in a dark condition and temperature was varied from 50 °C to 200 °C at 50 °C intervals. The room temperature measurements were carried out in normal atmospheric conditions.

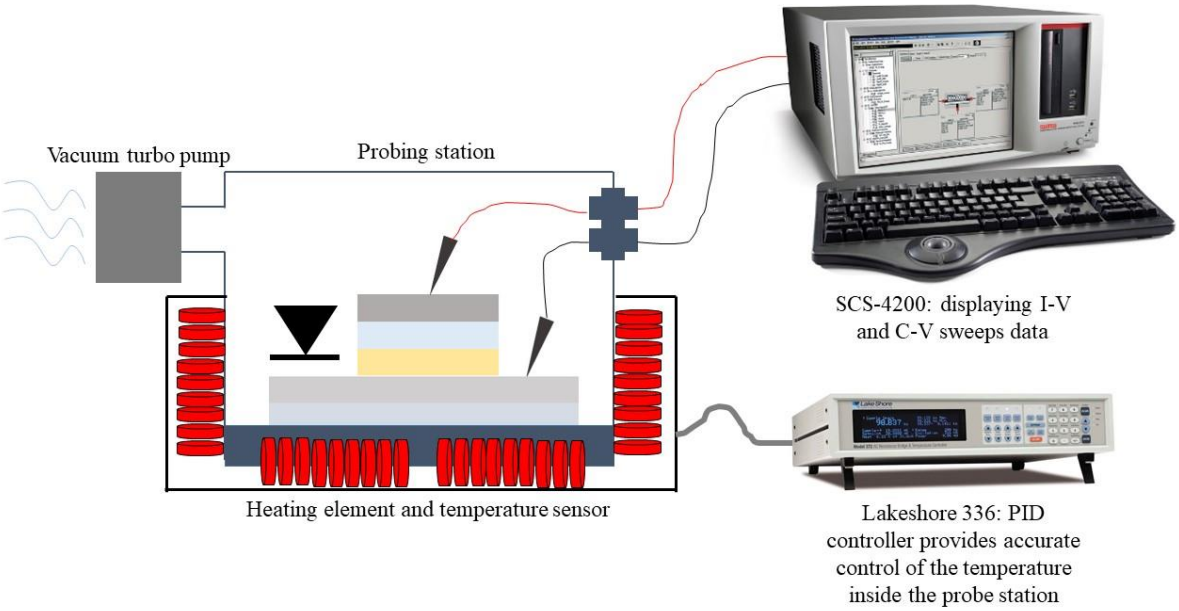
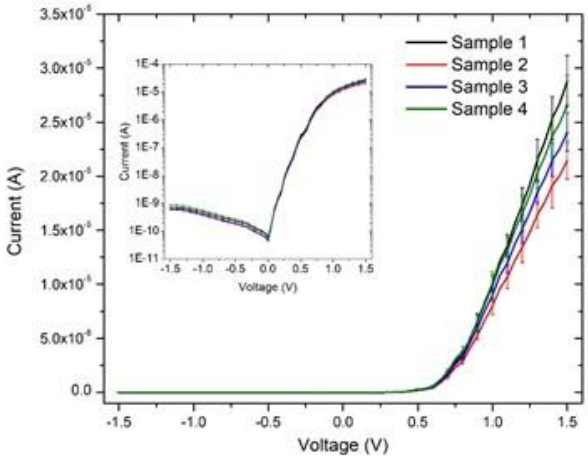


Figure 5.9: Characterisation setup of the fabricated diode.

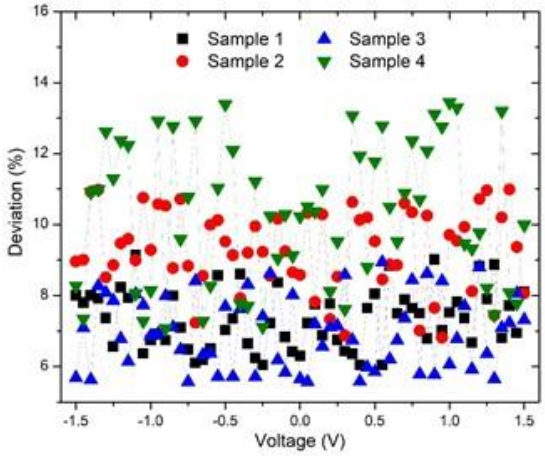
c. Reproducibility

The main challenge with the semiconductor fabrication process is to produce devices with a consistent performance regardless of different fabrication batches. This is mainly due to the limited controllability over the competitive reaction between zinc with oxygen and nitrogen, and limited control can only be achieved via regulating the gas flow rate into the reaction chamber. Reproducibility is one of the most important features that must be present in the fabrication process of any critical devices. To test the reproducibility of the ZnON film used in this experiment (the fabrication processes for other layers are considered consistent and reproducible), a set of 4 different samples (from 4 fabrication processes) was fabricated. Each sample contains 9 diodes (from the shadow mask). The fabrication processes for each sample were exactly the same.

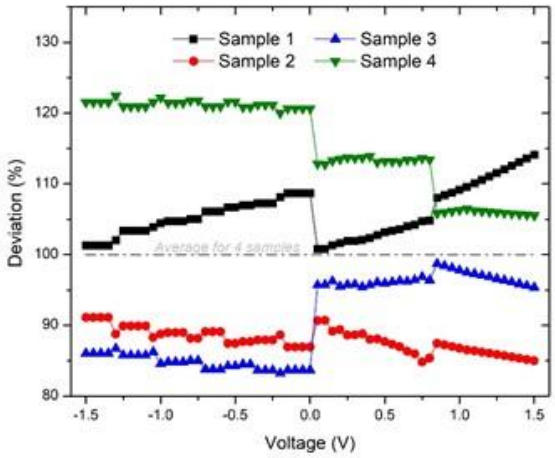
The performance of the as deposited samples was then tested. In particular, the I-V was swept from -1.5 V to 1.5 V at 0.05 V intervals. The results for all 4 samples (average of 9 diodes in each sample) are shown in Figure 5.10 (a). Generally, deviations between samples are only apparent after the diodes have been turned on in a forward direction. No significant deviations between samples can be observed in reverse bias and in low voltage region in forward bias. This is suspected to arise mainly due to the different magnitude of series resistance of the fabricated diodes.



(a) Average I-V for all samples with their respective deviations



(b) Max. deviations of I-V (taken from one of 9 diodes in each sample) from average of all 9 diodes in each sample



(c) Deviations of I-V (taken from average of 9 diodes in each sample) from average of 4 samples

Figure 5.10: Reproducibility of the performance of the diode for an as deposited film demonstrated by the fabrication of 4 samples from different batches.

The deviations in each sample were further investigated. The performance of 9 diodes from each sample was averaged, and the maximum deviations from the average at every voltage interval were shown in Figure 5.10 (b). From this, it can be observed that although deviations can be observed even between diodes from the same sample, these deviations are very small and are mostly constrained within 10 % of the average. For each sample, although all diodes were fabricated on the same substrate and went into the same fabrication process, there would be a slight difference in chemical composition and thickness. Although the difference is very small, the diode in the centre of the substrate would be slightly thicker than the diodes at the edges of the substrate. Furthermore, the diode at the centre also was positioned directly beneath the sputtering target, which might produce a different chemical composition.

The deviations between samples were further investigated as shown in Figure 5.10 (c). The average of I-V curves of all samples is shown as 100 % (grey line) and the deviations for each sample at each interval are shown around the grey line. From this, it can be observed that the deviations between samples are mostly constrained within 20 % of the average. From the data obtained in this section, it can be concluded that reproducible results within 20 % of the average can be easily obtainable from the fabrication of the diode.

d. Evidence of Schottky Contact Behaviour

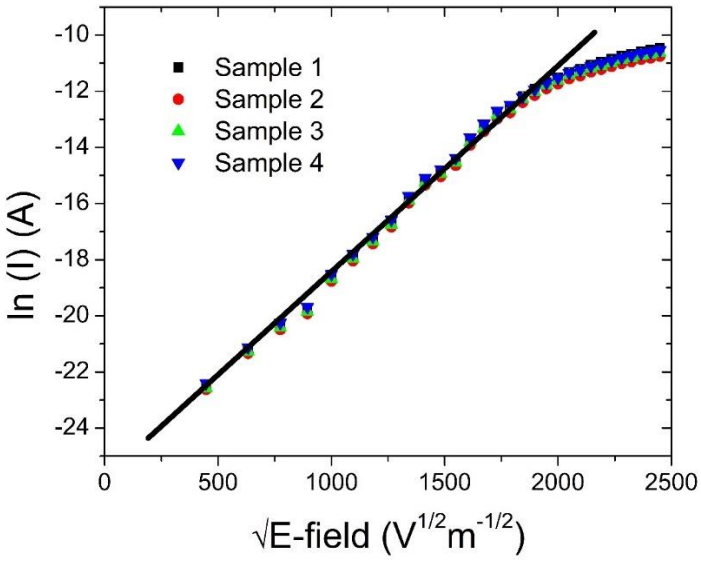


Figure 5.11: Evidence of the formation of Schottky contact and thermionic emission transport mechanism in the fabricated diode.

Evidence that the Schottky contact behaviour is formed between the nickel electrode and ZnON semiconductor can be obtained by observing the Schottky plot (natural logarithmic value of

forward current against square root of electric field). Additionally, the linear relationship between these two parameters at low bias indicate the dominant of thermionic emission current transport mechanism across the diode. This plot is shown in Figure 5.11. In this figure, the forward current data is obtained from the previous reproducibility section. From the linear relationship observed in this plot, it is apparent that the thermionic emission current transport mechanism dominates the current transport across the diode and therefore, this model is implemented to elucidate the characteristic of the diode in the following sections.

e. Effects of Post Deposition Annealing

The performance of the ZnON semiconductor has been reported to be enhanced when post deposition thermal annealing treatment is carried out. Annealing treatment has been carried out in a normal atmospheric pressure post fabrication process and the effect of the annealing to the performance of the diode is investigated. Three films from the same fabrication batch have been annealed at 3 different temperatures (150 °C, 250 °C, and 350 °C) for three hours (measurements were taken at one-hour interval) and the performance of the diode was then investigated. The I-V was swept from -1.5 V to 1.5 V at 0.05 V intervals.

Figure 5.12 shows the effect of annealing at different temperatures to the I-V behaviour of the diode. For all temperatures, annealing increases the leakage current in reverse bias and also the saturation current of the diode. However, this trend is not consistent in forward bias. For 150 °C and 250 °C, annealing significantly increases the forward current up until the duration of 2 hours, and after that the performance starts to degrade. The extent of this degradation is more apparent when the diode is annealed at 350 °C. The findings from this experiment corroborate with the results reported in [73]. It was postulated that the enhancement in the performance of the ZnON film when annealed at 150 °C and 250 °C is due to the increase in electrons concentration caused by the increase in the nitrogen vacancies in the defective Zn_xN_y bonds in the ZnON. However, annealing ZnON film at significantly higher temperature such as 350 °C would increase the oxygen concentration in the film thus reducing the electrons concentration.

This reduction of electrons concentrations could also possibly occur when the film is annealed at longer durations in lower temperatures, thus explaining the degradation of performance when the diode is annealed for more than 3 hours at 150 °C and 250 °C. Another possible explanation for the degradation of the performance is not due to the ZnON film, rather degradation in the metal contacts and thin insulator quality. This is another possible factor since Ok *et al*. [71] reported that the ZnON enhancement can still be observed even after the film was annealed at

250 °C for 5 hours. This observation is contradicting the results obtained from this experiment, however it should be noted that their film was annealed in low pressure ambient. In publications, the same annealing condition has been used in [79]. Ye *et al*. [72] reported that apart from enhancing the electrical performance of the film, annealing can also increase the shelf life of ZnON film.

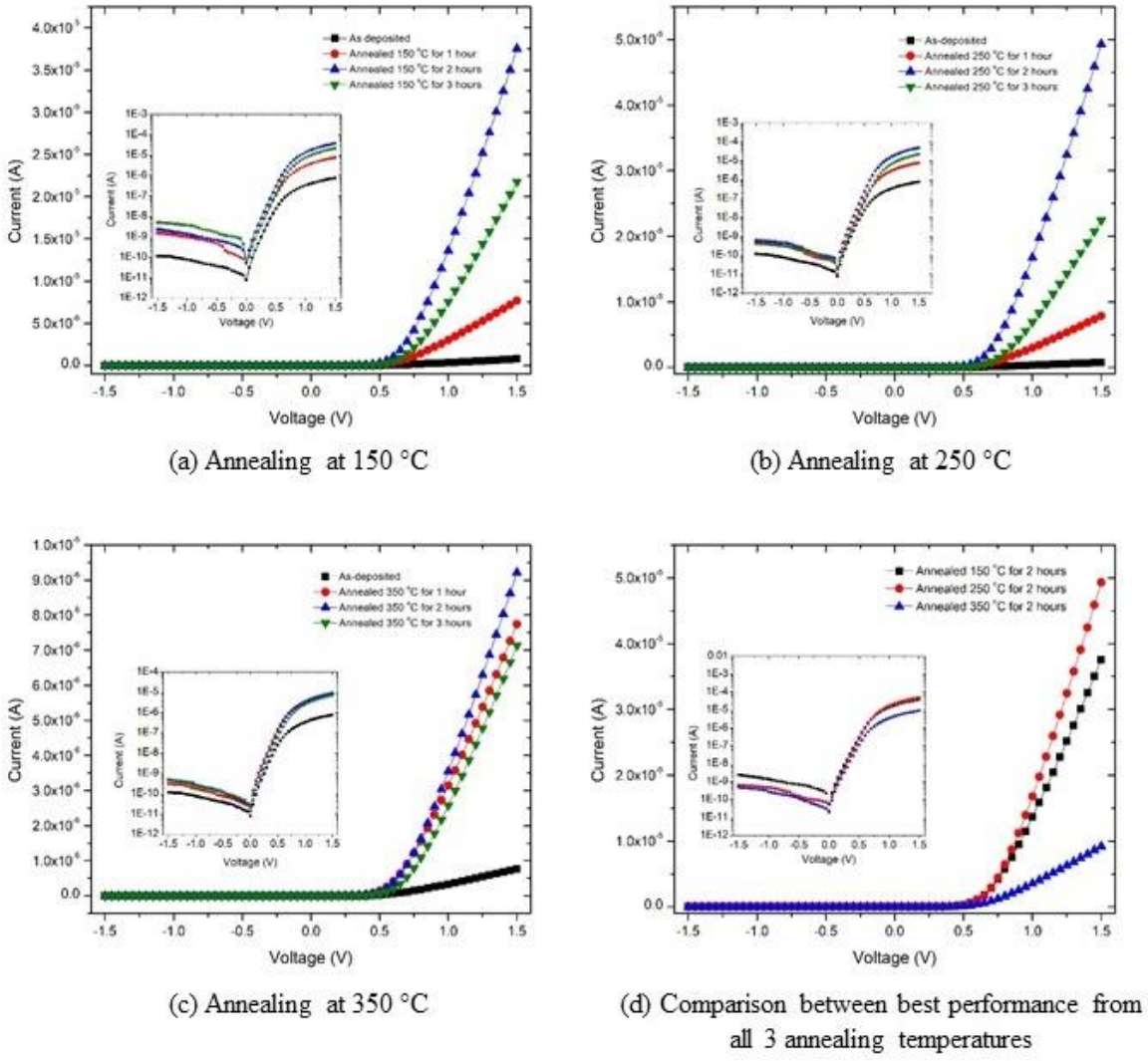


Figure 5.12: Effects of post deposition annealing with different temperatures and duration to the performance of the diode.

Another way to elucidate the implications of annealing on the magnitude of current in the forward bias characteristics is through Arrhenius plot. The reduction in the forward characteristics could be associated to the increase of trap concentration in the insulator interface. The activation energy (E_T) of the trap can be determined from the thermal emission

rate (e_n) from the deep level into the conduction band of ZnON through the Arrhenius relationship:

$$e_n = \sigma_n v_{th} N_{cb} \exp\left(\frac{-E_T}{kT}\right) = \frac{1}{\tau_e}$$

Here σ_n is the capture cross section, v_{th} is the thermal velocity, N_{cb} is the density of states in the conduction band of ZnON, k is Boltzmann constant, T is temperature (K), and τ_e is the emission rate constant. v_{th} and N_{cb} can be calculated from:

$$v_{th} = \sqrt{\frac{3kT}{m^*}}$$

$$N_{cb} = 2\left(\frac{2\pi m^* kT}{h^2}\right)^{\frac{3}{2}}$$

Here m* is the effective mass of electron in ZnON and h is Planck's constant [79][80]. From this relationship, the thermal activation energy can be obtained from the slope of $\ln(e_n/T^2)$ against 1000/T plot (Arrhenius plot) and is shown in Figure 5.13. Additionally, the magnitude of capture cross section can be extracted from the y-intercept in the plot. The trap activation energies for the different annealing duration were calculated from the slope of the linear regression fits and are shown in the same figure. From this, it can be observed that the traps have the highest estimated activation energy when the film has been annealed for two hours, hence this could explain the improvement for the forward behaviour of the diode in this annealing condition for all annealing temperatures.

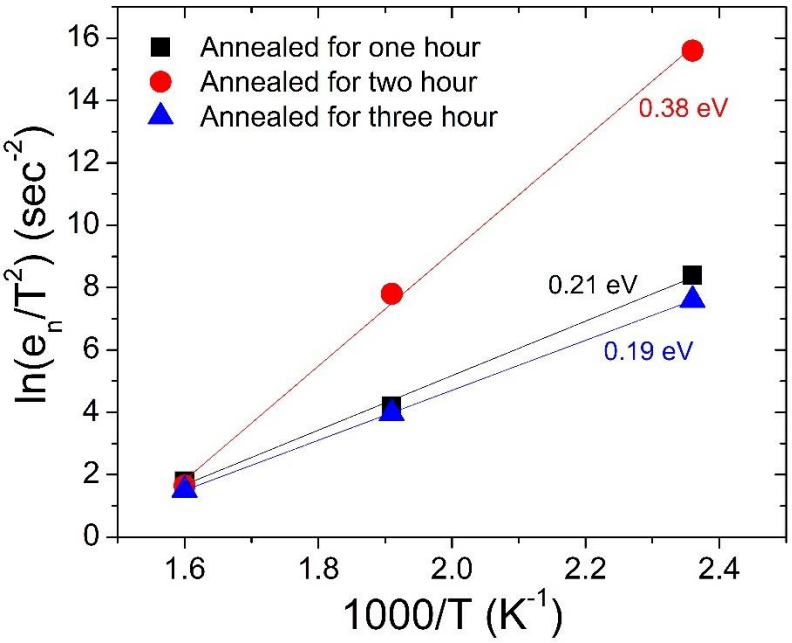


Figure 5.13: Arrhenius plot to obtain the thermal activation energy of the traps in the diode.

The three best forward characteristics obtained from three different annealing temperatures are shown in Figure 5.12 (d). From this, it can be observed that the best performance diode in terms of forward bias is obtained from annealing the sample at 250 °C for 2 hours. This post deposition annealing condition was then used throughout the experiments in this chapter.

5.3.2 Temperature Dependent I-V Measurements

In this section, the results of temperature dependent I-V measurements of the diode are presented and a curve fitting method based on the thermionic emission model is proposed to extract the parameters from the I-V curves. The trends of each of these parameters are then discussed.

For the MIS Schottky barrier diode, the forward bias characteristic can be modelled by the thermionic emission-diffusion theory with series resistance expression, neglecting the effect of shunt resistance:

$$I = I_O \exp\left(\frac{q(V - IR_s)}{nkT} - 1\right) \quad \ldots \quad \text{eq. (5.1)}$$

Here I_o, R_s, n, and T are the saturation current, series resistance of the diode, ideality factor, and temperature (K), respectively. All of the values in the equation are constant except these three parameters; saturation current, ideality factor, and series resistance which are of interest in evaluating the diode.

Multiple extraction methods for these three main parameters have been proposed in the literature. Whilst some extraction methods are straightforward and easily implemented, few methods are only applicable to certain types of dominant transport mechanism, interface quality, and diode structure. The saturation current is normally extracted from the 0 V intercept of the ln(I)-V curve and from the value, the barrier height can be obtained by the following relation:

$$I_O = AA^{**}T^2 \exp\left(-\frac{q\Phi_B}{kT}\right) \quad \ldots \quad \text{eq. (5.2)}$$

Here A, A**, and Φ_B are the diode active area, effective Richardson constant, and barrier height (eV), respectively. The effective Richardson constant here is the value of universal Richardson constant multiplied with the correction factor associated with the semiconductor material used in the device. It should be noted that the above expression considers the thermionic emission as the main transport mechanism ($n \rightarrow 1$). One of the disadvantages of using the intercept to

extract the value is the noise from the measurement. At a very low current level, the noise could dominate the measured current, hence could provide deviation from the true value.

The ideality factor is commonly extracted according to the following relation:

$$n = \frac{q}{kT}\frac{dV}{d\ln(I)}$$

This expression omits the effect of series resistance of the diode, therefore the dV/dln(I) expression needs to be evaluated in the linear low current region, where the effect of any series resistance is minimal. If the series resistance is large, the region where the plot is linear is very small, thus making it harder to determine the ideality factor. Moreover, the shunt resistance of the diode which can dominate the current at low bias is assumed to be infinity.

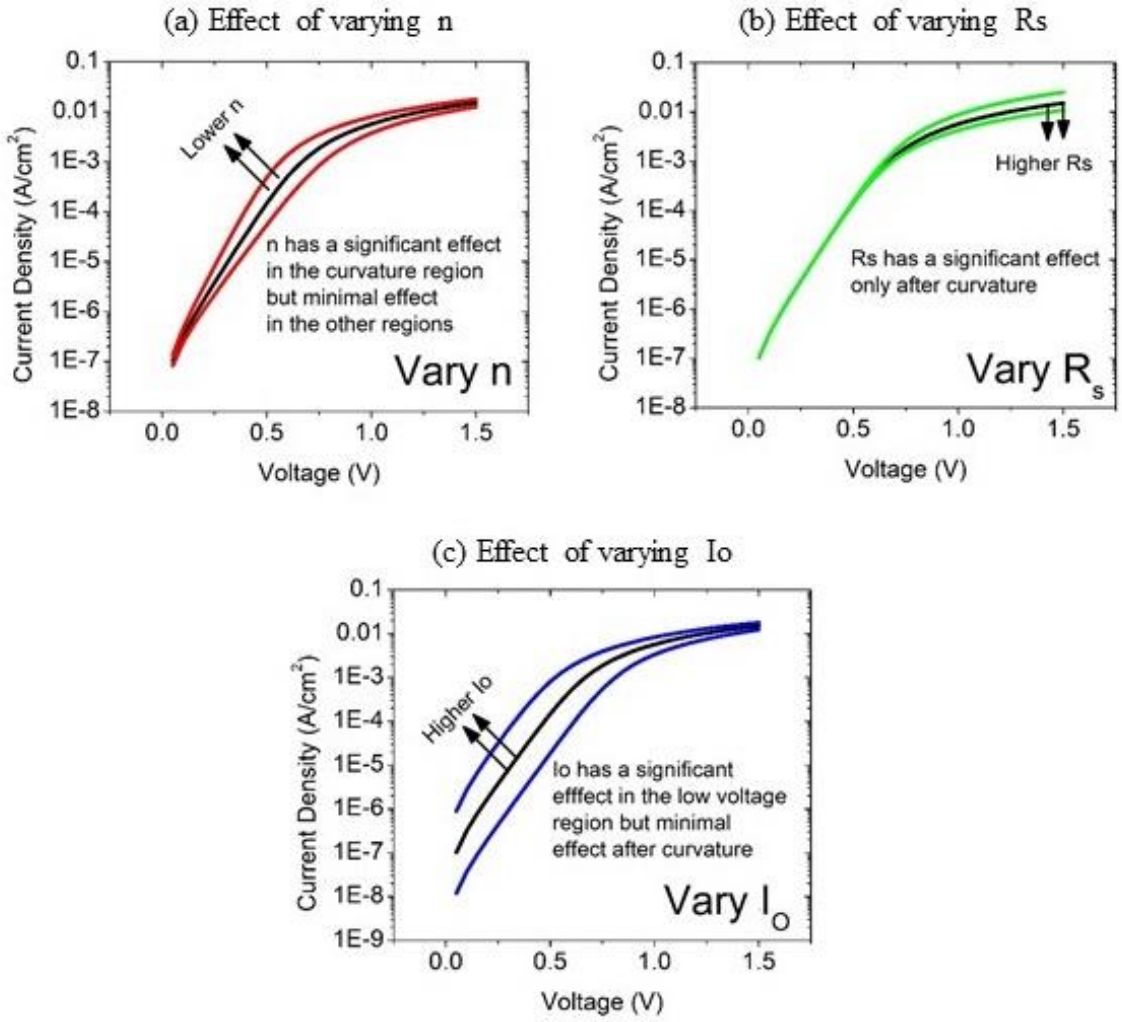


Figure 5.14: Effects of varying specific parameters whilst maintaining other parameters as constant on the overall shape of the graph.

Whilst the literature appears to agree with the method of extracting the saturation current and ideality factor, for series resistance, multiple methods have been proposed and used in the

literature. Norde [81] has proposed to extract the series resistance from the minimum of the auxiliary function *F(V)*, however there can exist several minimums and it was assumed that the ideality factor is unity, which is not the case for most diodes. Few improvement methods [82][83] were suggested but each of them failed to take into account the variation of the ideality factor and barrier height with temperature. Cheung and Cheung [84] have proposed a method in which the resistance is extracted from the curvature region of the I-V curve, however few published work [85][86] argue that this method could produce inaccurate results and is very sensitive to noise. Werner [86] has proposed a method by including the shunt conductance of the diode, however this method suffers from inaccuracy due to the fact that the reverse bias current is not linear for shunt conductance determination and few issues with evaluating the forward conductance as highlighted by E.K Evangelou *et. al*. [85]. Jung and Guziewicz [87] have proposed a method in which both shunt and series resistance can be determined simultaneously by using the Lambert W function, however the method is complicated and the effect of shunt resistance can actually be omitted in the conduction process if it is in the GOhm range. Herein, a simple curve fitting method based on eq. (5.1) is proposed and utilised to extract all 3 parameters, which is suitable for all types of diode.

In order to implement the curve fitting method in the equation, the effects of each parameter to the overall shape of the curve was first investigated. The effects of varying the value for these 3 parameters whilst maintaining the magnitude of other parameters as a constant are shown in Figure 5.14. From the figure, it can be observed that each of these 3 parameters significantly affect different regions of the curve, which makes the fitting method in the diode equation easier and simpler. This also means that there is only one combination of all parameters that can produce a good fit. The saturation current only significantly affects the low voltage region, in particular the magnitude of the starting point of the curve from 0 V. The ideality factor mainly affects the area around the curvature, in particular the extent of the bending up until the curvature, and the series resistance have a significant effect on the area after the curvature, where the resistance starts to dominate the current. From this, the fitting method is proposed as follows; first the saturation current was estimated from the starting point of the curve, next by using the estimated saturation current, the ideality factor is varied whilst maintaining the series resistance as 0 Ω until a good fit from the low voltage region up until the curvature can be obtained (this region should be almost linear in a semilog plot), and finally the series resistance is slowly increased until a good fit for the overall curve is obtained. After this, if needed, all 3 parameters can be varied to produce a better fit. As can be seen from eq. (5.1), the current term

appears twice in the equation, which makes the plotting difficult since the current needs to be solved iteratively. To counter this issue, a short programme was written in Wolfram Mathematica to plot the curve when each value is being varied. The programme was provided by Prof. John Wager of Oregon State University and is shown in Appendix 4.

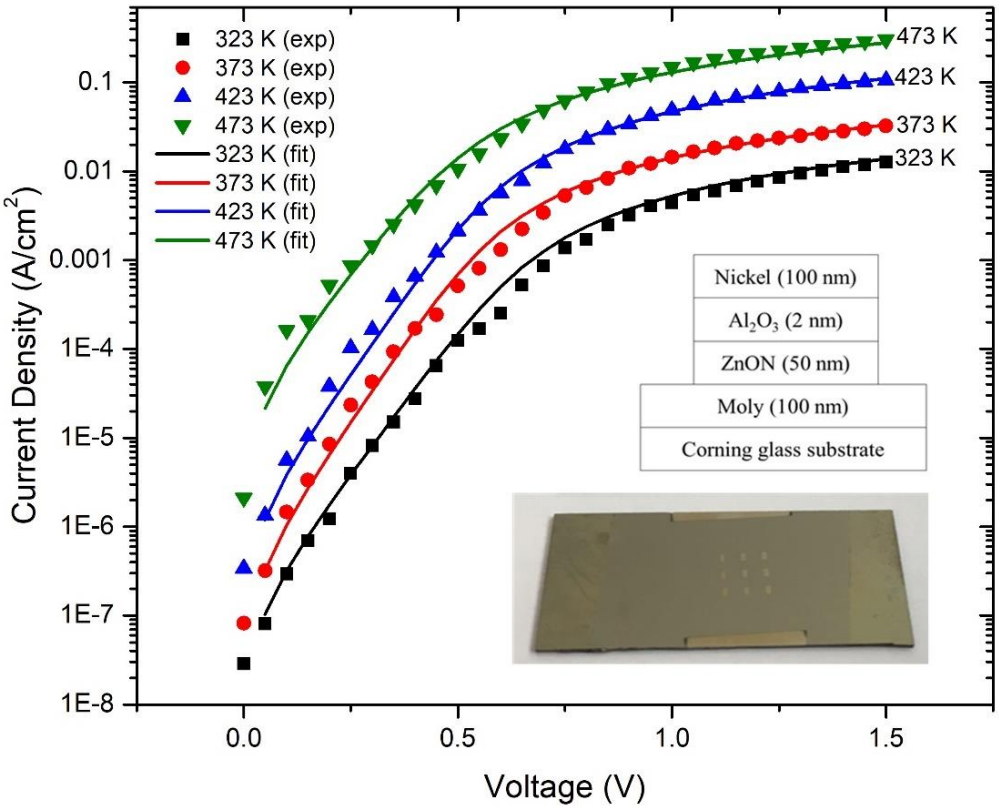


Figure 5.15: Experimental and fitted curve for J-V temperature dependent measurements.

Figure 5.15 shows the J-V results in forward bias for the diode at all four temperatures. It can be observed that the J-V characteristic depends strongly on temperature, depicting the usual trend of the saturation current increasing with temperature. The curvature starts to form at around 0.5 V, indicating the effect of series resistance starting to dominate the current at this voltage. Using the proposed 3-parameter fitting method for V > 0 V yield the solid coloured lines, which can be observed to produce good fits for the measured J-V curves. The extracted parameters from all curves are tabulated in Table 5.2. From the table, it can be observed that these parameters vary strongly with temperature. The barrier height was extracted by using eq. (5.2). The Richardson constant for the ZnON semiconductor was calculated based on the following relation:

$$A^{**} = \frac{4\pi q m^{*} k^{2}}{h^{3}}$$

Here h is a Planck constant and m* is the effective mass of the electron. We use the value for effective mass of the electron for ZnON film as reported by Ryu *et al*. [79] and Ok *et al*. [80], i.e. $m^* = 0.19\ m_e$, where m_e is the rest mass of an electron, yielding the constant to be 22.8 A/cm^2K^2. It should be noted that the value of effective mass of the electron in the fabricated semiconductor film may differ from the reported values due to the different fabrication conditions used in this thesis and in the reported work.

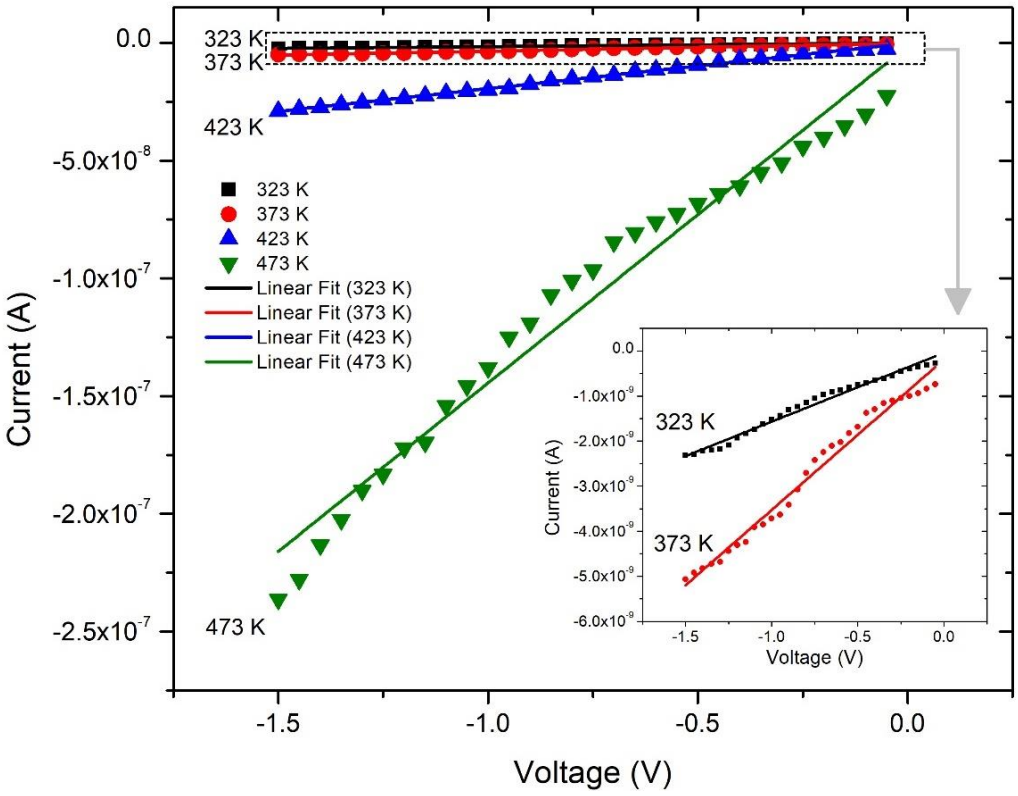
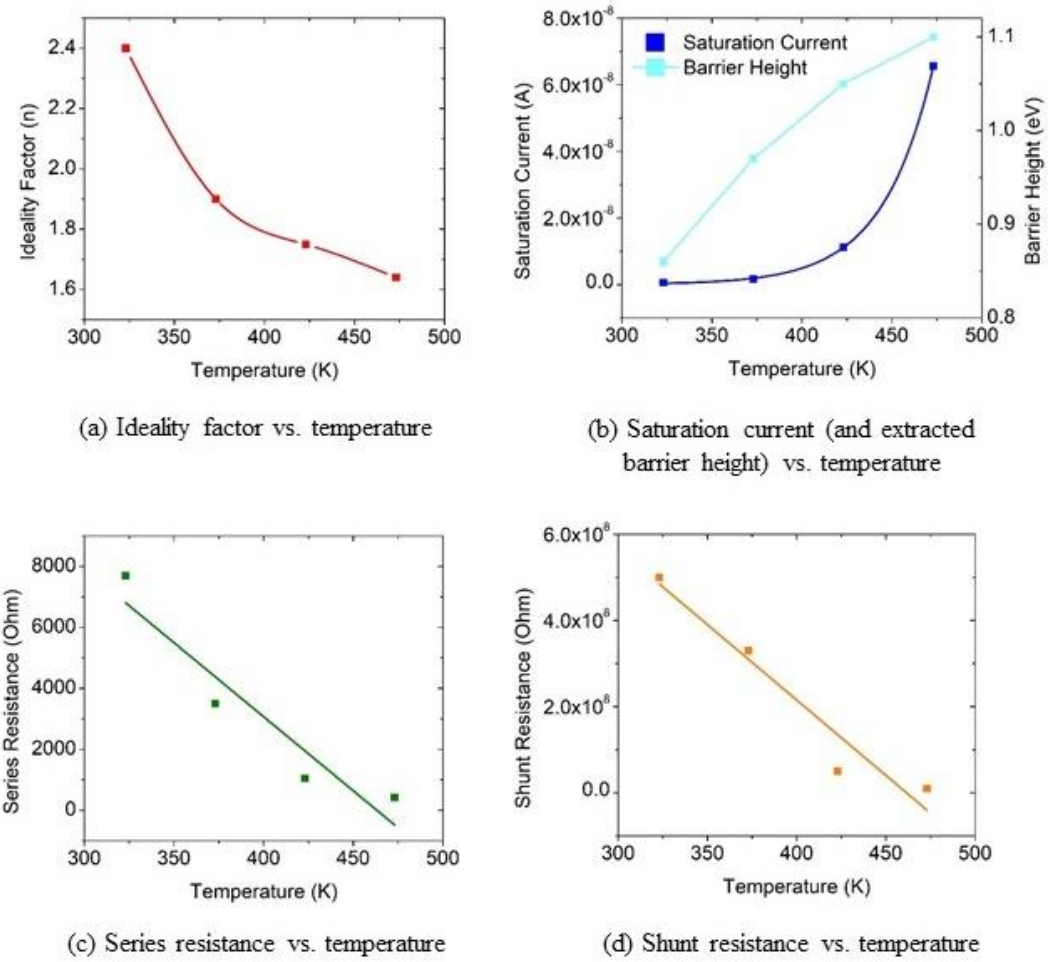


Figure 5.16: Temperature dependent reverse bias experimental and fitted I-V data.

Next, the reverse trend against temperature was investigated and is shown in Figure 5.16. Similar to the forward bias characteristic, the reverse trend shows a great dependence on temperature and the current increases with temperature. No sign of saturation is observed which is due to the effect of image force lowering of the barrier height of the diode [88]. Another interesting observation from the measurement is that the trend at each temperature shows an almost linear behaviour, which suggests that the reverse current is dominated by the shunt resistance of the diode, in particular this trend suggests the existence of a parallel resistive leakage path in this diode [89]. Werner [86][90] has suggested that the effect of parallel conductance is exceptionally more dominant in reverse bias and high barrier diode (> 0.83 eV), which agrees with this experiment. From this, the linear fit of each line was extrapolated and the fit was used to estimate the shunt resistance. These values are tabulated in Table 5.2.

Table 5.2: Extracted parameters from the curve fitting method.

Temp. (K)	I_o (A)	n	R_S (Ω)	Φ_B (eV)	R_{shunt} (GΩ)
323	6.15×10^{-10}	2.43	7700	0.86	0.50
373	1.68×10^{-9}	1.90	3550	0.97	0.33
423	1.12×10^{-8}	1.72	1050	1.04	0.05
473	6.56×10^{-8}	1.65	420	1.10	0.01



(a) Ideality factor vs. temperature

(b) Saturation current (and extracted barrier height) vs. temperature

(c) Series resistance vs. temperature

(d) Shunt resistance vs. temperature

Figure 5.17: Trends of each extracted parameter against temperature.

All of the five extracted parameters; saturation current, barrier height, ideality factor, series and shunt resistance are temperature dependent parameters and the trends of each of these parameters are plotted against the temperature in Figure 5.17. The saturation current increases with temperature, which shows the expected behaviour as more carriers are generated at a higher temperature. The barrier height shows an interesting trend; it increases with temperature. This is against the typically negative temperature coefficient of II-IV compound

semiconductor. This disagreement has been observed in numerous literature [91]–[93] and the main reason is due to the barrier height inhomogeneities around the insulator-semiconductor interface. In a model developed by Tung [94], a scattered region of 'patches' with a distribution of lower barrier heights than the main barrier height are assumed to exist at the junction. These patches may result from atomic defects such as grain boundaries and facets or from high electric field at the edge of the diode. In the barrier height inhomogeneity model, the current mechanism is assumed to be thermionic emission over an inhomogeneous barrier. The area of these patches might be much smaller than the total area of the diode. At high temperatures, the current is dominated by the thermionic emission over the main barrier because of high current density and the transport through these patches becomes gradually important with decreasing temperature, hence explaining the variation of the effective barrier height with temperature. The ideality factor decreases with increase in temperature, suggesting that other transport mechanisms apart from thermionic emission are more dominant at lower temperatures. These include generation-recombination near the space charge region and electron tunnelling through the barrier and across the thin insulating layer. As the temperature increases, more electrons are being emitted over the barrier hence the ideality factor approaches unity. It can also be observed that the values for the ideality factor are significantly high, suggesting the presence of bias dependent Schottky barrier height and image force lowering. The shape of the ideality factor curve against the temperature is almost reciprocal, which agrees with the T_0 anomaly effect. Both series and shunt resistance decrease with an increase in temperature, which is expected as at higher temperatures, the conductivity of the semiconductor is being enhanced as more free carriers are available. The series resistance of the diode is significantly high, even in high temperature, and this would limit the electrical performance of the diode. The series resistance from this diode arises from the contact resistance, semiconductor bulk resistance, and interfacial layer resistance. It is suspected that the semiconductor bulk resistance and the interfacial layer resistance significantly contribute to the overall series resistance. Furthermore, the high temperature annealing process is also suspected to cause the nickel from the top metal contact to diffuse to the semiconductor and contribute to the increase in this series resistance. In this experiment, the device was annealed for 2 hours at a moderately high temperature (250 °C), therefore the high resistance could be attributed to this. The voltage drop across the interfacial layer is also reflected in the magnitude of the series resistance and ideality factor [89]. The voltage drop across this layer will increase both the ideality factor and series resistance, which agrees with the trend of these two parameters in this experiment. Although the reverse bias trend is dominated by shunt resistance, the calculated magnitude of the

resistance is very high, therefore unlike the series resistance, the shunt resistance would not hinder the performance of the diode. It is suspected to arise from the existence of a leakage path around the edges of the device. In this experiment, the same shadow mask was used to pattern the layers, therefore there is a high possibility of leakage path around the edges to occur. It was also suggested by some published work that the shunt resistance could also be due to the crystal defects [95].

5.3.3 Room Temperature I-V and C-V Measurements

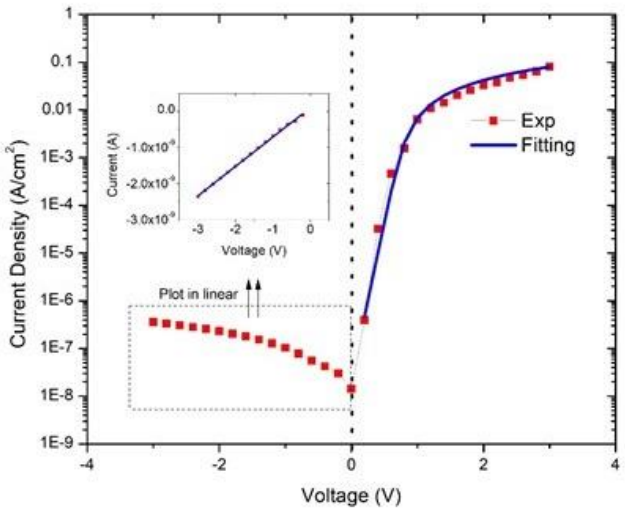
In the final results section in this chapter, the I-V and C-V measurement results for the diode are presented and discussed. The method proposed to extract the parameters of the diode from the I-V curve in the previous section is implemented. From the C-V measurement results, the carrier concentration is determined and discussed.

a. I-V Measurements

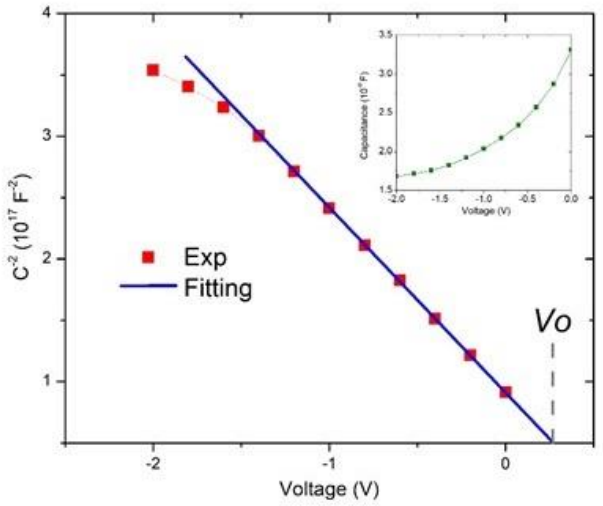
The performance of the diode was then measured in an uncontrolled room temperature environment under a dark condition and the voltage was swept from -3 V to 3 V at 0.2 V intervals. The J-V plot is shown in Figure 5.18 (a). The diode shows typical rectifying behaviour (exponential increase of current in forward bias and weak dependence in reverse bias) with a threshold voltage of around 0.75 V and leakage current density of 0.4 $\mu A/cm^2$ at -3 V. It has been suggested that the introduction of a thin interfacial layer between the metal and semiconductor is not only able to reduce the leakage current, but could also possibly shift and increase the threshold voltage [75]. This could explain why the threshold voltage of the fabricated diode is quite high.

The 3-parameter curve fitting method was implemented to extract all 3 main parameters for the room temperature measurement. From this, a good fit was obtained and the extracted parameters are as follows; ideality factor of 2.55, saturation current of 1.59×10^{-10} A (yielding a barrier height of 0.83 eV), and series resistance of 3800 Ω. Similar to before, the reverse bias current is almost linear as shown in Figure 5.18 (a), and the magnitude of the shunt resistance determined from this is 1.3 GΩ. All values agree with the trends obtained from the previous temperature dependent section, except for the series resistance. This is mainly due to the effects of temperature dependent measurements that were carried out on the sample after room temperature measurement. Unlike room temperature measurement, the temperature dependent measurement was carried out at high temperature in low pressure chamber and the period in

which the sample was subject to high temperature was significantly longer to ensure that the sample reached the desired temperature, thus it might change the behaviour of the device.



(a) J-V experimental and fitted data at room temperature



(b) C-V experimental, $1/C^2$ experimental and fitted data at room temperature

Figure 5.18: J-V and C-V data and analysis at room temperature.

Table 5.3: Extracted parameters from the curve fitting method.

Parameter	Magnitude
Ideality factor (n)	2.55
R_{series}	3800 Ω
R_{shunt}	1.3 GΩ
Φ_B (I-V)	0.83 eV
Φ_B (C-V)	0.86 eV

b. C-V Measurements and Carrier Concentration

The C-V characterisation was done to determine the carrier concentration and zero bias barrier height. The C-V sweep was carried out in a dark environment at 1 MHz with an ac modulation voltage of 30 mV. At this frequency, the effect of interface state is omitted since the carrier lifetime (τ) is larger than the measured period ($1/2\pi f$). To determine the carrier concentration and barrier height, the $1/C^2$-V plot in the reverse biased condition was constructed according to the following relation and is shown in Figure 5.15 (b):

$$\frac{1}{C^2} = \frac{2(V_R + V_O)}{q\varepsilon_s N_C A^2}$$

Here, V_R is the reverse biased voltage, V_O is the built-in potential and is determined from the x-intercept of the $1/C^2$-V plot, ε_s is the dielectric constant of the semiconductor, and N_C is the carrier concentration. As can be observed from Figure 5.18 (b), the $1/C^2$ against V plot in the reverse biased condition yields a straight line. This linearity shows that at the measured frequency, the interface states and the inversion layer charge do not significantly contribute to the diode capacitance. By rearranging the expression, the following relation can be obtained and the slope from the plot was used to determine the carrier concentration:

$$\frac{d(C^{-2})}{dV} = \frac{2}{q\varepsilon_s N_C A^2}$$

The barrier height was determined based on the following relation:

$$\Phi_b = V_0 + \frac{kT}{q} + \Phi_n$$

where Φ_n is the Fermi energy measured from the conduction band edge. From this, the calculated carrier concentration and barrier height are 2.15×10^{18} cm^{-3} and 0.86 eV, respectively. The small discrepancy of the barrier height obtained from C-V and I-V methods is due to the nature of the measurement. The C-V method is less sensitive to potential fluctuations at length scale less than the space-charge width and it averages over the whole area. However, the direct current in the I-V method increases exponentially with barrier height, and thus is more sensitive to the detailed barrier distribution at the interface. Several other reasons include the possibility of the existence of an interfacial native oxide layer near the insulator-semiconductor interface and barrier height inhomogeneities.

5.3.4 Comments on the Overall Performance of the Diode

The fabricated diode is intended for power circuits in energy harvesting applications. In this final section, the performance of the diode is discussed and compared with other published

work. In order to be utilised in power circuits such as rectifier and power converter, few characteristics of the diode are important. These include turn on voltage, series resistance, forward current, forward and reverse breakdown voltage, leakage current, rectification ratio, and maximum operating frequency. A summary of this work and a few related published works is presented in Table 5.4.

For the diode structure, most of the work focused on a p-n diode, which requires intricate and expensive fabrication technique and lengthy processes due to multiple different layers, unlike the Schottky diode which only requires one deposition of the semiconductor active layer and metal contact (and an insulator for MIS Schottky diode). The thickness plays an important role as it is one of the factors that enable flexibility. It can be seen from Table 5.4 that the diode produced in this work has one of the best thicknesses. In terms of performance, the diode has a moderate turn on voltage and forward current density, low leakage current density, and good rectification ratio. However, a comparison for breakdown voltage cannot be drawn as this was not reported or stated in most of the published work. Nevertheless, our test has shown that the fabricated diode has a good operating voltage range (-25 to 25 V). Although the turn on voltage is slightly higher and the forward current density is slightly smaller than some reported work, no important issues nor significant effects can be foreseen as the intended application for this diode is for energy harvesting, where the voltage and current are expected to be high and low respectively, such as the output produced by a piezoelectric transducer and electromagnetic micro-generator. The only limiting factor of the performance of the diode is the series resistance. Similar to the breakdown voltage, a comparison cannot be drawn as this value is not reported in the literature. However, our diode shows a very high resistive behaviour, which makes it unsuitable to be used in power circuits, especially for high current application. Overall, we believe that the only issue with the diode is the series resistance, and provided the series resistance can be further reduced, we believe that this diode is suitable to be used in power circuits in energy harvesting applications. The future work will focus on reducing the series resistance of the diode, and at the same time exploring the possibility of other semiconductor material in the same group to be used in the same intended applications.

Table 5.4: Comparison between diode in this chapter and other published work.

Publication	Diode Structure	Layer Material	Thickness (nm)	Turn-on Voltage (V)	Break-down Voltage (V)	Leak. Current Density (A/cm^2)	For. Current Density (A/cm^2)	Rectification Ratio
B V Mistry *et al.* (2011) [96]	p-n	p-NiO / n-ITO	160	0.06	-	0.15×10^{-3} at -5 V	3.75 at 0.35 V	-
A N Banerjee and K K Chattopadhyay (2008) [97]	p-n	p-$CuAlO_2$ / n-ZnO:Al	1100	0.8	-	3×10^{-6} at -4 V	0.1×10^{-3} at 5 V	50 at ± 2 V
B S Kang *et al.* (2008) [98]	p-n	p-CuO / n-$InZnO_x$	-	0.5 – 0.7	-	35×10^{-3} at -2.45 V	35×10^{3} at 2.45 V	10^6 at ± 2.45 V
B N Pal *et al.* (2008) [99]	p-n	p-pentacene / n-ZnO	200 nm (excluding n-ZnO thickness)	1.5	25 (forward)	53×10^{-3} at -5.5 V	160 at 5.5 V	3000 at ± 5.5 V
R S Ajimsha *et al.* (2007) [100]	p-n	p-$AgCoO_2$ / n-ZnO	200	0.5 – 0.7	-	185.7 at -5.5 V	1.3×10^{3} at 1.5 V	7 at ± 1.5 V
D S Kim *et al.* (2006) [101]	p-n	p-$CuAlO_2$ / n-ZnO	400	0.3	-	2.5×10^{-3} at -4 V	0.1 at 4 V	40 at ± 4 V
A S Juarez *et al.*(2005) [102]	p-n	p-SnS / n-SnS_2	500	0.6 – 0.8	-	3.98×10^{-3} at -1 V	1.19 at 1 V	300 at ± 1 V
S Steudel *et al.* (2005) [103]	MS (organic)	Au / Pedot:PSS - Pentacene / Al	570	2 – 4	19 (forward) and -30 (reverse)	N/A	150 at 5V	-
A Kudo *et al.* (1999) [104]	p-n	p-$SrCu_2O_2$ / n-ZnO	1300	0.3 – 0.6	-	-	-	80 at ± 1.5 V
This work	MIS	Ni / Al_2O_3 / ZnON	252	0.6 - 0.9	25 (forward) and -25 (reverse)	0.4×10^{-6} at -3 V	3.79×10^{-3} at 3 V	9500 at ± 3 V

5.4 Summary

In this chapter, the low temperature fabrication of a ZnON thin film diode in an MIS structure is presented. The reasons behind selecting the ZnON semiconductor and MIS diode structure is discussed. From multiple fabrications, it was demonstrated that good reproducibility can be attained despite the amorphous structure and limited controllability over the reaction processes. Post deposition annealing treatment has been carried out and the effects of different temperature and duration were investigated. From this, it was determined that annealing the device at 250 °C for 2 hours leads to the enhancement of the device performance.

From the temperature dependent I-V measurements, the parameters for the diode were extracted based on the proposed 3 parameter curve fitting method. From this, the ideality factor, saturation current, barrier height, and series resistance were extracted. The trends of these parameters with temperature were investigated and discussed. The high ideality factor indicates that thermionic emission is not the main current transport mechanism in the diode.

From room temperature I-V measurements, the proposed 3 parameter curve fitting method was used to extract the main parameters, and the trends of these parameters with the previous parameters obtained from the temperature dependent I-V measurements were discussed. The room temperature C-V measurements at high frequency enable determination of barrier height and carrier concentration of the semiconductor.

Finally, the overall performance of the diode is presented and discussed. The performance was then compared with other relevant published work in this field. It was concluded that although the overall performance and some of the parameters of the diode are better than other reported work, the series resistance would hinder the performance of the diode if this diode were to be used in power circuit applications. Overall, this work has paved a possibility of integrating this semiconductor material and device into the pico-grid system.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

In this thesis, an integrated low power energy harvesting system specifically designed for WSN and WBAN applications is proposed and the proof-of-concept pico-grid system is presented. This system is designed to be capable of delivering power simultaneously from multiple sources at the same time to the target load. Furthermore, due to the requirements of the applications, few other necessary features such as plug-and-play functionality, equal load sharing, energy storage integration for charging and discharging mechanism, and portability are presented and discussed. A side project aiming to fabricate a thin film diode at low temperatures in order to achieve the flexibility feature in a rectifier circuit with the final objective to be integrated in the final pico-grid system is also presented.

The contents of this thesis can be segregated into two main parts; the first part focuses on the development of the system itself, from the discussion of the load sharing mechanism to the presentation of the first wearable prototype. The first part comprises Chapter 2 to Chapter 4. The second part focuses on the side project and presents the work related to the fabrication and characterisations of the device. These work are presented in Chapter 5. Separate key findings, contributions, and concluding sections are presented for both parts.

6.1.1 Key Findings, Contributions, and Conclusion for Part 1

The key findings, contributions, and conclusion for part 1 are summarised as follow:

- For a parallel connected power converter system, a load sharing mechanism is needed to regulate the power flow between converters in the system. In this thesis, a voltage droop method is proposed. This method introduces a virtual impedance in the output side of a converter connected in parallel with another converters to provide a load sharing regulation.
- With the time-varying nature of the output power for energy harvesters, the voltage droop mechanism integrated in the power converters responsible to regulate the output voltage of these harvesters also need to be time-varying and capable of adjusting automatically to the variation of the power of the harvesters. A method for a self-adjusted voltage droop mechanism is proposed for solar panel and TEG energy harvesting scheme by introducing a variable resistor whose resistance varies in the same way as the energy source for the harvesters in the voltage droop feedback loop. LDR and thermistor are selected for the solar panel and TEG scheme, respectively. Through a series of presented calculations, specific LDRs and thermistors are chosen to meet the requirements of the energy harvesting scheme and the power converter circuit. A series of experiments is carried out and a self-adjusted voltage droop mechanism for these two harvesting schemes are successfully demonstrated. The magnitude of the droop is shown to almost accurately follow the variation in the output power of the harvesters, with a small error attributed to the deviations of the actual resistance value for the LDRs and thermistors from the required resistance value in the full range of the expected output power of the energy harvesters. The proposed self-adjusted voltage droop mechanism is relatively simple and only relies on the operation of passive components to accurately follow the variation in input power.
- The same concept is also further demonstrated to work for MPPT functionality.
- A full test for the parallel connected converters is carried out to test the load sharing accuracy of the proposed concept. Power from all converters is simultaneously delivered to the load. A maximum load sharing error of 5 % (in terms of input rated power) is demonstrated, indicating a successful load sharing operation. The system is also shown to possess an inherent plug-and-play capability for both the harvesters and load. Furthermore, due to the nature of the voltage droop mechanism, the bus voltage can be used as an indicator for the loading magnitude in the system.
- Since the proposed energy harvesting scheme has an intermittent output power, a storage system comprised of a rechargeable battery pack and a supercapacitor pack is integrated in

the system to ensure a continuous power is available for the load. This storage system needs to be charged when excess power is available in the system, and needs to be discharged to support the load demand when the loading level is high/available power in the system is low. In order to achieve this, a method for discharging and charging based on the level of the bus voltage is proposed and presented. A test is carried out to test the operation of the proposed method and successful charging and discharging operations are accomplished.

- Several important operations such as start-up, no source condition, no load condition, and load shedding mechanism are presented and successfully demonstrated.
- The first on-bench prototype is built from the integrated system. The performance of the prototype is successfully demonstrated and an almost perfect load sharing is achieved. The energy storage system is shown to absorb the power from the system when the power level is high and deliver power to the system when the power level is low. The efficiency for the energy storage system is relatively high for low power applications (> 75 %), however the efficiency of the power converter for the harvesters is relatively low (< 50 %) due to the high power consumption of the droop feedback circuitry.
- The first wearable prototype is built from the on-bench prototype. The system is shown to perform according to expectations. However, since the prototype is not optimised for real world applications, few recommendations are suggested.

Overall, the main objectives for part 1 have been successfully achieved. An equal load sharing mechanism is successfully shown and a self-adjusted voltage droop mechanism based on a novel concept is introduced and successfully demonstrated. Two main contributions from this part are; (1) the introduction and demonstration of the self-adjusted voltage droop mechanism based on variable resistor (passive component) and suitable for low power applications and (2) the introduction of the pico-grid system for WSN and WBAN applications.

6.1.2 Key Findings, Contributions, and Conclusion for Part 2

The key findings, contributions, and conclusion for part 2 are summarised as follow:

- The low temperature fabrication of ZnON MIS diode is presented. The whole structure can be fabricated at room temperature, except for the thin insulator which is deposited at a higher temperature (250 °C). This insulator is intentionally sandwiched in between the metal and semiconductor to further improve the electrical performance of the diode. However, in actual applications, this insulator can be replaced with any other high quality insulator that can be deposited at lower temperatures (this cannot be done in this thesis due to the

unavailability of material and facility for this purpose). The low temperature fabrication and the thin film structure means the actual device can be fabricated on a flexible substrate, opening up the possibility of fabricating a fully flexible thin film rectifier circuit.

- The I-V characterisation results obtained from 4 different fabrication batches undergo similar fabrication processes suggesting that the I-V performance of the diode is reproducible and within 20 % maximum deviations from each other. The deviations can be attributed to the limited controllability over the reaction processes during the deposition of the ZnON film.
- The effects of annealing to the performance of the diode, in particular in the forward bias condition are investigated. It is determined that annealing the sample at 250 °C for 2 hours in atmospheric pressure produces the best performance sample in terms of the magnitude of forward bias current.
- From the temperature I-V measurement results, a novel 3-parameter curve fitting method to extract important parameters of the diode is proposed. From this method, the ideality factor, series and shunt resistance, and barrier height are successfully extracted and the trends of these parameters with temperature are discussed. One important observation from the data obtained from the measurements is the magnitude of the series resistance of the diode. The extracted series resistance value for the diode is significantly high, and is suspected due to the contribution from the resistance of the interfacial layer, semiconductor film, and also due to the possible oxidation and diffusion of nickel into the semiconductor layer. In actual rectifier circuit application, this high series resistance would limit the magnitude of the forward current hence will degrade the efficiency of the conversion operation.
- The parameters extracted from the I-V characterisation results obtained from room temperature measurement agree with the expected trends, except for the series resistance. This is suspected possibly due to the nature of the measurement and the post heating effects from the temperature dependent I-V measurements carried out before. From the C-V measurements, the barrier height and carrier concentration are determined. The magnitude of barrier height obtained from the C-V measurements is in a good agreement with the magnitude of the same parameter obtained from the I-V measurements.
- The general performance of the diode in terms of the turn-on voltage, rectification ratio, thicknesses, leakage current density, and reverse breakdown voltage is compared with some other relevant and similar published work. It is determined that although other parameters of the diode possess a comparable or better performance than some of the published work,

the significantly high series resistance of the diode is deemed to be the main factor that would downgrade the overall performance of the diode, should the diode be implemented as a rectifier circuit.

Overall, the main objectives for part 2 have not been fully achieved. Although the performance of the device has been successfully demonstrated, the high series resistance presents in the device make it unsuitable to be implemented in the rectifier circuit since the overall efficiency will be significantly reduced. Three main contributions from this part are; (1) the first demonstration of a successful thin film diode fabricated from a ZnON semiconductor with the possibility to be fully deposited at room temperature and (2) the proposal of a 3-parameter curve fitting method.

6.2 Future Work

Similar to the conclusion section, this section is also separated into two different parts.

6.2.1 Future Work for Work Package Part 1

Most of the future work for the pico-grid system is focused on the improvements of the prototype in order to be implemented for a real world applications. These have been presented in Section 4.3.3. These include the reconstruction of the whole circuitry on a flexible PCB, the integration of flexible passive components that can be achieved via printing/low temperature thin film/organic deposition technique, the use of conductive fibres to replace the connection wires, the integration of flexible solar panels and TEGs to replace the existing harvesters, and the use of flexible thin film battery and supercapacitor to replace the existing storage system. One of the most important future works is to integrate other possible energy harvesting schemes such as a piezoelectric generator, electromagnetic induction generator, and wireless power (flexible wireless coil receiver). Since these harvesting schemes would also require a variable and self-adjusted voltage droop mechanism, some other possible method to achieve this such as open circuit voltage sampling of the energy harvester need to be explored and investigated.

6.2.2 Future Work for Work Package Part 2

Due to the high resistance of the fabricated ZnON thin film diode, the diode is deemed unsuitable for a rectifier circuit. In order to possibly reduce this resistance, the metal used for the top metal contact should be changed to another metal (with work function > 4.2 eV) and the performance of the diode needs to be re-evaluated. Nickel is a very reactive metal and hence at high annealing temperature, there is a high possibility for this metal to diffuse through the

insulator and react with the semiconductor material. Furthermore, nickel is also easily oxidised and forms a p-type semiconductor. Any of these effects could occur during the fabrication process presented in this thesis, hence contributing to the increase in the magnitude of the series resistance. Moreover, since the work function of nickel is relatively high (5.1 eV), this causes the turn-on voltage of the diode to be high. By changing the top metal contact with another type of metal, two possible advantages can be achieved; the reduction in turn-on voltage and series resistance of the diode. Another possible improvement is to perform argon plasma treatment on the semiconductor film after the deposition process has finished.

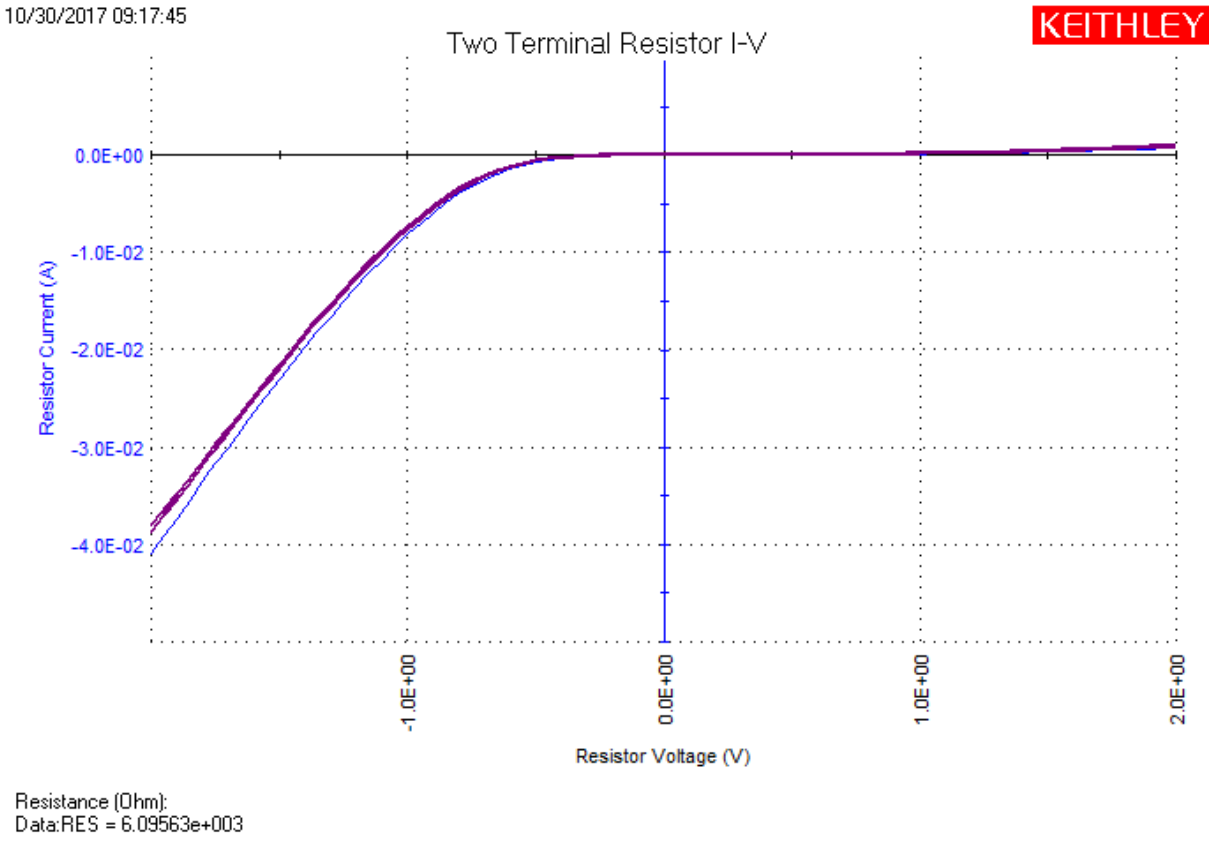


Figure 6.1: I-V characterisation result for the ISO MIS diode.

By the end of the PhD, it was discovered that a diode fabricated from another new oxide semiconductor material, indium silicon oxide (ISO) possesses better performance than the ZnON diode. The I-V characteristic of this diode in a similar structure and thicknesses to the ZnON diode except this time the ZnON layer was replaced with an ISO layer is presented in Figure 6.1. It can be observed that this diode possesses a lower turn-on voltage and lower series resistance when compared to the ZnON diode. This material can be deposited at similar room temperature and therefore, has a huge potential to be implemented in a flexible rectifier circuit. It should be noted that the presented I-V characterisation was done without any post fabrication

treatment performed to the film. Typically, an oxide semiconductor will demonstrate a superior property after annealing, and therefore this material can be further optimised.

References

[1] A. Demidenko, “Wearables Market Overview,” *Teslasuit*, 2017. [Online]. Available: https://teslasuit.io/blog/wearables/wearables-market-overview. [Accessed: 04-Feb-2018].

[2] T. Starner, “Human-powered wearable computing,” *IBM Syst. J.*, vol. 35, pp. 618–629, 1996.

[3] “Low power Wearables,” *RoweBots*, 2015. [Online]. Available: http://rowebots.com/en/solutions/low-power-wearables. [Accessed: 04-Feb-2018].

[4] R. Riemer and A. Shapiro, “Biomechanical energy harvesting from human motion: theory, state of the art, design guidelines, and future directions.,” *J. Neuroeng. Rehabil.*, vol. 8, p. 22, 2011.

[5] H. Im, H. G. Moon, J. S. Lee, I. Y. Chung, T. J. Kang, and Y. H. Kim, “Flexible thermocells for utilization of body heat,” *Nano Res.*, vol. 7, no. 4, pp. 1–10, 2014.

[6] C. H. Hyoung, Y. T. Kim, J. H. Hwang, and K. H. Park, “Energy harvesting from ambient electromagnetic wave using human body as antenna,” *Electron. Lett.*, vol. 49, no. 2, pp. 149–151, 2013.

[7] Q. Brogan, T. O. Connor, and D. S. Ha, “Solar and Thermal Energy Harvesting with a Wearable Jacket,” *2014 IEEE Int. Symp. Circuits Syst.*, pp. 1412–1415, 2014.

[8] Z. Lu, H. Zhang, C. Mao, and C. M. Li, “Silk fabric-based wearable thermoelectric generator for energy harvesting from the human body,” *Appl. Energy*, vol. 164, pp. 57–63, 2016.

[9] S. J. Kim, J. H. We, and B. J. Cho, “A wearable thermoelectric generator fabricated on a glass fabric,” *Energy Environ. Sci.*, vol. 7, no. 6, p. 1959, 2014.

[10] Z. Wang, V. Leonov, P. Fiorini, and C. Van Hoof, “Realization of a wearable miniaturized thermoelectric generator for human body applications,” *Sensors Actuators A Phys.*, vol. 156, no. 1, pp. 95–102, Nov. 2009.

[11] K. Ylli, D. Hoffmann, A. Willmann, P. Becker, B. Folkmer, and Y. Manoli, “Energy harvesting from human motion: Exploiting swing and shock excitations,” *Smart Mater.*

Struct., vol. 24, no. 2, 2015.

[12] Z. Tian, J. He, X. Chen, T. Wen, C. Zhai, Z. Zhang, J. Cho, X. Chou, and C. Xue, "Core–shell coaxially structured triboelectric nanogenerator for energy harvesting and motion sensing," *RSC Adv.*, vol. 8, no. 6, pp. 2950–2957, 2018.

[13] B. J. Kim, D. H. Kim, Y.-Y. Lee, H.-W. Shin, G. S. Han, J. S. Hong, K. Mahmood, T. K. Ahn, Y.-C. Joo, K. S. Hong, N.-G. Park, S. Lee, and H. S. Jung, "Highly efficient and bending durable perovskite solar cells: toward a wearable power source," *Energy Environ. Sci.*, vol. 8, no. 3, pp. 916–921, 2015.

[14] R. K. Tallos, Z. Wang, and J. L. Volakis, "Wi-Fi Energy Harvesting System Using Body-worn Antennas," *2014 IEEE Antennas Propag. Soc. Int. Symp.*, pp. 1405–1406, 2014.

[15] R. Negra, I. Jemili, and A. Belghith, "Wireless Body Area Networks: Applications and Technologies," *Procedia Comput. Sci.*, vol. 83, pp. 1274–1281, 2016.

[16] Y. Li and R. Shi, "An intelligent solar energy-harvesting system for wireless sensor networks," *Eurasip J. Wirel. Commun. Netw.*, vol. 2015, no. 1, pp. 1–12, 2015.

[17] P. Dziurdzia and J. Stepien, "Autonomous wireless link powered with harvested heat energy," *2011 IEEE Int. Conf. Microwaves, Commun. Antennas Electron. Syst. COMCAS 2011*, 2011.

[18] C. Alippi and C. Galperti, "An Adaptive System for Optimal Solar Energy Harvesting in Wireless Sensor Network Nodes," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 55, no. 6, pp. 1742–1750, 2008.

[19] D. Dondi, a. Bertacchini, D. Brunelli, L. Larcher, and L. Benini, "Modeling and Optimization of a Solar Energy Harvester System for Self-Powered Wireless Sensor Networks," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2759–2766, 2008.

[20] H. Guo, Z. Wen, Y. Zi, M. H. Yeh, J. Wang, L. Zhu, C. Hu, and Z. L. Wang, "A Water-Proof Triboelectric-Electromagnetic Hybrid Generator for Energy Harvesting in Harsh Environments," *Adv. Energy Mater.*, vol. 6, no. 6, pp. 1–7, 2016.

[21] Y. Wu, X. Zhong, X. Wang, Y. Yang, and Z. L. Wang, "Hybrid energy cell for simultaneously harvesting wind, solar, and chemical energies," *Nano Res.*, vol. 7, no. 11, pp. 1631–1639, 2014.

[22] L. Zheng, Z. H. Lin, G. Cheng, W. Wu, X. Wen, S. Lee, and Z. L. Wang, “Silicon-based hybrid cell for harvesting solar energy and raindrop electrostatic energy,” *Nano Energy*, vol. 9, pp. 291–300, 2014.

[23] S. Lee, S. H. Bae, L. Lin, S. Ahn, C. Park, S. W. Kim, S. N. Cha, Y. J. Park, and Z. L. Wang, “Flexible hybrid cell for simultaneously harvesting thermal and mechanical energies,” *Nano Energy*, vol. 2, no. 5, pp. 817–825, 2013.

[24] S. Lemey, F. Declercq, and H. Rogier, “Textile antennas as hybrid energy-harvesting platforms,” *Proc. IEEE*, vol. 102, no. 11, pp. 1833–1857, 2014.

[25] Y. K. Tan, S. Member, S. K. Panda, and S. Member, “Energy Harvesting from Hybrid Indoor Ambient Light and Thermal Energy Sources for Enhanced Performance of Wireless Sensor Nodes,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4424–4435, 2011.

[26] A. Romani, M. Filippi, and M. Tartagni, “Micropower design of a fully autonomous energy harvesting circuit for arrays of piezoelectric transducers,” *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 729–739, 2014.

[27] D. Carli, D. Brunelli, L. Benini, and M. Ruggeri, “An effective multi-source energy harvester for low power applications,” *2011 Des. Autom. Test Eur.*, pp. 1–6, 2011.

[28] M. Magno, D. Boyle, D. Brunelli, B. O. Flynn, E. Popovici, S. Member, and L. Benini, “Extended Wireless Monitoring Through Intelligent Hybrid Energy Supply,” *IEEE Trans. Ind. Electron.*, vol. 61, no. 4, pp. 1871–1881, 2014.

[29] J. Colomer-Farrarons, P. Miribel-Català, A. Saiz-Vela, and J. Samitier, “A Multiharvested Self-Powered System in a Low-Voltage Low-Power Technology,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4250–4263, 2011.

[30] C. Park and P. H. Chou, “AmbiMax : Autonomous Energy Harvesting Platform for Multi-Supply Wireless Sensor Nodes,” *2006 3rd Annu. IEEE Commun. Soc. Sens. Ad Hoc Commun. Networks*, pp. 168–177, 2016.

[31] T. Kang, S. Kim, C. Hyoung, S. Kang, and K. Park, “An Energy Combiner for a Multi-Input Energy-Harvesting System,” *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 62, no. 9, pp. 911–915, 2015.

[32] B. Sai Srujana, N. Neha, P. Mathews, and V. P. Harigovindan, “Multi-source energy

harvesting system for underwater wireless sensor networks," *Procedia Comput. Sci.*, vol. 46, no. Icict 2014, pp. 1041–1048, 2015.

[33] R. Morais, S. G. Matos, M. A. Fernandes, A. L. G. Valente, S. F. S. P. Soares, P. J. S. G. Ferreira, and M. J. C. S. Reis, "Sun, wind and water flow as energy supply for small stationary data acquisition platforms," *Comput. Electron. Agric.*, vol. 64, no. 2, pp. 120–132, 2008.

[34] M. Dini, A. Romani, M. Filippi, and M. Tartagni, "A Nano-Current Power Management IC for Low Voltage Energy Harvesting," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 1–1, 2015.

[35] C. Shi, B. Miller, K. Mayaram, and T. Fiez, "A multiple-input boost converter for low-power energy harvesting," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 58, no. 12, pp. 827–831, 2011.

[36] A. S. Weddell, N. J. Grabham, N. R. Harris, and N. M. White, "Modular plug-and-play power resources for energy-aware wireless sensor nodes," *2009 6th Annu. IEEE Commun. Soc. Conf. Sensor, Mesh Ad Hoc Commun. Networks, SECON 2009*, 2009.

[37] Y. Huang and C. K. Tse, "Circuit theoretic classification of parallel connected dc-dc converters," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 54, no. 5, pp. 1099–1108, 2007.

[38] "Ni-MH Battery Series," *Power Sonic Rechargeable Battery Product Page*. [Online]. Available: http://www.directindustry.com/prod/power-sonic/product-19906-438155.html. [Accessed: 18-Aug-2015].

[39] G. Gache, "What Makes Li-ion Batteries Burst into Flames," *Softpedia*, 2008. [Online]. Available: http://news.softpedia.com/news/What-Makes-Li-ion-Batteries-Burst-into-Flames-87778.shtml. [Accessed: 18-Aug-2015].

[40] "1000F / 2. 8V(EDLC) LS Ultra Capacitor," *LS MTRON LTD Product Page*. [Online]. Available: http://doogiejeong.fm.alibaba.com/product/108815297-105990409/1000F_2_8V_EDLC_LS_Ultra_Capacitor.html. [Accessed: 18-Aug-2015].

[41] S. Hobley, "3000 Farad Supercapacitor – Any Ideas?," *StephenHobley.com*, 2010. [Online]. Available: http://www.stephenhobley.com/blog/2010/09/30/3000-farad-supercapacitor-any-ideas/. [Accessed: 18-Aug-2015].

[42] I. Buchmann, “What’s the Best Battery?,” 2010. [Online]. Available: http://batteryuniversity.com/learn/article/whats_the_best_battery. [Accessed: 29-Jul-2015].

[43] C. Simpson, “Characteristics of Rechargeable Batteries,” *Natl. Semicond.*, pp. 1–12, 2011.

[44] A. Schneuwly and R. Gallay, “Properties and applications of supercapacitors From the state-of-the-art to future trends,” *Pcim2000*, pp. 1–10, 2000.

[45] P. Harrop and H. Zervos, “Batteries , Alternative Storage for Portable Devices,” *IdTechEx*, p. 217, 2009.

[46] “Technology Brief 8: Supercapacitors as Batteries,” 2013.

[47] C. Lerman, A. Horosov, and A. Kuperman, “Capacitor semi-active battery-ultracapacitor hybrid energy source,” *2012 IEEE 27th Conv. Electr. Electron. Eng. Isr. IEEEI 2012*, pp. 8–11, 2012.

[48] I. Sefik, D. a. Asfani, and T. Hiyama, “Electric double layer capacitor impact on the performance of Hybrid Electric Vehicle,” *2012 11th Int. Conf. Environ. Electr. Eng.*, pp. 102–107, May 2012.

[49] Y. Jia, R. Shibata, N. Yamamura, and M. Ishida, “A Control Method of Prolonging the Service Life of Battery in Stand-alone Renewable Energy System using Electric Double Layer Capacitor (EDLC),” *IEEE PEDS*, vol. 5, no. 5, pp. 228–233, 2005.

[50] B. Lawson, “State of Charge (SOC) Determination,” *Electropaedia*. [Online]. Available: http://www.mpoweruk.com/soc.htm. [Accessed: 15-Aug-2015].

[51] M. a. Alahmad and H. L. Hess, “Evaluation and analysis of a new solid-state rechargeable microscale lithium battery,” *IEEE Trans. Ind. Electron.*, vol. 55, no. 9, pp. 3391–3401, 2008.

[52] I. Buchmann, “Charging Lithium-ion Battery,” *Battery University*. [Online]. Available: http://batteryuniversity.com/learn/article/charging_lithium_ion_batteries. [Accessed: 01-Aug-2015].

[53] T. Leydecker, M. Herder, E. Pavlica, G. Bratina, S. Hecht, E. Orgiu, and P. Samorì, “Flexible non-volatile optical memory thin-film transistor device with over 256 distinct

levels based on an organic bicomponent blend," *Nat. Nanotechnol.*, vol. 11, no. 9, pp. 769–775, 2016.

[54] T. Georgiou, R. Jalil, B. D. Belle, L. Britnell, R. V. Gorbachev, S. V. Morozov, Y. J. Kim, A. Gholinia, S. J. Haigh, O. Makarovsky, L. Eaves, L. A. Ponomarenko, A. K. Geim, K. S. Novoselov, and A. Mishchenko, "Vertical field-effect transistor based on graphene-WS 2 heterostructures for flexible and transparent electronics," *Nat. Nanotechnol.*, vol. 8, no. 2, pp. 100–103, 2013.

[55] S. Park, S. H. Shin, M. N. Yogeesh, A. L. Lee, S. Rahimi, and D. Akinwande, "Extremely High-Frequency Flexible Graphene Thin-Film Transistors," *IEEE Electron Device Lett.*, vol. 37, no. 4, pp. 512–515, 2016.

[56] D. Ji, L. Jiang, X. Cai, H. Dong, Q. Meng, G. Tian, D. Wu, J. Li, and W. Hu, "Large scale, flexible organic transistor arrays and circuits based on polyimide materials," *Org. Electron. physics, Mater. Appl.*, vol. 14, no. 10, pp. 2528–2533, 2013.

[57] C. D. Sheraw, L. Zhou, J. R. Huang, D. J. Gundlach, T. N. Jackson, M. G. Kane, I. G. Hill, M. S. Hammond, J. Campi, B. K. Greening, J. Francl, and J. West, "Organic thin-film transistor-driven polymer-dispersed liquid crystal displays on flexible polymeric substrates," *Appl. Phys. Lett.*, vol. 80, no. 6, pp. 1088–1090, 2002.

[58] D. Liu and T. L. Kelly, "Perovskite solar cells with a planar heterojunction structure prepared using room-temperature solution processing techniques," *Nat. Photonics*, vol. 8, no. 2, pp. 133–138, 2014.

[59] C. Roldán-Carmona, O. Malinkiewicz, A. Soriano, G. Mínguez Espallargas, A. Garcia, P. Reinecke, T. Kroyer, M. I. Dar, M. K. Nazeeruddin, and H. J. Bolink, "Flexible high efficiency perovskite solar cells," *Energy Environ. Sci.*, vol. 7, no. 3, pp. 994–997, 2014.

[60] J. H. Heo, M. H. Lee, H. J. Han, B. R. Patil, J. S. Yu, and S. H. Im, "Highly efficient low temperature solution processable planar type $CH_3NH_3PbI_3$ perovskite flexible solar cells," *J. Mater. Chem. A*, vol. 4, no. 5, pp. 1572–1578, 2016.

[61] A. R. M. Siddique, R. Rabari, S. Mahmud, and B. Van Heyst, "Thermal energy harvesting from the human body using flexible thermoelectric generator (FTEG) fabricated by a dispenser printing technique," *Energy*, vol. 115, pp. 1081–1091, 2016.

[62] F. Suarez, D. P. Parekh, C. Ladd, D. Vashaee, M. D. Dickey, and M. C. Öztürk, "Flexible

thermoelectric generator using bulk legs and liquid metal interconnects for wearable electronics," *Appl. Energy*, vol. 202, pp. 736–745, 2017.

[63] Y. Ohya, S. Itoda, T. Ban, M. Decomposition, K. M. A. Salam, H. Konishi, S. Kwon, S. Bang, Y. Son, and R. L. Peterson, "Thin Film Transistor of ZnO Fabricated by Chemical Solution Deposition," pp. 13–15, 2001.

[64] R L. Hoffman, B. J. Norris, J. F. Wager, "ZnO-based transparent thin-film transistors.," *Appl. Phys. Lett.*, vol. 26, no. 1–2, pp. 25–27, 1989.

[65] P. F. Carcia, R. S. McLean, M. H. Reilly, and G. Nunes, "Transparent ZnO thin-film transistor fabricated by rf magnetron sputtering," *Appl. Phys. Lett.*, vol. 82, no. 7, pp. 1117–1119, 2003.

[66] E. Fortunato, A. Pimentel, L. Pereira, A. Gonçalves, G. Lavareda, H. Águas, I. Ferreira, C. N. Carvalho, and R. Martins, "High field-effect mobility zinc oxide thin film transistors produced at room temperature," *J. Non. Cryst. Solids*, vol. 338–340, no. 1 SPEC. ISS., pp. 806–809, 2004.

[67] M. Futsuhara, K. Yoshioka, and O. Takai, "Optical properties of zinc oxynitride thin films," *Thin Solid Films*, vol. 317, no. 1–2, pp. 322–325, 1998.

[68] B. Yao, D. Z. Shen, Z. Z. Zhang, X. H. Wang, Z. P. Wei, B. H. Li, Y. M. Lv, X. W. Fan, L. X. Guan, G. Z. Xing, C. X. Cong, and Y. P. Xie, "Effects of nitrogen doping and illumination on lattice constants and conductivity behavior of zinc oxide grown by magnetron sputtering," *J. Appl. Phys.*, vol. 99, no. 12, 2006.

[69] Y. Ye, R. Lim, and J. M. White, "High mobility amorphous zinc oxynitride semiconductor material for thin film transistors," *J. Appl. Phys.*, vol. 106, no. 7, 2009.

[70] E. Lee, A. Benayad, T. Shin, H. Lee, D.-S. Ko, T. S. Kim, K. S. Son, M. Ryu, S. Jeon, and G.-S. Park, "Nanocrystalline ZnON; High mobility and low band gap semiconductor material for high performance switch transistor and image sensor application.," *Sci. Rep.*, vol. 4, p. 4948, 2014.

[71] K. C. Ok, H. J. Jeong, H. S. Kim, and J. S. Park, "Highly stable ZnON thin-film transistors with high field-effect mobility exceeding 50 cm^2/Vs," *IEEE Electron Device Lett.*, vol. 36, no. 1, pp. 38–40, 2015.

[72] Y. Ye, R. Lim, H. You, E. Scheer, A. Gaur, H. C. Hsu, J. Liu, D. K. Yim, A. Hosokawa,

and J. M. White, “Development of high mobility zinc oxynitride thin film transistors,” *Dig. Tech. Pap. - SID Int. Symp.*, vol. 44, no. 1, pp. 14–17, 2013.

[73] H. Jeong, H.-S. Jeong, D.-H. Kim, C.-Y. Jeong, and H.-I. Kwon, “Effects of Post-Deposition Thermal Annealing Temperature on Electrical Properties of ZnON Thin-Film Transistors,” *IEEE Electron Device Lett.*, vol. 3106, no. c, pp. 1–1, 2016.

[74] E. Lee, T. Kim, A. Benayad, H. Kim, S. Jeon, and G. S. Park, “Ar plasma treated ZnON transistor for future thin film electronics,” *Appl. Phys. Lett.*, vol. 107, no. 12, 2015.

[75] E. Arslan, S. Bütün, Y. Safak, H. Uslu, I. Tascioglu, S. Altindal, and E. Özbay, “Electrical characterization of MS and MIS structures on AlGaN/AlN/GaN heterostructures,” *Microelectron. Reliab.*, vol. 51, no. 2, pp. 370–375, 2011.

[76] J. F. Wager and J. Robertson, “Metal-induced gap states modeling of metal-Ge contacts with and without a silicon nitride ultrathin interfacial layer,” *J. Appl. Phys.*, vol. 109, no. 9, 2011.

[77] M. K. Hudait and S. B. Krupanidhi, “Effects of thin oxide in metal-semiconductor and metal-insulator-semiconductor epi-GaAs Schottky diodes,” *Solid. State. Electron.*, vol. 44, no. 6, pp. 1089–1097, 2000.

[78] D. Klaitabtim, S. Pratontep, and J. Nukeaw, “Growth and characterization of zinc oxynitride thin films by reactive gas-timing RF magnetron sputtering,” *Jpn. J. Appl. Phys.*, vol. 47, no. 1 PART 2, pp. 653–656, 2008.

[79] M. Ryu, T. S. Kim, K. S. Son, H. S. Kim, J. S. Park, J. B. Seon, S. J. Seo, S. J. Kim, E. Lee, H. Lee, S. H. Jeon, S. Han, and S. Y. Lee, “High mobility zinc oxynitride-TFT with operation stability under light-illuminated bias-stress conditions for large area and high resolution display applications,” *Tech. Dig. - Int. Electron Devices Meet. IEDM*, vol. 717, no. 2006, pp. 112–114, 2012.

[80] K. C. Ok, H. J. Jeong, H. M. Lee, J. Park, and J. S. Park, “Comparative studies on the physical and electronic properties of reactively sputtered ZnO and ZnON semiconductors,” *Ceram. Int.*, vol. 41, pp. 13281–13284, 2015.

[81] H. Norde, “A modified forward I-V plot for Schottky diodes with high series resistance,” *J. Appl. Phys.*, vol. 50, no. 7, pp. 5052–5053, 1979.

[82] J. C. Manifacier, N. Brortryb, R. Ardebili, and J. P. Charles, “Schottky diode: Comments

concerning the diode parameters determination from the forward I-V plot," *J. Appl. Phys.*, vol. 64, no. 5, pp. 2502–2504, 1988.

[83] K. Sato and Y. Yasumura, "Study of forward I-V plot for Schottky diodes with high series resistance," *J. Appl. Phys.*, vol. 58, no. 9, pp. 3655–3657, 1985.

[84] S. K. Cheung and N. W. Cheung, "Extraction of Schottky diode parameters from forward current-voltage characteristics," *Appl. Phys. Lett.*, vol. 49, no. 2, pp. 85–87, 1986.

[85] S. E. Vol and G. Britain, "Extraction of schottky diode (and p-n junction) parameters from I-V characteristics," *Solid. State. Electron.*, vol. 36, no. 11, pp. 1633–1635, 1993.

[86] J. H. Werner, "Schottky barrier and pn-junction I/V Plots - Small signal evaluation," *Appl. Phys. A Solids Surfaces*, vol. 47, no. 3, pp. 291–300, 1988.

[87] W. Jung and M. Guziewicz, "Schottky diode parameters extraction using Lambert W function," *Mater. Sci. Eng. B Solid-State Mater. Adv. Technol.*, vol. 165, no. 1–2, pp. 57–59, 2009.

[88] S. Demirezen, Z. Sönmez, U. Aydemir, and S. Altndal, "Effect of series resistance and interface states on the I-V, C-V and G/ω-V characteristics in Au/Bi-doped polyvinyl alcohol (PVA)/n-Si Schottky barrier diodes at room temperature," *Curr. Appl. Phys.*, vol. 12, no. 1, pp. 266–272, 2012.

[89] M. Gökçen, S. Altndal, M. Karaman, and U. Aydemir, "Forward and reverse bias currentvoltage characteristics of Au/n-Si Schottky barrier diodes with and without SnO_2 insulator layer," *Phys. B Condens. Matter*, vol. 406, no. 21, pp. 4119–4123, 2011.

[90] V. Aubry and F. Meyer, "Schottky diodes with high series resistance: Limitations of forward I-V methods," *J. Appl. Phys.*, vol. 76, no. 12, pp. 7973–7984, 1994.

[91] H. Tecimer, A. Türüt, H. Uslu, S. Altindal, and I. Uslu, "Temperature dependent current-transport mechanism in Au/(Zn-doped)PVA/n- GaAs Schottky barrier diodes (SBDs)," *Sensors Actuators, A Phys.*, vol. 199, pp. 194–201, 2013.

[92] S. Zeyrek, Ş. Altındal, H. Yüzer, and M. M. Bülbül, "Current transport mechanism in Al/Si_3N_4/p-Si (MIS) Schottky barrier diodes at low temperatures," *Appl. Surf. Sci.*, vol. 252, no. 8, pp. 2999–3010, 2006.

[93] I. Dökme, Ş. Altindal, and M. M. Bülbül, “The barrier height inhomogeneity in Al/p-Si Schottky barrier diodes with native insulator layer,” *Appl. Surf. Sci.*, vol. 252, no. 22, pp. 7749–7754, 2006.

[94] R.T.Tung, “Electron transport at metal-semiconductor ihterfaces: General theory,” *Phys. Rev. B*, vol. 45, no. 23, pp. 13509–13523, 1992.

[95] J. . Ranuárez, a Ortiz-Conde, and F. . García Sánchez, “A new method to extract diode parameters under the presence of parasitic series and shunt resistance,” *Microelectron. Reliab.*, vol. 40, no. 2, pp. 355–358, 2000.

[96] B. V. Mistry, P. Bhatt, K. H. Bhavsar, S. J. Trivedi, U. N. Trivedi, and U. S. Joshi, “Growth and properties of transparent p-NiO/n-ITO (In_2O_3:Sn) p-n junction thin film diode,” *Thin Solid Films*, vol. 519, no. 11, pp. 3840–3843, 2011.

[97] A. N. Banerjee and K. K. Chattopadhyay, “Electro-optical properties of all-oxide p-$CuAlO_2$/n-ZnO: Al transparent heterojunction thin film diode fabricated on glass substrate,” *Cent. Eur. J. Phys.*, vol. 6, no. 1, pp. 57–63, 2008.

[98] B. S. Kang, S. E. Ahn, M. J. Lee, G. Stefanovich, K. H. Kim, W. X. Xianyu, C. B. Lee, Y. Park, I. G. Back, and B. H. Park, “High-current-density CuO_x/$InZnO_x$ thin-film diodes for cross-point memory applications,” *Adv. Mater.*, vol. 20, no. 16, pp. 3066–3069, 2008.

[99] B. N. Pal, J. Sun, B. J. Jung, E. Choi, A. G. Andreou, and H. E. Katz, “Pentacene-zinc oxide vertical diode with compatible grains and 15-MHz rectification,” *Adv. Mater.*, vol. 20, no. 5, pp. 1023–1028, 2008.

[100] R. S. Ajimsha, K. A. Vanaja, M. K. Jayaraj, P. Misra, V. K. Dixit, and L. M. Kukreja, “Transparent p-$AgCoO_2$/n-ZnO diode heterojunction fabricated by pulsed laser deposition,” *Thin Solid Films*, vol. 515, no. 18, pp. 7352–7356, 2007.

[101] D. S. Kim, T. J. Park, D. H. Kim, and S. Y. Choi, “Fabrication of a transparent p-n heterojunction thin film diode composed of p-$CuAlO_2$/n-ZnO,” *Phys. Status Solidi Appl. Mater. Sci.*, vol. 203, no. 6, pp. 51–53, 2006.

[102] A. Sanchez-Juarez, A. Tiburcio-Silver, and A. Ortiz, “Fabrication of SnS_2/SnS heterojunction thin film diodes by plasma-enhanced chemical vapor deposition,” *Thin Solid Films*, vol. 480–481, pp. 452–456, 2005.

[103] S. Steudel, K. Myny, V. Arkhipov, C. Deibel, S. De Vusser, J. Genoe, and P. Heremans, “50 MHz rectifier based on an organic diode,” *Nat. Mater.*, vol. 4, no. 8, pp. 597–600, 2005.

[104] A. Kudo, H. Yanagi, K. Ueda, H. Hosono, H. Kawazoe, and Y. Yano, “Fabrication of transparent p-n heterojunction thin-film diodes based entirely on oxide semiconductors,” *Appl. Phys. Lett.*, vol. 75, no. 18, pp. 2851–2853, 1999.

[105] I. Buchmann, “How does a Supercapacitor Work ?,” *Battery University*. [Online]. Available: http://batteryuniversity.com/learn/article/whats_the_role_of_the_supercapacitor. [Accessed: 05-Aug-2015].

Appendix

Appendix 1 – Datasheets for DC-DC converter ICs

LINEAR TECHNOLOGY

LTC3129

15V, 200mA Synchronous Buck-Boost DC/DC Converter with 1.3µA Quiescent Current

FEATURES

- **Regulates V_{OUT} Above, Below or Equal to V_{IN}**
- **Wide V_{IN} Range: 2.42V to 15V, 1.92V to 15V After Start-Up (Bootstrapped)**
- **Wide V_{OUT} Range: 1.4V to 15.75V**
- **200mA Output Current in Buck Mode**
- **Single Inductor**
- **1.3µA Quiescent Current**
- Programmable Maximum Power Point Control
- 1.2MHz Ultralow Noise PWM
- Current Mode Control
- Pin Selectable Burst Mode® Operation
- Up to 95% Efficiency
- Accurate RUN Pin Threshold
- Power Good Indicator
- 10nA Shutdown Current
- Thermally Enhanced 3mm × 3mm QFN and 16-Lead MSOP Packages

APPLICATIONS

- Industrial Wireless Sensor Nodes
- Post-Regulator for Harvested Energy
- Solar Panel Post-Regulator/Charger
- Intrinsically Safe Power Supplies
- Wireless Microphones
- Avionics-Grade Wireless Headsets

DESCRIPTION

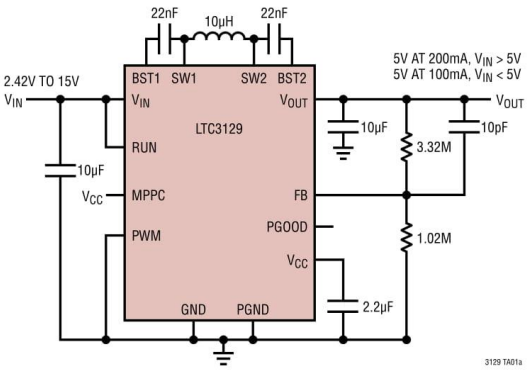
The LTC®3129 is a high efficiency, 200mA buck-boost DC/DC converter with a wide V_{IN} and V_{OUT} range. It includes an accurate RUN pin threshold to allow predictable regulator turn-on and a maximum power point control (MPPC) capability that ensures maximum power extraction from non-ideal power sources such as photovoltaic panels.

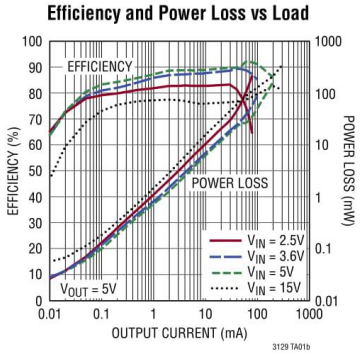
The LTC3129 employs an ultralow noise, 1.2MHz PWM switching architecture that minimizes solution footprint by allowing the use of tiny, low profile inductors and ceramic capacitors. Built-in loop compensation and soft-start simplify the design. For high efficiency operation at light loads, automatic Burst Mode operation can be selected, reducing the quiescent current to just 1.3µA.

Additional features include a power good output, less than 10nA of shutdown current and thermal shutdown.

The LTC3129 is available in thermally enhanced 3mm × 3mm QFN and 16-lead MSOP packages. For fixed output voltage options, see the functionally equivalent LTC3129-1, which eliminates the need for an external feedback divider.

TYPICAL APPLICATION



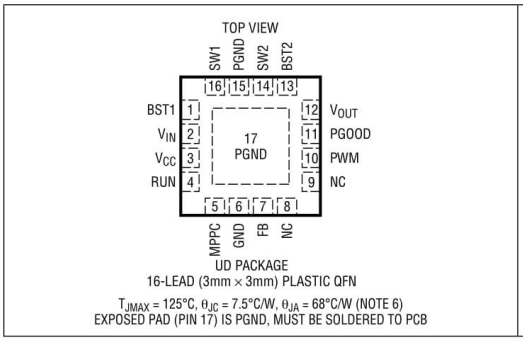


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 8)

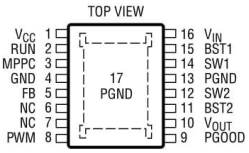
V_{IN}, V_{OUT} Voltages ..... –0.3V to 18V
SW1 DC Voltage..... –0.3V to (V_{IN} + 0.3V)
SW2 DC Voltage.....–0.3V to (V_{OUT} + 0.3V)
SW1, SW2 Pulsed (<100ns) Voltage .....–1V to 19V
BST1 Voltage .....(SW1 – 0.3V) to (SW1 + 6V)
BST2 Voltage .....(SW2 – 0.3V) to (SW2 + 6V)
RUN, PGOOD Voltages..... –0.3V to 18V
V_{CC}, FB, PWM, MPPC Voltages.....–0.3V to 6V
PGOOD Sink Current 15mA
Operating Junction Temperature Range
(Notes 2, 5).....–40°C to 125°C
Storage Temperature Range .....–65°C to 150°C
MSE Lead Temperature (Soldering, 10 sec) .....300°C

PIN CONFIGURATION



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JC} = 7.5°C/W, θ_{JA} = 68°C/W (NOTE 6)
EXPOSED PAD (PIN 17) IS PGND, MUST BE SOLDERED TO PCB



MSE PACKAGE
16-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JC} = 10°C/W, θ_{JA} = 40°C/W (NOTE 6)
EXPOSED PAD (PIN 17) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3129EUD#PBF	LTC3129EUD#TRPBF	LGDR	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LTC3129IUD#PBF	LTC3129IUD#TRPBF	LGDR	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LTC3129EMSE#PBF	LTC3129EMSE#TRPBF	3129	16-Lead Plastic MSOP	–40°C to 125°C
LTC3129IMSE#PBF	LTC3129IMSE#TRPBF	3129	16-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). Unless otherwise noted, V_{IN} = 12V, V_{OUT} = 5V.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Start-Up Voltage		●		2.25	2.42	V
Input Voltage Range	V_{CC} > 2.42V (Back-Driven)	●	1.92		15	V
V_{IN} UVLO Threshold (Rising)	V_{CC} > 2.42V (Back-Driven)	●	1.8	1.9	2.0	V
V_{IN} UVLO Hysteresis		●	80	100	130	mV
Output Voltage Adjust Range		●	1.4		15.75	V
Feedback Voltage		●	1.151	1.175	1.199	V
Feedback Input Current	FB = 1.25V			0.1	10	nA
Quiescent Current (V_{IN}) – Shutdown	RUN = 0V, Including Switch Leakage			10	100	nA
Quiescent Current (V_{IN}) UVLO	Either V_{IN} or V_{CC} Below Their UVLO Threshold, or RUN Below the Threshold to Enable Switching			1.9	3	µA
Quiescent Current – Burst Mode Operation	Measured on V_{IN}, FB > 1.25V PWM = 0V, RUN = V_{IN}			1.3	2.0	µA
N-Channel Switch Leakage on V_{IN} and V_{OUT}	SW1 = 0V, V_{IN} = 15V SW2 = 0V, V_{OUT} = 15V RUN = 0V			10	50	nA
N-Channel Switch On-Resistance	V_{CC} = 4V			0.75		Ω
Inductor Average Current Limit	V_{OUT} > UV Threshold (Note 4) V_{OUT} < UV Threshold (Note 4)	● ●	220 80	275 130	350 200	mA mA
Inductor Peak Current Limit	(Note 4)	●	400	500	680	mA
Maximum Boost Duty Cycle	FB = 1.10V. Percentage of Period SW2 is Low in Boost Mode (Note 7)	●	85	89	95	%
Minimum Duty Cycle	FB = 1.25V. Percentage of Period SW1 is High in Buck Mode (Note 7)	●			0	%
Switching Frequency	PWM = V_{CC}	●	1.0	1.2	1.4	MHz
SW1 and SW2 Minimum Low Time	(Note 3)			90		ns
MPPC Voltage		●	1.12	1.175	1.22	V
MPPC Input Current	MPPC = 5V			1	10	nA
RUN Threshold to Enable V_{CC}		●	0.5	0.9	1.15	V
RUN Threshold to Enable Switching (Rising)	V_{CC} > 2.4V	●	1.16	1.22	1.28	V
RUN (Switching) Threshold Hysteresis			50	80	120	mV
RUN Input Current	RUN = 15V			1	10	nA
PWM Input High		●	1.6			V
PWM Input Low		●			0.5	V
PWM Input Current	PWM = 5V			0.1	1	µA
Soft-Start Time				3		ms
V_{CC} Voltage	V_{IN} > 4.85V	●	3.4	4.1	4.7	V
V_{CC} Dropout Voltage (V_{IN} – V_{CC})	V_{IN} = 3.0V, Switching V_{IN} = 2.0V (V_{CC} in UVLO)			35 0	60 2	mV mV
V_{CC} UVLO Threshold (Rising)		●	2.1	2.25	2.42	V
V_{CC} UVLO Hysteresis				60		mV
V_{CC} Current Limit	V_{CC} = 0V	●	4	20	60	mA
V_{CC} Back-Drive Voltage (Maximum)		●			5.5	V
V_{CC} Input Current (Back-Driven)	V_{CC} = 5.5V (Switching)			2	4	mA
V_{CC} Leakage to V_{IN} if V_{CC} > V_{IN}	V_{CC} = 5.5V, V_{IN} = 1.8V, Measured on V_{IN}			–27		µA
V_{OUT} UV Threshold (Rising)		●	0.95	1.15	1.35	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). Unless otherwise noted, V_{IN} = 12V, V_{OUT} = 5V.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT} UV Hysteresis				150		mV
V_{OUT} Current – Shutdown	RUN = 0V, V_{OUT} = 15V Including Switch Leakage			10	100	nA
V_{OUT} Current – Sleep	PWM = 0V, FB = 1.25V			10		nA
V_{OUT} Current – Active	PWM = V_{CC}, V_{OUT} = 15V (Note 4), FB = 1.25V			5	9	µA
PGOOD Threshold, Falling	Referenced to Programmed V_{OUT} Voltage		–5.5	–7.5	–10	%
PGOOD Hysteresis	Referenced to Programmed V_{OUT} Voltage			2.5		%
PGOOD Voltage Low	I_{SINK} = 1mA			250	300	mV
PGOOD Leakage	PGOOD = 15V			1	50	nA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3129 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3129E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3129I is guaranteed over the full –40°C to 125°C operating junction temperature range. The junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) according to the formula: $T_J = T_A + (P_D \bullet \theta_{JA}°C/W)$, where θ_{JA} is the package thermal impedance. Note that the maximum ambient temperature consistent with these specifications, is determined by specific operating conditions in conjunction with board layout, the rated thermal package thermal resistance and other environmental factors.

Note 3: Specification is guaranteed by design and not 100% tested in production.

Note 4: Current measurements are made when the output is not switching.

Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

Note 6: Failure to solder the exposed backside of the package to the PC board ground plane will result in a much higher thermal resistance.

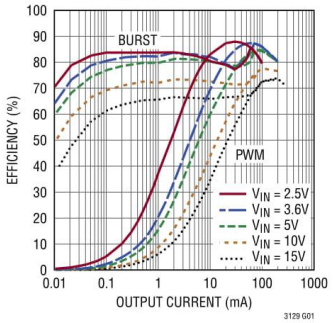
Note 7: Switch timing measurements are made in an open-loop test configuration. Timing in the application may vary somewhat from these values due to differences in the switch pin voltage during non-overlap durations when switch pin voltage is influenced by the magnitude and duration of the inductor current.

Note 8: Voltage transients on the switch pin(s) beyond the DC limits specified in the Absolute Maximum Ratings are non-disruptive to normal operation when using good layout practices as described elsewhere in the data sheet and application notes and as seen on the product demo board.

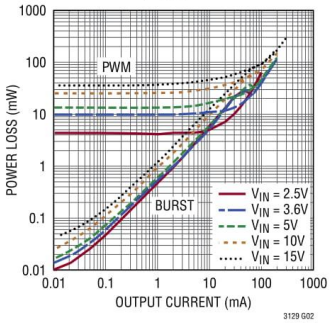
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

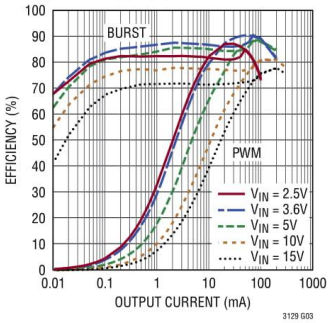
Efficiency, V_{OUT} = 2.5V



Power Loss, V_{OUT} = 2.5V

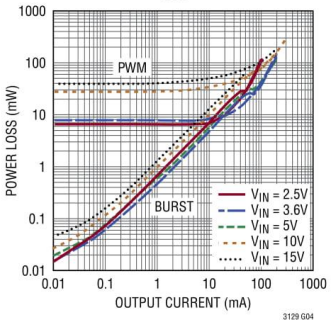


Efficiency, V_{OUT} = 3.3V

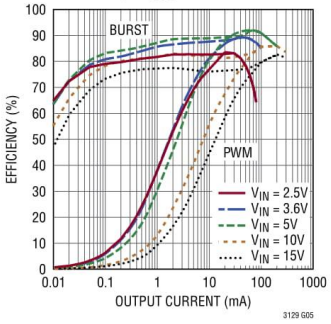


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

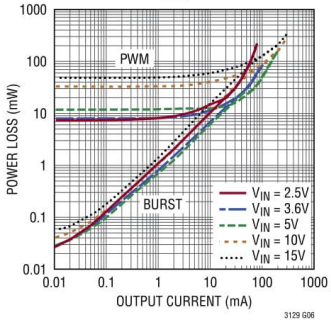
Power Loss, V_{OUT} = 3.3V



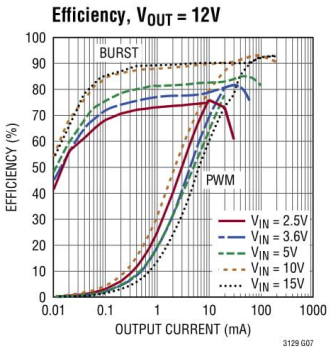
Efficiency, V_{OUT} = 5V



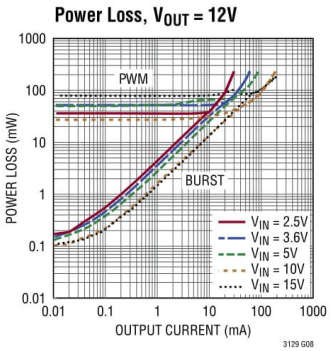
Power Loss, V_{OUT} = 5V



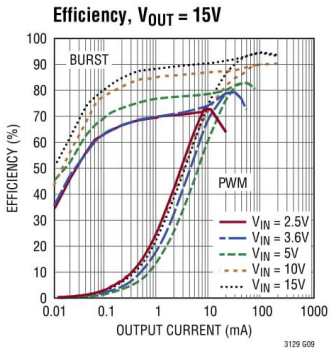
Efficiency, V_{OUT} = 12V



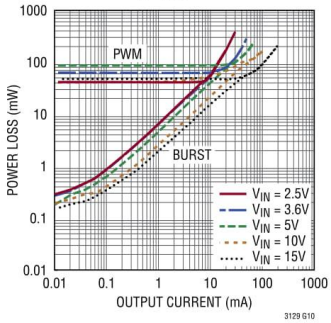
Power Loss, V_{OUT} = 12V



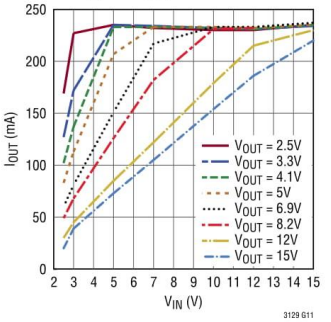
Efficiency, V_{OUT} = 15V



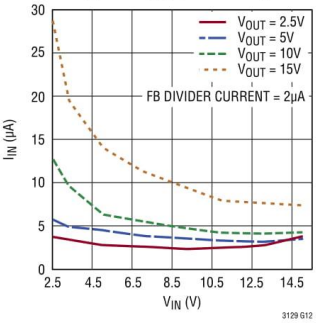
Power Loss, V_{OUT} = 15V



Maximum Output Current vs V_{IN} and V_{OUT}

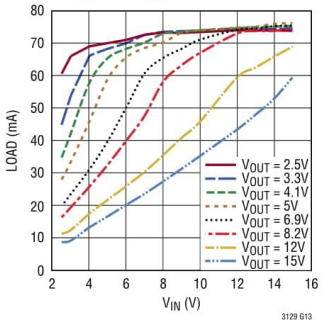


No Load Input Current vs V_{IN} and V_{OUT} (PWM = 0V)

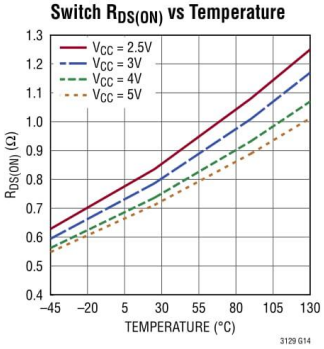


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

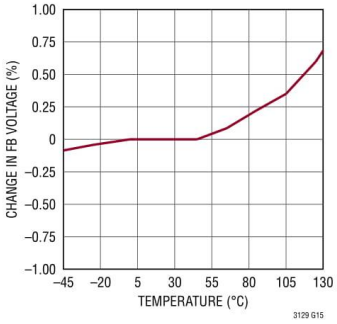
Burst Mode Threshold vs V_{IN} and V_{OUT}



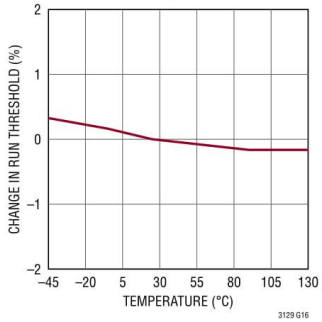
Switch $R_{DS(ON)}$ vs Temperature



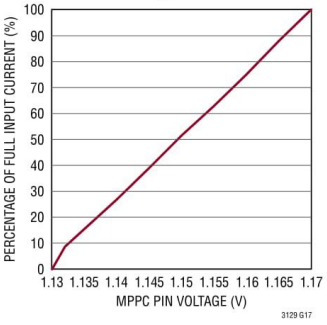
FB Voltage vs Temperature (Normalized to 25°C)



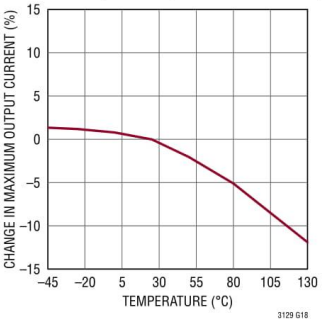
Accurate RUN Threshold vs Temperature (Normalized to 25°C)



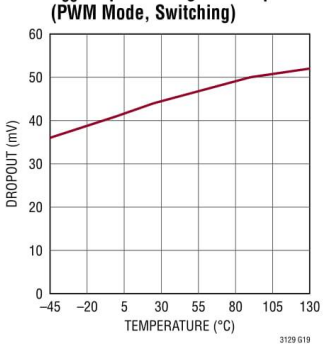
Average Input Current Limit vs MPPC Voltage



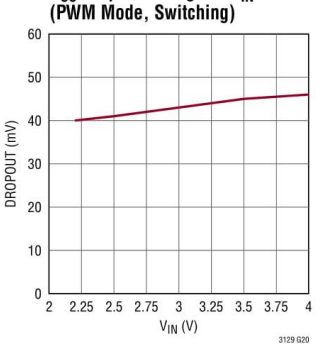
Maximum Output Current vs Temperature (Normalized to 25°C)



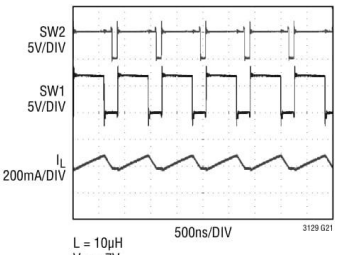
V_{CC} Dropout Voltage vs Temperature (PWM Mode, Switching)



V_{CC} Dropout Voltage vs V_{IN} (PWM Mode, Switching)



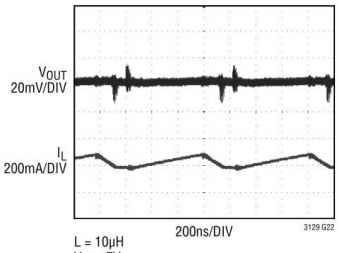
Fixed Frequency PWM Waveforms



L = 10µH
V_{IN} = 7V
V_{OUT} = 5V
I_{OUT} = 200mA

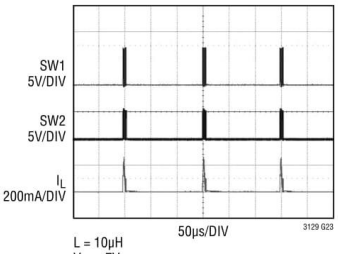
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Fixed Frequency Ripple on V_{OUT}



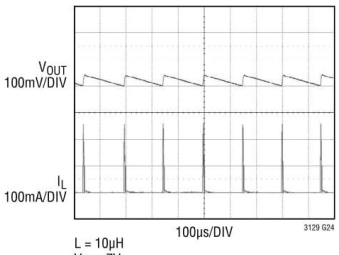
$L = 10\mu H$
$V_{IN} = 7V$
$V_{OUT} = 5V$
$I_{OUT} = 200mA$
$C_{OUT} = 10\mu F$

Burst Mode Waveforms



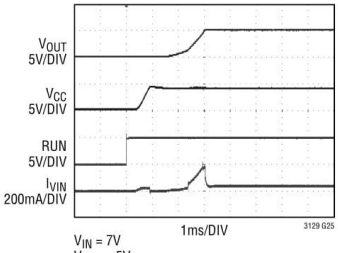
$L = 10\mu H$
$V_{IN} = 7V$
$V_{OUT} = 5V$
$I_{OUT} = 5mA$
$C_{OUT} = 22\mu F$

Burst Mode Ripple on V_{OUT}



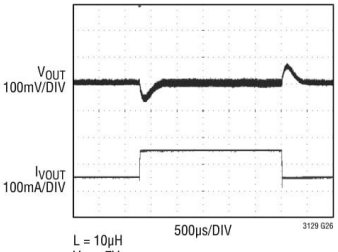
$L = 10\mu H$
$V_{IN} = 7V$
$V_{OUT} = 5V$
$I_{OUT} = 5mA$
$C_{OUT} = 22\mu F$ (WITH THE RECOMMENDED FEEDFORWARD CAPACITOR)

Start-Up Waveforms



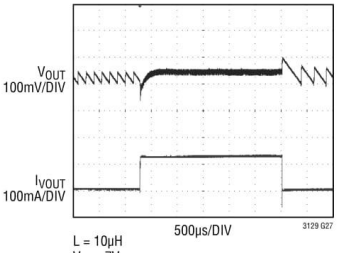
$V_{IN} = 7V$
$V_{OUT} = 5V$
$I_{OUT} = 50mA$
$C_{OUT} = 22\mu F$

Step Load Transient Response in Fixed Frequency



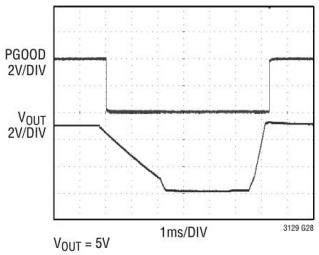
$L = 10\mu H$
$V_{IN} = 7V$
$V_{OUT} = 5V$
$C_{OUT} = 10\mu F$
$I_{OUT} = 50mA$ to $150mA$ STEP

Step Load Transient Response in Burst Mode Operation



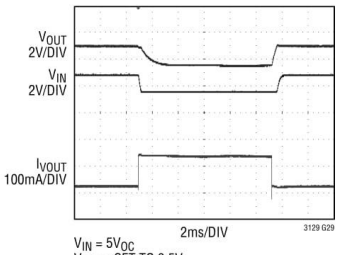
$L = 10\mu H$
$V_{IN} = 7V$
$V_{OUT} = 5V$
$C_{OUT} = 22\mu F$ (WITH THE RECOMMENDED FEEDFORWARD CAPACITOR)
$I_{OUT} = 5mA$ to $125mA$ STEP

PGOOD Response to a Drop On V_{OUT}



$V_{OUT} = 5V$

MPPC Response to a Step Load



$V_{IN} = 5V_{DC}$
V_{MPPC} SET TO 3.5V
$C_{IN} = 22\mu F$, $R_{IN} = 10\Omega$,
$V_{OUT} = 5V$, $C_{OUT} = 22\mu F$
$I_{OUT} = 25mA$ to $125mA$ STEP

PIN FUNCTIONS (QFN/MSOP)

BST1 (Pin 1/Pin 15): Bootstrapped Floating Supply for High Side NMOS Gate Drive. Connect to SW1 through a 22nF capacitor, as close to the part as possible. The value is not critical. Any value from 4.7nF to 47nF may be used.

V_{IN} (Pin 2/Pin 16): Input Voltage for the Converter. Connect a minimum of 4.7µF ceramic decoupling capacitor from this pin to the ground plane, as close to the pin as possible.

V_{CC} (Pin 3/Pin 1): Output voltage of the internal voltage regulator. This is the supply pin for the internal circuitry. Bypass this output with a minimum of 2.2µF ceramic capacitor close to the pin. This pin may be back-driven by an external supply, up to a maximum of 5.5V.

RUN (Pin 4/Pin 2): Input to the Run Comparator. Pull this pin above 1.1V to enable the V_{CC} regulator and above 1.28V to enable the converter. Connecting this pin to a resistor divider from V_{IN} to ground allows programming a V_{IN} start threshold higher than the 1.8V (typical) V_{IN} UVLO threshold. In this case, the typical V_{IN} turn-on threshold is determined by $V_{IN} = 1.22V \bullet [1+(R3/R4)]$ (see Figure 2).

MPPC (Pin 5/Pin 3): Maximum Power Point Control Programming Pin. Connect this pin to a resistor divider from V_{IN} to ground to enable the MPPC functionality. If the V_{OUT} load is greater than what the power source can provide, the MPPC will reduce the inductor current to regulate V_{IN} to a voltage determined by: $V_{IN} = 1.175V \bullet [1+(R5/R6)]$ (see Figure 3). By setting the V_{IN} regulation voltage appropriately, maximum power transfer from the limited source is assured. Note this pin is very noise sensitive, therefore minimize trace length and stray capacitance. Please refer to the Applications Information section for more detail on programming the MPPC for different sources. If this function is not needed, tie the pin to V_{CC}.

GND (Pin 6/Pin 4): Signal Ground. Provide a short direct PCB path between GND and the ground plane where the exposed pad is soldered.

FB (Pin 7/Pin 5): Feedback Input to the Error Amplifier. Connect to a resistor divider from V_{OUT} to ground. The output voltage can be adjusted from 1.4V to 15.75V by: $V_{OUT} = 1.175V \bullet [1+(R1/R2)]$. Note this pin is very noise sensitive, therefore minimize trace length and stray capacitance.

NC (Pins 8, 9/Pins 6, 7): Unused. These pins should be grounded.

PWM (Pin 10/Pin 8): Mode Select Pin.

PWM = Low (ground): Enables automatic Burst Mode operation.

PWM = High (tie to V_{CC}): Fixed frequency PMW operation.

This pin should not be allowed to float. It has an internal 5M pull-down resistor.

PGOOD (Pin 11/Pin 9): Open drain output that pulls to ground when FB drops too far below its regulated voltage. Connect a pull-up resistor from this pin to a positive supply. This pin can sink up to the absolute maximum rating of 15mA when low. Refer to the Operation section of the data sheet for more detail.

V_{OUT} (Pin 12/Pin 10): Output voltage of the converter. Connect a minimum value of 4.7µF ceramic capacitor from this pin to the ground plane, as close to the pin as possible.

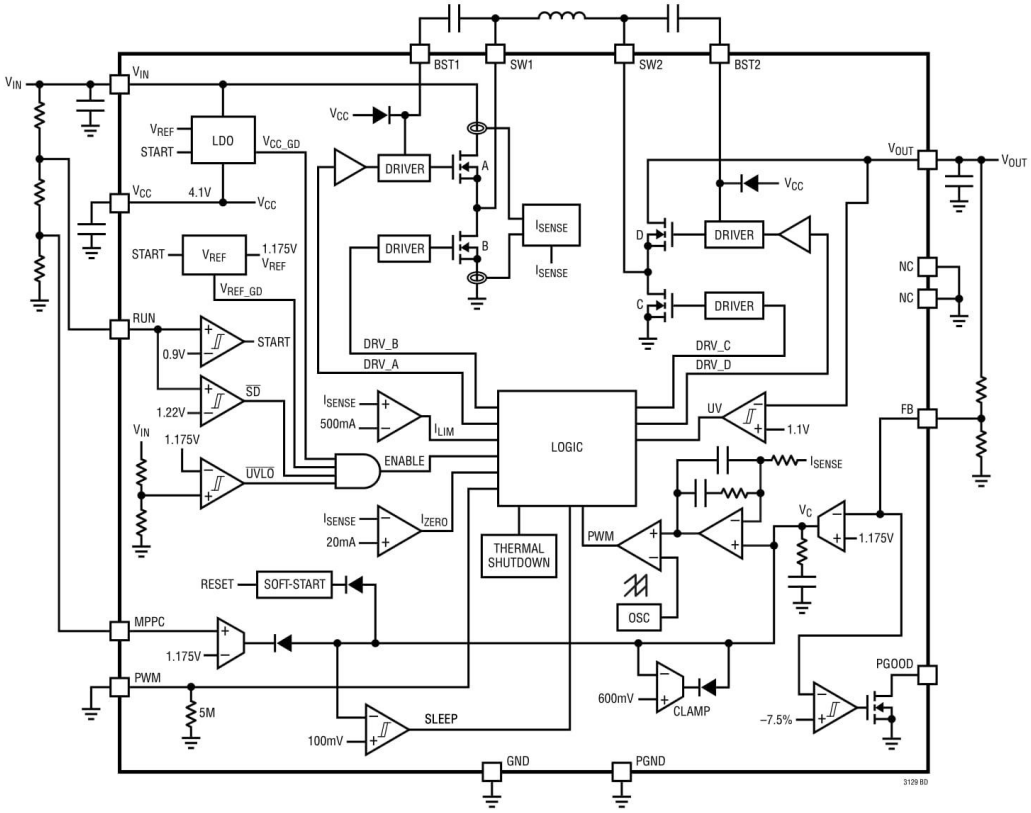
BST2 (Pin 13/Pin 11): Bootstrapped floating supply for high side NMOS gate drive. Connect to SW2 through a 22nF capacitor, as close to the part as possible. The value is not critical. Any value from 4.7nF to 47nF may be used.

SW2 (Pin 14/Pin 12): Switch Pin. Connect to one side of the inductor. Keep PCB trace lengths as short and wide as possible to reduce EMI.

PGND (Pin 15, Exposed Pad Pin 17/Pin 13, Exposed Pad Pin 17): Power Ground. Provide a short direct PCB path between PGND and the ground plane. **The exposed pad must also be soldered to the PCB ground plane**. It serves as a power ground connection, and as a means of conducting heat away from the die.

SW1 (Pin 16/Pin 14): Switch Pin. Connect to one side of the inductor. Keep PCB trace lengths as short and wide as possible to reduce EMI.

BLOCK DIAGRAM



OPERATION

INTRODUCTION

The LTC3129 is a 1.3µA quiescent current, monolithic, current mode, buck-boost DC/DC converter that can operate over a wide input voltage range of 1.92V to 15V and provide up to 200mA to the load. Internal, low $R_{DS(ON)}$ N-channel power switches reduce solution complexity and maximize efficiency. A proprietary switch control algorithm allows the buck-boost converter to maintain output voltage regulation with input voltages that are above, below or equal to the output voltage. Transitions between the step-up or step-down operating modes are seamless and free of transients and sub-harmonic switching, making this product ideal for noise sensitive applications. The LTC3129 operates at a fixed nominal switching frequency of 1.2MHz, which provides an ideal trade-off between small solution size and high efficiency. Current mode control provides inherent input line voltage rejection, simplified compensation and rapid response to load transients.

Burst Mode capability is also included in the LTC3129 and is user-selected via the PWM input pin. In Burst Mode operation, the LTC3129 provides exceptional efficiency at light output loading conditions by operating the converter only when necessary to maintain voltage regulation. The Burst Mode quiescent current is a miserly 1.3µA. At higher loads, the LTC3129 automatically switches to fixed frequency PWM mode when Burst Mode operation is selected. (Please refer to the Typical Performance Characteristics curves for the mode transition point at different input and output voltages.) If the application requires extremely low noise, continuous PWM operation can also be selected via the PWM pin.

A MPPC (maximum power point control) function is also provided that allows the input voltage to the converter to be servo'd to a programmable point for maximum power when operating from various non-ideal power sources such as photovoltaic cells. The LTC3129 also features an accurate RUN comparator threshold with hysteresis, allowing the buck-boost DC/DC converter to turn on and off at user-selected V_{IN} voltage thresholds. With a wide voltage range, 1.3µA Burst Mode current and programmable RUN and MPPC pins, the LTC3129 is well suited for many diverse applications.

PWM MODE OPERATION

If the PWM pin is high or if the load current on the converter is high enough to command PWM mode operation with PWM low, the LTC3129 operates in a fixed 1.2MHz PWM mode using an internally compensated average current mode control loop. PWM mode minimizes output voltage ripple and yields a low noise switching frequency spectrum. A proprietary switching algorithm provides seamless transitions between operating modes and eliminates discontinuities in the average inductor current, inductor ripple current and loop transfer function throughout all modes of operation. These advantages result in increased efficiency, improved loop stability and lower output voltage ripple in comparison to the traditional buck-boost converter.

Figure 1 shows the topology of the LTC3129 power stage which is comprised of four N-channel DMOS switches and their associated gate drivers. In PWM mode operation both switch pins transition on every cycle independent of the input and output voltages. In response to the internal control loop command, an internal pulse width modulator generates the appropriate switch duty cycle to maintain regulation of the output voltage.

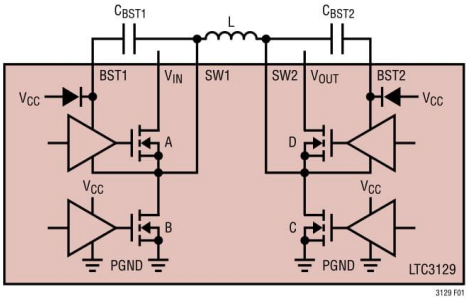


Figure 1. Power Stage Schematic

OPERATION

When stepping down from a high input voltage to a lower output voltage, the converter operates in buck mode and switch D remains on for the entire switching cycle except for the minimum switch low duration (typically 90ns). During the switch low duration, switch C is turned on which forces SW2 low and charges the flying capacitor, C_{BST2}. This ensures that the switch D gate driver power supply rail on BST2 is maintained. The duty cycle of switches A and B are adjusted to maintain output voltage regulation in buck mode.

If the input voltage is lower than the output voltage, the converter operates in boost mode. Switch A remains on for the entire switching cycle except for the minimum switch low duration (typically 90ns). During the switch low duration, switch B is turned on which forces SW1 low and charges the flying capacitor, C_{BST1}. This ensures that the switch A gate driver power supply rail on BST1 is maintained. The duty cycle of switches C and D are adjusted to maintain output voltage regulation in boost mode.

Oscillator

The LTC3129 operates from an internal oscillator with a nominal fixed frequency of 1.2MHz. This allows the DC/DC converter efficiency to be maximized while still using small external components.

Current Mode Control

The LTC3129 utilizes average current mode control for the pulse width modulator. Current mode control, both average and the better known peak method, enjoy some benefits compared to other control methods including: simplified loop compensation, rapid response to load transients and inherent line voltage rejection.

Referring to the Block Diagram, a high gain, internally compensated transconductance amplifier monitors Vout through a voltage divider connected to the FB pin. The error amplifier output is used by the current mode control loop to command the appropriate inductor current level. The inverting input of the internally compensated average current amplifier is connected to the inductor current sense circuit. The average current amplifier's output is compared to the oscillator ramps, and the comparator outputs are used to control the duty cycle of the switch pins on a cycle-by-cycle basis.

The voltage error amplifier monitors the output voltage, V_{OUT} through a voltage divider and makes adjustments to the current command as necessary to maintain regulation. The voltage error amplifier therefore controls the outer voltage regulation loop. The average current amplifier makes adjustments to the inductor current as directed by the voltage error amplifier output via V_C and is commonly referred to as the inner current loop amplifier.

The average current mode control technique is similar to peak current mode control except that the average current amplifier, by virtue of its configuration as an integrator, controls average current instead of the peak current. This difference eliminates the peak to average current error inherent to peak current mode control, while maintaining most of the advantages inherent to peak current mode control.

Average current mode control requires appropriate compensation for the inner current loop, unlike peak current mode control. The compensation network must have high DC gain to minimize errors between the actual and commanded average current level, high bandwidth to quickly change the commanded current level following transient load steps and a controlled mid-band gain to provide a form of slope compensation unique to average current mode control. The compensation components required to ensure proper operation have been carefully selected and are integrated within the LTC3129.

Inductor Current Sense and Maximum Output Current

As part of the current control loop required for current mode control, the LTC3129 includes a pair of current sensing circuits that measure the buck-boost converter inductor current.

The voltage error amplifier output, V_C, is internally clamped to a nominal level of 0.6V. Since the average inductor current is proportional to V_C, the 0.6V clamp level sets the maximum average inductor current that can be programmed by the inner current loop. Taking into account the current sense amplifier's gain, the maximum average

OPERATION

inductor current is approximately 275mA (typical). In Buck mode, the output current is approximately equal to the inductor current I_L.

$$I_{OUT(BUCK)} \approx I_L \bullet 0.89$$

The 90ns SW1/SW2 forced low time on each switching cycle briefly disconnects the inductor from V_{OUT} and V_{IN} resulting in about 11% less output current in either buck or boost mode for a given inductor current. In boost mode, the output current is related to average inductor current and duty cycle by:

$$I_{OUT(BOOST)} \approx I_L \bullet (1 - D) \bullet \text{Efficiency},$$

where D is the converter duty cycle.

Since the output current in boost mode is reduced by the duty cycle (D), the output current rating in buck mode is always greater than in boost mode. Also, because boost mode operation requires a higher inductor current for a given output current compared to buck mode, the efficiency in boost mode will be lower due to higher $I_L^2 \bullet R_{DS(ON)}$ losses in the power switches. This will further reduce the output current capability in boost mode. In either operating mode, however, the inductor peak-to-peak ripple current does not play a major role in determining the output current capability, unlike peak current mode control.

With peak current mode control, the maximum output current capability is reduced by the magnitude of inductor ripple current because the peak inductor current level is the control variable, but the average inductor current is what determines the output current. The LTC3129 measures and controls average inductor current, and therefore, the inductor ripple current magnitude has little effect on the maximum current capability in contrast to an equivalent peak current mode converter. Under most conditions in buck mode, the LTC3129 is capable of providing a minimum of 200mA to the load. In boost mode, as described previously, the output current capability is related to the boost ratio or duty cycle (D). For example, for a 3.6V V_{IN} to 5V output application, the LTC3129 can provide up to 150mA to the load. Refer to the Typical Performance characteristics section for more detail on output current capability.

Overload Current Limit and I_{ZERO} Comparator

The internal current sense waveform is also used by the peak overload current (I_{PEAK}) and zero current (I_{ZERO}) comparators. The I_{PEAK} current comparator monitors Isense and turns off switch A if the inductor current level exceeds its maximum internal threshold, which is approximately 500mA. An inductor current level of this magnitude will occur during a fault, such as an output short-circuit, or during large load or input voltage transients.

The LTC3129 features near discontinuous inductor current operation at light output loads by virtue of the I_{ZERO} comparator circuit. By limiting the reverse current magnitude in PWM mode, a balance between low noise operation and improved efficiency at light loads is achieved. The I_{ZERO} comparator threshold is set near the zero current level in PWM mode, and as a result, the reverse current magnitude will be a function of inductance value and output voltage due to the comparator's propagation delay. In general, higher output voltages and lower inductor values will result in increased reverse current magnitude.

In automatic Burst Mode operation (PWM pin low), the I_{ZERO} comparator threshold is increased so that reverse inductor current does not normally occur. This maximizes efficiency at very light loads.

Burst Mode OPERATION

When the PWM pin is held low, the LTC3129 is configured for automatic Burst Mode operation. As a result, the buck-boost DC/DC converter will operate with normal continuous PWM switching above a predetermined minimum output load and will automatically transition to power saving Burst Mode operation below this output load level. Note that if the PWM pin is low, reverse inductor current is not allowed at any load. Refer to the Typical Performance Characteristics section to determine the Burst Mode transition threshold for various combinations of V_{IN} and V_{OUT}. If PWM is low, at light output loads, the LTC3129 will go into a standby or sleep state when the output voltage achieves its nominal regulation level. The sleep state halts PWM switching and powers down all non-essential

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functions of the IC, significantly reducing the quiescent current of the LTC3129 to just 1.3µA typical. This greatly improves overall power conversion efficiency when the output load is light. Since the converter is not operating in sleep, the output voltage will slowly decay at a rate determined by the output load resistance and the output capacitor value. When the output voltage has decayed by a small amount, typically 1%, the LTC3129 will wake and resume normal PWM switching operation until the voltage on V_{OUT} is restored to the previous level. If the load is very light, the LTC3129 may only need to switch for a few cycles to restore V_{OUT} and may sleep for extended periods of time, significantly improving efficiency. If the load is suddenly increased above the burst transition threshold, the part will automatically resume continuous PWM operation until the load is once again reduced.

A feedforward capacitor on the feedback divider can be used to reduce Burst Mode V_{OUT} ripple. This is discussed in more detail in the Applications Information section of this data sheet.

Note that Burst Mode operation is inhibited until soft-start is done, the MPPC pin is greater than 1.175V and V_{OUT} has reached regulation.

Soft-Start

The LTC3129 soft-start circuit minimizes input current transients and output voltage overshoot on initial power up. The required timing components for soft-start are internal to the LTC3129 and produce a nominal soft-start duration of approximately 3ms. The internal soft-start circuit slowly ramps the error amplifier output, V_C. In doing so, the current command of the IC is also slowly increased, starting from zero. It is unaffected by output loading or output capacitor value. Soft-start is reset by the UVLO on both V_{IN} and V_{CC}, the RUN pin and thermal shutdown.

V_{CC} Regulator

An internal low dropout regulator (LDO) generates a nominal 4.1V V_{CC} rail from V_{IN}. The V_{CC} rail powers the internal control circuitry and the gate drivers of the LTC3129. The V_{CC} regulator is disabled in shutdown to reduce quiescent current and is enabled by raising the RUN pin above its logic threshold. The V_{CC} regulator includes current-limit protection to safeguard against accidental short-circuiting of the V_{CC} rail.

Undervoltage Lockout (UVLO)

There are two undervoltage lockout (UVLO) circuits within the LTC3129 that inhibit switching; one that monitors V_{IN} and another that monitors V_{CC}. Either UVLO will disable operation of the internal power switches and keep other IC functions in a reset state if either V_{IN} or V_{CC} are below their respective UVLO thresholds.

The V_{IN} UVLO comparator has a falling voltage threshold of 1.8V (typical). If V_{IN} falls below this level, IC operation is disabled until V_{IN} rises above 1.9V (typical), as long as the V_{CC} voltage is above its UVLO threshold.

The V_{CC} UVLO has a falling voltage threshold of 2.19V (typical). If the V_{CC} voltage falls below this threshold, IC operation is disabled until V_{CC} rises above 2.25V (typical) as long as V_{IN} is above its nominal UVLO threshold level.

Depending on the particular application, either of these UVLO thresholds could be the limiting factor affecting the minimum input voltage required for operation. Because the V_{CC} regulator uses V_{IN} for its power input, the minimum input voltage required for operation is determined by the V_{CC} minimum voltage, as input voltage (V_{IN}) will always be higher than V_{CC} in the normal (non-bootstrapped) configuration. Therefore, the minimum V_{IN} for the part to startup is 2.25V (typical).

In applications where V_{CC} is bootstrapped (powered through a Schottky diode by either V_{OUT} or an auxiliary power rail), the minimum input voltage for operation will be limited only by the V_{IN} UVLO threshold (1.8V typical). *Please note that if the bootstrap voltage is derived from the LTC3129 V_{OUT} and not an independent power rail, then the minimum input voltage required for initial startup is still 2.25V (typical).*

Note that if either V_{IN} or V_{CC} are below their UVLO thresholds, or if RUN is below its accurate threshold of 1.22V (typical), then the LTC3129 will remain in a soft shutdown state, where the V_{IN} quiescent current will be only 1.9µA typical.

OPERATION

V_{OUT} Undervoltage

There is also an undervoltage comparator that monitors the output voltage. Until V_{OUT} reaches 1.15V (typical), the average current limit is reduced by a factor of two. This reduces power dissipation in the device in the event of a shorted output. In addition, N-channel switch D, which feeds V_{OUT}, will be disabled until V_{OUT} exceeds 1.15V.

RUN Pin Comparator

In addition to serving as a logic level input to enable certain functions of the IC, the RUN pin includes an accurate internal comparator that allows it to be used to set custom rising and falling ON/OFF thresholds with the addition of an optional external resistor divider. When RUN is driven above its logic threshold (0.9V typical), the V_{CC} regulator is enabled, which provides power to the internal control circuitry of the IC. If the voltage on RUN is increased further so that it exceeds the RUN comparator's accurate analog threshold (1.22V typical), all functions of the buck-boost converter will be enabled and a start-up sequence will ensue, assuming the V_{IN} and V_{CC} UVLO thresholds are satisfied.

If RUN is brought below the accurate comparator threshold, the buck-boost converter will inhibit switching, but the V_{CC} regulator and control circuitry will remain powered unless RUN is brought below its logic threshold. Therefore, in order to completely shut down the IC and reduce the Vin current to 10nA (typical), it is necessary to ensure that RUN is brought below its worst case low logic threshold of 0.5V. RUN is a high voltage input and can be tied directly to V_{IN} to continuously enable the IC when the input supply is present. Also note that RUN can be driven above V_{IN} or V_{OUT} as long as it stays within the operating range of the IC (up to 15V).

With the addition of an optional resistor divider as shown in Figure 2, the RUN pin can be used to establish a user-programmable turn-on and turn-off threshold. This feature can be utilized to minimize battery drain below a certain input voltage, or to operate the converter in a hiccup mode from very low current sources.

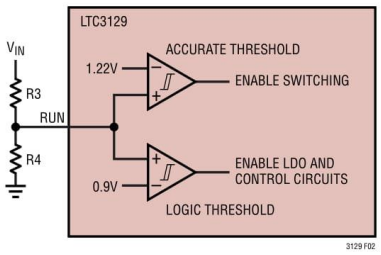

Figure 2. Accurate RUN Pin Comparator

Note that once RUN is above 0.9V typical, the quiescent input current on V_{IN} (or V_{CC} if back-driven) will increase to about 1.9µA typical until the V_{IN} and V_{CC} UVLO thresholds are satisfied.

The converter is enabled when the voltage on RUN exceeds 1.22V (nominal). Therefore, the turn-on voltage threshold on V_{IN} is given by:

$$V_{IN(TURN\text{-}ON)} = 1.22V \bullet (1 + R3/R4)$$

The RUN comparator includes a built-in hysteresis of approximately 80mV, so that the turn off threshold will be 1.14V.

There may be cases due to PCB layout, very large value resistors for R3 and R4, or proximity to noisy components where noise pickup may cause the turn-on or turn-off of the IC to be intermittent. In these cases, a small filter capacitor can be added across R4 to ensure proper operation.

OPERATION

PGOOD Comparator

The LTC3129 provides an open-drain PGOOD output that pulls low if V_{OUT} falls more than 7.5% (typical) below its programmed value. When V_{OUT} rises to within 5% (typical) of its programmed value, the internal PGOOD pull-down will turn off and PGOOD will go high if an external pull-up resistor has been provided. An internal filter prevents nuisance trips of PGOOD due to short transients on V_{OUT}. Note that PGOOD can be pulled up to any voltage, as long as the absolute maximum rating of 18V is not exceeded, and as long as the maximum sink current rating is not exceeded when PGOOD is low. Note that PGOOD will also be driven low if V_{CC} is below its UVLO threshold or if the part is in shutdown (RUN below its logic threshold) while V_{CC} is being held up (or back-driven). PGOOD is not affected by V_{IN} UVLO or the accurate RUN threshold.

In cases where V_{CC} is not being back-driven in shutdown, PGOOD will not be held low indefinitely. The internal PGOOD pull-down will be disabled as the V_{CC} voltage decays below approximately 1V.

Maximum Power-Point Control (MPPC)

The MPPC input of the LTC3129 can be used with an optional external voltage divider to dynamically adjust the commanded inductor current in order to maintain a minimum input voltage when using high resistance sources, such as photovoltaic panels, so as to maximize input power transfer and prevent V_{IN} from dropping too low under load. Referring to Figure 3, the MPPC pin is internally connected to the non-inverting input of a g_m amplifier, whose inverting input is connected to the 1.175V reference. If the voltage at MPPC, using the external voltage divider, falls below the reference voltage, the output of the amplifier pulls the internal V_C node low. This reduces the commanded average inductor current so as to reduce the input current and regulate V_{IN} to the programmed minimum voltage, as given by:

$$V_{IN(MPPC)} = 1.175V \bullet (1 + R5/R6)$$

The MPPC feature provides capabilities to the LTC3129 that can ease the design of intrinsically safe power supplies.

Note that external compensation should not be required for MPPC loop stability if input filter capacitor, C_{IN}, is at least 22µF.

The divider resistor values can be in the MΩ range to minimize the input current in very low power applications. However, stray capacitance and noise pickup on the MPPC pin must also be minimized.

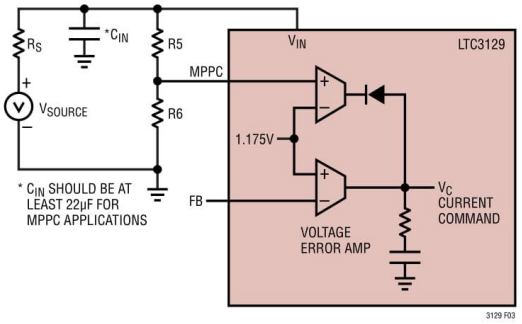

Figure 3. MPPC Amplifier with External Resistor Divider

OPERATION

The MPPC pin controls the converter in a linear fashion when using sources that can provide a minimum of 5mA to 10mA of continuous input current. For operation from weaker input sources, refer to the Applications Information section to see how the programmable RUN pin can be used to control the converter in a hysteretic manner to provide an effective MPPC function for sources that can provide as little as 5µA or less. If the MPPC function is not required, the MPPC pin should be tied to V_{CC}.

Thermal Considerations

The power switches of the LTC3129 are designed to operate continuously with currents up to the internal current limit thresholds. However, when operating at high current levels, there may be significant heat generated within the IC. In addition, the V_{CC} regulator can also generate wasted heat when V_{IN} is very high, adding to the total power dissipation of the IC. As described elsewhere in this data sheet, bootstrapping of the V_{CC} for 5V output applications can essentially eliminate the V_{CC} power dissipation term and significantly improve efficiency. As a result, careful consideration must be given to the thermal environment of the IC in order to provide a means to remove heat from the IC and ensure that the LTC3129 is able to provide its full rated output current. Specifically, the exposed die attach pad of both the QFN and MSE packages must be soldered to a copper layer on the PCB to maximize the conduction of heat out of the IC package. This can be accomplished by utilizing multiple vias from the die attach pad connection underneath the IC package to other PCB layer(s) containing a large copper plane. A typical board layout incorporating these concepts is shown in Figure 4.

If the IC die temperature exceeds approximately 180°C, over temperature shutdown will be invoked and all switching will be inhibited. The part will remain disabled until the die temperature cools by approximately 10°C. The soft-start circuit is re-initialized in overtemperature shutdown to provide a smooth recovery when the IC die temperature cools enough to resume operation.

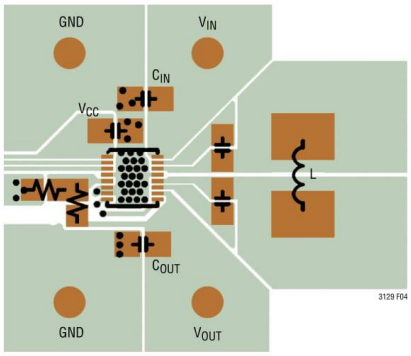

Figure 4. Typical 2-Layer PC Board Layout (MSE Package)

APPLICATIONS INFORMATION

A standard application circuit for the LTC3129 is shown on the front page of this data sheet. The appropriate selection of external components is dependent upon the required performance of the IC in each particular application given considerations and trade-offs such as PCB area, input and output voltage range, output voltage ripple, transient response, required efficiency, thermal considerations and cost. This section of the data sheet provides some basic guidelines and considerations to aid in the selection of external components and the design of the applications circuit, as well as more application circuit examples.

Programming V_{OUT}

The output voltage of the LTC3129 is set by connecting the FB pin to an external resistor divider from V_{OUT} to ground, as shown in Figure 5, according to the equation:

$$V_{OUT} = 1.175V \bullet (1+ R1/R2)$$

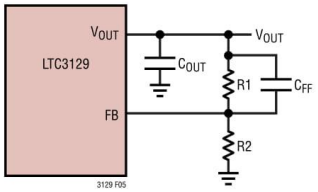

Figure 5. V_{OUT} Feedback Divider

A small feedforward capacitor can be added in parallel with R1 (in Figure 5) to reduce Burst Mode ripple and improve transient response. Details on selecting a feedforward capacitor are provided later in this data sheet.

V_{CC} Capacitor Selection

The V_{CC} output of the LTC3129 is generated from V_{IN} by a low dropout linear regulator. The V_{CC} regulator has been designed for stable operation with a wide range of output capacitors. For most applications, a low ESR capacitor of at least 2.2µF should be used. The capacitor should be located as close to the V_{CC} pin as possible and connected to the V_{CC} pin and ground through the shortest traces possible. V_{CC} is the regulator output and is also the internal supply pin for the LTC3129 control circuitry as well as the gate drivers and boost rail charging diodes. The V_{CC} pin is not intended to supply current to other external circuitry.

Inductor Selection

The choice of inductor used in LTC3129 application circuits influences the maximum deliverable output current, the converter bandwidth, the magnitude of the inductor current ripple and the overall converter efficiency. The inductor must have a low DC series resistance, when compared to the internal switch resistance, or output current capability and efficiency will be compromised. Larger inductor values reduce inductor current ripple but may not increase output current capability as is the case with peak current mode control as described in the Maximum Output Current section. Larger value inductors also tend to have a higher DC series resistance for a given case size, which will have a negative impact on efficiency. Larger values of inductance will also lower the right half plane (RHP) zero frequency when operating in boost mode, which can compromise loop stability. Nearly all LTC3129 application circuits deliver the best performance with an inductor value between 3.3µH and 10µH. Buck mode-only applications can use the larger inductor values as they are unaffected by the RHP zero, while mostly boost applications generally require inductance on the low end of this range depending on how large the step-up ratio is.

Regardless of inductor value, the saturation current rating should be selected such that it is greater than the worst-case average inductor current plus half of the ripple current. The peak-to-peak inductor current ripple for each operational mode can be calculated from the following formula, where f is the switching frequency (1.2MHz), L is the inductance in µH and t_{LOW} is the switch pin minimum low time in µs. The switch pin minimum low time is typically 0.09µs.

$$\Delta I_{L(P-P)(BUCK)} = \frac{V_{OUT}}{L}\left(\frac{V_{IN}-V_{OUT}}{V_{IN}}\right)\left(\frac{1}{f}-t_{LOW}\right) A$$

$$\Delta I_{L(P-P)(BOOST)} = \frac{V_{IN}}{L}\left(\frac{V_{OUT}-V_{IN}}{V_{OUT}}\right)\left(\frac{1}{f}-t_{LOW}\right) A$$

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It should be noted that the worst-case peak-to-peak inductor ripple current occurs when the duty cycle in buck mode is minimum (highest V_{IN}) and in boost mode when the duty cycle is 50% (V_{OUT} = 2 • V_{IN}). As an example, if V_{IN} (minimum) = 2.5V and V_{IN} (maximum) = 15V, V_{OUT} = 5V and L = 10µH, the peak-to-peak inductor ripples at the voltage extremes (15V V_{IN} for buck and 2.5V V_{IN} for boost) are:

Buck = 248mA peak-to-peak

Boost = 93mA peak-to-peak

One half of this inductor ripple current must be added to the highest expected average inductor current in order to select the proper saturation current rating for the inductor.

To avoid the possibility of inductor saturation during load transients, an inductor with a saturation current rating of at least 600mA is recommended for all applications.

In addition to its influence on power conversion efficiency, the inductor DC resistance can also impact the maximum output current capability of the buck-boost converter particularly at low input voltages. In buck mode, the output current of the buck-boost converter is primarily limited by the inductor current reaching the average current limit threshold. However, in boost mode, especially at large step-up ratios, the output current capability can also be limited by the total resistive losses in the power stage. These losses include, switch resistances, inductor DC resistance and PCB trace resistance. Avoid inductors with a high DC resistance (DCR) as they can degrade the maximum output current capability from what is shown in the Typical Performance Characteristics section and from the Typical Application circuits.

As a guideline, the inductor DCR should be significantly less than the typical power switch resistance of 750mΩ each. The only exceptions are applications that have a maximum output current requirement much less than what the LTC3129 is capable of delivering. Generally speaking, inductors with a DCR in the range of 0.15Ω to 0.3Ω are recommended. Lower values of DCR will improve the efficiency at the expense of size, while higher DCR values will reduce efficiency (typically by a few percent) while allowing the use of a physically smaller inductor.

Different inductor core materials and styles have an impact on the size and price of an inductor at any given current rating. Shielded construction is generally preferred as it minimizes the chances of interference with other circuitry. The choice of inductor style depends upon the price, sizing, and EMI requirements of a particular application. Table 1 provides a wide sampling of inductors that are well suited to many LTC3129 applications.

Table 1. Recommended Inductors

VENDOR	PART
Coilcraft www.coilcraft.com	EPL2014, EPL3012, EPL3015, LPS3015, LPS3314, XFL3012
Coiltronics www.cooperindustries.com	SDH3812, SD3814, SD3114, SD3118
Murata www.murata.com	LQH3NP, LQH32P, LQH44P
Sumida www.sumida.com	CDRH2D16, CDRH2D18, CDRH3D14, CDRH3D16
Taiyo-Yuden www.t-yuden.com	NR3012T, NR3015T, NRS4012T, BRC2518
TDK www.tdk.com	VLS3012, VLS3015, VLF302510MT, VLF302512MT
Toko www.tokoam.com	DB3015C, DB3018C, DB3020C, DP418C, DP420C, DEM2815C, DFE322512C, DFE252012C
Würth www.we-online.com	WE-TPC 2813, WE-TPC 3816, WE-TPC 2828

Recommended inductor values for different operating voltage ranges are given in Table 2. These values were chosen to minimize inductor size while maintaining an acceptable amount of inductor ripple current for a given V_{IN} and V_{OUT} range.

Table 2. Recommended Inductor Values

V_{IN} AND V_{OUT} RANGE	RECOMMENDED INDUCTOR VALUES
V_{IN} and V_{OUT} Both < 4.5V	3.3µH to 4.7µH
V_{IN} and V_{OUT} Both < 8V	4.7µH to 6.8µH
V_{IN} and V_{OUT} Both < 11V	6.8µH to 8.2µH
V_{IN} and V_{OUT} Up to 15.75V	8.2µH to 10µH

Feedforward Capacitor

The use of a voltage feedforward capacitor, as shown in Figure 5, offers a number of performance advantages. A feedforward capacitor will reduce output voltage ripple in

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Burst Mode operation and improve transient response. In addition, due to the wide V_{IN} and V_{OUT} operating range of the LTC3129 and its fixed internal loop compensation, some applications may require the use of a feedforward capacitor to assure light-load stability (less than ~15mA) when operating in PWM mode (PWM pin pulled high).

Therefore, to reduce Burst Mode ripple and improve phase margin at light load when PWM mode operation is selected, a feedforward capacitor is recommended for all applications. The recommended feedforward capacitor value can be calculated by:

$$C_{FF} = 66/R1$$

Where R1 is the top feedback divider resistor value in MΩ and C_{FF} is the recommended feedforward capacitor value in picofarads (use the nearest standard value). Refer to the application circuits for examples.

Output Capacitor Selection

A low effective series resistance (ESR) output capacitor of 4.7µF minimum should be connected at the output of the buck-boost converter in order to minimize output voltage ripple. Multilayer ceramic capacitors are an excellent option as they have low ESR and are available in small footprints. The capacitor value should be chosen large enough to reduce the output voltage ripple to acceptable levels. Neglecting the capacitor's ESR and ESL (effective series inductance), the peak-to-peak output voltage ripple in PWM mode can be calculated by the following formula, where f is the frequency in MHz (1.2MHz), C_{OUT} is the capacitance in µF, t_{LOW} is the switch pin minimum low time in µs (0.09µs typical) and I_{LOAD} is the output current in amperes.

$$\Delta V_{P-P(BUCK)} = \frac{I_{LOAD} t_{LOW}}{C_{OUT}} V$$

$$\Delta V_{P-P(BOOST)} = \frac{I_{LOAD}}{f C_{OUT}} \left(\frac{V_{OUT} - V_{IN} + t_{LOW} f V_{IN}}{V_{OUT}} \right) V$$

Examining the previous equations reveals that the output voltage ripple increases with load current and is generally higher in boost mode than in buck mode. Note that these equations only take into account the voltage ripple that occurs from the inductor current to the output being discontinuous. They provide a good approximation to the ripple at any significant load current but underestimate the output voltage ripple at very light loads where the output voltage ripple is dominated by the inductor current ripple.

In addition to the output voltage ripple generated across the output capacitance, there is also output voltage ripple produced across the internal resistance of the output capacitor. The ESR-generated output voltage ripple is proportional to the series resistance of the output capacitor and is given by the following expressions where R_{ESR} is the series resistance of the output capacitor and all other terms as previously defined.

$$\Delta V_{P-P(BUCK)} = \frac{I_{LOAD} R_{ESR}}{1 - t_{LOW} f} \cong I_{LOAD} R_{ESR} \; V$$

$$\Delta V_{P-P(BOOST)} = \frac{I_{LOAD} R_{ESR} V_{OUT}}{V_{IN} \left(1 - t_{LOW} f\right)}$$

$$\cong I_{LOAD} R_{ESR} \left(\frac{V_{OUT}}{V_{IN}} \right) V$$

In most LTC3129 applications, an output capacitor between 10µF and 22µF will work well. To minimize output ripple in Burst Mode operation, or transients incurred by large step loads, values of 22µF or larger are recommended.

Input Capacitor Selection

The V_{IN} pin carries the full inductor current and provides power to internal control circuits in the IC. To minimize input voltage ripple and ensure proper operation of the IC, a low ESR bypass capacitor with a value of at least 4.7µF should be located as close to the V_{IN} pin as possible. The traces connecting this capacitor to V_{IN} and the ground plane should be made as short as possible.

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When powered through long leads or from a power source with significant resistance, a larger value bulk input capacitor may be required and is generally recommended. In such applications, a 47µF to 100µF low-ESR electrolytic capacitor in parallel with a 1µF ceramic capacitor generally yields a high performance, low cost solution.

Note that applications using the MPPC feature should use a minimum C_{IN} of 22µF. Larger values can be used without limitation.

Recommended Input and Output Capacitor Types

The capacitors used to filter the input and output of the LTC3129 must have low ESR and must be rated to handle the AC currents generated by the switching converter. This is important to maintain proper functioning of the IC and to reduce output voltage ripple. There are many capacitor types that are well suited to these applications including multilayer ceramic, low ESR tantalum, OS-CON and POSCAP technologies. In addition, there are certain types of electrolytic capacitors such as solid aluminum organic polymer capacitors that are designed for low ESR and high AC currents and these are also well suited to some LTC3129 applications. The choice of capacitor technology is primarily dictated by a trade-off between size, leakage current and cost. In backup power applications, the input or output capacitor might be a super or ultra capacitor with a capacitance value measuring in the Farad range. The selection criteria in these applications are generally similar except that voltage ripple is generally not a concern. Some capacitors exhibit a high DC leakage current which may preclude their consideration for applications that require a very low quiescent current in Burst Mode operation. Note that ultra capacitors may have a rather high ESR, therefore a 4.7µF (minimum) ceramic capacitor is recommended in parallel, close to the IC pins.

Ceramic capacitors are often utilized in switching converter applications due to their small size, low ESR and low leakage currents. However, many ceramic capacitors intended for power applications experience a significant loss in capacitance from their rated value as the DC bias voltage on the capacitor increases. It is not uncommon for a small surface mount capacitor to lose more than 50% of its rated capacitance when operated at even half of its maximum rated voltage. This effect is generally reduced as the case size is increased for the same nominal value capacitor. As a result, it is often necessary to use a larger value capacitance or a higher voltage rated capacitor than would ordinarily be required to actually realize the intended capacitance at the operating voltage of the application. X5R and X7R dielectric types are recommended as they exhibit the best performance over the wide operating range and temperature of the LTC3129. To verify that the intended capacitance is achieved in the application circuit, be sure to consult the capacitor vendor's curve of capacitance versus DC bias voltage.

Using the Programmable RUN Function to Operate from Extremely Weak Input Sources

Another application of the programmable RUN pin is that it can be used to operate the converter in a hiccup mode from extremely low current sources. This allows operation from sources that can only generate microamps of output current, and would be far too weak to sustain normal steady-state operation, even with the use of the MPPC pin. Because the LTC3129 draws only 1.9µA typical from V_{IN} until it is enabled, the RUN pin can be programmed to keep the IC disabled until V_{IN} reaches the programmed voltage level. In this manner, the input source can trickle-charge an input storage capacitor, even if it can only supply microamps of current, until V_{IN} reaches the turn-on threshold set by the RUN pin divider. The converter will then be enabled using the stored charge in the input capacitor, until Vin drops below the turn-off threshold, at which point the converter will turn off and the process will repeat.

This approach allows the converter to run from weak sources such as thin-film solar cells using indoor lighting. Although the converter will be operating in bursts, it is enough to charge an output capacitor to power low duty cycle loads, such as wireless sensor applications, or to trickle charge a battery. In addition, note that the input voltage will be cycling (with a small ripple as set by the RUN hysteresis) about a fixed voltage, as determined by the divider. This allows the high impedance source to operate at the programmed optimal voltage for maximum power transfer.

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When using high value divider resistors (in the MΩ range) to minimize current draw on V_{IN}, a small noise filter capacitor may be necessary across the lower divider resistor to prevent noise from erroneously tripping the RUN comparator. The capacitor value should be minimized so as not to introduce a time delay long enough for the input voltage to drop significantly below the desired V_{IN} threshold before the converter is turned off. Note that larger V_{IN} decoupling capacitor values will minimize this effect by providing more holdup time on V_{IN}.

Programming the MPPC Voltage

As discussed in the previous section, the LTC3129 includes an MPPC function to optimize performance when operating from voltage sources with relatively high source resistance. Using an external voltage divider from V_{IN}, the MPPC function takes control of the average inductor current when necessary to maintain a minimum input voltage, as programmed by the user. Referring to Figure 3:

$$V_{IN(MPPC)} = 1.175V \bullet (1 + R5/R6)$$

This is useful for such applications as photovoltaic powered converters, since the maximum power transfer point occurs when the photovoltaic panel is operated at about 75% of its open-circuit voltage. For example, when operating from a photovoltaic panel with an open-circuit voltage of 5V, the maximum power transfer point will be when the panel is loaded such that its output voltage is about 3.75V. Choosing values of 2MΩ for R5 and 909kΩ for R6 will program the MPPC function to regulate the maximum input current so as to maintain V_{IN} at a minimum of 3.74V (typical). Note that if the panel can provide more power than the LTC3129 can draw, the input voltage will rise above the programmed MPPC point. This is fine as long as the input voltage doesn't exceed 15V.

For weak input sources with very high resistance (hundreds of Ohms or more), the LTC3129 may still draw more current than the source can provide, causing V_{IN} to drop below the UVLO threshold. For these applications, it is recommended that the programmable RUN feature be used, as described in the previous section.

MPPC Compensation and Gain

When using MPPC, there are a number of variables that affect the gain and phase of the input voltage control loop. Primarily these are the input capacitance, the MPPC divider ratio and the V_{IN} source resistance (or current). To simplify the design of the application circuit, the MPPC control loop in the LTC3129 is designed with a relatively low gain, such that external MPPC loop compensation is generally not required when using a V_{IN} capacitor value of at least 22µF. The gain from the MPPC pin to the internal VC control voltage is about 12, so a drop of 50mV on the MPPC pin (below the 1.175V MPPC threshold), corresponds to a 600mV drop on the internal VC voltage, which reduces the average inductor current all the way to zero. Therefore, the programmed input MPPC voltage will be maintained within about 4% over the load range.

Note that if large value V_{IN} capacitors are used (which may have a relatively high ESR) a small ceramic capacitor of at least 4.7µF should be placed in parallel across the V_{IN} input, near the V_{IN} pin of the IC.

Bootstrapping the V_{CC} Regulator

The high and low side gate drivers are powered through the V_{CC} rail, which is generated from the input voltage, V_{IN}, through an internal linear regulator. In some applications, especially at high input voltages, the power dissipation in the linear regulator can become a major contributor to thermal heating of the IC and overall efficiency. The Typical Performance Characteristics section provides data on the V_{CC} current and resulting power loss versus V_{IN} and V_{OUT}.

A significant performance advantage can be attained in high V_{IN} applications where converter output voltage (V_{OUT}) is programmed to 5V, if V_{OUT} is used to power the V_{CC} rail. Powering V_{CC} in this manner is referred to as bootstrapping. This can be done by connecting a Schottky diode (such as a BAT54) from V_{OUT} to V_{CC} as shown in Figure 6. With the bootstrap diode installed, the gate driver currents are supplied by the buck-boost converter at high efficiency rather than through the internal linear regulator. The internal linear regulator contains reverse blocking circuitry

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that allows V_{CC} to be driven above its nominal regulation level with only a very slight amount of reverse current. Please note that the bootstrapping supply (either V_{OUT} or a separate regulator) must be limited to less than 5.7V so as not to exceed the maximum V_{CC} voltage of 5.5V after the diode drop.

By maintaining V_{CC} above its UVLO threshold, bootstrapping, even to a 3.3V output, also allows operation down to the V_{IN} UVLO threshold of 1.8V (typical).

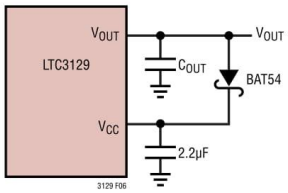


Figure 6. Example of V_{CC} Bootstrap

Sources of Small Photovoltaic Panels

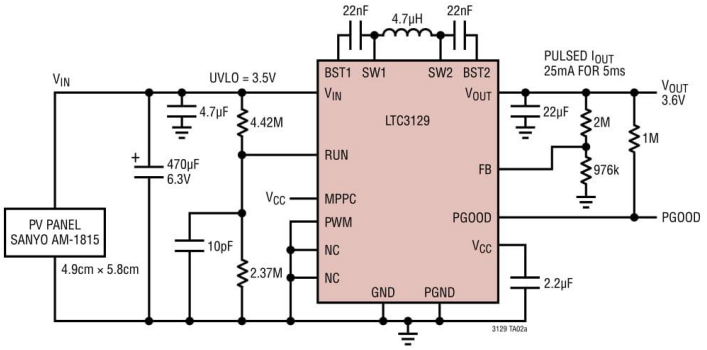
A list of companies that manufacture small solar panels (sometimes referred to as modules or solar cell arrays) suitable for use with the LTC3129 is provided in Table 3.

Table 3. Small Photovoltaic Panel Manufacturers

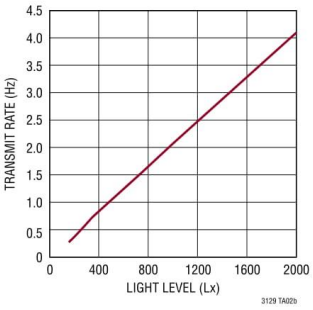
Sanyo	http://panasonic.net/energy/amorton/en/
PowerFilm	http://www.powerfilmsolar.com/
Ixys Corporation	http://www.ixys.com/ProductPortfolio/GreenEnergy.aspx
G24 Innovations	http://www.g24i.com/

TYPICAL APPLICATIONS

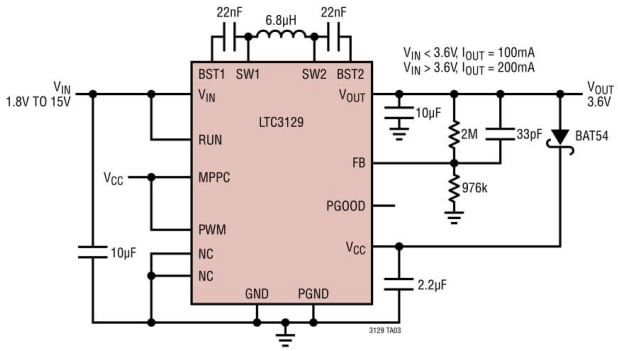
Hiccup Converter Powers Wireless Sensor from Indoor Lighting



Transmit Rate vs Light Level (Fluorescent)

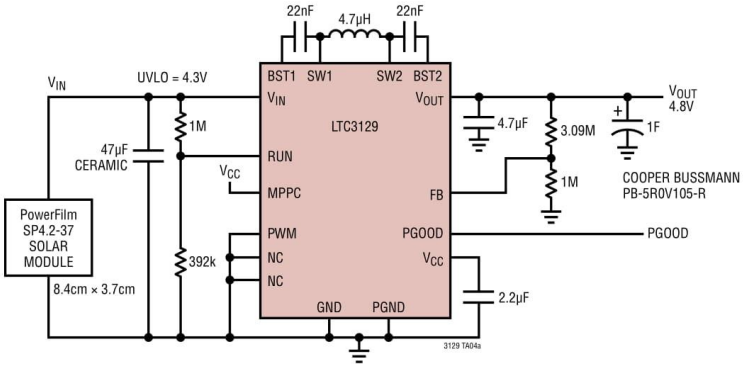


Low Noise 3.6V Converter Using Bootstrap Diode to Extend Lower V_{IN} Range

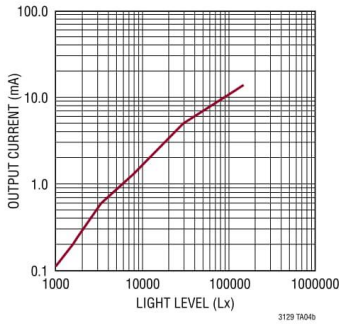


TYPICAL APPLICATIONS

Solar Powered Converter with MPPC Charges Storage Capacitor

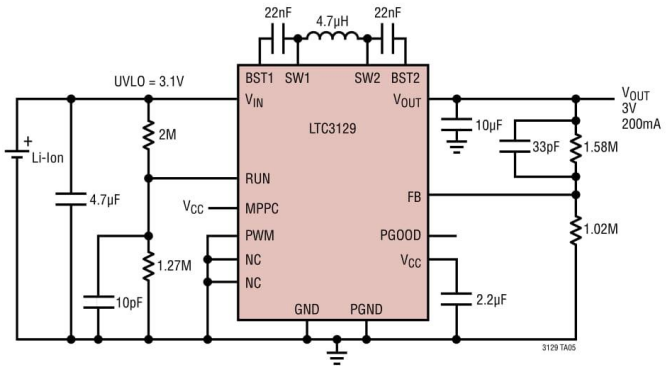


Average Output Current vs Light Level (Daylight)

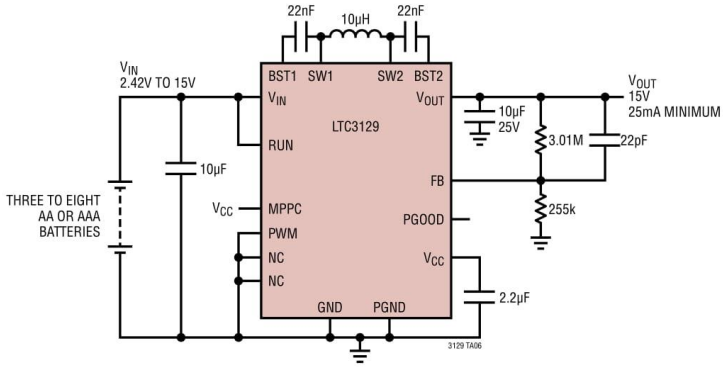


TYPICAL APPLICATIONS

Li-Ion Powered 3V Converter with 3.1V Input UVLO Reduces Low Battery I_Q to 3µA

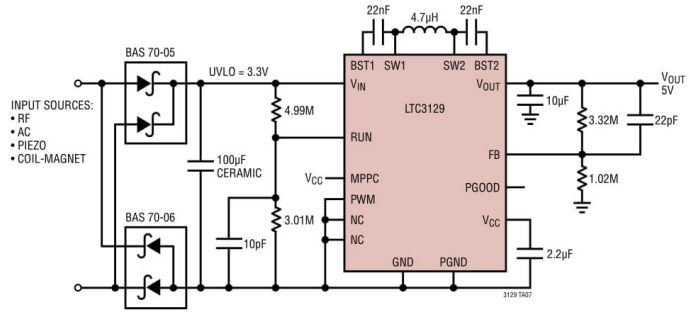


15V Converter Operates from Three to Eight AA or AAA Cells

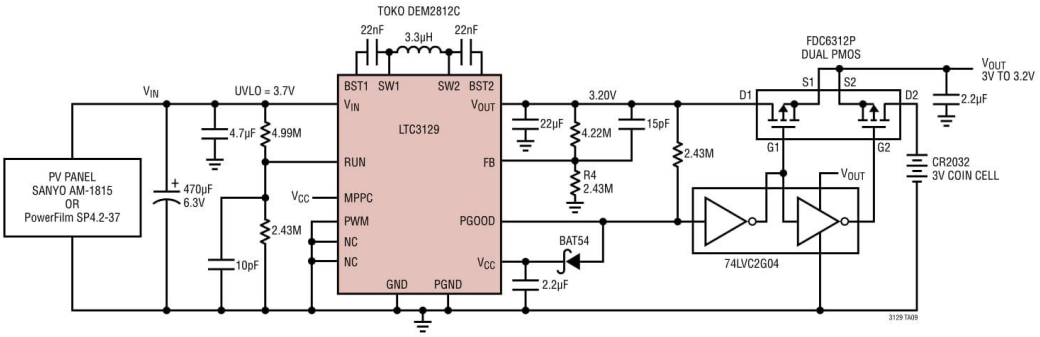


TYPICAL APPLICATIONS

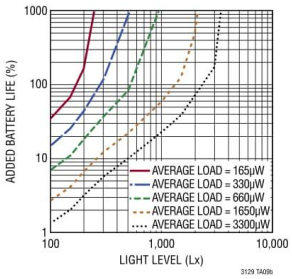
Energy Harvesting Converter Operates from a Variety of Weak Sources



Solar Powered Converter Extends Battery Life in Low Power 3V Primary Battery Applications



Percentage of Added Battery Life vs Light Level and Load (PowerFilm SP4.2-37, 30sq cm Panel)

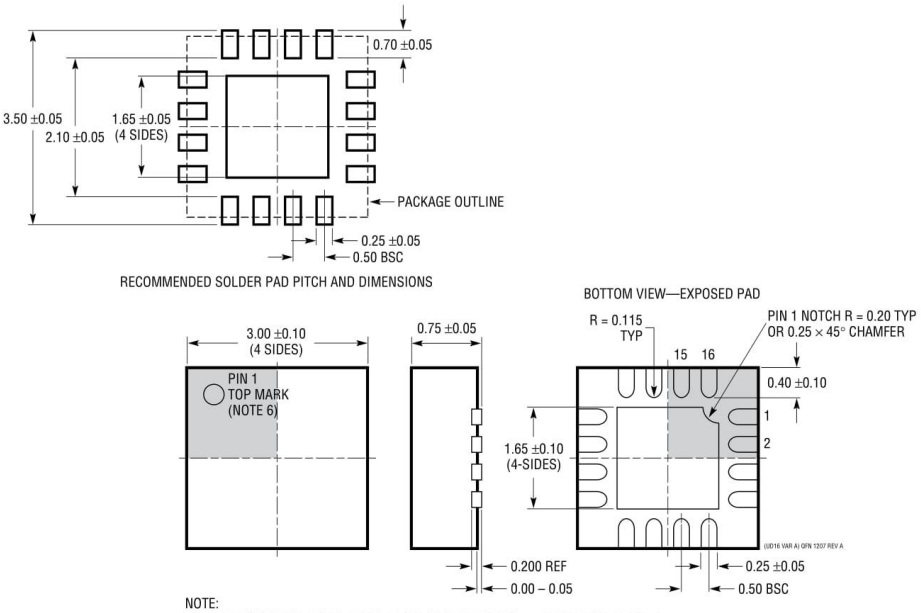


PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3129#packaging for the most recent package drawings.

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1700 Rev A)

Exposed Pad Variation AA

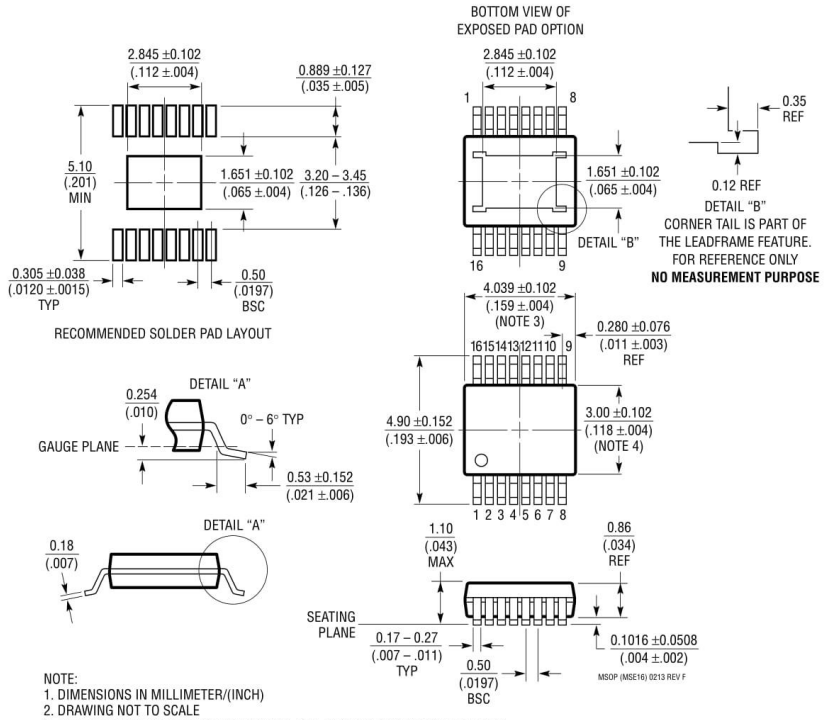


NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-4)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3129#packaging for the most recent package drawings.

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev F)



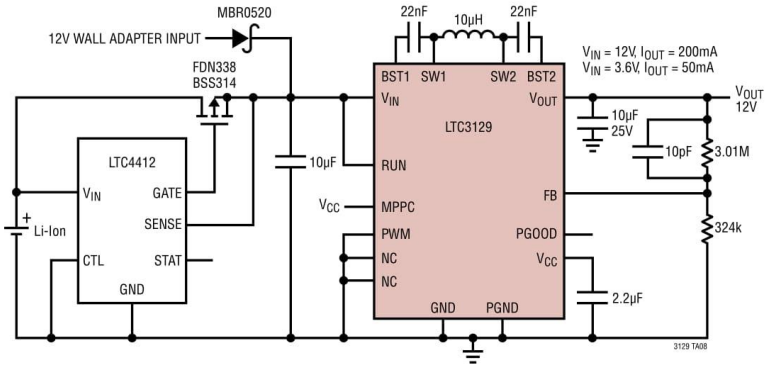
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	5/14	Clarified V_{CC} Leakage to V_{IN} if $V_{CC} > V_{IN}$: from –7µA to –27µA	4
B	10/14	Clarified typ V_{OUT} Current in Sleep Mode Clarified PGOOD Pin Description Clarified Operation Paragraph	4 8 15
C	10/15	Changed MAX V_{CC} Current Limit Modified MPPC section Modified Table 3	3 15 22

TYPICAL APPLICATION

Dual V_{IN} Application, Using the LTC4412 PowerPath™ Controller



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3103	15V, 300mA Synchronous Step-Down DC/DC Converter with Ultralow Quiescent Current	$V_{IN(MIN)}$ = 2.2V, $V_{IN(MAX)}$ = 15V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 1.8µA, I_{SD} <1µA, 3mm × 3mm DFN-10, MSOP-10 Packages
LTC3104	15V, 300mA Synchronous Step-Down DC/DC Converter with Ultralow Quiescent Current and 10mA LDO	$V_{IN(MIN)}$ = 2.2V, $V_{IN(MAX)}$ = 15V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.8µA, I_{SD} <1µA, 4mm × 3mm DFN-14, MSOP-16 Packages
LTC3105	400mA Step-up Converter with MPPC and 250mV Start-Up	$V_{IN(MIN)}$ = 0.2V, $V_{IN(MAX)}$ = 5V, $V_{OUT(MIN)}$ = 0 5.25V_{MAX}, I_Q = 22µA, I_{SD} <1µA, 3mm × 3mm DFN-10/MSOP-12 Packages
LTC3112	15V, 2.5A, 750kHz Monolithic Synch Buck/Boost	$V_{IN(MIN)}$ = 2.7V, $V_{IN(MAX)}$ = 15V, $V_{OUT(MIN)}$ = 2.7V to 14V, I_Q = 50µA, I_{SD} <1µA, 4mm × 5mm DFN-16 TSSOP-20E Packages
LTC3115-1	40V, 2A, 2MHz Monolithic Synch Buck/Boost	$V_{IN(MIN)}$ = 2.7V, $V_{IN(MAX)}$ = 40V, $V_{OUT(MIN)}$ = 2.7V to 40V, I_Q = 50µA, I_{SD} <1µA, 4mm × 5mm DFN-16 and TSSOP-20E Packages
LTC3531	5.5V, 200mA, 600kHz Monolithic Synch Buck/Boost	$V_{IN(MIN)}$ = 1.8V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 2V to 5V, I_Q = 16µA, I_{SD} <1µA, 3mm × 3mm DFN-8 and ThinSOT Packages
LTC3388-1/ LTC3388-3	20V, 50mA High Efficiency Nano Power Step-Down Regulator	$V_{IN(MIN)}$ = 2.7V, $V_{IN(MAX)}$ =20V, $V_{OUT(MIN)}$ = Fixed 1.1V to 5.5V, I_Q = 720nA, I_{SD} = 400nA, 3mm × 3mm DFN-10, MSOP-10 Packages
LTC3108/ LTC3108-1	Ultralow Voltage Step-Up Converter and Power Manager	$V_{IN(MIN)}$ = 0.02V, $V_{IN(MAX)}$ = 1V, $V_{OUT(MIN)}$ = Fixed 2.35V to 5V, I_Q = 6µA, I_{SD} <1µA, 3mm × 4mm DFN-12, SSOP-16 Packages
LTC3109	Auto-Polarity, Ultralow Voltage Step-Up Converter and Power Manager	$V_{IN(MIN)}$ = 0.03V, $V_{IN(MAX)}$ = 1V, $V_{OUT(MIN)}$ = Fixed 2.35V to 5V, I_Q = 7µA, I_{SD} <1µA, 4mm × 4mm QFN-20, SSOP-20 Packages
LTC3588-1	Piezo Electric Energy Harvesting Power Supply	$V_{IN(MIN)}$ = 2.7V, $V_{IN(MAX)}$ = 20V, $V_{OUT(MIN)}$ = Fixed 1.8V to 3.6V, I_Q = 950nA, I_{SD} 450nA, 3mm × 3mm DFN-10, MSOP-10E Packages
LTC4070	Li-Ion/Polymer Low Current Shunt Battery Charger System	$V_{IN(MIN)}$ = 450nA to 50mA, V_{FLOAT} + 4.0V, 4.1V, 4.2V, I_Q = 300nA, 2mm × 3mm DFN-8, MSOP-8 Packages

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LTC3105

400mA Step-Up DC/DC Converter with Maximum Power Point Control and 250mV Start-Up

FEATURES

- **Low Start-Up Voltage: 250mV**
- **Maximum Power Point Control**
- **Wide V_{IN} Range: 225mV to 5V**
- **Auxiliary 6mA LDO Regulator**
- **Burst Mode® Operation: I_Q = 24µA**
- Output Disconnect and Inrush Current Limiting
- $V_{IN} > V_{OUT}$ Operation
- Antiringing Control
- Soft Start
- Automatic Power Adjust
- Power Good Indicator
- 10-Lead 3mm × 3mm × 0.75mm DFN and 12-Lead MSOP Packages

APPLICATIONS

- Solar Powered Battery/Supercapacitor Chargers
- Energy Harvesting
- Remote Industrial Sensors
- Low Power Wireless Transmitters
- Cell Phone, MP3, PMP and GPS Accessory Chargers

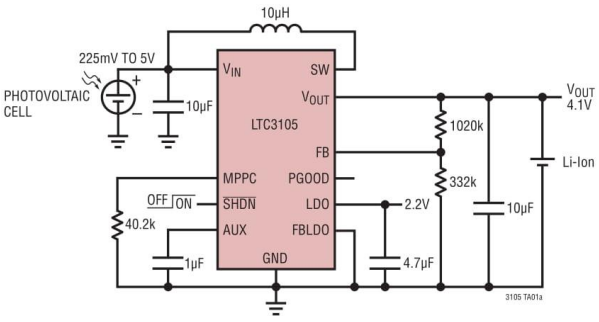
DESCRIPTION

The LTC®3105 is a high efficiency step-up DC/DC converter that can operate from input voltages as low as 225mV. A 250mV start-up capability and integrated maximum power point controller (MPPC) enable operation directly from low voltage, high impedance alternative power sources such as photovoltaic cells, TEGs (thermoelectric generators) and fuel cells. A user programmable MPPC set point maximizes the energy that can be extracted from any power source. Burst Mode operation, with a proprietary self adjusting peak current, optimizes converter efficiency and output voltage ripple over all operating conditions.

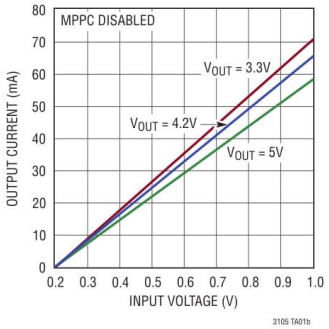
The AUX powered 6mA LDO provides a regulated rail for external microcontrollers and sensors while the main output is charging. In shutdown, I_Q is reduced to 10µA and integrated thermal shutdown offers protection from overtemperature faults. The LTC3105 is offered in 10-lead 3mm × 3mm × 0.75mm DFN and 12-lead MSOP packages.

TYPICAL APPLICATION

Single Photovoltaic Cell Li-Ion Trickle Charger



Output Current vs Input Voltage



ABSOLUTE MAXIMUM RATINGS (Note 1)

SW Voltage
- DC ..... –0.3V to 6V
- Pulsed (<100ns) ..... –1V to 7V

Voltage, All Other Pins ..... –0.3V to 6V
Operating Junction Temperature Range (Note 2) ..... –40°C to 85°C
Maximum Junction Temperature (Note 4) ..... 125°C
Storage Temperature ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.)
- MS Package ..... 300°C

PIN CONFIGURATION

DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC} = 3°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

MS PACKAGE
12-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 130°C/W, θ_{JC} = 21°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3105EDD#PBF	LTC3105EDD#TRPBF	LFQC	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC3105EMS#PBF	LTC3105EMS#TRPBF	3105	12-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{AUX} = V_{OUT} = 3.3V, V_{LDO} = 2.2V, V_{IN} = 0.6V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Step-Up Converter						
Input Operating Voltage		●	0.225		5	V
Input Start-Up Voltage	(Note 5) T_J = 0°C to 85°C (Note 5)	●		0.25	0.4 0.36	V V
Output Voltage Adjust Range		●	1.6		5.25	V
Feedback Voltage (FB Pin)		●	0.984	1.004	1.024	V
V_{OUT} I_Q in Operation	V_{FB} = 1.10V			24		µA
V_{OUT} I_Q in Shutdown	$\overline{SHDN}$ = 0V			10		µA
MPPC Pin Output Current	V_{MPPC} = 0.6V		9.72	10	10.28	µA
$\overline{SHDN}$ Input Logic High Voltage		●	1.1			V
$\overline{SHDN}$ Input Logic Low Voltage		●			0.3	V
N-Channel SW Pin Leakage Current	V_{IN} = V_{SW} = 5V, $V_{\overline{SHDN}}$ = 0V			1	10	µA
P-Channel SW Pin Leakage Current	V_{IN} = V_{SW} = 0V, V_{OUT} = V_{AUX} = 5.25V			1	10	µA
N-Channel On-Resistance: SW to GND				0.5		Ω
P-Channel On-Resistance: SW to V_{OUT}				0.5		Ω
Peak Current Limit	V_{FB} = 0.90V, V_{MPPC} = 0.4V (Note 3)		0.4	0.5		A
Valley Current Limit	V_{FB} = 0.90V, V_{MPPC} = 0.4V (Note 3)		0.275	0.35		A
PGOOD Threshold (% of Feedback Voltage)	V_{OUT} Falling		85	90	95	%
LDO Regulator						
LDO Output Adjust Range	External Feedback Network, V_{AUX} > V_{LDO}	●	1.4		5	V
LDO Output Voltage	V_{FBLDO} = 0V	●	2.148	2.2	2.236	V
Feedback Voltage (FBLDO Pin)	External Feedback Network	●	0.984	1.004	1.024	V
Load Regulation	I_{LDO} = 1mA to 6mA			0.40		%
Line Regulation	V_{AUX} = 2.5V to 5V			0.15		%
Dropout Voltage	I_{LDO} = 6mA, V_{OUT} = V_{AUX} = 2.2V			105		mV
LDO Current Limit	V_{LDO} 0.5V Below Regulation Voltage	●	6	12		mA
LDO Reverse-Blocking Leakage Current	V_{IN} = V_{AUX} = V_{OUT} = 0V, $V_{\overline{SHDN}}$ = 0V			1		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3105 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3105E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 85°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: Current measurements are performed when the LTC3105 is not switching. The current limit values measured in operation will be somewhat higher due to the propagation delay of the comparators.

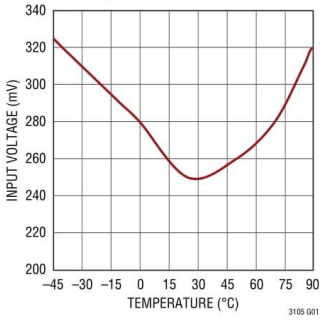
Note 4: This IC includes over temperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 5: The LTC3105 has been optimized for use with high impedance power sources such as photovoltaic cells and thermoelectric generators. The input start-up voltage is measured using an input voltage source with a series resistance of approximately 200mΩ and MPPC enabled. Use of the LTC3105 with lower resistance voltage sources or with MPPC disabled may result in a higher input start-up voltage.

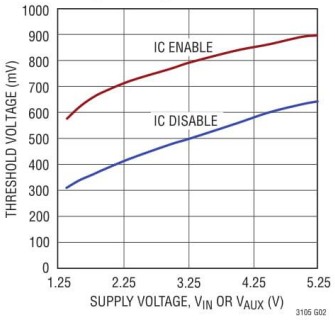
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{AUX} = V_{OUT} = 3.3V, V_{LDO} = 2.2V, V_{IN} = 0.6V, unless otherwise noted.

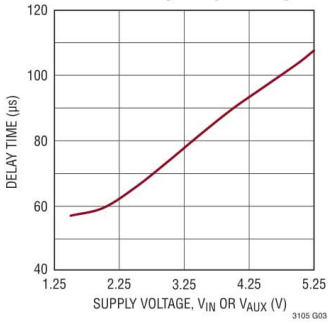
Minimum Input Start-Up Voltage vs Temperature



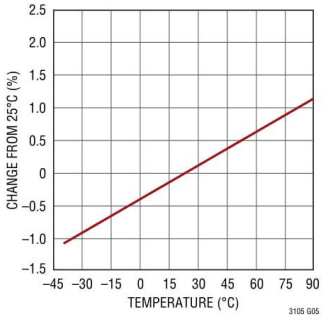
Shutdown Thresholds vs Input Voltage



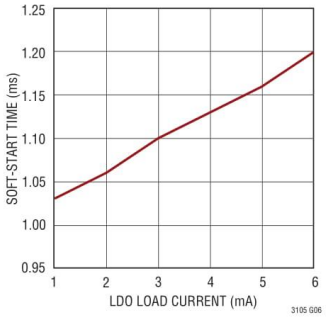
IC Enable Delay vs Input Voltage



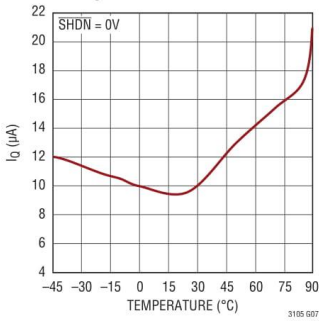
MPPC Current Variation vs Temperature



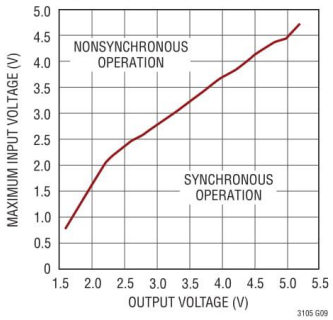
LDO Soft-Start Duration vs LDO Load



V_{OUT} I_Q vs Temperature During Shutdown



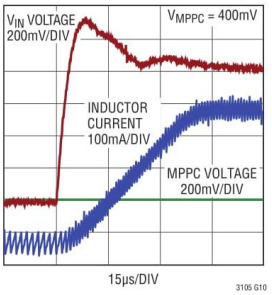
V_{IN} for Synchronous Operation



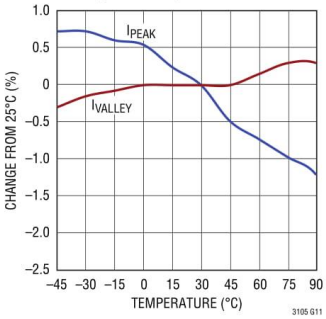
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{AUX} = V_{OUT} = 3.3V, V_{LDO} = 2.2V, V_{IN} = 0.6V, unless otherwise noted.

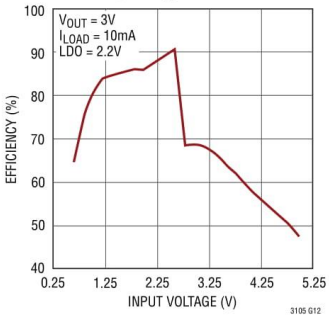
Exiting MPPC Control on Input Voltage Step



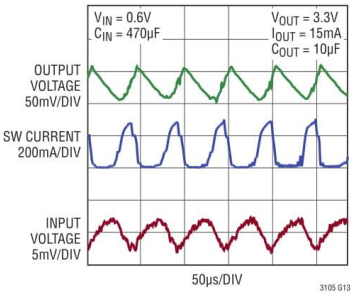
I_{PEAK} and I_{VALLEY} Current Limit Change vs Temperature



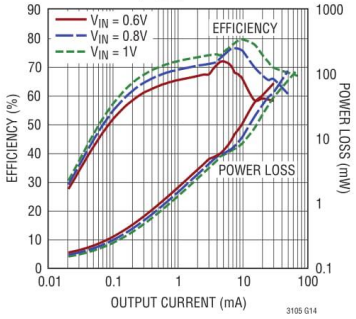
Efficiency vs V_{IN}



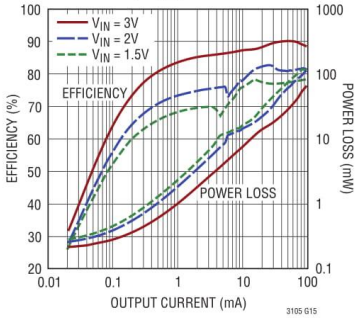
Input and Output Burst Ripple



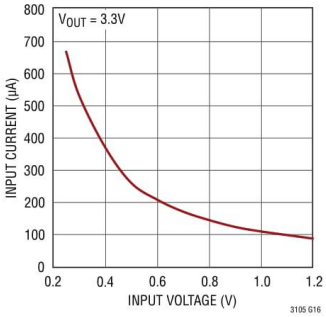
Efficiency vs Output Current and Power Loss, V_{OUT} = 3.3V



Efficiency vs Output Current and Power Loss, V_{OUT} = 5V



No-Load Input Current vs Input Voltage



PIN FUNCTIONS (DFN/MSOP)

FB (Pin 1/Pin 1): Step-Up Converter Feedback Input. Connect the V_{OUT} resistor divider tap to this input. The output voltage can be adjusted between 1.6V and 5.25V.

LDO (Pin 2/Pin 2): LDO Regulator Output. Connect a 4.7µF or larger capacitor between LDO and GND.

FBLDO (Pin 3/Pin 3): LDO Feedback Input. Connect the LDO resistive divider tab to this input. Alternatively, connecting FBLDO directly to GND will configure the LDO output voltage to be internally set at 2.2V (nominal).

$\overline{\text{SHDN}}$ (Pin 4/Pin 4): Logic Controlled Shutdown Input. With $\overline{\text{SHDN}}$ open, the converter is enabled by an internal 2MΩ pull-up resistor. The $\overline{\text{SHDN}}$ pin should be driven with an open-drain or open-collector pull-down and floated until the converter has entered normal operation. Excessive loading on this pin may cause a failure to complete start-up.

$\overline{\text{SHDN}}$ = Low: IC Disabled

$\overline{\text{SHDN}}$ = High: IC Enabled

MPPC (Pin 5/Pin 5): Set Point Input for Maximum Power Point Control. Connect a resistor from MPPC to GND to program the activation point for the MPPC loop. To disable the MPPC circuit, connect MPPC directly to GND.

V_{IN} (Pin 6/Pin 8): Input Supply. Connect a decoupling capacitor between this pin and GND. The PCB trace length from the V_{IN} pin to the decoupling capacitor should be as short and wide as possible. When used with high impedance sources such as photovoltaic cells, this pin should have a 10µF or larger decoupling capacitor.

GND (Exposed Pad Pin 11/Pins 6, 7) : Small Signal and Power Ground for the IC. The GND connections should be soldered to the PCB ground using the lowest impedance path possible.

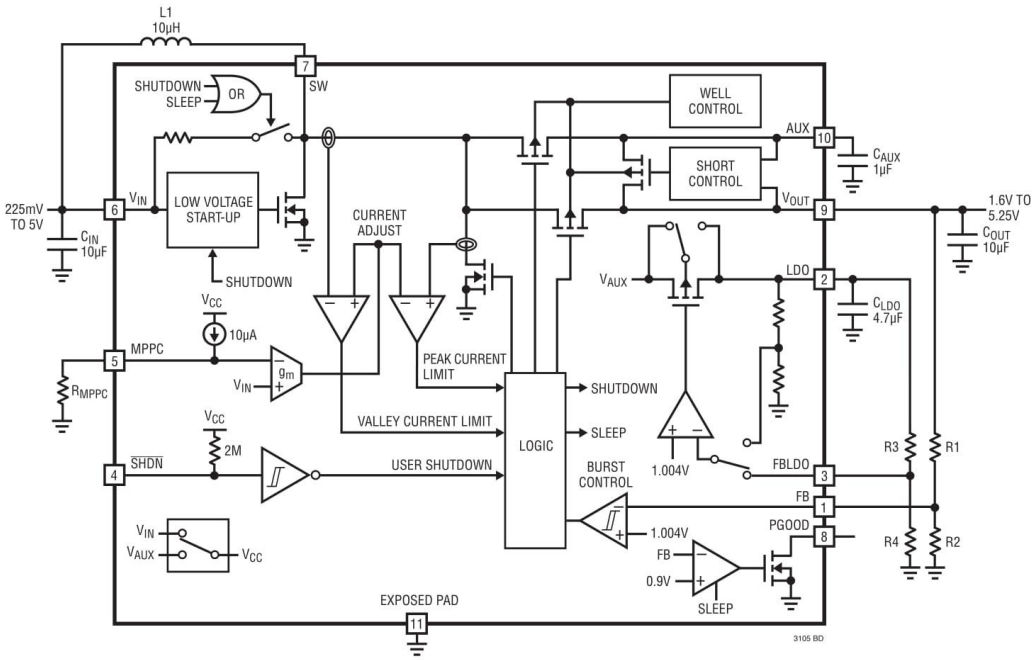
SW (Pin 7/Pin 9): Switch Pin. Connect an inductor between SW and V_{IN}. PCB trace lengths should be as short as possible to reduce EMI. While the converter is sleeping or is in shutdown, the internal antiringing switch connects the SW pin to the V_{IN} pin in order to minimize EMI.

PGOOD (Pin 8/Pin 10): Power Good Indicator. This is an open-drain output. The pull-down is disabled when V_{OUT} has achieved the voltage defined by the feedback divider on the FB pin. The pull-down is also disabled while the IC is in shutdown or start-up mode.

V_{OUT} (Pin 9/Pin 11): Step-Up Converter Output. This is the drain connection of the main output internal synchronous rectifier. A 10µF or larger capacitor must be connected between this pin and GND. The PCB trace length from the V_{OUT} pin to the output filter capacitor should be as short and wide as possible.

AUX (Pin 10/Pin 12): Auxiliary Voltage. Connect a 1µF capacitor between this pin and GND. This pin is used by the start-up circuitry to generate a voltage rail to power internal circuitry until the main output reaches regulation. AUX and V_{OUT} are internally connected together once V_{OUT} exceeds V_{AUX}.

BLOCK DIAGRAM (Pin Numbers for DFN Package Only)



OPERATION

Introduction

The LTC3105 is a unique, high performance, synchronous boost converter that incorporates maximum power point control, 250mV start-up capability and an integrated LDO regulator. This part operates over a very wide range of input voltages from 225mV to 5V. Its Burst Mode architecture and low 24µA quiescent current optimize efficiency in low power applications.

An integrated maximum power point controller allows for operation directly from high impedance sources such as photovoltaic cells by preventing the input power source voltage from collapsing below the user programmable MPPC threshold. Peak current limits are automatically adjusted with proprietary techniques to maintain operation at levels that maximize power extraction from the source.

The 250mV start-up voltage and 225mV minimum operating voltage enable direct operation from a single photovoltaic cell and other very low voltage, high series impedance power sources such as TEGs and fuel cells.

Synchronous rectification provides high efficiency operation while eliminating the need for external Schottky diodes. The LTC3105 provides output disconnect which prevents large inrush currents during start-up. This is particularly important for high internal resistance power sources like photovoltaic cells and thermoelectric generators which can become overloaded if inrush current is not limited during start-up of the power converter. In addition, output disconnect isolates V_{OUT} from V_{IN} while in shutdown.

$V_{IN} > V_{OUT}$ Operation

The LTC3105 includes the ability to seamlessly maintain regulation if V_{IN} becomes equal to or greater than V_{OUT}. With V_{IN} greater than or equal to V_{OUT}, the synchronous rectifiers are disabled which may result in reduced efficiency.

Shutdown Control

The $\overline{SHDN}$ pin is an active low input that places the IC into low current shutdown mode. This pin incorporates an internal 2MΩ pull-up resistor which enables the converter if the $\overline{SHDN}$ pin is not controlled by an external circuit. The $\overline{SHDN}$ pin should be allowed to float while the part is in start-up mode. Once in normal operation, the $\overline{SHDN}$ pin may be controlled using an open-drain or open-collector pull-down. Other external loads on this pin should be avoided, as they may result in the part failing to reach regulation. In shutdown, the internal switch connecting AUX and V_{OUT} is enabled.

When the $\overline{SHDN}$ pin is released, the LTC3105 is enabled and begins switching after a short delay. When either V_{IN} or V_{AUX} is above 1.4V, this delay will typically range between 20µs and 100µs. Refer to the Typical Performance Characteristics section for more details.

Start-Up Mode Operation

The LTC3105 provides the capability to start with voltages as low as 250mV. During start-up the AUX output initially is charged with the synchronous rectifiers disabled. Once V_{AUX} has reached approximately 1.4V, the converter leaves start-up mode and enters normal operation. Maximum power point control is not enabled during start-up, however, the currents are internally limited to sufficiently low levels to allow start-up from weak input sources.

While the converter is in start-up mode, the internal switch between AUX and V_{OUT} remains disabled and the LDO is disabled. Refer to Figure 1 for an example of a typical start-up sequence.

The LTC3105 is optimized for use with high impedance power sources such as photovoltaic cells. For operation from very low impedance, low input voltage sources, it may be necessary to add several hundred milliohms of series input resistance to allow for proper low voltage start-up.

Normal Operation

When either V_{IN} or V_{AUX} is greater than 1.4V typical, the converter will enter normal operation.

The converter continues charging the AUX output until the LDO output enters regulation. Once the LDO output is in regulation, the converter begins charging the V_{OUT} pin. V_{AUX} is maintained at a level sufficient to ensure the LDO remains in regulation. If V_{AUX} becomes higher than required to maintain LDO regulation, charge is transferred from the AUX output to the V_{OUT} output. If V_{AUX} falls too low, current is redirected to the AUX output instead of being used to charge the V_{OUT} output. Once V_{OUT} rises

OPERATION

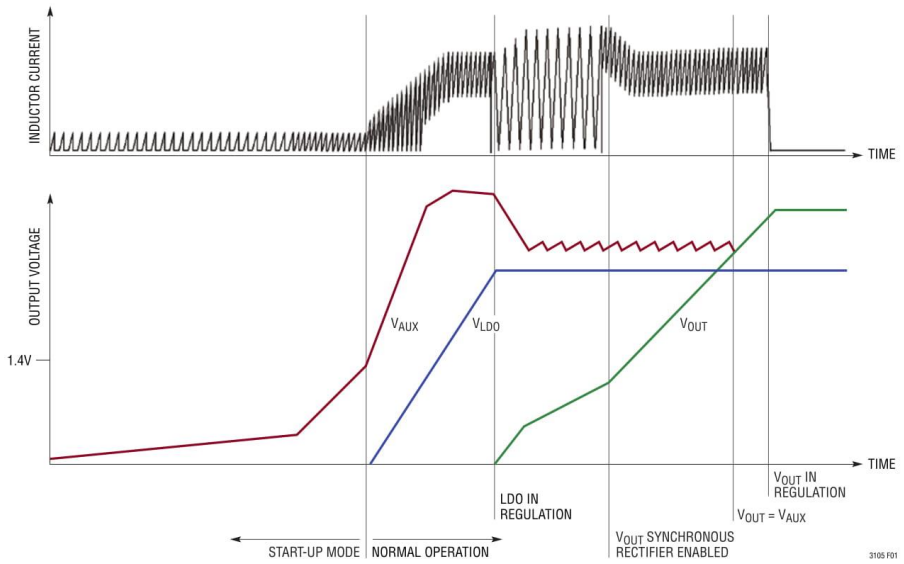


Figure 1. Typical Converter Start-Up Sequence

above V_{AUX}, an internal switch is enabled to connect the two outputs together.

If V_{IN} is greater than the voltage on the driven output (V_{OUT} or V_{AUX}), or the driven output is less than 1.2V (typical), the synchronous rectifiers are disabled. With the synchronous rectifiers disabled, the converter operates in critical conduction mode. In this mode, the N-channel MOSFET between SW and GND is enabled and remains on until the inductor current reaches the peak current limit. It is then disabled and the inductor current discharges completely before the cycle is repeated.

When the output voltage is greater than the input voltage and greater than 1.2V, the synchronous rectifier is enabled. In this mode, the N-channel MOSFET between SW and GND is enabled until the inductor current reaches the peak current limit. Once current limit is reached, the N-channel MOSFET turns off and the P-channel MOSFET between SW and the driven output is enabled. This switch remains on until the inductor current drops below the valley current limit and the cycle is repeated.

When V_{OUT} reaches the regulation point, the N- and P-channel MOSFETs connected to the SW pin are disabled and the converter enters sleep.

Auxiliary LDO

The integrated LDO provides a regulated 6mA rail to power microcontrollers and external sensors. When the input voltage is above the minimum of 225mV, the LDO is powered from the AUX output allowing the LDO to attain regulation while the main output is still charging. The LDO has a 12mA current limit and an internal 1ms soft-start to eliminate inrush currents. The LDO output voltage is set by the FBLDO pin. If a resistor divider is connected to this pin, the ratio of the resistors determines the LDO output voltage. If the FBLDO pin is connected directly to GND, the LDO will use a 2MΩ internal divider network to program a 2.2V nominal output voltage. The LDO should be programmed for an output voltage less than the programmed V_{OUT}.

OPERATION

When the converter is placed in shutdown mode, the LDO is forced into reverse-blocking mode with reverse current limited to under 1µA. After the shutdown event has ended, the LDO remains in reverse-blocking mode until V_{AUX} has risen above the LDO voltage.

MPPC Operation

The maximum power point control circuit allows the user to set the optimal input voltage operating point for a given power source. The MPPC circuit dynamically regulates the average inductor current to prevent the input voltage from dropping below the MPPC threshold. When V_{IN} is greater than the MPPC voltage, the inductor current is increased until V_{IN} is pulled down to the MPPC set point. If V_{IN} is less than the MPPC voltage, the inductor current is reduced until V_{IN} rises to the MPPC set point.

Automatic Power Adjust

The LTC3105 incorporates a feature that maximizes efficiency at light load while providing increased power capability at heavy load by adjusting the peak and valley of the inductor current as a function of load. Lowering the peak inductor current to 100mA at light load optimizes efficiency by reducing conduction losses. As the load increases, the peak inductor current is automatically increased to a maximum of 500mA. At intermediate loads, the peak inductor current can vary between 100mA to 500mA. This function is overridden by the MPPC function and will only be observed when the power source can deliver more power than the load requires.

PGOOD Operation

The power good output is used to indicate that V_{OUT} is in regulation. PGOOD is an open-drain output, and is disabled in shutdown. PGOOD will indicate that power is good at the beginning of the first sleep event after the output voltage has risen above 90% of its regulation value. PGOOD remains asserted until V_{OUT} drops below 90% of its regulation value at which point PGOOD will pull low.

APPLICATIONS INFORMATION

Component Selection

Low DCR power inductors with values between 4.7µH and 30µH are suitable for use with the LTC3105. For most applications, a 10µH inductor is recommended. In applications where the input voltage is very low, a larger value inductor can provide higher efficiency and a lower start-up voltage. In applications where the input voltage is relatively high (V_{IN} > 0.8V), smaller inductors may be used to provide a smaller overall footprint. In all cases, the inductor must have low DCR and sufficient saturation current rating. If the DC resistance of the inductor is too high, efficiency will be reduced and the minimum operating voltage will increase.

Input capacitor selection is highly important in low voltage, high source resistance systems. For general applications, a 10µF ceramic capacitor is recommended between V_{IN} and GND. For high impedance sources, the input capacitor should be large enough to allow the converter to complete start-up mode using the energy stored in the input capacitor. When using bulk input capacitors that have high ESR, a small valued parallel ceramic capacitor should be placed between V_{IN} and GND as close to the converter pins as possible.

A 1µF ceramic capacitor should be connected between AUX and GND. Larger capacitors should be avoided to minimize start-up time. A low ESR output capacitor should be connected between V_{OUT} and GND. The main output capacitor should be 10µF or larger. The main output can also be used to charge energy storage devices including tantalum capacitors, supercapacitors and batteries. When using output bulk storage devices with high ESR, a small valued ceramic capacitor should be placed in parallel and located as close to the converter pins as possible.

APPLICATIONS INFORMATION

Step-Up Converter Feedback Configuration

A resistor divider connected between the V_{OUT} and FB pins programs the step-up converter output voltage, as shown in Figure 2. An optional 22pF feedforward capacitor, C_{FF1}, can be used to reduce output ripple and improve load transient response. The equation for V_{OUT} is:

$$V_{OUT} = 1.004V \bullet \left(\frac{R1}{R2} + 1\right)$$

LDO Regulator Feedback Configuration

Two methods can be used to program the LDO output voltage, as shown in Figure 3. A resistor divider connected between the LDO and FBLDO pins can be used to program the LDO output voltage. The equation for the LDO output voltage is:

$$V_{LDO} = 1.004V \bullet \left(\frac{R3}{R4} + 1\right)$$

Alternatively, the FBLDO pin can be connected directly to GND. In this configuration, the LDO is internally set to a nominal 2.2V output.

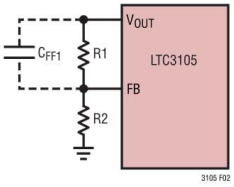


Figure 2. FB Configuration

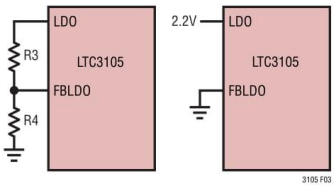


Figure 3. FBLDO Configuration

MPPC Threshold Configuration

The MPPC circuit controls the inductor current to maintain V_{IN} at the voltage on the MPPC pin. The MPPC pin voltage is set by connecting a resistor between the MPPC pin and GND, as shown in Figure 4. The MPPC voltage is determined by the equation:

$$V_{MPPC} = 10\mu A \bullet R_{MPPC}$$

In photovoltaic cell applications, a diode can be used to set the MPPC threshold so that it tracks the cell voltage over temperature, as shown in Figure 5. The diode should be thermally coupled to the photovoltaic cell to ensure proper tracking. A resistor placed in series with the diode can be used to adjust the DC set point to better match the maximum power point of a particular source if the selected diode forward voltage is too low. If the diode is located far from the converter inputs, a capacitor may be required to filter noise that may couple onto the MPPC pin, as shown in Figure 5. This method can be extended to stacked cell sources through use of multiple series connected diodes.

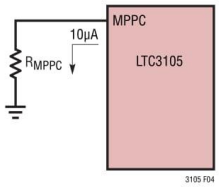


Figure 4. MPPC Configuration

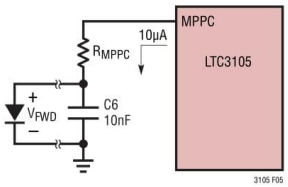


Figure 5. MPPC Configuration with Temperature Adjustment

APPLICATIONS INFORMATION

Industrial Current Loops

The low 250mV start-up and low voltage operation of the LTC3105 allow it to be supplied by power from a diode placed in an industrial sensor current loop, as shown in Figure 6. In this application, a large input capacitor is required due to the very low available supply current (less than 4mA). The loop diode should be selected for a minimum forward drop of 300mV. The MPPC pin voltage should be set for a value approximately 50mV below the minimum diode forward voltage.

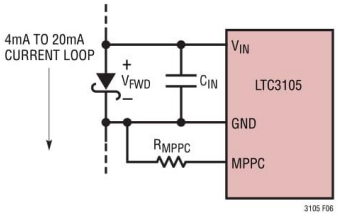
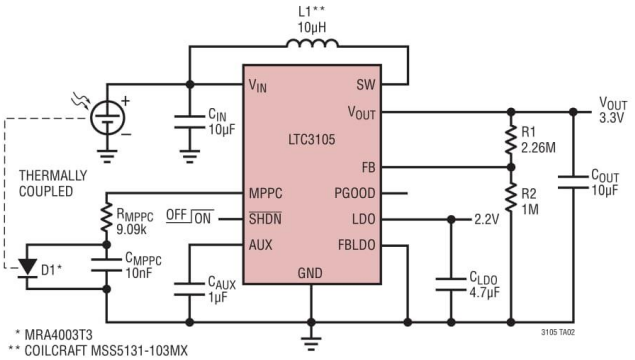


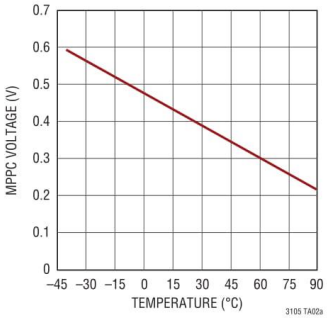
Figure 6. Current Loop Power Tap

TYPICAL APPLICATIONS

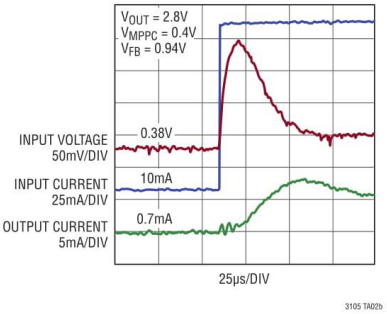
3.3V from a Single-Cell Photovoltaic Source with Temperature Tracking



V_{MPPC} vs Temperature

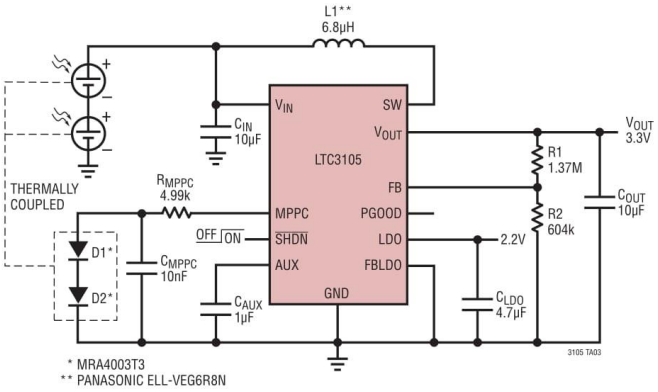


MPPC Response to Input Source Current Step



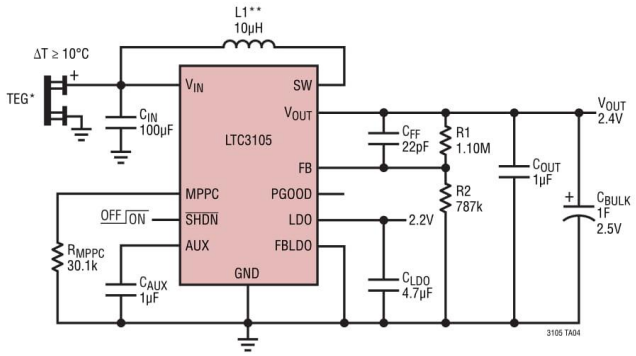
TYPICAL APPLICATIONS

3.3V from Multiple Stacked-Cell Photovoltaic with Source Temperature Tracking



* MRA4003T3
** PANASONIC ELL-VEG6R8N

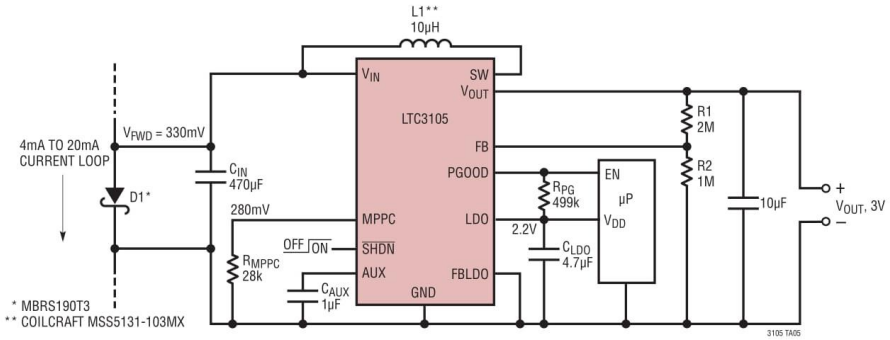
Thermoelectric Generator to 2.4V Super Capacitor Charger



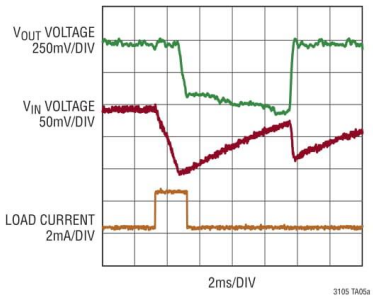
* MICROPELT MPG-D751
** COILCRAFT MSS5131-103MX

TYPICAL APPLICATIONS

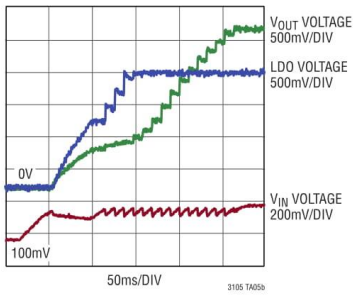
Industrial Sensor 4mA to 20mA Current Loop Power Tap



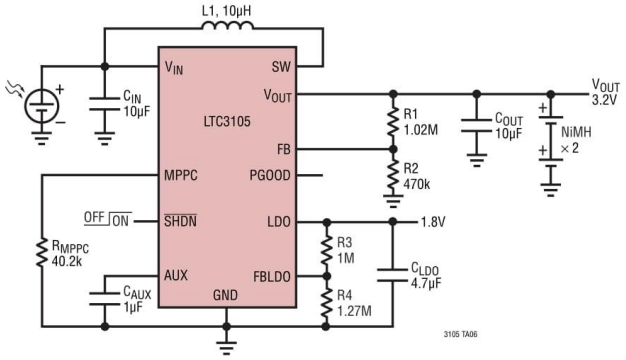
Transient Response to Load Pulse with 4mA Loop Current



Start-Up V_{IN}, V_{OUT}, V_{LDO}



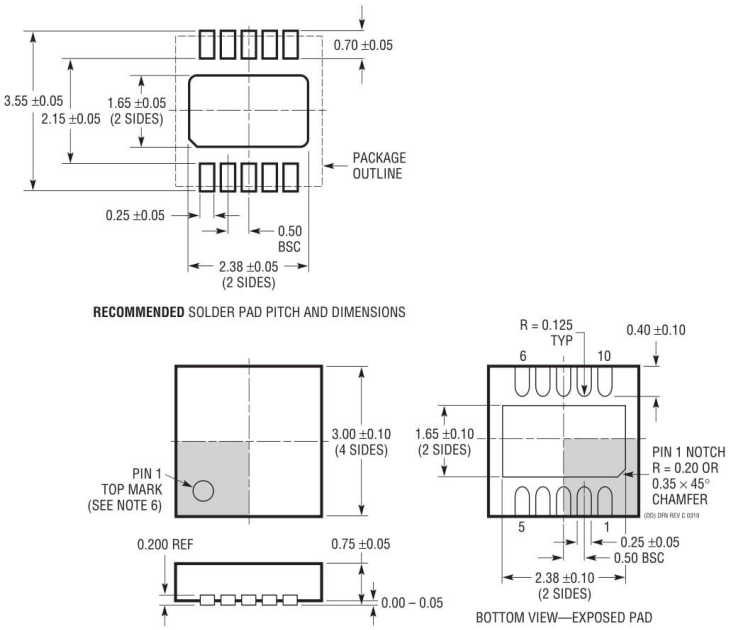
Single-Cell Photovoltaic NiMH Trickle Charger



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3105#packaging for the most recent package drawings.

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)

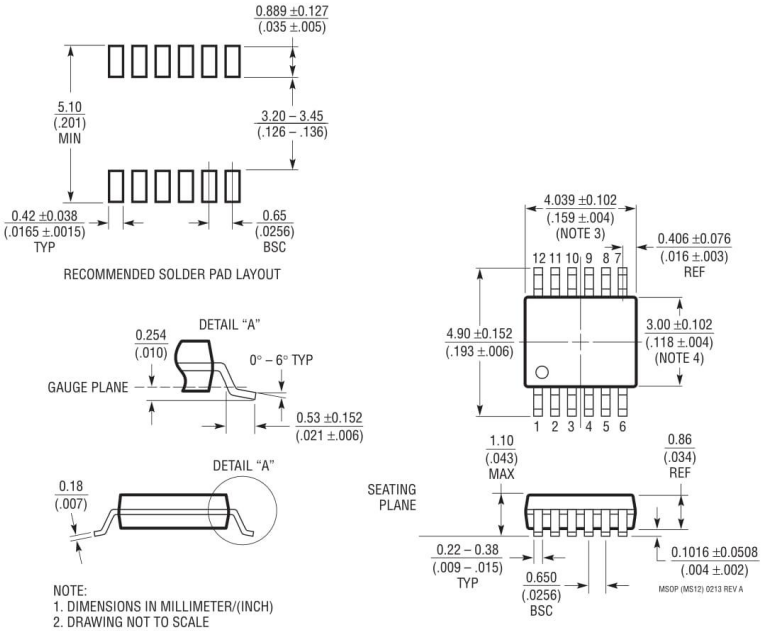


NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3105#packaging for the most recent package drawings.

MS Package
12-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1668 Rev A)



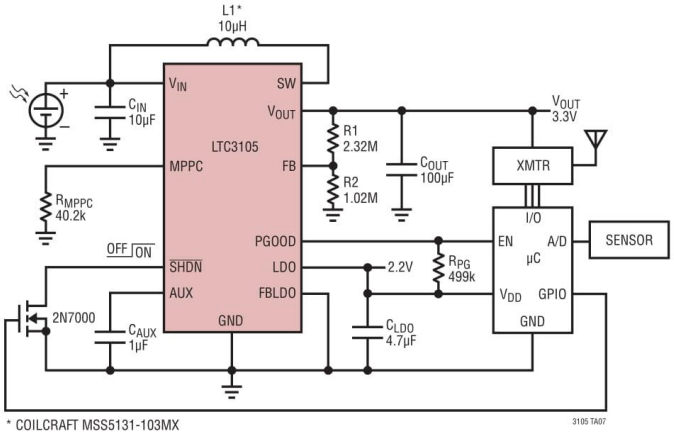
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	01/11	Added (Note 5) notation to Input Start-Up Voltage conditions.	3
		Added Note 5.	3
		Updated Start-Up Mode Operation section.	8
B	11/15	V_{OUT} range changed.	3
		Changed G09 curve.	4
		Changed feedback description.	6
		Changed V_{OUT} range.	7

TYPICAL APPLICATION

Single-Cell Powered Remote Wireless Sensor



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3106	300mA Low Voltage Buck-Boost Converter with PowerPath™ and 1.6µA Quiescent Current	300mV ≤ V_{IN} ≤ 5.1V; Selectable Output Voltages Primary or Rechargeable Backup Batteries, MPPC, 3mm × 4mm QFN-20, TSSOP-20E Packages, Solar and TEG
LTC3330	Dual Input Nanopower Buck-Boost DC/DC with Energy Harvesting Battery Life Extender, Input Prioritizer and Up to 50mA of I_{OUT}	3V ≤ V_{IN} ≤ 19V for EH; 1.8V ≤ V_{IN} ≤ 5V for Battery Full-Wave Bridge Rectifier, Super Cap Balancer 5mm × 5mm QFN-32, Solar and Vibration
LTC3331	Dual Input Nanopower Buck-Boost DC/DC with Energy Harvesting 10mA Shunt Battery Charger Input Prioritizer and Up to 50mA of I_{OUT}	3V ≤ V_{IN} ≤ 19V for EH; 1.8V ≤ V_{IN} ≤ 4.2V for Battery Full-Wave Bridge Rectifier, Super Cap Balancer Programmable Float Voltages, 5mm × 5mm QFN-32, Solar and Vibration
LTC3109	Auto-Polarity, Ultralow Voltage Step-Up Converter and Power Manager	±0.03V ≤ V_{IN} ≤ ±0.50V, Selectable V_{OUT} of 2.35V, 3.3V, 4.1V or 5V Uses Compact Step-Up Transformers, I_Q = 7µA; 4mm × 4mm QFN-20 SSOP-20 Packages, TEG and Thermopiles
LTC3108/ LTC3108-1	Ultralow Voltage Step-Up Converter and Power Manager	0.03V ≤ V_{IN} ≤ 0.50V, Selectable V_{OUT} of 2.5V, 3V, 3.7V or 4.5V Uses Compact Step-Up Transformers, I_Q = 7µA; 3mm × 4mm DFN-12 SSOP-16 Packages, TEG and Thermopiles
LTC4070	Li-Ion/Polymer Shunt Battery Charger System	450nA I_Q; 1% Float Voltage Accuracy; 50mA Shunt Current 4.0V/4.1V/4.2V, DFN-8 and MSOP-8E Packages
LTC4071	Li-Ion/Polymer Shunt Battery Charger System with Low Battery Disconnect	550nA I_Q; 1% Float Voltage Accuracy; <10nA Low Battery Disconnect; 4.0V/4.1V/4.2V; 8-Lead 2mm × 3mm DFN and MSOP Packages
LTC3588-1/ LTC3588-2	Piezoelectric Energy Harvesting Power Supply	< 1µA I_Q in Regulation; 2.7V to 20V Input Range; Integrated Bridge Rectifier. MSOP-10E and 3mm × 3mm DFN-10 Packages

18 Linear Technology Corporation
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TEXAS INSTRUMENTS

bq25504

SLUSAH0C – OCTOBER 2011 – REVISED JUNE 2015

bq25504 Ultra Low-Power Boost Converter With Battery Management for Energy Harvester Applications

1 Features

- Ultra Low-Power With High-Efficiency DC-DC Boost Converter/Charger
  - Continuous Energy Harvesting From Low-Input Sources: V_{IN} ≥ 80 mV (Typical)
  - Ultra-Low Quiescent Current: I_Q < 330 nA (Typical)
  - Cold-Start Voltage: V_{IN} ≥ 330 mV (Typical)
- Programmable Dynamic Maximum Power Point Tracking (MPPT)
  - Integrated Dynamic Maximum Power Point Tracking for Optimal Energy Extraction From a Variety of Energy Generation Sources
  - Input Voltage Regulation Prevents Collapsing Input Source
- Energy Storage
  - Energy Can be Stored to Rechargeable Li-ion Batteries, Thin-film Batteries, Super-Capacitors, or Conventional Capacitors
- Battery Charging and Protection
  - User Programmable Undervoltage and Overvoltage Levels
  - On-Chip Temperature Sensor With Programmable Overtemperature Shutoff
- Battery Status Output
  - Battery Good Output Pin
  - Programmable Threshold and Hysteresis
  - Warn Attached Microcontrollers of Pending Loss of Power
  - Can be Used to Enable or Disable System Loads

2 Applications

- Energy Harvesting
- Solar Chargers
- Thermal Electric Generator (TEG) Harvesting
- Wireless Sensor Networks (WSNs)
- Industrial Monitoring
- Environmental Monitoring
- Bridge and Structural Health Monitoring (SHM)
- Smart Building Controls
- Portable and Wearable Health Devices
- Entertainment System Remote Controls

3 Description

The bq25504 device is the first of a new family of intelligent integrated energy harvesting nano-power management solutions that are well suited for meeting the special needs of ultra low power applications. The device is specifically designed to efficiently acquire and manage the microwatts (µW) to miliwatts (mW) of power generated from a variety of DC sources like photovoltaic (solar) or thermal electric generators. The bq25504 is the first device of its kind to implement a highly efficient boost converter/charger targeted toward products and systems, such as wireless sensor networks (WSNs) which have stringent power and operational demands. The design of the bq25504 starts with a DC-DC boost converter/charger that requires only microwatts of power to begin operating.

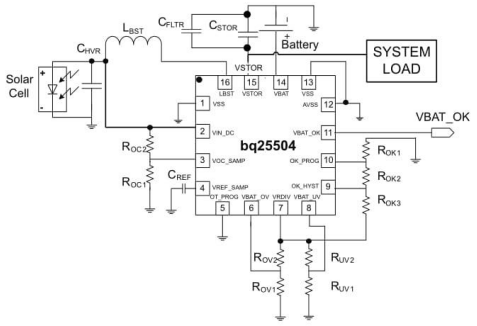
Once started, the boost converter/charger can effectively extract power from low-voltage output harvesters such as thermoelectric generators (TEGs) or single- or dual-cell solar panels. The boost converter can be started with V_{IN} as low as 330 mV, and once started, can continue to harvest energy down to V_{IN} = 80 mV.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq25504	VQFN (16)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Solar Application Circuit



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4 Revision History

Changes from Revision B (December 2014) to Revision C — **Page**

- Changed the Test Condition for $P_{IN(CS)}$ in the *Electrical Characteristics* ... 6
- Changed the values for $P_{IN(CS)}$ in the *Electrical Characteristics* From: TYP = 10, MAX = 50 To: TYP = 15, MAX deleted ... 6
- Changed C_{FLTR} To: C_{BYP} Figure 14 ... 18
- Changed CBYP = 0.1 µF To: CBYP = 0.01 µF in *Detailed Design Procedure* ... 18
- Changed C_{FLTR} To: C_{BYP} in Figure 21 ... 21
- Changed CBYP = 0.1 µF To: CBYP = 0.01 µF in *Detailed Design Procedure* ... 21
- Changed C_{FLTR} To: C_{BYP} in Figure 28 ... 23
- Changed CBYP = 0.1 µF To: CBYP = 0.01 µF in *Detailed Design Procedure* ... 23
- Changed Figure 34 ... 26

Changes from Revision A (September 2012) to Revision B — **Page**

- Added *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Original (October 2011) to Revision A — **Page**

- Added the INTENDED OPERATION section ... 9
- Changed the Cold -Start Operation section ... 13
- Changed the Boost Converter, Charger Operation section ... 14
- Changed the Storage Element section ... 14
- Changed the CAPACITOR SELECTION section ... 17
- Added C_{FLTR} and Notes 1 and 2 to Figure 14 ... 18
- Added C_{FLTR} and Notes 1 and 2 to Figure 21 ... 21
- Added C_{FLTR} and Notes 1 and 2 to Figure 28 ... 23

5 Description (Continued)

The bq25504 also implements a programmable maximum power point tracking sampling network to optimize the transfer of power into the device. Sampling the VIN_DC open-circuit voltage is programmed using external resistors, and held with an external capacitor (C_{REF}).

For example solar cells that operate at maximum power point (MPP) of 80% of their open-circuit voltage, the resistor divider can be set to 80% of the VIN_DC voltage and the network will control the VIN_DC to operate near that sampled reference voltage. Alternatively, an external reference voltage can be provide by a MCU to produce a more complex MPPT algorithm.

The bq25504 was designed with the flexibility to support a variety of energy storage elements. The availability of the sources from which harvesters extract their energy can often be sporadic or time-varying. Systems will typically need some type of energy storage element, such as a rechargeable battery, super capacitor, or conventional capacitor. The storage element ensures that constant power is available when needed for the systems. The storage element also allows the system to handle any peak currents that cannot directly come from the input source.

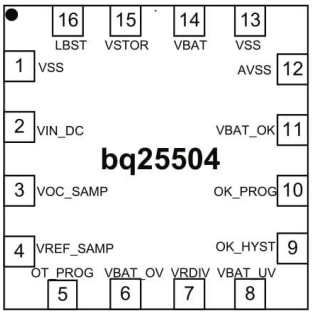
To prevent damage to a customer's storage element, both maximum and minimum voltages are monitored against the user programmed undervoltage (UV) and overvoltage (OV) levels.

To further assist users in the strict management of their energy budgets, the bq25504 toggles the battery good flag to signal an attached microprocessor when the voltage on an energy storage battery or capacitor has dropped below a preset critical level. This warning should trigger the shedding of load currents to prevent the system from entering an undervoltage condition. The OV, UV, and battery good thresholds are programmed independently.

All the capabilities of bq25504 are packed into a small-footprint, 16-lead, 3-mm x 3-mm VQFN package.

6 Pin Configuration and Functions

RGT Package
16 Pins
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AVSS	12	Supply	Signal ground connection for the device
LBST	16	Input	Inductor connection for the boost charger switching node. Connect a 22 µH inductor between this pin and pin 2 (VIN_DC).
OK_HYST	9	Input	Connect to the mid-point of external resistor divider between VRDIV and GND for setting the VBAT_OK hysteresis threshold. If not used, connect this pin to GND.
OK_PROG	10	Input	Connect to the mid-point of external resistor divider between VRDIV and GND for setting the VBAT_OK threshold. If not used, connect this pin to GND.
OT_PROG	5	Input	Digital Programming input for IC overtemperature threshold. Connect to GND for 60 C threshold or VSTOR for 120 C threshold.
VBAT	14	I/O	Connect a rechargeable storage element with at least 100 uF of equivalent capacitance to this pin.
VBAT_OK	11	Output	Digital output for battery good indicator. Internally referenced to the VSTOR voltage. Leave floating if not used.
VBAT_OV	6	Input	Connect to the mid-point of external resistor divider between VRDIV and GND for setting the VSTOR = VBAT overvoltage threshold.
VBAT_UV	8	Input	Connect to the mid-point of external resistor divider between VRDIV and GND for setting the VBAT undervoltage threshold. The PFET between VBAT and VSTOR opens if the voltage on VSTOR is below this threshold.
VIN_DC	2	Input	DC voltage input from energy harvesters. Connect at least a 4.7 µF capacitor as close as possible between this pin and pin 1.
VOC_SAMP	3	Input	Sampling pin for MPPT network. Connect to the mid-point of external resistor divider between VIN_DC and GND for setting the MPP threshold voltage which will be stored on the VREF_SAMP pin. To disable the MPPT sampling circuit, connect to VSTOR.
VRDIV	7	Output	Resistor divider biasing voltage.
VREF_SAMP	4	Input	Connect a 0.01 µF low leakage capacitor from this pin to GND to store the voltage to which VIN_DC will be regulated. This voltage is provided by the MPPT sample circuit. When MPPT is disabled, either use an external voltage source to provide this voltage or tie this pin to GND to disable input voltage regulation (i.e. operate from a low impedance power supply).
VSS	1	Input	General ground connection for the device
VSS	13	Supply	General ground connection for the device
VSTOR	15	Output	Connection for the output of the boost charger, which is typically connected to the system load. Connect at least a 4.7 µF capacitor in parallel with a 0.1 µF capacitor as close as possible to between this pin and pin 1 (VSS).

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VIN_DC, VOC_SAMP, VREF_SAMP, VBAT_OV, VBAT_UV, VRDIV, OK_HYST, OK_PROG, VBAT_OK, VBAT, VSTOR, LBST(2)	–0.3	5.5	V
Peak Input Power, P_{IN_PK}			400	mW
Operating junction temperature range, T_J		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}/ground terminal.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)		2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)		500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
$V_{IN\ (DC)}$	DC input voltage into VIN_DC(1)	0.13		3	V
VBAT	Battery voltage range(2)	2.5		5.25	V
C_{HVR}	Input capacitance	4.23	4.7	5.17	µF
C_{STOR}	Storage capacitance	4.23	4.7	5.17	µF
C_{BAT}	Battery pin capacitance or equivalent battery capacity	100			µF
C_{REF}	Sampled reference storage capacitance	9	10	11	nF
$R_{OC1} + R_{OC2}$	Total resistance for setting for MPPT reference.	18	20	22	MΩ
$R_{OK}1 + R_{OK}2 + R_{OK3}$	Total resistance for setting reference voltage.	9	10	11	MΩ
$R_{UV1} + R_{UV2}$	Total resistance for setting reference voltage.	9	10	11	MΩ
$R_{OV1} + R_{OV2}$	Total resistance for setting reference voltage.	9	10	11	MΩ
L_{BST}	Input inductance	19.8	22	24.2	µH
T_A	Operating free air ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		105	°C

(1) Maximum input power ≤ 300 mW. Cold start has been completed
(2) VBAT_OV setting must be higher than VIN_DC

7.4 Thermal Information

THERMAL METRIC(1)		bq25504 QFN 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	22	
ψ_{JT}	Junction-to-top characterization parameter	1.8	
ψ_{JB}	Junction-to-board characterization parameter	22	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

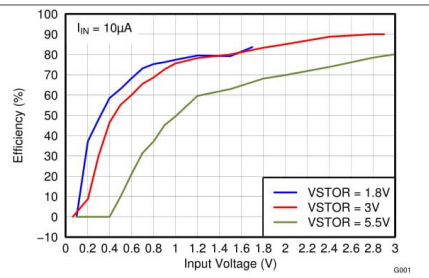
7.5 Electrical Characteristics

Over recommended temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for conditions of VIN_DC = 1.2V, VBAT = VSTOR = 3V. External components L_{BST} = 22 µH, C_{HVR} = 4.7 µF C_{STOR}= 4.7 µF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BOOST CONVERTER \ CHARGER STAGE						
$V_{IN(DC)}$	DC input voltage into VIN_DC	Cold-start completed	130		3000	mV
$I_{IN(DC)}$	Peak Current flowing from V_{IN} into VIN_DC input	0.5V < V_{IN} < 3 V; VSTOR = 4.2 V		200	300	mA
P_{IN}	Input power range for normal charging	VBAT > VIN_DC; VIN_DC = 0.5 V	0.01		300	mW
$V_{IN(CS)}$	Cold-start Voltage. Input voltage that will start charging of VSTOR	VBAT < VBAT_UV; VSTOR = 0 V; 0°C < T_A < 85°C		330	450	mV
$P_{IN(CS)}$	Minimum cold-start input power to start normal charging	VBAT < $VSTOR_{(CHGEN)}$ VIN_DC clamped to VIN_CS by cold start circuit VBAT = 100 µF ceramic		15		µW
V_{STOR_CHGEN}	Voltage on VSTOR when cold start operation ends and normal charger operation begins		1.6	1.77	1.95	V
$R_{BAT(on)}$	Resistance of switch between VBAT and VSTOR when turned on.	VBAT = 4.2 V; VSTOR load = 50 mA			2	Ω
$R_{DS(on)}$	Charger Low Side switch ON resistance	VBAT = 2.1 V			2	Ω
		VBAT = 4.2 V			2	
	Charger rectifier High Side switch ON resistance	VBAT = 2.1 V			5	Ω
		VBAT = 4.2 V			5	
f_{SW_BST}	Boost converter mode switching frequency				1	MHz
BATTERY MANAGEMENT						
I_{VBAT}	Leakage on VBAT pin	VBAT = 2.1 V; VBAT_UV = 2.3 V, T_J = 25°C VSTOR = 0 V		1	5	nA
		VBAT = 2.1 V; VBAT_UV = 2.3 V, –40°C < T_J < 65°C, VSTOR = 0 V			80	nA
I_{VSTOR}	VSTOR Quiescent current Charger Shutdown in UV Condition	VIN_DC = 0V; VBAT < VBAT_UV = 2.4V; VSTOR = 2.2V, No load on VBAT		330	750	nA
	VSTOR Quiescent current Charger Shutdown in OV Condition	VIN_DC = 0V, VBAT > VBAT_OV, VSTOR = 4.25, No load on VBAT		570	1400	nA
V_{BAT_OV}	Programmable voltage range for overvoltage threshold (Battery voltage is rising)	VSTOR increasing	2.5		5.25	V
$V_{BAT\_OV\_HYST}$	Battery voltage overvoltage hysteresis threshold (Battery voltage is falling), internal threshold	VSTOR decreasing	18	35	89	mV
V_{BAT_UV}	Programmable voltage range for under voltage threshold (Battery voltage is falling)	VSTOR decreasing; VBAT_UV > V_{Bias}	2.2		VBAT_OV	V
$V_{BAT\_UV\_HYST}$	Battery under voltage threshold hysteresis, internal thershold	VSTOR increasing	40	80	125	mV
V_{BAT_OK}	Programmable voltage range for threshold voltage for high to low transition of digital signal indicating battery is OK,	VSTOR decreasing	VBAT_UV		VBAT_OV	V
$V_{BAT\_OK\_HYST}$	Programmable voltage range for threshold voltage for low to high transition of digital signal indicating battery is OK,	VSTOR increasing	50		VBAT_OV-VBAT_UV	mV
$V_{BAT\_ACCURACY}$	Overall Accuracy for threshold values, UV, OV, VBAT_OK	Selected resistors are 0.1% tolerance	–5%		5%	
V_{BAT_OKH}	VBAT OK (High) threshold voltage	Load = 10 µA			VSTOR-200mV	V
V_{BAT_OKL}	VBAT OK (Low) threshold voltage	Load = 10 µA			100	mV
TSD_PROTL	The temperature at which the boost converter is disabled and the switch between VBAT and VSTOR is disconnected to protect the battery	OT_Prog = LO		65		°C
TSD_PROTH		OT_Prog = HI		120		
OT_Prog	Voltage for OT_PROG High setting		2			V
	Voltage for OT_PROG Low setting				0.3	V
BIAS and MPPT CONTROL STAGE						
VOC_sample	Sampling period of VIN_DC open circuit voltage			16		s
VOC_Settling	Sampling period of VIN_DC open circuit voltage			256		ms
VIN_Reg	Regulation of VIN_DC during charging	0.5 V <V_{IN} < 3 V; I_{IN} (DC) = 10 mA	–10%		10%	
VIN_shutoff	DC input voltage into VIN_DC when charger is turned off		40	80	130	mV
MPPT_Disable	Threshold on VOC_SAMP to disable MPPT functionality		VSTOR-15 mV			V
VBIAS	Voltage node which is used as reference for the programmable voltage thresholds	VIN_DC ≥ 0.5V; VSTOR ≥ 1.8 V	1.21	1.25	1.27	V

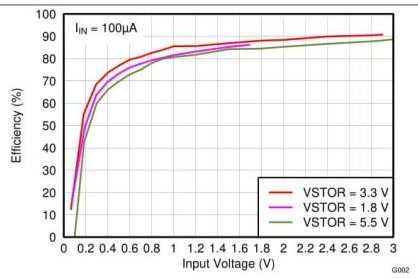
7.6 Typical Characteristics

VSTOR = Keithley Sourcemeter configured to measure current & voltage source set to hold the VSTOR voltage = 1.8V, 3.0V or 5.5V; VBAT_OV = 5.5V and measurement taken between MPPT measurements



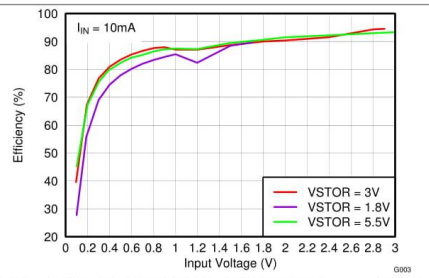
VIN_DC = Keithley Source Meter configured with I_{COMP} = 10 µA and outputting 0 to 3.0 V

Figure 1. Efficiency vs Input Voltage



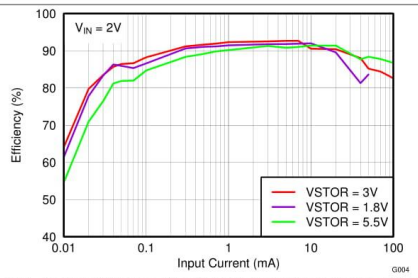
VIN_DC = Keithley Source Meter configured with I_{COMP} = 100 µA and voltage source varied from 0.1 V to 3.0 V

Figure 2. Efficiency vs Input Voltage



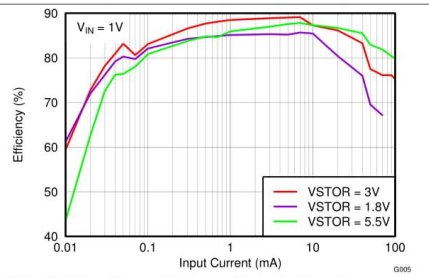
VIN_DC = Keithley Source Meter configured with I_{COMP} = 10 mA and voltage source varied from 0.1 V to 3.0 V

Figure 3. Efficiency vs Input Voltage



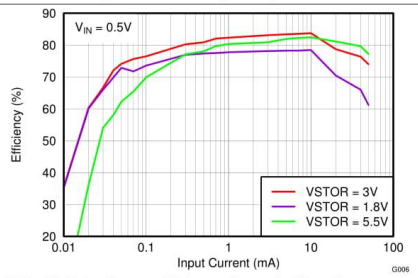
VIN_DC = Keithley Source Meter configured with voltage source = 2.0 V and I_{COMP} varied from 0.01 mA to 100 mA

Figure 4. Efficiency vs Input Current



VIN_DC = Keithley Source Meter configured with voltage source = 1.0 V and I_{COMP} varied from 0.01 mA to 100 mA

Figure 5. Efficiency vs Input Current

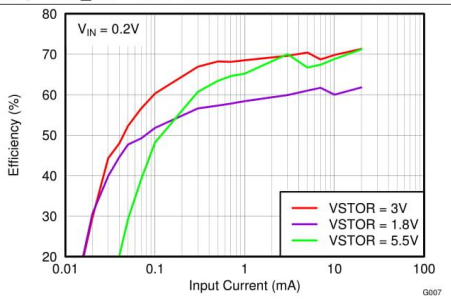


VIN_DC = Keithley Source Meter configured with voltage source = 0.5 V and I_{COMP} varied from 0.01 mA to 100 mA

Figure 6. Efficiency vs Input Current

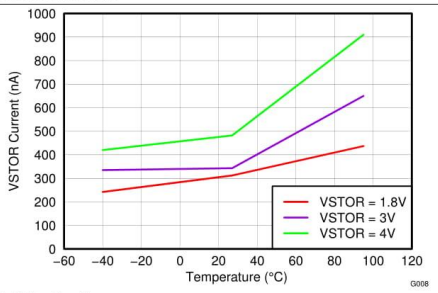
Typical Characteristics (continued)

VSTOR = Keithley Sourcemeter configured to measure current & voltage source set to hold the VSTOR voltage = 1.8V, 3.0V or 5.5V; VBAT_OV = 5.5V and measurement taken between MPPT measurements



VIN_DC = Keithley Source Meter configured with voltage source = 0.2 V and I_{COMP} varied from 0.01 mA to 100 mA
VSTOR = Keithley Source Meter configured to measure current and voltage source set to hold the VSTOR voltage = 2.0 V, 3.0 V or 5.5 V

Figure 7. Efficiency vs Input Current



VIN_DC = floating
VBAT = Keithley Sourcemeter configured to measure current and voltage source varied from 1.8 V, 3 V or 4 V

Figure 8. VSTOR Quiescent Current vs Temperature

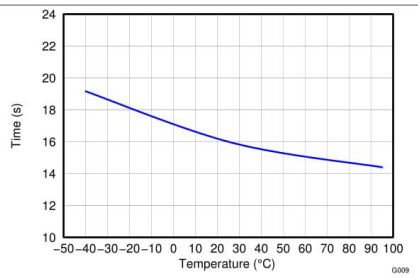


Figure 9. Sample Period vs Temperature

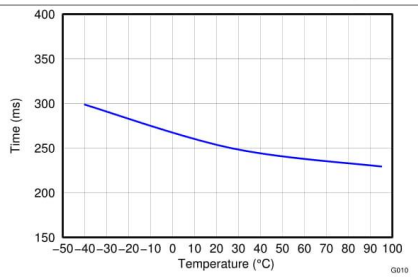


Figure 10. Settling Period vs Temperature

8 Detailed Description

8.1 Overview

The bq25504 is the first of a new family of intelligent integrated energy harvesting Nano-Power management solutions that are well suited for meeting the special needs of ultra low power applications. The product is specifically designed to efficiently acquire and manage the microwatts (µW) to miliwatts (mW) of power generated from a variety of DC sources like photovoltaic (solar) or thermal electric generators (TEGs). The bq25504 is a highly efficient boost charger targeted toward products and systems, such as wireless sensor networks (WSN) which have stringent power and operational demands. The design of the bq25504 starts with a DCDC boost charger that requires only microwatts of power to begin operating.

Once the VSTOR voltage is above VSTOR_CHGEN (1.8V typical), for example, after a partially discharged battery is attached to VBAT, the boost charger can effectively extract power from low voltage output harvesters such as TEGs or single or dual cell solar panels outputing voltages down to VIN(DC) (130mV minimum). When starting from VSTOR=VBAT < 100mV, the cold start circuit needs at least VIN(CS), 330 mV typical, to charge VSTOR up to 1.8V.

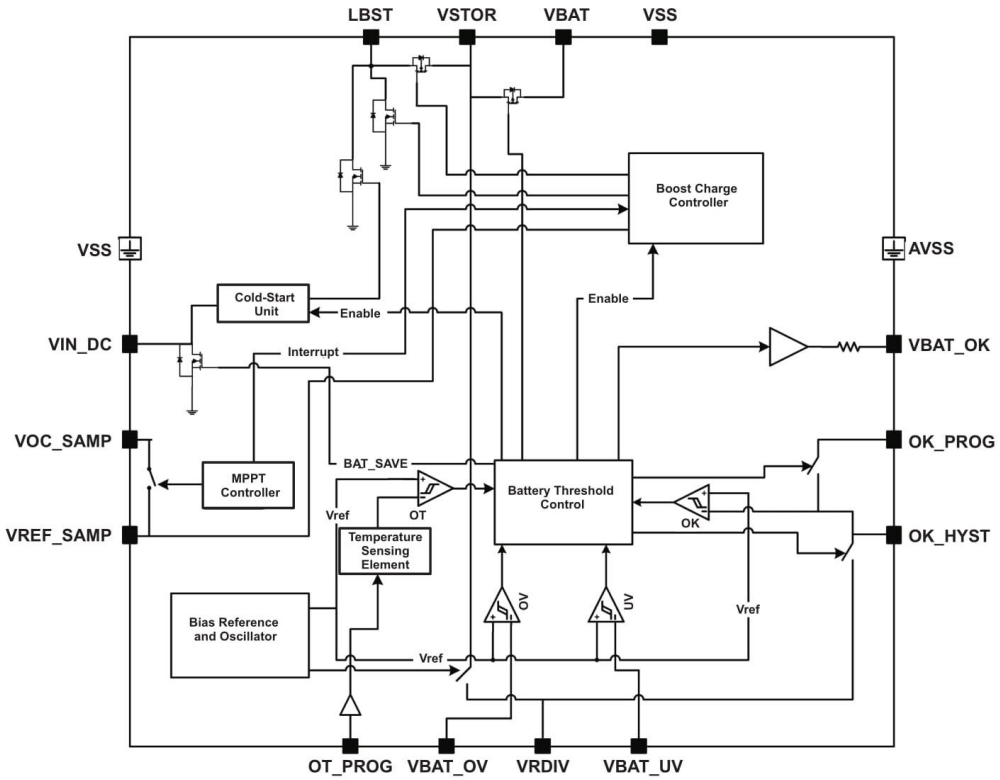
The bq25504 implements a programmable maximum power point tracking (MPPT) sampling network to optimize the transfer of power into the device. Sampling of the VIN_DC open circuit voltage is programmed using external resistors, and that sample voltage is held with an external capacitor connected to the VREF_SAMP pin.

For example solar cells that operate at maximum power point (MPP) of 80% of their open circuit voltage, the resistor divider can be set to 80% of the VIN_DC voltage and the network will control the VIN_DC to operate near that sampled reference voltage. Alternatively, an external reference voltage can be applied directly to the VREF_SAMP pin by a MCU to implement a more complex MPPT algorithm.

The bq25504 was designed with the flexibility to support a variety of energy storage elements. The availability of the sources from which harvesters extract their energy can often be sporadic or time-varying. Systems will typically need some type of energy storage element, such as a re-chargeable battery, super capacitor, or conventional capacitor. The storage element will make certain constant power is available when needed for the systems. The storage element also allows the system to handle any peak currents that can not directly come from the input source. To prevent damage to the storage element, both maximum and minimum voltages are monitored against the user programmable undervoltage (VBAT_UV) and overvoltage (VBAT_OV) levels.

To further assist users in the strict management of their energy budgets, the bq25504 toggles the battery good flag to signal an attached microprocessor when the voltage on an energy storage battery or capacitor has dropped below a pre-set critical level. This should trigger the shedding of load currents to prevent the system from entering an undervoltage condition. The OV and battery good (VBAT_OK) thresholds are programmed independently.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Maximum Power Point Tracking

Maximum power point tracking (MPPT) is implemented in order to maximize the power extracted from an energy harvester source. The boost converter indirectly modulates the input impedance of the main boost charger by regulating the charger's input voltage, as sensed by the VIN_DC pin, to the sampled reference voltage stored on the VREF_SAMP pin. The MPPT circuit obtains a new reference voltage every 16 s (typical) by periodically disabling the charger for 256 ms (typical) and sampling a fraction of the harvester's open-circuit voltage (VOC). For solar harvesters, the maximum power point is typically 70%-80% of VOC and for thermoelectric harvesters, the MPPT is typically 50%. The exact ratio for MPPT can be optimized to meet the needs of the input source being used by connecting external resistors R_{OC1} and R_{OC2} between VIN_DC and GND with mid-point at VOC_SAMP.

$$VREF\_SAMP = VIN\_DC(OpenCircuit)\left(\frac{R_{OC1}}{R_{OC1} + R_{OC2}}\right) \quad (1)$$

Spreadsheet SLUC484 provides help on sizing and selecting the resistors.

Feature Description (continued)

The internal MPPT circuitry and the periodic sampling of VIN_DC can be disabled by tying the VOC_SAMP pin to VSTOR. An external reference voltage can be fed to the VREF_SAMP pin. The boost converter will then regulate VIN_DC to the externally provided reference. If input regulation is not desired (i.e. the input source is a low-impedance output battery or power supply instead of a high impedance output energy harvester), VREF_SAMP can be tied to GND.

8.3.2 Battery Undervoltage Protection

To prevent rechargeable batteries from being deeply discharged and damaged, and to prevent completely depleting charge from a capacitive storage element, the undervoltage (VBAT_UV) threshold must be set using external resistors. The VBAT_UV threshold voltage when the battery voltage is decreasing is given by Equation 2:

$$VBAT\_UV = VBIAS\left(1 + \frac{R_{UV2}}{R_{UV1}}\right) \quad (2)$$

The sum of the resistors is recommended to be no higher than 10 MΩ that is, $R_{UV1} + R_{UV2}$ = 10 MΩ. Spreadsheet SLURAQ1 provides help on sizing and selecting the resistors.

The undervoltage threshold when the battery voltage is increasing is VBAT_UV plus an internal hysteresis voltage denoted by VBAT_UV_HYST. For the VBAT_UV feature to function properly, the load must be connected to the VSTOR pin while the storage element should be connected to the VBAT pin. Once the VSTOR pin voltage goes above VBAT_UV plus VBAT_UV_HYST threshold, the VSTOR pin and the VBAT pins are effectively shorted through an internal PMOS FET. The switch remains closed until the VSTOR pin voltage falls below the VBAT_UV threshold. The VBAT_UV threshold should be considered a fail safe to the system. The system load should be removed or reduced based on the VBAT_OK threshold which should be set above the VBAT_UV threshold.

8.3.3 Battery Overvoltage Protection

To prevent rechargeable batteries from being exposed to excessive charging voltages and to prevent over charging a capacitive storage element, the over-voltage (VBAT_OV) threshold level must be set using external resistors. This is also the voltage value to which the charger will regulate the VSTOR/VBAT pin when the input has sufficient power. The VBAT_OV threshold when the battery voltage is rising is given by Equation 3:

$$VBAT\_OV = \frac{3}{2}VBIAS\left(1 + \frac{R_{OV2}}{R_{OV1}}\right) \quad (3)$$

The sum of the resistors is recommended to be no higher 10 MΩ that is, $R_{OV1} + R_{OV2}$ = 10 MΩ. Spreadsheet SLURAQ1 provides help with sizing and selecting the resistors.

The overvoltage threshold when the battery voltage is decreasing is given by VBAT_OV - VBAT_OV_HYST. Once the voltage at the battery reaches the VBAT_OV threshold, the boost converter is disabled. The charger will start again once the battery voltage drop by VBAT_OV_HYST. When there is excessive input energy, the VBAT pin voltage will ripple between the VBAT_OV and the VBAT_OV - VBAT_OV_HYST levels.

CAUTION

If VIN_DC is higher than VSTOR and VSTOR is higher than VBAT_OV, the input VIN_DC is pulled to ground through a small resistance to stop further charging of the attached battery or capacitor. It is critical that if this case is expected, the impedance of the source attached to VIN_DC be higher than 20 Ω and not a low impedance source.

8.3.4 Battery Voltage in Operating Range (VBAT_OK Output)

The IC allows the user to set a programmable voltage independent of the overvoltage and undervoltage settings to indicate whether the VSTOR voltage (and therefore the VBAT voltage when the PFET between the two pins is turned on) is at an acceptable level. When the battery voltage is decreasing the threshold is set by Equation 4:

Feature Description (continued)

$$VBAT\_OK\_PROG = VBIAS\left(1 + \frac{R_{OK2}}{R_{OK1}}\right) \quad (4)$$

When the battery voltage is increasing, the threshold is set by Equation 5:

$$VBAT\_OK\_HYST = VBIAS\left(1 + \frac{R_{OK2} + R_{OK3}}{R_{OK1}}\right) \quad (5)$$

The sum of the resistors are recommended to be approximately 10 MΩ i.e., R_{OK1} + R_{OK2} + R_{OK3}= 10 MΩ. Spreadsheet SLURAQ1 provides help on sizing and selecting the resistors.

The logic high level of this signal is equal to the VSTOR voltage and the logic low level is ground. The logic high level has ~20 KΩ internally in series to limit the available current to prevent MCU damage until it is fully powered. The VBAT_OK_PROG threshold must be greater than or equal to the UV threshold. Figure 11 shows the relative position of the various threshold voltages.

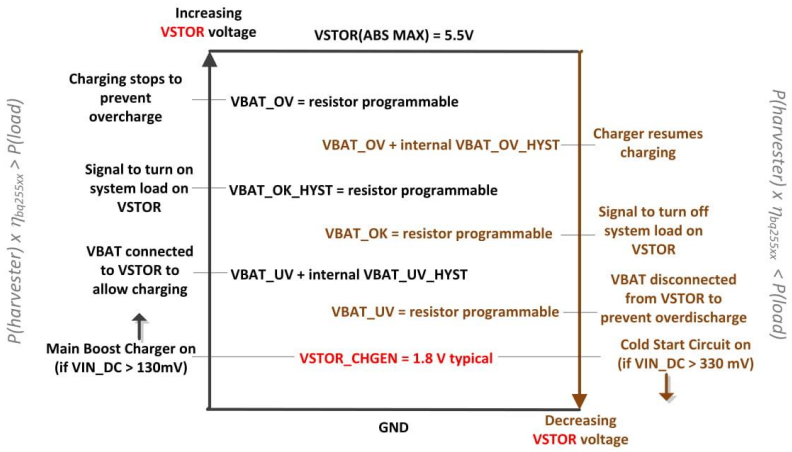


Figure 11. Summary of VSTOR Threshold Voltages

8.3.5 Nano-Power Management and Efficiency

The high efficiency of the bq25504 charger is achieved via the proprietary Nano-Power management circuitry and algorithm. This feature essentially samples and holds the VSTOR voltage in order to reduce the average quiescent current. That is, the internal circuitry is only active for a short period of time and then off for the remaining period of time at the lowest feasible duty cycle. A portion of this feature can be observed in Figure 19 where the VRDIV node is monitored. Here the VRDIV node provides a connection to the VSTOR voltage (first pulse) and then generates the reference levels for the VBAT_OV and VBAT_OK resistor dividers for a short period of time. The divided down values at each pin arecompared against VBIAS as part of the hysteretic control. Since this biases a resistor string, the current through these resistors is only active when the Nano-Power management circuitry makes the connection—hence reducing the overall quiescent current due to the resistors. This process repeats every 64 ms.

The bq25504's boost charger efficiency is shown for various input power levels in Figure 1 through Figure 7. All data points were captured by averaging the overall input current. This must be done due to the periodic biasing scheme implemented via the Nano-Power management circuitry. In order to properly measure the resulting input current when calculating the output to input efficiency, the input current efficiency data was gathered using a source meter set to average over at least 50 samples. Quiescent current curves into VSTOR over temperature and voltage is shown at Figure 8.

8.4 Device Functional Modes

The bq25504 has three functional modes: cold-start operation, main boost charger enabled and thermal shutdown. The cold start circuitry is powered from VIN_DC. The main boost charger circuitry is powered from VSTOR while the boost power stage is powered from VIN_DC. Details of entering and exiting each mode are explained below.

8.4.1 Cold-Start Operation (VSTOR < VSTOR_CHGEN, VIN_DC > VIN(CS) and PIN > PIN(CS))

Whenever VSTOR < VSTOR_CHGEN, VIN_DC ≥ VIN(CS) and PIN > PIN(CS), the cold-start circuit is on. This could happen when there is not input power at VIN_DC to prevent the load from discharging the battery or during a large load transient on VSTOR. During cold start, the voltage at VIN_DC is clamped to VIN(CS) so the energy harvester's output current is critical to providing sufficient cold start input power, PIN(CS) = VIN(CS) X IIN(CS). The cold-start circuit is essentially an unregulated, hysteretic boost converter with lower efficiency compared to the main boost charger. None of the other features function during cold start operation. The cold start circuit's goal is to charge VSTOR higher than VSTOR_CHGEN so that the main boost charger can operate. When a depleted storage element is initially attached to VBAT, as shown in Figure 12 and the harvester can provide a voltage > VIN(CS) and total power at least > PIN(CS), assuming minimal system load or leakage at VSTOR and VBAT, the cold start circuit can charge VSTOR above VSTOR_CHGEN. Once the VSTOR voltage reaches the VSTOR_CHGEN threshold, the IC

1. first performs an initialization pulse on VRDIV to reset the feedback voltages,
2. then disables the charger for 32 ms (typical) to allow the VIN_DC voltage to rise to the harvester's open-circuit voltage which will be used as the input voltage regulation reference voltage until the next MPPT sampling cycle and
3. lastly performs its first feedback sampling using VRDIV, approximately 64 ms after the initialization pulse.

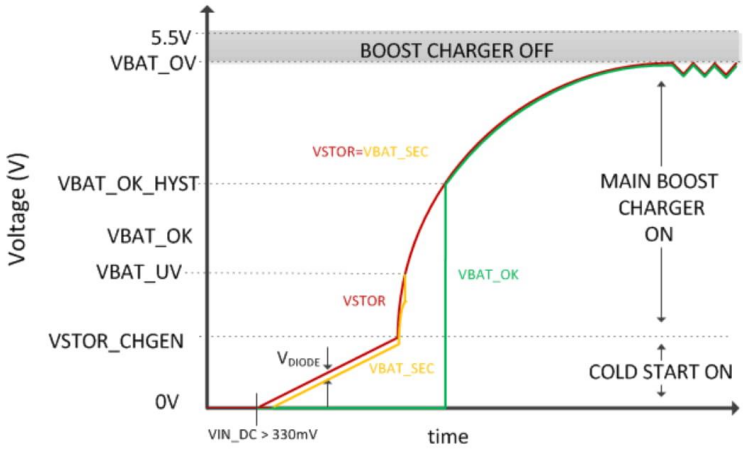


Figure 12. Charger Operation After a Depleted Storage Element is Attached and Harvester is Available

The energy harvester must supply sufficient power for the IC to exit cold start. Due to the body diode of the PFET connecting VSTOR and VBAT, the cold start circuit must charge both the capacitor on CSTOR up to the VSTOR_CHGEN and the storage element connected to VBAT up to VSTOR_CHGEN less a diode drop. When a rechargeable battery with an open protector is attached, the intial charge time is typically short due to the minimum charge needed to close the battery's protector FETs. When large, discharged super capacitors with high DC leakage currents are attached, the intial charge time can be signficant.

Device Functional Modes (continued)

When the VSTOR voltage reaches VSTOR_CHGEN, the main boost charger starts up. When the VSTOR voltage rises to the VBAT_UV threshold, the PMOS switch between VSTOR and VBAT turns on, which provides additional loading on VSTOR and could result in the VSTOR voltage dropping below both the VBAT_UV threshold and the VSTOR_CHGEN voltage, especially if system loads on VSTOR or VBAT are active during this time. Therefore, it is not uncommon for the VSTOR voltage waveform to have incremental pulses (i.e. stair steps) as the IC cycles between cold-start and main boost charger operation before eventually maintaing VSTOR above VSTOR_CHGEN.

The cold start circuit initially clamps VIN_DC to VIN(CS) = 330 mV typical. If sufficient input power (i.e.,output current from the harvester clamped to VIN(CS)) is not available, it is possible that the cold start circuit cannot raise the VSTOR voltage above VSTOR_CHGEN in order for the main boost conveter to start up. It is highly recommended to add an external PFET between the system load and VSTOR. An inverted VBAT_OK signal can be used to drive the gate of this system-isolating, external PFET. See the *Power Supply Recommendations* section for guidance on minimum input power requirements.

8.4.2 Main Boost Charger Enabled (VSTOR > VSTOR_CHGEN, VIN_DC > VIN(DC) and $\overline{EN}$ = LOW)

One way to avoid cold start is to attach a partially charged storage element as shown in Figure 13.

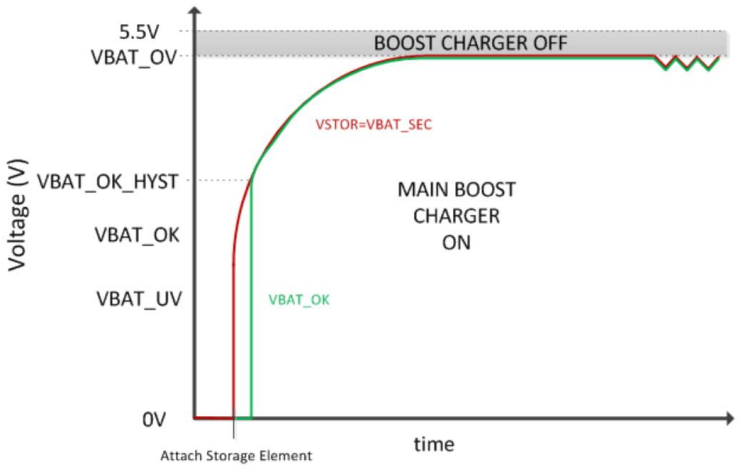


Figure 13. Charger Operation after a Partially Charged Storage Element is Attached and Harvester Power is Available

When no input source is attached, the VSTOR node should be discharged to ground before attaching a storage element. Hot-plugging a storage element that is charged (e.g., the battery protector PFET is closed) and with the VSTOR node more than 100 mV above ground results in the PFET between VSTOR and VBAT remaining off until an input source is attached.

Assuming the voltages on VSTOR and VBAT are both below 100mV, when a charged storage element is attached (i.e. hot-plugged) to VBAT, the IC.

1. first turns on the internal PFET between the VSTOR and VBAT pins for $t_{BAT\_HOT\_PLUG}$ (45ms) in order to charge VSTOR to VSTOR_CHGEN then turns off the PFET to prevent the battery from overdischarge,
2. then performs an initialization pulse on VRDIV to reset the feedback voltages,
3. then disables the charger for 32 ms (typical) to allow the VIN_DC voltage to rise to the harvester's open-circuit voltage which will be used as the input voltage regulation reference voltage until the next MPPT sampling cycle and
4. lastly performs its first feedback sampling using VRDIV, approximately 64 ms after the initialization pulse.

Device Functional Modes (continued)

If the VSTOR pin voltage remains above the internal under voltage threshold (VBAT_UV) for the additional 64 ms after the VRDIV initialization pulse (following the 45-ms PFET on time), the internal PFET turns back on and the main boost charger begins to charge the storage element assuming there is sufficient power available from the harvester at the VIN_DC pin. If VSTOR does not reach the VBAT_UV threshold, then the PFET remains off until the main boost charger can raise the VSTOR voltage to VBAT_UV. If a system load tied to VSTOR discharges VSTOR below VSTOR_GEN or below VBAT_UV during the 32 ms initial MPPT reference voltage measurement or within 110 ms after hot plug, it is recommended to add an external PFET between the system load and VSTOR. An inverted VBAT_OK signal can be used to drive the gate of this system-isolating, external PFET. Otherwise, the VSTOR voltage waveform will have incremental pulses as the IC turns on and off the internal PFET controlled by VBAT_UV or cycles between cold-start and main boost charger operation.

Once VSTOR is above VSTOR_CHGEN, the main boost charger employs pulse frequency modulation (PFM) mode of control to regulate the voltage at VIN_DC close to the desired reference voltage. The reference voltage is set by the MPPT control scheme as described in the features section. Input voltage regulation is obtained by transferring charge from the input to VSTOR only when the input voltage is higher than the voltage on pin VREF_SAMP. The current through the inductor is controlled through internal current sense circuitry. The peak current in the inductor is dithered internally to up to three pre-determined levels in order to maintain high efficiency of the charger across a wide input current range. The charger transfers up to a maximum of 100 mA average input current (230mA typical peak inductor current). The boost charger is disabled when the voltage on VSTOR reaches the user set VBAT_OV threshold to protect the battery connected at VBAT from overcharging. In order for the battery to charge to VBAT_OV, the input power must exceed the power needed for the load on VSTOR. See the *Power Supply Recommendations* section for guidance on minimum input power requirements.

Steady state operation for the boost charger is shown in Figure 16. These plots highlight the inductor current, the VSTOR voltage ripple, input voltage regulation and the LBOOST switching node. The cycle-by-cycle minor switching frequency is a function of the boost converter's inductor value, peak current limit and voltage levels on each side of each inductor. Once the VSTOR capacitor, CSTOR, droops below a minimum value, the hysteretic switching repeats.

CAUTION

If VIN_DC is higher than VSTOR and VSTOR is higher than VBAT_OV, the input VIN_DC is pulled to ground through a small resistance to stop further charging of the attached battery or capacitor. It is critical that if this case is expected, the impedance of the source attached to VIN_DC be higher than 20 Ω and not a low impedance source.

8.4.3 Thermal Shutdown

Rechargeable Li-ion batteries need protection from damage due to operation at elevated temperatures. The application should provide this battery protection and ensure that the ambient temperature is never elevated greater than the expected operational range of 85°C.

The bq25504 uses an integrated temperature sensor to monitor the junction temperature of the device. If the OT_PROG pin is tied low, then the temperature threshold for thermal protection is set to TSD_ProtL which is 65°C typically. If the OT_PROG is tied high, then the temperature is set to TSD_ProtH which is 120°C typically. Once the temperature threshold is exceeded, the boost converter/charger is disabled and charging ceases. Once the temperature of the device drops below this threshold, the boost converter and or charger can resume operation. To avoid unstable operation near the overtemp threshold, a built-in hysteresis of approximately 5°C has been implemented. Care should be taken to not over discharge the battery in this condition since the boost converter/charger is disabled. However, if the supply voltage drops to the VBAT_UV setting, then the switch between VBAT and VSTOR will open and protect the battery even if the device is in thermal shutdown.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Storage Element Selection

In order for the charge management circuitry to protect the storage element from over-charging or discharging, the storage element must be connected to VBAT pin and the system load tied to the VSTOR pin. Many types of elements can be used, such as capacitors, super capacitors or various battery chemistries. A storage element with 100 uF equivalent capacitance is required to filter the pulse currents of the PFM switching charger. The equivalent capacitance of a battery can be computed as computed as:

$$C_{EQ} = 2 \times mAHr_{BAT(CHRGD)} \times 3600\ s/Hr / V_{BAT(CHRGD)} \quad (6)$$

In order for the storage element to be able to charge VSTOR capacitor (CSTOR) within the $t_{VB\_HOT\_PLUG}$ (50 ms typical) window at hot-plug; therefore preventing the IC from entering cold start, the time constant created by the storage element's series resistance (plus the resistance of the internal PFET switch) and equivalent capacitance must be less than $t_{VB\_HOT\_PLUG}$. For example, a battery's resistance can be computed as:

$$R_{BAT} = V_{BAT} / I_{BAT(CONTINUOUS)\ from\ the\ battery\ specifications.} \quad (7)$$

The storage element must be sized large enough to provide all of the system load during periods when the harvester is no longer providing power. The harvester is expected to provide at least enough power to fully charge the storage element while the system is in low power or sleep mode. Assuming no load on VSTOR (i.e., the system is in low power or sleep mode), the following equation estimates charge time from voltage VBAT1 to VBAT2 for given input power is:

Refer to SLUC462 for a design example that sizes the storage element.

$$PIN \times \eta_{EST} \times t_{CHRG} = 1/2 \times CEQ\ X\ (VBAT2^2 - VBAT1^2) \quad (8)$$

Note that if there are large load transients or the storage element has significant impedance then it may be necessary to increase the CSTOR capacitor from the 4.7uF minimum or add additional capacitance to VBAT in order to prevent a droop in the VSTOR voltage. See below for guidance on sizing capacitors.

9.1.2 Inductor Selection

The boost charger needs an appropriately sized inductor for proper operation. The inductor's saturation current should be at least 25% higher than the expected peak inductor currents recommended below if system load transients on VSTOR are expected. Since this device uses hysteretic control, the boost charger is considered naturally stable systems (single order transfer function).

For the boost charger to operate properly, an inductor of appropriate value must be connected between LBOOST, pin 20, and VIN_DC, pin 2. The boost charger internal control circuitry is designed to control the switching behavior with a nominal inductance of 22 µH ± 20%. The inductor must have a peak current capability of > 300 mA with a low series resistance (DCR) to maintain high efficiency.

A list of inductors recommended for this device is shown in Table 1.

Table 1. Recommended Inductors

Inductance (µH)	Dimensions (mm)	Part Number	Manufacturer(1)
22	4.0x4.0x1.7	LPS4018-223M	Coilcraft
22	3.8x3.8x1.65	744031220	Wurth
22	2.8x2.8x2.8	744025220	Wurth

(1) See **WHAT?** concerning recommended third-party products.

9.1.3 Capacitor Selection

In general, all the capacitors need to be low leakage. Any leakage the capacitors have will reduce efficiency, increase the quiescent current and diminish the effectiveness of the IC for energy harvesting.

9.1.3.1 VREF_SAMP Capacitance

The MPPT operation depends on the sampled value of the open circuit voltage and the input regulation follows the voltage stored on the CREF capacitor. This capacitor is sensitive to leakage since the holding period is around 16 seconds. As the capacitor voltage drops due to any leakage, the input regulation voltage also drops preventing proper operation from extraction the maximum power from the input source. Therefore, it is recommended that the capacitor be an X7R or COG low leakage capacitor.

9.1.3.2 VIN_DC Capacitance

Energy from the energy harvester input source is initially stored on a capacitor, CIN, connected to VIN_DC, pin 2, and VSS, pin 1. For energy harvesters which have a source impedance which is dominated by a capacitive behavior, the value of the harvester capacitor should scaled according to the value of the output capacitance of the energy source, but a minimum value of 4.7 µF is recommended.

9.1.3.3 VSTOR Capacitance

Operation of the bq25504 requires two capacitors to be connected between VSTOR, pin 15, and VSS, pin 1. A high frequency bypass capacitor of at 0.1 µF should be placed as close as possible between VSTOR and VSS. In addition, a low ESR capacitor of at least 4.7 µF should be connected in parallel.

9.1.3.4 Additional Capacitance on VSTOR or VBAT

If there are large, fast system load transients and/or the storage element has high resistance, then the CSTOR capacitors may momentarily discharge below the VBAT_UV threshold in response to the transient. This causes the bq25504 to turn off the PFET switch between VSTOR and VBAT and turn on the boost charger. The CSTOR capacitors may further discharge below the VSTOR_CHGEN threshold and cause the bq25504 to enter Cold Start. For instance, some Li-ion batteries or thin-film batteries may not have the current capacity to meet the surge current requirements of an attached low power radio. To prevent VSTOR from drooping, either increasing the CSTOR capacitance or adding additional capacitance in parallel with the storage element is recommended. For example, if boost charger is configured to charge the storage element to 4.2 V and a 500 mA load transient of 50 µs duration infrequently occurs, then, solving I = C x dv/dt for CSTOR gives:

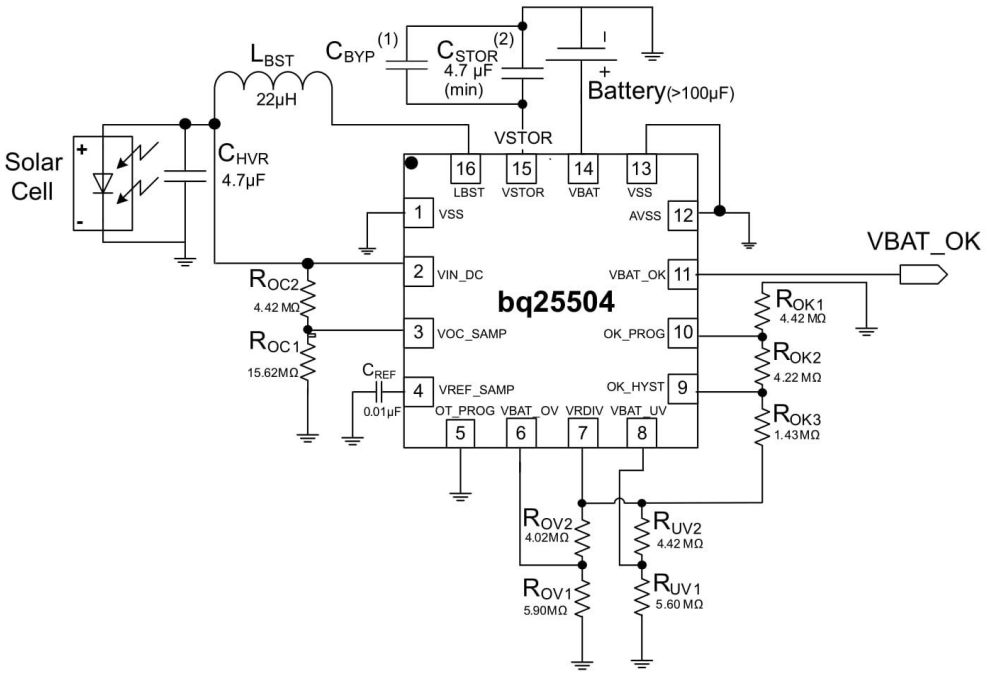
$$\text{CSTOR} \geq \frac{500\ \text{mA} \times 50\ \mu\text{s}}{(4.2\ \text{V} - 1.8\ \text{V})} = 10.5\ \mu\text{F} \tag{9}$$

Note that increasing CSTOR is the recommended solution but will cause the boost charger to operate in the less efficient cold start mode for a longer period at startup compared to using CSTOR = 4.7 µF. If longer cold start run times are not acceptable, then place the additional capacitance in parallel with the storage element.

For a recommended list of standard components, see the EVM User's Guide (SLUUAA8).

9.2 Typical Applications

9.2.1 Solar Application Circuit



(1) Place close as possible to IC pin 15 (VSTOR) and pin 13 (VSS)

(2) See the Capacitor Selection section for guidance on sizing C_{STOR}

Figure 14. Typical Solar Application Circuit

9.2.1.1 Design Requirements

The desired voltage levels are VBAT_OV = 3.15 V, VBAT_UV = 2.20 V, VBAT_OK = 2.44 V, VBAT_OK_HYST = 2.80 V and MPP (V_{OC}) = 78% which is typical for solar panels. There are no large load transients expected. The IC must stop charging if its junction temperature is above 65°C. The simulated solar panel open circuit voltage is 1.0 V.

9.2.1.2 Detailed Design Procedure

The recommended L1 = 22 µH, C_{BYP} = 0.01 µF and low leakage CREF = 10 nF are selected. In order to ensure the fastest recovery of the harvester output voltage to the MPPT level following power extraction, the minimum recommended CIN = 4.7 µF is selected. Because no large system load transients are expected and to ensure fast charge time during cold start, the minimum recommended CSTOR = 4.7 µF. To stop charging when the IC junction temperature is above 65°C, the OT_PROG pin is tied to ground.

- With VBAT_UV < VBAT_OV ≤ 5.5 V, to size the VBAT_OV resistors, first choose $RSUM_{OV} = R_{OV1} + R_{OV2}$ = 10 MΩ then solve Equation 3 for

$$R_{OV1} = \frac{3}{2} \times \frac{RSUM_{OV} \times VBIAS}{VBAT\_OV} \times \frac{3}{2} \frac{10\ M\Omega \times 1.25\ V}{3.15\ V} = 5.95\ M\Omega \rightarrow 5.90\ M\Omega \text{ closest 1\% value then} \quad (10)$$

- $R_{OV2} = RSUM_{OV} - R_{OV1}$ = 10 MΩ - 5.95 MΩ = 4.05 MΩ → 4.02 MΩ resulting in VBAT_OV = 3.15 V

Typical Applications (continued)

- To size the VBAT_UV resistors, first choose $RSUM_{UV} = R_{UV1} + R_{UV2} = 10\ M\Omega$ then solve Equation 2 for

$$R_{UV1} = \frac{RSUM_{UV} \times VBIAS}{VBAT_{UV}} = \frac{10\ M\Omega \times 1.25\ V}{2.2\ V} = 5.68\ M\Omega \rightarrow 5.60\ M\Omega \text{ closest 1\% value then} \quad (11)$$

- $R_{UV2} = RSUM_{UV} - R_{UV1} = 10\ M\Omega - 5.60\ M\Omega = 4.4\ M\Omega \rightarrow 4.42\ M\Omega$ closest 1% resistor resulting in VBAT_UV = 2.2 V.
- With VBAT_OV ≥ VBAT_OK_HYST > VBAT_OK ≥ VBAT_UV, to size the VBAT_OK and VBAT_OK_HYST resistors,
  first choose $RSUM_{OK} = R_{OK1} + R_{OK2} + R_{OK3} = 10\ M\Omega$ then solve Equation 4 and Equation 5 for

$$R_{OK1} = \frac{VBIAS \times RSUM_{OK}}{VBAT\_OK\_HYST} = \left(\frac{1.25\ V}{2.8\ V}\right) \times 10\ M\Omega = 4.46\ M\Omega \rightarrow 4.42\ M\Omega \text{ closest 1\% resistor then} \quad (12)$$

$$R_{OK2} = \left(\frac{VBAT\_OK\_PROG}{VBIAS} - 1\right) \times R_{OK1} = \left(\frac{2.45\ V}{1.25\ V} - 1\right) \times 4.24\ M\Omega = 4.07\ M\Omega, \text{ then} \quad (13)$$

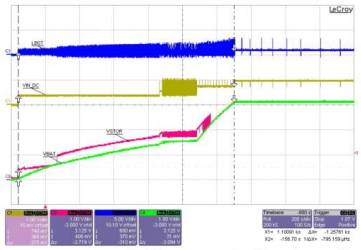
- $R_{OK3} = RSUM_{OK} - R_{OK1} - R_{OK2} = 10\ M\Omega - 4.42\ M\Omega - 4.22\ M\Omega = 1.36\ M\Omega \rightarrow 1.43\ M\Omega$ to give VBAT_OK = 2.44 V and VBAT_OK_HYST = 2.85 V.
- Keeping in mind that VREF_SAMP stores the MPP voltage for the harvester, first choose $RSUM_{OC} = R_{OC1} + R_{OC2} = 20\ M\Omega$ then solve Equation 1 for

$$R_{OC1} = \left(\frac{VREF\_SAMP}{VIN\_DC(OC)}\right) \times RSUM_{OC} = 0.78 \times 20\ M\Omega = 15.6\ M\Omega, \text{ then} \quad (14)$$

$$R_{OC2} = RSUM_{OC} \times \left(1 - \frac{VREF\_SAMP}{VIN\_DC(OC)}\right) = 20\ M\Omega\left(1 - 0.78\right) = 4.4\ M\Omega \text{ closest 1\% resistors} \quad (15)$$

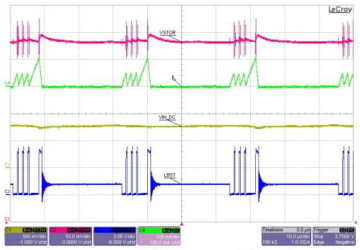
- SLURAQ1 provides help on sizing and selecting the resistors.

9.2.1.3 Application Curves



VINDC = sourcemeter with V_{SOURCE} = 1.0 V and compliance of 2.75 mA
VBAT connected to 0.1 F depleted supercap
No resistance load on VSTOR

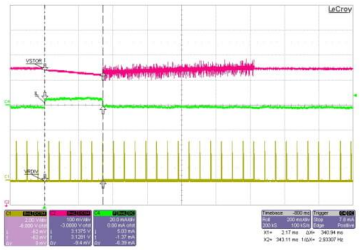
Figure 15. Startup into Depleted Storage Element



VIN_DC = sourcemeter with V_{SOURCE} = 1 V and compliance of 10.5 mA
VBAT = 0.1 F supercap
VSTOR = 2 kΩ resistive load

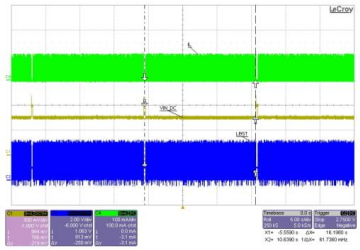
Figure 16. Boost Charger Operational Waveforms

Typical Applications (continued)



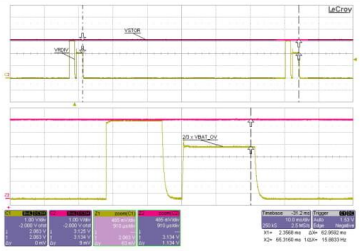
VIN_DC = sourcemeter with V_{SOURCE} = 1 V and compliance of 10.5 mA
VBAT = 0.1 F supercap
VSTOR = open to 500 Ω to open resistive load (IL = load current on VSTOR)

Figure 17. 5 mA Load Transient on VSTOR



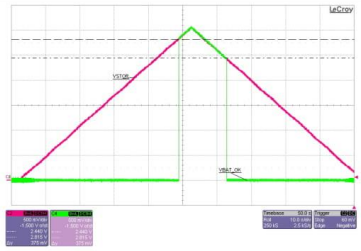
VIN_DC = sourcemeter with V_{SOURCE} = 1 V and compliance of 10.5 mA
VBAT = sourcemeter with V_{SOURCE} = 2.8V and compliance of 1A
IL = inductor current

Figure 18. MPPT Operation



VIN_DC = sourcemeter with V_{SOURCE} = 1 V and compliance of 10.5 mA
VBAT = sourcemeter with V_{SOURCE} = 2.8 V and compliance of 1A

Figure 19. VRDIV Operation

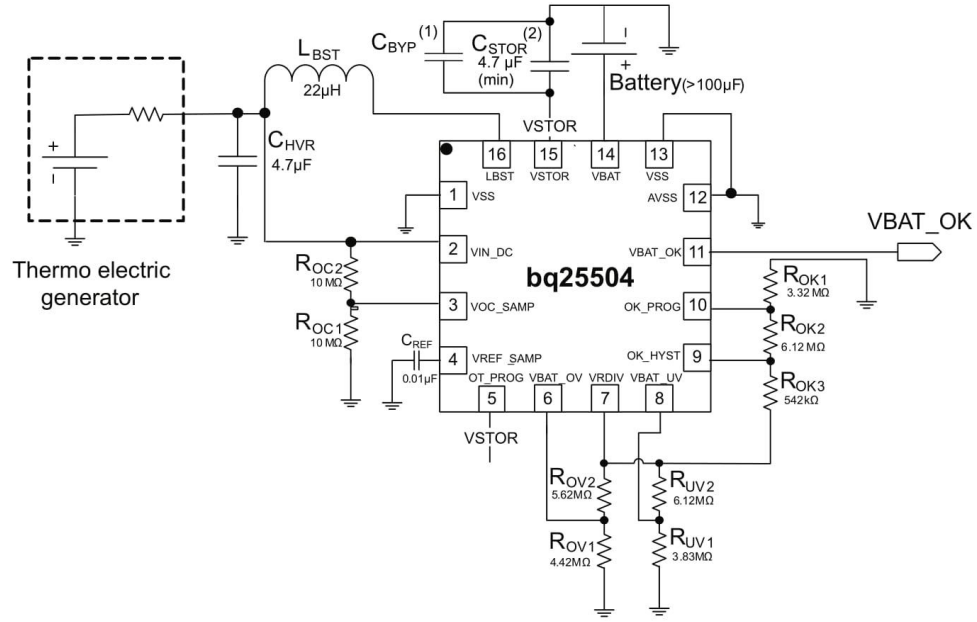


VIN_DC = sourcemeter with V_{SOURCE} = 1 V and compliance of 2.75 mA
No storage element on VBAT
VSTOR artificially ramped from 0V to 3.15 V to 0 V using a power amp driven by a function generator

Figure 20. VBAT_OK Operation

Typical Applications (continued)

9.2.2 TEG Application Circuit



(1) Place close as possible to IC pin 15 (VSTOR) and pin 13 (VSS)

(2) See the Capacitor Selection section for guidance on sizing C_{STOR}

Figure 21. Typical TEG Application Circuit

9.2.2.1 Design Requirements

The desired voltage levels are VBAT_OV = 4.25 V, VBAT_UV = 3.20 V, VBAT_OK = 3.55 V, VBAT_OK_HYST = 3.76 V and MPP (V_{OC}) = 50% which is typical for TEG harvesters. The IC must stop charging if its junction temperature is above 120°C. The simulated TEG open circuit voltage is 1.0 V.

9.2.2.2 Detailed Design Procedure

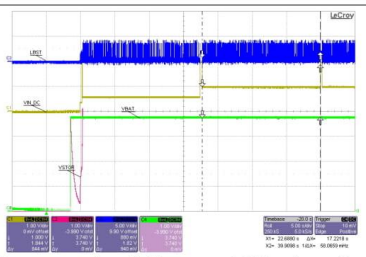
The recommended L1 = 22 µH, C_{BYP} = 0.01 µF and low leakage CREF = 10 nF are selected. In order to ensure the fastest recovery of the harvester output voltage to the MPPT level following power extraction, the minimum recommended CIN = 4.7 µF is selected. Because no large system load transients are expected and to ensure fast charge time during cold start, the minimum recommended CSTOR = 4.7 µF. To stop charging when the IC junction temperature is above 120°C, the OT_PROG pin is tied to VSTOR.

Referring back to the procedure in *Detailed Design Procedure* or using the spreadsheet calculator at SLURAQ1 gives the following values:

- R_{OV1} = 4.42 MΩ, R_{OV2} = 5.49 MΩ resulting in VBAT_OV = 4.26 V due to rounding to the nearest 1% resistor.
- R_{UV1} = 3.83 MΩ, R_{UV2} = 6.04 MΩ resulting in VBAT_UV = 3.22 V due to rounding to the nearest 1% resistor
- R_{OK1} = 3.32 MΩ, R_{OK2} = 6.04 MΩ, R_{OK3} = 0.536 MΩ resulting in VBAT_OK = 3.52 V and VBAT_OK_HYST = 3.73 V after rounding.
- R_{OC1} = 10 MΩ and R_{OC2} = 10 MΩ gives 50% MPP voltage.

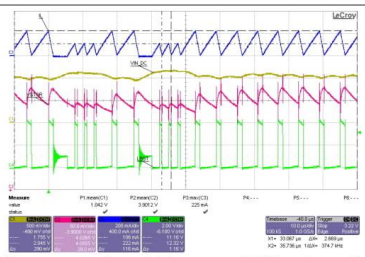
Typical Applications (continued)

9.2.2.3 Application Curves



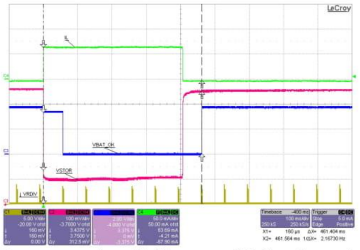
VINDC = sourcemeter with V_{SOURCE} = 2.0 V and compliance of 1 mA
VBAT connected to LiIon battery
VSTOR = 50 kΩ resistor

Figure 22. Startup by Attaching Charged Storage Element



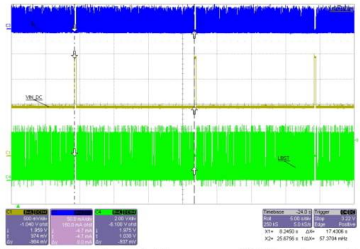
VIN_DC = sourcemeter with V_{SOURCE} = 2.0 V and compliance of 100 mA
VBAT connected to LiIon battery
VSTOR = 100 kΩ resistive load (IL = inductor current)

Figure 23. Boost Charger Operational Waveforms



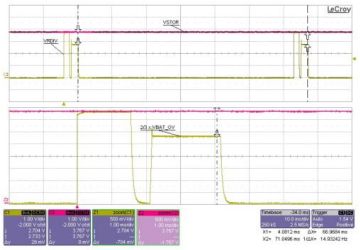
VIN_DC = sourcemeter with V_{SOURCE} = 2.0 V and compliance of 1 mA
VBAT connected to LiIon battery
VSTOR = open to 50Ω to open resistive load (IL = load current on VSTOR)

Figure 24. 50 mA Load Transient on VSTOR



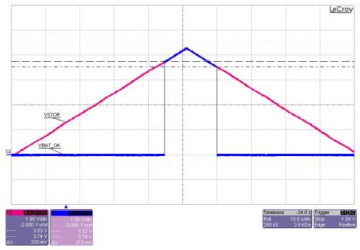
VIN_DC = sourcemeter with V_{SOURCE} = 2.0 V and compliance of 1 mA
VBAT connected to LiIon battery
IL = inductor current

Figure 25. MPPT Operation



VIN_DC = sourcemeter with V_{SOURCE} = 2.0 V and compliance of 1 mA
VBAT connected to LiIon battery

Figure 26. VRDIV Operation

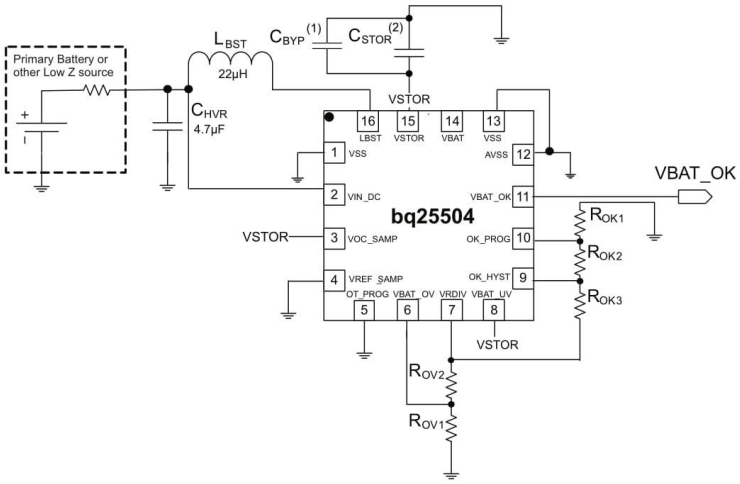


VIN_DC = sourcemeter with V_{SOURCE} = 2.0 V and compliance of 1 mA
No storage element on VBAT
VSTOR artificially ramped from 0V to 4.25V to 0V using a power amp driven by a function generator

Figure 27. VBAT_OK Operation

Typical Applications (continued)

9.2.3 MPPT Disabled, Low Impedance Source Application Circuit



(1) Place close as possible to IC pin 15 (VSTOR) and pin 13 (VSS)

(2) See the Capacitor Selection section for guidance on sizing C_{STOR}

Figure 28. Typical MPPT Disabled Application Circuit (Low Iq Boost Converter from Low Impedance Source)

9.2.3.1 Design Requirements

The input source is a low impedance 1.2 V battery therefore MPPT is not needed. The output will be a low ESR capacitor therefore VSTOR can be tied to VBAT and VBAT_UV is not needed. The desired voltage levels are VBAT_OV = 3.30 V, VBAT_OK = 2.80 V, VBAT_OK_HYST = 3.10 V, and MPPT disabled. The IC must stop charging if its junction temperature is above 65°C. Load transients are expected.

9.2.3.2 Detailed Design Procedure

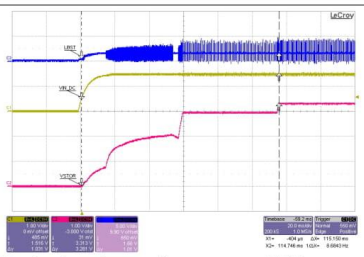
The recommended L1 = 22 µH, C_{BYP} = 0.01 µF and low leakage CREF = 10 nF are selected. The minimum recommended CIN = 4.7 µF is selected. To prevent VSTOR from drooping during system load transients, CSTOR is set to 100 µF. To disable the sampling for MPPT, the VOC_SAMP pin is tied to VSTOR. To disable the input voltage regulation circuit, the VREF_SAMP pin is tied to GND. Since the VBAT_UV function is not needed, the VBAT_UV can be tied to VSTOR. To stop charging when the IC junction temperature is above 65°C, the OT_PROG pin is tied to GND.

Referring back to the procedure in *Detailed Design Procedure* or using the spreadsheet calculator at SLURAQ1 gives the following values:

- R_{OV1} = 5.62 MΩ, R_{OV2} = 4.22 MΩ resulting in VBAT_OV = 3.28 V due to rounding to the nearest 1% resistor.
- R_{OK1} = 4.12 MΩ, R_{OK2} = 5.11 MΩ, R_{OK3} = 0.976 MΩ resulting in VBAT_OK = 2.80 V and VBAT_OK_HYST = 3.10 V after rounding.

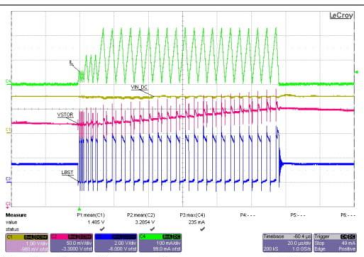
Typical Applications (continued)

9.2.3.3 Application Curves



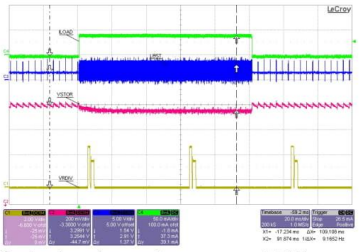
VIN_DC = low impedance voltage source = 1.5 V
VBAT = VSTOR = 100 µF
VSTOR = 500 Ω resistor

Figure 29. Startup



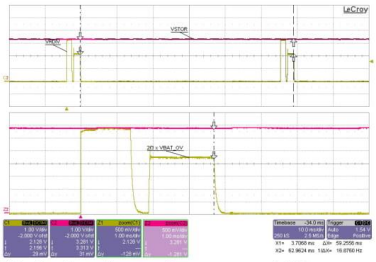
VIN_DC = low impedance voltage source = 1.5 V
VBAT = VSTOR = 100 µF
VSTOR = 330 Ω resistive load (IL = inductor current)

Figure 30. Boost Charger Operational Waveforms



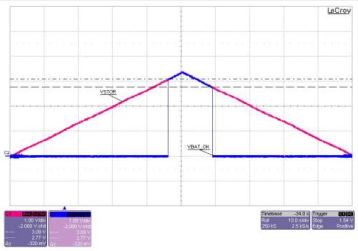
VIN_DC = low impedance voltage source = 1.5 V)
VBAT = VSTOR = 100 µF
VSTOR = open to 75 Ω to open resistive load (IL = load current on VSTOR

Figure 31. 40 mA Load Transient on VSTOR



VIN_DC = low impedance voltage source = 1.5 V
VBAT = VSTOR = 100 µF

Figure 32. VRDIV Operation



VIN_DC = low impedance voltage source = 1.5 V
VBAT = VSTOR = 100 µF
VSTOR artificially ramped from 0 V to 3.3 V to 0 V using a power amp driven by a function generator

Figure 33. VBAT_OK Operation

10 Power Supply Recommendations

The energy harvesting source (e.g., solar panel, TEG, vibration element) must provide a minimum level of power for the IC to operate as designed. The IC's minimum input power required to exit cold start can be estimated as:

$$PIN > PIN(CS) = VIN(CS) \times IIN(CS) > \frac{\left(I - STR\_ELM\_LEAK_{@1.8V} \times 1.8V\right) + \frac{(1.8V)^2}{RSTOR(CS)}}{0.05} \quad (16)$$

where I-STR_ELM_LEAK$_{@1.8V}$ is the storage element leakage current at 1.8V and

RSTOR(CS) is the equivalent resistive load on VSTOR during cold start and 0.05 is an estimate of the worst case efficiency of the cold start circuit.

Once the IC is out of cold start and the system load has been activated (e.g., using the VBAT_OK signal), the energy harvesting element must provide the main boost charger with at least enough power to meet the average system load. Assuming RSTOR(AVG) represents the average resistive load on VSTOR, the simplified **equation below** gives an estimate of the IC's minimum input power needed during system operation:

$$PIN \times \eta_{EST} > PLOAD = \frac{(VBAT\_OV)^2}{RSTOR(AVG)} + VBAT\_OV \times I - STR\_ELM\_LEAK_{@VBAT\_OV} \quad (17)$$

where η_{EST} can be derived from the datasheet efficiency curves for the given input voltage and current and VBAT_OV. The simplified equation above assumes that, while the harvester is still providing power, the system goes into low power or sleep mode long enough to charge the storage element so that it can power the system when the harvester eventually is down. Refer to spreadsheet SLUC462 for a design example that sizes the energy harvester.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the PCB layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the boost charger could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitors as well as the inductors should be placed as close as possible to the IC. For the boost charger, first priority are the output capacitors, including the 0.1 uF bypass capacitor (CBYP), followed by CSTOR, which should be placed as close as possible between VSTOR, pin 15, and VSS, pin 1 or 13. Next, the input capacitor, CIN, should be placed as close as possible between VIN_DC, pin 2, and VSS, pin 1. Last in priority is the boost charger inductor, L1, which should be placed close to LBOOST, pin 16, and VIN_DC, pin 2 if possible. It is best to use vias and bottom traces for connecting the inductor to its respective pins instead of the capacitors.

To minimize noise pickup by the high impedance voltage setting nodes (VBAT_OV, VBAT_UV, OK_PROG, OK_HYST), the external resistors should be placed so that the traces connecting the midpoints of each divider to their respective pins are as short as possible. When laying out the non-power ground return paths (e.g. from resistors and CREF), it is recommended to use short traces as well, separated from the power ground traces and connected to AVSS pin 12. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current. The PowerPad should not be used as a power ground return path.

The remaining pins are digital signals with minimal layout restrictions. See Figure 34 for an example layout.

In order to maximize efficiency at light load, the use of voltage level setting resistors > 1 MΩ is recommended. In addition, the sample and hold circuit output capacitor on VREF_SAMP must hold the voltage for 16 s. During board assembly, contaminants such as solder flux and even some board cleaning agents can leave residue that may form parasitic resistors across the physical resistors/capacitors and/or from one end of a resistor/capacitor to ground, especially in humid, fast airflow environments. This can result in the voltage regulation and threshold levels changing significantly from those expected per the installed components. Therefore, it is highly

Layout Guidelines (continued)

recommended that no ground planes be poured near the voltage setting resistors or the sample and hold capacitor. In addition, the boards must be carefully cleaned, possibly rotated at least once during cleaning, and then rinsed with de-ionized water until the ionic contamination of that water is well above 50 Mohm. If this is not feasible, then it is recommended that the sum of the voltage setting resistors be reduced to at least 5X below the measured ionic contamination.

11.2 Layout Example

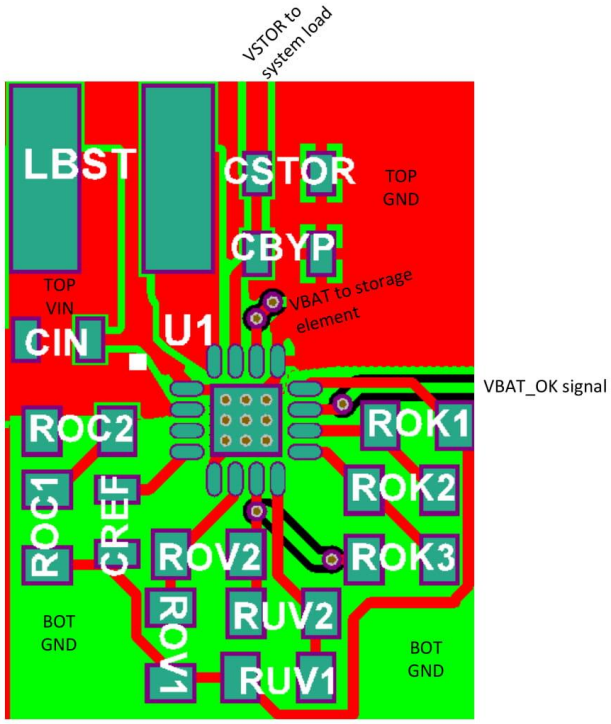


Figure 34. Recommended Layout

11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power-dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

For more details on how to use the thermal parameters in the Thermal Table, check the Thermal Characteristics Application Note (SZZA017) and the IC Package Thermal Metrics Application Note (SPRA953).

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.1.2 Zip Files

- http://www.ti.com/lit/zip/SLUC484
- http://www.ti.com/lit/zip/SLURAQ1
- http://www.ti.com/lit/zip/SLUC462

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- EVM User's Guide, SLUUAA8
- Thermal Characteristics Application Note, SZZA017
- IC Package Thermal Metrics Application Note, SPRA953

12.3 Trademarks

All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

TEXAS INSTRUMENTS

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PACKAGE OPTION ADDENDUM

11-Aug-2017

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ25504RGTR	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B5504	Samples
BQ25504RGTT	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B5504	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

11-Aug-2017

TEXAS INSTRUMENTS

PACKAGE MATERIALS INFORMATION

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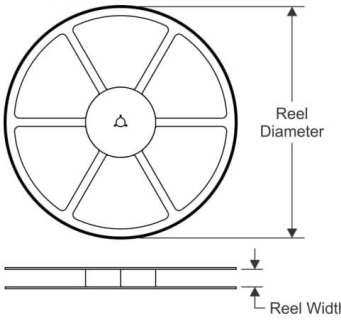
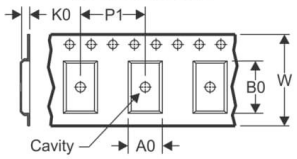
11-Aug-2017

TAPE AND REEL INFORMATION

REEL DIMENSIONS

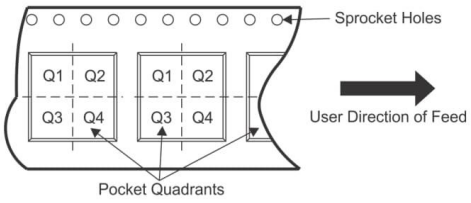


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25504RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ25504RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TEXAS INSTRUMENTS

PACKAGE MATERIALS INFORMATION

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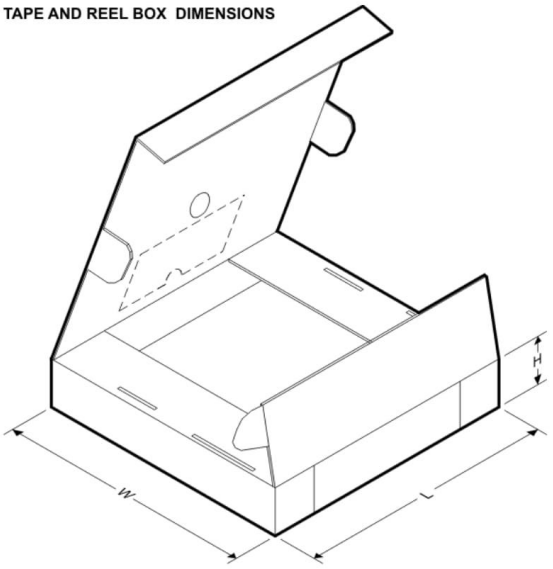
11-Aug-2017

TAPE AND REEL BOX DIMENSIONS



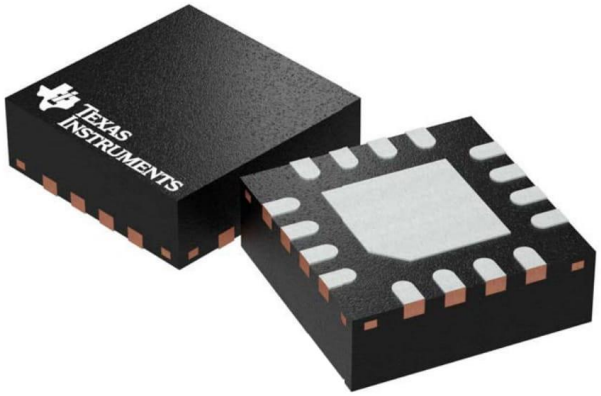
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25504RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
BQ25504RGTT	VQFN	RGT	16	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RGT 16 **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203495/I

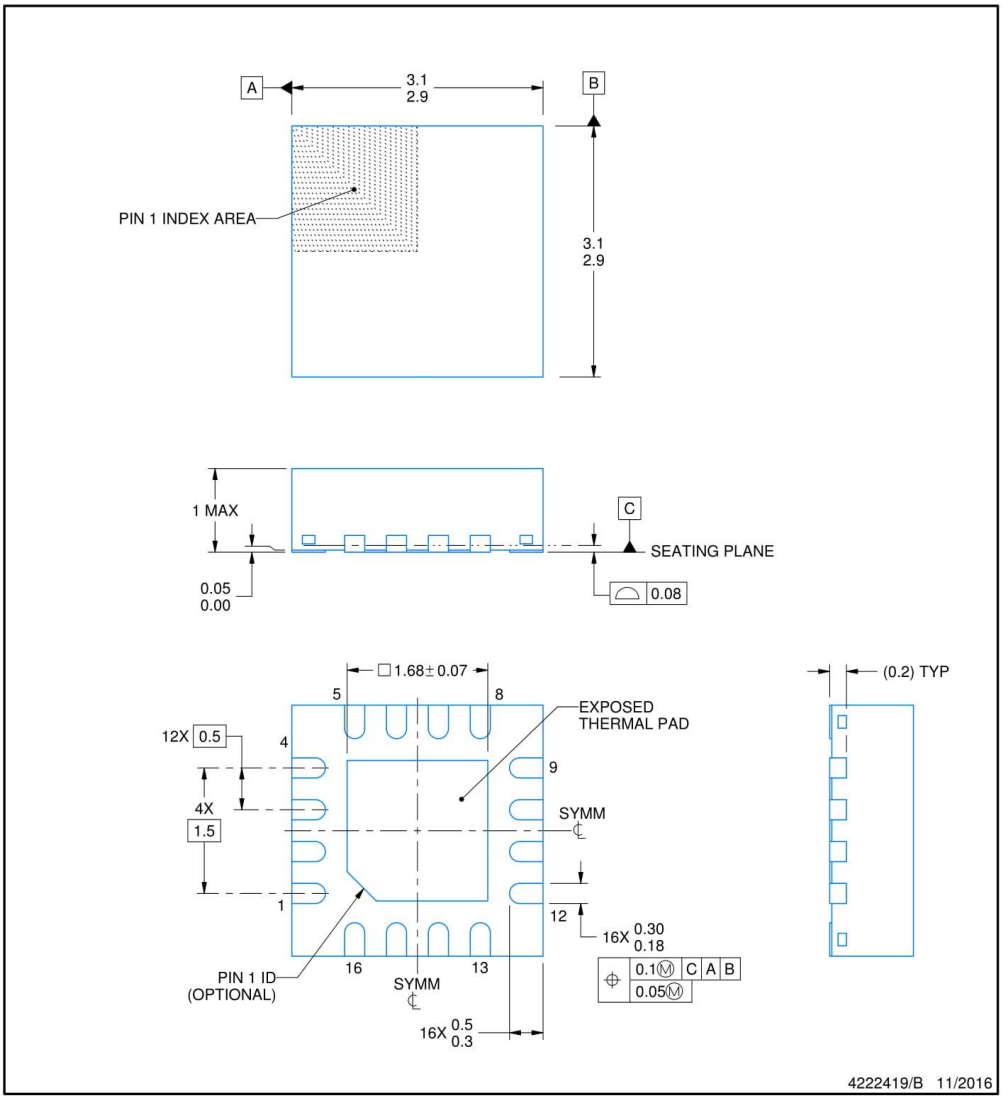
Texas Instruments

RGT0016C

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



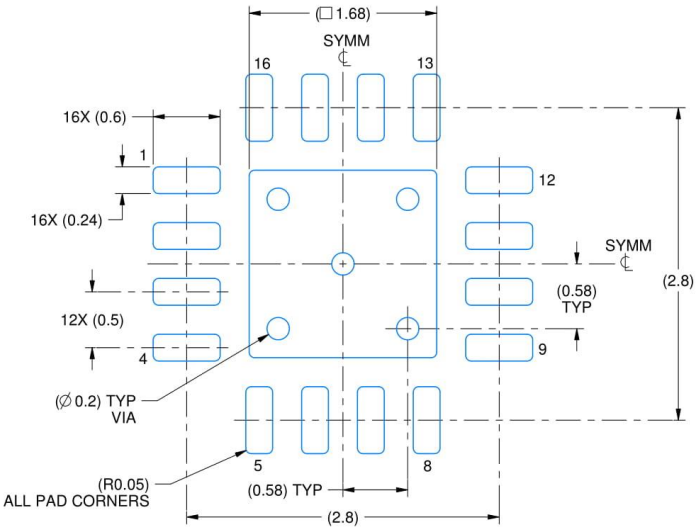
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

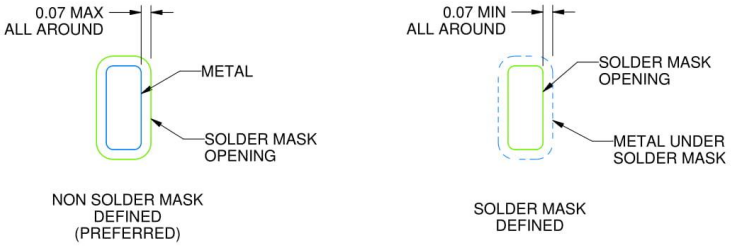
EXAMPLE BOARD LAYOUT

RGT0016C — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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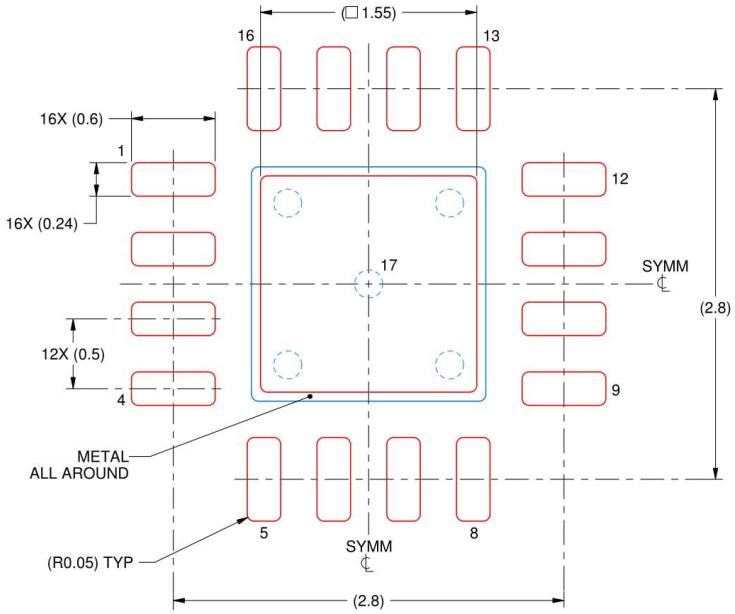
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGT0016C — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Appendix 2 – Comparison between rechargeable batteries and supercapacitor

Table 7.1: Comparison between different types of rechargeable battery and supercapacitor [42][44][105].

Parameter	**Ni-Cd**	**Ni-MH**	**Li-ion**	**Supercapacitor**
Power Density (W/kg)	10-500	10-500	10-500	3000
Energy Density (Wh/kg)	45-80	60-120	110-160	1-10
Cycle Life	1500	300-500	500-1000	10^6
Charging Time (seconds)	> 1000	> 1000	> 1000	0.3-100
Overcharge Tolerance	Moderate	Low	Very Low	Very High
Operating Temperature (ºC)	-40 - 60	-20 - 60	-20 - 60	-40 - 65
Cell Voltage (V)	1.25	1.25	3.6	-
Cost Per Cycle (USD)	0.04	0.12	0.14	0.0001
Cost Per Wh (USD)	0.90	0.55	0.81	20
Efficiency (%)	70-85	70-85	70-85	> 95
Maintenance Requirement	Yes	Yes	No	No
In Use Since	1950	1990	1991	1982

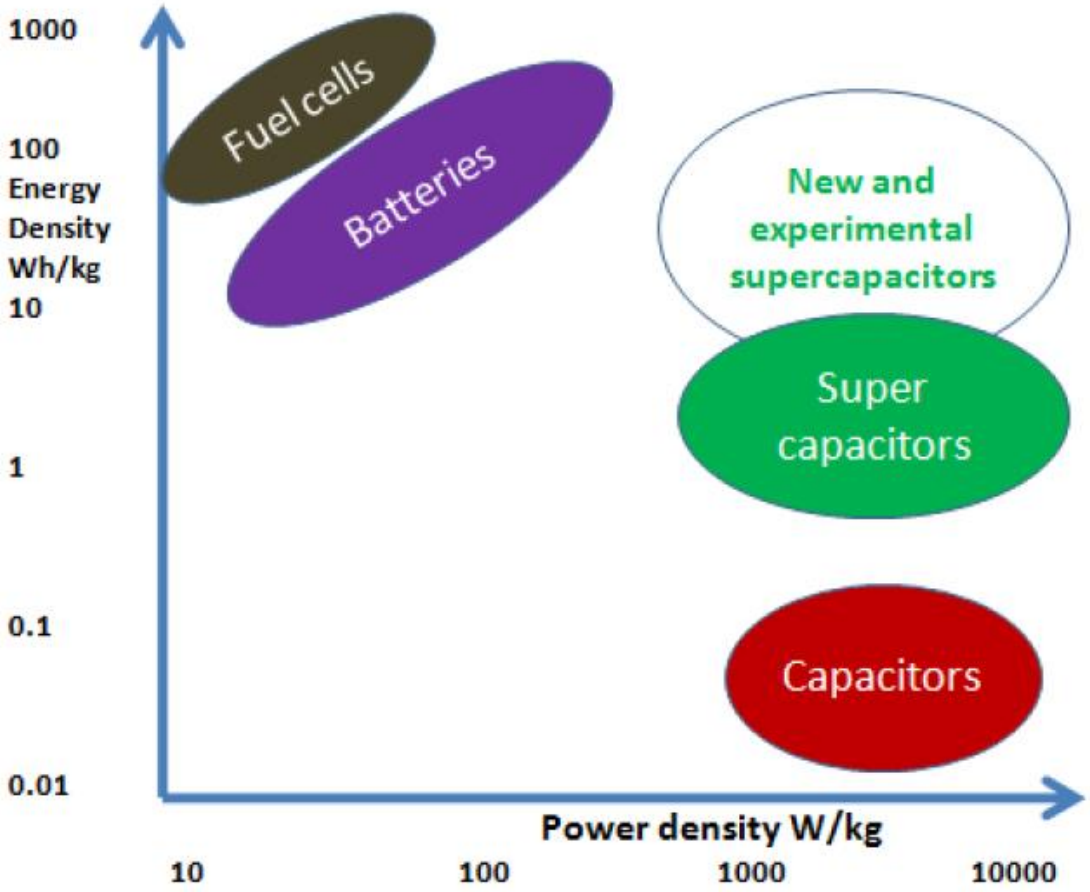

Figure 7.1: Ragone chart for different energy storage technology [45].

Appendix 3 – Bill of materials (BOM) for the pico-grid first prototype

Table 7.2: Bill of materials for the constructed prototype.

No.	Description	Category	Quantity	Unit Cost (£)	Total Cost (£)
1	Sanyo 852mW Amorphous Solar Cell Photovoltaic Solar Panel	Energy harvester	2.0	54.8800	109.7600
2	Peltier Module, 9.32W, 1.47A, 15.4V, 40 x 40mm	Energy harvester	2.0	43.5800	87.1600
3	LTC3105EMS#PBF - DC-DC Switching Boost (Step Up) Regulator, Adjustable, 225mV-5Vin, 1.5V-5.25Vout, 400mAout, MSOP-12	DC-DC converter	4.0	2.4700	9.8800
4	LTC3129EMSE#PBF - DC-DC Switching Buck-Boost Regulator, Adjustable, 1.92V-15Vin, 1.4V-15.75Vout, 200mAout, MSOP-16	DC-DC converter	2.0	5.5800	11.1600
5	ENIX Energies 3.7V Rechargeable Lithium Battery Pack, 1840mAh	Energy storage	1.0	38.1500	38.1500
6	Vishay 15F Supercapacitor EDLC -20 → +80% Tolerance 196 HVC Series 4.2V dc Through Hole	Energy storage	2.0	6.7600	13.5200
7	BQ25504RGTT - Battery Charger Li-Ion battery, 3V input, 5.25V charge, QFN-16	DC-DC converter	1.0	4.6700	4.6700
8	**Multiple resistors:**				
	Resistor; Wirewound; Res 0.5 Ohms	Passive component	5.0	1.5200	7.6000
	Resistor; Wirewound; Res 1 Ohms		2.0	0.7300	1.4600
	330 Ω 0.25W 250V ±5% tolerance		3.0	0.0080	0.0240
	470 Ω 0.25W 250V ±5% tolerance		5.0	0.0080	0.0400
	680 Ω 0.25W 250V ±5% tolerance		2.0	0.0080	0.0160
	1 kΩ 0.25W 250V ±5% tolerance		14.0	0.0080	0.1120
	1.5 kΩ 0.25W 250V ±5% tolerance		2.0	0.0080	0.0160
	2.2 kΩ 0.25W 250V ±5% tolerance		6.0	0.0080	0.0480
	3.3 kΩ 0.25W 250V ±5% tolerance		13.0	0.0080	0.1040

	4.7 kΩ 0.25W 250V ±5% tolerance		17.0	0.0080	0.1360
	6.8 kΩ 0.25W 250V ±5% tolerance		4.0	0.0080	0.0320
	10 kΩ 0.25W 250V ±5% tolerance		19.0	0.0080	0.1520
	15 kΩ 0.25W 250V ±5% tolerance		15.0	0.0080	0.1200
	22 kΩ 0.25W 250V ±5% tolerance		15.0	0.0080	0.1200
	33 kΩ 0.25W 250V ±5% tolerance		21.0	0.0080	0.1680
	47 kΩ 0.25W 250V ±5% tolerance		9.0	0.0080	0.0720
	68 kΩ 0.25W 250V ±5% tolerance		9.0	0.0080	0.0720
	100 kΩ 0.25W 250V ±5% tolerance		10.0	0.0080	0.0800
	150 kΩ 0.25W 250V ±5% tolerance		8.0	0.0080	0.0640
	220 kΩ 0.25W 250V ±5% tolerance		9.0	0.0080	0.0720
	330 kΩ 0.25W 250V ±5% tolerance		6.0	0.0080	0.0480
	470 kΩ 0.25W 250V ±5% tolerance		8.0	0.0080	0.0640
	680 kΩ 0.25W 250V ±5% tolerance		10.0	0.0080	0.0800
	1 MΩ 0.25W 250V ±5% tolerance		8.0	0.0080	0.0640
	1.5 MΩ 0.25W 250V ±5% tolerance		4.0	0.0080	0.0320
	2.2 MΩ 0.25W 250V ±5% tolerance		4.0	0.0080	0.0320
	3.3 MΩ 0.25W 250V ±5% tolerance		2.0	0.0080	0.0160
	4.7 MΩ 0.25W 250V ±5% tolerance		2.0	0.0080	0.0160
	6.8 MΩ 0.25W 250V ±5% tolerance		1.0	0.0080	0.0080
	10 MΩ 0.25W 250V ±5% tolerance		4.0	0.0080	0.0320
9	**Multiple capacitors:**	Passive component			

	100 pF X1/Y2 Ceramic Disc Capacitor		4.0	0.0160	0.0640
	2.2 nF X1/Y2 Ceramic Disc Capacitor		8.0	0.0160	0.1280
	1 uF X1/Y2 Ceramic Disc Capacitor		10.0	0.0160	0.1600
	0.1 uF X1/Y2 Ceramic Disc Capacitor		6.0	0.0160	0.0960
	4.7 nF X1/Y2 Ceramic Disc Capacitor		2.0	0.0160	0.0320
	10 nF X1/Y2 Ceramic Disc Capacitor		1.0	0.0160	0.0160
	470 pF X1/Y2 Ceramic Disc Capacitor		4.0	0.0160	0.0640
	Electrolytic Capacitor, 4.7 µF, 50 V		8.0	0.1090	0.8720
	Electrolytic Capacitor, 10 µF, 50 V		18.0	0.1090	1.9620
	Electrolytic Capacitor, 22 µF, 50 V		6.0	0.1090	0.6540
	Electrolytic Capacitor, 100 µF, 50 V		4.0	0.1090	0.4360
	Electrolytic Capacitor, 1 mF, 50 V		1.0	0.1090	0.1090
	Electrolytic Capacitor, 2.2 µF, 50 V		14.0	0.1090	1.5260
	Electrolytic Capacitor, 1 µF, 50 V		18.0	0.1090	1.9620
10	**Multiple inductors:**				
	Inductor SMD shielded 22uH 12.5x12.5x6	Passive component	1.0	0.3180	0.3180
	C429 - Inductor Kit, XAL40xx Series Shielded Power Inductors, 8.2uH		2.0	0.6520	1.3040
	C429 - Inductor Kit, XAL40xx Series Shielded Power Inductors, 10uH		4.0	0.6520	2.6080
11	**Light dependent resistors:**				
	NSL 19M51. - LDR, 20 Mohm, 50 mW, 100 V	Passive component	2.0	0.6320	1.2640
	N5AC501085 - LDR, 5 Mohm, 50 mW, 100 V		2.0	1.5400	3.0800

12	**Thermistors:**				
	LT300014T2610KJ - PTC Thermistor, 10 kohm, Through Hole, -5% to +5%, LT Series		2.0	0.3620	0.7240
	B57871S0123H000 - Thermistor, NTC, 12 kohm, B57871S Series, 3760 K, Through Hole, Radial Leaded	Passive component	3.0	0.7880	2.3640
	ND03U00105J-- - Thermistor, NTC, 1 Mohm, ND03 Series, 4840 K, Through Hole, Radial Leaded		1.0	0.7310	0.7310
	B57861S0503H040 - Thermistor, NTC, 50 kohm, B57861S Series, 3760 K, Through Hole, Wire Leaded		3.0	1.3800	4.1400
13	Texas Instruments INA283AID, Current Shunt Monitor Single Bidirectional 8-Pin SOIC	Active component/IC	3.0	3.2500	9.7500
14	STMicroelectronics TSV632IDT, Low Power, Op Amp, RRIO, 880kHz, 1.5 → 5.5 V, 8-Pin SOIC	Active component/IC	3.0	0.7370	2.2110
15	Microchip MCP6542-I/SN Dual Comparator, Push-Pull O/P, 1.6 → 5.5 V 8-Pin SOIC	Active component/IC	2.0	0.5370	1.0740
16	Voltage reference IC, REF3012AIDBZT 1.25V	Active component/IC	1.0	1.2400	1.2400
17	Through Hole Slide Switch DPDT On-On 300 mA Slide	Switches	6.0	0.3620	2.1720
18	Diodes Inc DMG2302UK-7 N-channel MOSFET, 2.8 A, 20 V DMG2302UK, 3-Pin SOT-23	Active component/IC	5.0	0.0730	0.3650
19	Panasonic Lithium CR2032 3V Lithium Manganese Dioxide Coin Battery	Battery	7.0	1.4400	10.0800
20	**12 AWG insulated copper wires:**				
	Alpha Wire EcoWire Series Black, 30m MPPE UL11028 Hook Up Wire, 3.3 mm² CSA Flame Retardant, 600 V 12 AWG	Connector/wire	1.0	42.6400	42.6400
	Alpha Wire EcoWire Series Red, 30m MPPE UL11028 Hook Up Wire, 3.3 mm² CSA Flame Retardant, 600 V 12 AWG		1.0	42.6400	42.6400
21	**Multiple IC to board adaptors:**				
	LCQT-SOIC8-8 - IC Adapter, 8-SOIC to 8-DIP, 2.54mm Pitch Spacing, 7.62mm Row Pitch, Correct-A-Chip Series	IC adaptor	13.0	3.7300	48.4900

	RE909 - IC Adapter, Fibreglass, 3-SOT-23, 2.54mm Pitch Spacing		5.0	1.6200	8.1000
	RE935-06E - IC Adapter, Fibreglass, 1 6-QFN, 2.54mm Pitch Spacing, RE935 Series		1.0	1.6200	1.6200
	IPC0079 - MSOP-16 to DIP-20 SMT Adaptor		2.0	5.0900	10.1800
	IPC0078 - MSOP-12 to DIP-16 SMT Adaptor		4.0	4.4900	17.9600
22	RE520-HP, Single-Sided Stripboard FR-2 100 x 160 x 1.5mm FR2	Circuit board	7.0	4.1600	29.1200
23	AB77 - Plastic Enclosure, PCB Guides, Multipurpose, ABS, 178 mm, 122 mm, 36 mm	Prototyping	7.0	6.5200	45.6400
24	Thermawrap 400mm x 5m x 3.7mm Loft Wrap Easy Fit Loft Insulation without Thickness	Prototyping	1.0	7.7000	7.7000
25	Heatsink ICK PGA 9.8 K/W	Prototyping	2.0	1.7700	3.5400
26	Thermal interface material 40mm polyimid	Prototyping	2.0	2.0700	4.1400
27	VELCRO VEL-EC60245 Brand Heavy Duty Stick-On Tape, Black, 50 mm x 2.5 m	Prototyping	1.0	16.8500	16.8500
28	JST connectors (male and female pair) with headers (set)	Connector/wire	1.0	8.9900	8.9900
				Grand Total	**£624.32**

Appendix 4 – Wolfram Mathematica programme to plot the I-V curve of the diode

```
(*
This is a Mathematica program for assessing Schottky barrier data for ZnON from Arokia Nathan. 7 September 2017 *)

Clear["Global`*"];
Unprotect[In, Out]; Clear[In, Out]; Protect[In, Out];
$Line = 0;

(* CONSTANTS *)
kB := 1.38×10^(-23)
q := 1.6×10^(-19)
temp := 273+50
StringForm["Temperature = `` K ", NumberForm[temp, 3]]
mo := 9.1096*10^(-31)
h := 6.6262×10^(-34)
hbar := 1.0546×10^(-34)
epsilon := 8.8544×10^(-12)

(* Input *)
area := 6.6×10^(-3)
StringForm["Area = `` cm^2 ", NumberForm[area, 4]]
astar := 22.8
StringForm["Effective Richardson constant = `` Acm^-2K^-2 ", NumberForm[astar, 3]]
phiB := 0.86
StringForm["Barrier height = `` eV ", NumberForm[phiB, 4]]
rs := 7000
StringForm["Series resistance = `` Ohms ", NumberForm[rs, 2]]
n := 2.4
StringForm["Ideality factor = `` (unitless) ", NumberForm[n, 4]]

(* Calculations *)
isub0 := area astar temp^2 Exp[-q phiB / (kB temp)]
StringForm["Reverse saturation current  = `` A ", ScientificForm[isub0, 2]]
i[v_] := i1 /. FindRoot[i1 == isub0 (Exp[q (v - i1 rs) / (n kB temp)] - 1), {i1, 0}];
j[v_] := i[v] / area
plot1 = LogPlot[j[v], {v, 0, 3}, PlotRange → All, AxesLabel → {"Voltage (V)", "Current density (mA/cm^2)"}]
Quiet[tableJV := Table[{v, N[j[v]]}, {v, 0.05, 1.5, 0.05}]]
Quiet[Export["tableJV.xlsx", tableJV]]
```

Figure 7.2: Programme in Wolfram Mathematica used to plot the I-V curve of the diode.