A 40 Gb/s Optical Bus for Optical Backplane Interconnections

Nikolaos Bamiedakis, Aeffendi Hashim, Richard V. Penty, *Senior Member, IEEE*
and Ian H. White, *Fellow, IEEE*

Abstract— Optical technologies have received large interest in recent years for use in board-level interconnects. Polymer multimode waveguides in particular, constitute a promising technology for high-capacity optical backplanes as they can be cost-effectively integrated onto conventional printed circuit boards (PCBs). This paper presents the first optical backplane demonstrator based on the use of PCB-integrated polymer multimode waveguides and a regenerative shared bus architecture. The backplane demonstrator is formed with commercially-available low-cost electronic and photonic components onto conventional FR4 substrates and comprises two opto-electronic (OE) bus modules interconnected via a prototype regenerator unit. The system enables interconnection between the connected cards over 4 optical channels, each operating at 10 Gb/s. Bus extension is achieved by cascading OE bus modules via 3R regenerator units, overcoming therefore the inherent limitation of optical bus topologies in the maximum number of cards that can be connected to the bus. Details of the design, fabrication and assembly of the different parts of this optical bus backplane are presented and related optical and data transmission characterisation studies are reported. The optical layer of the OE bus modules comprises a 4-channel 3-card waveguide layout that is compatible with VCSEL/PD arrays and ribbon fibres. All on-board optical paths exhibit insertion losses below 13 dB and intra-channel crosstalk lower than -29 dB. The robustness of the signal distribution from the bus inputs to all respective bus output ports in the presence of input misalignment is demonstrated, while 1 dB input alignment tolerances of approximately ± 10 μm are obtained. The electrical layer of the OE bus modules comprises the essential driving circuitry for 1×4 VCSEL and PD arrays and the corresponding control and power regulation circuits. The interface between the optical and electrical layers of the bus modules is achieved with simple OE connectors that enable end-fired optical coupling into and out of the on-board polymer waveguides. The backplane demonstrator achieves error-free ($\text{BER} < 10^{-12}$) 10 Gb/s data transmission over each optical channel, enabling therefore, an aggregate interconnection capacity of 40 Gb/s between any connected cards.

Index Terms— optical interconnects, polymer waveguides, optical backplanes, optoelectronic integration

I. INTRODUCTION

Recent studies on the future of high-performance electronic systems have highlighted the importance of developing new interconnection technologies to overcome the inherent disadvantages of copper interconnection technologies when operating at high data rates [1-3]. Optical technologies constitute a promising alternative as they provide high bandwidth and high density links with reduced power consumption and relaxed thermal management requirements, while eliminating electromagnetic interference issues [4-6]. Fibre-based optical links are already widely deployed in supercomputers and large-scale data centres for rack-to-rack and intra-rack communication. Nevertheless, next generation supercomputers and data centres will require even larger interconnection bandwidths and increased power efficiency [7-9]. As a result, intensive research has been carried out in recent years on the development of optical technologies suitable for use in even shorter communication distances (< 1 m) and in closer proximity to the electronic chips. Various technologies including fibre-based technologies [10-12], free-space optics [13-15], polymer waveguides [16-21] and Si photonics [22-25], are being considered for use at the different levels of the interconnection hierarchy: board-to-board, chip-to-chip and on-chip communications. However, the cost-effective integration of optics into high-performance electronic systems constitutes a significant technological challenge. Optical technologies need to be compatible with existing electronic system architectures and conventional manufacturing processes of the electronics industry, and allow system assembly and packaging at low costs.

Optical backplanes have received particular interest as they are expected to be the next interconnection level in systems where optical technologies replace copper-based links. Polymer multimode waveguides are increasingly considered for use in such systems as they can be directly integrated with electronics on conventional printed circuit boards (PCBs) and, owing to their relaxed alignment tolerances, enable cost-effective system assembly with standard methods of the electronics industry [26-30]. Various passive interconnection architectures deploying polymer multimode waveguides have been proposed for use in optical backplanes including large parallel waveguide arrays [31-33], meshed waveguide architectures [34, 35] and shared optical buses [36-38]. Broadcast architectures, such as the shared bus topology, have been traditionally used in

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N. Bamiedakis, R. V. Penty and I. H. White, are with the Electrical Engineering Division, Engineering Department, University of Cambridge, CB3 0FA Cambridge, UK (tel: 0044-1223748356; e-mail: nb301@cam.ac.uk).

A. Hashim was based during this work at the Electrical Engineering Division, Engineering Department, University of Cambridge, and is now with the Core IP Network Development Division, Telekom Malaysia.

applications where communication between a large number of users with short bursts and high-throughput is required. Examples of such systems include data storage systems and blade servers where electrical buses have been widely used in the past. In recent years however, the use of such shared electrical buses has dwindled due to a number of issues when operating at high data rates, such as bus loading issues and impedance mismatches. Optical buses based on polymer waveguides can provide a high-bandwidth alternative for the interconnection of next-generation electronic systems. As a result, we recently proposed the use of a regenerative multi-channel optical bus architecture for the formation of cost-effective optical backplanes [38]. The architecture is scalable to large number of cards and interconnection channels as it allows bus extension with multiple modules through the use of 3R regenerators and relies on a scalable waveguide layout. It should be noted that the use of the signal regenerators, although not ultimately preferred, is required in order to overcome the inherent limitation of bus topologies in the maximum number of modules that can be connected to the bus [39, 40]. Unlike other reported optical backplane buses where the number of cards that can be connected is limited [36, 37, 40], the work presented here allows bus extension by cascading multiple bus segments and therefore, the connection of an arbitrary number of cards to the optical bus. The formation of such a cascade of bus modules and regenerator units also allows implementation costs that scale linearly with the desired number of connected cards. Initial work on the optical transmission characteristics of the bus repeating units and preliminary data transmission experiments carried out with external VCSEL sources and receivers has been reported in [38] and [41].

In this paper, we present the first reported optical backplane demonstrator based on the shared bus architecture and PCB-integrated polymer waveguides. The demonstrator comprises two 4-channel 3-card OE bus modules and a prototype 3R regenerator unit, all formed on low-cost FR4 substrates and with commercially-available electronic and photonic components. The system enables communication between any two connected cards at an aggregate data rate of 40 Gb/s (4×10 Gb/s). The design details of the optical and electrical layers of the fabricated opto-electronic PCBs as well as the fabrication and assembly of the system demonstrator are described in the sections that follow.

The paper is organised as follows. In Section II the optical bus architecture is reviewed and the optimised waveguide layout of the 4-channel 3-card bus repeating unit is presented. Section III reports the optical performance of the optimised polymeric bus modules while Section IV describes the implemented optical backplane demonstrator, presents its different parts and details its fabrication and assembly. Section V reports the data transmission experiments carried out. Finally, section VI briefly discusses issues related to the broadcast interconnection architecture and the operation of the bus modules, while section VII concludes the paper.

II. OPTICAL BUS ARCHITECTURE AND WAVEGUIDE LAYOUT

The bus architecture employed in this work has been proposed in [38]. It relies on the use of polymeric bus modules in order to form an optical bus and achieve optical interconnection between the connected electrical cards, and 3R (re-shape, re-time, re-transmit) signal regenerators to enable bus extension with multiple bus segments (Fig. 1a). Each bus segment contains one optical bus in each signal transmission direction which is implemented with polymer multimode waveguides. Each optical bus is made up of multiple optical waveguide channels that feature a signal input (“add”) and output (“drop”) port at each card interface (Fig. 1b). The number of cards that can be accommodated on a single bus segment is limited by the available optical power budget for the on-board links and depends on the launched optical power, the receiver sensitivity and the losses of the optical paths on the bus module. Given the current lack of suitable optical amplification schemes for on-board interconnections, the use of 3R signal regenerators, although not ultimately preferred, is the only solution available to overcome this inherent disadvantage of bus interconnection architectures. The 3R regenerators are used as “bridges” enabling bus extension through the concatenation of multiple bus segments and therefore, the connection of an arbitrary number of cards to the bus.

Fig. 1. (a) Illustration of the regenerative shared bus architecture and (b) schematic of a bus segment with various features noted.

Each bus segment can be formed with two bus repeating units, as shown in Fig. 1b, which are essentially identical in their layout. Their basic waveguide layout, shown in Fig. 2, makes use of parallel multimode waveguide arrays in order to implement the multiple optical channels and is designed to be compatible with standard ribbon fibre input and outputs and VCSEL/PD arrays. Moreover, the layout is scalable to larger numbers of optical channels. Each input (Tx) and output (Rx) port of the bus repeating unit features an array of multimode waveguides whose pitch matches the desired type of input/output (I/O) interface (ribbon fibre, VCSEL/PD arrays).

Each bus channel comprises optical power taps and signal combiners at each card interface to implement the signal “drop” and “add” functions and 90° waveguide bends to route the optical signals from and to the card I/O ports. The bend radius is chosen to be sufficiently large (8.5 mm) to ensure low-loss optical transmission [42]. At the regenerator input (Tx_{3R}) and output (Rx_{3R}) ports, raised-cosine S-bends are employed to generate the required waveguide separation to ensure low-loss waveguide crossings (crossing angle of 90°) and sufficient space for the waveguide bends. The proposed waveguide layout can be readily scaled up to a larger number of optical channels as this would only require longer S-bends and a larger number of 90° waveguide crossings, which have been demonstrated to induce low additional optical losses of ~ 0.01 dB/crossing [42].

Fig. 2. Scalable waveguide layout of an N-channel M-card bus repeating unit.

Link studies using a realistic optical power budget of 15 dB calculated based on commercially-available VCSEL and PD components (launched VCSEL power: 2 dBm, receiver sensitivity: -13 dBm for a BER of 10^{-12} at 10 Gb/s) and estimated optical losses for the waveguide components, indicate that 3 cards can be connected to the bus before regeneration is required [38]. As a result, initial 4-channel 3-card polymeric bus modules have been designed and fabricated onto FR4 substrates. The optical transmission performance of these preliminary modules reported in [41] suffered from non-ideal power splitting at the optical tap of the 1st card interface and high excess losses at the signal combiners, resulting in large optical losses for some of the on-board optical paths. As a result, optimisation of the waveguide design of the 4-channel 3-card bus module has been carried out based on separate studies on the multimode waveguide components used in the optical bus [43] and an empirical method for the design of complex on-board optical paths employing multimode waveguide components [44]. The layout design targets the availability of a 2 dB power margin for all on-board optical paths. The waveguide layout of the 4-channel 3-card polymeric bus modules as well as details of the optimised main bus structure are shown in Fig. 3.

III. 4-CHANNEL 3-CARD POLYMERIC BUS MODULES

Sample optimised polymeric bus modules have been fabricated on 0.5 mm-thick FR4 substrates with standard

photolithographic methods. The polymer materials employed in this work are the siloxane materials OE-4140 (core) and OE-4141 (cladding) developed by Dow Corning Co. These polymer materials have been appropriately engineered for use in board-level optical interconnects: they can withstand the high temperatures in excess of 250°C required for solder reflow and board lamination processes, they exhibit low optical absorption of ~0.04 dB/cm at the 850 nm wavelength and the required environmental stability to withstand the typical operating conditions of electronic systems [44-46]. The fabricated samples measure 90×50 mm² and are diced with a Disco DAD341 dicing saw to expose the waveguide facets. Unlike other work on polymer waveguides, no polishing steps are undertaken to improve the quality of the exposed facets. A photograph of a fabricated sample is shown in Fig. 4 while some images of waveguide components on the main optical bus are also depicted.

Fig. 3. Waveguide layout of 4-channel 3-card polymeric bus module and inset schematic of the optimized main optical bus structure with dimensions noted.

Fig. 4. (a) Photographs of (a) a fabricated 4-channel 3-card polymeric bus module on a 0.5 mm FR4 substrate. Input ports 2 and 3 are illuminated with red and green light respectively, while path 3a with blue light. (b) Images of waveguide components noted on main optical bus in Fig. 3: (I) Y-splitter, (II) Y-combiner and (III) 90° crossings.

The optical transmission characteristics of the optimised bus modules are studied under different launch conditions that represent the different input types that can be used with the bus modules: a cleaved 50/125 μm OM3 MMF patchcord and a

Fig. 5. Insertion loss of all optical paths of the 4-channel polymer bus module when a butt-coupled 1×4 VCSEL array and a $50 \mu\text{m}$ MMF input are used. For comparison, losses obtained from the initial waveguide design are also shown.

butt-coupled 1×4 VCSEL array. The insertion loss of all on-board optical paths, the crosstalk performance as well as the input alignment tolerances are assessed. For all measurements, a cleaved $62.5/125 \mu\text{m}$ MMF is employed at the bus output ports to collect the light and deliver it to an optical power meter. Index-matching gel is used at the waveguide outputs for all measurements in order to minimise Fresnel and scattering losses while, at the waveguide input, index-matching gel is only applied for the measurements carried out with the $50 \mu\text{m}$ MMF.

To measure the insertion loss of all on-board optical paths and the induced crosstalk, the input is aligned with each input port of the bus module while the power received at all bus outputs is recorded. Fig. 5 shows the insertion loss of all on-board optical paths for the optimised bus module for both input types. The respective values obtained from the preliminary waveguide design reported in [41] are also shown for comparison. It can be seen that the path losses in the optimised bus module have been significantly reduced and that all paths exhibit losses within the 15 dB available power budget and with a power margin larger than 2 dB for both input types. The variation in the insertion losses of the different on-board optical paths observed in Fig. 5 is expected as the paths are intentionally designed not to be identical by varying the tap widths and combiner merging widths along the optical bus. The optical paths are not symmetric while the excess loss of each waveguide component depends on its exact position along each specific optical path. Typical values for the excess losses of the components used in the bus module (splitters, combiners, crossings) can be found in the studies reported in [43] and [44], while the loss breakdown analysis for the preliminary bus module design is presented in [44]. For the optimised bus module, a similar loss breakdown analysis has been carried out and is included in [47]. The total coupling losses are estimated to be roughly 1 dB and 1.5 dB for a $50 \mu\text{m}$ MMF input and a butt-coupled VCSEL array respectively.

The total path loss for each input port is also calculated by adding up the power received at all respective bus outputs (e.g. for input port 1, corresponding output ports: a, e, i and l') and subtracting the power launched at the input (Fig. 6). The

Fig. 6. Total path loss for all input ports of the bus module for a $50 \mu\text{m}$ MMF input and a butt-coupled 1×4 VCSEL array. Inset image of the butt-coupled VCSEL array with the input waveguides.

obtained loss value includes the coupling losses for the input and the respective output ports, and the losses due to all the waveguide components in the respective optical paths. The optimisation of the waveguide components along the optical paths [43, 44] has lead to significant total loss reductions in the modules. The main loss component that has been reduced through the optimisation process is the excess loss of the combiners along the main bus. It can also be noted that the VCSEL launch results in slightly larger total and insertion loss values for all paths due to the higher coupling losses (no index-matching gel used at the waveguide input) and the higher excess losses at the various waveguide components due to the larger percentage of power coupled to higher order modes at the waveguide inputs.

The crosstalk induced at the other bus outputs is assessed by recording the power received at the other bus outputs for each input port (Fig. 7). The largest crosstalk values are found to be approximately -30 dB with respect to the launched input power and are recorded for opposite-located transmitter and receiver arrays (Fig. 7c). Assuming a worst-case received signal of -13 dB, the obtained signal-to-crosstalk ratio is > 17 dB for all on-board paths. Given however, than only one transmitter (Tx)

Fig. 7. Crosstalk in the 4-channel 3-card polymeric bus module when a (a) 50 μm MMF and a (b) butt-coupled 1 $\times$ 4 VCSEL array are employed. (c) Illustration of the worst-case crosstalk.

should operate at any time in the optical bus architecture (neglecting transmission collisions), only intra-channel crosstalk is relevant to the normal bus operation. Intra-channel crosstalk is hence assessed by examining the crosstalk induced at the bus outputs due to the operation of all the other waveguide channels on the same Tx input array. For each on-board optical link the intra-channel signal-to-crosstalk ratio is calculated for each channel by taking into account the respective received signal power and induced crosstalk when light is simultaneously launched at all four bus inputs on the same Tx array. Table I shows the calculated intra-channel signal-to-crosstalk ratio for all on-board links when a butt-coupled 1 $\times$ 4 VCSEL array is used at the Tx input and a launched optical power of 0 dBm is assumed for all 4 input channels. The large majority of the on-board links exhibit an intra-channel signal-to-crosstalk ratio larger than 30 dB, while the lowest obtained value is found to be $\sim$ 29 dB for channel 2 of the Tx_{3R}-Rx₁ link.

TABLE I. INTRA-CHANNEL SIGNAL-TO-CROSSTALK RATIO (dB) FOR ALL ON-BOARD LINKS WHEN A 1 $\times$ 4 VCSEL ARRAY IS USED AT EACH Tx INPUT.

Link	Ch. 1	Ch. 2	Ch. 3	Ch. 4
Tx ₁ -Rx ₂	34.4	32.2	34.3	34.7
Tx ₁ -Rx ₃	36.5	35.4	37.1	37.7
Tx ₁ -Rx _{3R}	38.5	34.8	40.3	39.3
Tx ₂ -Rx ₃	34.6	32.2	35.7	36.4
Tx ₂ -Rx _{3R}	35.1	31.6	36.1	39.2
Tx ₃ -Rx _{3R}	36.8	32.5	37.4	35.7
Tx _{3R} -Rx ₁	36.5	28.6	33.7	33.3
Tx _{3R} -Rx ₂	31.9	33.3	35.5	33.9
Tx _{3R} -Rx ₃	36.8	33.7	34.3	36.2
Tx _{3R} -Rx _{3R}	38.6	34.7	35.7	37.6

The robustness of the power splitting function of the optimised optical bus to input misalignments is also studied. Given the requirement for relaxed alignment tolerances and the use of low-cost assembly methods, it is important to ensure that the power splitting characteristics of the optical bus are not significantly affected by the position of the input. The power received at all respective outputs for some of the input ports is recorded as the input position is offset in both transverse directions. Fig. 8 shows the normalised received power at all respective bus outputs for the regenerator input 1 (Tx_{3R}) and the card input 6 (Tx₁) when a 50 μm MMF input is used. It can be noticed that the power splitting characteristics of the optical bus are not significantly affected by the launch position for either the regenerator or card input ports. Moreover, 1 dB alignment tolerances of approximately $\pm$ 10 μm are obtained in both transverse directions.

IV. OPTICAL BACKPLANE DEMONSTRATOR

An optical backplane demonstrator based on the use of the optimised polymeric bus modules is formed. Different system implementations can be produced depending on the location of the active optoelectronic devices (lasers and photodiodes) and their respective driving circuits. The interface between the optical backplane and the electrical cards can be achieved either with optical connections at the backplane's input/output ports, assuming that the optical transceivers reside on the electrical cards, or with short high-speed electrical connections assuming that the optical transceivers are fitted onto the backplane. The use of optical connections offers clear performance advantages enabling the positioning of the optical transceivers in close proximity to the high-performance electronic chips on the cards but requires the development of suitable low-cost pluggable optical connectorisation schemes. Various such schemes have been proposed in recent years based on the use of either

Fig. 8. Normalised received power at all respective bus output for bus input: (a-b) port 1 (ch.1, Tx_{3R}) and (c-d) port 6 (ch2, Tx_1) as a function of the position of the 50 μm MMF input in the horizontal, (a) and (c), and vertical, (b) and (d), directions.

MT-based ribbon fibres or flexible connectors [48–51], butt-coupled VCSEL sources [26, 27, 52] or beam-turning elements to achieve a direct interface with the active components that reside on the electrical cards [53, 54]. The beam-turning elements which typically consist of 45° micro-mirror structures can either be formed directly in the optical layer of the backplane [55, 56] or be integrated in a discrete optical connector that is mounted appropriately onto the backplane [57, 58]. On the other hand, pluggable electrical connections between the backplane and electrical cards are easier to implement and can provide a short-term alternative until the use of optical connectors for such applications is standardised. For the demonstration purposes of this work, the optoelectronic active devices and their respective driving circuits are chosen to reside on the backplane. As a result, the fabricated polymeric bus modules are interfaced with appropriately-designed electrical driving boards to form opto-electronic (OE) bus modules. Two similar OE bus modules are connected through a prototype 3R regenerator unit to form an optical backplane demonstrator (Fig. 9). In the sections that follow, the electrical layer of the OE bus modules is presented as well as the 3R regenerator unit. Details of the fabrication and assembly of the demonstrator are also reported.

Fig. 9. Schematic of the implemented optical backplane demonstrator.

A. OE bus modules

The optical layer of the OE bus modules consists of the 4-channel 3-card polymeric bus repeating units presented in the previous section, while their electrical layer comprises the electronic circuits to drive the 1×4 VCSEL and PD arrays and therefore, transmit and receive the I/O data signals over the optical bus. The design and fabrication of the opto-electronic

(OE) bus modules are based on the integration method described in [28]. The optical layer of the board resides on one of the board surfaces while the electronic circuitry is located on the other side of the board. The interface between the optical and electrical layers of the board is achieved with OE connectors that carry the active components and are fitted in appropriately-located through-board slots to enable end-fire optical coupling into and out of the polymer waveguides. The end-fire optical coupling scheme is intrinsically simpler to implement as it does not require the formation of any beam-turning elements in the optical layer.

1) Electrical layer

The electrical layout of OE bus modules is designed for 0.5-mm thick FR4 boards. 4-channel 12.5 Gb/s VCSEL driving and transimpedance amplifier (TIA) integrated circuits (ICs) in die form, IPVD12G011 and IPTA12G011 respectively, provided by IPtronics are employed at each Tx and Rx card interface of the backplane. The ICs take differential input data signals and generate differential data signal outputs, and are controlled through digital serial management (SPI) interfaces allowing independent control of the operating point of each VCSEL and PD on the 1×4 array. The data I/Os of the ICs are connected to surface-mounted (SMA) connectors through impedance matched co-planar microwave transmission lines. Each IC features a separate voltage regulation circuitry, a dedicated edge-mounted SMA connector to attach a separate power supply, and a pin connector to feed the SPI control signals to the chip. Due to the large number of SMA connections for each Tx and Rx card interface (8 data I/Os per driving Tx/Rx IC) and the limited space of the bus repeating unit (90×50 mm²), the designed electrical layer of the OE bus modules comprises the electronic circuitry for two out of the three card interfaces: Tx_1/Rx_1 for card #1, and Tx_3/Rx_3 for card #3. Fig. 10 shows the layout of the top copper electrical layer of the OE bus modules with some details of the board design noted.

Fig. 10. Layout of the top copper electrical layer of the OE bus modules with inset images of the areas of the VCSEL and PD driving chips and details noted.

2) OE connectors

Simple L-shaped OE connectors which carry the 1×4 VCSEL and PD arrays are employed to interface the optical layer of the OE bus modules with their electrical layer. These OE connectors, described in greater detail in [28], are micro-machined with a PCB prototyping machine from 1.3 mm-thick Duroid substrates (Duroid 5880LZ) with a low dielectric constant $\epsilon_r = 2$ and a loss tangent δ of 0.002, and carry appropriately positioned pads to mount the active devices and short copper tracks to connect them to the electrical layer of the board (Fig. 11a). The dimensions of the OE connectors used are $7.3 \times 5.2 \times 1.3 \text{ mm}^3$ for the Rx connector and $5.6 \times 5.0 \times 1.3 \text{ mm}^3$ for the Tx connector. The employed width and pitch of the tracks on the connectors is $180 \mu\text{m}$ and matches the copper traces used at the IC's I/O interfaces. The short copper traces on the board from the ICs to the OE connectors as well as the traces on the OE connector are not impedance-matched and therefore are kept as short as possible to minimise signal degradation and electrical crosstalk. The longest trace on the OE connectors is approximately 3 mm in length while the connecting traces on the boards are 1 mm long. RF simulations carried out with the Agilent ADS software indicate that the frequency response of these OE connectors has a large enough 3 dB bandwidth for the transmission of 10 Gb/s data signals (Fig. 11b and Fig. 11c). Due to the symmetry of the Tx connector, similar frequency response is obtained for channels 1 and 4 with a 3dB frequency of $\sim 13 \text{ GHz}$ and for channels 2 and 3 with a 3dB frequency of $\sim 15 \text{ GHz}$. For the Rx connector, the obtained 3dB frequencies for the 4 channels are $\sim 9 \text{ GHz}$, 15 GHz , 8.5 GHz and 10 GHz respectively. The difference in bandwidth is due to the asymmetry in the connector layout with respect to the data tracks.

Fig. 11 (a) Layout of OE connectors with dimensions noted and simulated S21 parameters for the (b) Rx and (c) Tx connector. (d) Photograph of realised OE connector on Duroid substrates and (e) schematic of the board cross section illustrating the end-fire optical coupling scheme.

1×4 10 Gb/s VCSEL (ULM850-10-TN-N0104U) and PD (ULMPIN-10-TT-N0104U) arrays in die form are mounted on the OE connectors and wire-bonded to the copper tracks. For the demonstrator purposes, additional connection pads that are compatible with a customised pick-and-place assembly tool are also incorporated onto the connector design. These electrical pads enable active optical alignment of the OE connectors with the on-board polymer waveguides minimising therefore the probability of misplaced connectors during the modules' assembly. The connection pads are used to power up the first and last VCSEL/PD on the 1×4 array and ensure sufficiently small angular misalignment between the array of waveguides at the bus modules I/O ports and the device array. Each connector is fitted in a through-board slot located in close proximity to the respective driving chip, positioning the active devices directly opposite the input/output facets of the optical waveguides, enabling therefore end-fired optical coupling. The active

devices are mounted onto the OE connectors in a way so that the wire bonds protrude over the optical layer of the boards enabling therefore butt-coupling of the active devices very close to the waveguide facets without damaging the wire bonds. Moreover, the use of a small gap between the active devices and the waveguide facets facilitates the electrical connection of the OE connectors to the copper traces on the electrical layer of the board. The gap that needs to be bridged between them is slightly larger than the thickness of the optoelectronic dies ($\sim 150 \mu\text{m}$). Photographs of the realised artefacts are shown in Fig. 11d while Fig. 11e depicts a schematic of the cross section of the assembled board with an OE connector fitted.

3) OE bus modules' fabrication and assembly

Due to the complexity of the electronic circuitry on the OE bus modules and the limited resources available (electronic ICs, polymer materials), the fabrication of the optical and electrical layers of the OE bus modules is chosen to be decoupled from each other for the purposes of the demonstration described here. In that way, any issues that might arise during the production and assembly of one layer of the OE boards (electrical or optical) would not require the complete reproduction of the other layer. As a result, the polymeric bus repeating units and the electrical layouts of the OE bus modules are produced on separate 0.5 mm thick FR4 substrates, tested independently to ensure operation of all on-board optical paths within the optical power budget and good electrical connections respectively, and are then assembled together and interfaced through the OE connectors.

The electrical layouts of OE bus modules are produced on 0.5 mm-thick FR4 substrates with the PCB prototyping machine and measure $90 \times 110 \text{ mm}^2$. Electroless nickel immersion gold (ENIG) surface finishing is applied to the boards to facilitate the wire bonding of the VCSEL and PD driving chips. Appropriately-positioned through-board slots are produced with the same PCB prototyping machine. Two 4-channel VCSEL and PD driver ICs are mounted onto each OE board using non-conductive adhesives and are electrically connected to the board with a wire bonder and a gold wire of $25 \mu\text{m}$ in diameter. Each chip requires approximately 80 wires bonds to connect all electrical pads, yielding a number of total required wire bonds per OE bus module of ~ 320 .

Two 4-channel 3-card polymeric bus units are produced on 0.5 mm-thick FR4 substrates with standard photolithographic processes. The insertion losses of all on-board optical paths are measured to ensure the proper operation of the electrical layer. All on-board optical paths for both modules exhibit insertion losses within the 15 dB target power budget.

The electrical and optical layers of the OE bus modules are aligned using visual markers on the substrates and clamped together using metallic clamps and common adhesives. The OE connectors are mounted onto the boards using a customised pick-and-place tool and active optical alignment. Active alignment of the OE connectors is essential in the assembly of these modules due to the limited accuracy in the manual alignment of their electrical and optical layers and the

production of the OE connectors with the CNC milling machine. The direct fabrication of the optical layer on patterned PCBs, as in [28], would enable precise alignment of the two layers during waveguide fabrication with the high positioning accuracy of the mask alignment process, while the use high-precision micro-machined OE connectors or moulded connectors would provide increased accuracy in the modules' assembly. The active alignment of the OE connectors during the board assembly is enabled by appropriate connection pads located on their back side (Fig. 11a) and customised pick-and-place tools. Two out of the four VCSELs and PDs on each array are powered up during the alignment process ensuring sufficiently good alignment with the waveguides. The connectors are then secured in place with common adhesive while the received power levels are monitored during the curing phase. Some performance degradation is noticed during the curing process and connector release as expected, but the changes are not significant (maximum change observed $\sim 10\%$). The gap between the active devices (VCSEL or PD array) and the optical waveguides are on the order of $50 \mu\text{m}$. The electrical connection of the OE connectors is achieved with conductive epoxy applied between the traces on the connectors and the board (Fig. 11e). Photographs of the OE module during the assembly are shown in Fig. 12.

Fig. 12. Photographs of an OE bus module during assembly with some features noted: (a) planar view of the module with the optical and electrical layers put together, (b) top view of the electrical layer, (c) top view of the optical layer with 3 out of 4 OE connectors mounted and (d) underside view of the assembled OE module with the polymer waveguides on the optical layer slightly apparent.

B. 3R Regenerator unit

The 3R generator unit comprises 4-channel Rx and Tx optical transceiver units connected back-to-back via clock and data recovery (CDR) ICs. The Rx and Tx parts of the regenerator unit are designed and fabricated on separate 0.5 mm thick FR4 substrates and then put together and electrically connected through plated-through vias. 4-channel 12.5 Gb/s VCSEL and PD driver ICs from IPtronics, same as the ones used for the OE bus modules, are employed for the 3R regenerator unit. Here, the 1×4 active devices are mounted directly onto the FR4 substrate and connected to the ICs in die form with gold wire

bonds. The received data signals from the Rx_{3R} on the 3R unit are connected to the signal conditioning electronic chips and, after regeneration, are fed to the inputs of the Tx_{3R} optical transmitter. In this work, the commercially-available Gennum GN2405A (Quad 10 Gb/s CDR with Input Equalizer & Transmit De-Emphasis) and GN2406 (Quad 10 Gb/s CDR with Transmit De-Emphasis) chips are used to regenerate the received data signals from the optical bus and re-transmit them onto the next bus segment. The signal conditioning ICs are controlled through an I²C control interface and programmed through pin connectors. A schematic of the core parts of the electrical layout of the 3R regenerator and a photograph of the realised unit are shown in Fig. 13.

Fig. 13. (a) Schematic of the 3R regenerator unit, (b) electrical layouts of the core part of the unit with some details noted and (c) photograph of the transmitter side Tx_{3R} of the realised unit.

C. Optical backplane demonstrator

The optical backplane demonstrator comprises two similar OE bus repeating units interconnected via the 3R regenerator

unit (Fig. 9). The active devices on the regenerator unit (1x4 VCSEL and PD arrays) are butt-coupled with the respective input and output ports of the OE bus modules. To facilitate the interface of the 3R regenerator unit with the OE bus modules appropriately-positioned MT-compatible holes are included in the electrical layout and produced with the PCB prototyping machine (Fig. 13). Although not used in the assembly of the demonstrator presented here, these holes can enable passive MT-compatible connectorisation schemes similar to the ones proposed and demonstrated in [27], facilitating therefore the optical alignment between the regenerator unit and the polymeric bus repeating units. Photographs of the overall system and details of the interface between the polymeric bus modules and the 3R regeneration unit are shown in Fig. 14.

V. DATA TRANSMISSION EXPERIMENTS

The operation of the OE bus modules and the 3R regenerator unit is controlled with two desktop PCs enabling the independent control of all VCSELs and PDs on the backplane demonstrator system. A bit-error-rate (BER) test set (Anritsu MP1763C) and a digital communication analyser (HP83480A) are used to assess the data transmission performance of the optical backplane demonstrator. High-bandwidth RF cables are used to feed the input data signals from the pattern generator to the OE bus modules and deliver the output data signals to the test instruments. All backplane links are tested under two operating conditions: when all other channels (transmitting VCSELs and receiving PDs) on the same transmitter (Tx) and receiver (Rx) array as well as the respective ones on the regenerator unit (Tx_{3R} and Rx_{3R}) are: (i) switched off, and (ii) are operating under dc bias conditions (CW light transmitted through the optical paths but without any data). The former allows independently testing all on-board links while the latter assesses the transmission degradation due to optical and electrical crosstalk in the Tx and Rx arrays on the backplane. The operating condition for each VCSEL on the backplane is controlled via the driving ICs and is optimised to achieve best

Fig. 14. Photographs of realised optical backplane demonstrator: (a) top view and (b) planar view with inset images showing the interface between the OE modules and the 3R regenerator unit at the boards' underside. Note the reflection of the electronic components on the polymer layer of the OE modules. The 1x4 PD array is illuminated with red light incident from the 4 waveguides of the output port Rx_{3R} of the OE bus module 1.

high-speed performance. Bias currents in the range of 6 to 9 mA and modulation currents between 5 and 8 mA are typically used. For all data transmission experiments, 10 Gb/s 2⁷-1 pseudo-random binary data signals (PRBS) are employed in order to emulate the short codes typically used in datacommunication links (e.g. 8B10B). The operating conditions of the VCSEL (bias and modulation current, pre-emphasis) are optimised for each link in order to achieve best performance.

Fig. 15 summarises the results obtained for all backplane links showing the received 10 Gb/s eye diagrams for each interconnection path under both test conditions. Error-free (BER<10⁻¹²) operation is achieved from all on-board links for both operating conditions, while open eye diagrams are recorded. Channels 1 and 4 exhibit the worst performance for all Tx-Rx combinations as these links exhibit the highest optical losses (Fig. 5) and feature the longest non-matched transmission lines on the OE connectors and the longest bond wire connections between the driving ICs and active devices.. The simultaneous operation of the entire VCSEL and PD array results in a degradation in the quality of received data signals as it can be observed from the eye diagrams in Fig. 15. The eyes exhibit a slightly reduced eye opening, increased jitter and noise. Optimisation of the RF design of the OE connectors can minimise electrical crosstalk while improvements in the assembly and alignment of the OE connectors can reduce background scattered noise and crosstalk due to non-optimum optical coupling. Finally, it should be noted that the link connection on channel 1 for the Tx₄-Rx₆ link on the 2nd bus module was proven to be problematic due to the position of the respective input SMA connectors very close to the board edge (Fig. 14, rightmost SMA connectors on the 2nd module), resulting in poorer recorded eye diagrams for this channel (Fig. 15). The connection of the RF cables very close to the board edge induced mechanical stress on the board resulting in link performance degradation. Nevertheless, error-free operation of the link could still be achieved by using appropriate mechanical support for the RF connection cables.

The power consumption of this backplane demonstrator formed with commercially-available electronic and photonic components is evaluated. Each 4-channel VCSEL and PD driver IC consumes 225 mW and 320 mW respectively, resulting in a total power consumption for each card of 545 mW. The 3R regenerator unit consumes approximately 1.8 W when operating in full capacity: ~0.55 W for the 4-channel VCSEL and PD drivers and ~1.25W for the CDR chips. The total power consumption for each card is therefore 545 mW+1800/3 mW =1145 mW which provides a 40 Gb/s interconnection capability. As a result, a figure of merit of 28.6 mW/Gb/s is achieved for each card on the backplane for each communication direction. The full optical bus would require a doubled power consumption of 56.2 mW/Gb/s per card to enable optical interconnection in both directions. Although a direct comparison is not straightforward, current commercially-available 10-GbE serial transceivers for electrical backplanes (10GBASE-KR) exhibit power consumptions of ~120 mW/Gb/s [59]. The power consumption of the optical backplane demonstrator can be significantly reduced if state-of-the-art VCSEL and PD drivers and CDR chips are used instead of the commercially-available components. VCSEL and PD drivers with full link power consumption of 2 mW/Gb/s at 10 Gb/s have been reported [60] while various 10 Gb/s CDR chips with power consumptions between 70 and 120 mW per channel have been demonstrated [61-64].

VI. DISCUSSION

Some points regarding the employed interconnection architecture and operation of the optical bus modules are briefly discussed in the following sections.

A. Broadcast architectures vs point-to-point links

Bus architectures have been traditionally used in applications where communication is characterised by short bursts, during which high throughput is required (e.g. in data storage systems). When compared with point-to-point architectures, broadcast

INPUT \ OUTPUT		Tx ₁				Tx ₃				Tx ₄			
		Ch. 1	Ch. 2	Ch. 3	Ch. 4	Ch. 1	Ch. 2	Ch. 3	Ch. 4	Ch. 1	Ch. 2	Ch. 3	Ch. 4
Rx ₃	ONLY												
	ALL ON												
Rx ₄	ONLY												
	ALL ON												
Rx ₆	ONLY												
	ALL ON												

Fig. 15. Received 10 Gb/s eye diagrams for all optical links on the backplane demonstrator when all other channels on the same Tx and Rx array as well as on the Tx_{3R} and Rx_{3R} arrays are turned off (ONLY) and when operating (ALL ON) under DC bias conditions (CW light transmitted but no data).

systems require a smaller number of optoelectronic components and electronic driving circuits which scale with the number N of connected entities (rather than N^2 for point-to-point architectures) and therefore require less space and, in some cases, might provide power consumption advantages. Moreover, broadcast systems can be readily expanded by concatenating bus segments whereas in point-to-points the backplane system needs to be replaced by a larger one. On the other hand, interconnection architectures based on point-to-point systems are intrinsically simpler to implement and do not require any control algorithms to handle transmission collisions. Significant work on optical backplanes based on point-to-point links has been reported in recent years [31, 32, 34, 35]. The work presented herein, provides an interesting alternative which features complex multimode optical paths and can be produced with low-cost optoelectronic components and standard fabrication methods.

B. Optical bus limitations and bus upgrade

Link studies presented in [38] indicate the maximum number N of cards that can be connected onto each bus module as a function of the optical losses in each bus segment. The use of regenerators enables however the concatenation of multiple bus segments and therefore the connection of large number of cards onto the bus. The specific bus modules presented in this paper are designed for 10 Gb/s operation with a 15 dB power budget. The number of cards N that can be accommodated on each bus module can be increased by increasing the available optical power budget or by reducing the component losses along the optical paths. Towards this direction, work on 90° waveguide bends with improved performance has been recently reported and the benefit of their use in an optical bus configuration has been demonstrated [65]. Higher aggregate data rates on the optical bus can be readily achieved by increasing the number of parallel waveguide channels on each bus module as shown in Fig. 2 (e.g. 12×10 Gb/s channels for a 120 Gb/s bus). As indicated in section II, the employed waveguide layout is scalable to larger numbers of channels, which would only result in a slightly larger number of crossings in each channel (loss of 0.1 dB/crossing [42, 43]). A direct increase in the data rate on each waveguide channel (e.g. from 10 Gb/s to 25 Gb/s) is not applicable as the waveguide layout needs to be re-designed to satisfy the reduced power budget requirements. Alternative waveguide designs (e.g. single mode waveguides), waveguide components (e.g. lower loss splitters/combiners) or interconnection architectures (e.g. point-to-point links) are therefore required in this case.

C. Modal noise

The use of multimode waveguides in optical backplanes raises the important issue of modal noise which exists in general in any multimode waveguide system. The phenomenon however has not yet been fully studied and understood in short-reach polymer waveguide links. It can be argued though, that modal noise becomes a more significant issue when a relatively small set of modes is excited in the waveguides while a point of mode

selective loss exists in the system. The higher the number of modes excited at the waveguide input, the smaller the effect is. In the case of the systems studied here, the highly-multimoded nature of the guides (large step-index difference), the relatively large number of waveguide modes excited at the waveguide inputs due to the multimode sources used (VCSELs, MMF) suggest that the effect should not be severe. The effect has not been properly studied for the complex optical paths reported here and therefore no clear conclusions can be drawn. Initial theoretical and experimental work on straight polymer waveguides indicate that modal noise in such systems should not be as important as in fibre-based links [66], [67].

The use of the multimode power splitters along the optical paths raises however further concerns regarding the mode selective loss in these components and therefore potential modal noise issues. The robustness of the splitting performance with respect to input position is demonstrated both through the component studies reported in [42] and [44], and through the reported studies on the bus modules. The variation of the received power at the bus outputs as function of the input position for the initial bus module has been reported in [38], while for the optimised bus module is reported here in section III (Fig. 8). The use of the bent sections before the splitters (90° bends for Tx inputs and S-bends for 3R inputs) as well as the gradual increase in the branch separation along the splitter devices, ensures that the power splitting at the outputs does not significantly vary with small changes in input position ($< \pm 10 \mu\text{m}$). A rigorous investigation on modal noise and the effect induced due to the presence of the splitters are however essential to reach safe conclusions on its magnitude and importance in this multimode waveguide system.

VII. CONCLUSIONS

Optical technologies based on polymer multimode waveguides are an attractive candidate for the formation of cost-effective high-capacity next-generation backplanes. Shared-based architectures can enable interconnection in applications where the number of connected entities is variable and communication with short-bursts but high-throughput is required. A 4-channel optical backplane demonstrator is designed based on a regenerative optical architecture and PCB-integrated polymer waveguides, and fabricated with low-cost commercially-available electronic and photonic components. This proof-of-principle demonstrator comprises 2 OE polymeric bus modules and a prototype 3R regenerator unit, all formed on low-cost FR4 substrates. The optical layer of the polymeric bus modules comprises a scalable multi-channel waveguide layout which is compatible with the use of VCSEL and PD arrays and ribbon fibres at the bus I/O ports. The electrical layer of the OE bus modules comprises 4-channel driver ICs at each card interface as well as the required control and power regulation circuitry. The interface between the optical and electrical layers of the OE bus modules is achieved with simple OE connectors that carry the VCSEL and PD arrays and are mounted on appropriately-positioned through-board slots. The optical backplane achieves error-free (BER<10⁻¹²)

4×10 Gb/s interconnection between any two card interfaces on the bus while enables bus extension and therefore, connection of an arbitrary number of cards to the bus, by concatenating multiple bus segments via 3R regeneration units that operate as “bridges”. The formation of this demonstrator system with commercially-available components and onto low-cost substrates demonstrates the potential of this technology in real-world systems.

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