TFT Small Signal Model and Analysis

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***Abstract*—We present an accurate small signal model for thin film transistors (TFTs) taking into account non-idealities such as contact resistance, parasitic capacitance, and threshold voltage shift. The model gives high accuracy in s-parameters, and the predicted cutoff frequency yields 1% discrepancy compared with measurement results. In contrast, the conventional CMOS small signal model adapted for TFTs yields 12.5% error. The TFT's cutoff frequency is also evaluated under bias stress to examine the effect of device instability on small signal behavior.**

***Index Terms*—Small signal model, s-parameter, thin film transistor (TFT), cutoff frequency, threshold voltage (V_T) shift**

I. Introduction

Small signal modeling simplifies the analysis of non-linear devices, in which the signal in question is treated as a small perturbation around the bias point [1]–[3]. The resulting linear approximation reduces design complexity of circuits such as amplifiers [4]–[9]. When compared to MOSFETs, TFTs have a different structure and unique material properties, which result in, for example, larger contact resistance, high parasitic capacitance, and stress-induced V_T shift [10]–[20]. This is true for a-Si:H [10]–[12], organic [13]–[17] and metal-oxide [18]–[20] TFTs alike. Therefore, it is imperative that these non-idealities be captured in the small signal model. This is especially crucial in TFT-based analog circuit design and in particular, for the accurate prediction of the circuit's dynamic behavior.

In this letter, we present an accurate TFT small signal model where the contact resistance (R_C), parasitic capacitance, and stress induced threshold voltage (V_T) shift are considered. The small signal behavior is analyzed through measurements of S-parameters, current-voltage (I-V) and capacitance-voltage (C-V) characteristics, and bias-induced instability. From these measurements, we assess if the MOSFET's small signal model is adequate or examine the modifications needed for TFTs using a-InGaZnO (IGZO) test TFT structures.

II. Theoretical Analysis

The TFT structure examined here and equivalent passive components are shown in Fig. 1(a), in which the transistor is working in the saturation regime, where the bias conditions follow $V_{DS}>V_{GS}>V_T$. The shaded region indicates the formed channel and pinch-off happens at the edge adjacent to the drain electrode. As illustrated, the channel capacitance only contributes to the source side since the drain side is pinched off. The corresponding small signal equivalent circuit model is shown in Fig. 2(b), where the contact resistances and overlap capacitances are connected. The working channel in saturation is then represented by a voltage controlled current source in parallel with an output resistance (r_o), which is supported by Thévenin's theorem [21], [22] since other capacitance or inductance effects are negligible.

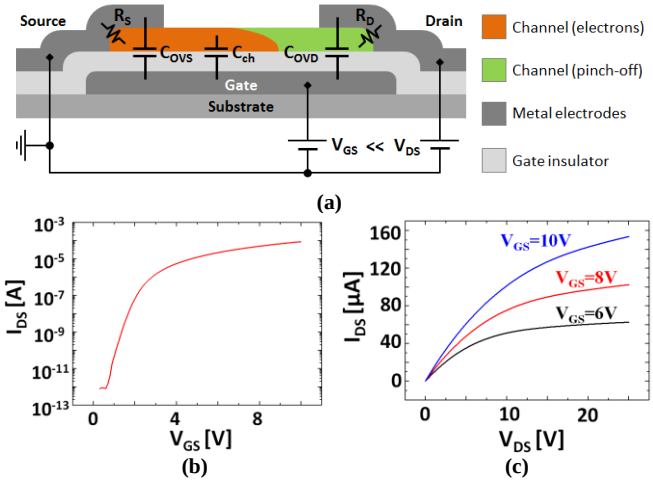

Fig. 1. (a) Bottom gate TFT structure and equivalent passive components, where C_{ch} is the channel capacitance, $C_{OVS/OVD}$ the overlap capacitance at source/drain side, $R_{S/D}$ the contact resistance at source/drain side. (b) Transfer characteristics (c) output characteristic of the TFT under test. Test structures used for model synthesis were IGZO TFTs reported in [23], [26]. The device under test has following physical and geometrical parameters: t_s=50nm, V_T=1.6V, C_{OX}=30nF/cm^2, μ=8.6cm^2/Vs

This approach takes a different path from the CMOS small signal model (see also Fig. 2). In particular, the contact resistance separates the channel capacitor (C_{ch}) and the overlap capacitor at the source side (C_{OVS}), which would yield a different frequency response, especially for the S_{11} parameter. In addition, the transconductance (g_m) in the TFT model seen in Fig. 2(b) is no longer in linear operation as a function of the bias voltage. Note that the connection of contact resistance and C_{ch} are also valid for other material families and device structures.

A. Small signal model at low frequency

At very low frequencies, all the parasitic capacitances and channel capacitances can electrically be treated as open-circuit connections. This is valid when the frequency of concern is much smaller than the first pole of the frequency response (i.e.$f \ll f_p \approx 1/2\pi R_L C_{OVD}$, where R_L is the load resistance connected at the drain of the TFT, assuming no parasitic at input). In this frequency regime, the TFT model can be

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equivalent to the CMOS model omitting all the capacitors according to Thévenin's theorem. Note that the g_m and r_o in Fig. 2(a) can be calculated directly from the derivative of the measured drain current vs. gate-source voltage (i.e. I_D-V_{GS}) and drain current vs. drain-source voltage (i.e. I_D-V_{DS}) curves, respectively, while g_{mi} and an internal output resistance (r_{oi}) cannot be obtained directly from the static behavior. As both models should capture the same derivatives of the static behavior, the expressions for g_{mi} and r_{oi} as a function of measurable parameters can be derived as follows:

$$g_{mi} = \frac{g_m r_o}{r_o - g_m r_o R_C - 2R_C} \quad (1)$$

$$r_{oi} = r_o - g_m r_o R_C - 2R_C \quad (2)$$

Here, R_C=R_D=R_S, assuming the contact properties at source and drain sides are symmetrical.

According to the static models developed in [23] based on the same set of samples, the internal g_{mi} (Fig. 2(b)) considering V_T shift can be expressed as:

$$\begin{aligned} g_{mi} &= K\frac{W}{L}(V_{GA} - V_T - \Delta V_T)^{\alpha+1} \\ &\approx K\frac{W}{L}(V_{GA} - V_T)^{\alpha+1} - K\frac{W}{L}(\alpha+1)(V_{GA} - V_T)^{\alpha}\Delta V_T \\ &= g_{mi0} - K'\Delta V_T \end{aligned} \quad (3)$$

where g_{mi0} is the initial value without any V_T shift, $K' = K(W/L)(\alpha+1)(V_{GA} - V_T)^{\alpha}$, as α is a constant close to zero, K' is weakly dependent on bias and can be treated as a constant. The $|\Delta V_T|$ can be represented with the following stretched exponential functions for stress and recovery stages, respectively, as $|\Delta V_T| = (V_{GS} - V_T)\left(1 - exp\left(-(t/\tau_S)^{\beta_S}\right)\right)$ and $|\Delta V_T| = \Delta V_{Tst}\, exp\left(-(t/\tau_R)^{\beta_R}\right)$ [10], [18]. Here, ΔV_{Tst} is the initial value of ΔV_T at the start of recovery stage, τ_S and τ_R are time constants for stress and recovery stages, respectively, and β_S and β_R are exponents for stress and recovery stages, respectively. These parameters are different relating to stress conditions, such as bias stress and illumination stress [10], [18], [24]. The assumption of $\Delta V_T << V_{GS}$-V_T is used in the approximation of Eq. (3).

The derivation above shows that the V_T shift can be represented by a separate component. The corresponding small-signal model is shown in Fig. 2(b).

B. Small signal model at high frequency

At higher frequencies, capacitance effects are no longer negligible (i.e. when the low frequency assumption in the above section is violated), and the small signal model becomes different from the CMOS counterpart. This means that the two models in Fig.2 should give different cut-off frequencies and different bode-plots for the current gain (H_{21}).

The short circuit current gain (A_i) calculated from the CMOS model in Fig.2(a) is represented as,

$$\boldsymbol{A_i} = \frac{sC_{OVD} - g_m}{s(C_{OVD} + C_{OVS} + C_{ch})}. \quad (4)$$

In the bode plot for Eq.(4), there should be one pole and zero. And the cutoff frequency (f_T) is then approximated by assuming that the zero of g_m/C_{OVD} is far from the point of the cutoff frequency. Thus,

$$\boldsymbol{f_T} = \frac{g_m}{2\pi(C_{OVD} + C_{OVS} + C_{ch})} = \frac{g_m}{2\pi C_{tot}}, \quad (5)$$

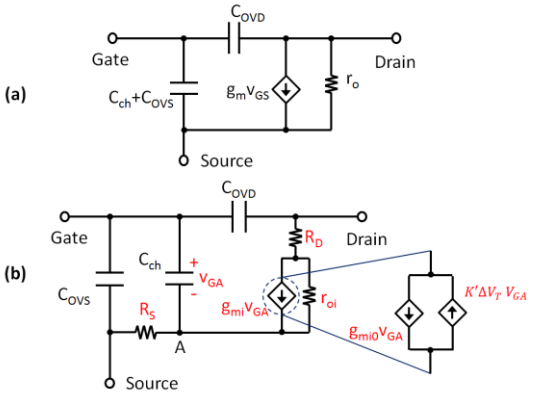

Fig. 2. (a) CMOS small signal model and (b) TFT model. Here, V_{GA} is the voltage difference between gate and the node 'A', where $V_{GA} = V_{GS} - I_{DS}R_S$

where C_{tot} is the sum of all capacitances of the transistor.

In contrast, the current gain calculated for the TFT small signal model seen in Fig.2(b) is

$$\boldsymbol{A_i} = \frac{-g_{mi}r_{o1} + ((2R_C + r_{oi} + g_{mi}R_C r_{oi})C_{OVD} + C_{ch}R_C)s + C_{OVD}C_{ch}R_C(R_C + r_{oi})\,s^2}{s(g_{mi}C_{OV}\,R_C r_{oi} + (2R_C + r_{oi})\,(C_{OV} + C_{ch}) + C_{OV}(R_C + r_{oi})C_{ch}\,s)} \quad (6)$$

where $C_{OV} = C_{OVS} + C_{OVD}$. Therefore the cut-off frequency is:

$$\boldsymbol{f_T} = \frac{g_{mi}r_{oi}}{2\pi(g_{mi}C_{OV}R_C r_{oi} + (2R_C + r_{oi})(C_{OV} + C_{ch}))} = \frac{g_m}{2\pi(C_{tot} - g_m R_C C_{ch})} \quad (7)$$

From Eqs.(5) and (7), we can clearly see that the major difference between Figs.2(a) and (b) comes from the term $g_m R_C C_{ch}$. This implies that this difference depends on the value of R_C and the fraction C_{ch} is of the total capacitance. Note that C_{ch} is related to both free and trapped charges associated with the degree of disorder in the channel layer [25], [26]. This also indicates that the CMOS model can be inaccurate especially when the contact resistance and overlap capacitance are big and small, respectively.

III. Results and Discussions

The s-parameters are measured using the Keysight E5061B network analyzer calibrated by CS-11 calibration substrate provided by GGB Industries, Inc. The DC bias is at V_{GS}=8V and and V_{DS}=15V. The cut-off frequency extracted from the converted H_{21} parameter yields the result shown in Fig. 3. The extracted device parameters used here are as follows: g_m=16.5 μS, C_{ch}=0.2 pF, C_{OVD}=C_{OVS}=0.43 pF, r_o=1.4MΩ, R_C=30kΩ. The $C_{OVD/S}$> C_{ch} due to a longer overlap length than the channel and the value of g_m mentioned above is extracted from S21 directly, which is consistent with that of g_m from a static I-V measurement (~16.4μS).

The measurement results show a cutoff frequency of 3.11MHz while the proposed TFT and CMOS models predict cutoff frequencies of 3.14MHz and 2.72MHz, respectively. This yields an error of 1% and 12.5%, respectively.

Note that H_{21} can be calculated from all four s-parameters using the following relation,

$$\mathbf{H_{21}} = -\frac{2\,S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}\,S_{21}}. \quad (8)$$

However, since the TFT is very resistive in s-parameter measurements, Eq.(8) can be approximated as,

$$|\mathbf{H_{21}}| \approx \left|\frac{S_{21}}{S_{11} - 1}\right|. \quad (9)$$

Therefore, the frequency response of the TFT is dominated by the S_{11} and S_{21}. The measurement and computational results

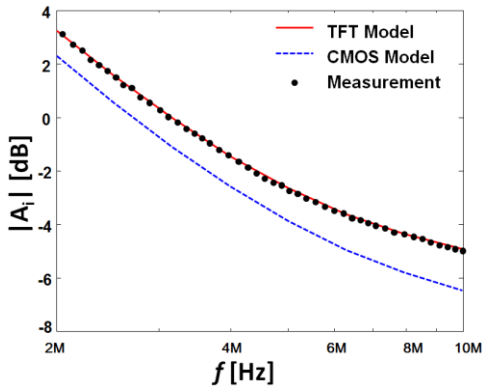

Fig. 3. Short-circuit current gain (A_i) for the TFT with channel width (W) = 100μm and channel length (L) = 10μm, which is converted from the S-parameter measurement.

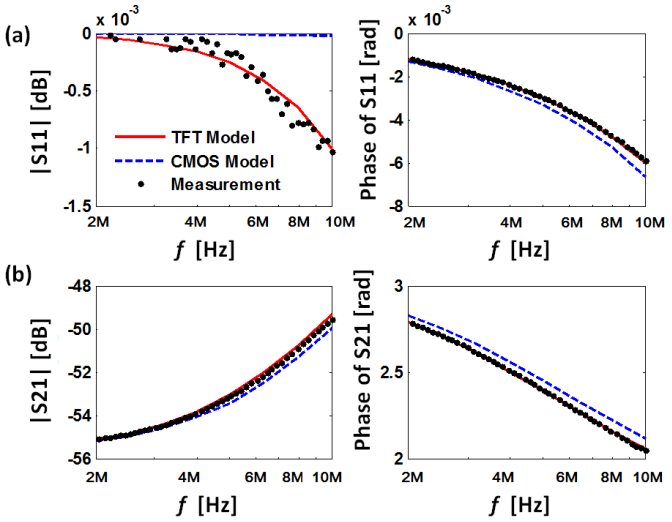

Fig. 4. (a) Amplitude and phase plots for S_{11} and (b) those of S_{21}, respectively. Here, the measurements are compared with the computational results for the CMOS model and TFT model, respectively.

shown in Fig. 4 indicate that the major difference of the two models lies in S_{11}, which can be explained by the different C_{ch} connection at the gate-source port.

Another important factor for TFTs is the threshold voltage shift (ΔV_T). In order to examine its influence on the small signal behavior, a constant bias stress measurement is performed on a W/L=50μm/10μm TFT with V_{GS}=8 V and V_{DS}=15 V for total 10 hours while f_T and V_T are measured at every logarithmic time interval (the I-V sweep is done to extract the value of V_T, which briefly disrupts the constant bias). The measurement result is shown in Fig 5. The ΔV_T increases to +0.2 V in total after the 10 hours bias stress and the respective Δf_T drops to 0.08 MHz almost linearly. This is due to the relatively small ΔV_T compared with V_{GS} which leads to first order approximation of Eq. (7). From Eq. (3) & (7) we have:

$$\Delta f_T \approx -\frac{r_{oi}(2R_C + r_{oi})(C_{OV} + C_{ch})}{2\pi(g_{mi0}C_{OV}R_C r_{oi} + (2R_C + r_{oi})(C_{OV} + C_{ch}))} K' \Delta V_T = \beta \Delta V_T \quad (10)$$

where β is the constant found to be about -3.2×10^6 [Hz/V] for the examined TFTs. Eq.(10) allows to estimate the shift in unity gain frequency with threshold voltage shift. Here, the coefficient β will be different for different material- and process-based TFTs.

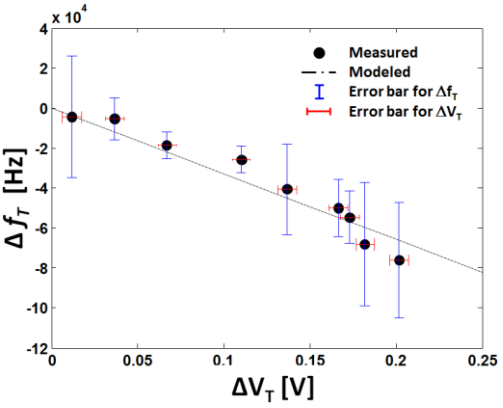

Fig. 5. Measured Δf_T with respect to ΔV_T for the examined IGZO TFT.

Table I. Summary of parameters for the CMOS and TFT models

Category	R_C=0	C_{ch}<<C_{OV}	General case
CMOS and TFT model equivalence	Equivalent	Equivalent	Not equivalent
Parameter relation	$g_m = g_{mi} = \frac{dI_{DS}}{dV_{GS}}$ $r_o = r_{oi} = \frac{dV_{DS}}{dI_{DS}}$	$g_m = \frac{dI_{DS}}{dV_{GS}}$ $r_o = \frac{dV_{DS}}{dI_{DS}}$	$g_{mi} = \frac{g_m r_o}{r_o - g_m r_o R_C - 2R_C}$ $r_{oi} = r_o - g_m r_o R_C - 2R_C$
Cut-off frequency	$f_T = \frac{g_m}{2\pi C_{tot}}$		$f_T = \frac{g_m}{2\pi(C_{tot} - g_m R_C C_{ch})}$
V_T shift terms	$g_{mi} = g_{mi0} - K'\Delta V_T$		$K' \approx \frac{g_{mi0}}{V_{GS} - V_{T0}}$

The summary of the model equivalence and parameter relations is given in Table I. Note that when CMOS model is used, the effect of R_C is included in g_m term. When the equivalent conditions are met, the TFT model yields to the CMOS model in all frequency range. The significance of the model difference is determined by value of R_C and C_{ch}.

IV. Conclusion

Small signal models are indispensable for the design of analog circuits, especially in the former for the correct phase margin and bandwidth of amplifiers and analog filters. This work reports on an accurate small signal model that takes into account the contact resistance, parasitic capacitance, and threshold voltage shift, while introducing internal transconductance (g_{mi}) and output resistance (r_{oi}). The proposed TFT model yields a 1% error in predicting the unity gain frequency, in contrast to 12.5% error using the CMOS model. It also provides a better fit to the measured s-parameters.

Theoretical analysis suggests that accuracy improvement stems from C_{ch} & R_C connection in the TFT model. It also suggests that the CMOS model can be inaccurate especially when the channel capacitance is more dominant and the contact resistance (R_C) is bigger. The increase of R_C due to down scaling of TFTs indicates that the proposed TFT model can be more beneficial to use in smaller devices. As R_C and its separation of channel capacitance and overlap capacitance generally exist in many other types of device structures and material families, the model is potentially applicable to other TFTs fabricated on insulator substrate such as glass and plastic. Additional bulk parasitics should be considered when modelling TFT on a semiconductor substrate.

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