Stabilizing a Graphene Platform toward Discrete Components

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Abstract

We report on statistical analysis and consistency of electrical performances of devices based on a large scale passivated graphene platform. More than 500 graphene field effect transistors (GFETs) based on graphene grown by chemical vapor deposition (CVD) and transferred on 4 inches SiO_2/Si substrates were fabricated and tested. We characterized the potential of a two-step encapsulation process including an Al_2O_3 protection layer to avoid graphene contamination during the lithographic process followed by a final Al_2O_3 passivation layer subsequent to the GFET fabrication. Devices were investigated for occurrence and reproducibility of conductance minimum related to the Dirac point. While no conductance minimum was observed in unpassivated devices, 75% of the passivated transistors exhibited a clear conductance minimum and low hysteresis. The maximum of the device number distribution corresponds to a residual doping below $5x10^{11}$ cm^{-2} (0.023 V/nm). This yield shows that GFETs integrating low-doped graphene and exhibiting small hysteresis in the transfer characteristics can be envisaged for discrete components, with even further potential for low power driven electronics.

The science of graphene has been maturing for more than a decade now [1], with the community keeping a constant eye on potential applications of this material [2]. In particular applications in micro-electronics [3] [4], in flexible electronics [5] [6], and in optoelectronics [7] [8] [9] have been widely discussed due to graphene's unique and attractive properties. Obviously still, the adoption of graphene at industrial scales will necessarily require numerous further challenges to be overcome. While one isolated demonstration device on micron-sized graphene may lead to unprecedented performances [1], industrial focus is based on (i) scalability and (ii) device characteristics uniformity and related statistics. The key developments in years to come will thus be related to the eased access by industrial groups to a large-scale material with uniform and predictable electrical properties, enabling the mass production of working devices. While graphene is already available in large scale as large as 300 mm Si substrates [10], unfortunately, unintentional doping of graphene due to adsorbates at the graphene surface leads to various charge carrier densities. As a consequence, the conductance minimum of a field effect graphene transistor is obtained for large gate fields (around or above 0.2 V/nm). Moreover trap states due to adsorbates at the dielectric/graphene interface and on the graphene surface lead to transfer characteristics exhibiting a large hysteresis [11]. To address these issues, the passivation of graphene transistors with atomic layer deposited (ALD) Al_2O_3 films has been studied [12] [13] [14] [15]. However, a statistical analysis of a large scale passivated graphene platform performed with hundreds of devices, without any previous selection, is not available.

In this study we propose a scheme to fabricate, on large scale 4" SiO_2/Si wafers, GFETs integrating low-doped graphene and exhibiting small hysteresis in the transfer characteristics. For this purpose, we have analyzed the electrical performances of 500 devices as a function of the fabrication process. The process takes as an input a commercially available low-cost and large-scale chemical vapor deposited (CVD) graphene produced and transferred on SiO_2/Si substrate [16] [17], and leads as an output to a relevant material platform with statistically stabilized performances. It consists in using a thin oxide as a protection layer before the lithographic process (after graphene transfer) and a 30 nm thick passivation layer after device fabrication. This process drastically increases the statistical availability of high performance GFETs. 75% of the protected/passivated devices exhibit a conductance minimum for a gate induced field below 0.17 V/nm (15 V on 90 nm SiO_2 gate oxide). Furthermore, our statistical study shows a hysteretic free operation under ambient conditions on about 25% of our protected/passivated devices.

Fig. 1a shows the used CVD graphene material. The studied devices are fabricated from graphene grown by CVD on Cu foils (the potential of the CVD technique for single-layer graphene growth on copper has been detailed elsewhere [18]) and then wet transferred onto target SiO_2/Si substrate using the standard poly(methyl methacrylate) (PMMA) technique. These steps are routinely realized, and result in standardized, commercially available Graphene on SiO_2/Si wafers [19]. A Scanning Electron Microscopy (SEM) image of a typical graphene device is presented in Fig. 1b. It corresponds to a Hall bar structure with a well-defined graphene channel and with metallic contacts deposited by evaporation.

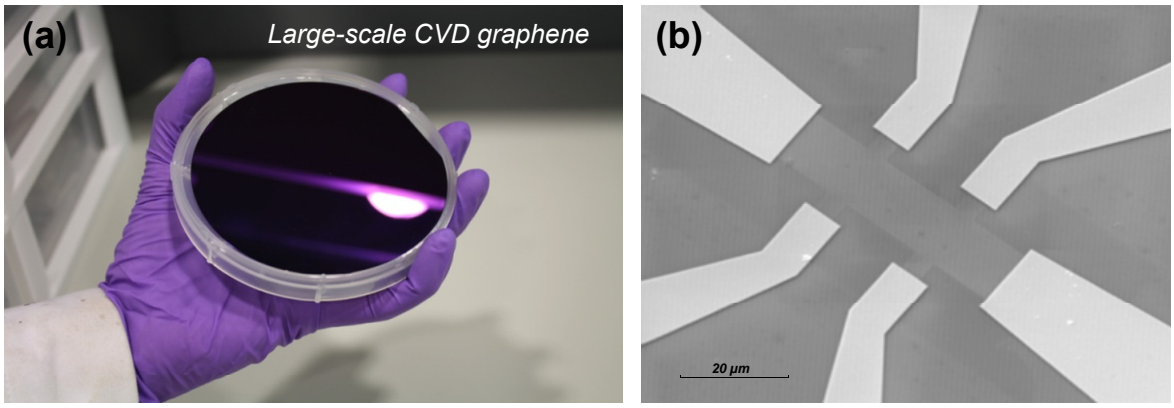

FIG. 1. (a) Large-scale monolayer CVD graphene transferred onto a 4 inches SiO_2/Si wafer (b) SEM observation of Hall bars structures.

Fig. 2a shows the process flow for graphene-based devices fabrication without any protection/passivation layer. Graphene devices are fabricated using both standard photolithography and electron beam lithography. First, the metallic alignment marks are realized by the lift-off technique. Then, we pattern photoresist pads to define the graphene channel by oxygen plasma etching. Eventually, we define source/drain electrodes using a lithography step followed by Ti/Au (20 nm/80 nm) layer evaporation and a subsequent lift-off process. Thus in this first set of devices, the graphene layer is directly exposed to fabrication processes and to air. In parallel, a second set of devices (see Fig. 2b) is prepared with a similar fabrication process flow, except that a protection layer is introduced. It is a thin (1 nm) aluminum layer deposited on top of the transferred graphene layer by electron beam evaporation. This thickness has been chosen to ensure full oxidation of the Al film in O_2 atmosphere. This layer avoids graphene contamination during the fabrication process; it suppresses graphene contact with photoresists, solvents, chemicals, etc and thus acts as a protection layer. Then, we perform lithographic steps to pattern graphene channels and to

define metallic source/drain contacts. The Al_2O_3 layer is removed solely on contact areas prior to metal deposition in a Tetramethylammonium hydroxide (TMAH) based solution. A third set of devices (see Fig. 2c) is prepared with the same protection layer and with a post-fabrication 30 nm thick Al_2O_3 film deposited by ALD [20] [21].

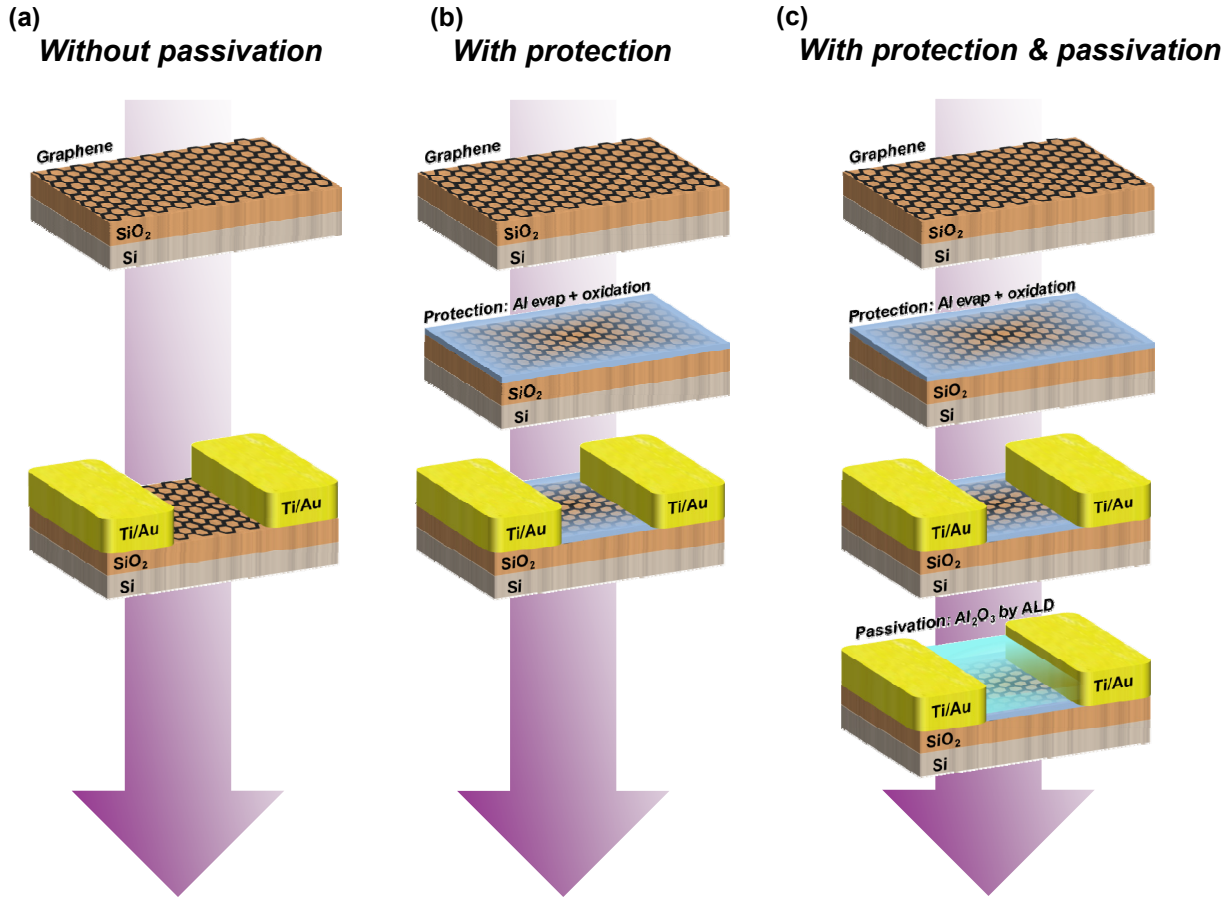

FIG. 2. Process flows of graphene devices fabrication without any protection/passivation layers (a), with protection process (b) and with protection/passivation process (c).

Complementary techniques such as optical microscopy, micro-Raman spectroscopy and Atomic Force Microscopy have been then used to characterize the resulting graphene layers. In particular, as presented in Fig. 3, we probe the preservation of graphene quality after Al_2O_3 deposition with Raman spectroscopy: we compare spectra of as-transferred graphene and graphene channels after deposition of both Al_2O_3 layers. Raman spectra are obtained in air at room temperature with an excitation wavelength of 514 nm. The black curve for as-transferred graphene shows a typical Raman spectrum with the G and 2D peaks located at 1593 cm^{-1} and 2690 cm^{-1}, respectively, and with the quasi absence of D peak. First we note that the intensity ratio of the G to the 2D peak is of about 0.3 and that the 2D band is a single sharp peak [22] which confirms that our film is monolayer graphene [23][24]. Importantly, the ratio I_D/I_G of D to G peak intensities is below few percent which indicates a very low amount of disorder in our graphene layers. We then probe the impact of the protection/passivation process on the graphene layer. The blue curve in Fig. 3 corresponds to a Raman spectrum of a protected and passivated graphene film (Fig.

2c). We do not observe any variation of the D peak intensity after the deposition of these two films. Thus we can conclude that our alumina passivation process does not introduce any structural defects in the graphene film, which is a major assessment towards our objective of identifying a large-scale high quality graphene platform.

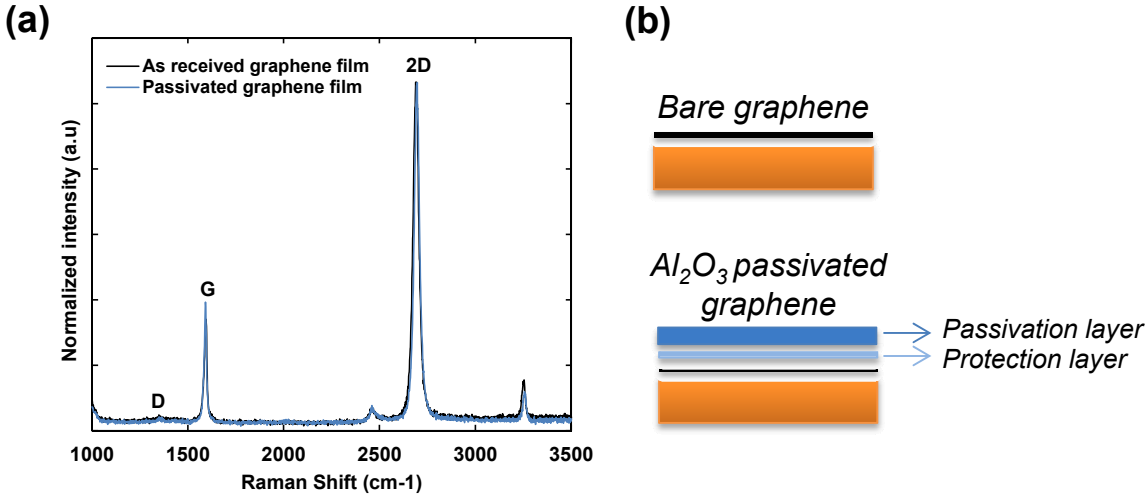

FIG. 3. Raman spectra of graphene films transferred on Si/SiO_2 substrate (black curve) and of the graphene channels after (blue curve) the deposition of the Al_2O_3 protection/passivation layers. The excitation wavelength is 514 nm.

We now turn to electrical characterization of the fabricated devices to study the effect of graphene passivation on the doping level. The electrical measurements were carried out with a probe station at room temperature and in ambient air. As a reference, the transfer curve of a graphene device without protection/passivation (process in Fig. 2a) is measured. It displays a highly p-doped behavior as the conductance minimum cannot be obtained for gate fields up to 0.5 V/nm (grey curve in Fig. 4a). This observed behavior shows that a specific fabrication process has to be used to strongly reduce graphene doping. In comparison, the purple curve in Fig. 4a shows the transfer characteristics of a typical graphene device fabricated with the protection/passivation process (process in Fig. 2c). In contrast to the first set of devices with bare graphene channels, this device shows a conductance minimum for a gate field (E_{min}) close to 0 and a good control of the conductance.

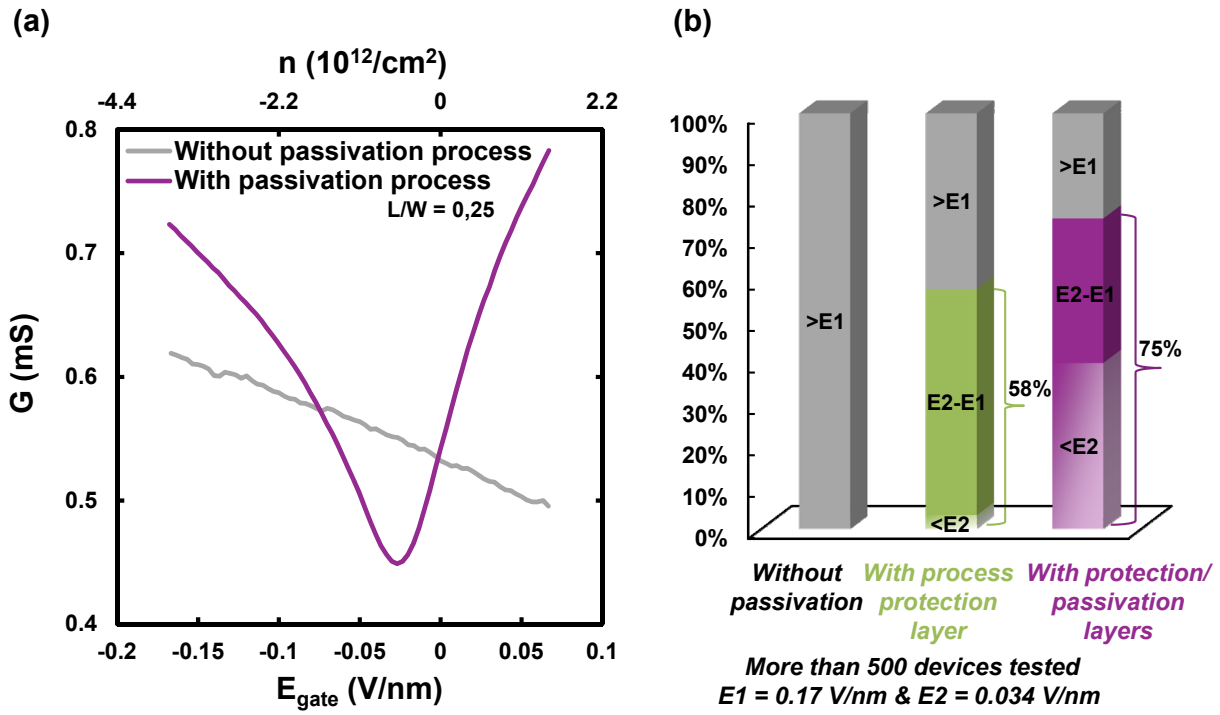

FIG. 4. (a) Typical transfer characteristics of GFETs fabricated on SiO_2/Si substrates without passivation process (grey curve) and with protection/passivation process (purple curve) under ambient conditions. (b) Percentage of devices exhibiting a conductance minimum for a gate field below E1 (0.17 V/nm) and E2 (0.034 V/nm) for each fabrication process: without protection/passivation, with only the protection layer and with both protection and passivation layers. Among the 500 graphene devices that have been tested, about 1/3 of them are fully passivated with both protection and passivation layers.

A statistical study was carried out on our graphene devices. The results are illustrated in Fig. 4b. To compare GFETs with our three different fabrication processes, we show the percentage of GFETs exhibiting an E_{min} value below E1 = 0.17 V/nm (15 V on 90 nm SiO_2/Si) and E2 = 0.034 V/nm (3 V on 90 nm SiO_2/Si). E1 is relevant for discrete components operated from the charge neutrality point with 15 V power supply and E2 is an even more stringent requirement for low power 3 V electronics (JEDEC standards definition [25]). We note that while voltage values are given for 90 nm SiO_2 which optimizes graphene optical contrast [26], thinner gate oxides could be implemented. For devices based on bare graphene, E_{min} is never observed below E1. On the contrary, 58% of protected devices and 75% of protected/passivated devices showed E_{min} below E1. We also analyzed the percentage of devices that exhibit an E_{min} below E2. The percentage of devices satisfying this criterion is only 3% for the protected devices but attains 40% when the two-step protection and passivation process is performed.

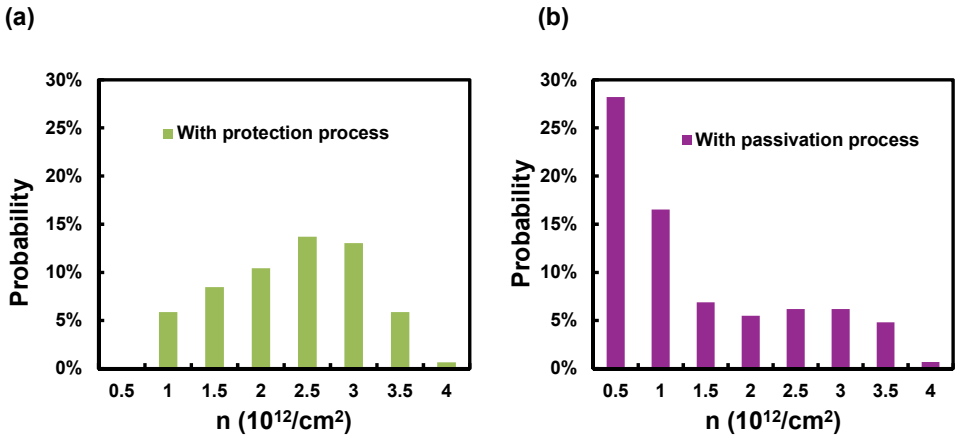

FIG. 5. Charge density histograms deduced from conductance minimum value with only the protection layer (a) and with both protection and passivation layers (b).

For each measured transistor, we extracted the residual charge density from the E_{min} value. Fig. 5 shows the residual doping histograms with protection or protection/passivation process. For the (only) protected devices, the distribution maximum is in the 2.5 – 3. $10^{12}/cm^2$ range and 100% of the graphene channels are p-doped. For the protection/passivation process, the distribution maximum is clearly shifted to the 0 – $5x10^{11}/cm^2$ range and graphene channels are n or p-doped. Thus the whole two-step process leads to transistors based on very low doped graphene. We note that these devices are characterized by very low E_{min} values (<E2). Very interestingly, this should allow a significant fabrication yield for devices operating at charge neutrality point (such as optoelectronics devices [9]) with even a very low power supply.

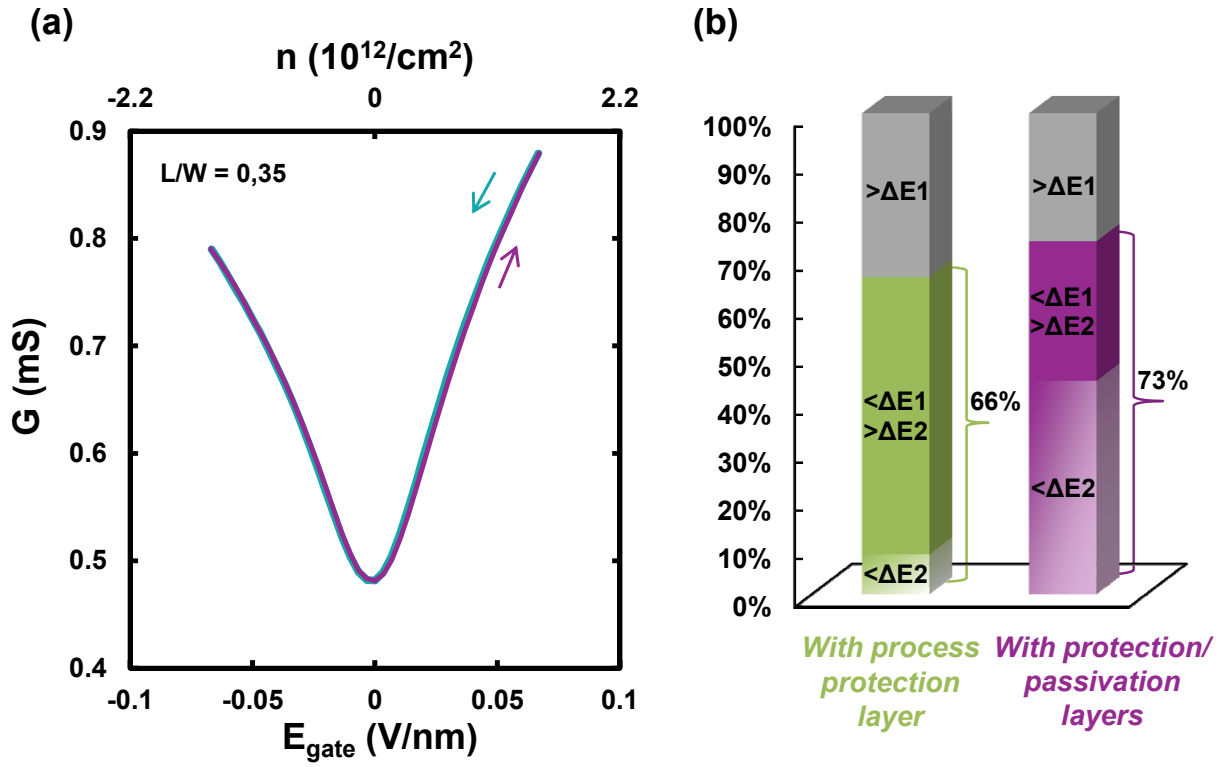

FIG. 6. (a) Typical transfer characteristics of GFETs with protection/passivation process (purple curve) displaying a hysteresis free behavior under ambient conditions. (b) Gate field hysteresis statistics on devices satisfying $E_{min} < E1$, with the protection process and the protection/passivation process. Devices are sorted as a function of their hysteresis amplitude (ΔE) with: ΔE1 and ΔE2 corresponding to 10% of E1 and E2 fields.

We now turn to the gate field hysteresis statistics performed on devices with $E_{min} < E1$. The purple curve in Fig. 6 shows the transfer characteristics of a graphene device fabricated with the protection/passivation process (third process in Fig. 2c). This device shows a conductance minimum for a gate field below E2 and also displays no hysteresis. The percentage of protected and protected/passivated devices that display a hysteresis below ΔE1 = E1/10 = 0.017 V/nm is respectively 66 and 73% (Fig. 6b). Besides, with a more stringent criterion (hysteresis below ΔE2 = E2/10 = 0.0034 V/nm), the percentages become 44% for protected/passivated devices and only 8% for only protected devices. Even more remarkable, 23% of working protected/passivated devices exhibit no hysteresis (the percentage is 1% without passivation). These results highlight the necessity of performing both protection and passivation layers to obtain hysteresis free graphene devices based on very low doped graphene. Importantly, we observed the stability of these results in time, a crucial requirement for applications, over a period of more than 1 month thanks to the passivation process.

While not being the main motivation of our work, the impact of graphene passivation on electrical parameters, especially the mobility, was investigated as well. The graphene mobility was extracted by fitting the total measured resistance of the graphene device with the commonly used constant mobility model [27]. Illustratively, the field effect mobility of the protected/passivated device presented in Fig. 1b is about 6.900 cm^2/Vs which is comparable to its Hall-mobility value of 6.100 cm^2/Vs. These values are similar to carrier mobilities reported in the literature for CVD graphene [27][15].

In summary, a large statistical study of transistor characteristics was conducted on devices based on a commercially available large scale CVD graphene source. We defined a fabrication process integrating an oxidized Al film performed after graphene transfer and an Al_2O_3 ALD layer deposited after device fabrication. This allowed us to demonstrate a scheme to fabricate transistors based on low-doped graphene and exhibiting small hysteresis with a high yield. 75% of the devices showed characteristics compatible with discrete electronic components and strong potential for low power applications has been demonstrated. This stabilized graphene platform paves the way for further investigations of the potential of graphene in electronic applications.

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