Design of a Normally-Off Diamond JFET for High Power Integrated Applications

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Abstract— Normally-on (depletion mode) and normally-off (enhancement mode) diamond Junction Field Effect Transistors (JFETs) have been analyzed by means of a commercially available TCAD software. First, the parameters used for describing the incomplete ionization, avalanche, and mobility models in diamond have been discussed and assessed against the state-of-the-art. The on- and off-state electrical characteristics of diamond JFETs have been simulated with the suggested parameter values and matched with a set of available experimental data. Secondly, an optimization technique which can improve the performance of an enhancement mode diamond JFET that operates in the unipolar conduction regime has been proposed. This method takes into account the unique properties and limitations of diamond and highlights the main issues that can arise from the design of a normally-off diamond JFET. In particular, the crucial effect of the high temperature on the performance of the normally-off JFET has been investigated. The adopted technique is mainly based on a design of TCAD experiments and no mathematical algorithms have been developed for the calculation of the optimized set of parameters.

Keywords— Diamond JFET, Diamond power devices, TCAD Modeling, Incomplete ionization, Wide Band Gap Semiconductors

Contents

1. Introduction

Diamond is considered to be the ultimate wide band gap (WBG) semiconductor thanks to its superior properties in terms of thermal conductivity (24 W/K·cm), saturation velocity (2×10^7 cm/s), high operating temperature (>700 K) and high electrical breakdown field (7.7 MV/cm) [1-3]. Despite the fact that the technology is still at an early stage, several diamond devices have been realized for power electronics [3-9], RF (radio-frequency) [10-12] and chemical and biological sensors [2, 13] applications and circuits. Regarding the power electronics applications of diamond, the high activation energy of n-type dopants (0.57 eV for phosphorus) has hindered the fabrication of bipolar devices such as BJTs (Bipolar Junction Transistors) and IGBTs (Insulated Gate Bipolar Transistors) due to the high resistivity of the n-layers and the large turn-on junction voltages. For this reason, the research on diamond FETs (Field Effect Transistors) devices has been essentially focused on unipolar p-type devices, especially delta-doped FETs, HFETs (Hydrogen terminated FETs) and p-type JFETs (Junction FETs) [14-19]. However, the large leakage current observed in delta-doped structures [19] and the lack of the mobility enhancement in such devices have limited the performance and applications of delta-doped diamond FETs. On the other hand, the recent improvements in the selective growth of n-type diamond on <111> face [20] and in the stability control of the hydrogen terminated diamond interfaces [5], have pushed the research towards JFETs and HFETs respectively, where high on- and off-state performance have been demonstrated [5, 14, 17, 18]. In this scenario, diamond JFETs have the main advantage of being oxide free devices and avoiding problems encountered with the oxide reliability, hot carrier injection and interface traps and defects [21]. Nevertheless, due to the incomplete ionization caused by the absence of shallow dopants, diamond JFETs devices cannot outperform so far the state of the art WBG semiconductors for high power devices applications unless special techniques such as mobility enhancement or shallow dopants are developed. In this work, starting from the matching of experimental data of a normally-on diamond p-type JFET, an improved normally-off design is theoretically identified through an extensive set of two dimensional

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TCAD (Technology Computer Aided Design) simulations. The superior performance of the designed enhancement mode p-type JFET, has been assessed at different temperatures and compared with that of the state-of-the-art diamond JFETs.

2. Numerical Modeling of CVD Diamond

Predicting the electrical characteristics and developing new design architectures is fundamental for advancing research in diamond power devices. In the past, several works have dealt with parameter extraction starting from matching of experimental data on diamond devices [22-25]. In this paper, in addition to the mobility models [26, 27] already implanted in [23], the diamond physical models have been updated taking into account recent experimental results [28, 29] and including a temperature dependence for the saturation velocity and for the impact ionization phenomenon. This allowed to correctly simulate diamond JFET devices in the unipolar working mode at different temperatures and biasing conditions. The models of the physical phenomena that determine the behavior of diamond power devices are detailed in the following section.

Incomplete Ionization

The high activation energy of boron and phosphorus dopants (respectively acceptor and donor dopants) in diamond devices leads to the so called incomplete ionization effect [24]. This means that only a fraction of the dopants is activated and contribute to the conductivity of the material. The equations and parameters that determine the concentration of activated n-dopants, N_D, (1a) and p-dopants, N_A, (1b) are given below [22, 23]:

$$N_D = \frac{N_{D0}}{1+g_D \exp\left(\frac{E_{FN}-E_D}{kT}\right)} \qquad N_{D0} < N_{Dcritic} \qquad (1a)$$

$$N_A = \frac{N_{A0}}{1+g_A \exp\left(\frac{E_A-E_{FP}}{kT}\right)} \qquad N_{A0} < N_{Acritic} \qquad (1b)$$

$$N_X = N_{X0} \qquad N_{x0} > N_{xcritic} \qquad (1c)$$

$$E_x = E_{x0} - \xi_x N_x^{1/3} \qquad (1d)$$

$$g_x = g_{x0} + k_x \cdot \exp\left(\frac{-\Delta_{gx}}{kT}\right) \qquad (1e)$$

Where the parameters in the formulas are:

N_A (N_D), activated number of acceptors (donors) impurities.

N_{A0} (N_{D0}), total number of acceptors (donors) impurities.

g_A (g_D), degeneracy factor for acceptors (donors).

E_A(E_D), ionization energy for acceptors (and donors).

E_{FP} (E_{FN}), quasi fermi level for holes (electrons). E_{FP} is defined with reference to the valence band maximum (E_V).

k, Boltzmann constant.

T, temperature expressed in kelvin.

$N_{Acritic}$ ($N_{Dcritic}$), critical value of the acceptor (donor) doping.

E_{A0} (E_{D0}), the value of E_A (E_D) for low doping concentrations.

ξ_A (ξ_D), Pearson-Bardeen coefficient of acceptors (donors) which computes the reduction of the activation energy for high doping levels.

g_{A0} (g_{D0}), the low temperature degeneracy factors.

k_A, k_D, Δ_{gA}, Δ_{gD}, constants that determine the variation of the degeneracy factor with the temperature.

Table 1. Parameters for the incomplete ionization model for acceptors (boron) and donors (phosphorous) dopants in CVD Diamond.

x	E_{x0} (eV)	$N_{xcritic}$ (cm^{-3})	ξ_x (eVxcm)	g_{x0}	kx	Δ_{gx} (meV)
A (Acceptors)	0.37 [30, 31]	4.5×10^{20} [32]	4.7×10^{-8} [30]	4 [30]	2 [33]	6 [33]
D (Donors)	0.57[34]	1×10^{20}	0[35]	2[36]	0	0

The above equations compute the partial activation of the dopants through the Fermi-Dirac distribution, (1a), (1b), (1c), the experimental law of Pearson and Bardeen, which takes into account the reduction of the activation energy for higher doping, (1d), and the degeneracy factors temperature dependence, (1e). Some of the parameters mentioned in table 1 have been characterized in literature[30-36]. However, other crucial factors, such as the dependence of the degeneracy factors for donors on the temperature (Δ_{gD}, k_D) and the critical value of phosphorous doping ($N_{Dcritic}$), are still to be identified. Equations (1) also include a dependence of the activated dopants on the electric field through the quasi-Fermi levels for electrons and holes (E_{FN} and E_{FP}, respectively). The amount of ionized dopants depends of course on the position of the quasi-Fermi levels with respect to the conduction and valence band. Due to the fact that these energy levels shift in the non-neutral region as a consequence of the variation of the electric field, the activated number of dopants in the space charge regions (SCR) varies, possibly generating full ionization of the dopants. This increased activation at higher electric fields influences in turn the depletion region extension and the distribution of the electric field. This feedback mechanisms cannot be neglected in the modeling of diamond JFETs, as it will be illustrated in this work. In this study, the hopping conduction regime [37] has not been modelled and the transition from the "incomplete" to the "total" ionization occurs at a certain level of

doping which has been called "critical". While this critical value of doping has been experimentally discovered for acceptors (4.5×10^{20} cm^{-3})[32], it is still unidentified for donors and it will be assumed to be 1×10^{20} cm^{-3} in this study. Furthermore, because the experimental law of Pearson and Bardeen has been reported not to be valid for phosphorus [35], the reduction of the activation energy for increasing n-doping has been neglected (i.e. ξ_D=0) together with the temperature dependence of the degeneracy factors (Δ_{gD}, k_D). To have an overall idea of the number of activated holes, one can implement the neutrality balance equation (2) and compute the activated p-dopants with the Fermi-Dirac distribution using (1). Figure 1 shows the result of this calculation as a function of doping concentration and for the case N_D=0 cm^{-3} at three operating temperatures.

$$n + N_A = p + N_D \tag{2}$$

A similar analysis can be conducted for n-dopants.

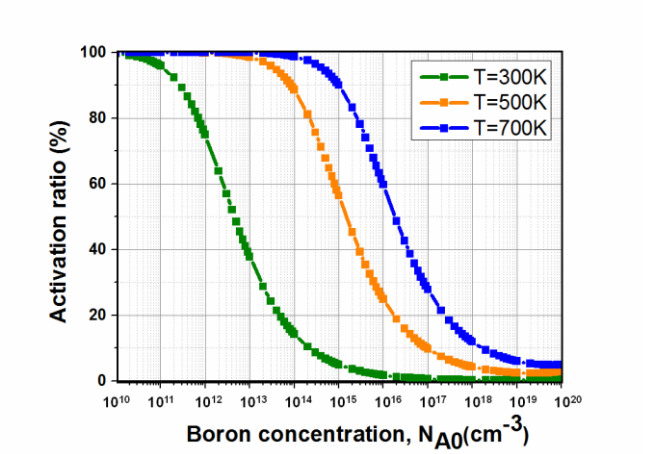

Figure 1, Hole activation rate (N_A/N_{A0}) as function of the boron concentration (N_{A0}) at three different operating temperatures. For $N_{A0}>4\times10^{20}$ cm^{-3} the activation ratio becomes 100% (see equation 1c).

Empirical Mobility Models

Recent Hall effect measurements for hole and electron mobility [26] have been successfully implemented in Sentaurus TCAD with the Arora Model [38]. This mobility model (3) takes simultaneously into account the temperature, the doping dependence, and different values of compensation doping. The values of the parameters for holes and electrons adopted in the set of equations (3) are available in[26, 27].

$$\mu(T, N_{A0}) = \mu(300, N_{A0}) \cdot \left(\frac{T}{300}\right)^{-\beta(N_{A0})} \tag{3a}$$

$$\mu(300, N_{A0}) = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + \left(\frac{N_{A0}}{N_\mu}\right)^{\gamma_\mu}} \tag{3b}$$

$$\beta(N_{A0}) = \beta_{min} + \frac{\beta_{max} - \beta_{min}}{1 + \left(\frac{N_{A0}}{N_\beta}\right)^{\gamma_\beta}} \tag{3c}$$

High Field Saturation

Under the influence of high electric fields, the mobility degradation can be modeled through the high field saturation model based on Canali model and on the Caughey Thomas Law [39]. The reduction of the saturation velocity at high temperature has been modelled as in equation (4). In the literature, the saturation velocity of carriers in CVD diamond which has been determined by means of Monte-Carlo simulations and experimental measurements, have exhibited a significant variation from 0.96×10^7 cm/s up to 2.3×10^7 cm/s [2, 40]. In this work, we assumed $v_{sat0}=2\times10^7$ cm/s [41] and b=6, where the coefficient b has been adopted as a fitting parameter for the high temperature transfer curve of the normally-on JFETs (figure 6).

$$v_{sat} = v_{sat0}\left(\frac{T}{300}\right)^{-b} \tag{4}$$

Impact Ionization Coefficients

A reliable impact ionization (II) model is vital for the correct evaluation of the breakdown capability of diamond power devices. So far, several models and coefficients have been proposed in the literature [24, 42, 43] and the majority of those are based on the Chynoweth [44] model. This model is shown in equation (5), where E is the electric field and the coefficients implemented in this study and in the literature, are listed in table 2.

$$\alpha_{n,p} = a_{n,p} \exp\left(-\frac{b_{n,p}}{E}\right) \tag{5}$$

Table 2. Diamond impact ionization coefficients for the Chynoweth model adopted in the literature [45, 46].

	a_p (cm^{-1})	a_n (cm^{-1})	b_p (V/cm)	b_n (V/cm)
Hiraiwa[46]	6.1×10^4	1.46×10^5	1.4×10^7	2.4×10^7
Kamakura[45]	4.2×10^6	3.7×10^6	2.1×10^7	5.8×10^7
This work	5.48×10^6	5.48×10^6	6.5×10^7	6.5×10^7

The simulations using the II coefficients in the literature[45, 46] do not fit the reported JFET results. Therefore, the values listed in Table 2 are adopted in this study. They, however, do not rule out other choices of a_p and b_p that result in the same breakdown voltage (BV),

as projected by the scaling law [43, 46]. For this study, the impact ionization rates are assumed equals for both holes and electrons, as widely discussed also in [46]. This assumption is validated as an approximation by adopting the geometric average of the values for holes and electrons as the common value. Additionally, a temperature dependence of the ionization coefficients has been included, as shown in the equation (6a) through the parameter γ (6b). This parameter expresses the temperature dependence of the phonon gas against with holes and electrons are accelerated [47, 48]. In (6), T_0 is the room temperature (300K) and $h\omega_{op}$ is the optical phonon energy assumed equal to 0,063eV [47, 48], which is the default value for Silicon.

$$\alpha_{n,p} = \gamma a_{n,p} \exp\left(-\gamma \frac{b_{n,p}}{E}\right) \tag{6a}$$

$$\gamma = \frac{\tanh\left(\frac{h\omega_{op}}{2kT_0}\right)}{\tanh\left(\frac{h\omega_{op}}{2kT}\right)} \tag{6b}$$

Simulations of a Normally-On JFET

To validate our models, experimental data for unipolar normally-on JFET [14] were compared with two-dimensional TCAD simulations. In order to reduce the computational time and optimize the TCAD simulations, we defined a simplified 2D unit cell, shown in figure 2.

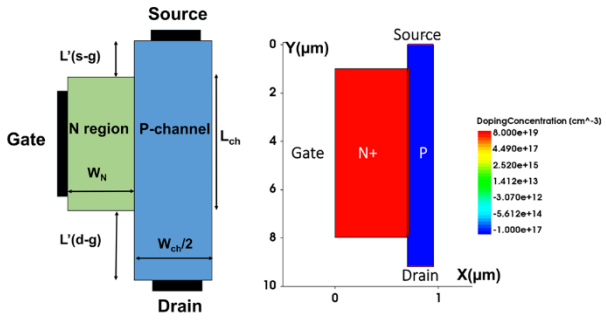

Figure 2 (left) schematic 2D unit cell used for the TCAD simulations of the normally-on p-type diamond JFET. (right) 2D TCAD unit cell with details on doping concentrations and geometry. N+ doping is fixed at 8×10^{19} cm^{-3}, p doping is fixed at 1×10^{17} cm^{-3}, the channel length (L_{ch}) is 7 μm and the channel width (W_{ch}) is 0.5 μm. The drain, source and gate contacts have been declared as ohmic. More details about the structure can be found in [14].

The choice of the simplified unit cell in figure 2 (left) is based on the fact that the device is symmetrical to a cut along the p-channel and the two lateral n+ gates are driven concomitantly for power electronic applications. However, such simplified 2D structure does not take into consideration some aspects of the real device structure. The buffer layer region is in fact not modelled in the 2D unit cell and the n-regions (phosphorus doped) are defined as rectangles whilst in the reality they have a trapezoidal shape due to the selective growth of n-diamond on the sidewalls of the p-channel. Figure 3 shows the breakdown voltage obtained from the numerical simulation of the 2D cell at different temperatures and its comparison with the measurement data, showing a good agreement at T=300 K and a slight overestimation at higher temperatures (T=473 K).

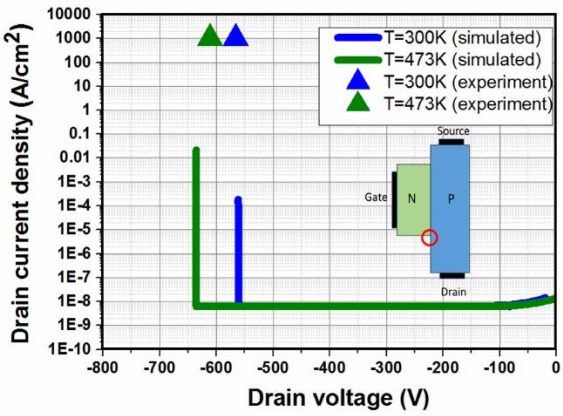

Figure 3, Breakdown voltage simulations for the normally-on JFET with the set of avalanche coefficients of table 2 at two different operational temperatures (300K and 473K). In these simulations, the gate voltage (V_G) has been fixed at 20V. The breakdown voltage has been extracted by visual inspection of the drain current (when this value increases of more than 3 orders of magnitude compared to the simulated leakage current) and compared with the experimental results[14]. The point where the highest electric field is reached is located near the pn junction in correspondence of the red circle.

For the off-state simulations, a constant background carrier generation rate of 1×10^{12} cm^{-3}s^{-1} has been introduced since the simulated leakage current is much lower than the measured one and this can lead to serious convergence problems. Additionally, an external resistance of 1×10^{11} Ωμm has been attached to the drain contact to facilitate the convergence at the onset of the impact ionization phenomenon. The simulated breakdown current shows a steeper variation compared to the measured one [14] in correspondence of the voltages at which the leakage current increases with the reverse drain voltage. Indeed, the constant value of the simulated leakage current is fixed by the previous mentioned background carrier concentration and it is much lower than the experimental value of the leakage current which could be mainly caused by defects and impurities. Moreover, the breakdown simulation stops converging after the current density increases of 4/5 orders of magnitude, before reaching the experimental value of ~1×10^3 A/cm^2. One can note from figure 3 a positive temperature coefficient of the breakdown

voltage. This is a clear signal that the breakdown occurs as a consequence of the impact ionization phenomenon (see equations 6) as opposed to the punch-through, which is expected to give a negative temperature coefficient. Additionally, a plot of the electric field in the structure (figure 4) displays the maximum electric field at the breakdown voltage which is located at the Drain-Gate junction in agreement with the experimental results reported in [14]. In figure 4, all the assumptions and the biasing conditions such as the drain-source voltage (V_{DS}) and the gate voltage (V_G) values adopted have been reported.

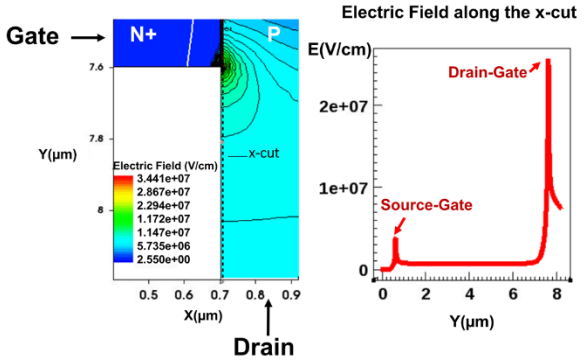

Figure 4, Electric field distribution at the gate-drain corner (left) at the RT breakdown voltage (V_{DS}=-570 V, V_G=20 V and T=300 K). The electric field distribution along an x cut (at x=0.7μm) shows that the peak electric field value is located at the Drain-Gate corner (right), where a maximum value >20 MV/cm is reached.

On-state simulations at room and high temperature were carried out (figures 5 and 6) to verify the reliability of the proposed models. The small mismatch between the experimental results and the simulations in figure 6 can be mainly attributed to the non-uniform doping concentration in the p-channel of the real device and to the not uniform width of the channel [14, 20, 49] which has not been considered in this 2D design. For V_G lower than -5 V the bipolar action of the JFET occurs and minority carriers (electrons) are injected in the channel from the n+ regions, so increasing the total conductivity of the JFET, as reported in [18]. To fully understand the potentials and the limits of the bipolar action in diamond JFET, a better insight into the recombination process and carrier lifetime is needed. However, this goes beyond the purpose of this work.

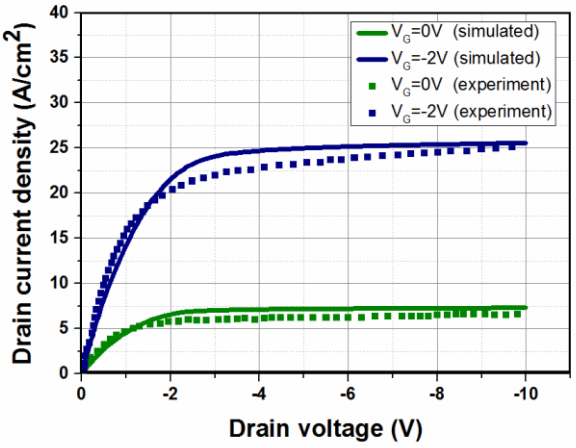

Figure 5, Measured [14] and simulated output characteristics for the structure in figure 2 for V_G= 0 and -2 V, and at T=300 K.

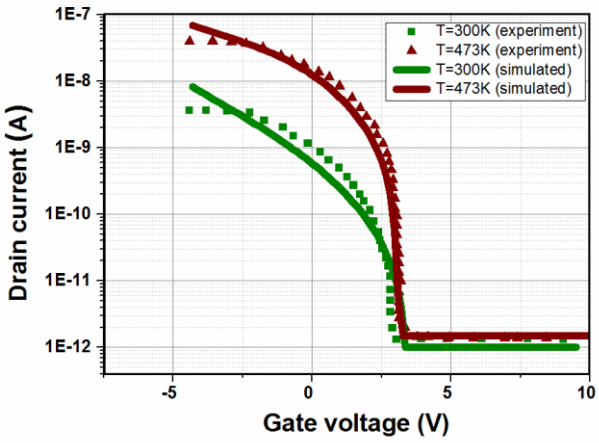

Figure 6, Experimental [14] and simulated transfer curves for the structure in figure 2 at T=300 and 473 K (V_{DS}=-0.1 V).

3. Design technique for a Normally-Off JFET

Normally-off JFETs [21, 50, 51] are preferable over the normally-on technologies as they are easier to drive due to the fact that they are less prone to unexpected behaviours during the switching. A possible way to convert a normally-on technology into a normally-off is via the cascode configuration where the high voltage normally-on FET is connected in series with a low voltage FET [52]. However, this configuration has several drawbacks such as a higher specific on-state resistance (R_{on_spec}), larger form factor due to unmatched voltage rating, and higher losses. Normally-off devices are therefore preferable to any normally-on based technology. On the other hand, in order to ensure a normally-off operation in diamond-based FETs, the channel width together with the channel doping have to be reduced. This is detrimental in terms of R_{on_spec} [53]. A recent publication demonstrates the first attempt to realize a normally-off diamond JFET device [15]. In the proposed device, the submicron channel allows the

depletion regions to touch each other when the gate is at zero bias and provides the normally-off behaviour. This device is the first experimental demonstration of a normally-off FET in diamond and some improvements in the design are still possible. The on-state current density (R_{on_spec}~20 Ωcm^2 at V_G=-4 V) is more than two orders of magnitude lower than those of the normally-on JFET devices proposed in literature and the small channel width (0.2 µm) makes difficult to control the uniformity of the channel in terms of geometry and doping profile. This work proposes an improved design of this first normally-off JFET, taking into considerations the physical and technological limitations of diamond. It is worth noting that contrary to the conventional definition[54], the R_{on_spec} for diamond JFETs proposed in [14, 15, 18] has been calculated adopting the cross sectional area and not the planar one. Such approach can be validated only after the vertical operation is realized. For the design technique, we have used an extensive set of TCAD simulations based on the models discussed in the previous section. Firstly, we defined a simplified 2D unit cell as already done for the normally-on JFET, neglecting in this way some of the 3D effects which occur in the real device (see figure 2).

The main targets of the procedure are listed below:

- Normally-off operation at high temperatures.
- Minimum R_{on} specific (R_{on_spec}) per unit cell.
- Avoid Punch-Through breakdown.
- Breakdown target: 2 kV.

The breakdown voltage target has been arbitrarily chosen to be 2 kV which is a value comparable with the state-of-the-art breakdown voltage of other diamond FETs [6, 16, 55]. Then, we defined the input parameters which are the gate doping (n-doping), the gate-to-source distance (L'(s-g)) and the gate width (W_N). The n-gate doping has been fixed at the value adopted for all the manufactured diamond JFETs (both in normally-on and in normally-off configurations) and it is equal to 8×10^{19} cm^{-3}; L'(s-g) is fixed at 1 µm. This value guarantees a safe margin for the source contact deposition without an unnecessary increase in the drift resistance and it is of the same order of magnitude (µm) of the values reported for other JFETs in the literature [14, 20, 49]; the gate width W_N, is fixed at 0.7 µm.

Table 3. Fixed parameters for the design technique.

n-doping	W_N	L'(s-g)
8×10^{19} cm^{-3}	0.7 µm	1 µm

From these assumptions, we propose a technique to define an optimum value for the channel width (W_{ch}), the drain-to-gate distance (L'(d-g)), the doping of the channel (p-doping), the channel length (L_{ch}) and the optimal operational temperature (Topt). The steps involved are described below:

Step 1: identification of the optimal junction temperature. The choice is based on the minimum value of the resistivity. The optimal temperature has been chosen to be lower or equal to the maximum one (Topt ≤ Tmax).
Step 2: analysis of the channel doping due to the technological limitations and the requirements of the design ($P_1 \leq$ p-doping $\leq P_2$).
Step 3: evaluation of the limits imposed for the channel width in order to ensure the normally-off operation until the optimal temperature ($W_1 \leq W_{ch} \leq W_2$).
Step 4: TCAD simulations varying the channel length ($L_1 \leq L_{ch} \leq L_2$), the channel width and the doping of the channel are carried out based on the technological and physical limitations discussed in the previous steps. The influence of the channel length on the performances of the device is here discussed.
Step 5: selection of the best design based on the principal targets. First, designs were selected for their capability to avoid Punch-through breakdown (>2kV) between RT and Topt. Then, designs with normally-on operation before Topt have been discarded, and the best performing design in terms of minimum R_{on_spec} in the range RT ≤ T ≤ Topt , has been selected. Successively, the gate-to-drain distance (L'(d-g)) has been varied, to fulfil the target on the breakdown voltage (2kV). If the selected design does not allow to reach the required breakdown voltage specification, the "second best performing design" is considered and so on, until all the targets of the procedure have been satisfied.

STEP 1

Ensuring normally-off operation for a diamond JFET is not an easy task at high temperatures. This is because the doping activation increases with temperature, hence decreasing the depletion region extent in the channel. The risk is therefore that the device can become normally-on at high temperatures. This risk is enhanced also by the reduction of the built-in potential. In addition to this effect, higher temperature operations can lead to an increased pn junction leakage current [49] which could reduce the breakdown voltage of the JFET. For these reasons, the design of a diamond normally-off JFET should be done keeping in mind the temperature effect. Moreover, the combined effect of the incomplete ionization and the hole mobility in 1(b) and 3(a) at high temperature, leads to an optimum resistivity (ρ) window. The resistivity (ρ) has been calculated as $(N_A(T)\cdot q \cdot \mu(T))^{-1}$, where q is the electron charge. As illustrated in

figure 7, where the resistivity of p-type diamond has been sketched as a function of the temperature for different doping levels (N_{A0}) and a negligible value of the donor compensation doping (less than 1×10^{10} cm^{-3}), an optimum resistivity window can be identified between 450 K and 600 K. Since it is difficult to ensure normally-off operation up to 600 K without sacrificing too much the on-state resistance (reducing the channel width and the p-doping) and without significantly increasing the gate leakage current, T=450 K has been selected as the optimum temperature (Topt) for this design. During the choice of the best performing design (step 5), we will guarantee that the optimal temperature is lower or equal to the maximum junction temperature (Tmax) at which the designed normally-off JFET becomes normally-on (Topt ≤ Tmax).

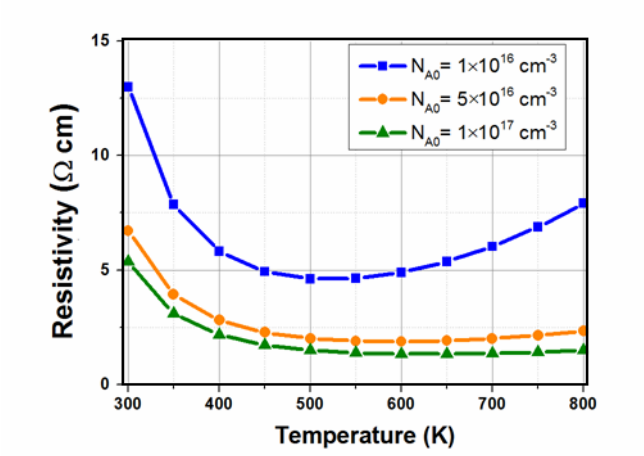

Figure 7, Resistivity of p-diamond vs temperature for different acceptor concentration (N_{A0}).

STEP 2

Regarding the channel doping which in this design is equal to the drift region one, two main limitations can be identified. The first limitation is technological: it is not possible to accurately control the p-doping in diamond substrate for values below 1×10^{15} cm^{-3}. This evidence sets a lower limit for the channel doping (P_1). On the other hand, when the doping is increased the electric field distribution in the drift region can easily become NPT (Non Punch Through) and it could be not possible to fulfil the specification on the breakdown. Additionally, by increasing the drift region doping, the design of a normally-off JFET becomes more difficult since the channel width (W_{ch} in figure 2) has to be dramatically reduced in order to ensure normally-off operation. Furthermore, the gate control can become weaker for higher channel doping in a diamond JFET, since the incomplete ionization effect occurs also in the n-gate giving only partial activation of the donor dopants. For all these reasons, the upper limit (P_2) for the channel doping has been fixed at 1×10^{17} cm^{-3}. The suggested channel doping window is therefore between 1×10^{15} cm^{-3} and 1×10^{17} cm^{-3}.

STEP 3

The lower and higher possible channel width values are here discussed. It is in fact necessary that the channel width is sufficiently small to be fully depleted at zero gate bias but at the same time it has to be wide enough to ensure current flow through the channel before the pn+ junction switches on. This imposes two limitations: (i) the half channel width cannot exceed the depletion region at zero bias in order to be normally-off (limit W_1); (ii) the channel width cannot be lower than the depletion region calculated before the onset of the pn junction in order to prevent the bipolar mode regime and ensure a safe voltage control of the gate (limit W_2). In this technique, the margin W_2 has been evaluated in order to provide at least 0.5 V before the onset of the bipolar mode (since we are dealing with a unipolar mode JFET). When the drain voltage is at zero bias, the depletion region can be calculated according to equations (7), where the dependence of the built-in potential on the temperature and of the activated doping on the electric field and temperature have been included. For a uniform doping of the p-type channel and when the potential difference between source and drain is zero (V_{DS}=0 V), the depletion region width (W_D) in the channel, can be considered as independent on the position [21] and evaluated as in 7(a). In the formula ε_s is the dielectric constant of diamond, Ψ_{bi} is the built-in voltage, N_V and N_C are the density of states for the valence and conduction band and E is the electric field.

$$W_D = \sqrt{\frac{2\varepsilon_S\left[\psi_{bi}(T)+V_G\right]}{qN_A(T,E)}} \qquad 7(a)$$

$$\psi_{bi}(T) = \frac{kT}{q}\ln\left(\frac{N_A N_D}{N_V N_C}\right) + \frac{E_G}{q} \qquad 7(b)$$

In the space charge region (SCR) where the electric field (E) is significant, the number of activated dopants is higher compared to the one in the neutral region. Simulation results revealed that the effective width of the depletion region in the channel for the JFET cannot be theoretically evaluated taking into account a total activation in the SCR (N_A=N_{A0}) and TCAD simulations are so necessary for a correct design. Indeed, it is worth noting that the incomplete ionization phenomenon slightly reduces the effective channel width at high temperatures, complicating so the normally-off operations of diamond JFETs at high temperatures. Furthermore, the limits illustrated in figure 8 do not take

into account the potential barrier lowering induced by the drain voltage. This phenomenon brings to the reduction of the channel barrier for increasing drain voltage, thus allowing a significant hole current in the channel also when the device should be off. The effect of the drain induced barrier lowering (DIBL) is more pronounced for short channel devices. The DIBL effect can switch on a device which should be "never on" and make it conduct a significant amount of current at high drain voltages.

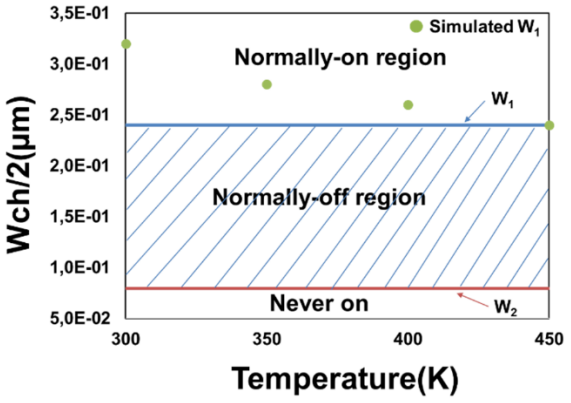

Figure 8, channel width limitations for a p-type JFET calculated with formula 7 for a channel doping of 5×10^{16} cm^{-3} and comparison with TCAD simulations (green points). W_1 (blue line) and W_2 (red line) have been calculated considering full activation and substituting V_G=0 V and $\Psi_{bi}(T)+V_G$=0.5 V in equation 7(a) respectively.

STEP 4

TCAD simulations were performed based on the previous considerations in order to fulfil the primary targets (min R_{on_spec}, punch-through breakdown avoided and high temperature normally-off operation). In this set of simulations, a value of L'(d-g) is fixed at 2 µm and the avalanche generation has been disabled. As it will be explained later on, the L'(d-g) distance slightly influences only the on-state performances of the device and does not affect at all the PT (punch-through) breakdown which is mainly regulated by the channel length L_{ch}.

Table 4. JFET's parameters varied in the TCAD simulations.

L_{ch}	0.5 µm to 5 µm.
$W_{ch}/2$	0.1 µm to 0.5 µm.
p-doping	1×10^{15} cm^{-3} to 1×10^{17} cm^{-3}.

The channel length has a key role in the design of the normally-off JFET. This is because a high value of this parameter ensures a high blocking voltage avoiding the PT breakdown as shown in figure 9.

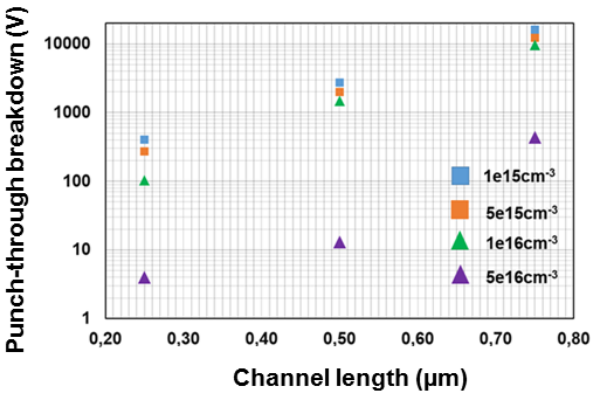

Figure 9, punch through breakdown vs channel length for different doping concentrations and for a fixed $W_{ch}/2$ of 0.2µm. Punch through breakdown occurs when the potential energy barrier in the channel region lowers at high drain voltage and allows the flow of carriers (holes) from the source to the drain contact. This effect must not be confused with the PT design of the gate-drain region[21].

On the other hand, from TCAD simulations it has been found that the main contribution of the R_{on_spec} [54] is given by the specific channel resistance, R_{ch_spec} (more than 90% of the total R_{on_spec}).

As shown in the equation 8(a), R_{ch_spec} is proportional to the channel length (L_{ch}), the channel mobility (μ_{ch}) and the number of activated dopants in the channel (function of the gate voltage) $N_{ch}(V_G)$. Additionally, the specific drift resistance R_{drift_spec} (8b), which is the sum of the gate-source and drain-source specific resistance (R_{GS_spec} and R_{GD_spec}, respectively), is proportional to the total drift length (L_{drift}) which is the sum of L'(s-g) and L'(d-g), the drift mobility (μ_{drift}) and the number of activated dopants in the drift region (N_{drift}).

The total R_{on_spec} (8c) is the sum of the specific resistance of the drift region (R_{drift_spec}), the channel region (R_{ch_spec}) and the contacts (R_{cont_spec}). Nevertheless, the resistance of the gate, drain and source contacts (R_{cont_spec}) has been neglected in this study.

$$R_{ch\_spec} = \frac{L_{ch}}{q\mu_{ch}N_{ch}(V_G)} \qquad 8(a)$$

$$R_{drift\_spec} = \frac{L_{drift}}{q\mu_{drift}N_{drift}} = R_{GS\_spec} + R_{GD\_spec} \qquad 8(b)$$

$$R_{on\_spec} = R_{ch\_spec} + R_{drift\_spec} + R_{cont\_spec} \qquad 8(c)$$

Since the R_{on_spec} is mainly due to the channel resistance, increasing L'(d-g) in PT can push upwards the BV (primary target) until PT ends up NPT, without lowering the on-state performance.

It is worth noting that the set of equations 8 for the specific on-state resistance applies to vertical JFETs and it has been calculated adopting the cross sectional area instead of the planar one[54].

STEP 5

Designs which did not guarantee normally-off characteristics until Topt and were subjected to the PT breakdown have been discarded in this step of the optimization. Then, the selection of the best performing device has been based on the minimum R_{on_spec} at RT and at Topt. In the end, the L'(d-g) distance has been increased to fulfil the specification on the minimum breakdown voltage. At the end of the procedure, the final design has the following features:

Table 5. Final specifications for the optimized normally-off JFET

W_{ch}	p-doping	L_{ch}	L'(d-g)	Topt
0.4 µm	$5\times10^{16}cm^{-3}$	1 µm	5 µm	450 K

Table 6. Avalanche breakdown as a function of the temperature and the gate-drain length. The 1D minimum length of the drift region (2µm) does not allow to reach a BV=2kV because of the 2D effects occurring at the D-G junction.

L'(d-g)	**2 µm**	**5 µm**	**10 µm**
T=300 K	BV=1.4k V	BV=2.1k V	BV=2.1k V
T=450 K	BV=1.6 kV	BV=2.7 kV	BV=2.7 kV

An optimum value of 5 µm for this dimension has been found for a p-doping concentration of 5×10^{16} cm^{-3}. Increasing L'(d-g) over 5µm has only detrimental effects in terms of R_{on_spec} (primary target) and does not improve the breakdown capability of the JFET.

Further simulations with small variations of the parameters around the optimum configuration set have been conducted. However, a small reduction of the channel length, which is the main component of the R_{on_spec}, is detrimental for the PT breakdown as much as an increase of the channel width or of the channel doping.

4. TCAD results and discussion

Once the optimum design has been identified, TCAD simulations have been carried out in order to analyse the on-state and off-state performance of the final device. In figure 10, the RT on-state characteristics confirm that the device effectively behaves as a normally-off JFET.

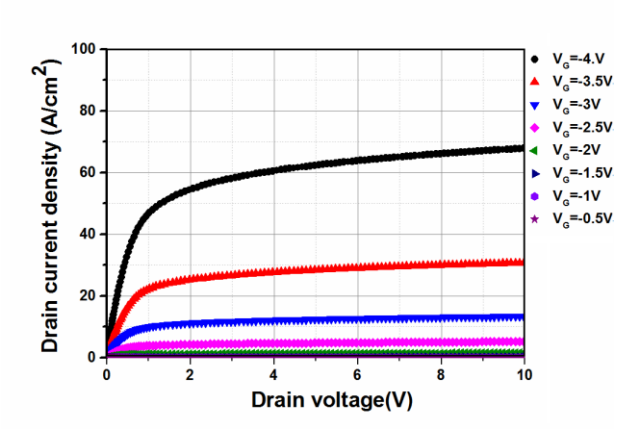

Figure 10, RT J_D-V_{DS} on state characteristics of the optimum normally-off JFET for different gate bias.

The transfer characteristic in figure 11 illustrates that the optimum design is normally-off until the maximum temperature of 600 K (which allows to be inside the optimal resistivity window) and the threshold voltage ensures a good control in the unipolar mode (before the pn junction turns on). For the same design specifications, the R_{on_spec} of a normally-off JFET with L_{ch}=2L_{ch} (optimum) is almost doubled, confirming the predominance of the channel resistance on the total R_{on_spec}.

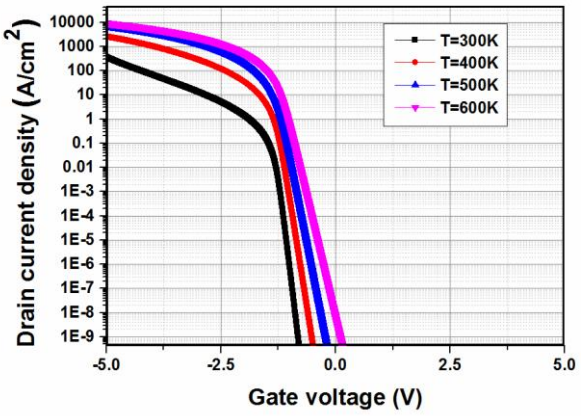

Figure 11, Transfer characteristics J_D-V_{GS} of the JFET at different temperatures for a fixed V_{DS}=-10 V. As it can be observed from the curves, the device becomes normally-on at 600 K (maximum temperature) since the threshold voltage becomes negative. The threshold voltage (Vth) is ~1V at RT and it reduces until ~0.4 V at the Topt , so guaranteeing a margin similar to the device reported in [18].

Breakdown voltage simulations showed that the avalanche phenomenon was responsible for the high increase in the current density (figure 12) and that the PT breakdown was effectively avoided by a correct design of the device (in terms of channel length and channel doping) also at high temperature.

The positive coefficient of the breakdown voltage (table 6) is indeed a clear signal of the avalanche phenomenon. In fact, the acceleration of minority carriers in the N+P (gate-channel) junction is reduced at high operational temperature because of the decreased impact ionization rate (equation 6).

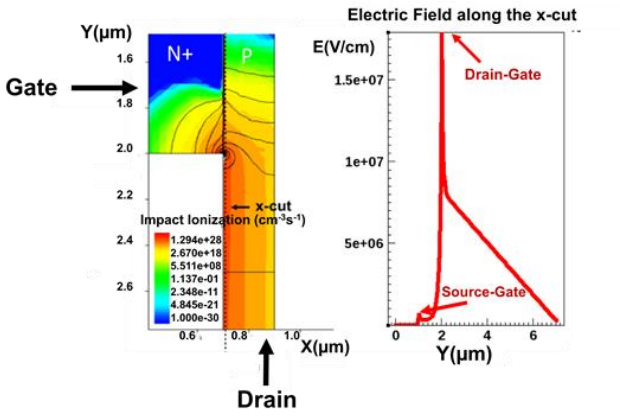

Figure 12, 2D electric field distribution and impact ionization at the RT breakdown voltage (2.1kV) for the normally-off optimum JFET. The peak of the electric field is located near the gate-drain junction, where the avalanche generation occurs. The electric field reaches 0 V/cm before the drain contact, confirming the NPT design of the gate drain region, as it can be also deduced from the results of table 6.

In the bar charts of figures 13,14 and 15 the performances of the normally-off device were compared with other diamond JFETs (in both unipolar/bipolar mode and normally-on/off configurations). At RT(fig.13), the R_{on_spec} of the optimized enhancement mode JFET shows only a small reduction if compared with the bipolar mode JFET [56] and a reduction if compared with the state-of-the-art unipolar mode normally-on diamond JFET [14, 49]. At high temperature (fig.14), the optimized JFET shows similar performances if compared with the bipolar mode JFET and it outperforms the other normally-on configurations.

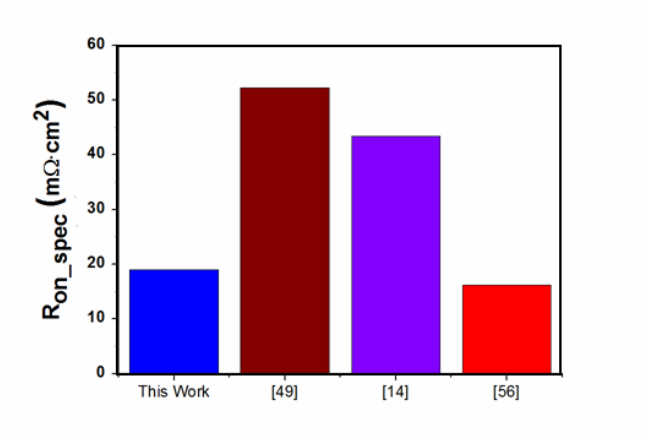

Figure 13, R_{on_spec} comparison between experimental results of diamond JFETs[14, 49, 56] and the optimised theoretical value for normally-off JFET at RT. R_{on_spec} has been calculated with the reference to the cross section and it applies to future vertical JFETs.

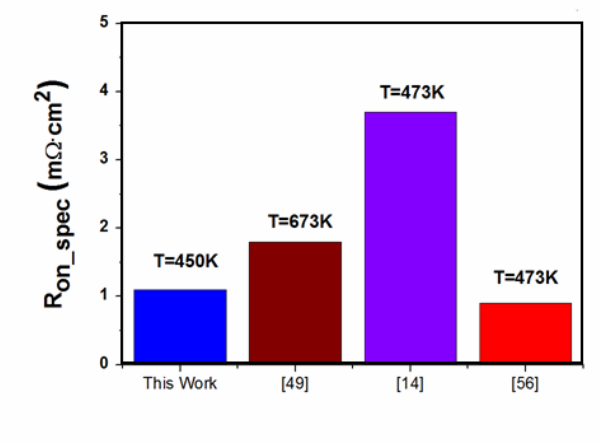

Figure 14, R_{on_spec} comparison between experimental results of diamond JFETs [14, 49, 56] and the optimised theoretical value for normally-off JFET at high temperature.

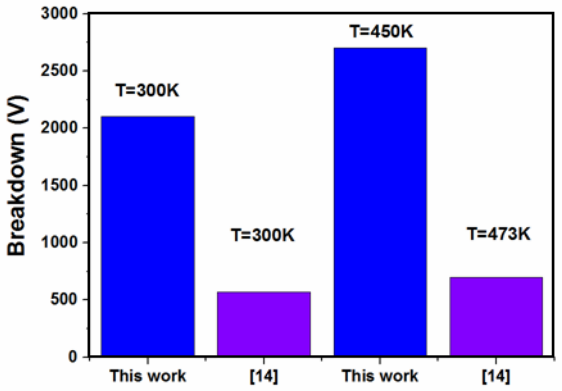

Figure 15, breakdown voltage comparison of our theoretical optimized device and the diamond normally-on JFET reported in [14].

Conclusions

An optimization technique for normally-off diamond JFETs has been proposed and described in this paper. The temperature effect on the incomplete ionization of the dopants has proven to be the main limiting factor in designing diamond JFETs with normally-off behaviour. A TCAD model was calibrated against existing data and an optimised structure was proposed which shows substantial improvement over the reported state of the art JFETs. It is however acknowledged that present technological tolerances of the parameters (such as the channel width and doping) could currently represent an obstacle for the fabrication of the diamond JFET proposed in this paper.

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