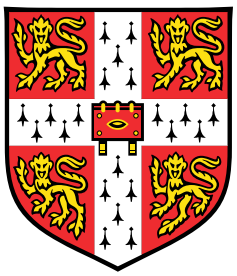
TFT's Circuit Simulation Models and Analogue Building Block Designs



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I would like to dedicate this thesis to my loving parents
and my beautiful and considerate wife …

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Abstract

Building functional thin-film-transistor (TFT) circuits is crucial for applications such as wearable, implantable and transparent electronics. Therefore, developing a compact model of an emerging semiconductor material for accurate circuit simulation is the most fundamental requirement for circuit design. Further, unique analogue building blocks are needed due to the specific properties and non-idealities of TFTs.

This dissertation reviews the major developments in thin-film transistor (TFT) modelling for the computer-aided design (CAD) and simulation of circuits and systems. Following the progress in recent years on oxide TFTs, we have successfully developed a Verilog-AMS model called the CAMCAS model, which supports computer-aided circuit simulation of oxide-TFTs, with the potential to be extended to other types of TFT technology families.

For analogue applications, an accurate small signal model for thin film transistors (TFTs) is presented taking into account non-idealities such as contact resistance, parasitic capacitance, and threshold voltage shift to exhibit higher accuracy in comparison with the adapted CMOS model. The model is used to extract the zeros and poles of the frequency response in analogue circuits.

In particular, we consider the importance of device-circuit interactions (DCI) when designing thin film transistor circuits and systems and subsequently examine temperature- and process-induced variations and propose a way to evaluate the maximum achievable intrinsic performance of the TFT. This is aimed at determining when DCI becomes crucial for a specific application. Compensation methods are reviewed to show examples of how DCI is considered in the design of AMOLED displays.

Based on these design considerations, analogue building blocks including voltage and current references and differential amplifier stages have been designed to expand the analogue library specifically for TFT circuit design. The V_T shift problem has been compensated based on unique circuit structures.

For a future generation of application, where ultra low power consumption is a critical requirement, we investigate the TFT's subthreshold operation through examining several figures of merit including intrinsic gain (A_i), transconductance efficiency (g_m/I_{DS}) and cut-off frequency (f_T). Here, we consider design sensitivity for biasing circuitry and the impact of device variations on low power circuit behaviour.

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Chapter 1

Introduction

The wide usage of amorphous silicon (a-Si:H) thin film transistors (TFT) in TFT-LCD display [**?**] which dates back to the 1980s has boosted research on materials and the processing technology of TFTs [**? ?**], and has subsequently enables another success in organic displays [**?**].

Further improvements in TFT device performances and its flexibility, transparency, roll-to-roll compatibility and low cost make them promising in many other applications such as radio-frequency identification (RFID) tags [**?**], sensors [**?**] and wearable devices. In order to reduce the integration complexity and system cost, a system-on-panel approach has been pointed out aiming at producing all kinds of circuit building blocks on a single substrate [**?**].

Although circuit blocks such as logic gates [**?**], amplifiers [**?**] and analogue-to-digital coverters (ADCs) [**?**] have been reported in recent years, the capability of TFT circuits is still low. Complex systems with only TFTs are still lacking, especially for TFT analogue circuits and applications. The reasons are various. Firstly, due to the ever-changing nature of the semiconductors used in newly developed TFT technologies, device models can vary because of changes in the underlying physics. However, an accurate model for newly developed technology is essential for circuit design. Secondly, the design flexibility of TFTs is not comparable with the well-developed silicon metal–oxide–semiconductor field-effect transistors (MOSFET) or even bipolar junction transistors (BJTs). Lacking complementary semiconductors and the capability of making enhancement and depletion TFTs on the same substrate, many existing circuit blocks are not directly usable thus limiting the flexibility of designing TFT circuits.

Therefore, the dissertation as a whole is dedicated to exploring and synthesising a more accurate model specifically for circuit simulation along with development of essential building blocks for analogue circuits so as to build a bridge between the existing circuit topologies to the TFT domain.

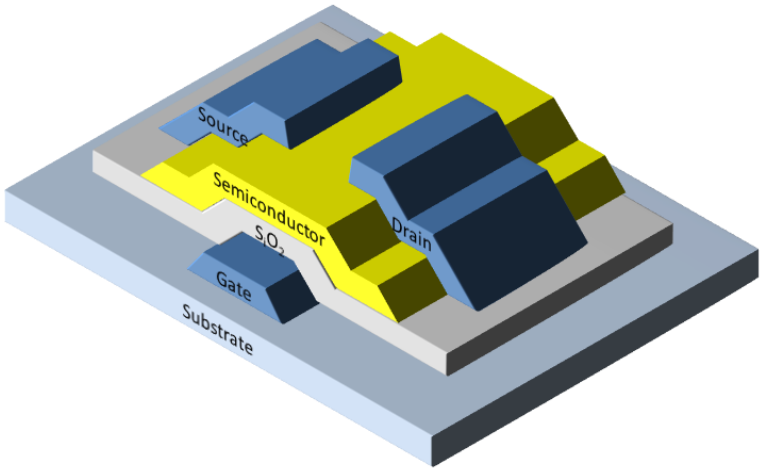


Fig. 1.1 Conceptual structure of a bottom-gate TFT.

1.1 Thin-Film Transistors

It is surprising to find out that the first concept of the thin film transistor dates back to the 1930s, even before the first point contact transistor was demonstrated. The early failure of the attempt to make TFT devices and the later success of the crystalline silicon devices lead to an abandonment of the TFT concept in the industry until a killer application was identified, i.e. the TFT-LCD, in the 1980s [**?**]. Extensive research on different materials started from then on.

The TFT by definition is “a field effect transistor made of nonsingle crystal semiconductor film deposited on an insulating substrate”, quoting the definition used in [**?**]. A conceptual figure of a TFT structure is shown in Fig. 1.1 where a bottom-gate structure is used. The device is designed following the same principle as other field effect transistors. The rule of thumb is that under working conditions, the vertical electric field through semiconductor is much higher than the horizontal electric field along the surface of the semiconductor. Therefore, the gate electrode can have dominating control over the semiconductor characteristics.

By virtue of its working principle, a TFT is the same as a floating body MOSFET. However, as semiconductors used in these devices are normally amorphous or poly-crystalline, the effective mobility if much lower than single crystal silicon in MOSFETs, yielding a much lower operating current. This motivates researchers to improve the effective mobility of TFTs in subsequent years.

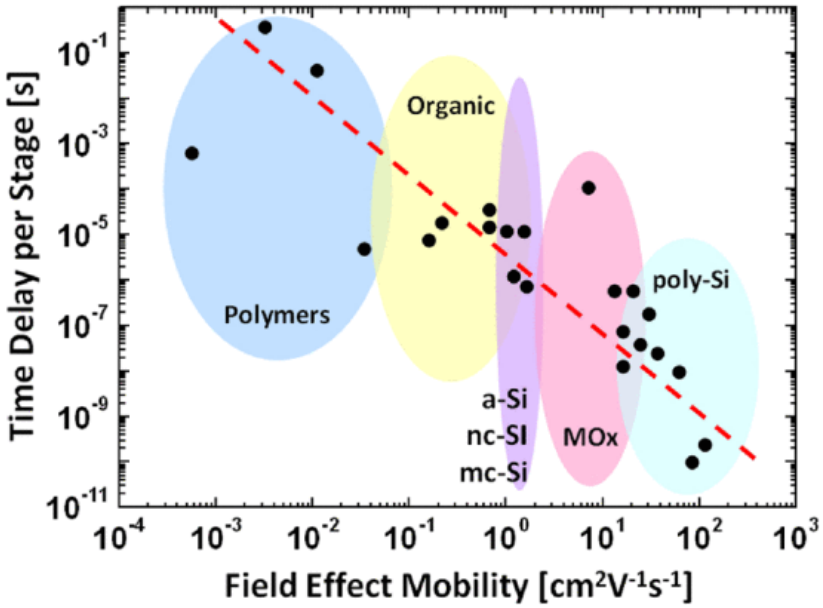


Fig. 1.2 Field effect mobility and stage delay for different semiconductor families. Captured from [**?**].

Up until now, many alternative materials have been found to exhibit higher or comparable effective mobility against the first widely used TFT technology which is based on a-Si. Fig. 1.2 lists the mobility achieved in a range of different semiconductor materials [**?**].

Among the materials listed in Fig. 1.2, metal-oxide semiconductors stand out as the potential leading semiconductor material for TFTs as they exhibit high mobility and good uniformity in large scale and amenable to low-temperature fabrication. In addition, metal oxide semiconductors are very promising for transparent and flexible electronics due to their wide bandgap. Therefore, it will be used as the main consideration in developing the models and circuit blocks in this dissertation.

1.2 TFT Enabled Flexible and Transparent Electronics

The low processing temperature of TFT technologies such as a-Si:H, metal oxide and organic TFTs has made them compatible with several flexible substrates, for example, plastic or paper substrates. This directly makes large-area, low cost, roll-to-roll, transparent and flexible systems promising [**?**]. Prototypes of flexible displays, digital circuits and amplifiers have been reported in recent years demonstrating the possibility of realising modern electronics in a different and flexible manner [**? ? ? ? ? ?**]. Several examples are shown in Fig. 1.3.

Another promising approach for flexible electronics lies in healthcare. Lower power consumptions is a critical requirement in health care monitoring systems especially when

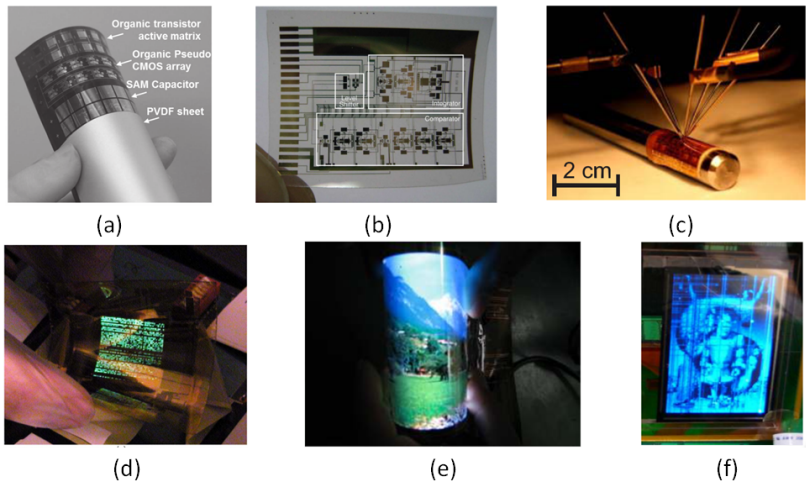


Fig. 1.3 Flexible circuits and displays with TFTs (a) stress sensor array with built-in amplifiers (b) $\Sigma - \Delta$ ADC (c) op-amp (d-f) flexible and transparent displays. Figures are captured from [**?** **?** **?** **?** **?** **?**].

continuous monitoring is needed in daily life, and in implantable applications where long lifetime is of concern. As TFTs are generally working at a lower current level compared with silicon MOSFET technology, they are naturally more suited for low power applications. Recent research has reported that ultra-low power working (<1nW) is possible [**?**] when biasing TFTs in the subthreshold region, which could potentially lead to battery-less systems.

It is worth mentioning that although many prototype applications have been demonstrated, building a full system on a flexible substrate is still very challenging as in most applications, rigid crystalline silicon-based integrated circuits or components are still needed in biasing and operating the TFT circuits, which are not currently replaceable with TFT circuits.

1.3 Research Goals

To enable various functionalities efficiently, TFT circuit designs and simulations are indispensable. However, the simulation platforms for newly emerging technologies are not readily available. For a-Si TFTs, the well-known RPI model [**?**] has become a commercial standard supported by many simulation platforms including SmartSpice, HSPICE, Spectre, etc where designers can easily simulate various circuits with adequate accuracy.

However, as a newly emerging technology, no computer-aided design (CAD) tool for metal-oxide TFTs has yet become a standard despite the improved performances compared with a-Si. In order to accurately simulate circuits and design various functions with metal oxide TFTs, we need to first investigate both the static and dynamic models in a simulation en-

vironment. Subsequently, building blocks at the bottom level should be engineered to connect TFT designs with the well-researched silicon complementary metal-oxide-semiconductor (CMOS) circuit and systems.

Therefore the main goal of the dissertation is as follows:

1. Investigate compact modelling for circuit simulations.
2. Investigate linear models for design simplicity, and develop an accurate small signal model specifically for TFTs.
3. Design building blocks for bottom level analogue circuits in order to build a bridge between the TFT circuit design with the well studied CMOS designs.

1.4 Thesis Organization

The dissertation includes 5 chapters and 2 appendices. This first chapter introduces the background and the motivation of the research and explains the main goal of this research. Chapter 2 mainly reviews the CAMCAS model developed in Cambridge where a lot of work has been completed from previous efforts. Chapter 3 investigates the widely used CMOS small signal model and the inadequacy of its application in TFTs. A new model is developed taking into consideration of non-idealities in TFT devices. In Chapter 4, several building blocks for analogue circuits are designed and simulated with the CAMCAS model. The design of a supply independent op-amp is presented. Chapter 5 concludes this dissertation and discusses possible extensions of this research.

The two appendices discuss the device circuit interaction (DCI) and subthreshold circuit possibilities of TFT devices. In particular Appendix A considers DCI that happens in TFT circuit designs and available approaches are reviewed. Thermal and geometric variations are measured and the effects on simple analogue circuit performance are analysed. Based on the knowledge developed in the above chapters, Appendix B evaluates the analogue performance and the design difficulties in the newly proposed way of biasing Schottky-barrier TFTs in subthreshold region, which extends the subthreshold modelling of Chapter 2.

Chapter 2

TFT Compact Modelling

2.1 Computer Aided Design

The growing maturity of thin film transistor (TFT) technology coupled with newly emerging materials and processes are enabling integration of circuits and systems for a new family of applications ranging from biosensing systems to areas augmenting displays and imaging [**? ? ? ?**]. The design of systems places great demand for fast computer aided design (CAD) tools to accurately and reliably predict system behaviour.

CAD always requires accuracy, high speed and reliable convergence of device models. In order to achieve high accuracy in all working regions without use of many fitting parameters, a good understanding of device physics is needed. However, physical models are not necessarily sufficient for good CAD in the sense that the equations could be complex, which can lead to slow execution or convergence problems. Therefore, simplification of the model equations without sacrificing accuracy is one of the major requirements for a good CAD model. In addition, the model should be adaptive to a wide range of technological/process parameters through simple extraction procedures.

During the past 30 years, a great amount of effort has been made in the TFT modelling area for various semiconductor technologies, including amorphous silicon [**? ? ? ? ? ? ?**], polysilicon [**?**], organics [**? ? ? ? ?**] and metal oxides [**? ? ? ? ? ? ?**]. For a-Si TFTs, several SPICE models have been developed. Specifically, the model developed by Rensselaer Polytechnic Institute, also known as the RPI model [**?**], has become a commercial standard supported by many simulation platforms including SmartSpice, HSPICE, Spectre, etc. However, no CAD tool for organic and metal-oxide TFTs has yet become a standard due to the rapid evolution of materials and device structures.

In this chapter, we will review the major contributions to the TFT modelling area and compare the differences between Verilog-AMS and SPICE from the standpoint of compact

device modelling. Finally, we present the implementation of the Cambridge TFT compact model [**?**] for oxide TFTs in Verilog-AMS for Spectre simulation. The major goal of this review is to give the reader guidelines for implementing device models for the CAD of circuits and systems.

2.1.1 Physical and Empirical Modelling

Physical and empirical modelling approaches are generally aimed at providing an accurate model for a given transistor or transistor family, which covers all working regions of the device. While the major consideration is accuracy, the developed model is not necessarily physical. In this sense, it is theoretically possible to use polynomial approximation or other empirical ways to fit any kind of transistor behaviour with acceptable accuracy. However, without a proper understanding of the underlying device physics, the resulting number of fitting parameters could be large and difficult to extract from measurements since the model should cover a wide range of different bias conditions and transistor scales. Therefore, the transistor models used in a simulator are often a combination of terms and coefficients that are physically and empirically based.

Recent efforts have primarily focused on physically-based approaches in an attempt to develop simple and accurate models. The most well-studied material for TFTs is amorphous silicon (a-Si:H). Several models have been developed based on different distributions of deep states and tail states of the semiconductor to describe static and dynamic behaviour for the above and subthreshold regions [**? ? ?**]. Other properties including trap related V_T shift [**?**] and the off/leakage currents [**?**]. The RPI model [**?**] captures most of the device properties leading to satisfactory simulation results and thus has been widely used.

For organic TFTs, researchers have developed models based on multiple trapping and release (i.e. trap-limited conduction) [**?**] and variable range hopping (VRH) [**? ? ?**]. However, due to the diverse use of materials in the TFT, the underlying physics differs, and therefore a trend has emerged to develop a model that is unified but less physical [**?**].

As for metal oxide TFTs, modelling efforts are still in their infancy, although there are growing interests in the area for implementation of circuits and systems. In what follows, early efforts in compact models for CAD of oxide TFTs are reviewed.

2.2 Cambridge's TFT Models

Compared with a-Si TFTs, the oxide system has unique properties, which need to be captured. For example, localised traps or band tail states in oxides do not exist to the same extent as

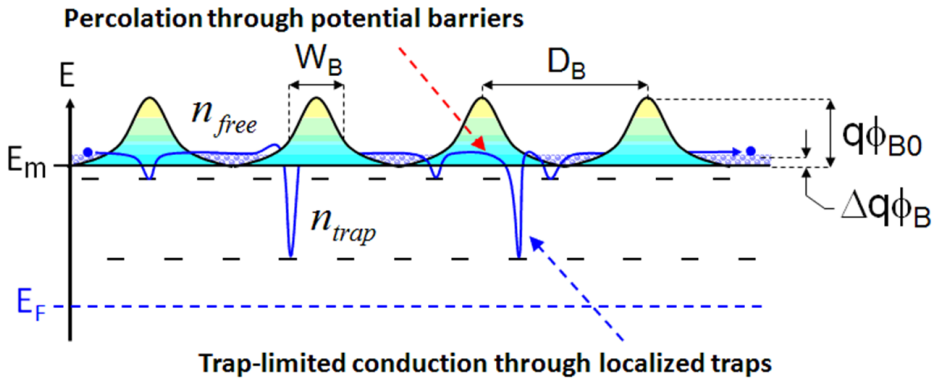


Fig. 2.1 Carrier transport combining percolation with trap-limited conduction (TLC) for oxide semiconductor TFTs (Here, D_B and W_B denote spatial distance and width of potential barriers, respectively)

a-Si [**?**]. Their tail state density is much lower and hence trap-limited conduction is generally insignificant [**? ?**]. In addition, more complex systems such as amorphous indium gallium zinc oxide (a-IGZO) can have compositional disorder due to the random distribution of metal constituents [**? ?**]. This gives rise to potential barriers above the conduction band minima (E_m), suggesting the presence of percolation conduction [**? ? ?**].

In the following, compact models for the terminal current-voltage behaviour are presented taking into account the different transport mechanisms in the device for the above- and sub-threshold regions of TFT operation. The former is based on a mobility model that combines trap-limited conduction (TLC) with percolation conduction. The latter takes into account diffusion and drift current components [**?**]. A unified model is then presented that covers both regions based on a single expression that uses a reference turn-on voltage V_{on} rather than V_T [**?**]. Good agreement with measured terminal characteristics is obtained over the entire range of gate-source voltage (V_{GS}) > V_{on} for the test TFTs with an a-IGZO channel.

2.2.1 Above-Threshold Model

As illustrated in Fig. 2.1, oxide TFTs have potential barriers above E_m due to compositional disorder, suggesting percolation conduction when electrons are released into the conduction band. Moreover, there are localised tail states within the gap states, implying trap-limited conduction. In particular, oxide semiconductors can have a shallow slope of the tail states (kT_t) $\sim 20meV$, smaller than the thermal energy (kT) at $300K$, leading to different mobility behaviour. This suggests that the field effect mobility (μ_{FE}) model needs to be modelled based on TLC and percolation conduction, although the former is not as significant as compared to a-Si.

1. Trap-limited conduction (TLC)

   Effect of trap-limited conduction (TLC) can be considered as μ_{FE} being proportional to ratio (γ_{TLC}) of free carrier density (n_{free}) and trapped carrier density (n_{trap}), yielding $\gamma_{TLC} = n_{free}/(n_{free}+n_{trap})$. Here, $n_{free} = N_C exp[(E_F - E_m)/kT]$, where N_C is effective density of states in conduction band and kT the thermal energy. And the expression for n_{trap} is approximated with $kT_t < kT$ using exponential distribution of tail states. This yields $n_{trap} = N_{tc} kT_t exp[(E_F - E_m)/kT]$, where N_{tc} is the density of trap states at conduction band edge. Now, we have γ_{TLC} as just a constant,

$$\gamma_{TLC} \equiv \frac{n_{free}}{(n_{free}+n_{tail})} \approx \frac{N_C}{N_C + N_{tc} kT_t} \tag{2.1}$$

2. Percolation Conduction

   Percolation conduction associated with potential barriers above E_m can be considered as mobility scaled from band mobility (μ_0), assuming Gaussian random distribution of potential barriers with the mean (ϕ_{B0}) and the variance (σ_{B0}). This yields $\mu_0^* = \mu_0 exp[-q\phi_{B0}/kT + (q\sigma_{B0})^2/(kT)^2]$. Here, ϕ_{B0} can be reduced by $\Delta\phi_{B0}$ due to thermally released electrons, depending on Fermi level change (ΔE_F), as described in Fig. 2.1. The thermally reduced barrier height can be expressed as $\phi_{B0} exp(-\gamma_B \Delta E_F/kT)$, where $\gamma_B \equiv (D_B - W_B)/D_B$, which can be approximated as $\phi_{B0}(1-\gamma_B \Delta E_F/kT)$ when $\gamma_B \Delta E_F/kT << 1$ by Taylor expansion. Thus, $\Delta\phi_{B0}$ is defined as $\gamma_B \Delta E_F/kT\phi_{B0}$. These conditions yield the percolation mobility (μ_{Per}) as follows,

$$\begin{aligned} \mu_{Per} &\equiv \mu_0 exp\left(-\frac{q(\phi_{B0}-\Delta\phi_B)}{kT} + \frac{(q\sigma_{B0})^2}{2(kT)^2}\right) \\ &= \mu_0^* exp\left(\frac{\gamma_B \Delta E_F}{kT}\phi_{B0}\right) \end{aligned} \tag{2.2}$$

   where $\mu_0^* = \mu_0 exp[-q\phi_{B0}/kT + (q\sigma_{B0})^2/2(kT)^2]$ considered as an effective band mobility.

3. Combined Mobility Model with V_{GS} dependence

   In Eq. (2.2), the ΔE_F is controlled by gate voltage (V_{GS}). The relationship between them can be derived by solving Poisson's equation, yielding $\Delta E_F = 2(kT/q) ln[C_{ox}(V_{GS} - V_T)/Q_{ref}]$, where C_{ox} is gate-insulator capacitance, V_T threshold voltage, and $Qref \equiv \{2\varepsilon_S N_C kT exp[(E_{F0} - E_m)/kT]\}^{0.5}$. Combining TLC with percolation from Eqs. (2.1) to (2.2), we now have the V_{GS} dependent mobility relation,

$$\mu_{FE} \equiv \mu_{Per}\gamma_{TLC} \quad = \mu_0^* \left(\frac{N_C}{N_C + N_{tc}kT_t}\right)\left(\frac{C_{ox}}{Q_{ref}}\right)^{\alpha_p}(V_{GS}-V_T)^{\alpha_p} \tag{2.3}$$

As can be seen, Eq. (2.3) follows a power law. Here, $\alpha_p \equiv 2q\phi_{B0}\gamma_B/kT$, related to percolation. In Eq. (2.3), TLC affects the constant term, while the exponent is determined by percolation.

4. Current-Voltage Relation

With Eq. (2.3) and the definition of drift current: $I_{DS} = \mu_{FE}C_{ox}(V_{GS}-V_T-V_{ch})\mathrm{d}V_{ch}/\mathrm{d}x$, current-voltage relation $I_{DS}(V_{GS})$ can be derived with the integral ranges: x=0 to L and channel potential $(V_{ch}) = 0$ to V_{DS},

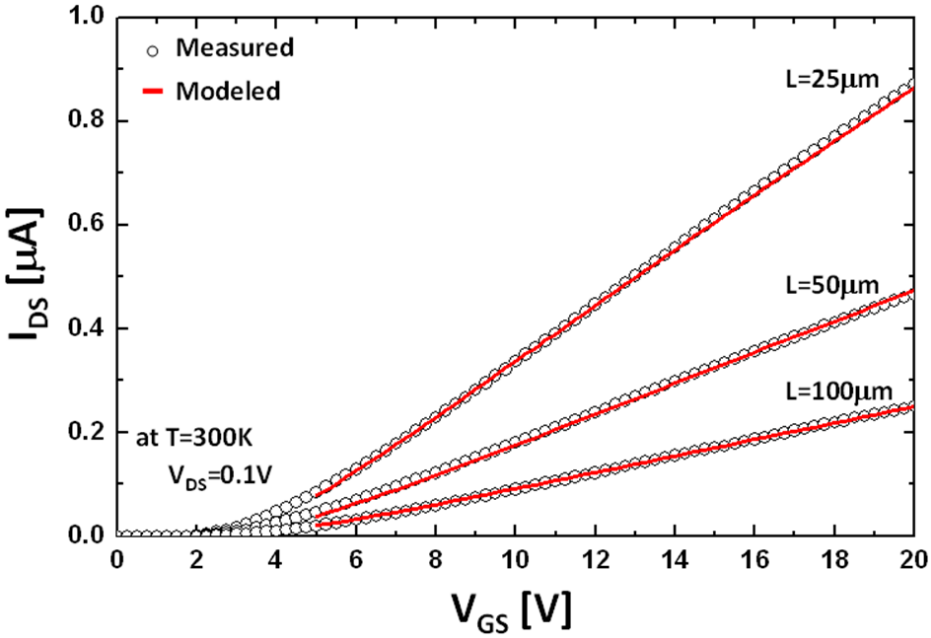
$$I_{DS} \equiv \mu_0^* \left(\frac{N_C}{N_C + N_{tc}kT_t}\right)\frac{W}{L'}\frac{C_{ox}^{\alpha_p+1}}{Q_{ref}^{\alpha_p}}(V_{GS}-V_T)^{\alpha_p+1}V'_{DS} \tag{2.4}$$

In Eq. (2.4), L' is defined as $L-\Delta L$, where ΔL is effective channel length reduction, and effective drain voltage $V'_{DS} = V_{DS} - 2R_C I_{DS}$, where R_C is contact resistance. For saturation region expression, Eq. (2.4) can be reformed with a saturation parameter (β_{sat}), replacing V'_{DS} by $\beta_{sat}(V_{GS}-V_T)$. Fig. 2.2a shows a comparison between measured and modelled transfer characteristics (I_{DS} vs. V_{GS}) at $V_{DS} = 0.1V$, providing a good agreement. The measured saturation characteristics at $V_{DS} = 20V$ is also well matched with the modelled results, as seen in Fig. 2.2b.

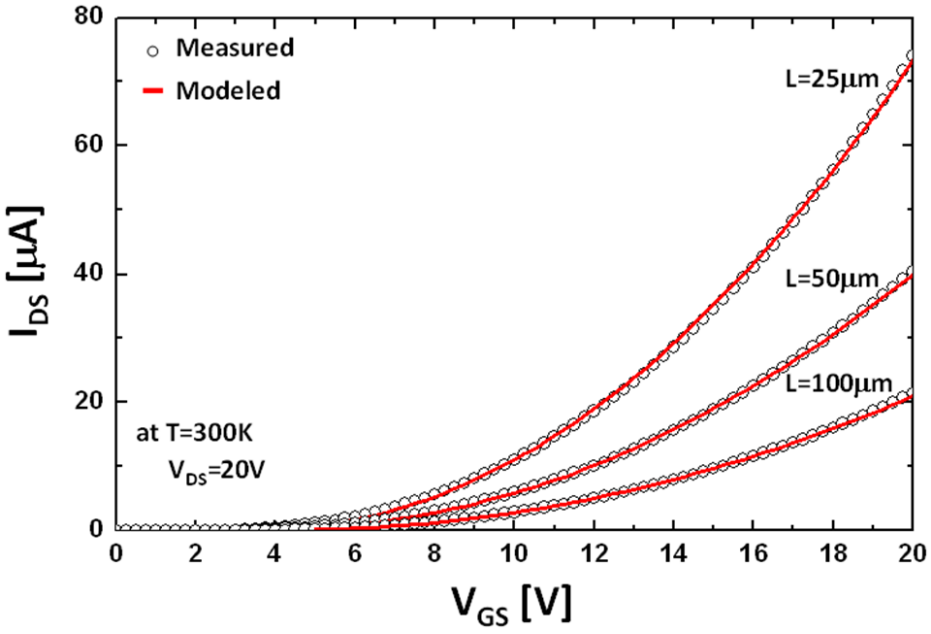
To check the model validity for temperature dependency, we measured and simulated the drain current as a function of gate bias for different temperatures, e.g. $100K$, $200K$, and $300K$, respectively. As seen in Fig. 2.3a, there is good agreement between the measurements and the model, Eq. (2.4). For purposes of validation, the modelled values of exponent (α_p) in the power-law, Eq. (2.4), are compared with the extracted values from the best fit since it has a unique signature of percolation conduction, i.e. $a = \alpha_p + 1 \equiv 2q\phi_{B0}\cdot\gamma_B/kT + 1$. As seen in Fig. 2.3b, the proposed percolation model for $\phi_{B0}\cdot\gamma_B = 2.5meV$ shows better agreement compared to the conventional model (e.g. trap-limited conduction model with $a = 2kT_t/kT - 1$ for $kT_t = 30meV$).

2.2.2 Subthreshold Model

The subthreshold current in the limit of low V_{GS} shows a linear dependence on V_{GS} in a semi-log plot, as illustrated in Fig. 2.6, suggesting diffusion current, as follows,

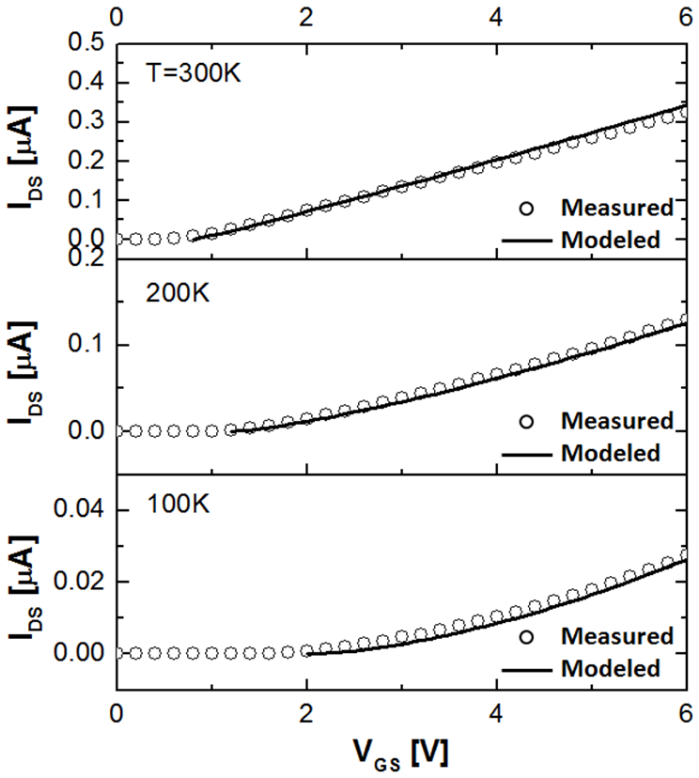


(a) linear region with a small drain voltage (V_{DS}) of $0.1V$

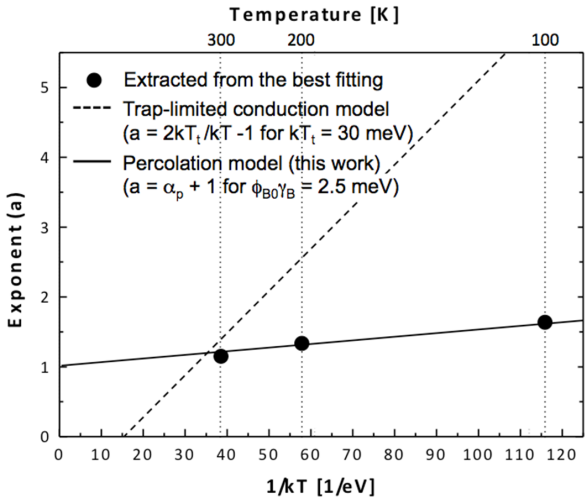


(b) saturation region with a high V_{DS} of $20V$

Fig. 2.2 Comparison between measured and modelled transfer characteristics (I_{DS} vs. V_{GS}) for the above-threshold region. For each region, a good agreement between measurement and modelling is achieved.



(a) Measured and modeled I_{DS}-V_{GS} for above-threshold region at $V_{DS} = 0.1V$ for different temperatures (100K, 200K, 300K, respectively)



(b) Retrieved exponent (a) vs. temperature

Fig. 2.3 Comparison between measured and modelled transfer characteristics at different temperatures. Here, the proposed model shows a better agreement compared to the conventional model (e.g. trap-limited conduction model).

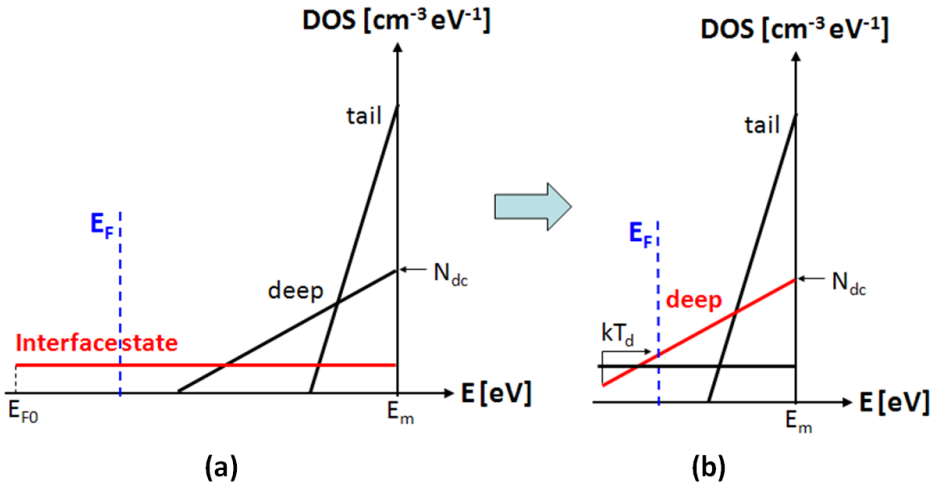


Fig. 2.4 Density of states profile with (a) Fermi level within interface states at low gate voltage, and (b) the case of deep states dominant with increasing gate voltage corresponding Fermi level now within deep states.

$$I_{Diff} \approx \mu_0 \frac{kT}{q} \frac{W}{L'} Q_{fi} exp\left(\frac{q}{kT}\left(\frac{V_{GS}-V_{FB}}{1+q^2 D_{it}/C_{ox}}\right)\right)\left(1-exp\left(-\frac{qV'_{DS}}{kT}\right)\right) \tag{2.5}$$

where μ_0 is the band mobility for electrons. Note that the subthreshold slope (SS) can be derived from Eq. 2.5 with the definition $\mathrm{d}V_{GS}/\mathrm{d}log I_{DS}$,

$$S \equiv ln10 \frac{kT}{q}\left(1+\frac{q^2 D_{it}}{C_{ox}}\right) \tag{2.6}$$

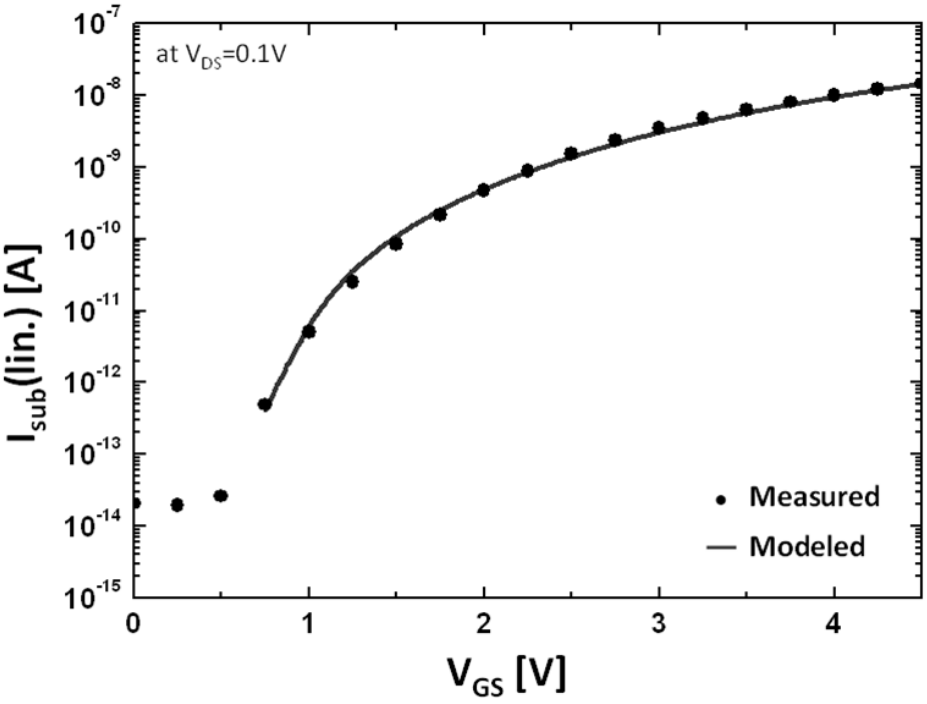
As described in Fig. 2.4, interface states are occupied first, followed by filling deep states located in the bulk at higher V_{GS}. So, as the E_F moves to the location of deep states for increasing V_{GS}, the drain current can be defined as a drift current (I_{Drift}),

$$I_{Drift} \approx \mu_0 \frac{W}{L'} \frac{C_{ox}^{\alpha_d+1}}{Q_d^{\alpha_d}} (V_{GS}-V_{FB})^{\alpha_d+1} V'_{DS} \tag{2.7}$$

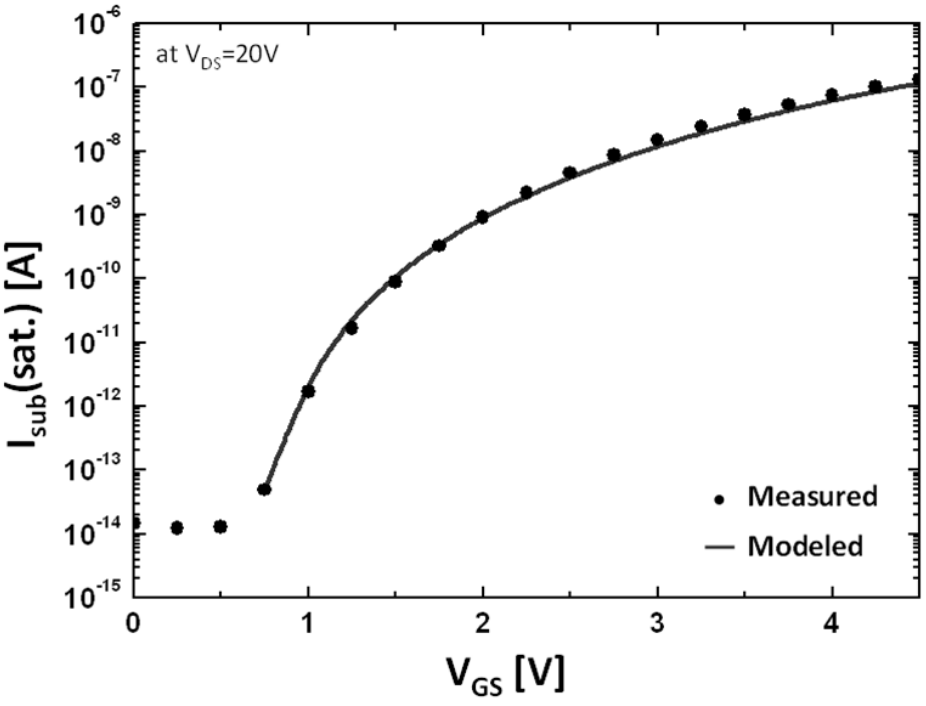
where Q_d is a reference charge density associated with deep states, α_d is power-law exponent defined as $2(T_d/T-1)$, and T_d is the characteristic temperature of deep states.

We now have the current-voltage relations for both diffusion and drift components as given by Eqs. (2.5) & (2.7). These equations can be combined as a total drain current (I_{sub}) in the subthreshold region using a harmonic average,

$$I_{sub} \equiv (I_{Diff}^{-m} + I_{Drift}^{-m})^{-1/m} \tag{2.8}$$



(a) linear region with $V_{DS} = 0.1V$



(b) saturation region with $V_{DS} = 20V$

Fig. 2.5 Measured and modelled subthreshold current (I_{sub}) as a function of V_{GS}

Table 2.1 Extracted Subthreshold Parameters at T=300K

Parameters	Value
SS	$0.19V/dec$
D_{it}	$1.64\times10^{11}cm^{-2}eV^{-1}$
I_{off}	$2\times10^{-14}A$
Q_{fi}	$7.05\times10^{-14}C/cm^2$
α_d	2.26
T_d	639K
Q_d	$7.8\times10^{-8}C/cm^2$

The examined TFT to verify this model, which is the same as that used in the previous sections, has the following geometrical and physical parameters (extracted in the previous sections): $W = 100\mu m$, $L = 100\mu m$, channel thickness $t_S = 40nm$, channel permittivity $\varepsilon_S = 11.5\varepsilon_0$ (where ε_0 is vacuum permittivity), $V_{FB} \sim 0.6V$, $V_T \sim 4V$, $C_{ox} = 11.5nF/cm^2$, $\mu_0 = 15cm^2/V\cdot s$, and $N_C = 5\times10^{18}cm^{-3}$ at $300K$. $2R_C \equiv R_{SD} = 9637\Omega$ for $W = 100\mu m$ (equivalent to $R_{SD}W = 96.37\Omega\cdot cm$) and $\Delta L = -3.5m$ ($L' = L - \Delta L = L + 3.5\mu m$). Other extracted model parameters are summarized in Table 2.1. Fig. 2.5 shows the measured subthreshold characteristics for a different V_{DS}, providing a good agreement with each other.

To validate the subthreshold model in terms of the diffusion component in the examined transistors, we measured the drain current for small V_{DS}=0.01, 0.1, and 1V. Comparing to the model, we get good agreement as seen in Fig. 2.6. In particular, as shown in the inset of Fig. 2.6, the measured I_{DS} vs. V_{DS} at the diffusion dominant region of V_{GS} (e.g. V_{GS} = 0.5V) is compared with the Eq. (2.5). Here, the dependence of the drain current on V_{DS} is found to follow the law of $(1-exp(-qV_{DS}/kT))$ of Eq. (2.5) which is a signature of the presence of the diffusion current.

Regarding continuity and symmetry of the compact model where above- and sub-threshold models are combined, the model was subject to the Gummel symmetry test (GST) [**?** **?**]. As seen in the inset of Fig. 2.7(a), V_X represents a symmetrical voltage applied on source and drain sides, respectively. Fig. 2.7 demonstrates perfect continuity and symmetry as a function of V_X even for the 4th derivative of I_{DS} with respect to V_X, suggesting it has successfully passed the GST. For this, we employed smoothness and continuity functions for the effective drain voltage and threshold voltage terms [**?**].

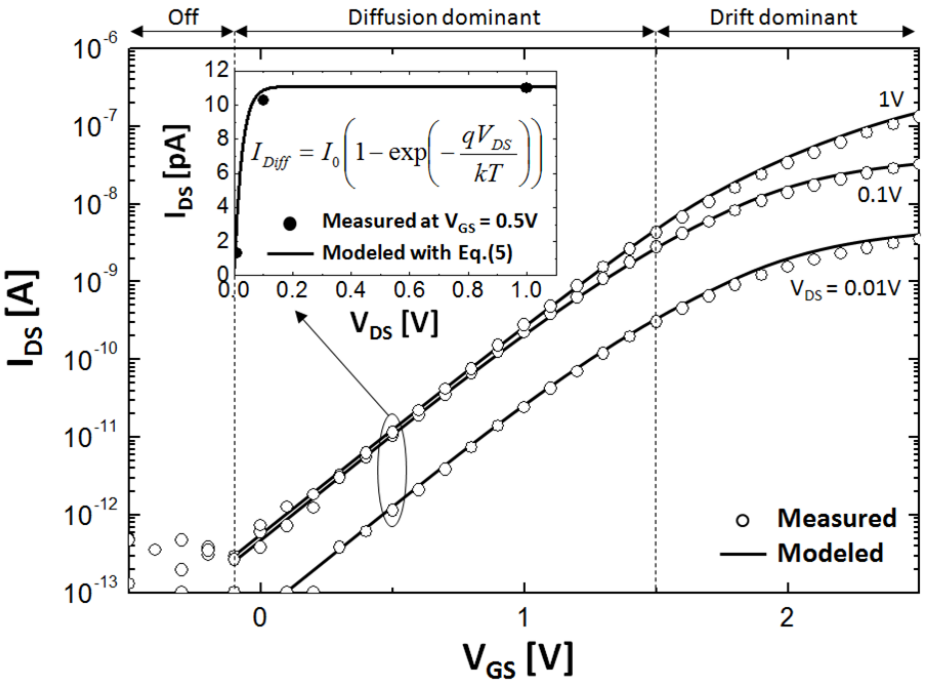


Fig. 2.6 Measured and modeled I_{DS} vs. V_{GS} at subthreshold region for a different V_{DS}. Inset: Measured and modeled I_{DS} vs. V_{DS} for $V_{GS} = 0.5V$. Here, the equation is simplified from Eq. (2.5) introducing the pre-constant I_0 which is around 10pA at V_{GS} = 0.5V.

2.2.3 Off Region Model

The off current can defined according to [**?**] at $V_{GS} = V_{FB}$,

$$I_{off} \approx \mu_0 \frac{kT}{q} \frac{W}{L'} Q_{fi} \left(1 - exp\left(-\frac{qV'_{DS}}{kT}\right)\right) \tag{2.9}$$

2.2.4 Unified Model

As seen in the previous sections 2.2.1 & 2.2.2, the current-voltage relation needs to be derived separately to describe the subthreshold and above-threshold characteristics. Here, we need separate expressions for the subthreshold and above-threshold regions, implying two different equation systems to describe total current (see Fig. 2.8). Moreover, in this case, threshold voltage (V_T) is not immediately apparent from the I-V plot and needs to be extracted from above-threshold region of the characteristic as a fitting parameter. However, the extracted value of V_T can be quite different depending on extraction method and the I-V data range chosen for the fit. In contrast, turn-on-voltage (V_{on}) is the gate voltage (V_{GS}) at which drain current (I_{DS}) starts increasing rapidly, thus it is easy to identify V_{on} on a semi-log plot of I_{DS} vs. V_{GS}.

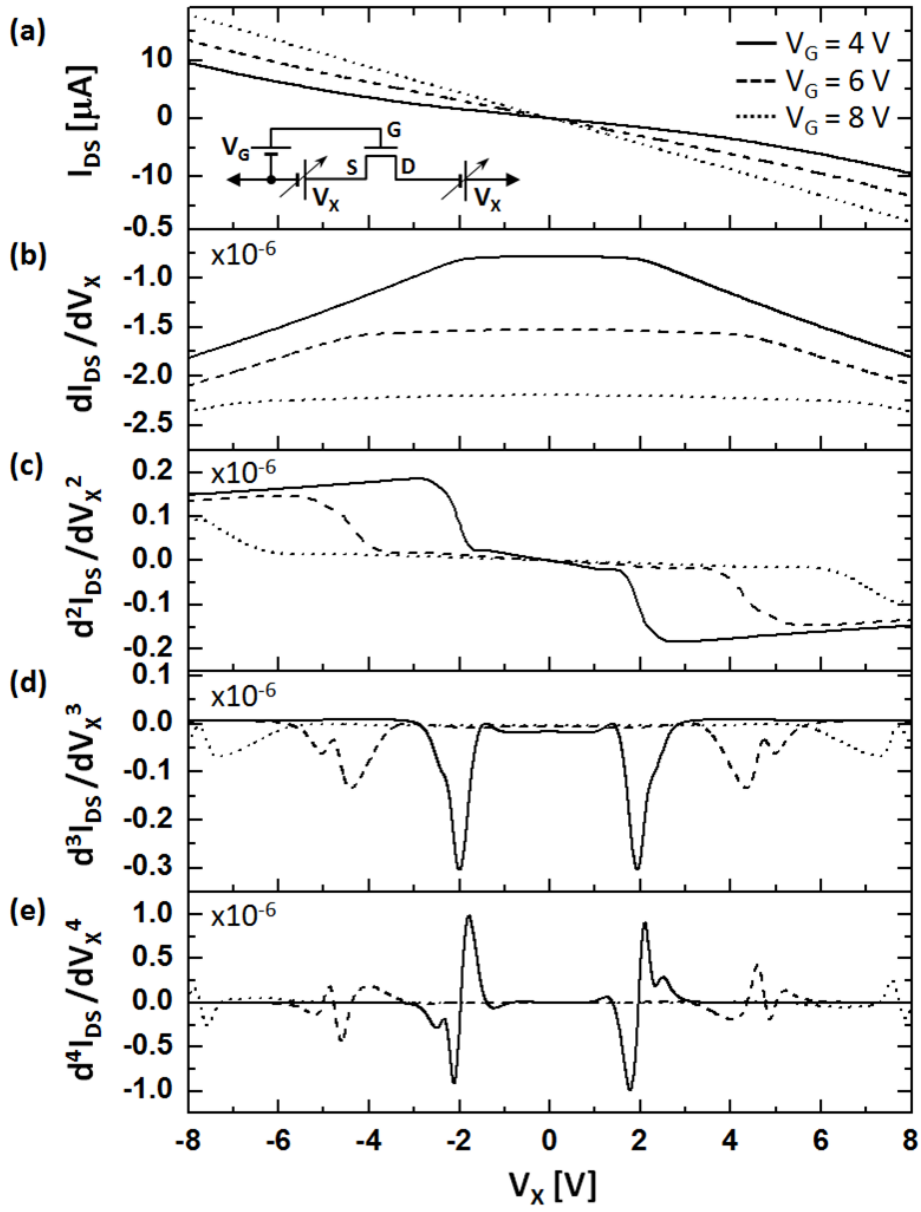


Fig. 2.7 (a) Calculated I_{DS} vs. V_X of the combined above- and sub-threshold model for different V_G (4, 6, 8V). (b) First, (c) second, (d) third, and (e) fourth derivatives of I_{DS} with respect to V_X. The inset of (a): test circuit configuration of the GST.

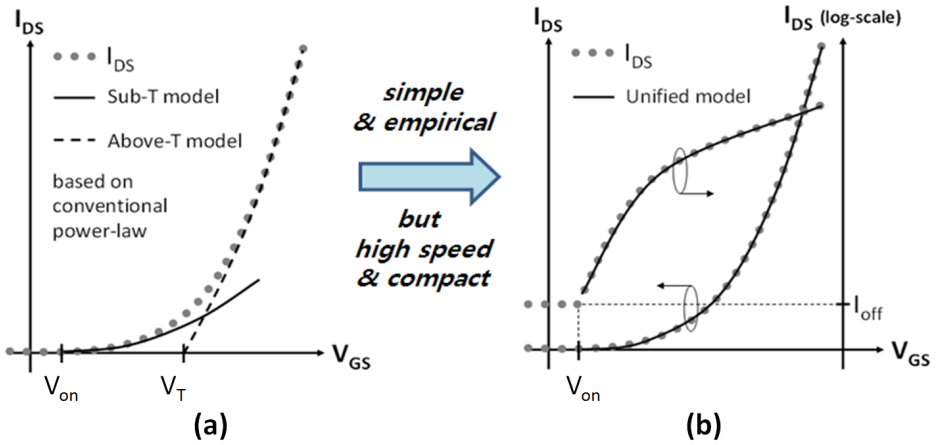


Fig. 2.8 (a) Schematic I_{DS} vs. V_{GS} curves (gray circles) with the conventional power-law models for subthreshold (Sub-T, solid line) and above-threshold (Above-T, dot line) characteristics. In this case, we need two models for these two different operational regions. Here, V_{on} and V_T are on-voltage and threshold voltage, respectively. (b) Schematic I_{DS} vs. V_{GS} curves (gray circles) with only one model: unified model which can cover subthreshold as well as above-threshold regions at the same time.

We can unify this to cover both subthreshold and above-threshold characteristics. The proposed unified model is a single expression with a reference voltage level V_{on} rather than V_T, providing good agreement with measured terminal characteristics over the entire range of $V_{GS} > V_{on}$ for the test TFTs with an amorphous InGaZnO (a-IGZO) channel, which is the same TFT used in the previous sections. The derived equation for this model is as follows,

$$I_{DS} = G_0 \frac{W}{L'} exp\left(\kappa (V_{GS} - V_{on})^{\alpha}\right) V'_{DS} + I_{off} \tag{2.10}$$

where $G_0 = \mu_0 (\varepsilon_S kTN_C)^{1/2}$, $\kappa = \zeta / 2kT$, and ζ & α are related to trap states. To extract the values of κ and α, we can rewrite Eq. (2.10) as,

$$U \equiv \frac{I'_{DS}/V'_{DS}}{\mathrm{d}(I'_{DS}/V'_{DS})/\mathrm{d}V_{GS}} = \frac{1}{\alpha\kappa}(V_{GS} - V_{on})^{1-\alpha} \tag{2.11}$$

Here, $I'_{DS} \equiv I_{DS} - I_{off}$. Therefore, $1-\alpha$ and $1/(\alpha\kappa)$ can be extracted from the plot of lnU vs. $ln(V_{GS} - V_{on})$ as the slope and the intercept, respectively (as illustrated in Fig. 2.9a). The extracted model parameters are summarized in Table 2.2.

Fig. 2.9b shows modelled results for different L (=25, 50, and 100μm), providing good agreements with the measured characteristics. Also, they exhibit small average errors < 5% over a wide range of V_{GS} from 5 to 20V. Interestingly, the proposed model using only one equation covers both the sub- and above-threshold regions at the same time. This is mainly

Table 2.2 Extracted Parameters for Unified Model at T=300K

Parameters	Value
G_0	$2.34 \times 10^{-5} ohm^{-1}$
κ	$-10.812 V^{-\alpha}$
α	-0.675

due to a combination of the exponential function and power-law. Additional advantage of this unified model is that it just needs a few model parameters to be implemented in model code description, e.g. Veriog-A, thus providing a higher-speed simulation.

2.3 Computer Interpretation of Device Model

After having established an accurate analytical model for the TFT, computer implementation for circuit simulation is not always easy. Several considerations including speed, convergence and even the way of translating different form of equations into computer language should be taken into consideration in this step.

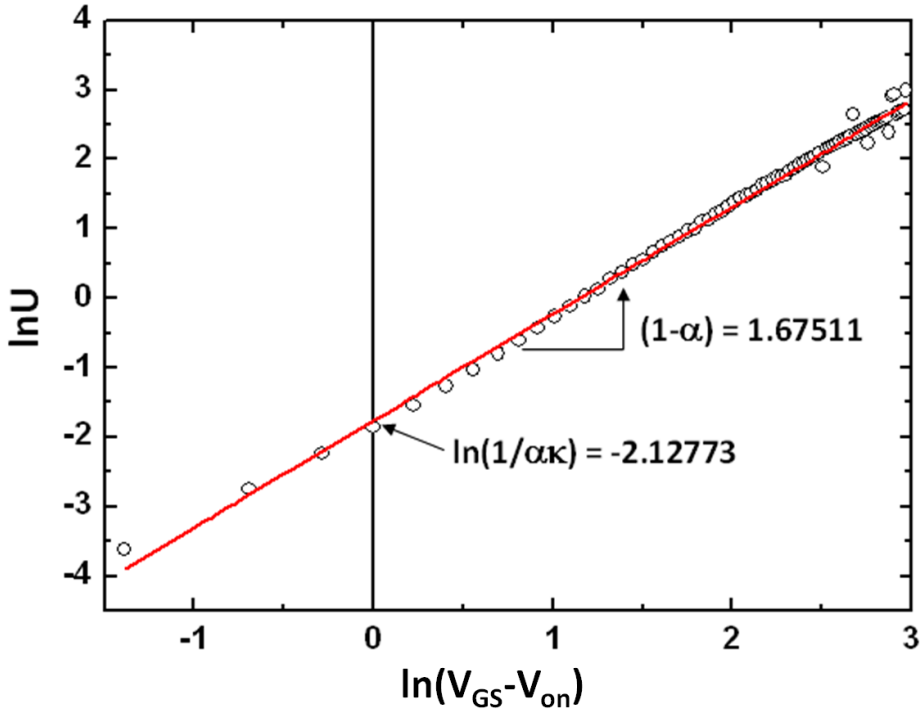
For a-Si TFTs, several SPICE models have been developed. Specifically the model developed by Rensselaer Polytechnic Institute, also known as the RPI model [**?**], has become a commercialized standard supported by many simulation platforms including SmartSpice, HSPICE and Spectre, etc. However, CAD of organic and metal-oxide TFTs is yet to become a standard due to the rapid and ongoing evolution in materials and device structures. In fact, and as mentioned previously, there is a quest for unifying the TFT model to meet simulation requirements of TFTs with ever changing structures and materials.

It is important to understand the benefits and drawbacks of SPICE and Verilog-A, while developing a device model to be used in further circuit simulation and system design.

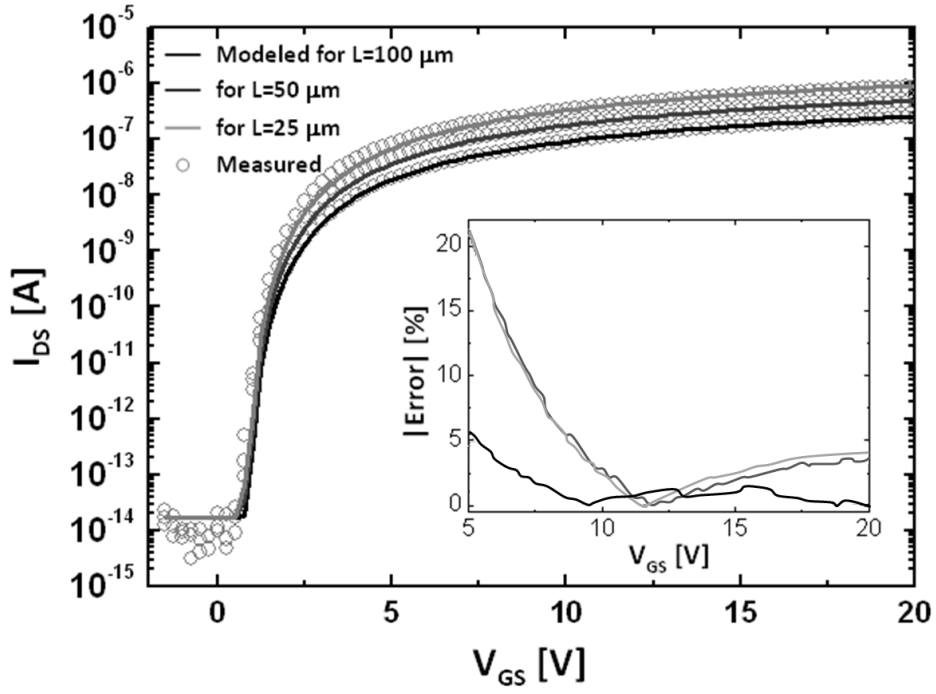
2.3.1 SPICE

SPICE is an open source analogue circuit simulation software firstly developed at the University of California, Berkeley [**?**]. The first two versions of this simulator was written in Fortran. SPICE2 included several elements widely used in circuit simulation at that time, including the diode, MOSFET, JFET and BJT, etc. In 1989, a version of the simulator SPICE3 was re-written in C. This version includes the well-known BSIM model [**?**].

Many commercial circuit simulators today are based on the aforementioned software including PSPICE, HSPICE, SmartSpice, Spectre, etc. The fast simulation speed, high accuracy and ease of use make the SPICE simulator extremely popular in the area of



(a) Plots of lnU vs. $ln(V_{GS} - V_{on})$. Here, linear fitting is applied over the entire range of $ln(V_{GS} - V_{on})$



(b) Modeled results for different L in comparison with the measured curves using a unified model, normalized error is illustrated in the inset.

Fig. 2.9 Parameter extraction for unified model & measured and modelled transfer curve with percentage error

circuit design. However, SPICE is written in a low level computer language (Fortran or C) and so are the models used in it. Therefore, researchers should not only have a good understanding of device physics but also need enough knowledge of the algorithms and limitations of the simulator. The procedure for developing a stand-alone SPICE model (not by combining existing elements) always takes time and resources. Due to the complexity of model development in SPICE, currently only well developed and widely used devices are having SPICE models.

It is worth noting that modern circuit simulators use a heavily modified original SPICE model but they separate as much as possible the simulation algorithm from the device model. For example, the Spectre simulator provides a Spectre Compiled Model Interface (CMI) for Spectre developers and others to use C code directly for device modelling.

2.3.2 Verilog

The Verilog Hardware Description Language (Verilog HDL) was designed in 1984 to meet the design demands of VLSI engineers working in the higher abstractive level to increase the number of transistors in simulating digital circuits. Subsequently adopted by Cadence Design Systems and Open Verilog International, VHDL has become an IEEE standard in 1995, i.e. IEEE Std 1364-1995 [**?**].

Since the original Verilog language did not support analogue systems, the extensive use of HDL languages led to a growing demand for high-level behavioural model for systems and components for use in analogue and mixed signal system design. Thus, Verilog-AMS standard was then developed by Accellera to include Verilog-A, a previously standalone behavioural language used for analogue modelling in Spectre, and extending both the digital part of the IEEE Std 1364 and the analogue part of Verilog-A [**?**].

In the early days of Verilog-A and Verilog-AMS, the behaviour model was limited in terms of accuracy for analogue devices. The language was first developed for design of systems and thus the behavioural language was at that time not intended for complex physical equations at the device level. Fig. 2.10 illustrates the mixed signal simulation environment in early days. In addition, device modelling often led to long execution times compared with SPICE models. Even so, the capability of behavioural modelling started to attract the attention of device modellers struggling with low level implementation.

In 2002, the open-source tool supporting automatic conversion [**?**] of Verilog-AMS models to C codes was introduced. Since then, several proposals have been made to use Verilog-AMS to efficiently develop compact device models [**? ?**] to integrate with SPICE like simulators. The report in 2010 [**?**] showed comparable performance of their Verilog-AMS device model against SPICE. The language has now become a major tool for device

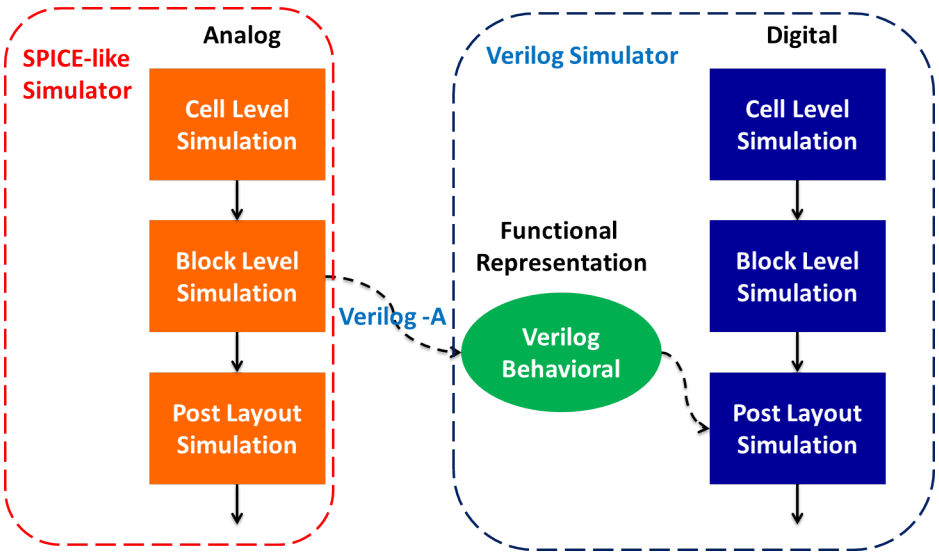


Fig. 2.10 Verilog-A behaviour model in early mixed signal simulation environment

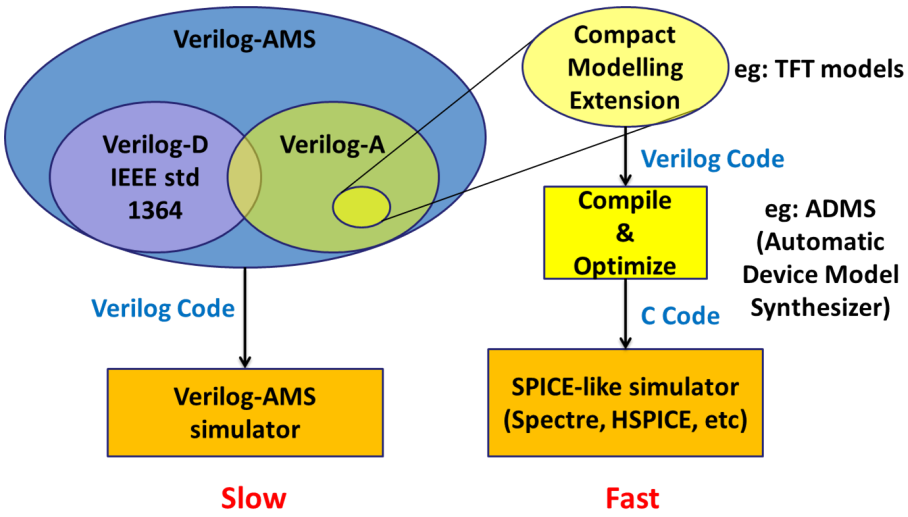


Fig. 2.11 Verilog-A(MS) extension for compact modelling with SPICE like simulator integration

Table 2.3 Comparison between different model languages

	SPICE	Spectre CMI	Verilog-AMS
Language	C/Fortran	C	Verilog
Language level	Low	Low	High
Easy to use	No	No	Yes
Efficiency & Speed	High	High	Low
Complexity	High	High	Low
Simulator information needed for developers	Simulation algorithm & limitations	Simulator limitation on equations	None
Users	SPICE developers	CAD engineers, Cadence programmers	End users

model developers. Fig. 2.11 illustrates the relation between different Verilog languages and the simulation flow in two types of simulators.

2.3.3 Short Summary of Comparison

Table 2.3 summarizes the comparison of different model languages. The SPICE model development based on a low level language is only used by model developers of components, which are not likely to change (due to heavy usage or technology maturity) in view of resource requirements. In the meantime, the Verilog approach is ideally suited to meet the modelling demands of ever-changing TFT or other device structures without requiring a mature physical understanding of the devices or underlying material system. The direct implementation of physical equations in Verilog-AMS will dramatically reduce the time between development of new devices and subsequent circuit simulation.

Despite all the benefits of Verilog-AMS, the model is still slower and less efficient than a well-developed SPICE model, due to the fact that the Verilog-AMS model should be converted to a lower level language form. The converted form although automatically optimized by the synthesizer (e.g. ADMS [**?**]) cannot be as efficient as a SPICE model because the latter is optimized directly in a lower level language. Therefore, it is recommended to use SPICE for circuit simulation whenever it could offer sufficient accuracy. On the other hand, Verilog-AMS is suited for devices that are new or under-development.

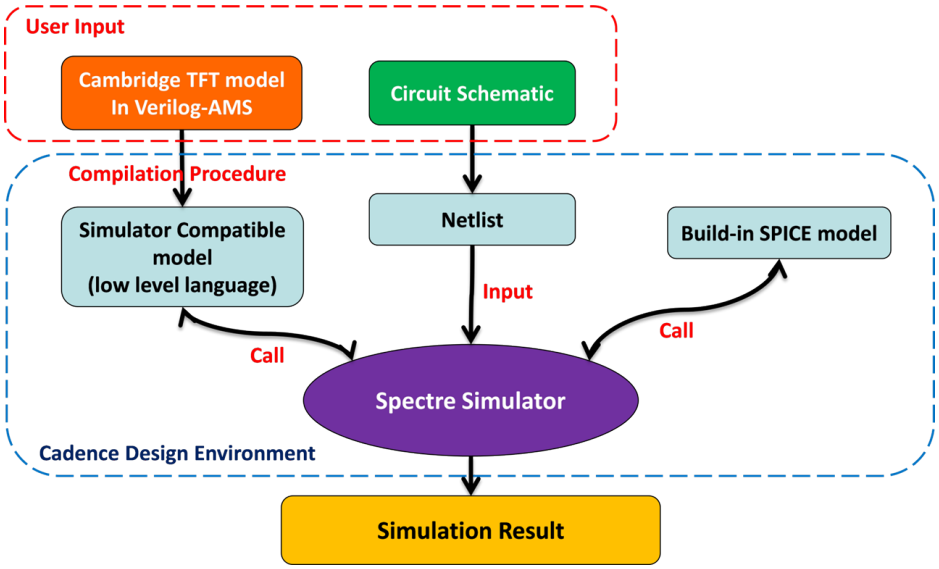


Fig. 2.12 Circuit design and simulation flow using CAMCAS model in Cadence Design Environment

2.4 CAMCAS Model in Simulation Environment

As discussed before, we implement the Cambridge's TFT compact model (i.e. CAMCAS model) directly into Verilog-A language for use in a Cadence Design Environment so as to focus on developing a more accurate model for circuit simulations. The simulation flow in the Cadence Design Environment is shown as Fig. 2.12.

The user extracts processing parameters based on the measurement results of their own devices and incorporates them into the CAMCAS Verilog-AMS model. In addition, the user can change the form of equations for better fitting to measurement results. Thus circuit designers can use the usual route of circuit design by simulating their TFT circuits before fabrication analogous to using the SPICE model in Cadence Spectre.

Fig. 2.13 shows an example of an IGZO TFT circuit simulated using the CAMCAS model in Cadence Spectre. The simulation results show a voltage gain of 12dB in both transient and AC simulation as shown in Fig. 2.14a and 2.14b, respectively.

2.5 Summary and Discussion

Physically-based compact models play an important role in computer-aided circuit design and simulation. This chapter reviews the major contributions in TFT analytical modelling and compares the pros and cons of SPICE and Verilog-AMS from the standpoint of device

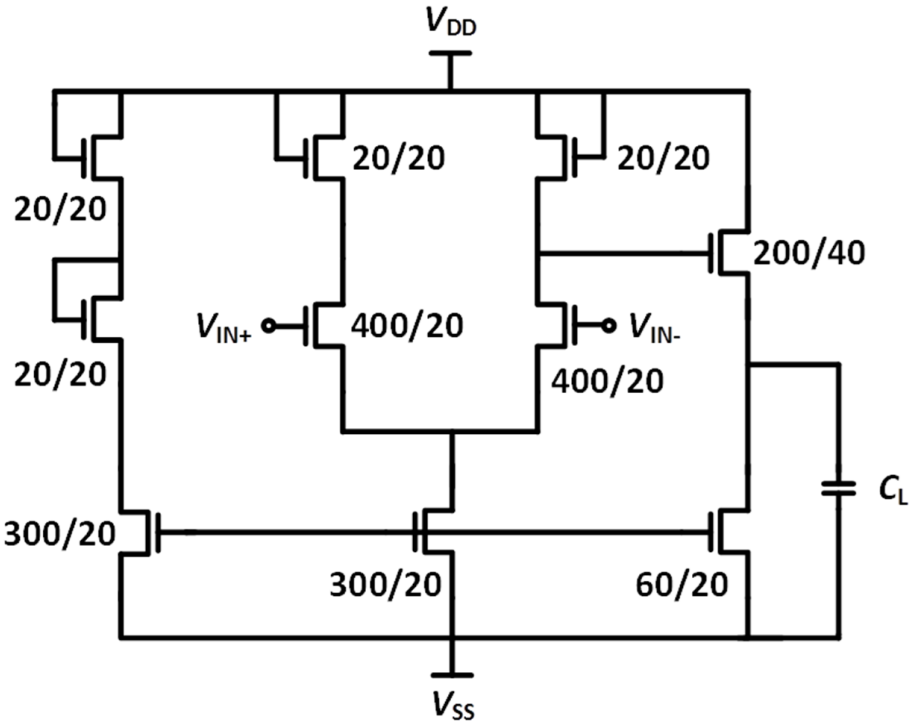
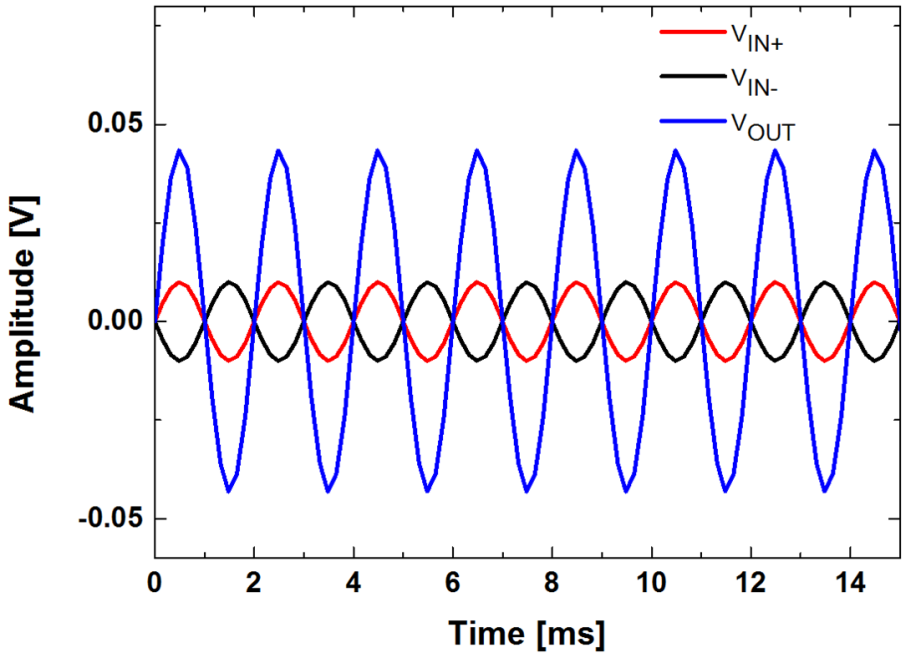


Fig. 2.13 A voltage amplifier used in simulation with CAMCAS model

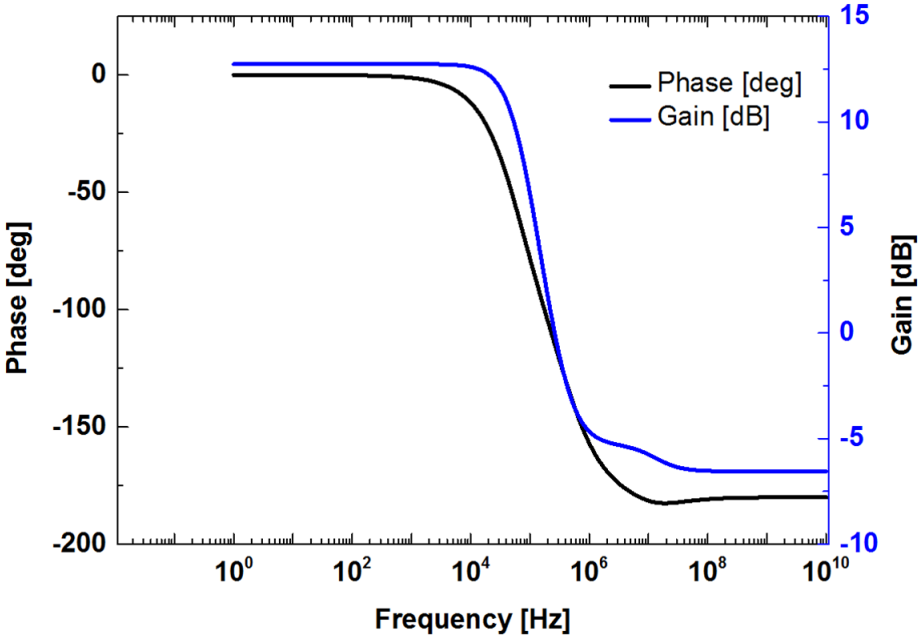
model development. Brief guidelines are provided to decide on choice of modelling language for implementation of models and to understand how models work within the simulator.

Regarding the device models, oxide TFTs are considered and two different approaches are reviewed. While considering physical and material properties of oxide semiconductors, both above- and subthreshold models have been presented. In particular, the above-threshold model uniquely addresses carrier transport properties in oxide TFTs, such as percolation conduction along with trap-limited conduction. Thus it is a fully-physical model. Also, using a harmonic average technique, diffusion and drift current components have been seamlessly combined to describe subthreshold current behaviour, providing good agreement with measurements. Using a different, more empirical-based approach, a unified model is discussed that covers both sub- and above-threshold regions with a single expression. This model provides higher speed circuit simulation since it has only a few number of parameters. The results presented here are essential for oxide circuit design and simulation, providing designers with a preference for fully physical but slower simulations on the one hand, and higher speed but less model complexity on the other.

The CAMCAS model described above is implemented in Verilog-AMS, and the validity of the approach is demonstrated by way of a voltage amplifier circuit simulation.



(a) Transient analysis for small signal amplitude at input and output



(b) AC analysis for gain and phase

Fig. 2.14 Simulation results of the voltage amplifier

Chapter 3

Small Signal Modelling

3.1 General Small Models

Small-signal model is used for linear approximation of many none linear electronic devices including diodes, MOSFET and BJT, etc. when the signal under processing is reasonably small compared with the DC bias of devices. The use of small-signal model significantly simplifies the design procedure of many analogue circuits, especially amplifiers. Different small-signal models exist for different electronic devices, for example MOSFET and BJT are having different small-signal models due to their different structure and working principles. However, researchers in the area of TFT circuit design are using the same small-signal model as MOSFET. In spite of the similarity of their structures, TFTs are having a much bigger contact resistance between different materials, more significant parasitic capacitance and a severe instability problem. Therefore, it is helpful to reevaluate the small-signal model specifically for TFTs.

3.1.1 Midband Small Signal Model

First, we review how a midband small signal model was developed. As linear systems are to be designed out of none linear devices, the straightforward solution is to use a small part of the none linear behaviour (I-V curves) to approximate a linear response (small signal model). Therefore, under the assumption that the signal is sufficiently small, the linear approximation would be equal to the derivative of the none linear device at the bias point. For a general 3 terminal device with terminal G, S and D (terminal names can be arbitrarily chosen, here

they are chosen in consistency with TFTs), The I-V formula can be written as:

$$\begin{cases} I_D = f_1(V_{GS}, V_{DS}) \\ I_G = f_2(V_{GS}, V_{DS}) \end{cases} \tag{3.1}$$

Here, V_{GS} and V_{DS} are the voltage drops between G-S terminals and D-S terminals, respectively. As V_{GD} can be calculated from $V_{GS} - V_{DS}$ and $I_S = -I_D - I_G$, Eq. (3.1) is enough to represent the I-V of an arbitrary 3 terminal device.

For small changes of V_{GS} and V_{DS}, the current differences would approximately follow the derivative of the I_D and I_G functions in Eq. (3.1).

$$\begin{cases} \mathrm{d}I_D = \dfrac{\partial f_1}{\partial V_{GS}}\mathrm{d}V_{GS} + \dfrac{\partial f_1}{\partial V_{DS}}\mathrm{d}V_{DS} \\ \mathrm{d}I_G = \dfrac{\partial f_2}{\partial V_{GS}}\mathrm{d}V_{GS} + \dfrac{\partial f_2}{\partial V_{DS}}\mathrm{d}V_{DS} \end{cases} \tag{3.2}$$

For sufficiently small signals and sufficiently good linearities at the bias point, the partial derivatives can be treated as a constant. The small signal relations should follow:

$$\begin{cases} i_d = g_{m1} v_{gs} + \dfrac{v_{ds}}{r_{o1}} \\ i_g = \dfrac{v_{gs}}{r_{o2}} + g_{m2} v_{ds} \end{cases} \tag{3.3}$$

where i and v in small cases represent the small change in current and voltage of the corresponding terminals, respectively. The coefficient of v_{ds} for i_d or v_{gs} for i_g can be represented as passive components (a resistor connection), while the coefficient of v_{gs} for i_d or v_{ds} for i_g can only be represented by active components, a voltage controlled current source (VCCS). Therefore, resistance is used to represent passive components (i.e. r_{o1} and r_{o2}) and transconductance is used to represent active components (i.e. g_{m1} and g_{m2}).

Now, from Eq. (3.3) we have the linear approximation of the device at a fixed bias point of V_{GS} and V_{DS} (Note that the coefficients in Eq. (3.3) can be a function of V_{GS} and V_{DS}, but not a function of v_{gs} and v_{ds} under the small signal assumption.) The corresponding small signal model of the equation can be drawn as Fig. 3.1. This is a general form of a hybrid-pi model which is consistent with both BJT and MOSFET. In the case of most transistors, V_{DS} does not affect I_G. Thus, $g_{m2} = 0$. And for the case of MOSFET, the gate resistance is huge and normally treated as open-circuit. Therefore, the corresponding components can be removed.

The analysis reviewed above is a general approach for all three terminal devices. Thus it should also be valid for TFTs at midband frequencies. However, as the parameters are derived

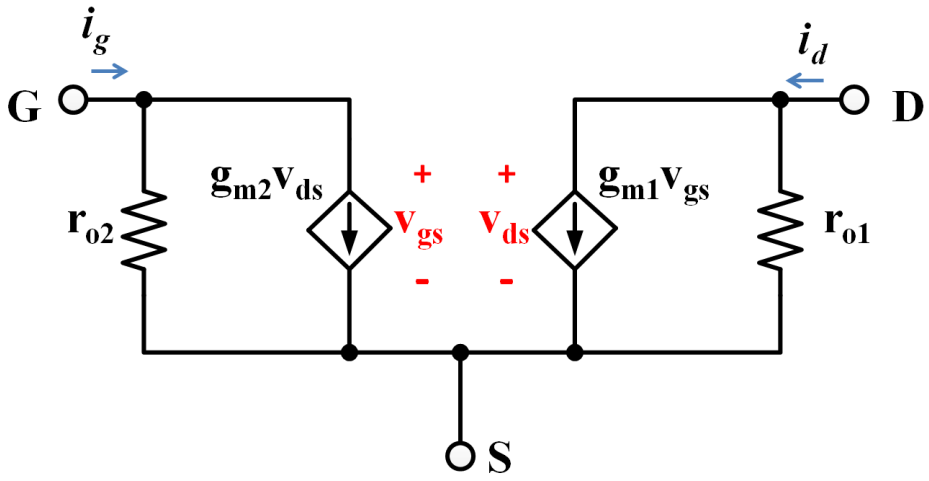


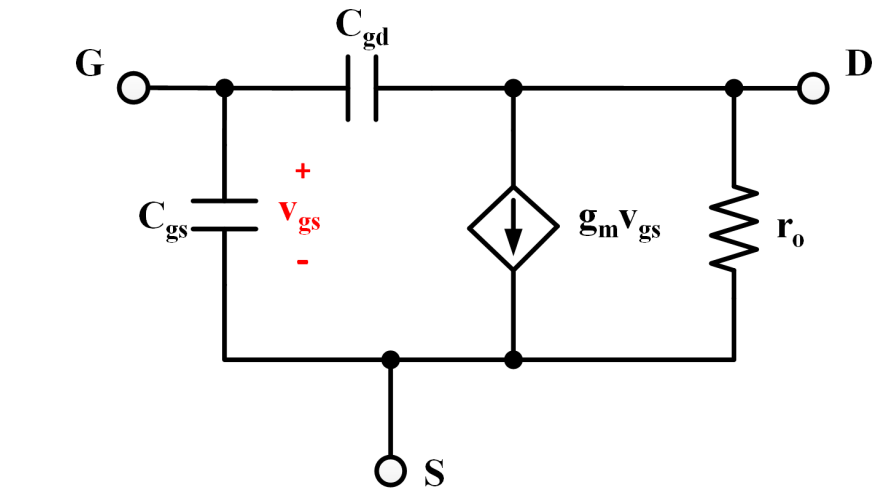
Fig. 3.1 Small signal model for a general 3 terminal device

from the derivative of I-V curves, a more physical representation of those parameters can be complicated and some of the parameters should be represented as separate components.

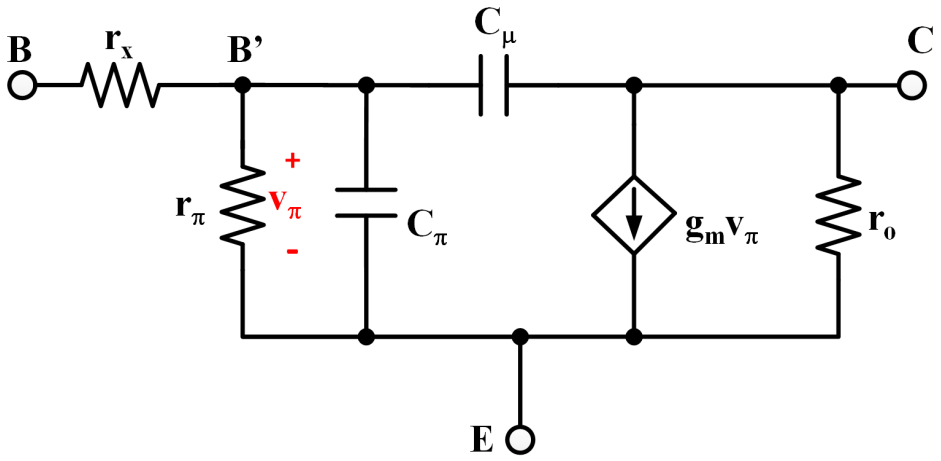
3.1.2 High-Frequency Small Signal Model

An accurate calculation of the circuit response at midband frequency is not enough for circuit designers as the bandwidth and phase margin should also be predicted when designing circuits. This is especially crucial for amplifiers and active filters to prevent self-oscillation. While midband small signal models can be developed through a general way from I-V curves, the high-frequency small signal model can only be developed by considering I-V, C-V and physical meanings of different components. This is why the high-frequency small signal models are very different for CMOS and BJT despite the similarities on their midband models.

The comparison of CMOS and BJT models is shown in Fig. 3.2 [**?**]. The CMOS high frequency model (Fig. 3.2a) is more consistent with the midband model that the parasitic capacitors are added to the midband model while keeping the original connections. In comparison, the BJT model (Fig. 3.2b) is less so as node B' is added between r_x and r_π (which are the same resistance in the midband model). The separation of r_x is due to the physical representation of a base spreading resistance which is the resistance of the connection to the base inside the device. The contribution of this resistor becomes more significant at high frequency because of the reduced impedance of the parasitic capacitors, namely C_μ and C_π.



(a) CMOS model



(b) BJT model

Fig. 3.2 High frequency small signal models for CMOS and BJT

The review of CMOS and BJT high-frequency small signal models suggests that physical structure should be considered while developing high-frequency models as the connections of parasitic capacitances may vary and affect the overall performance of the model. Therefore, it is imperative to evaluate the TFT structure to include physical resistance, capacitance and their connections correctly.

3.2 TFT Small Signal Model

As discussed in the introduction section, an accurate TFT small signal model needs to consider the physical representations and modelling not only for the sake of a simpler

expression of each component in the midband model but also for an accurate modelling in the high-frequency model. In this section, we will discuss the concerns at the stage of model developing and report the developed models.

3.2.1 Midband TFT Model

As discussed in section 3.1, the midband model can be developed using the general approach. Therefore, the small signal behaviour can be represented by a VCCS and an output resistor in parallel. The major concern of this approach is the expression of the two components, g_m and r_o. As the two components come from the derivative of $I_{DS}-V_{GS}$ and $I_{DS}-V_{DS}$ curves, the static characteristic of TFTs should be considered first before deriving the expressions of g_m and r_o.

The major concern here comes from the big contact resistance (R_C) [**? ? ? ? ? ?**] and the threshold voltage shift (V_T shift) [**? ? ? ? ? ?**] in TFTs which include TFTs from different material families such as amorphous silicon, organic and metal oxide semiconductors. Although TFTs are having a similar working principle with MOSFET, the contact resistance (R_C) is so dominant that even the static model should consider R_C as independent components. Most of the static models are developed based on a structure shown in Fig. 3.3 where the I-V characteristics are modelled for the internal transistor and the R_Cs (R_S and R_D here) are accounted for separately.

In this section, we will consider the effect of contact resistance and V_T shift in the midband TFT model.

The effect of contact resistance

As the overall I-V expression is complicated when considering R_S, R_D and the ideal TFT as a whole, it is more convenient to derive the small signal model of the ideal TFT and then consider the circuit as a linear network. Therefore, by using the I-V expression we can easily derive a small signal model shown in Fig. 3.4a. As reviewed in Chapter 2, the general I-V expression for a TFT can be written as:

$$I_{DS}=\frac{1}{\alpha_p+2}K\frac{W}{L'}(V_{GS'}-V_T)^{\alpha_p+2} \tag{3.4}$$

where $K=(\alpha_p+2)\mu_0^*(\frac{N_C}{N_C+N_{tc}kT_t})\frac{C_{ox}^{\alpha_p+1}}{Q_{ref}^{\alpha_p}}\beta_{sat}$. The transconductance g_{mi} in in Fig. 3.4a can then be calculated directly as:

$$g_{mi}=K\frac{W}{L'}(V_{GS'}-V_T)^{\alpha_p+1} \tag{3.5}$$

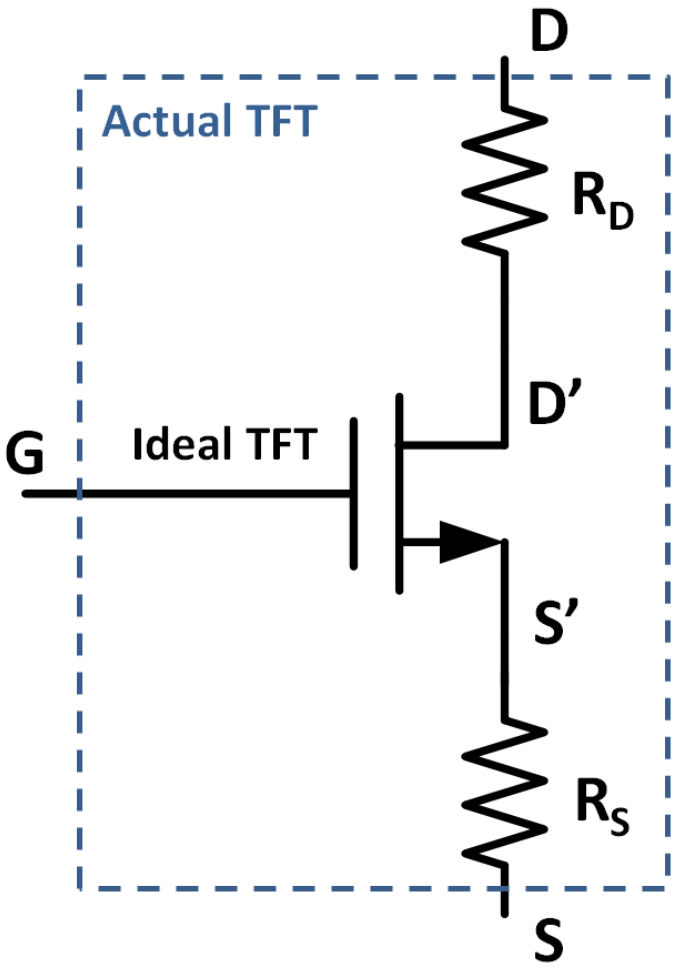


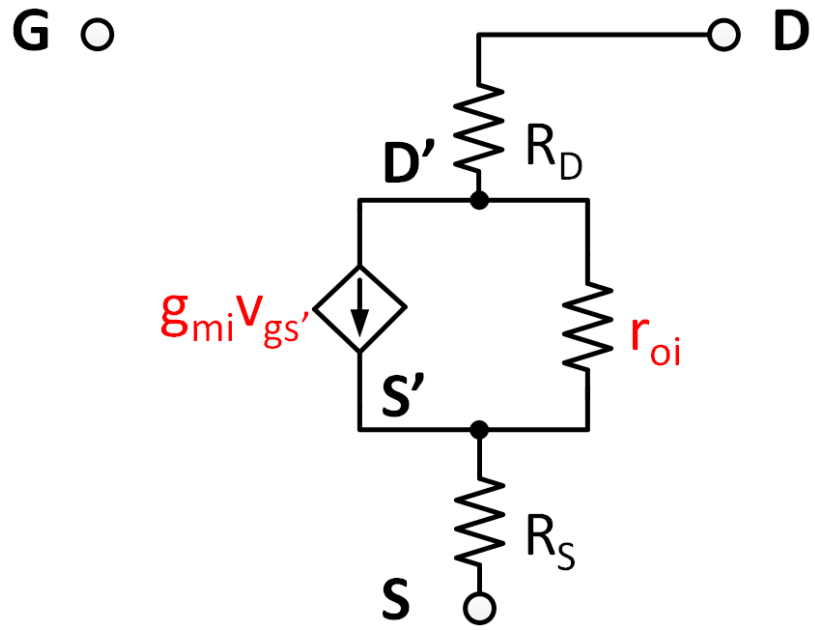
Fig. 3.3 The inner structure based on which static TFT models are developed

The r_{oi} in the figure, however, is harder to express in physical parameters. As the slope of the output characteristics are normally modeled using an empirical Early voltage (V_A)[1], r_{oi} is then calculated using:

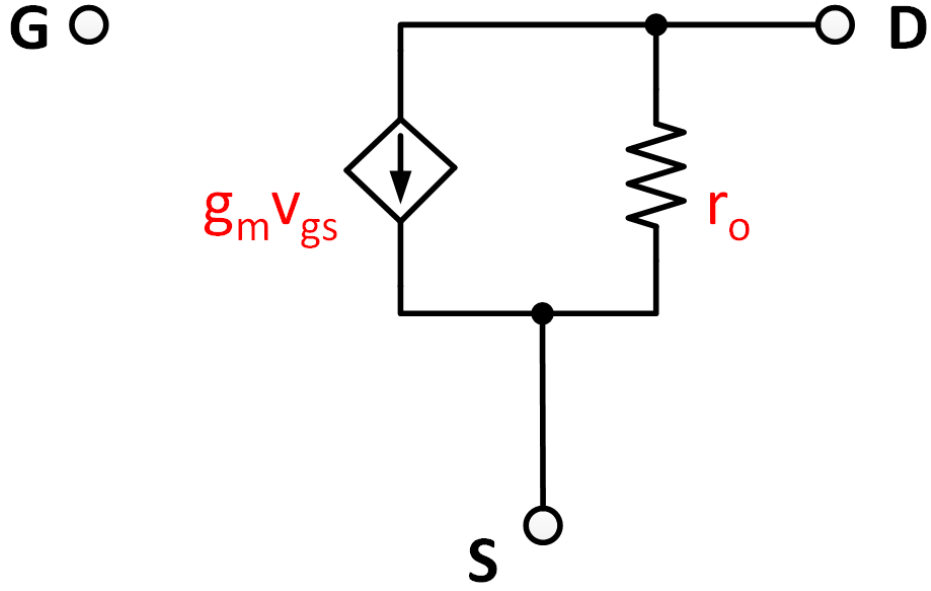
$$r_{oi} = \frac{V_A}{I_{DS}} \tag{3.6}$$

With the above equations, we can easily get an accurate midband small signal model for the TFT of concern and design suitable g_{mi} and r_{oi} by choosing W/L ratio, given that the TFT technology and processing parameters are already modeled with known R_S, R_D and V_A. However, it is not so convenient in terms of measurements as the results will be overall I-V curves directly. As the derivatives of the overall I-V curves can capture the overall g_m and r_o

[1]TFTs do not have the same short channel effect as CMOS does. But the output characteristics have similar trend of having an Early voltage. Thus, it is usually modeled by an empirical Early voltage.



(a) R_C as separate component



(b) Overall midband model

Fig. 3.4 Midband small signal models

in a equivalent midband model shown in Fig. 3.4b (the general approach). It is worth finding the relations between the two models shown in Fig. 3.4.

As the circuits are only consists of linear components, in this case only VCCS and resistors, the circuit in Fig. 3.4a should be equivalent to the one in Fig. 3.4b according to

Thévenin's theorem [**? ?**]. From Fig. 3.4a, we have:

$$\begin{cases} i_d = \dfrac{v_{s's}}{R_S} \\ i_d = g_{mi}(v_{gs} - v_{s's}) + \dfrac{v_{ds} - i_d R_D - v_{s's}}{r_{oi}} \end{cases} \tag{3.7}$$

Substituting $v_{s's}$ and considering [2] $R_S = R_D = R_C$, we get:

$$i_d = (\frac{g_{mi} r_{oi}}{g_{mi} r_{oi} R_C + 2R_C + r_{oi}}) v_{gs} + (\frac{1}{g_{mi} r_{oi} R_C + 2R_C + r_{oi}}) v_{ds} \tag{3.8}$$

Compared with Fig. 3.4b where we have:

$$i_d = g_m v_{gs} + \frac{v_{ds}}{r_o} \tag{3.9}$$

As both models should capture the same derivatives of the overall I-V curves (i.e. g_m and r_o), the relations should follow:

$$\begin{cases} g_m = \dfrac{g_{mi} r_{oi}}{g_{mi} r_{oi} R_C + 2R_C + r_{oi}} \\ r_o = g_{mi} r_{oi} R_C + 2R_C + r_{oi} \end{cases} \tag{3.10}$$

Here, we can derive the overall g_m and r_o out of the theoretical prediction of our transistor models. While designing real circuit applications, this will be the equations to use to estimate the circuit behavior. By solving Eq. (3.10), we can also get the values of internal components from measurement results:

$$\begin{cases} g_{mi} = \dfrac{g_m r_o}{r_o - g_m r_o R_C - 2R_C} \\ r_{oi} = r_o - g_m r_o R_C - 2R_C \end{cases} \tag{3.11}$$

This equation is very useful when the values of internal components are to be extracted out of measurement results. It also provides a convenient way of checking the validity of the model, which will be discussed later.

Eq. (3.10) and Eq. (3.11) not only show the relation between the static model parameters and the overall parameters from measurements but also reveal some insights of the parameters:

[2] As the semiconductor layer and source/drain contacts are made of the same material and have identical geometries and similar properties, the contact resistances are considered to be equal at both sides for convenience.

1. The intrinsic gain $g_m r_o$ of both the overall performance and the ideal internal TFT are the same. As the overall g_m is reduced due to the contact resistance (in comparison with g_{mi}), the r_o increases at the same rate making $g_m r_o = g_{mi} r_{oi}$. This also means that the contact properties of the semiconductor layer and the electrodes do not affect the intrinsic gain of the overall transistor. The measurement of $g_m r_o$ directly shows the maximum achievable single-stage gain of the semiconductor technology.

2. The term $g_{mi} R_C$ can be used to evaluate how different the measurement results will be from the ideal TFT in the model. As $g_{mi} r_{oi} R_C$ cannot be dominant over r_{oi}, otherwise the overall $g_m \approx \frac{1}{R_C}$ (which is impractical as there's no dependence on bias), and $R_C << r_{oi}$, the value of $g_{mi} R_C$ should be around 0 1 (might be a bit higher than 1 but should be around the order of magnitude).

The effect of V_T shift

Another property that might affect the midband model is the V_T shift under bias condition. As the implementation of TFTs in AMOLED display proves that bias-induced V_T shift must be compensated especially when the analogue properties are to be used (i.e. the output current needs to be actually controlled), the TFT small signal model should capture the behaviour to help design and evaluate TFT analogue circuits.

The major concern of V_T shift is that it would change the bias condition in effect, as in the static models, the V_T terms always appear in $V_{GS} - V_T$. Therefore, considering V_T shift, the expression of Eq. (3.5) can be rewritten as:

$$\begin{aligned} g_{mi} &= K\frac{W}{L'}\left(V_{GS'} - V_T - \Delta V_T\right)^{\alpha_p+1} \\ &= K\frac{W}{L'}(V_{GS'} - V_T)^{\alpha_p+1}\left(1 - \frac{\Delta V_T}{V_{GS'} - V_T}\right) \\ &= K\frac{W}{L'}(V_{GS'} - V_T)^{\alpha_p+1} - K\frac{W}{L'}(\alpha_p+1)(V_{GS'} - V_T)^{\alpha_p}\Delta V_T + O\left(\frac{\Delta V_T}{V_{GS'} - V_T}\right) \end{aligned} \tag{3.12}$$

Typically, $\Delta V_T << V_{GS'} - V_T$, as the experiments show that the V_T shift does not turn the transistor off (i.e. $\Delta V_T \sim V_{GS'} - V_T$) at least not within a reasonable time period. Hence, the higher order terms can be omitted in the above Taylor expansion. The first order approximation of $g_m i$ can then be written as follows:

$$g_{mi} \approx g_{mi0} - K'\Delta V_T \tag{3.13}$$

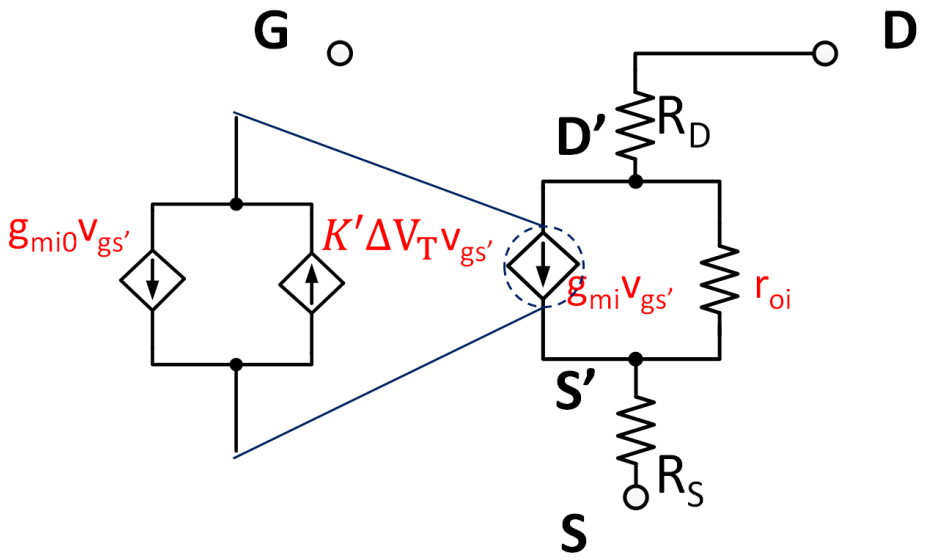


Fig. 3.5 Midband TFT model considering V_T shift

where $g_{mi0} = K\frac{W}{L'}(V_{GS'} - V_T)^{\alpha_p+1}$ is the initial value where there's no V_T shift, and $K' = K\frac{W}{L'}(\alpha_p+1)(V_{GS'} - V_T)^{\alpha_p}$ is the coefficient of the g_{mi} change per ΔV_T change. Here, as α_p is a constant value close to zero, K' can normally be treated as a constant coefficient.

This means that the V_T shift effect can be represented by a separate component. The corresponding modification of small-signal model is shown in Fig. 3.5.

3.2.2 High-Frequency TFT Model

Device structure and physical meanings of all components need to be considered in high-frequency small signal model, especially when capacitances come into the picture, as discussed in section 3.1 of the BJT model. The connection of contact resistances in TFTs plays a similar role as the base spread resistance of BJT which is connected in series with a parasitic capacitance. Here, as illustrated in Fig. 3.6 the contact resistance at source side (R_S) separates the overlap capacitance (C_{OVS}) and channel capacitance(C_{ch}). Hence, R_S might not be negligible nor included in overall components (i.e. g_m and r_o) especially at high frequencies. Combining the analysis of the midband model, the high-frequency small signal model for TFT can be drawn as Fig. 3.7a. In comparison, the CMOS model adapted to TFT parameters are shown in Fig. 3.7b. Here, C_{OVS} and C_{ch} are considered to be the same capacitor between source and gate terminals and the contact resistances are included in the overall g_m and r_o.

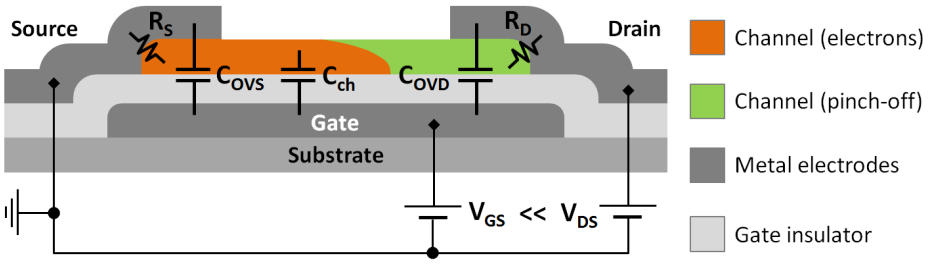
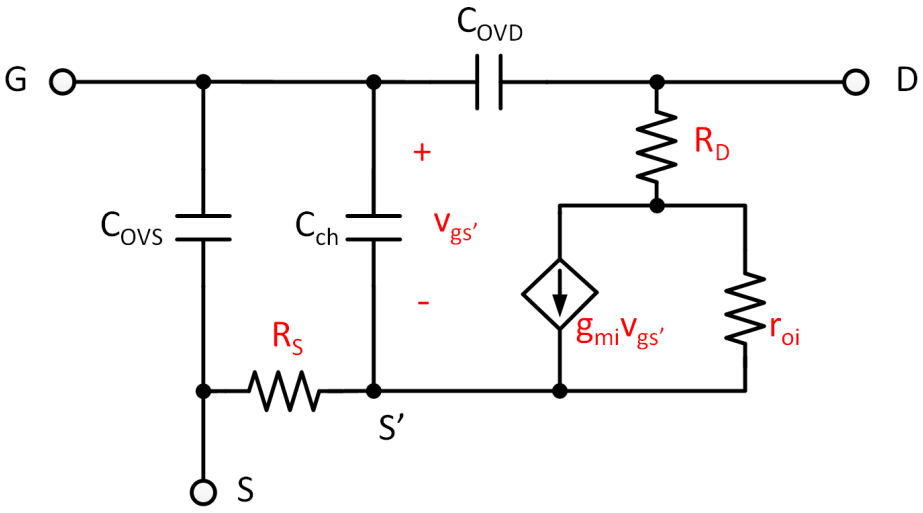
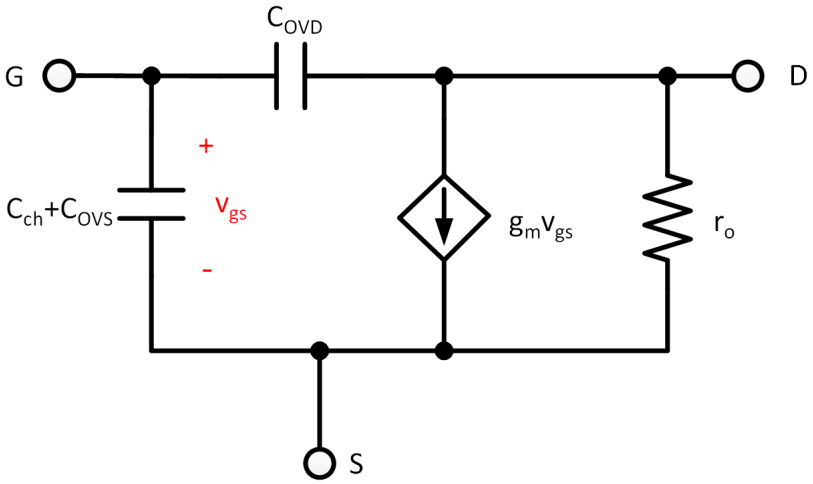


Fig. 3.6 Bottom-gate TFT structure considering passive components of the small signal equivalent circuit. C_{OVS} and C_{OVD} are the overlap capacitance at source and drain side; C_{ch} is the channel capacitance; R_S and R_D are the contact resistances at source and drain side.



(a) TFT model



(b) CMOS model adapted to TFTs

Fig. 3.7 High frequency small signal models

In order to evaluate the difference between the developed model and the CMOS model, we compare the expressions of the short circuit current gain (A_i) and the cutoff frequency of the two different circuits.

For CMOS model, A_i can be calculated as:

$$A_i = \frac{sC_{OVD} - g_m}{s(C_{OVD} + C_{OVS} + C_{ch})} \tag{3.14}$$

which contains one pole (at 0) and one zero (at g_m/C_{OVD}). Assuming the zero is far from the point of cutoff frequency. The unit-gain cutoff frequency can be calculated as:

$$f_T = \frac{g_m}{2\pi(C_{OVD} + C_{OVS} + C_{ch})} = \frac{g_m}{2\pi C_{tot}} \tag{3.15}$$

where C_{tot} is the sum of all capacitances of the TFT.

In contrast, the current gain calculated for the TFT small signal model seen in Fig. 3.7a is

$$A_i = \frac{-g_{mi}r_{oi} + ((2R_C + r_{oi} + g_{mi}R_C r_{oi})C_{OVD} + C_{ch}R_C)\,s + C_{OVD}C_{ch}R_C(R_C + r_{oi})s^2}{s\,(g_{mi}C_{OV}R_C r_{oi} + (2R_C + r_{oi})(C_{OV} + C_{ch}) + C_{OV}(R_C + r_{oi})R_C C_{ch}s)} \tag{3.16}$$

where $C_{OV} = C_{OVS} + C_{OVD}$ is the total overlap capacitance. The equation shows two zeros and two poles for this model. Assuming the poles and zeros are far from the cutoff point (for linear assumption at the point in Bode plot), the cutoff frequency expression is derived as:

$$f_T = \frac{g_{mi}r_{oi}}{2\pi\,(g_{mi}C_{OV}R_C r_{oi} + (2R_C + r_{oi})(C_{OV} + C_{ch}))} = \frac{g_m}{2\pi(C_{tot} - g_m R_C C_{ch})} \tag{3.17}$$

The simplification of the above equation shows that the major difference between Figs. 3.7a and 3.7b comes from the term $g_m R_C C_{ch}$. As g_m is a term already contains the R_C, it is preferable to consider this term as a function of independent variables. Thus, by substituting the g_m term, the expression of $g_m R_C$ is:

$$g_m R_C = \frac{g_{mi}r_{oi}R_C}{g_{mi}r_{oi}R_C + 2R_C + r_{oi}} \tag{3.18}$$

As g_{mi}, r_{oi} and R_C are independent values depending on semiconductor and interface properties with positive values, the whole term should be smaller than one. This indicates that the fraction C_{ch} is of the total capacitance plays an important role in determining whether the two models become identical. In the case when C_{OV} is dominant over C_{ch} or when the value of R_C is very small or close to zero, the $g_m R_C C_{ch}$ term can then be omitted and thus Eq. (3.17) becomes the same as Eq. (3.15). The CMOS model can be used despite the connection of $R_C s$ as in these cases the two high frequency models are equivalent.

In the case when the value of C_{ch} is at least of the same order of magnitude as C_{OV} or higher, the $g_m R_C C_{ch}$ term can reduce around 50% of the total capacitance (for the case when $g_{mi} R_C \approx 1$) making the two models very different in terms of modelling of the cutoff frequency. This also indicates that the CMOS model can be inaccurate especially when the contact resistance and overlap capacitance are big and small, respectively. As the contact resistance is known to be big in TFTs (from a few $k\Omega$ to several $100k\Omega$) and the reduction of overlap capacitance is preferable at the processing side for the sake of making faster TFTs, the inaccuracy of CMOS model might exist in most TFTs and may become more significant as processing technique becoming mature (e.g. for self-aligned TFTs the overlap capacitance is close to zero).

The other point to notice is that the assumptions used to derive Eq. (3.17) is supported by calculating the actual values of zeros and poles of the transfer function. As the extra zeros and poles are at way higher frequency compared with the cutoff frequency, they are not of concern as the transistor is dominated by capacitor effects and is not working properly at the frequency range.

3.3 Model Validation

From the theoretical analysis of small signal modelling, we know that the TFT small signal model can be very different from CMOS model when the contact resistance and overlap capacitance are big and small, respectively. In this section, we will evaluate the amount of difference by measurement of IGZO TFTs' cutoff frequency and the dominating s-parameters.

3.3.1 Measurement Setup

In order to evaluate the small signal model, we need to measure the current gain of the TFT and compare the cutoff frequency to see the model difference quantitatively. The common way of measuring the cutoff frequency of a transistor is to use a network analyser to measure the s-parameters and convert them to h-parameters. The calculated h_{21} directly reflect the short-circuit current gain of the device. Here, we use Keysight E5061B network analyser (ENA) calibrated by CS-11 calibration substrate provided by GGB Industries, Inc. The standard measurement setup is shown in Fig. 3.8. The bias-T provides DC bias to the TFT under test and separates the small signal input and output from the DC circuitry. The TFT is then connected to the ENA ports for s-parameter measurement.

The main reason of choosing the analyser is that it can provide low-frequency measurement down to 5Hz. In contrast, most of the network analysers on the market are targeted

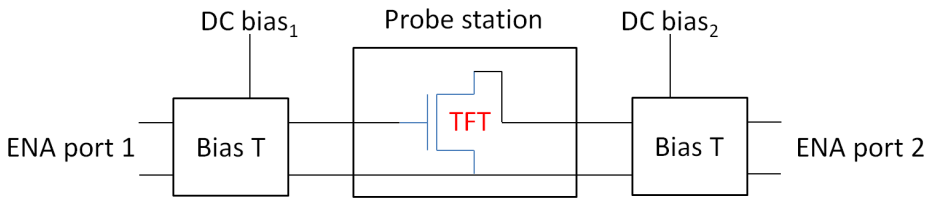


Fig. 3.8 Measurement setup for f_T and s-parameters

above 100kHz range, which is already a range close to TFT's cutoff. In the next section, we will see that even with the network analyzer low-frequency measurement is still hard, as the TFTs are more resistive at low frequencies.

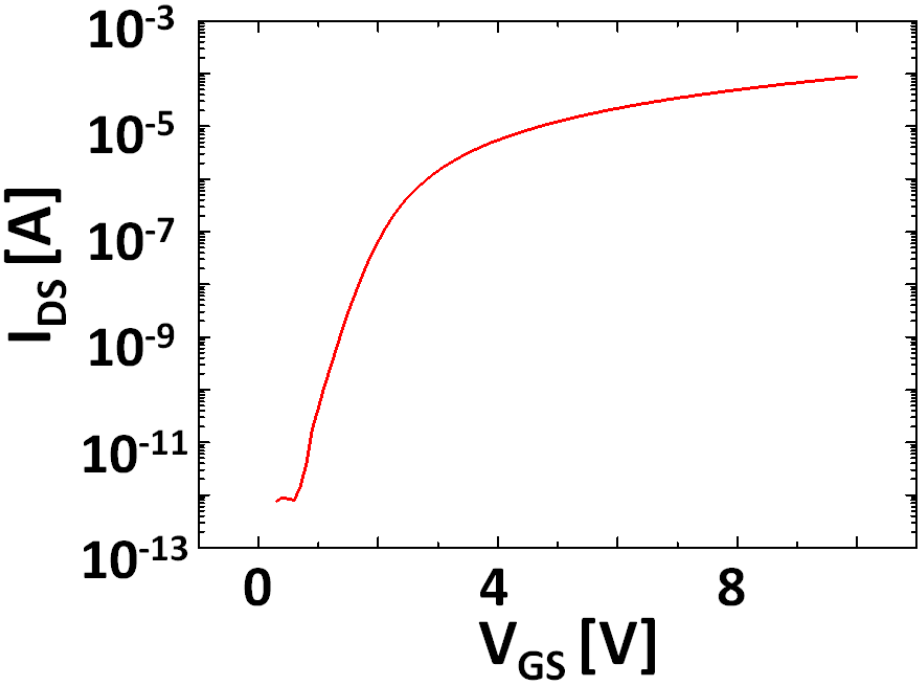
The ENA in use can only provide DC bias at port 1. Therefore, the bias-T at port 1 is already included inside the ENA. We still need to find a bias-T for port 2. As low frequency is important for our measurement, we choose Picosecond 5546 bias-T for this purpose. The low 3dB frequency is 3.5kHz, the lowest we managed to find on the market. We choose CS-11 calibration substrate and model 10 high-frequency probe (from DC to 6GHz) from GGB Industries, Inc. for the purpose of calibration, as the parasitics on the wires and the probes, etc. should be calibrated out before s-parameter measurement.

The DC bias conditions are chosen to be $V_{GS} = 8V$ $V_{DS} = 15V$ to make sure the TFT is working in the saturation region. It is to be noted that from the output characteristic (Fig. 3.9) the TFT saturates later than $V_{GS} - V_T$, which is the saturating point for CMOS. This is explained as the voltage drop on the contact resistance effectively reduced the $V_{D'S'}$ on the internal TFT (Fig. 3.3). The device under test has following physical and geometrical parameters: $t_s = 50nm$, $V_T = 1.6V$, $C_{ox} = 30nF/cm^2$, $\mu_0^* = 8.6cm^2/V \cdot s$. The device with W/L ratio of $100\mu m/10\mu m$ is used for model validation and $50\mu m/10\mu m$ is used for stress measurement.

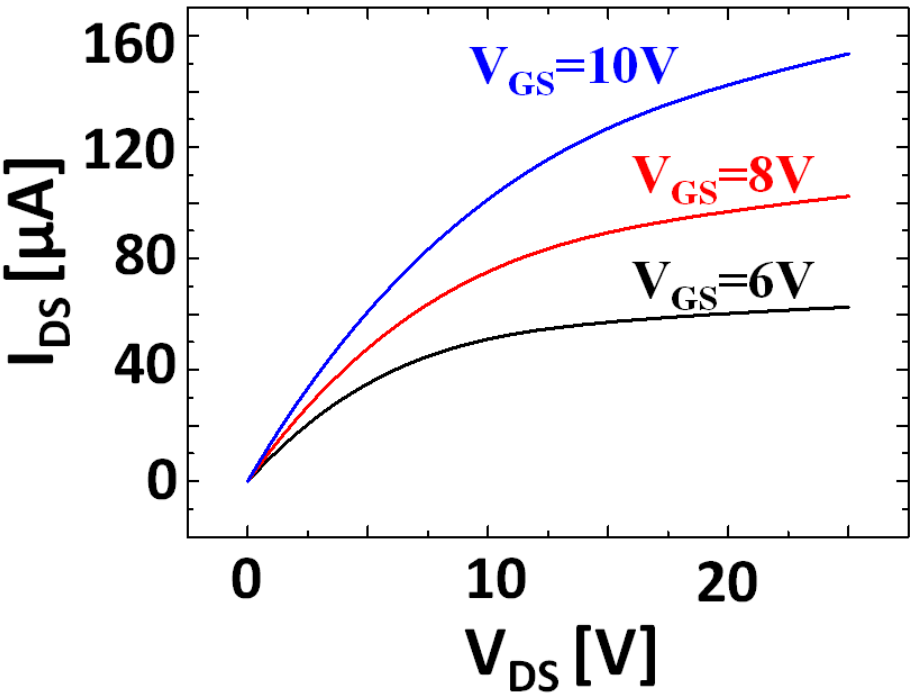
3.3.2 s-parameters and f_T Measurement

As f_T is calculated through s-parameter measurements, it is essential to understand how it is calculated and evaluate the measurement procedure as TFTs might have specific properties which may make the measurement very different from standard CMOS.

The most significant difference for TFTs is that the devices are very resistive. As TFTs are normally biased with a few volts to 20V level and the output current is normally around a few or a few tens μA, the corresponding resistances are around $100k\Omega$ or even a few $M\Omega$ level. Resistance at this level is huge particularly in s-parameter measurement as s-parameters are usually normalised with a characteristic resistance of 50Ω or 75Ω. For single port measurement such as S_{11} and S_{22}, the relation between corresponding impedance(Z_L)



(a) Transfer characteristic



(b) Output characteristic

Fig. 3.9 I-V characteristic of the TFT under test

and $S_{xx}(S_{11}/S_{22})$ is:

$$S_{xx} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{3.19}$$

where $Z_0 = 50\Omega$ is the characteristic resistance. Here, as Z_L is much larger than Z_0, the $S_{11} or S_{22}$ values should be very close to 1 (or very close to 0dB). This fact only changes at higher frequencies when the impedance of the capacitors drops significantly. As discussed before, the frequency range of concern is the range below the cutoff frequency. The impedance of the capacitor at the frequency range should be comparable with the internal components, otherwise, the circuit performance will be dominated by the capacitors. Therefore, the assumption will be valid in the whole frequency range of concern.

S_{11} and S_{22} are also called reflection coefficient. It expresses the ratio of the reflected power to the incident power of an electromagnetic wave. As the reflection coefficient is close to 1, the transmission coefficients (S_{12} and S_{21}) should be small as most of the power are reflected rather than transmitted. The experiment shows these two parameters are very close to 0.

Now as we know the estimated value of the 4 parameters, we need to evaluate the equation of h_{21} (Eq. (3.20)).

$$h_{21} = -\frac{2S_{21}}{(1-S_{11})(1+S_{22}) + S_{12}S_{21}} \tag{3.20}$$

Here, the major complexity comes from the denominator. Therefore, the next question is whether the denominator is dominated by some part of the terms or not. It is pretty hard to tell which part of the denominator is more dominant intuitively, as both terms of $(1-S_{11})(1+S_{22})$ and $S_{12}S_{21}$ are close to 0. One could estimate from the assumption that $1-S_{11}$ has a similar order of magnitude compared with S_{12} or S_{21} to conclude that $(1-S_{11})(1+S_{22})$ term dominates over $S_{12}S_{21}$. A further check from experiment based on the IGZO TFTs shows that the former term is 4 orders bigger than the latter term as shown in Fig. 3.10. Therefore, the $S_{12}S_{21}$ term can be omitted when calculating the current gain.

Further, as S_{22} is very close to 1, the product of $1-S_{11}$ and $1+S_{22}$ is much more sensitive to the change of S_{11} than S_{22}. The final approximation of the equation is then as follows:

$$A_i = |h_{21}| \approx |\frac{S_{21}}{S_{11}-1}| \tag{3.21}$$

Note that the approximation above is very accurate as the dominance of parameters is so significant. A comparison based on experiment result is shown in Fig. 3.11. The estimation gives 0.04% error in calculating the current gain of TFT within the frequency of concern. Therefore, Eq. (3.21) can be used in the measurement of current-gain or f_T of TFTs without the measurements of S_{12} and S_{22}.

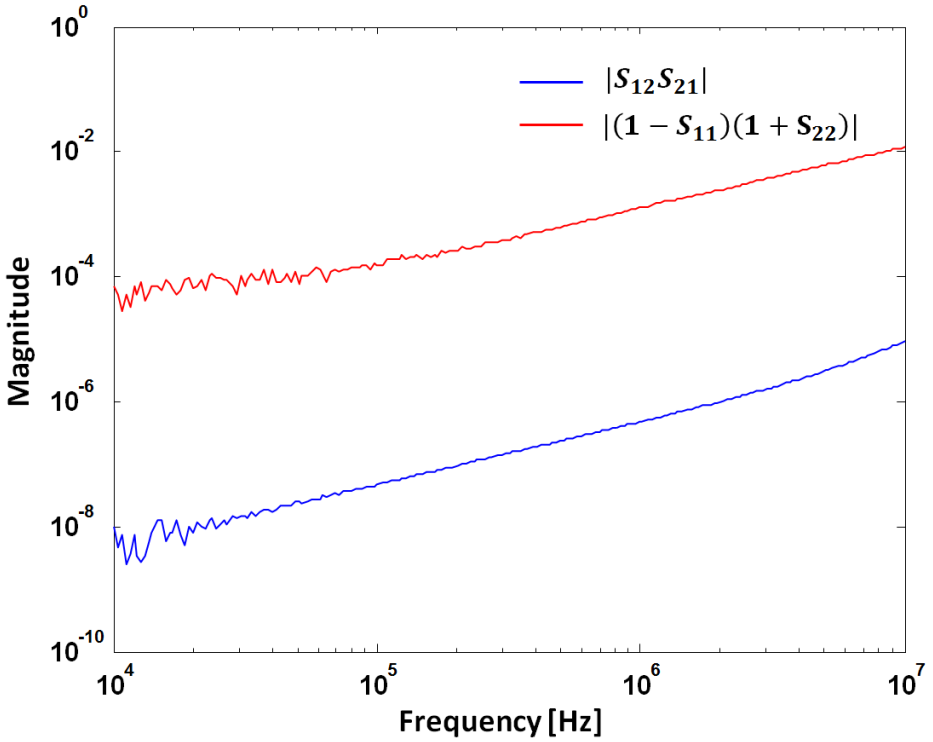
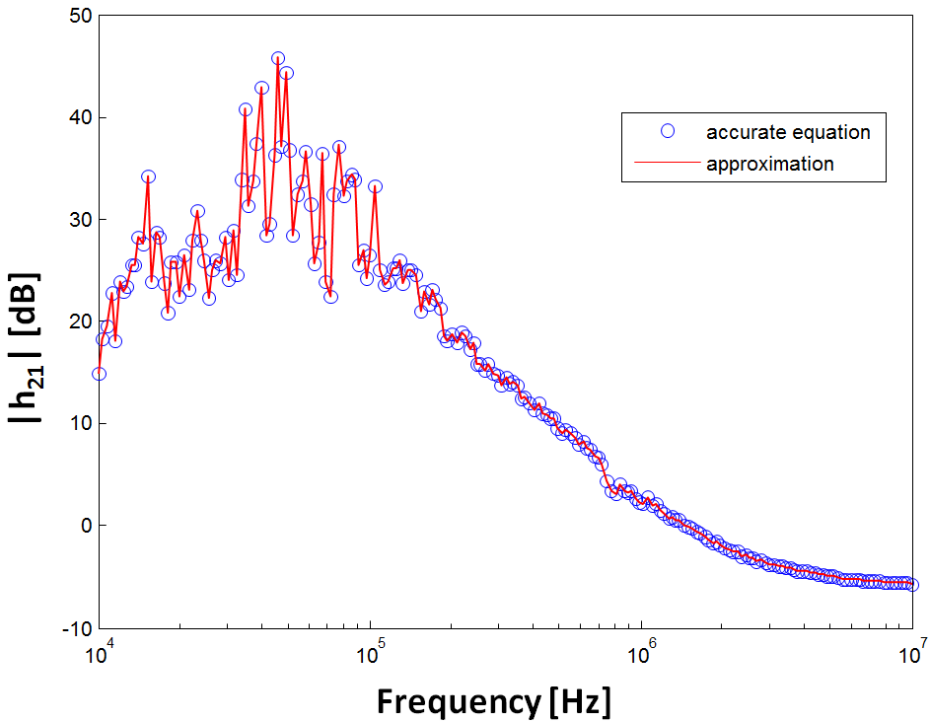


Fig. 3.10 Comparison between terms of $(1-S_{11})(1+S_{22})$ and $S_{12}S_{21}$

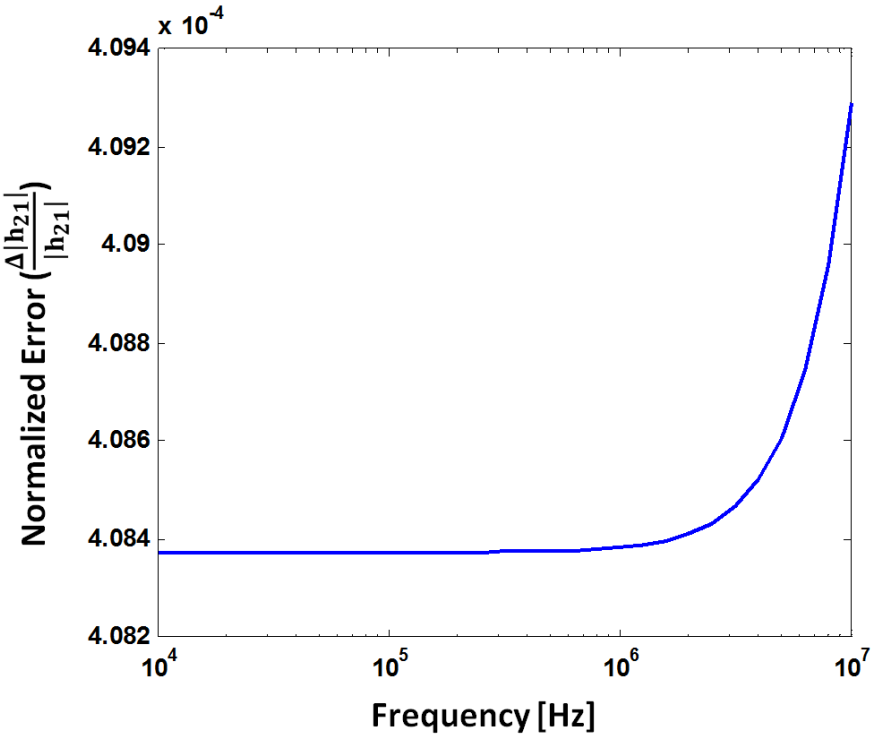
Now from the derivation and verification above, we know the dominating parameters for TFT f_T measurement are S_{11} and S_{21}. Thus, to evaluate the difference of TFT model and CMOS model, we need to evaluate and analyse the two parameters in both models. As both the two measurements need to connect a matched load at port 2 of the network, the equivalent circuit for the measurements is identical as shown in Fig. 3.12. The modelling of each parameter based on the equivalent circuit will be discussed in the following subsections. And the simulation will be based on the static and dynamic parameters extracted in Chapter 2.

S_{11} measurement and analysis

Fig. 3.10 and Fig. 3.11 shows that the measurement at lower frequencies is very noisy especially when S_{11} is involved. The main reason is the contribution of the $1-S_{11}$ term. As discussed before, the S_{11} parameter is very close to 1 due to the near open-circuit characteristic of capacitors at low frequencies. Therefore, the value of $1-S_{11}$ highly depends on the measurement accuracy of S_{11}. According to the datasheet of the network analyser E5061B, the measurement accuracy for S_{11} with different calibration kit is around 0.03 and 2 degree for magnitude and phase measurement respectively, when average factor equals to 1 and 10Hz bandwidth is selected. However, in order to measure the parameters for the device



(a) Calculated h_{21}



(b) Normalized error

Fig. 3.11 Comparison between Eq. (3.20) and its approximation Eq. (3.21)

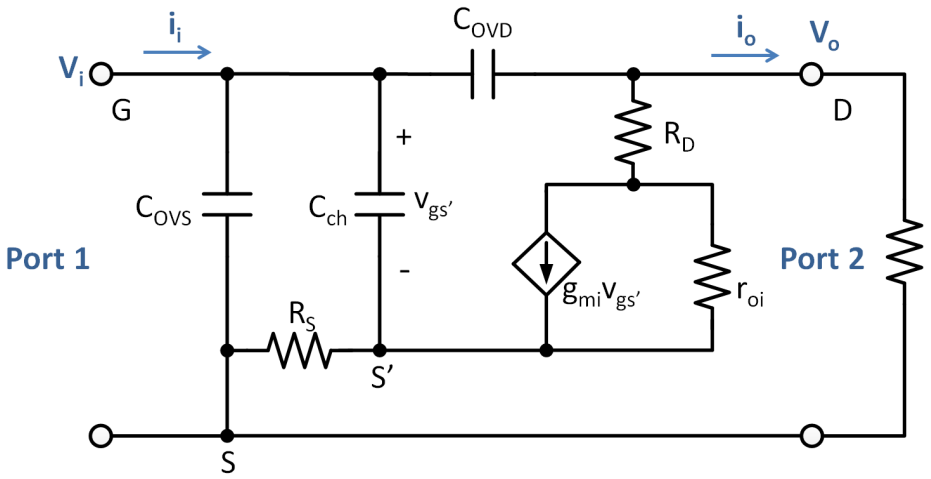


Fig. 3.12 Equivalent circuit for S_{11} and S_{21} measurement

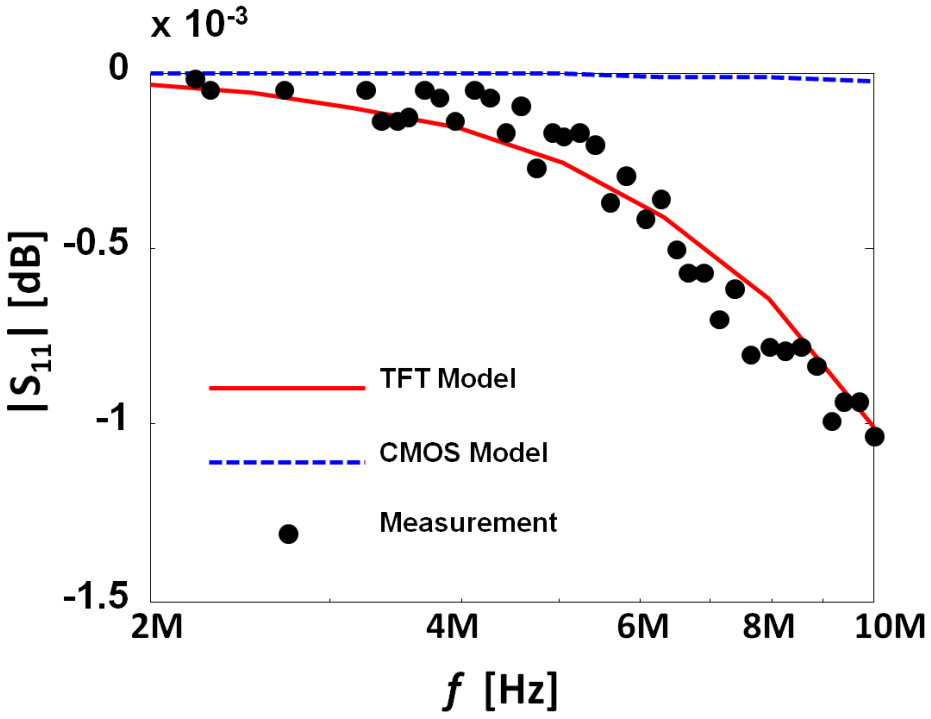
under test (DUT), the accuracy is not enough as the values of the S_{11} magnitude and phase are 1 order smaller than the corresponding accuracies.

Further, after checking the measurement results, we noticed that the major uncertainty comes from the shift of the machine property over time. As this shift in rather slow compared with one cycle of a frequency sweep, we choose to do two quick sweeps with and without the device connected to measure the S_{11} value. The open-circuit values are then subtracted from the measurement results to cancel the property shift of the machine.

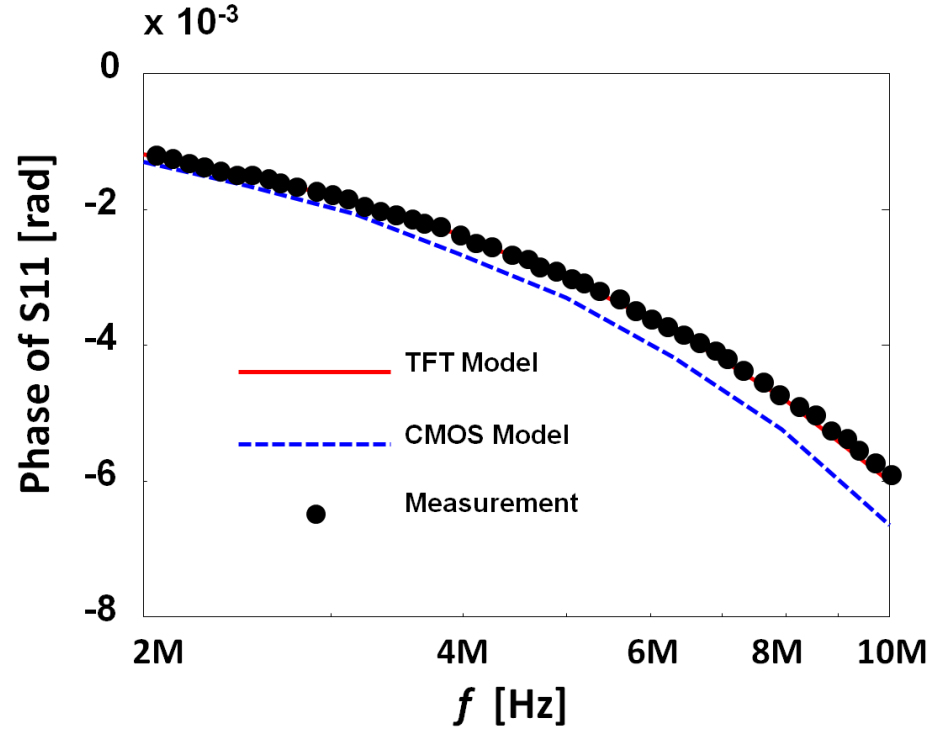
The measurement and simulation results are shown in Fig. 3.13. As can be seen, TFT model fits much better compared with adapted CMOS model. The major difference comes from the magnitude measurement as the measured curve drops, which suggests that there's at least an extra pole for the S_{11} expression of TFT model higher but close to the frequency of concern. The calculation based on CMOS model gives the S_{11} model below:

$$S_{11_{CMOS}} \approx -\frac{-g_0^2+(C_{OVS}+C_{ch})g_0 s+C_{OVD}(C_{OVS}+C_{ch})s^2}{g_0^2+(2g_0C_{OVD}+g_0(C_{OVS}+C_{ch}))s+C_{OVD}(C_{OVS}+C_{ch})s^2} \tag{3.22}$$

where $g_x = \frac{1}{r_x}$ is the conductance of the corresponding resistor. The conductance terms are used to make the equation looks simpler. An approximation is also used to simplify the equation based on the assumption that $g_0 >> g_m$ and $g_0 >> g_o$. This is particularly true in the case of TFT because of the high resistance of TFT devices. For example, $1/g_m$ is normally around a few $k\Omega$ to a few $100k\Omega$ and r_o is around a few $M\Omega$. However, the characteristic resistance is 50Ω. Therefore the conductance of the characteristic resistance g_0 should be more dominant compared with all other resistances and conductances in the



(a) Magnitude



(b) Phase

Fig. 3.13 Magnitude and phase measurement and simulation for S_{11} parameter based on TFT model and adapted CMOS model

small signal model of TFT (or the adapted CMOS one). The assumption is also used in the derivation of S_{11} of TFT model. This model suggests that the equation has 2 zeros and 2 poles. Calculation based on Eq. (3.22) shows that the 2 zeros are at $3.4462GHz$ and $10.853GHz$ and 2 poles at $2.4898GHz$ and $15.022GHz$. As the zeros and poles are all far above the frequency of concern (i.e. below $10MHz$), the S_{11} modelled by the CMOS model would remain at 1 at the frequency range as suggested in Fig. 3.13a (which suggests a very close to open circuit behaviour).

The calculation based on the equivalent circuit shown in Fig. 3.12 gives the S_{11} expression as follows:

$$S_{11_{TFT}} = -\frac{-g_{tot}g_c g_0^2 + a_1 s + a_2 s^2 + (g_c + g_{oi})C_{ch}C_{OVS}C_{OVD}s^3}{g_{tot}g_c g_0^2 + b_1 s + b_2 s^2 + (g_c + g_{oi})C_{ch}C_{OVS}C_{OVD}s^3}, \tag{3.23}$$

where $g_{tot} = g_{mi} + g_c + 2g_{oi}$

$$\begin{aligned}
a_1 &= [g_c g_{tot}C_{OVS} + g_c(g_c + g_{oi})C_{ch}]\, g_0 - (g_c + g_{oi})g_0^2 C_{ch},\\
a_2 &= (g_c + g_{oi})C_{ch}C_{OVS}g_0,\\
b_1 &= [g_c g_{tot}C_{OVS} + 2g_{tot}g_c C_{OVD} + (g_c + 3g_{oi})g_c C_{ch}]\, g_0 + (g_c + g_{oi})C_{ch}g_0^2,\\
b_2 &= (g_c + g_{oi})g_0 C_{ch}(C_{OVS} + 2C_{OVD}).
\end{aligned}$$

Here, the equation has 3 zeros and 3 poles. To further evaluate the difference between the two models we simulated their S_{11} parameters. The simulation results are shown in Fig. 3.14. Just as the figure suggests, two zeros lie between two poles to make a valley of the magnitude curves for both models. However, these poles and zeros are at much higher frequencies compared the cutoff of the transistor. Therefore, the simulation results only show a flat line below $10MHz$ for CMOS model. As for the TFT model, the numeric calculation shows that there are 3 poles at $54.755MHz$, $2.8314GHz$ and $19.389GHz$. The zeros are at $54.947MHz$, $4.5660GHz$ and $11.981GHz$. The 2 zeros and 2 poles at GHz level have similar values compared with the CMOS model to make a similar shape of the curve at very high frequency. However, they would not create much difference at the low frequency range of our concern either. The major difference we've noticed is the extra zero and pole at $54.947MHz$ and $54.755MHz$, respectively. These two points are pretty close to the cutoff frequency and the frequency of concern. From further inspection of Fig. 3.13 and Fig. 3.14, we notice that it is these pole and zero that cause a slight drop of the S_{11} magnitude. As the pole is slightly smaller than the zero (although only by less than 1%), the magnitude starts to drop a little before the effect is cancelled by the zero. This drop distinguishes the two model at around $10MHz$ range as the measurement in Fig. 3.13 suggests. This also suggests that the TFT

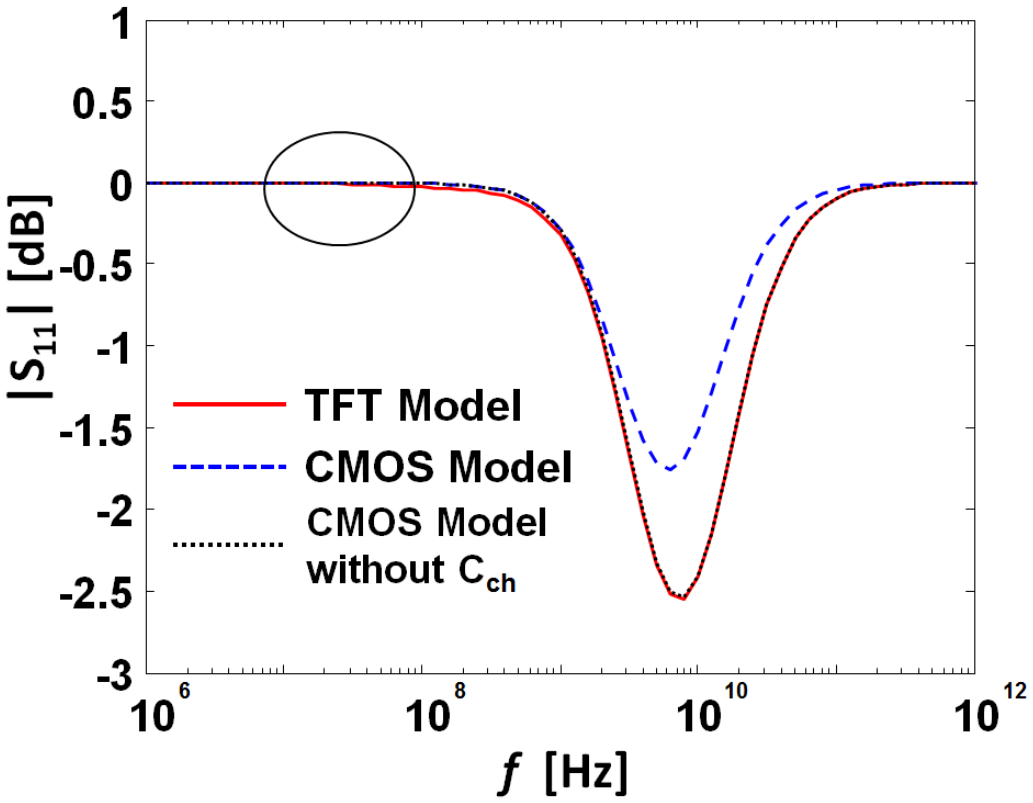


Fig. 3.14 S11 simulation of the TFT and CMOS models

model (with the contact resistance and the separation of the channel and overlap capacitance) captures an extra pole and zero, which results in a better accuracy than the CMOS model.

It can be noted that $|S_{11}|$ equals to $0dB$ (or 1) at both very low frequencies and very high frequencies. This can be explained by the connection of the C_{OVS} as it acts as open-circuit at low frequencies ($S_{11} = 1$) and short-circuit ($S_{11} = -1$) at high frequencies.

Here, as the major accuracy improvement comes from the extra zero and pole, it is worth finding the exact expression of their analytic form. The accurate expressions can be directly extracted from the Eq. (3.23) by solving the cubic equations. However, the expressions become too long for the purpose of estimating the positions of the extra zero and pole. Alternatively, we discovered that by taking out the C_{ch} in CMOS model, the simulation results of the two models become very similar at high frequencies (shown in Fig. 3.14). Therefore, we could compare the coefficients of Eq. (3.23) and Eq. (3.22) (taken out the C_{ch} term) to find the estimated expression of the extra zero and pole assuming that the CMOS model contains all the poles and zeros except the extra ones.

Considering the matching of coefficients, we found the estimated expressions as:

$$\begin{cases} f_{pe} = -\dfrac{g_{tot}g_c g_0}{2\pi(g_0+g_c)(g_c+g_{oi})C_{ch}} \\ f_{ze} = -\dfrac{g_{tot}g_c g_0}{2\pi(g_0-g_c)(g_c+g_{oi})C_{ch}} \end{cases} \tag{3.24}$$

where f_{pe} is the frequency of the extra pole and f_{ze} is the frequency of the extra zero. Here, the expressions give a rather accurate estimation of the extra pole and zero of $54.763MHz$ and $54.946MHz$, respectively, while the numeric calculation gives $54.755MHz$ and $54.947MHz$. Here, with the approximation of the extra zero and pole, one can easily draw the S_{11} curves without simulating of the more complicated equivalent circuit. It also provides support for the possibility of fitting a S_{11} measurement with one pole and one zero.

S_{21} measurement and analysis

As for S_{21}, the simulation and measurement results are shown in Fig. 3.15. The results show that the difference of S_{21} between models is less significant compared with S_{11}. This is because of the parameter varies much in a log scale axis (dB) and, therefore, the difference is not visibly prominent in comparison with that of S_{11}. For example, the measurement value at $8MHz$ is $|S_{21}| = 2.85\times10^{-3}$. The modelled value are $|S_{21_{TFT}}| = 2.88\times10^{-3}$ (yielding 1.1% error) and $|S_{21_{COMS}}| = 2.69\times10^{-3}$ (yielding 5.6% error).

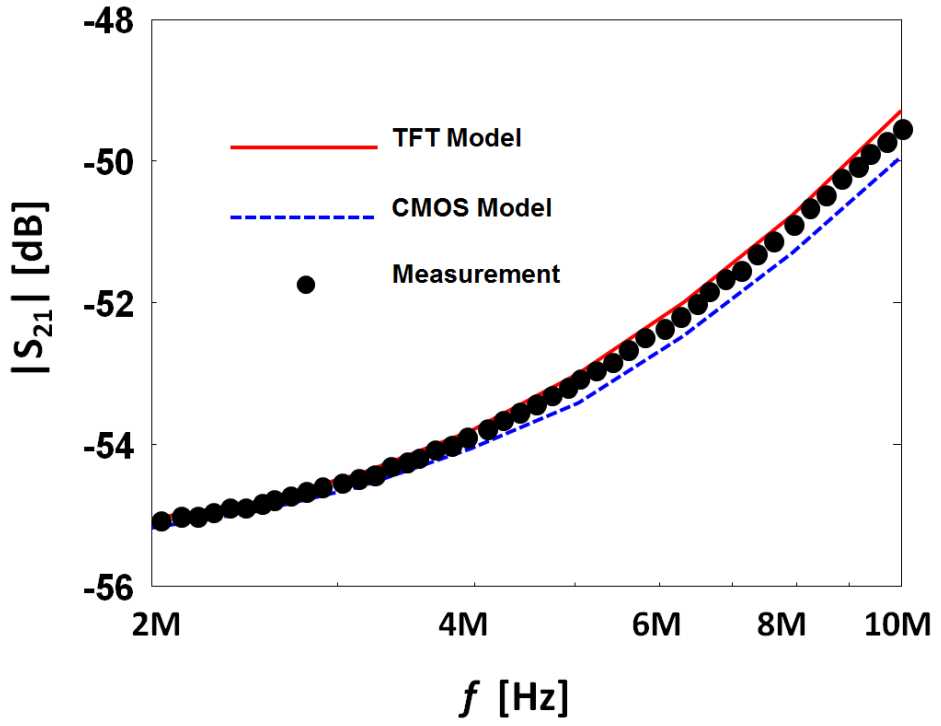
The analytic expression of S_{21} in CMOS model is shown as Eq. (3.25):

$$S_{21_{CMOS}} = \frac{2g_0(sC_{OVD}-g_m)}{g_0^2+(2C_{OVD}+C_{OVS}+C_{ch})g_0 s+C_{OVD}(C_{OVS}+C_{ch})s^2} \tag{3.25}$$

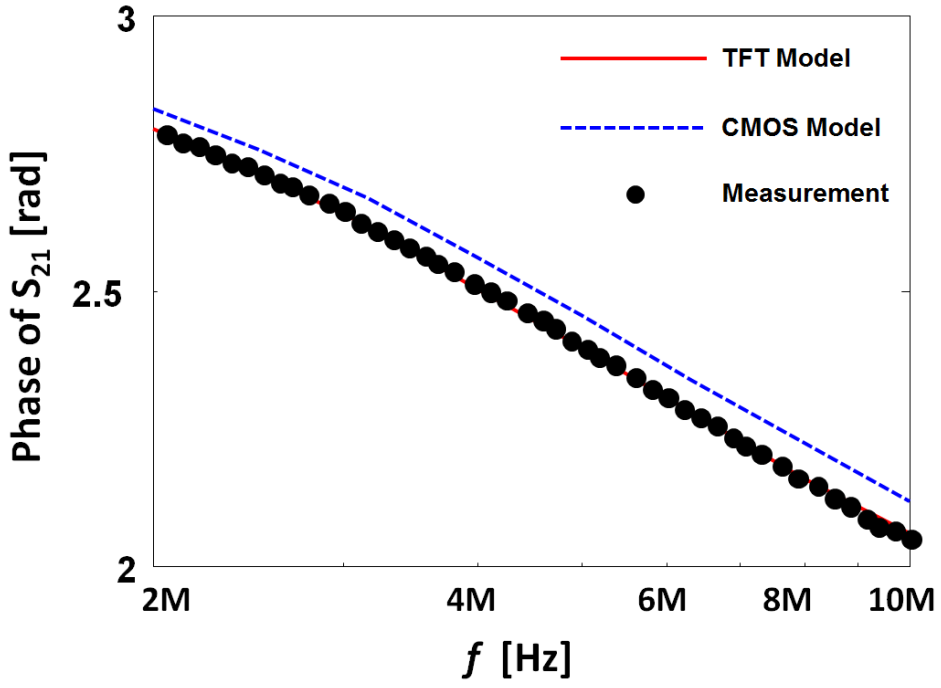
The equation shows that there are two poles and one zero in the model. Calculation based on the equation shows that the zero is at $6.107MHz$ and the two poles are at $2.490GHz$ and $15.02GHz$. Again, as the poles are all far above the frequency of concern, they would not affect the measurement results below $10MHz$. The results that there's only one dominant zero within the frequency range. The other point that should be noticed is that at very low frequencies Eq. (3.25) yields to:

$$S_{21_{CMOS}} = -\frac{2g_m}{g_0} \tag{3.26}$$

Here, the $g_0 = 1/50\Omega^{-1}$ is a known value. Therefore, the S_{21} measurement can directly reflect the small signal g_m for the CMOS model. As discussed in section 3.2.1, the TFT and CMOS models are equivalent at low frequencies as the capacitances can be ignored. Therefore, this g_m can also be used to extract the g_{mi} for TFT model at lower frequencies.



(a) Magnitude



(b) Phase

Fig. 3.15 Magnitude and phase measurement and simulation for S_{21} parameter based on TFT model and adapted CMOS model

As for TFT model, the equivalent circuit for the S_{21} calculation is the same as the one used for S_{11} as the equivalent connection for the measurements are the same (Fig. 3.12). Hence, we could derive the equation of S_{21} as below:

$$S_{21_{TFT}} = 2g_0 \frac{-g_c^2 g_{mi} + (g_c g_{tot} C_{OVD} + g_{oi} g_c C_{ch})s + (g_c + g_{oi}) C_{OVD} C_{ch} s^2}{g_{tot} g_c g_0^2 + c_1 s + c_2 s^2 + (g_c + g_o) C_{ch} C_{OVS} C_{OVD} s^3}, \tag{3.27}$$

where,

$$c_1 = (g_c + g_{oi}) C_{ch} g_0^2,$$
$$c_2 = (g_c + g_{oi}) C_{ch} (C_{OVS} + 2C_{OVD}) g_0.$$

Here, the equation shows two zeros and three poles for TFT model. Based on the parameters of the device under test, we have that the zeros are at $5.501MHz$ and $60.90MHz$ and that the poles are at $54.76MHz$, $2.831GHz$ and $19.39GHz$. Similar to the case for S_{11}, there's one extra zero and one extra pole at $60.90MHz$ and $54.76MHz$, respectively. These extra zero and pole would also contribute a slight drop on the magnitude of S_{21} as they are very close together, just as the case for S_{11}. The difference here is that there's a dominant zero at $5.501MHz$ which is different to the $6.107MHz$ zero for the CMOS model. Hence, the difference of the dominant zero contributes to the major difference between the CMOS and TFT model. And the difference caused by the extra zero and pole becomes less prominent. Here, the dominant zero for S_{21} can be expressed as:

$$f_{z0_{TFT}} = \frac{g_c \left(\sqrt{(g_{oi} C_{ch} + g_{tot} C_{OVD})^2 + 4 g_{mi} (g_c + g_{oi}) C_{ch} C_{OVD}} - g_{oi} C_{ch} + g_{tot} C_{OVD} \right)}{4\pi C_{ch} C_{OVD} (g_c + g_{oi})} \tag{3.28}$$

whereas the dominant zero for CMOS model can be express as:

$$f_{z0_{CMOS}} = \frac{g_m}{2\pi C_{OVD}} \tag{3.29}$$

While CMOS model gives a simpler solution for the dominant zero for the S_{21} parameter, it does not count the contribution of the channel capacitance (C_{ch}). The TFT model, however, accurately models the dominant zero with the contribution of C_{ch} but yields a much more complicated equation.

Again, at low frequencies Eq. (3.27) yields to:

$$S_{21_{TFT}} = \frac{-2 g_c g_{mi}}{g_{tot} g_0} \tag{3.30}$$

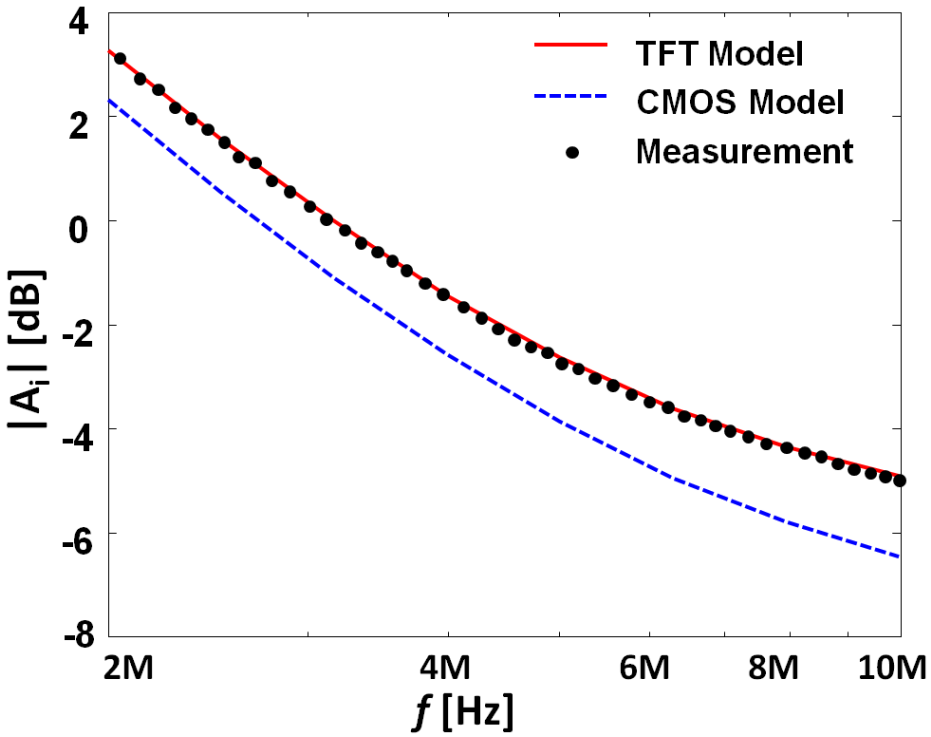


Fig. 3.16 S11 simulation of the TFT and CMOS models

Changing the conductance terms into resistance terms and combining Eq. (3.10), we have:

$$S_{21_{TFT}} = \frac{-2g_{mi}r_{oi}}{(g_{mi}r_{oi}r_c + 2r_c + r_{oi})g_0} = -\frac{2g_m}{g_0} \tag{3.31}$$

This is exactly Eq. (3.26). This confirms that the CMOS and TFT model can be equivalent at low frequencies.

f_T measurement and analysis

As discussed, we can use Eq. (3.21) to calculate the short-circuit current gain of the TFT with enough accuracy. Therefore, we used the measured S_{11} and S_{21} to derive the current gain of the TFT under test and then use a linear fitting to get the value of the f_T.

The measurement results of f_T along with simulations based on the TFT and CMOS model are shown in Fig. 3.16. The measurement results show a cutoff frequency of $3.11MHz$ while the proposed TFT and CMOS models predict cutoff frequencies of $3.14MHz$ and $2.72MHz$, respectively. This yields an error of 1% and 12.5%, respectively.

Here, we proved that the TFT model presented here is more accurate to predict the f_T compared with the CMOS counterpart. However, the measurement results of $|h_{21}|$ or $|A_i|$ only

became consistent with the model at frequencies around MHz level. At lower frequencies, the measurement became very noisy as illustrated in Fig. 3.11. However, as shown in the analysis of Eq. (3.16), the $|A_i|$ curve should be a straight line at lower frequencies as it is dominated by a single pole at 0Hz. The main reason for the discrepancy is the measurement accuracy of S_{11}, especially at low frequencies. As the value of $|S_{11}|$ is very close to, if not exactly equals to, $0dB$ at very low frequencies, the noise of the measurement becomes the major contribution to its value. Therefore, as Eq. (3.21) suggested that the accuracy of $|A_i|$ depends on the subtraction of S_{11} and 1 ($0dB$), the noise of the measurement at this frequency range would dominate the results of $|A_i|$ and make them unreliable. This brings a concern for the measurement of other TFTs with lower cutoff frequency, which means the frequency of concern is lower, or with smaller size, which means that the capacitances are smaller making the gate-source port behave even closer to open-circuit. Therefore, we should use a fitting method to fit the S_{11} parameter before using its value to calculate $|A_i|$ for the cases described above. More detailed discussion regarding S_{11} fitting will be discussed in the next subsection and also be used to measure the V_T shift effect in f_T measurement.

3.3.3 f_T and V_T shift

In this subsection, we will discuss the effect of the V_T shift. As the accuracy of TFT model is proved in the s-parameter and f_T measurements, we would focus on the TFT model.

V_T shift is another important factor for TFTs, as this is one the major concerns in TFT based circuit designs, especially where TFTs' analogue properties are of concern, for example in RFID tags. For the case of the small signal model, the TFT is used as a voltage controlled current source for the input of the small signal. Therefore, it is imperative to consider the impact of V_T shift on small signal model.

In order to examine its influence on the small signal behaviour, a constant bias stress measurement is needed to measure both f_T and V_T of the transistor. However, simultaneous measurement of the two parameters is not practical as the measurements of them need two different connections, i.e. f_T measurement needs network analyser and isolation for DC bias and small signal input and output, however, the V_T measurement needs I-V sweep to measure the transfer characteristics (which we use KEITHLEY 4200 to measure). Therefore, we need to find an alternative way to measure both parameters other than keep switching between different measurement platform.

Here, we decided to use two different constant bias measurements and connect the two parameters through g_m as a bridge. The basic idea is that although f_T and V_T can not be obtained simultaneously, the g_m value can be obtained together in the measurements of both. In specific, g_m can be obtained through derivative of transfer characteristics as discussed in

section 3.1.1. It can also be obtained through low-frequency S_{21} measurement as discussed in section 3.3.2. Also, as V_T directly affects the value of g_m (g_{mi} is considered to be near linearly related to the overdrive voltage ($V_{GS} - V_T$)) and g_m also relates with f_T, g_m can be a perfect link between the two measurements.

f_T and g_m

As discussed in section 3.3.2, a fitting method should be applied to the S_{11} data to obtain a better low-frequency response for the current gain result. Here, as the device under test is smaller in channel width and the cut-off frequency is lower, it is necessary to use the method for better accuracy. The measurement result of S_{11} is shown in Fig. 3.17. The results are fitted using 1 zero and 1 pole approximation following Eq. (3.32):

$$S_{11} \approx \frac{1+as}{1+bs} \tag{3.32}$$

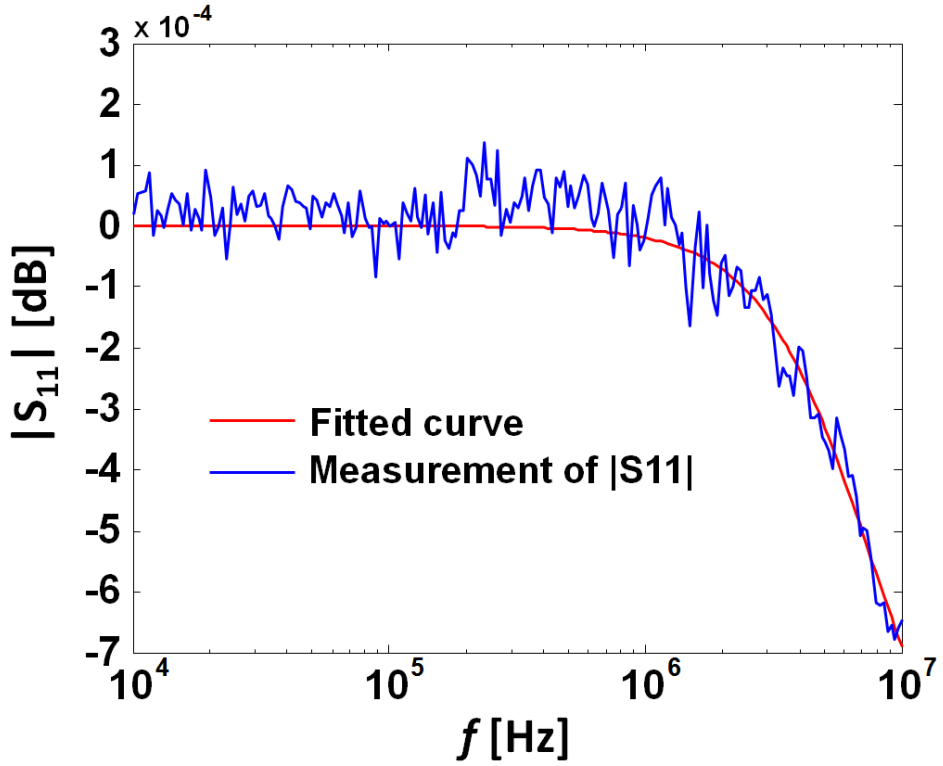
where a and b are fitting parameters. The measurement results are fitted using MATLAB. Here, as illustrated in Fig. 3.17, the measurement results are not reliable below $1MHz$ for magnitude measurement and below $100kHz$ for phase measurement. The major cause of the unreliable results is that the value of $|S_{11}|$ or its phase drops below the noise level at low frequency range. Therefore, the fitting method is imperative to obtain a reasonable low-frequency response. In addition, as the cut-off frequency for the device under test in this subsection is around $1.5MHz$, which is close to the unreliable range of $|S_{11}|$ (below $1MHz$), fitting method is even more important for a better accuracy, especially for capturing the small change of f_T caused by V_T shift.

In order to capture the f_T change under stress measurement, we kept the bias stress for 8 hours and measure the corresponding s-parameters. The converted $|h_{21}|$ with and without the fitting of S_{11} are shown in Fig. 3.18. As illustrated, the $|h_{21}|$ values without fitting are rather random at lower frequencies, which cannot reliably capture the change of the curves versus stress time. However, with fitted S_{11}, we can clearly capture the drop of the cut-off frequency when the stress time increases, as illustrated in the inset of Fig. 3.18b.

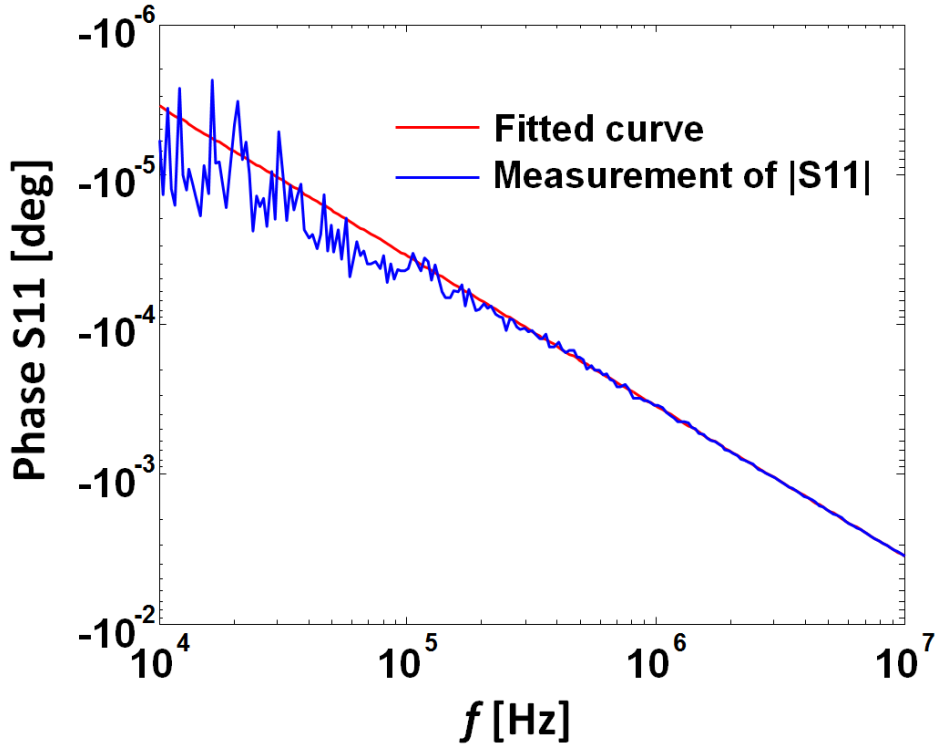
The low-frequency measurement of S_{21} can be used to extract g_m following a derivation from Eq. (3.31):

$$g_m = \frac{g_0|S_{21}|}{2} \tag{3.33}$$

Here, we can use the flat part of the $|S_{21}|$ measurement and calculate the average of $|S_{21}|$ as shown in Fig. 3.19. The value of $|S_{21}|$ drops when bias time increases, which is consistent with the drop of g_m caused by the V_T shift.

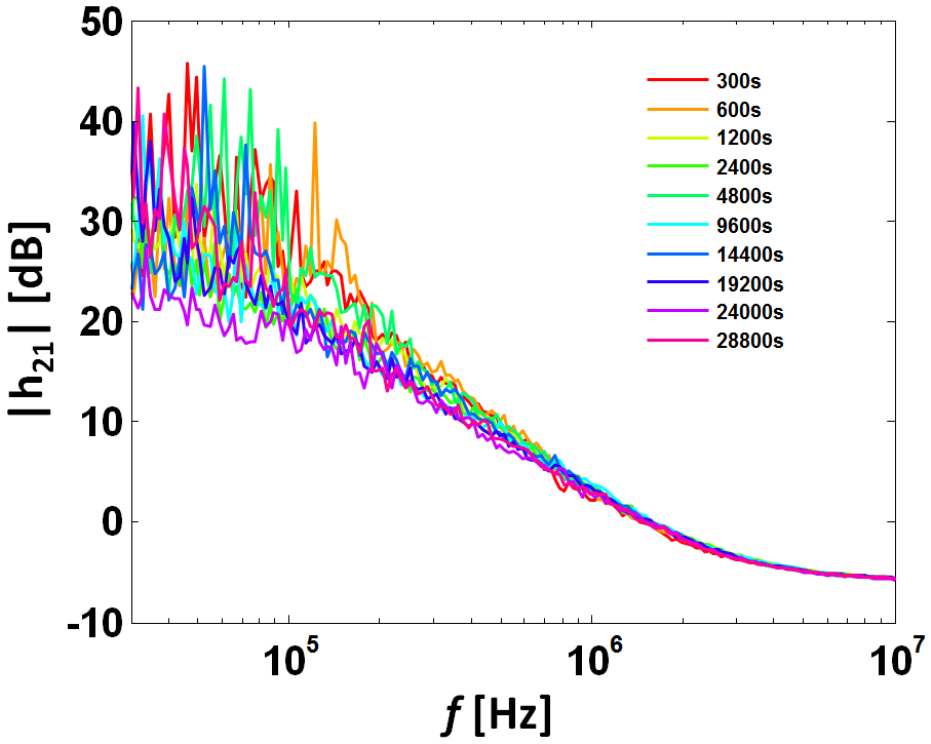


(a) Magnitude

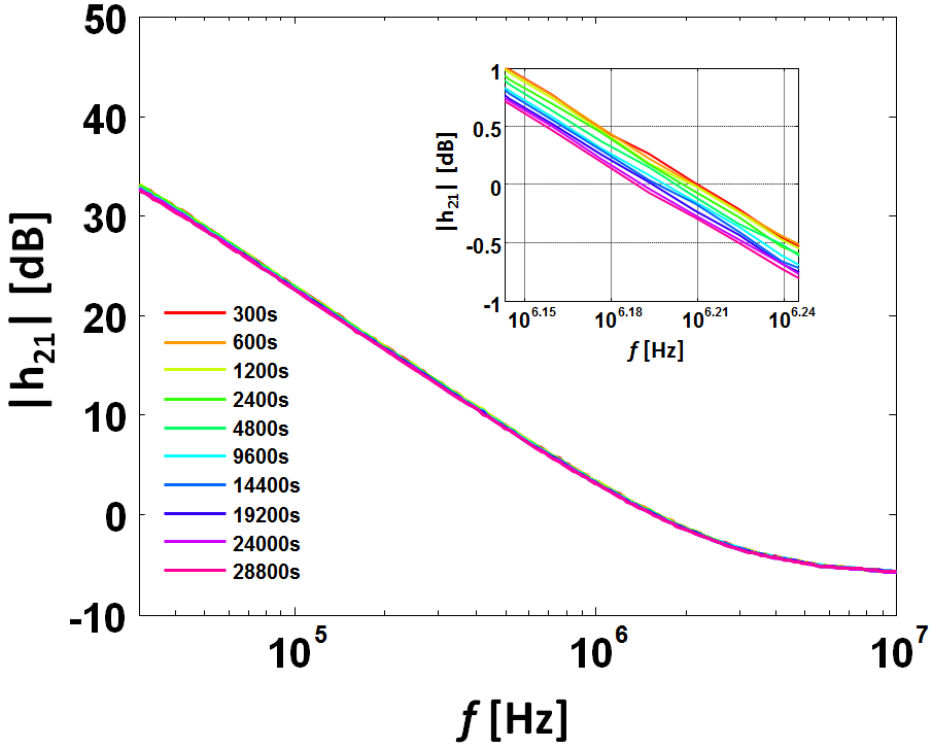


(b) Phase

Fig. 3.17 Magnitude and phase measurement and fitting for S_{11} parameter based on single pole and zero approximation



(a) with S_{11} fitting



(b) without S_{11} fitting

Fig. 3.18 h_{21} results with and without S_{11} fitting

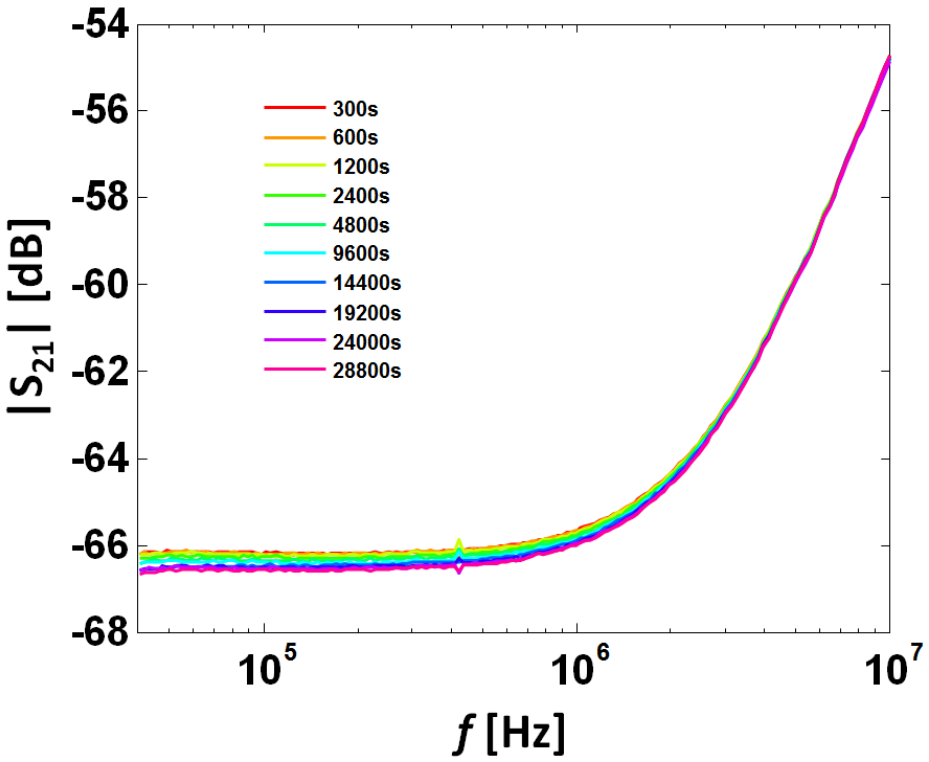


Fig. 3.19 S_{21} measurement showing low frequency range for g_m extraction

By extracting g_m through Fig. 3.19 and the corresponding f_T through Fig. 3.18b, we can get the f_T vs. g_m relation as shown in Fig. 3.20. The results show a linear approximation to Eq. (3.17).

g_m and V_T

The g_m vs. V_T relation can be measured through I-V measurement of the device. The TFT under test was biased at $V_{GS} = 8V$ and $V_{DS} = 15V$ and I-V sweep was done every logarithmic time interval in order to extract the g_m and V_T. The constant stress bias is disrupted for a short time due to the measurement. However, because the sweep time (V_T measurement) is much shorter compared with the bias time, we assume that the short pause for the constant stress can be omitted. Notwithstanding this, the results showed that V_T continued rising after the sweep and the extracted value is then used to extract the relation between g_m and ΔV_T. The extracted results are illustrated in Fig. 3.21.

Combining the results of Fig. 3.20 and Fig. 3.21, we can get the f_T vs. ΔV_T relation as illustrated in Fig. 3.22. The corresponding V_T was obtained through cubic polynomial fitting of the curve in Fig. 3.21. The error bar here is the standard deviation of the fitting to obtain the corresponding result. In specific, the standard deviation of Δf_T was obtained from the

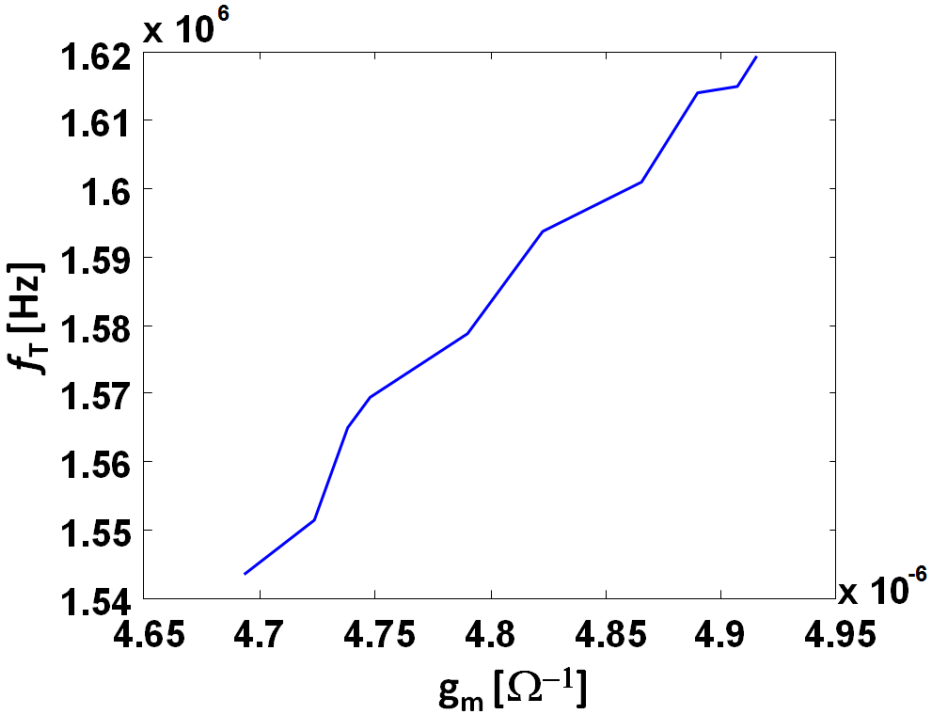


Fig. 3.20 f_T vs. g_m relation through S-parameter measurement

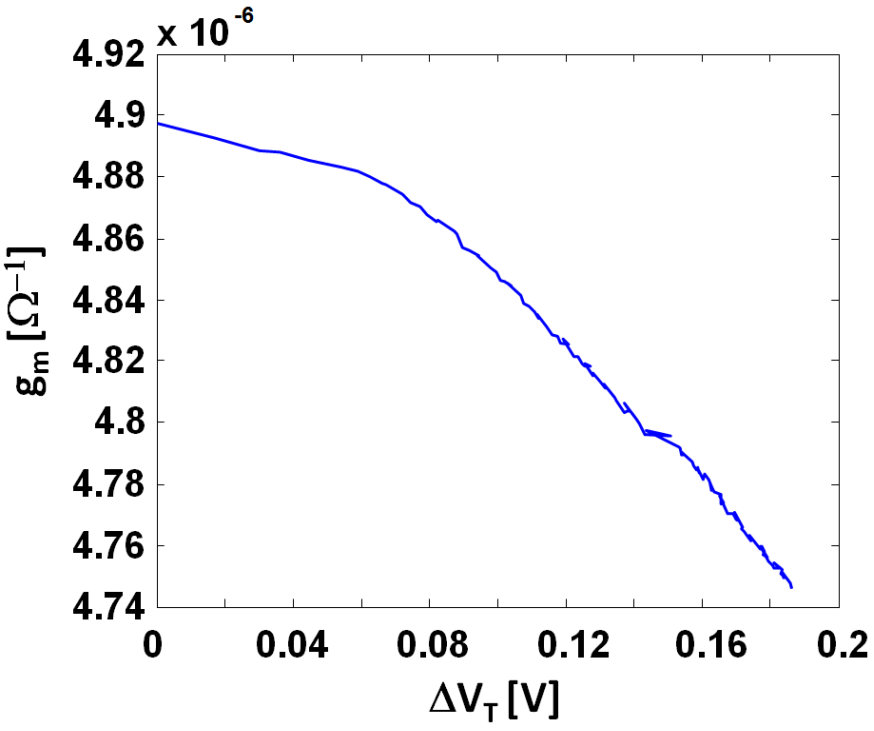


Fig. 3.21 g_m vs. V_T shift relation through stress measurement with I-V sweep

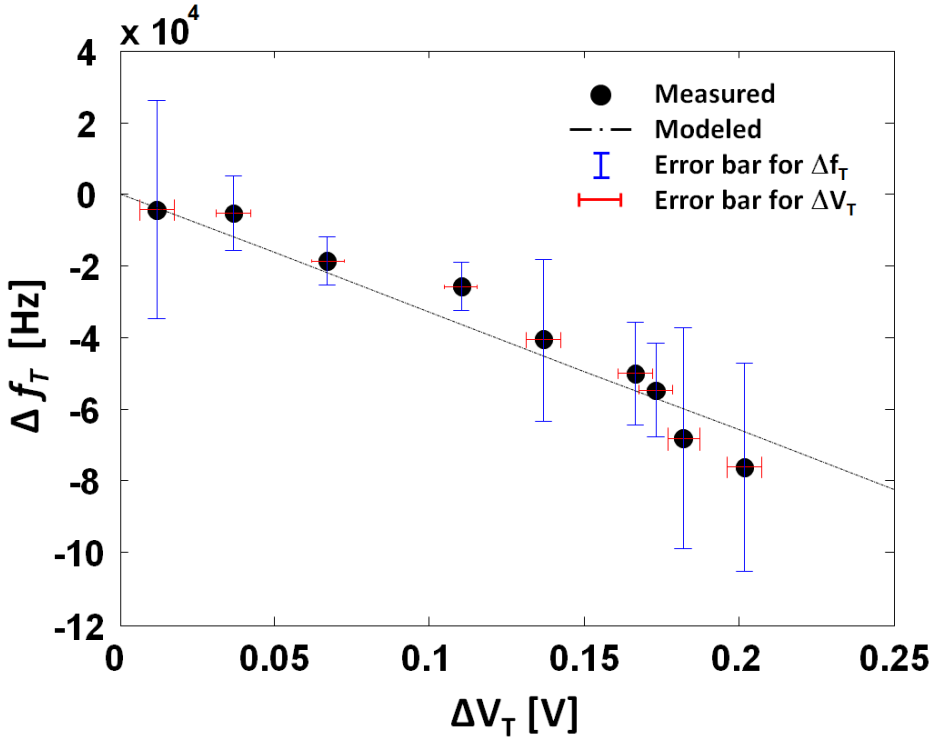


Fig. 3.22 Extracted Δf_T vs. V_T shift relation. The error bar here is the standard deviation of the fitting to obtain the corresponding result.

linear fitting to obtain the corresponding f_T. The standard deviation of ΔV_T was obtained from the polynomial fitting of the curve in Fig. 3.21.

The ΔV_T increased to $+0.2V$ in total after the 10 hours bias stress and the respective Δf_T drops to $0.08MHz$ almost linearly. This is due to the relatively small ΔV_T compared with V_{GS} which leads to a first-order approximation of Eq. (3.17). From Eq. (3.13) & (3.17), we have:

$$\Delta f_T \approx -\frac{r_{oi}(2R_C + r_{oi})(C_{OV} + C_{ch})}{2\pi\left(g_{mi}C_{OV}R_C r_{oi} + (2R_C + r_{oi})(C_{OV} + C_{ch})\right)} K' \Delta V_T = \beta \Delta V_T \tag{3.34}$$

where β is the constant found to be about $-3.2 \times 106[Hz/V]$ for the examined TFT. Eq. (3.34) allows estimating the shift in unity gain frequency with threshold voltage shift. Here, the coefficient β will be different for different material- and process-based TFTs.

3.4 Summary and Discussion

Small signal models are indispensable for the design of analogue circuits, especially in the former for the correct phase margin and bandwidth of amplifiers and analogue filters. This chapter reports on an accurate small signal model that takes into account the contact

Table 3.1 Summary of parameters for the CMOS and TFT models

Category	$R_C \approx 0$	$C_{ch} << C_{OV}$	General Case
CMOS and TFT model equivalence	Equivalent	Equivalent	Not Equivalent
Parameter Relation	$g_m = g_{mi} = \frac{dI_{DS}}{dV_{GS}}$ $r_o = r_{oi} = \frac{dV_{DS}}{dI_{DS}}$	$g_m = \frac{dI_{DS}}{dV_{GS}}$ $g_{mi} = \frac{g_m r_o}{r_o - g_m r_o R_C - 2R_C}$ $r_o = \frac{dV_{DS}}{dI_{DS}}$ $r_{oi} = r_o - g_m r_o R_C - 2R_C$	
Cut-off frequency	$f_T = \frac{g_m}{2\pi C_t ot}$		$f_T = \frac{g_m}{2\pi(C_t ot - g_m R_C C_{ch})}$
V_T shift terms	$g_{mi} = g_{mi0} - K'\Delta V_T$ $K' \approx \frac{g_{mi0}}{V_{GS} - V_{T0}}$		

resistance, parasitic capacitance, and threshold voltage shift while introducing internal transconductance (g_{mi}) and output resistance (r_{oi}). The proposed TFT model yields a 1% error in predicting the unity gain frequency, in contrast to 12.5% error using the CMOS model. It also provides a better fit to the measured s-parameters.

More importantly, the theoretical analysis suggests that accuracy improvement stems from C_{ch} & R_C connection in the TFT model. It also suggests that the CMOS model can be inaccurate especially when the channel capacitance is more dominant and the contact resistance (R_C) is bigger. Further to the discussion, the summary of the key parameter relations and equivalence of CMOS and TFT model are shown in Table 3.1.

The increase of R_C due to downscaling of TFTs indicates that the proposed TFT model can be more beneficial to use in smaller devices. As R_C and its separation of channel capacitance and overlap capacitance generally exist in many other types of device structures and material families, the model is potentially applicable to other TFTs fabricated on insulator substrates such as glass and plastic. Additional bulk parasitics should be considered when modelling TFT on a semiconductor substrate.

Chapter 4

TFT analogue circuit building blocks

4.1 Status of TFT Circuits

Since the success of TFTs in TFT-LCD and AMOLED industry [**?** **?**], using TFTs to achieve all kinds of functions that could otherwise only be realized by CMOS or BJTs has become an appealing topic for researchers in the field [**?** **?** **?**]. Despite the success in digital logic and ADCs, analogue TFT circuits are still in its infancy. Although quite a few amplifiers have been reported in recent years, few has reported the V_T shift compensation and many are very much relied on tuning the external power supply. However, in the CMOS counterpart, bias independent and stable op-amps are used as modular in many analogue applications [**?**]. Therefore, a more generally usable op-amp block is needed to design a more complicated TFT circuit systems and to implement TFT circuits in a wide range of analogue applications.

4.2 Challenges of TFT Analogue Circuits

TFTs fabricated with different semiconductor materials are generally governed by different internal physics. However, the problems we meet in designing circuit could be similar. Here, we list several outstanding challenges of TFT circuit design.

1. More Resistive Devices

   TFTs are generally more resistive compared with the conventional CMOS devices. This is due to the lower mobility of the semiconductor compared with crystalline silicon. As the electron or hole mobility (500-100 $cm^2/V \cdot s$ for μ_e and 100-400 $cm^2/V \cdot s$ for μ_h) in Si is normally 2 orders higher than the semiconductors used in TFT devices (around 1-20 $cm^2/V \cdot s$ for both except polysilicon). In addition, the insulator layers of TFTs are normally thicker than CMOS which leads to a smaller C_{ox}.

Therefore, the current voltage level becomes very different compared with conventional CMOS design. For example, at a similar voltage bias, TFTs will normally working at a much lower current level. This means that other components in the circuit (such as resistors, diodes etc) has to be working in a similar current and voltage level (i.e. not several orders different). Therefore, the resistors in the circuit need to have a much bigger resistance (approximately 2 orders larger than the ones used in CMOS). However, metal track resistors would take excessive area to achieve big enough resistance.

2. Lacking of complementary device

   The other difficulty of designing TFT gain stages is lacking of complementary devices. In specific, n-type organic TFTs are unstable or with very low equivalent carrier mobility. In the meantime, reliable p-type metal oxide TFTs does not exist either. However, processing limitations restrains circuit designers to integrate different material families on the same substrate. Here, as mono type (n-type or p-type) circuit design is symmetrical, we take IGZO TFTs as an example where only n-type TFTs are available.

   N-type transistors are generally good to be used as a current sink, where the source terminal should be grounded and current flows into the drain of the transistor. Here, the circuit will benefit from the high small signal impedance of the output curve, as the gate-source voltage (V_{GS}) can be easily maintained through fixed voltage bias.

   However, designing a current source (other than sink) with n-type transistors becomes much harder as the current should flow out of the source of the transistor (to supply current to the load). Therefore, the voltage level at the source terminal cannot be set at a fixed bias making it difficult to maintain a fixed V_{GS} and hard to benefit from the high output resistance from output characteristics. As n-type gain stages need a current source as load for amplification, the design of amplifier with high gain becomes difficult.

3. V_T shift

   V_T shift problem is one of the most recognised issues in TFT circuits. Successful compensation of V_T shift solves the stability issue in AMOLED display leading to a great success in AMOLED panels. As discussed in chapter A, a switched capacitor architecture is used for the compensation. However, switched capacitor circuits needs extra clock based biasing circuitry to be functional. The major difficulty in design is due to the stretched-exponential behaviour with respect to time, which can be

mathematically expressed as:

$$\Delta V_T = (V_{GS} - V_T)\left(1 - exp\left(-\left(\frac{t}{\tau}\right)^{\beta}\right)\right) \tag{4.1}$$

The equation is highly initial condition dependent. With a few switching, the coefficient β and τ cannot be the same as the initial condition before the TFT was turned on, making it difficult to predict the behaviour afterwards. The switched capacitor circuits was therefore used to sample the V_T. However, in analogue amplifier, we normally expecting a continuous amplification. This effect can be cancelled as ΔV_T is proportionally related with $V_{GS} - V_T$ for certain TFT connections [**?**]. In short, when TFTs are connected in series the voltage dividing behaviour will be V_T shift independent. When TFTs are connected as a current mirror, the current copying behaviour will be V_T shift independent. This discovery will be used in the circuit blocks we design in the next section.

4.3 Building Blocks and Simulations

Several analogue building blocks for n-type TFTs are designed with the aim of realizing a full op-amp in TFTs. It is worth mentioning that although TFT based amplifying stages has been reported in many publications to exhibit some gain, biasing circuitries are mostly ignored. However, a stable and supply-independent biasing circuitry is indispensible for a stable performance in practice where the power supply could be less accurately controlled than the power sources used in a labortory, for example a battery or a super-capacitor. In addition, for wearable applications, it is more preferable to use fully TFT based flexible circuits and remove the rigid CMOS based biasing circuitry. In this section, we will design several analogue building blocks including voltage reference, current mirror, current reference and a differential amplifying stage. Althought the designs here are aimed at realizing an op-amp, the building blocks are applicable to other applications and designs.

4.3.1 Voltage Reference

Many applications need a stable voltage reference to supply an accurate voltage. For example, a DC-DC converter would need a reference to maintain the output at an accurate level. An ADC would need a reference to compare and convert the measured voltage to digital signal. Here, we designed a supply independent voltage reference. Luis Toledo, et al. have reported a circuit with 4 transistors to generate a V_T related voltage reference where one transistor is

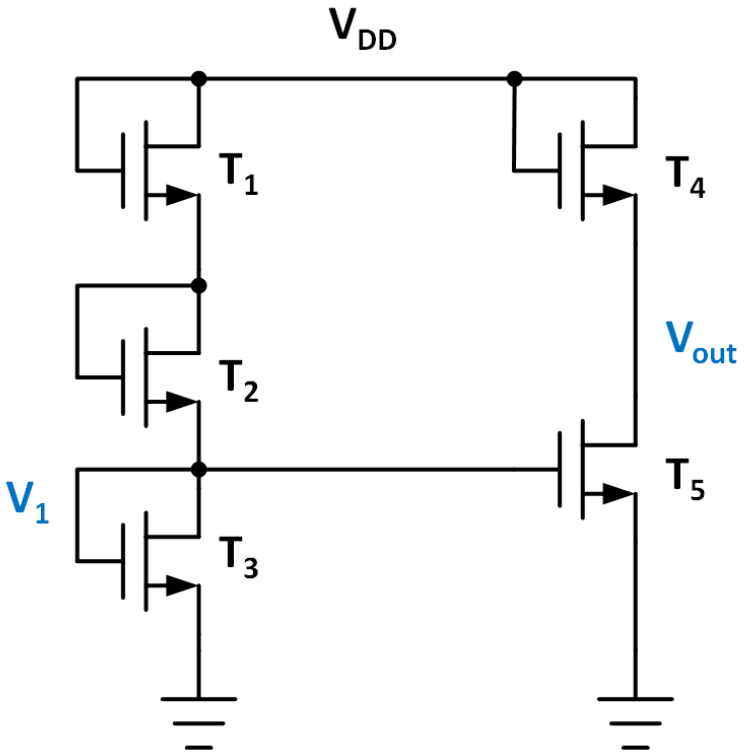


Fig. 4.1 Voltage reference circuit with all TFTs working in saturation region

working in linear region [**?**]. Here, we designed the circuit with the same concept but made all transistors working in saturation region. By changing all transistors to work in saturation, the circuit benefits from a V_T shift independent output [**?**]. The proposed circuit is illustrated in Fig. 4.1.

Here T_1 and T_2 are designed with the same W, $W_1 = W_2$. Based on the TFT saturation model reported in section 2.2.1, the output voltage can be expressed as:

$$V_{out} = \frac{1+2\beta_1-\beta_2}{1+2\beta_1} \cdot V_{DD} + \frac{3\beta_2-2\beta_1-1}{1+2\beta_1} \cdot V_T \tag{4.2}$$

where

$$\beta_1 \equiv \sqrt[2+\alpha]{\frac{W_3}{W_2}}, \quad \beta_2 \equiv \sqrt[2+\alpha]{\frac{W_5}{W_4}} \tag{4.3}$$

The V_{DD} term can be cancelled if the following condition is met:

$$\beta_2 = 2\beta_1 + 1 \tag{4.4}$$

Therefore,

$$V_{out} = 2V_T \tag{4.5}$$

To control the output voltage to be $n \cdot V_T$ is possible if one adds more TFTs in the TFT ladder of the first stage. Here, $2V_T$ is enough for our design. One interesting point here is that V_{out} can decrease with an increased V_{DD} if $\beta_2 > 2\beta_1 + 1$. This is very useful when a negative feedback is needed from the power supply.

As the circuit requires all TFTs to work in saturation region, we could calculate its working range. The lower limit of the working range is when V_{DD} is just enough to turn on all the TFTs at the TFT ladder. Thus, we have $V_{DD} > 3V_T$. The upper limit of the working range is limited mainly the working condition of T_5. As V_{out} remains a constant, high V_{DD} would eventually increase the gate voltage of T_5 making it work in linear region. Therefore, by writing down the saturation condition of T_5, we can get the expression of the whole working region:

$$3 \cdot V_T < V_{DD} < (5 + 4\beta_1) \cdot V_T \tag{4.6}$$

Here, a bigger β_1 could expand the working range by increasing the upper limit. For a more general case where $\beta_2 > 2\beta_1 + 1$ (thus a inverse related V_{out} with respect to V_{DD}), we have:

$$3 \cdot V_T < V_{DD} < \frac{2 + 3\beta_2 - 2\beta_1}{\beta_2 - 2\beta_1} \cdot V_T \tag{4.7}$$

The simulation results for two different β_1 are shown in Fig. 4.2. Here, $W_1/L_1 = 50/20\mu m$. The sizes of other transistors follow Eq. 4.4. The simulation results proves that the higher limit can be controlled by the value of β_1. Both circuits have an output voltage of 2.45V with and error of 0.05V in a 5V range. Considering the voltage supply of most applications would only vary less than 1V, the above design could be enough.

4.3.2 Current Mirror

As mentioned earlier, lacking of complementary devices is one of the challenges for TFT circuit design. Specifically, the load of fully n-type amplifying stages (i.e. resistor load or diode connected n-type load) often has lower small signal output resistance compared with a p-type load. [discussed in Appendix A] Also, as p-type current mirror is not available, differential pair could not benefit from the current steering as in the case of CMOS differential gain stage. To design a circuit block with the same functionality is very beneficial in terms of design flexibility as well as increasing the gain of amplifier stages.

Sanjiv and Nathan had reported a mirrorable current source in [**?**]. Although the design was mirrorable in the V_{DD} side, it needs 2 extra bias voltage to set the current level which do not copy current in the same way as a p-type mirror. Here, we redesigned the circuit and achieved a pseudo p-type current mirror which could replicate the function of a real p-type

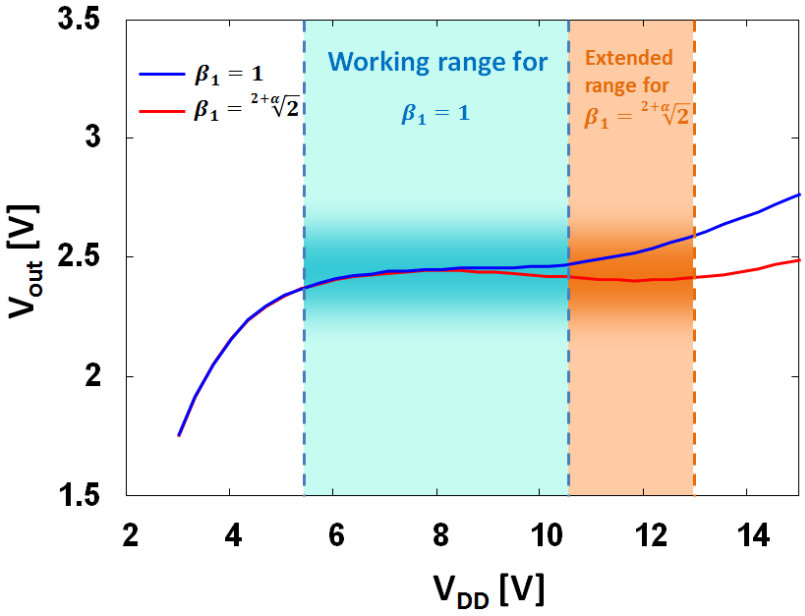


Fig. 4.2 Simulation results for the proposed voltage reference circuit with two different values of β_1

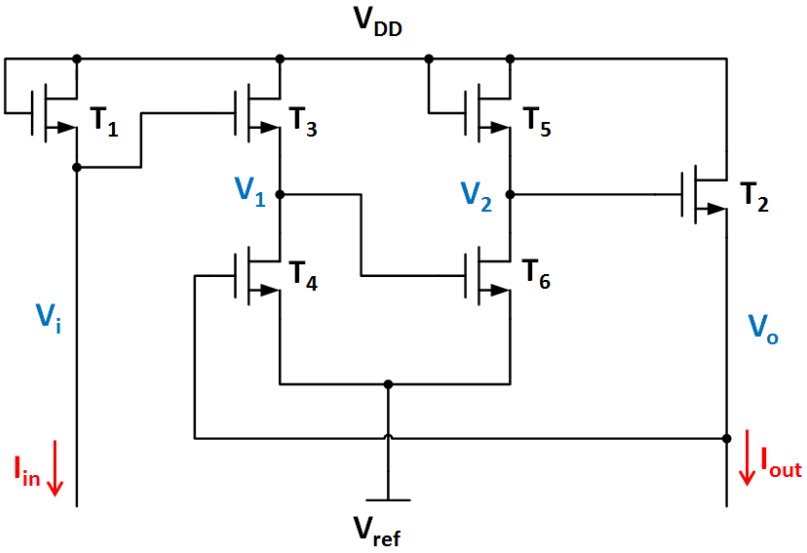


Fig. 4.3 Pseudo p-type current designed with all n-type TFTs

mirror which is shown in Fig. 4.3. The proposed circuit has an extra requirement of output voltage (V_o), as all TFTs especially those in the feedback unit should work in saturation region. The ground of feedback unit (T_3-T_6) are now connected to a reference voltage V_{ref} in order to tune the allowable output voltage range which will be discussed soon. The design

here could replace the p-type mirror in many CMOS design and make many designs available in fully n-type TFT design and keep the benefit of the complementary architecture.

To ensure the circuit's functionality, all TFTs should work in saturation region. This is mainly limited by T_4 and T_6 considering a changing in the level of V_o. Therefore, we have:

$$V_1 > V_o - V_T, \quad \textit{and} \quad V_2 > V_1 - V_T \tag{4.8}$$

By calculating the values of V_1 and V_2, we have the allowable output voltage range as:

$$V_i + \frac{1}{2}V_{ref} - \frac{1}{2}(V_{DD} + V_T) < V_o < \frac{1}{2}\left(V_i + V_{ref} + V_T\right) \tag{4.9}$$

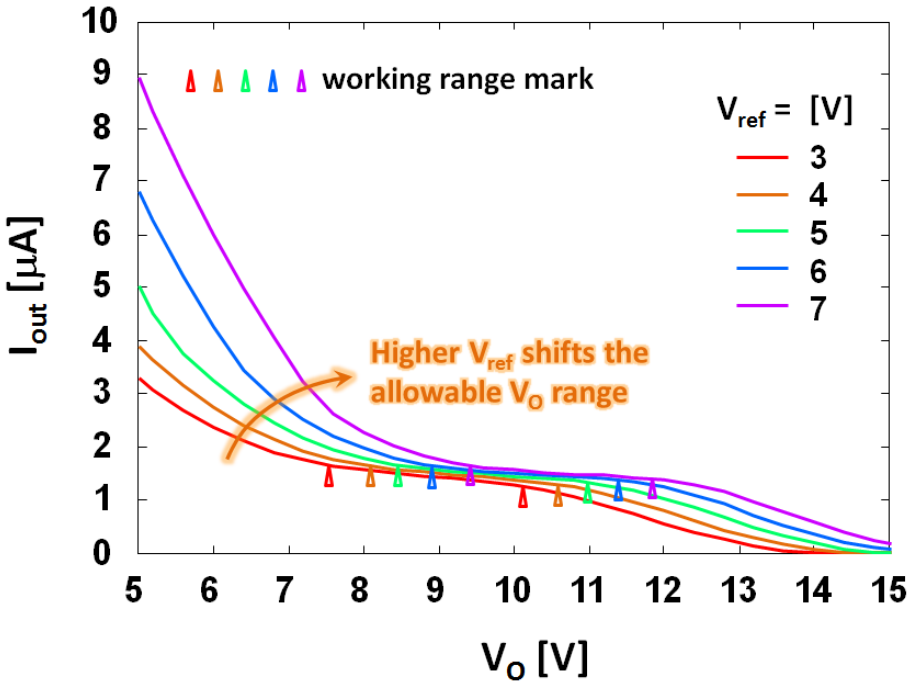
Thus the range of the output voltage is:

$$V_{range} = \frac{1}{2}(V_{DD} - V_i) + V_T \tag{4.10}$$

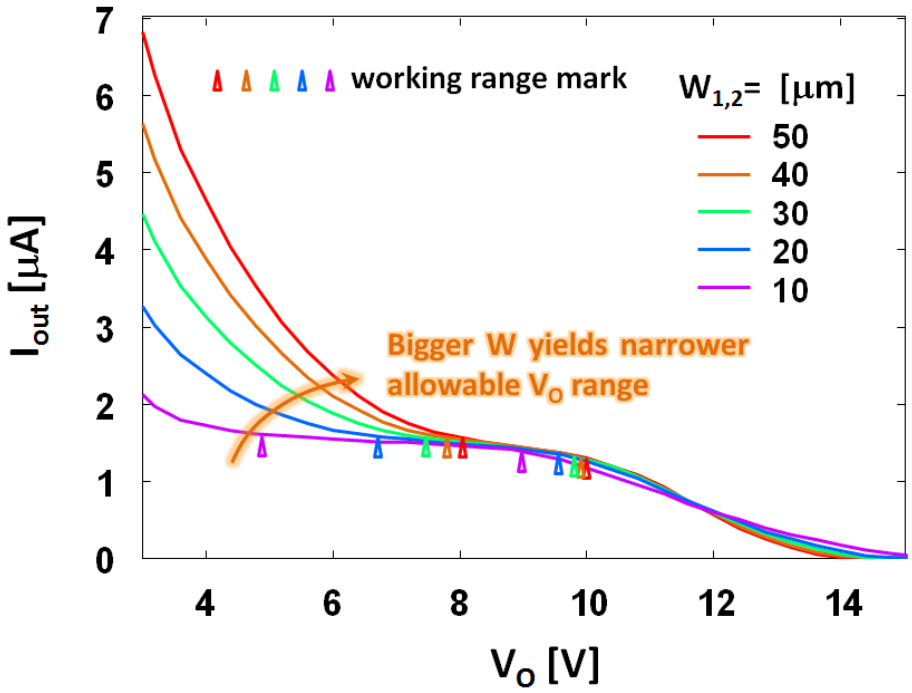
To maximize the output voltage range, one should design a bigger $V_{DD} - V_i$, which is the overdrive voltage of T_1 (meaning smaller W/L ratio is more beneficial for a bigger range of V_o). In addition, as the term $1/2V_{ref}$ appears at both side of the upper and lower limit of V_o, V_{ref} could be controlled to change position of the range but not affecting the width of the range. The circuit is simulated with different V_{ref} values, which is shown in Fig. 4.4a. Here, $W_{1,2}$ is chosen to be $50\mu m$. And T_3-T_6 are designed with the same size. As can be seen from the figure, higher V_{ref} shifts the allowable range of V_o to a higher position but maintaining the width of the range. Fig. 4.4b illustrates the simulation results with different $W_{1,2}$. As expected by the analysis above, shorter $W_{1,2}$ widens the allowable range. The lower limit of the allowable range is pushed further to a lower voltage level while the upper limit shifts only a little lower. Therefore, designer could change V_{ref} and $W_{1,2}$ to design the output voltage range with a desired position and width.

4.3.3 Current Reference

With the pseudo p-type current mirror available, we could implement the current reference circuit which is widely used in CMOS amplifier biasing. The proposed circuit is shown in Fig. 4.5. The CMOS version of this circuit has been reported in [**?**] where subthreshold operation has been considered. Here, we consider the circuit to work in saturation region. As the pseudo p-type mirror simply copies the current of T_1 to T_2. The reference current can be derived by solving the equation below:



(a) Simulation results of the pseudo p-type current mirror with different V_{ref} values



(b) Simulation results of the pseudo p-type current mirror with different $W_{1,2}$ values

Fig. 4.4 Simulation results of the proposed pseudo p-type current mirror

$$\begin{cases} \frac{1}{2}K_1(V_2 - V_R - V_T)^{2+\alpha} = \frac{1}{2}K_2(V_2 - V_T)^{2+\alpha} \\ V_R = \frac{1}{2}K_2(V_2 - V_T)^{2+\alpha}R \end{cases} \tag{4.11}$$

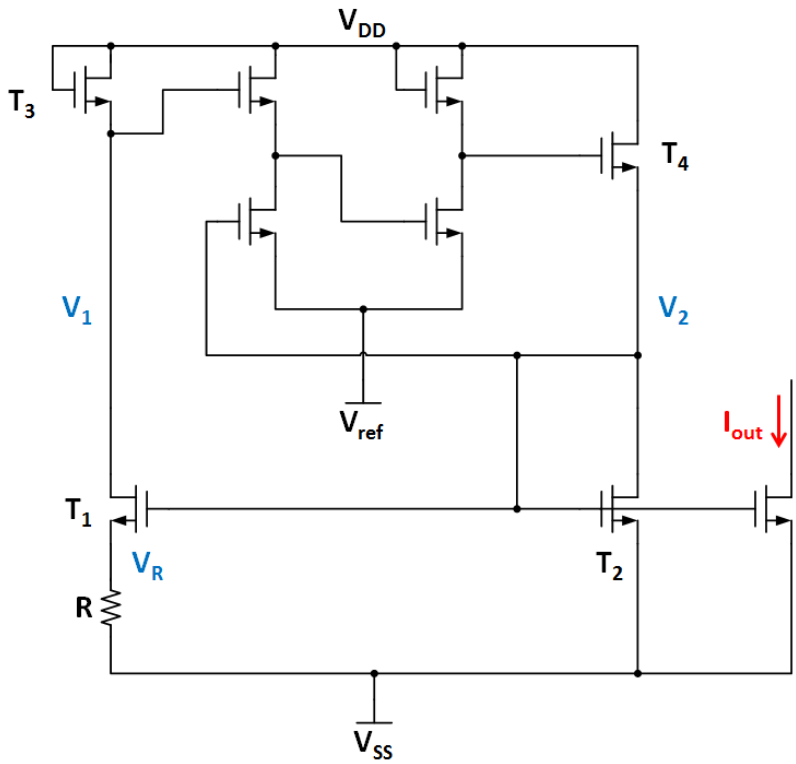


Fig. 4.5 Fully n-type current reference circuit with pseudo p-type current mirror and a reference resistor

Therefore, we get the overdrive voltage of T_2:

$$V_{ov2} = V_{GS2} - V_T = \sqrt[1+\alpha]{\frac{(2+\alpha)\left(1-\sqrt[2+\alpha]{\frac{K_2}{K_1}}\right)}{K_2 R}} \tag{4.12}$$

As V_{ov2} controls the current of T_2, the operating current is then fixed. The current can be expressed as:

$$I_{out} = \frac{1}{2+\alpha}\left(\frac{(2+\alpha)\left(1-\sqrt[2+\alpha]{\frac{K_2}{K_1}}\right)}{\sqrt[2+\alpha]{K_2}R}\right)^{\frac{2+\alpha}{1+\alpha}} \tag{4.13}$$

Therefore, the reference current can be designed by choosing the size of T_2, the ratio of W_2/W_1 and the value of the reference resistor R.

As the circuit also needs all TFTs working in saturation region, we could derive the working range by applying the saturation conditions. The final working range can be derived as:

$$\frac{2}{3}(\mathrm{V_{ov2}}+\mathrm{V_{ov3}})+\frac{1}{3}(\mathrm{V_{ref}}-\mathrm{V_T}) < \mathrm{V_{DD}} < \frac{\mathrm{V_{ov2}}}{2}+\mathrm{V_{ov3}}+\frac{(\mathrm{V_{ref}}+\mathrm{V_T})}{2} \tag{4.14}$$

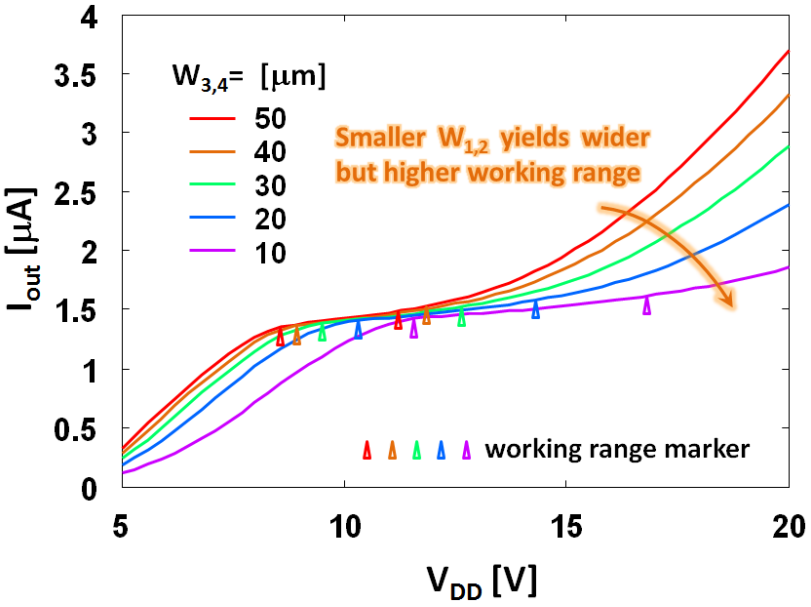


Fig. 4.6 Simulation results of the current reference circuit with resistor where $W_{3,4}$ are simulated with different value to exhibt the change of working range

where V_{ov2} and V_{ov3} are the overdrive voltage of T_2 and T_3. The total working range is then:

$$V_{range} = \frac{1}{3}V_{ov3} - \frac{1}{6}V_{ov2} + \frac{1}{6}V_{ref} + \frac{5}{6}V_T \tag{4.15}$$

Therefore, bigger W_2 and smaller $W_{3,4}$ would be more beneficial in terms of a wider working range (i.e. bigger V_{ov3} and smaller V_{ov2}). Here, we choose $W_1 = 400\mu m$, $W_2 = 100\mu m$ and $R = 600k\Omega$ to yield a current of around $1.5\mu A$, which is a reasonable bias current for a TFT amplifier stage. V_{ref} connected to the ground for an easier biasing of the whole circuit.

The circuit is simulated with different $W_{3,4}$ as shown in Fig. 4.6. The results prove that a smaller $W_{3,4}$ value would yield a wider but higher working range. This is consistent with Eq. 4.14 and 4.15. As can be seen from the figure, the output current is independent of V_{DD} in a 3-5V range for all the designs.

The above design creates a current reference circuit by replacing the p-type mirror of a CMOS design. However, we will need to choose a $600k\Omega$ resistor to generate the current. In many thin-film applications, resistors are not viable as metal track resistors consume too much area especially for a resistor as big as a few $100k\Omega$ and are not accurately controlled. Therefore, replacing the resistor with a TFT is more preferable.

As the resistor here is used mainly for its linear I/V relation, it cannot be replaced by a diode-connected TFT. Therefore, to get a good linearity, the simpliest way is to design a TFT

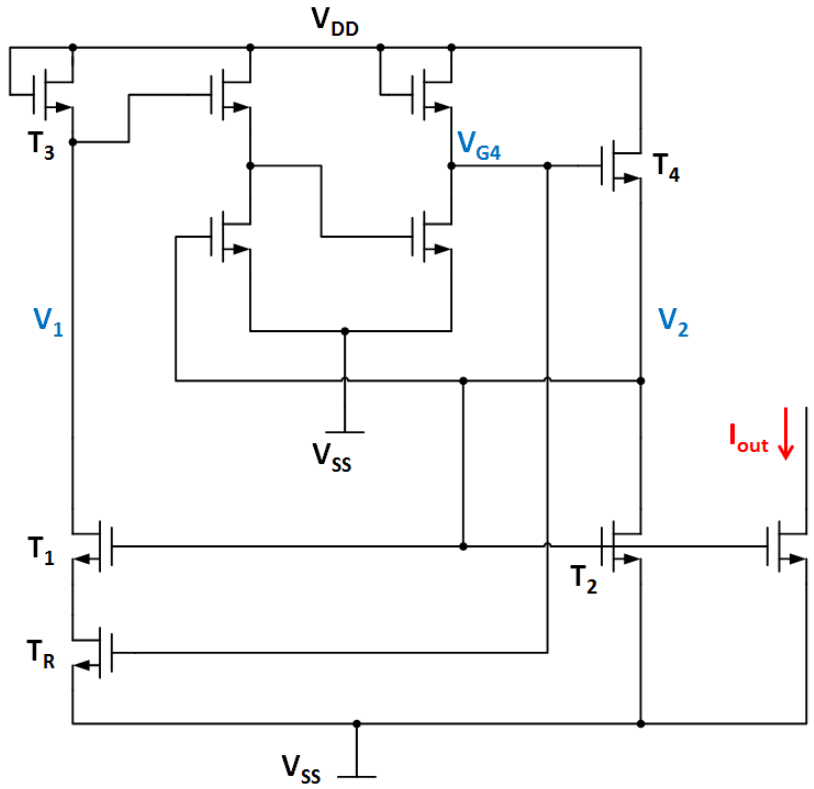


Fig. 4.7 Fully n-type current reference circuit without resistor

working in linear region. As the resistance of TFT in linear region can be calculated as:

$$R_{lin} = \frac{1}{K \cdot (V_{GS} - V_T)^{a+1}} \tag{4.16}$$

This is true when $V_{GS} >> V_{DS}$.

Therefore, to maintain a good linearity, the V_{GS} of the TFT should be fixed with a large value (i.e. independent of V_{DD} and with a value higher than the voltage at the source of T_1). Among all the nodes in the circuit shown in Fig. 4.6, the gate voltage of T_4 meets the aforementioned requirements. Therefore, the circuit is redesigned as shown in Fig. 4.7. The resistor is replaced with T_R whose gate electrode is connected to the gate of T_4.

The size of T_R should be chosen to exhibit a resistance of $600k\Omega$ between drain and source to match the output current with the previous design. The calculation result shows that the width of T_R should be around $29\mu m$.

The simulation of the circuit is done with different W_R which is shown in Fig. 4.8. As illustrated, the circuit still works with a low dependence on V_{DD}. However, the performance of this circuit is obviously worse than the one with a real resistor. The main reason of this comes from the small change of T_4's gate voltage (V_{G4}). As the V_{DD} increases, V_{G4} also

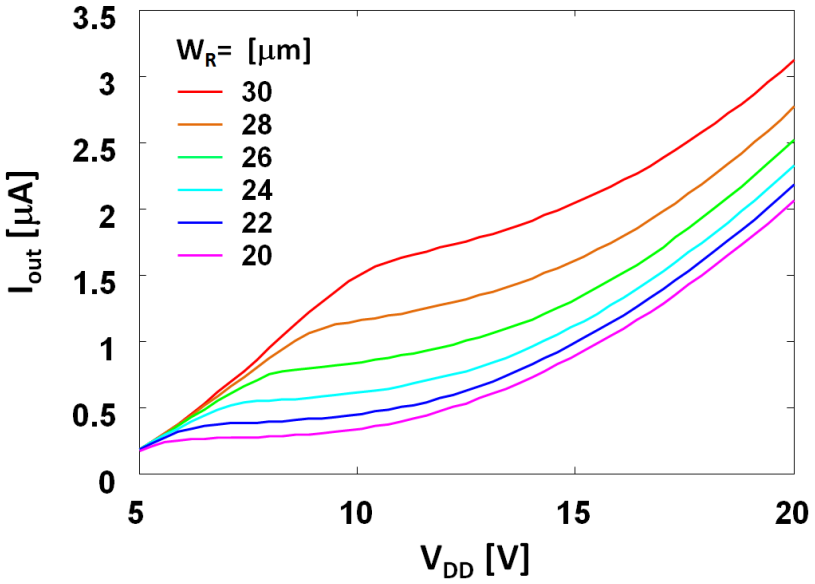


Fig. 4.8 Simulation results of the current reference circuit without resistor where W_R is simulated with different value to exhibt the change of output current

increases a little due to the none ideality of the devices (i.e. non-infinity output resistance). Therefore, the resistance of T_R will decrease according to Eq. 4.16. This will increase the output current and thus forms a positive feedback which deteriorate the circuit performance.

In the case where, the performance of the circuit in Fig. 4.7 is accurate enough we should break the positive feedback that appears on T_R. The voltage reference circuit developed earlier could be used. Thus, the gate voltage of T_R can be more stable, thereby, break the positive feedback loop. The improved circuit schematic is shown in Fig. 4.9. Here, the voltage reference circuit is connected to the gate of T_R making the resistance of T_R more reliable. In fact, as Eq. 4.2 suggests, we could increase β_2 to be higher than $2\beta_1 + 1$ making the output of the voltage inversely related with V_{DD}. Therefore the effect of non-infinity output resistance could be compensated. Hence, a negative feedback can be formed yielding a even better performance.

The simulation results of the improved circuit is shown in Fig. 4.10. As can be seen, output current is much more stable than the previous one and even more stable that the one with a resistor.

As the negative feedback exists in the new circuit, we have a few more bonuses. One of them is the sensitivity on the value of W_R. As can be seen from Fig. 4.10, even sweeping W_R at $100\mu m$ range, the output currents are all stable and with only $1\mu A$ change, which in the previous circuit was achieved with only a few μm change in W_R. Therefore, the improved circuit is more stable against process variations on the size of T_R.

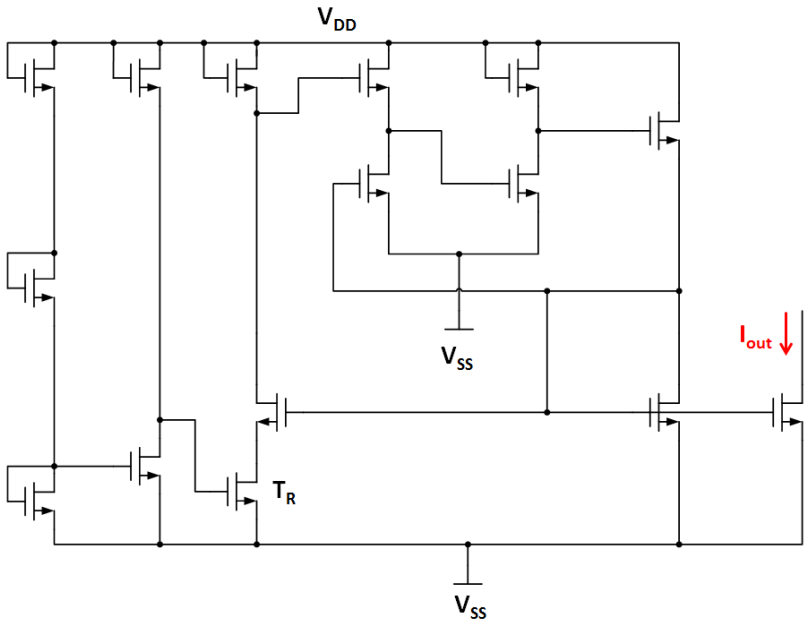


Fig. 4.9 Improved current reference circuit with negative feedback on T_R

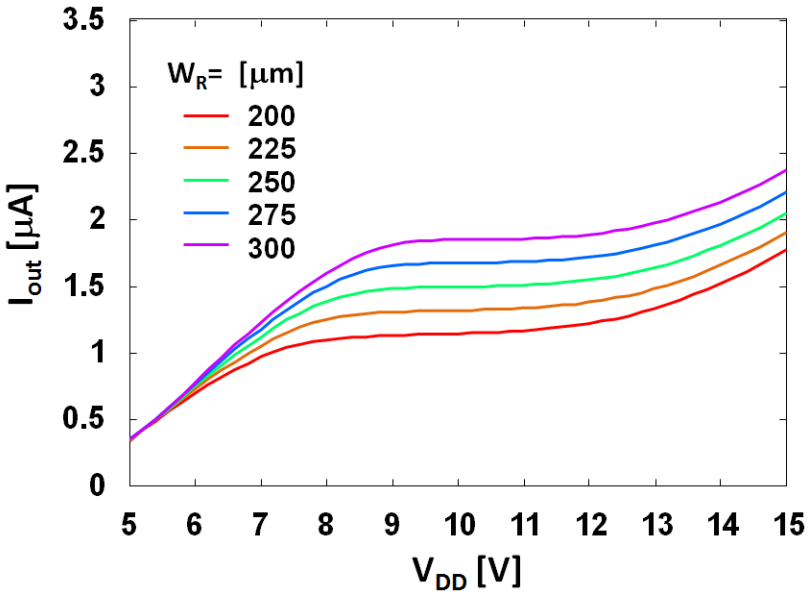


Fig. 4.10 Simulation results of the improved current reference circuit where W_R is simulated with different value to exhibt the change of output current

Another bonus is the V_T shift resistance. Although most blocks designed in this section are V_T shift independent, it is not so for the current reference circuit as T_1 and T_2 are having different V_{GS}. Therefore, as operation time increases, T_1 will become more conductive compared with T_2 and thus increasing the output current (by effectively reducing the value of

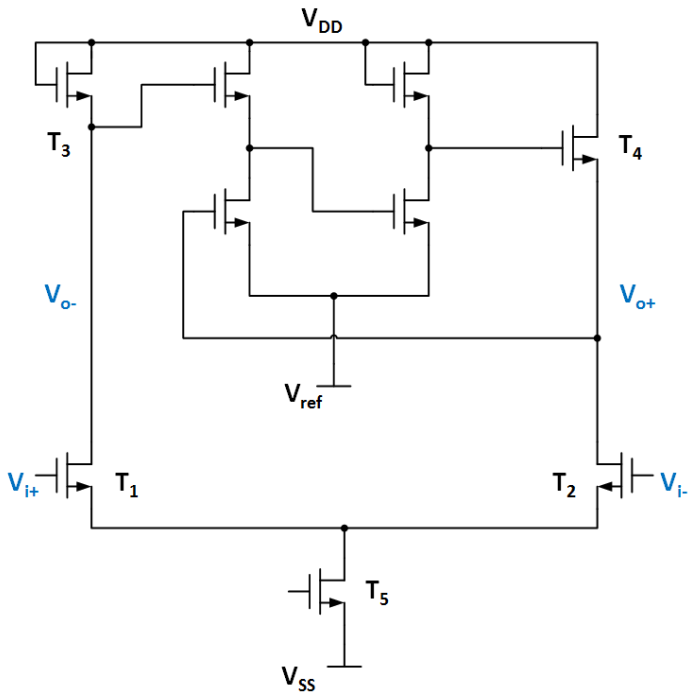


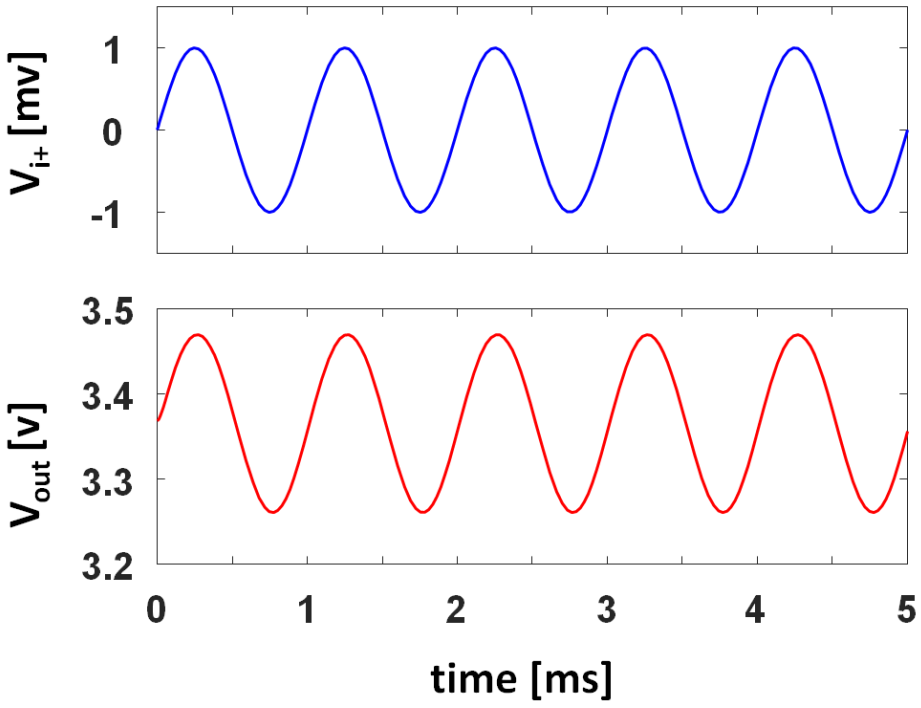
Fig. 4.11 Differential amplifier stage with pseudo p-type mirror

$\frac{K_2}{K_1}$ in Eq. 4.13). However, the V_T shift of T_R will also increase its resistance thus reducing the output current. Negative feedback also exists in terms of V_T shift. Therefore, this more complicated version of current reference yields better V_{DD} independence and at the same time better V_T shift resistance.

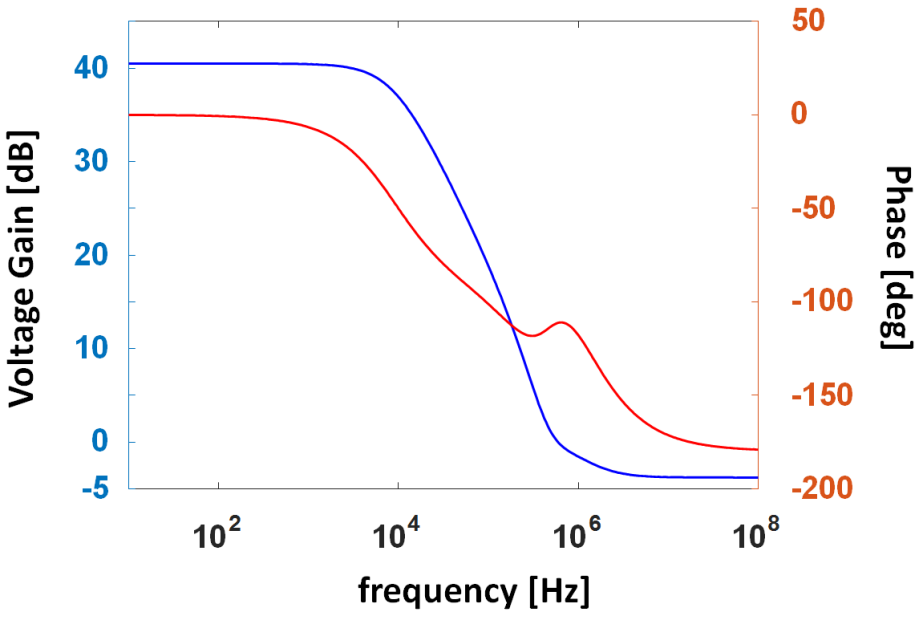
4.3.4 Differential Amplifier

In this section, we consider designing an amplifying stage. With the current mirror designed in section 4.3.2, we could replicate a CMOS differential stage by replacing the p-type current mirror. The design is shown in Fig. 4.11. Here, V_{ref} is connected to ground to optimize the output range. As the pseudo p-type mirror has big output resistance, the voltage gain of this differential stage should be the same as that of a real p-type mirror, in the mean time, current steering feature would also be available thus benefit the gain by an additional factor of 2. The sizes used for simulation is $W_{3,4} = 50\mu m$, $W_{1,2} = 500\mu m$ and $W_5 = 100\mu m$. T_1 and T_2 are designed with big W/L ratio for a higher g_m. Gate voltage of T_5 is set with 3V bias for a $1.5\mu A$ bias current on T_5 which matches the design of the current reference circuit in the previous section.

The transient and ac simulation results are shown in Fig. 4.12. The results suggest that proposed gain stage have over 40dB or 100 gain within the 3dB bandwidth. This is close to



(a) Transient simulation results of the proposed differential stage with $1mVpp$ input at $1kHz$ for $5ms$



(b) Gain-phase simulation of the proposed differential stage yielding a 600kHz unit-gain bandwidth

Fig. 4.12 Simulation results of the proposed differential amplifier stage

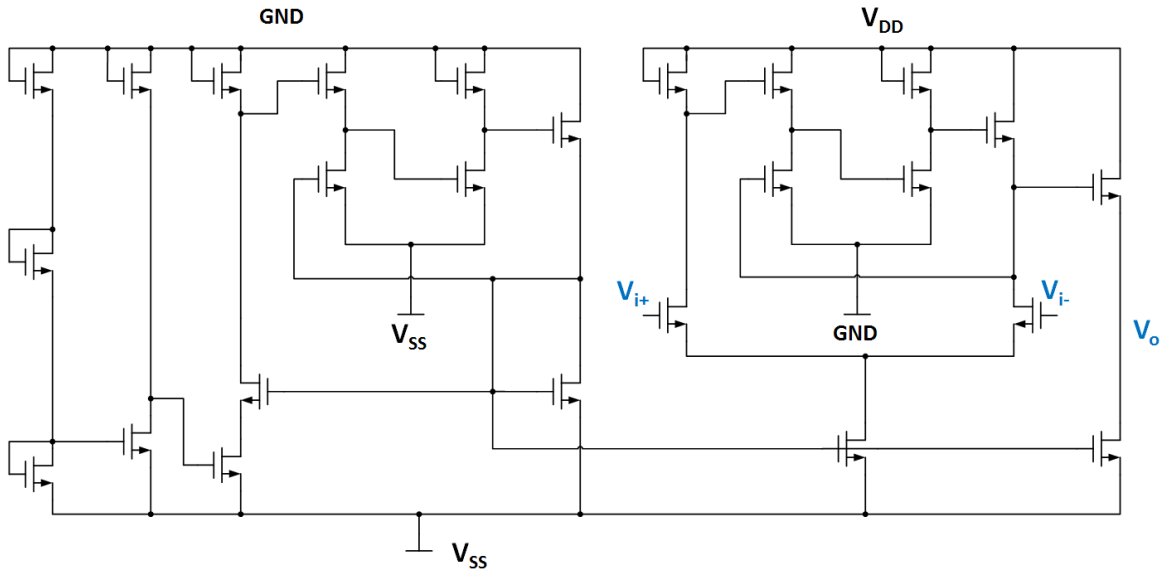


Fig. 4.13 Full op-amp design with supply independent bias

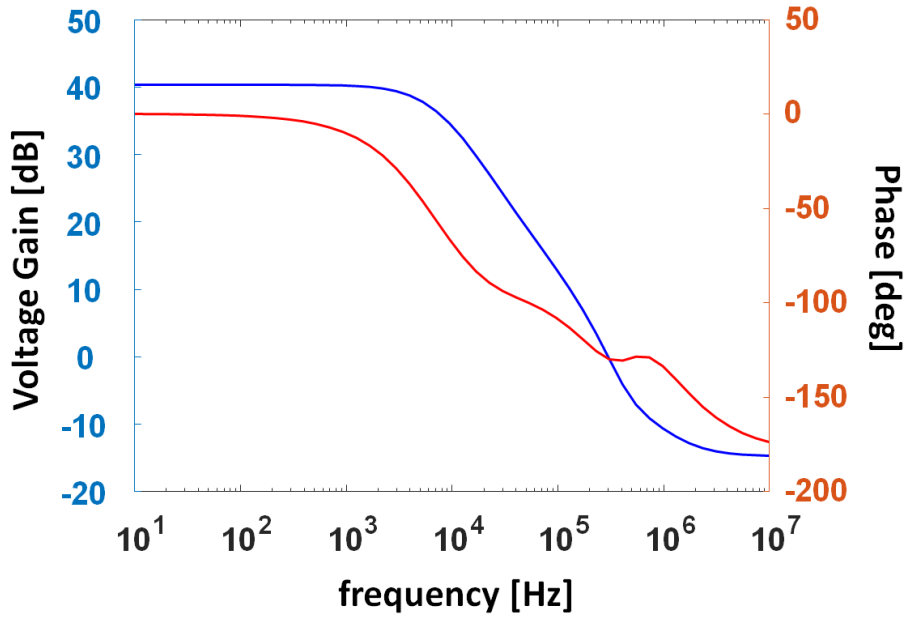
the intrinsic gain of the TFT at the working condition demonstrating that the pseudo p-type current mirror can be used as an promising load in fully n-type circuit design. The gain-phase simulation suggests a 600kHz unit-gain bandwidth of the stage.

4.4 Full Op-Amp Design

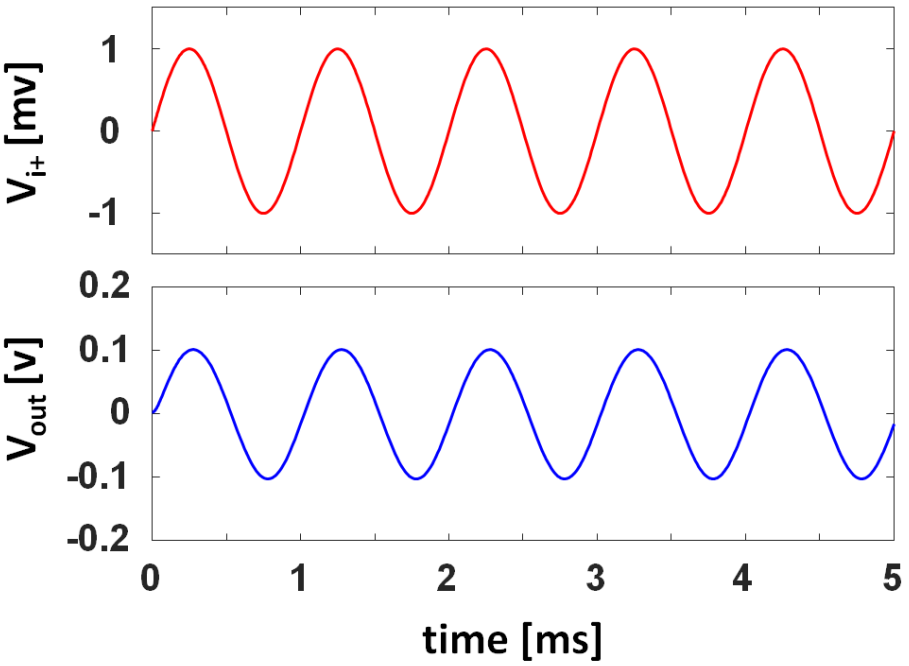
Combining all the building blocks we designed earlier and adding an output stage (which is a source follower stage), we have the full design of a op-amp which is illustrated in Fig. 4.13. The output stage is added to improve the driving capability of the circuit by reducing the output resistance. Simulation result of the proposed op-amp with open circuit load is illustrated in Fig. 4.14. The op-amp here exhibit a gain of 40dB which benefits from the high-gain of the differential stage and a unit-gain bandwidth of 300kHz, slightly reduced compared with the differential pair due to the added stage. The performance here is enough for many bio-medical applications where signal frequencies are below a few 10kHz. The output resistance is reduced to $50k\Omega$ making it capable of driving many CMOS circuits.

4.5 Current Mirror Layout and Measurement

In order to evaluate the effectiveness of the circuit design technique, Indium-Silicon-Oxide (ISO) based current mirrors are fabricated under vacuum process with different layouts. As will be noted, the layout design could also significantly affect the circuit performance.



(a) Transient simulation results of the proposed op-amp with $1mVpp$ input at $1kHz$ for $5ms$



(b) Gain-phase simulation of the proposed op-amp yielding a 300kHz unit-gain bandwidth

Fig. 4.14 Simulation results of the proposed op-amp

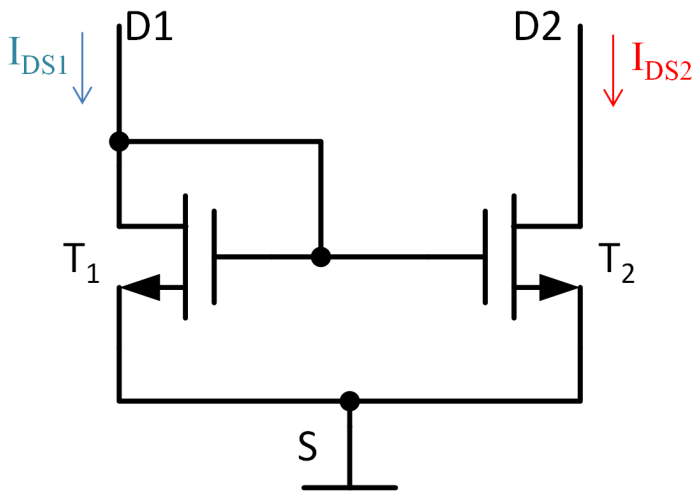


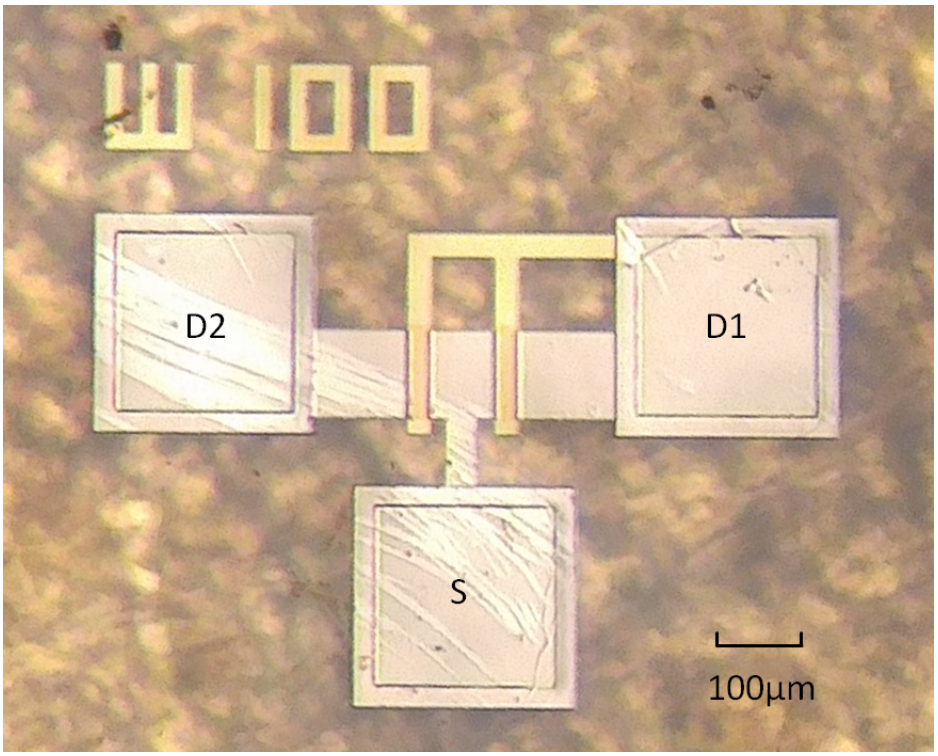
Fig. 4.15 Schematic of the fabricated ISO current mirror.

The circuit schematic is illustrated in Fig. 4.15. Assuming a perfect match between the two transistors, the drain current of T_2 (I_{DS2}) would copy the current that flows through the drain of T_1 (I_{DS1}). However, mismatch can happen due to the variance of material properties and dimensions in the fabrication process. Therefore, we designed two different layout for the current mirror. The first one is based on two separate devices which is shown in Fig. 4.16a. As the two devices are located separately, device mismatch would totally be reflected on the output current.

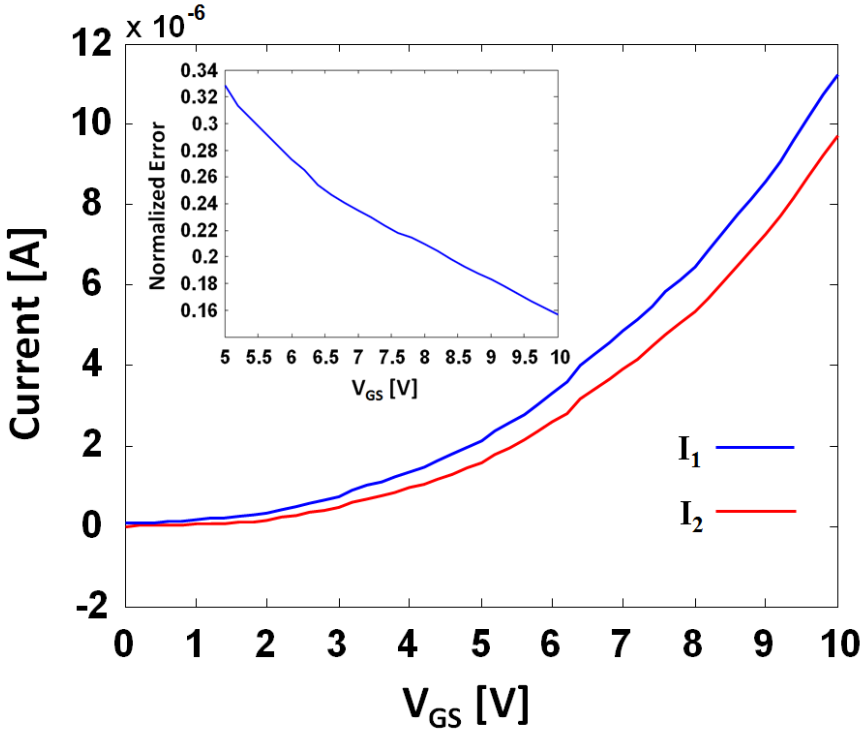
The current mirror with separate device layout is measured sweeping the voltage supply at the drain of T_1 ($V_{DS1} = V_{GS}$) where the drain voltage of T_2 (V_{DS2}) is kept at 10V. The measurement result is illustrated in Fig. 4.16b. As can be seen, the current of the two transistors are rising according to the increase of V_{GS}. However, there is a mismatch in current as I_{DS2} increases slower than I_{DS1}. The normalized current error is between 16% and 32% at a V_{GS} range of 5V to 10V, which is illustrated in the inset of Fig. 4.16b.

The other layout is designed based on the interdigitated stacked layout. The fabricated layout is shown in Fig. 4.17a. The layout effectively separate each device into 5 devices connected in parallel. This would average out mismatches between devices and improve the matching of the overall device. Also, devices are placed adjacent to each other in a interdigitated way to reduce the mismatch over long distance.

The same measurement is done for a current mirror using the interdigitated stacked layout. The measurement result is illustrated in Fig. 4.17b where V_{DS2} is maintained at 10V. As can be seen, the matching of the transistors is significantly improved. The normalized current error has been reduced to below 8% at the V_{GS} range of 5 to 10V. This indicates that the

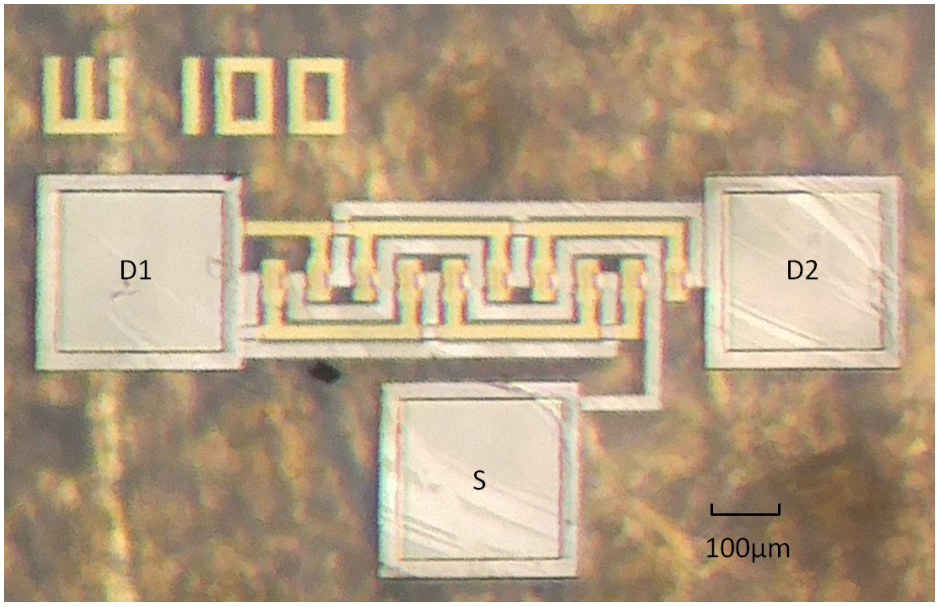


(a) Fabricated current mirror under microscope

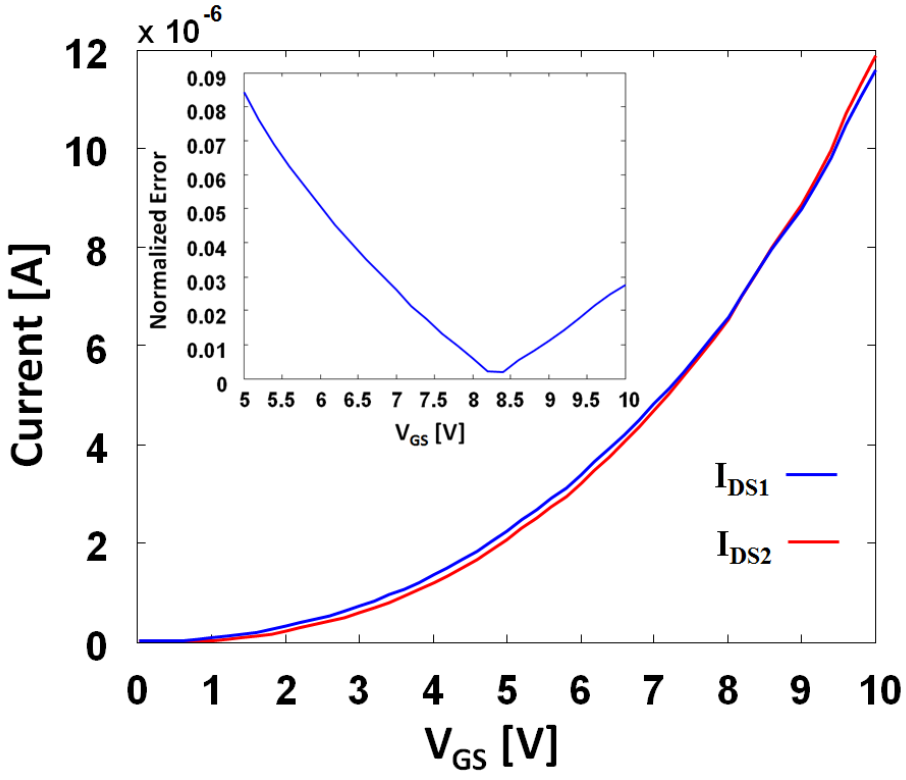


(b) Measurement of the fabricated current mirror

Fig. 4.16 Picture and measurement result of the fabricated current mirror based on a separate-device layout.



(a) Fabricated current mirror under microscope



(b) Measurement of the fabricated current mirror

Fig. 4.17 Picture and measurement result of the fabricated current mirror based on a interdigitated stacked layout.

layout technique used in silicon CMOS technology can be adapted to the vacuum processed TFTs.

Due to the large mismatch (20%) of separate devices, to fabricate a circuit based on dimension ratios reported in this chapter is very difficult without a specific layout design. It maybe beneficial to fabricate every device in a multi-finger layout. However, here we consider the full layout design as a future extension of this dissertation.

4.6 Summary and Discussion

Op-amp is a fundamental building block for any analogue systems. This chapter delves into the fully n-type circuits with a goal of building a bridge between the underdeveloped fully n-type TFT circuits and the well developed CMOS circuits. The result here is fruitful. With the pseudo p-type current mirror, many CMOS design can be converted to fully n-type designs with comparable performances. The V_T independent feature of most building blocks here also simplifies the V_T shift compensation procedure where a clock based compensation system is not needed.

One noticeable drawback of the pseudo p-type mirror is that the output range is rather limited compared with the PMOS counterpart. An external reference voltage supply may be needed in the case when a very wide output range is required. A dynamic reference could also be designed if another circuit block is added to generate a dynamic V_{ref}. In terms of power consumption, the feedback unit adds two more current path which consumes extra power. Designers should reduce the size of the TFTs used in this block to minimize the current and hence minimize the power consumption.

The op-amp designed here is a simple version to demonstrate the functionality of all the building blocks. More stages maybe needed depending on the requirement of applications. The high gain of the differential stage would effectively reduce the input referred noise making the existing blocks promising in all kinds of potential applications. The most outstanding issue remains here is the rail-to-rail output stage. As in this aspect integrated op-amps mostly benefit from the push-pull architecture which is enabled by complementary devices, design an output stage with similar performance remains a challenging topic with fully n-type devices.

Although the design reported in this chapter are all based on n-type devices, they are also usable in fully p-type designs for example in OTFTs due to the symmetrical nature of the two types of devices.

The fabrication of the circuit would need a lot of tuning of the layout and models regarding the variation of parameters. Here, due to the mismatch and especially the difficulty

of controlling the value of V_T, the full circuit fabrication is considered as a future extension of the research reported in this thesis. We have shown a current mirror stage to illustrate that 20% error is likely to happen between any two separate TFTs on the same substrate. Although the matching can be improved to some extent using layout techniques, special layout is needed for the dimension ratio based circuit designs. Therefore, extensive work is necessary to achieve a reliable circuit performance.

Chapter 5

Conclusion and Future Work

With the ultimate goal of creating circuits and systems with more functionality, this dissertation has presented the whole process of designing circuits with IGZO TFTs starting with accurate DC and AC modelling all the way to circuit designs taking into account the interaction between specific device performances and corresponding alternation of designs.

Physical and empirical models of IGZO TFTs have been successfully implemented in the Cadence simulation environment with good smoothness and convergence for fast circuit simulation.

A more precise small signal model for TFTs has been developed taken into account the non-idealities of TFTs. The proposed model is tested on IGZO TFTs and is potentially able to work for TFTs from other material families. Because the effects being considered generally exist in most material families due to the amorphous nature of semiconductors used in TFTs, although the underlying physics can be different. The proposed model yields much better accuracy in comparison with widely adapted CMOS small signal model.

Further, we discussed in a general way how TFT performance could affect circuit design from a device-circuit interaction stand point. Geometric and temperature dependence of TFT current accuracy are characterised through measurement, statistics and modelling. Techniques for extraction of defects and ageing in devices using closed-loop feedback are discussed with their possible extension to other applications.

Finally, fundamental building blocks including voltage and current reference circuits, pseudo p-type current mirror and differential gain stages are designed using n-type IGZO TFTs and simulated through the model developed in this dissertation. The op-amp designed with the aforementioned building blocks are presented for further application-orientated engineering.

As the dissertation mainly contributes to the device modelling, simulation and mono-type TFT circuit design, several extensions could be done in the future.

1. On device modelling, one noticeable improvement could be adding the V_T shift model. This is particularly difficult because the simulation environment would expect a device performance to be stable especially in AC simulations. More importantly, further study should be done physically and mathematically on the time-dependent (or real time) V_T model. Although we have mentioned in several chapters the stretched exponential function of the V_T shift, the function has fundamental flaws in circuit simulations due to the untraceable initial conditions. For example, if we switch on and off a transistor several times, all the parameters in the stretched exponential function (i.e. β and τ) would and should change. However, modelling β and τ based on switching events is very difficult if not impossible. Preliminary work along the line have been reported [**?**], although there is room for refinement if thermodynamic considerations are brought into the picture.

2. Several other circuit building blocks could be designed to expand the library of analogue building blocks. One of which is a rail-to-rail output stage. As class AB amplifier needs complementary devices to work, it will be meaningful to achieve a similar performance with mono-type TFTs.

3. The temperature dependence of circuit blocks was not compensated in the designs presented. Therefore, another meaningful improvement is to design a temperature independent circuit, in particular, a temperature independent reference circuit.

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Appendix A

Device Circuit Interaction

A.1 Importance of DCI in TFTs

Although the ever-evolving TFT technology continues to produce devices with improved performance, such as higher mobility, steeper subthreshold slope and lower V_T [**? ? ? ? ? ? ? ? ?**], circuit implementation is still somewhat constrained. This applies for most of the material families including metal-oxides, organics, and amorphous silicon (a-Si:H) although much less so with low temperature poly-silicon (LTPS). Here, a key design consideration is the device-circuit interaction (DCI), which has to be accounted for when circuits are designed with devices of poor performance and high degree of non-ideality [**? ? ? ? ? ? ? ? ? ?**] as compared to the CMOS counterpart. This is particularly true when the intrinsic performance of TFTs does not the meet the requirements of a desired application. As shown in Fig. A.1, if the performance of the desired application is much lower than the maximum achievable intrinsic performance of the TFT, it is then possible to design the circuit independently without considering device non-idealities. For example, when the error in the TFT's output current created by V_T shift is much lower than the required accuracy, the V_T shift problem is not of concern. However, when the performance requirement needs to be higher than the intrinsic performance, the designer should seek a compensation solution based on DCI or wait for improvements in the technology. We will discuss the intrinsic performance of TFTs in Section A.2 along with compensation methods in Section A.3.

Another aspect of DCI stems from the material and processing attributes of the TFT which usually come with specific, and often self-limiting, properties. For example, in analogue front-end and digital designs, alternative circuit architectures are needed to match the properties of the CMOS counterpart [**? ? ? ? ?**]. This will be discussed in Section A.4 along with solutions to deal with, for example, light-induced non-ideality in oxide TFTs.

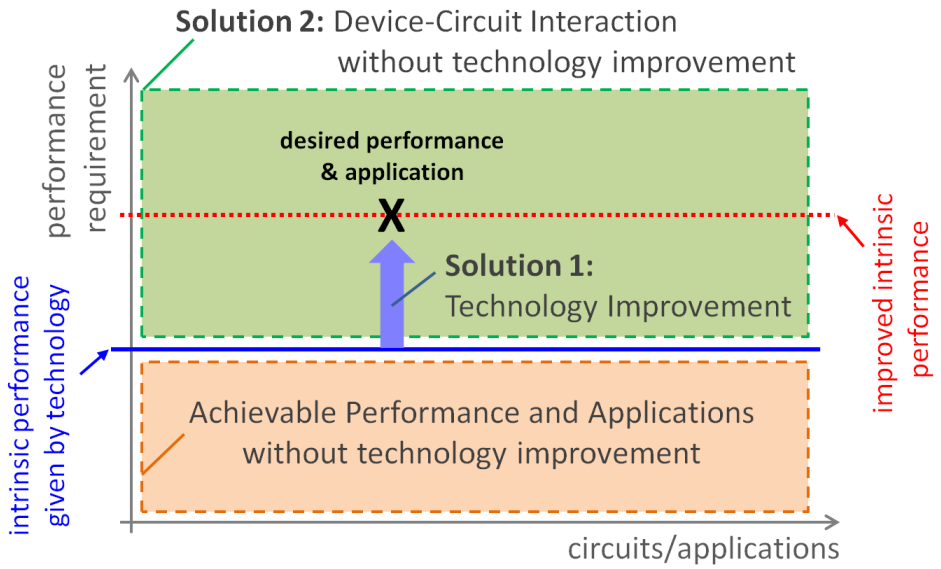


Fig. A.1 Illustration of DCI in relation to performance requirements of a desired application

A.2 Impact of TFT Properties

The TFT is the major building blocks of active thin film circuits and its properties determine circuit performance. In applications such as displays and analogue front-end circuits, the accuracy of the output signal strongly affects the quality of the displayed image without mura (luminance non-uniformity) or in processing analogue signal without significant error. The critical parameters for TFTs (e.g. mobility, C_{ox}, V_T, etc.) determine the performance of the circuit and are more often discussed when comparing TFT behaviour or modelling a single transistor's terminal characteristics [**? ? ? ? ? ? ? ?**]. However, other issues such as stability, temperature sensitivity and process variations can also limit the overall performance and may even affect the functionality of the circuit. There has been significant effort devoted to the study and modelling of bias induced V_T-shift [**? ? ?**] and V_T-shift compensation in AMOLED pixel circuits [**? ? ? ?**]. We will analyse the sensitivity of drain current on V_T-stability and temperature and process variations with the aim of establishing guidelines on the level of accuracy that can be achieved without applying compensation methods (i.e. the intrinsic performance) as well as identify the parameters that contribute most to error and how this can be improved with processing.

A.2.1 Temperature Dependence

The parameters of the TFT are affected by material properties and on temperature, which in turn impacts the terminal current-voltage (I-V) behaviour. According to the I-V model of the

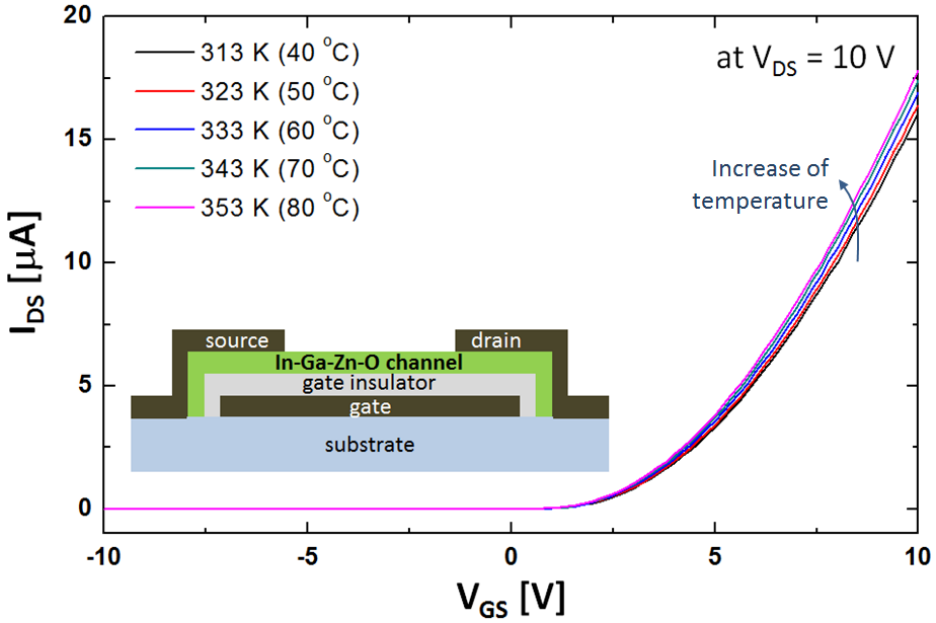


Fig. A.2 I-V characteristics of the examined TFT under different temperatures

TFT:

$$I_{DS} \approx \frac{1}{2+\alpha_p} \frac{\mu_0^*}{Q_{ref}^{\alpha_p - 1}} \frac{W}{L'} C_{ox}^{\alpha_p} (V_{GS} - V_T)^{\alpha_p + 1} \equiv K \times (V_{GS} - V_T)^{\alpha_p + 1} \tag{A.1}$$

where,

$$K \equiv \frac{1}{2+\alpha_p} \frac{\mu_0^*}{Q_{ref}^{\alpha_p}} \frac{W}{L'} C_{ox}^{\alpha_p} \tag{A.2}$$

The variations here can be specified as the variation of three key parameters: K, V_T and α_p. By considering these parameters as functions of temperature, the derivative of I_{DS} as a function of temperature can be expressed as follows:

$$\begin{aligned} \mathrm{d}I_{DS}(T) = {} & (V_{GS} - V_T)^{\alpha_p + 1} \frac{\partial K}{\partial T} \mathrm{d}T \\ & - K(\alpha_p + 1)(V_{GS} - V_T)^{\alpha_p} \frac{\partial V_T}{\partial T} \mathrm{d}T \\ & + K ln(V_{GS} - V_T)(V_{GS} - V_T)^{\alpha_p + 1} \frac{\partial \alpha_p}{\partial T} \mathrm{d}T \end{aligned} \tag{A.3}$$

Therefore the temperature sensitivity of the overall current can be separated into three parts, in which each part of the function is determined by the temperature sensitivity of K, V_T or α_p. The contribution of each parameter can then be calculated through extraction of the temperature sensitivity of the three parameters.

Consider the transfer characteristic for an indium-gallium-zinc-oxide (IGZO) TFT, measured every 10°C from 40°C to 80°C, shown in Fig. A.2. The results show that the overall current would increase when temperature increases. To further investigate the degree of influence of the three parameters, their values have been extracted from the measured transfer characteristics according to Eq. (A.1). Here, we extract the threshold voltage (V_T) independently from a multi-derivative method [**?**], and then use it to calibrate the gate voltage as $V_{GS}-V_T$. With this, I-V data is plotted in log-log plot. In this plot, all the data turns into a linear behaviour, where the intercept on the y-axis, $log(I_{DS})$, is $log(K)$, with slope α_p. From this, we will get K and α_p independently. The results are shown in Fig. A.3. As can be seen, all three parameters are approximately linearly related to 1/kT in the temperature range considered.

Therefore, through a linear fitting of the parameters, we get the empirical models of the parameters with the following relations:

$$\alpha_p(T) = \alpha_0 + \frac{E_\alpha}{kT} \tag{A.4}$$

$$K(T) = K_0 exp\left(-\frac{E_K}{kT}\right) \tag{A.5}$$

$$V_T(T) = V_{T_0} exp\left(-\frac{E_{VT}}{kT}\right) \tag{A.6}$$

Combining Eq. (A.4) (A.5) (A.6) and (A.3), the current sensitivity can be derived as:

$$\begin{aligned}\frac{\mathrm{d}I_{DS}(T)}{\mathrm{d}T} &= (V_{GS}-V_T)^{\alpha_p+1} K_0 \frac{E_K}{kT^2} exp\left(-\frac{E_K}{kT}\right) \\ &- K(\alpha_p+1)(V_{GS}-V_T)^{\alpha_p} V_{T_0} \frac{E_{VT}}{kT^2} exp\left(-\frac{E_{VT}}{kT}\right) \\ &- Kln(V_{GS}-V_T)(V_{GS}-V_T)^{\alpha_p+1} \frac{E_\alpha}{kT^2}\end{aligned} \tag{A.7}$$

Note that the three terms at the RHS of Eq. (A.7) define the contribution of K, V_T and α_p, respectively.

To understand how much the overall current is affected by ambient temperature and the associated contribution of the different parameters, the normalized temperature sensitivity is shown in Fig. A.4. As can be seen, the overall temperature sensitivity drops with increase in V_{GS} due to the fact that the contribution of V_T drops while V_{GS} increases. This tendency starts to saturate when V_{GS} increases to 4V, when the contribution of K becomes dominant. This analysis suggests that TFTs can be very unstable when biased at a voltage near V_T. Although higher stability can be achieved through intentionally biasing the transistor at higher voltage

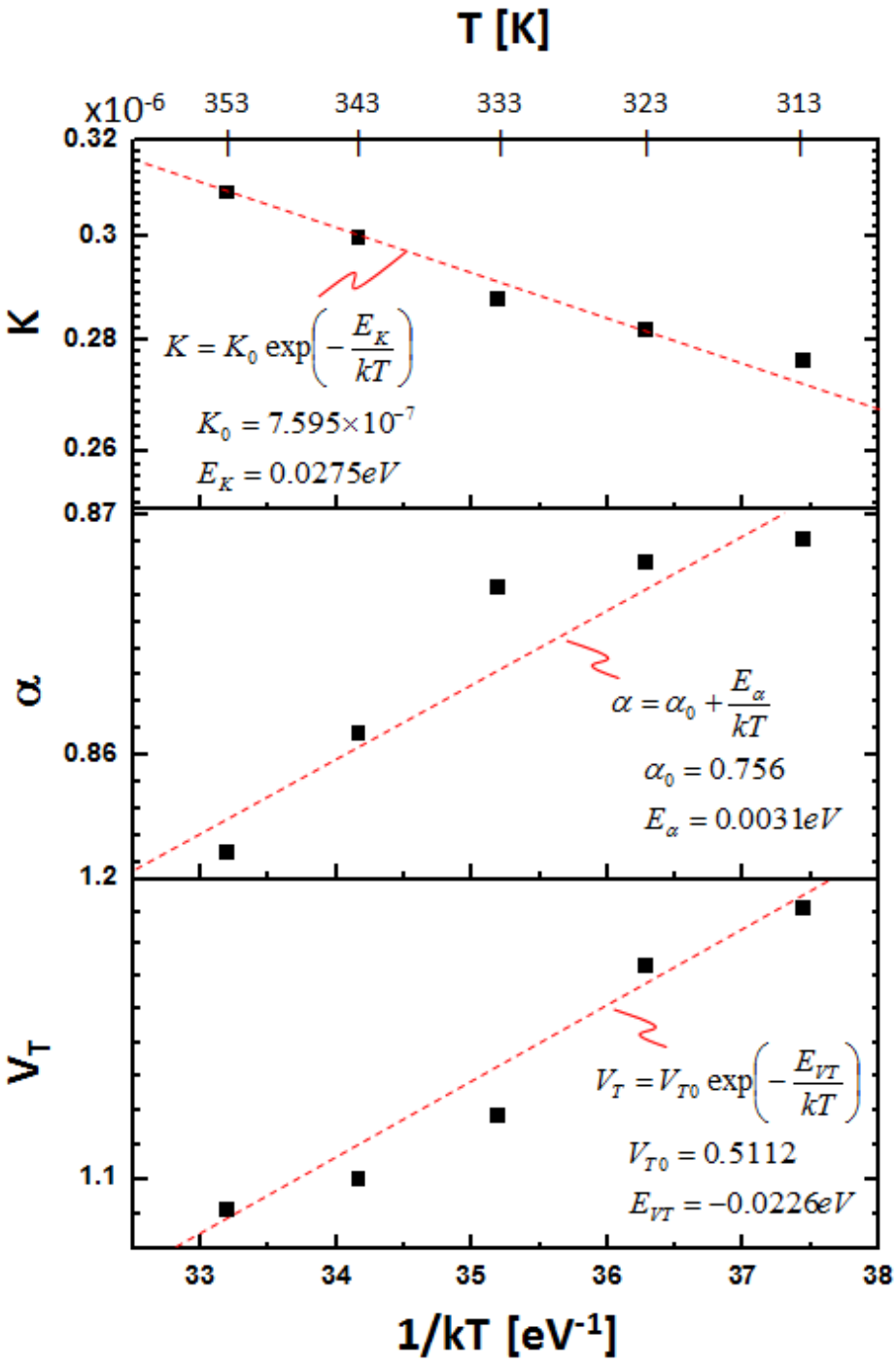


Fig. A.3 Extracted values of K, α_p and V_T at the different temperatures

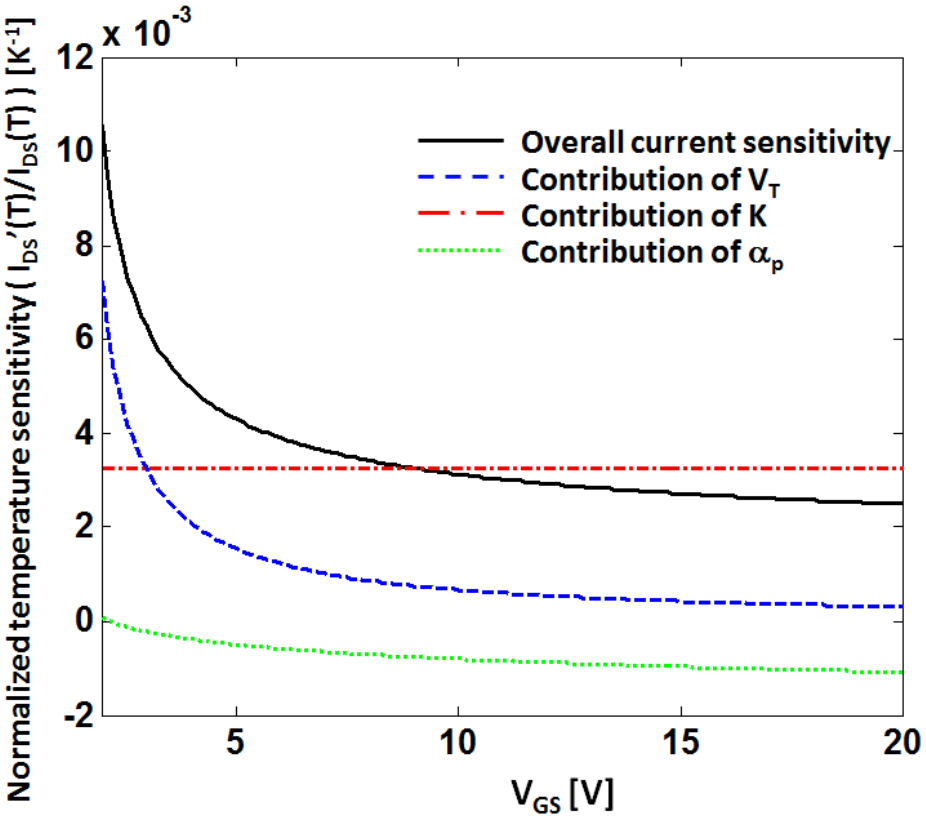


Fig. A.4 Normalized temperature sensitivity of current and the contribution of different parameters at 313K

levels, the maximum achievable level will be determined by the temperature sensitivity of K. As the temperature dependence of α_p has a negative contribution to current with respect to temperature and its contribution increases at higher bias, the temperature dependence of K can be compensated by α_p resulting in decreased sensitivity. However, a higher bias level implies increased power consumption of the circuit. Therefore, an appropriate bias point should be chosen for enough stability with acceptable power consumption.

A.2.2 Geometric Dependence

Apart from time- or temperature-dependent variations in device parameters, processing-induced spatial variations should be considered especially in pixelated arrays or analogue circuit applications. These variations would cause pixel non-uniformity in displays or imagers and create error or undesired behaviour in analogue circuit design. Note that the non-uniformity can be global (i.e. between panels) or local (i.e. between transistors). The latter is harder to deal with especially when transistor matching is of concern (such as in

differential pairs or current mirrors). This chapter will focus on the local non-uniformity and discuss the contribution of different parameters in creating the current mismatch.

Analysis of geometric dependence can follow a similar route as with temperature dependence. As different parameters would follow a certain probability distribution, the overall current will be determined by the randomness of all three parameters according to Eq. (A.1). As variations are usually smaller than the respective mean values, the mismatch in I_{DS} can be expressed as a first order approximation:

$$\begin{aligned}\Delta I_{DS} = &(V_{GS}-V_{T0})^{\alpha_{p0}+1}\Delta K \\ &- K_0(\alpha_{p0}+1)(V_{GS}-V_{T0})^{\alpha_{p0}}\Delta V_T \\ &+ K_0 ln(V_{GS}-V_{T0})(V_{GS}-V_{T0})^{\alpha_{p0}+1}\Delta\alpha_p\end{aligned} \tag{A.8}$$

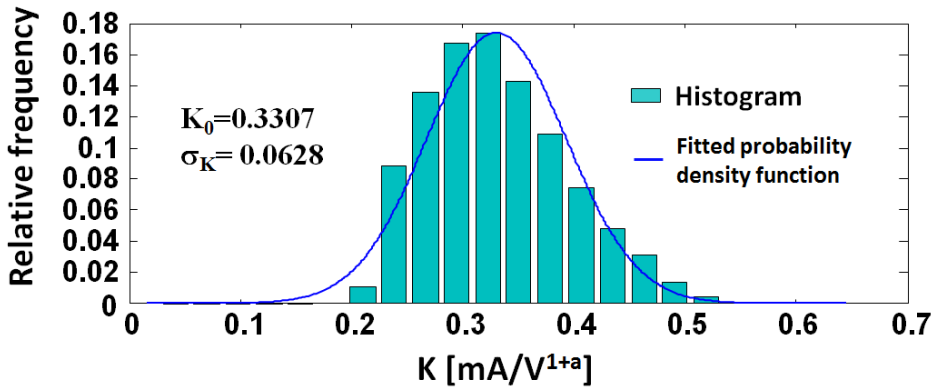
Here, K_0, V_{T0} and α_{p0} are the mean values of the parameters, and ΔK, ΔV_T and $\Delta\alpha_p$ their respective variations. Assuming K, α_p and V_T are independent variables and that all follow a normal distribution, the variance of I_{DS} can be expressed as:

$$\begin{aligned}\sigma^2_{I_{DS}} = &(V_{GS}-V_{T0})^{2(\alpha_{p0}+1)}\sigma^2_K \\ &+ K_0^2(\alpha_{p0}+1)^2(V_{GS}-V_{T0})^{2\alpha_{p0}}\sigma^2_{V_T} \\ &+ K_0^2[ln(V_{GS}-V_{T0})]^2(V_{GS}-V_{T0})^{2(\alpha_{p0}+1)}\sigma^2_{\alpha_p}\end{aligned} \tag{A.9}$$

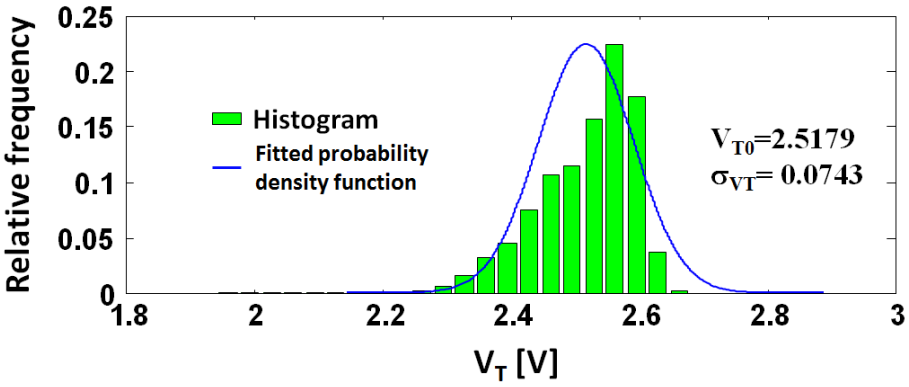
where σ_K, σ_{V_T} and σ_{α_p} are the standard deviation of K, α_p and V_T, respectively. As expected, the standard deviation of the overall current is determined by the deviation of all three parameters.

To analyze the variation sensitivity of the overall current, we need statistical data for all three parameters. Here, we acquired statistical data of the transfer characteristics by measuring a 1080×1920 RGBW OLED display panel. By using the pixel circuit described in [**?**], which will be reviewed in the next section, we could extract the I-V characteristics of the driver TFTs within the panel and extract statistical data for the three parameters. Here, the TFTs for driving the green OLED pixels are used as shown in Fig. A.5. The probability density functions are fitted to a normal distribution using MATLAB. With the fitted mean values and standard deviations, we calculate the relative contributions of each parameter to the current variance using Eq. (A.9).

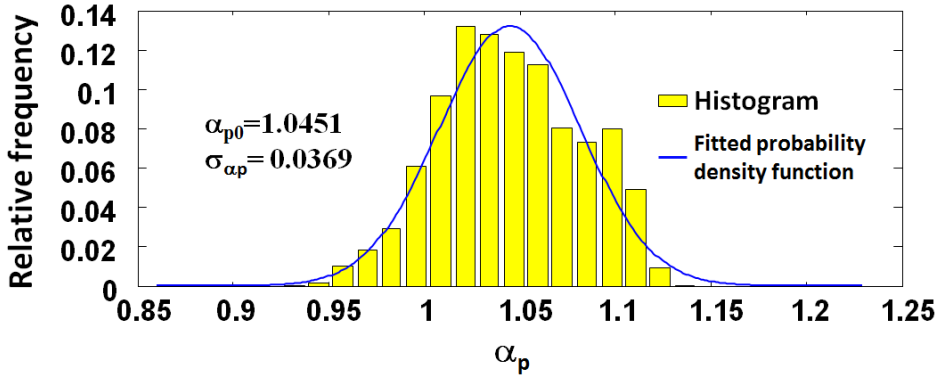
The standard deviation of I_{DS} and the contribution of each parameter are shown in Fig. A.6. We see a similar overall curve in the sense that the sensitivity is higher when biased near V_T. However, unlike the temperature dependence where sensitivity drops with increasing bias, the dependence on geometric shows a minimum at around V_{GS}=6V. This is due to the decreasing contribution of V_T and the increasing contribution of α_p. Therefore,



(a) Fitted probability distribution and histogram of K



(b) Fitted probability distribution and histogram of V_T



(c) Fitted probability distribution and histogram of α_p

Fig. A.5 Fitted probability distribution and histogram of the three key parameters. The data was extracted at room temperature from a 1080*1920 RGBW AMOLED panel with pixel circuits as described in Fig. A.7.

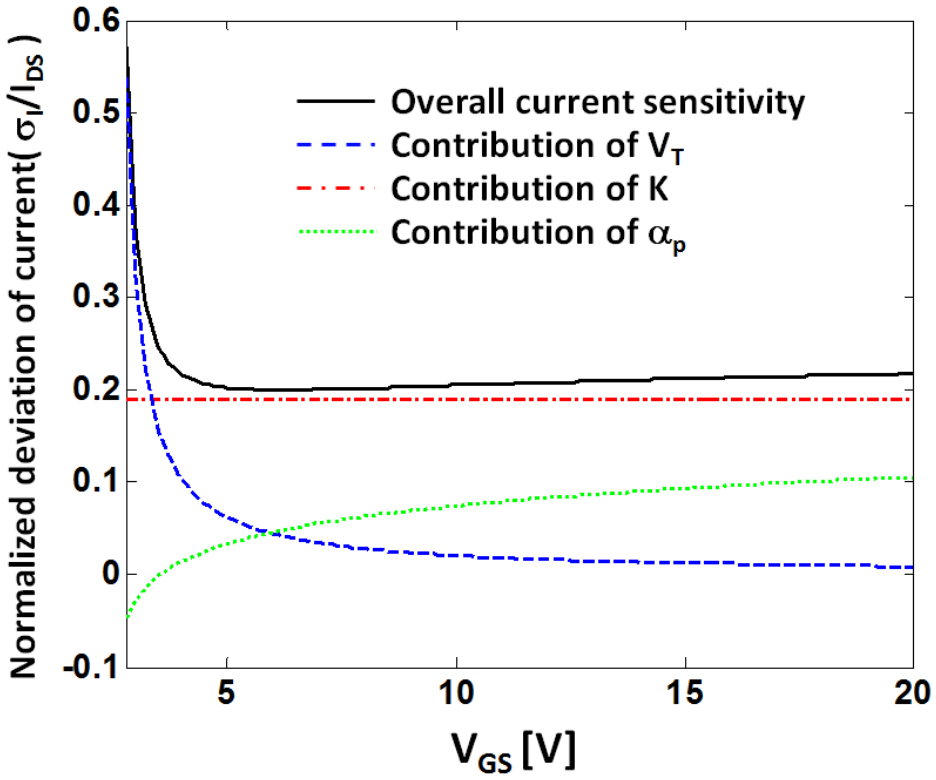


Fig. A.6 Normalized standard deviation of current and the contribution of different parameters(K, V_T and α)

analogue designers can intentionally choose a bias point close to the minimum point for the output transistor, when designing circuits to reduce the output current sensitivity to process variations.

The analysis of temperature and geometric dependence here is done using a generic approach since the current-voltage behaviour is estimated by three key parameters, namely K, V_T and α_p. This is adaptable to most TFT types because of the similar working principle albeit with different parameter values. Therefore, the methodologies and derivations presented here are generic and empirically approached for applicability to other material families including OTFTs and related material families.

A.3 Compensation Methods in Circuits & Applications

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The intrinsic performance of TFTs does not always meet the requirements of specific applications. For example, the threshold voltage shift in TFTs creates visible shadows or ghosting in displays or imagers after extended operation. The resulting non-uniformity

creates mismatch in output characteristics especially in matrix architectures (displays or sensors). These kinds of defects have proven difficult to improve by processing, and thus need to be compensated through circuit solutions. Here, we will discuss V_T shift and non-uniformity compensation methods such as on-pixel programming and by off-pixel feedback. The compensation methods can also be extended to other circuit applications.

A.3.1 On-Pixel Programming

The most common way of compensating TFT defects in active matrix arrays is through on-pixel compensation. The methods were first developed for a-Si:H TFTs in AMOLEDs as this family of TFTs have severe V_T shift under positive bias, which leads to big errors when supplying current to the OLED [**?**].

V_T compensation techniques can be categorized into two kinds: current programming [**? ? ? ? ? ? ? ?**] and voltage programming [**? ? ? ? ? ? ? ?**]. The basic working principles of these have been reviewed in [**? ?**]. Recent progress in voltage programming has been reported in [**? ?**]. Here, the working principle is slightly different from the original idea in that the technique does not capture the cut-off point of a diode-connected transistor. Instead, it uses a TFT to discharge a pre-charged capacitor with fixed gate bias in a fixed time period to capture the TFT's property (i.e. V_T). This technique can provide faster V_T extraction and is good particularly when the speed of the circuit is of concern.

A.3.2 Off-Pixel Feedback

Another way of defect compensation is based on off pixel feedback. Since in display applications the driving period of each pixel can be separated into several phases, it is possible to use part of the driving sequence to extract all of the defect and aging data present in the pixel and then drive with revised extracted parameters as feedback [**? ? ? ? ? ? ?**].

A pixel structure for defect extraction reported in [**?**] is shown in Fig. A.7. The pixel circuit shows a similar structure as the simple 2T1C structure – the only difference being addition of a monitor line to monitor the TFT and OLED characteristics and extract their defect and aging status. The driving sequence for this pixel circuit is similar to the 2T1C except for the addition of a defect extraction phase. Defect extraction starts after the SEL signal selects the pixel and before writing data to it. The extraction phase consists of two parts – the driver TFT and the OLED, respectively (shown in Fig. A.8).

Fig. A.8a shows an equivalent circuit of the extraction phase for the OLED. In this phase the gate voltage of the driver TFT is set to ground level to turn it off and the monitor line is set to a higher voltage of V_{OLED}. The current flowing through the OLED can then be

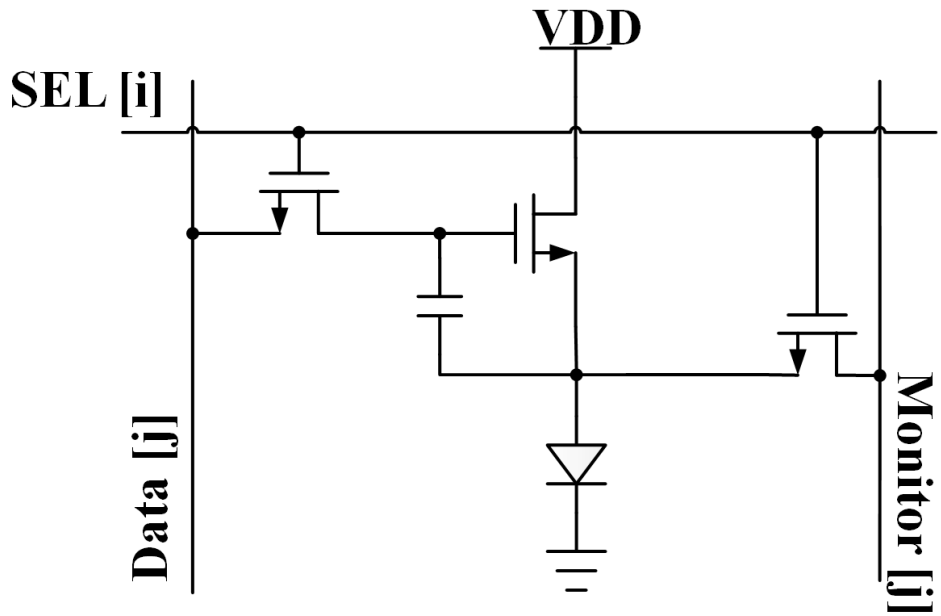


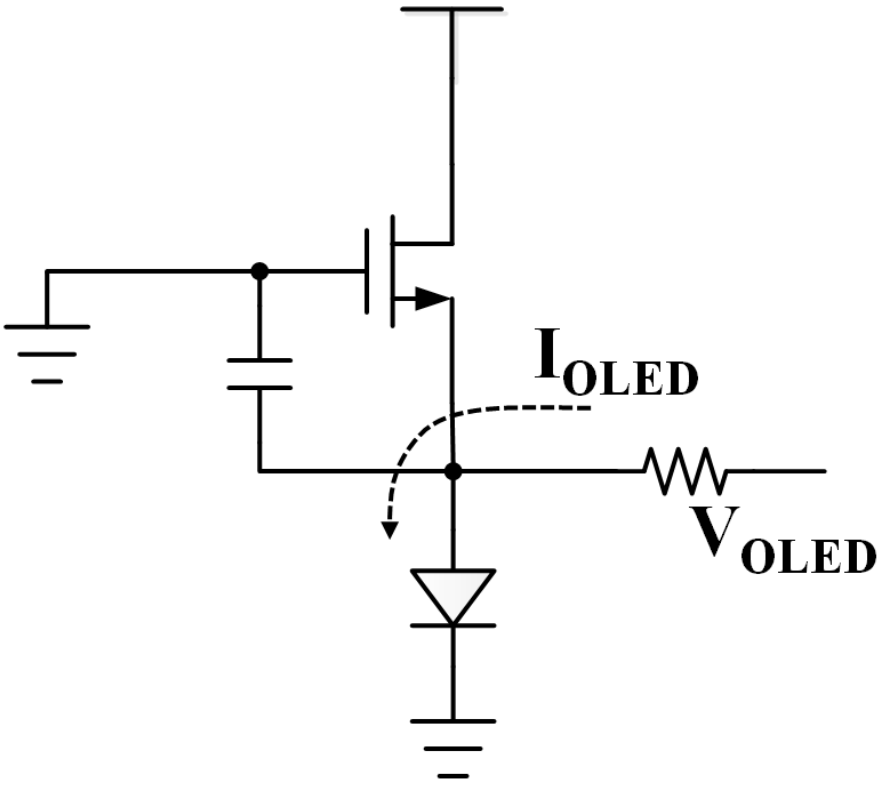
Fig. A.7 AMOLED pixel structure for off-pixel defect extraction and feedback

captured by measuring the current flowing into the monitor line. As the I-V characteristic of the OLED can be a signature of its efficiency, the aging of OLED can then be captured from pre-acquired data for this type of OLED. In Fig. A.8b, the gate voltage of the driver TFT is set to a higher level of V_P. The TFT is then turned on and part of the drain current flows to the monitor line. Combining the extracted I-V characteristic data of the OLED and the voltage and current measurements in this phase, the I-V characteristic of the driver TFT can be extracted.

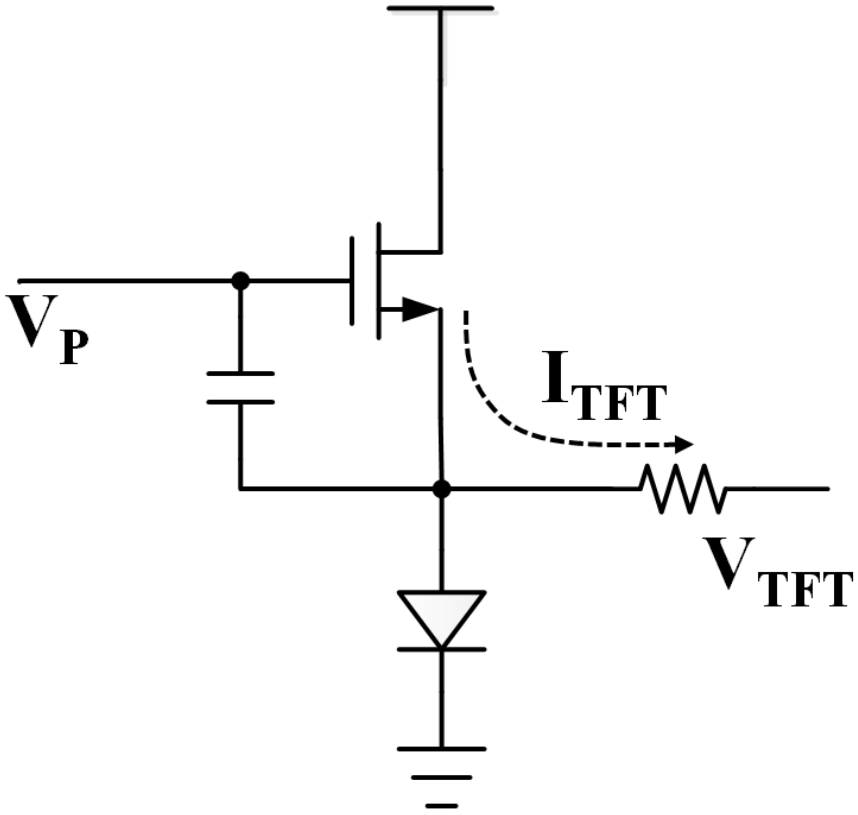
After capturing the defect and aging data for both the driver TFT and OLED, the data voltage for the desired luminance can be calculated and applied to the pixel by external circuitry.

The aging and defect status of TFTs and OLEDs extracted through the monitor lines are shown in Fig. A.9(a) and Fig. A.9(b), respectively. The sharp hazards that happen randomly among the panel show the fabrication defects of the pixels. And the patterns in red, yellow and green colour express the aging of each device. As the center of the displayed white square has higher temperature due to self-heating of the surrounding pixels, the aging of these pixels will be faster compared to other pixels.

The display panel using this method has the ability of compensating all kinds of defects that can be extracted through the monitor line. The compensation results are shown in Fig. A.10 depicting the defect status in Fig. 10(a)&(b) and temperature compensation in Fig. 10(c)&(d).



(a) OLED detection phase



(b) TFT detection phase

Fig. A.8 Equivalent circuit for the defect extraction phase of OLED and TFT

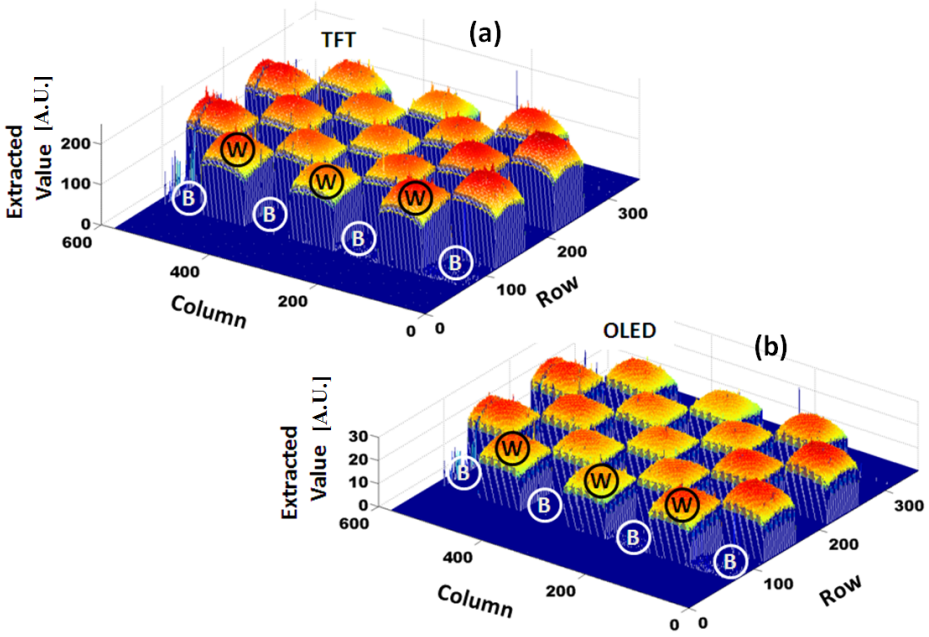


Fig. A.9 Extracted aging parameters for (a) TFTs and (b) OLEDs after continuously displaying a checker board (W: displayed with white squares, B: displayed with black squares)

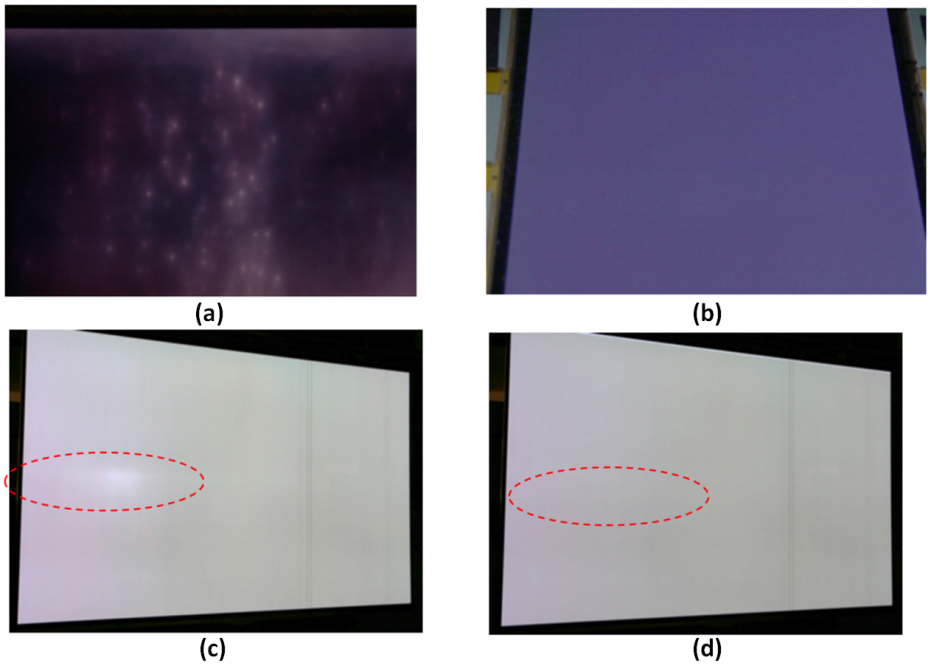


Fig. A.10 Extracted aging parameters for (a) TFTs and (b) OLEDs after continuously displaying a checker board (W: displayed with white squares, B: displayed with black squares)

This method provides a generic solution for TFT compensation and will be particularly useful in compensation of mechanically-induced (reversible) defects or aging in flexible displays. As measurement of the TFTs can be done in a monitoring phase, the obtained parameters can then be used to bias the TFTs to have an ideal overall performance. The geometric dependence of transistors can also be extracted from this pixel, as during the sequence described in Fig. A.8a & A.8b one can also apply voltage sweep to obtain the measured I-V characteristics for both TFT and OLED devices.

In summary, defects of TFTs can be compensated through separating the working sequence into several phases and by adding a compensation phase to extract and compensate non-idealities. To apply this method to other analogue circuits, it is possible to intentionally separate the working sequence and apply similar methods. Here, switch-capacitor circuits can be a promising candidate. An example of this applied to analogue building blocks was reported in [**?**].

A.4 Specific Device Properties and Alternate Circuit Architecture

Devices processed using different thin film technologies usually have a specific property, which can sometimes be self-limiting. This requires the use of alternate circuit architectures. For example, most TFT technologies lack complementarity, thus the circuits have to be designed using mono-type devices, which means the designs cannot benefit from the well-established CMOS architectures. Specifically, the load of an analogue amplifier needs to be redesigned to achieve high gain as the complementary load is not applicable. Another example is persistence photoconductivity in oxide TFTs, which, while ideal for image capture, requires a sharp gate a pulse to reset for high frame rates. We will discuss these examples in the following.

A.4.1 Analogue Gain Stage with Mono-type TFTs

CMOS gain stages benefit from the complementary structure [**? ? ?**]. For example, in the case of NMOS as the input stage and PMOS as the load, the gain of the stage can be boost up to the order of magnitude of $g_m r_o$. The use of PMOS load provides large enough bias current with small voltage and, at the same time, big small signal resistance. These requirements are hard to be achieved with only one type of transistors.

To simplify the problem, we consider a single common source amplifier stage as shown in Fig. A.11(a). Here, the load is considered as a two terminal device. Assuming the bias

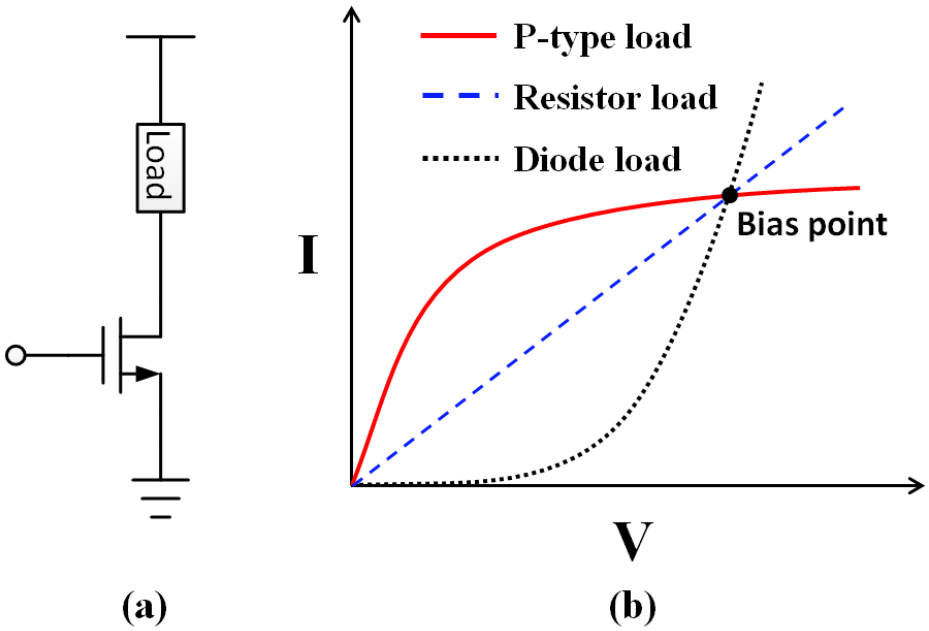


Fig. A.11 (a) Common-source gain stage of an amplifier (b) sketch of different type of loads passing through the same bias point

conditions of the driver TFT is fixed (to maintain gm for fair comparison between different loads), the load of this gain stage would have fixed bias current. Here, we consider a fixed bias point of the load for comparison, i.e. the I-V characteristic of the load should pass a fixed point in the I-V plot (Fig. A.11(b)). As the gain stage needs a higher small signal resistance of the load to produce high gain (i.e. derivative at the bias point should be close to zero), the current is better a concave function of voltage which means p-type load is more beneficial. Note that for other type of loads, the same small signal resistance can only be achieved by moving the bias point to the right hand side, i.e. increase the voltage bias of the load. However, a higher voltage bias would yield higher power consumption. From this standpoint, we conclude that for high gain, a p-type load with fixed gate bias (concave function) is more beneficial than a resistive load (linear function) and, subsequently, a diode or diode-connected TFT load (convex function) as it yields higher gain at the same power consumption.

The most familiar concave function in TFT behaviours is the output characteristic ($I_D - V_{DS}$ characteristic with fixed V_{GS}). However, the design is limited by the connection of n-type devices as the source terminal of the load TFT is connected to the output node of the gain stage. Thus, the gate terminal of the TFT cannot be chosen as a fixed level but should follow the change of the source terminal.

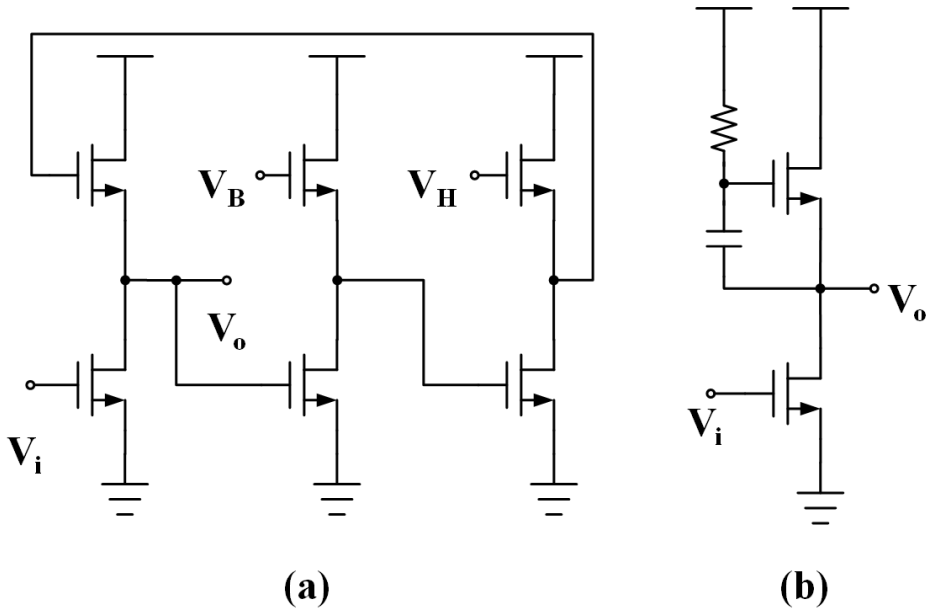


Fig. A.12 Gain stage of an amplifier with (a) feedback load (b) boost strap load

One straight forward solution is to use a depletion mode load and short circuit the load transistor's source and gate terminals. (Depletion mode transistor can work in saturation regime with zero V_{GS}.) Amplifiers have been designed around 1980s to achieve high gain with depletion and enhancement NMOS transistors [**? ? ?**]. However, in TFT circuit area, this approach is limited by process complexity. By far, only digital circuits have been fabricated out of depletion load [**? ? ?**].

In order to use only enhancement mode TFTs while still obtaining high enough gain, it is also possible to use feedback loop to maintain a fixed V_{GS} for high small signal resistance of the load. One approach is reported in [**? ?**]. The circuit reported is shown in Fig. A.12(a). Here, an analogue adder is designed for the DC bias of the load transistor. The feedback circuit, in effect, adds a bias voltage to the source terminal of the load transistor and applies the resulting voltage to the gate terminal. Here, the feedback voltage at the gate terminal of the load TFT can be calculated as:

$$V_F = V_H - V_B + V_O \tag{A.10}$$

Here, V_H and V_B are external bias voltages and V_O is the output of the gain stage (which is also the source terminal voltage of load). As the feedback voltage contains the output, this topology has a positive feedback.

Another approach using positive feedback has been reported by H.Marien et al [**?**]. The load of their gain stage is designed with boost strap structure. Other than maintaining the

V_{GS} level of the load TFT, the structure successfully separates the DC bias and the small signal resistance and as a result obtains a higher gain for small signals at a higher frequency. The circuit needs a large capacitor for the load (a high pass filter) to reduce its lower $3dB$ frequency close to DC range. This also makes the circuit hard to work at very low frequencies, especially when the original signal is close to DC. An NMOS version of the circuit has been shown in Fig. A.12(b). Other approaches regarding positive feedback are also reported in [**?**].

To summarize, positive feedback is used for gain-enhancement in single type TFT amplifiers. The major problem of this kind of approach is that positive feedback sacrifices the phase margin (PM) of the amplifier and would potentially cause instability. Although a cascode technique can be chosen to enhance the gain without sacrificing PM, it is not preferred in TFTs since a much higher supply voltage is needed because of the high threshold voltage of TFTs.

A.4.2 Persistent Photoconductivity

This can arise depending on the channel composition in oxide transistors when the transistor is under exposure to ambient light or when subject to negative bias illumination stress (NBIS) [**?**][21]. As the drain current of the TFT increases after exposure to ambient light, it is possible to use this characteristic for photo-sensing applications. In this application, the variation of current is not a defect that needs to be compensated. However, to use this property, the slow recovery process makes it hard to capture the changing image at high frame rate or to restore the TFT's initial state. Fig. A.13(a) depicts the drain current of an IGZO TFT under periodic luminance and darkness. The results show the drain current recovering only slowly even in a completely dark environment.

In order to remove the persistent photoconductivity and recover the TFT to its original state, it has been found that by applying a positive pulse to the gate of the TFT, the PPC can be eliminated very quickly. The results in Fig. A.13(b) show that fast PPC removal is possible after the gate pulse technique.

The phenomenon of PPC is explained by the band diagram shown in Fig. A.14. As the ambient light excites the electrons in defect states to the conduction band, ionized oxygen defects are created. The excited electrons effectively increase the conductivity of the device as the electron concentration is increased. In order to accelerate the recovery process, the recombination of photo-induced electrons and ionized oxygen defects $V_{O^{2+}}$ needs to be accelerated. By applying a positive voltage pulse to the gate of the transistor, the electrons are swept away from the conduction band to recombine with the ionized oxygen defects thus removing the PPC.

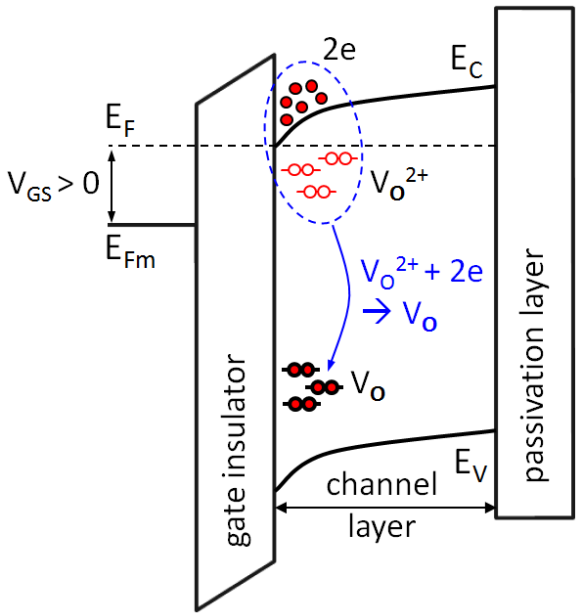
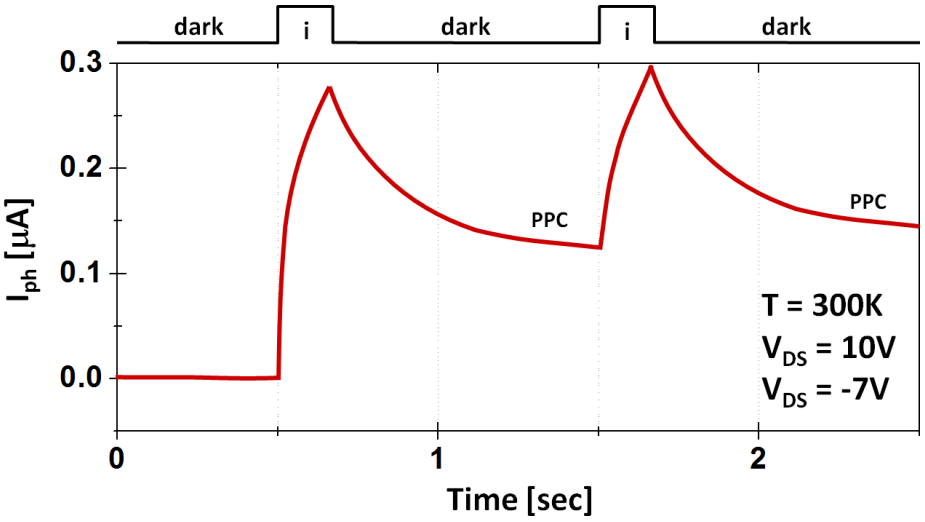


Fig. A.13 Band diagram to explain the effect of positive gate pulse on recovery.

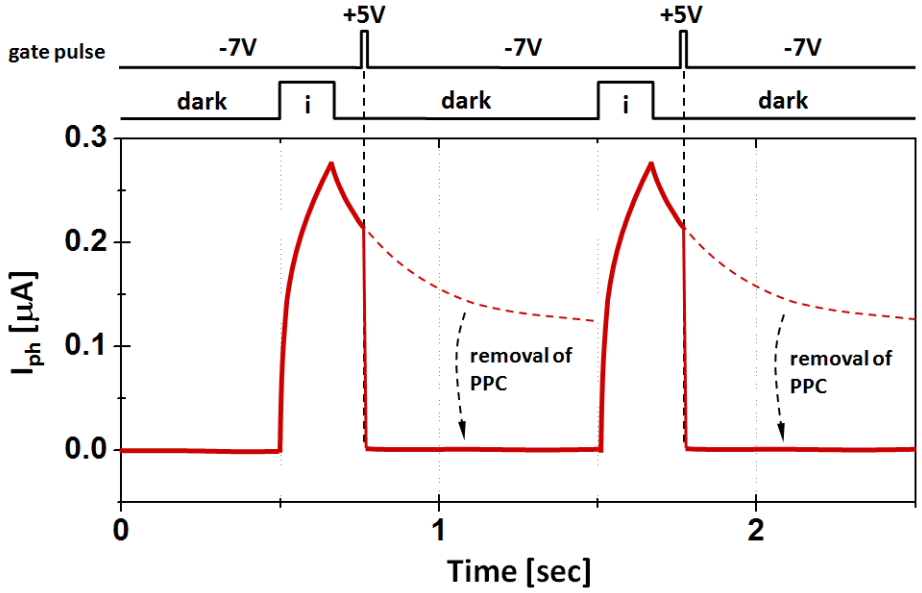
PPC removal is a great example of device circuit interaction as the defect (i.e. light induced instability) of a TFT can actually be utilized to sense luminance signal, i.e. as a photo sensor. Indeed DCI should be considered not only to enhance circuit performance and/or overcome difficulties in the design but also to utilize specific properties stemming from the operating environment.

A.5 Conclusion

This chapter reviewed and analysed the intrinsic parameters of TFTs and proposed ways of analysing the maximum achievable current accuracy of TFTs and to help determine when compensation becomes mandatory to enhance reliability and combat ageing. We presented techniques for extraction of defects and aging in devices using closed-loop feedback techniques and discussed their extension to other applications. In summary, device circuit interactions are crucial when designing high performance circuits and systems to either utilize or minimize the impact of intrinsic adversaties associated with low temperature thin film technology. Consideration of device circuit interactions in design of TFT systems is even more compelling than the case of CMOS technology because of the wide range of materials imperfections, which give rise to device instability and large area processing-induced non-uniformity. Of specific importance to mechanically flexible systems is the impact of bending-induced (reversible) defects and associated aging, which makes compensation



(a) Observation of persistent photoconductivity (PPC) as a slow recovery



(b) Removal of PPC with a positive gate pulse to get fast recovery

Fig. A.14 Persistent photoconductivity (PPC) and its removal

even more compelling. The techniques presented here can extend the current application of TFTs from active matrix pixelated arrays to newly-emerging application area that require TFT operation in analogue operation mode.

Appendix B

Subthreshold Operation for Schottky Barrier TFTs

B.1 Introduction

Recent research has shown that by biasing IGZO TFTs in deep subthreshold region could improve the small signal gain and significantly reduce the power consumption [**?**]. This is specifically useful in low power applications such as sensor networks, bio-medical sensing etc [**? ?**].

While subthreshold operation in Silicon based CMOS devices had been intensively researched in 1970s with great success in Swiss watch industry [**? ? ? ?**], the same has not been done for TFTs.

Due to the low effective carrier mobility of TFTs (perhaps with polysilicon as an exception), TFT devices are generally working in a lower current level [**? ?**]. Although this could limit the speed of the device, TFTs can be naturally suitable for low speed and low power applications. Biasing TFTs in subthreshold region could further reduce the power consumption to sub-nano-watt. This is particularly appealing as battery-less operation could be possible with this level of power consumption. However, as the subthreshold region is generally very narrow and current level is very sensitive to bias [**?**]. If a TFT has a steeper subthreshold slope (SS), a sensitivity of current variation is higher. The circuit design for this kind of devices could be challenging although a steep SS provides a high intrinsic gain. Here, a high intrinsic gain is an important property for circuit design, so many approaches to get it have been introduced for the above-threshold operation [**? ? ? ?**]. For the subthreshold operation, it is known than a TFT with a Schottky contact source/drain have a steeper SS

compared to an Ohmic contact TFT [**?** **?** **?**], thus a Schottky contact TFT provides a higher intrinsic gain within the subthreshold regime with a difficulty in a circuit design.

In this chapter, we will analyze several figures of merit for deep-subthreshold operating TFTs in analog circuit design with the aim of providing a guideline of analog circuits design capability of TFT devices using general architectures.

B.2 Subthreshold Model for IGZO TFTs

B.2.1 DC Model

The transfer curve of SB-TFTs in deep-subthreshold is reported to be linear in log-scale which is similar to CMOS devices. Here we convert the model reported in [**?**] to a more macroscopic form to help analyze the performance. The equation for drain voltage (V_{DS}) > saturation voltage (v_{sat}) is derived as follows [**?** **?**]:

$$I_{ds} = I_0' \exp\left(\frac{V_{GS} - V_T}{SS/\ln 10}\right)\left(1 + \frac{V_{DS}}{V_A}\right) \tag{B.1}$$

where I_0' is the effective subthreshold reference current at V_T normalized by W and SS is the subthreshold slope. V_T is the threshold voltage and V_A is the effective early voltage. The effective values can be derived as

$$I_0' \equiv A_J J_0 \exp\left(\frac{V_T - V_{ref}}{SS/\ln 10}\right) \tag{B.2}$$

where J_0 is the reference current density at V_{ref}, A_J is the junction area of the Schottky contact at the source and drain. In a Schottky contact TFT, A_J is proportional to the channel width (W) [**?**].

$$V_A \equiv n \cdot v_{th} \exp\left(\frac{v_{sat}}{n v_{th}}\right) \tag{B.3}$$

where n is the ideality factor of the junction and v_{th} is the thermal voltage.

With the above equations we can easily connect the DC parameters to several important small signal parameters such as gm and ro.

B.2.2 Small Signal Model

Although in previous publications [17], [18] we analysed the small signal mode for TFTs and figured out that contact resistance can cause big errors using CMOS small signal models,

small signal behaviour in subthreshold region can still be correctly modelled by CMOS model. This is due to the fact that channel capacitance in subthreshold is very small and normally negligible compared with overlap capacitance in TFTs.

Here we consider C_{gs} and C_{gd} are mainly the overlap capacitance at source and drain side [17]. The tranconductance and output resistance can be calculated as:

$$\begin{aligned} g_m &= \frac{\ln 10}{SS} I'_0 \exp\left(\frac{V_{GS}-V_T}{SS/\ln 10}\right)\left(1+\frac{V_{DS}}{V_A}\right) \\ &= \frac{\ln 10}{SS} I_{DS} \end{aligned} \tag{B.4}$$

$$r_o = \frac{I_{DS}}{V_A} \tag{B.5}$$

These equations take exactly the same form as the CMOS counterpart.

B.3 Figures of Merit

In this section, we consider several figure of merit for TFTs with emphasize in the subthreshold region. The model used for the simulation is based on the [**?**] and parameter values are extracted using the same samples. The W/L of the TFT under test is $50\mu m/20\mu m$.

B.3.1 Intrinsic Gain

Intrinsic gain is an important figure of merit for analog amplifier as it reflects the highest achievable single stage gain for an amplifier. The simulation based on the model developed earlier is shown in Fig. B.1. As seen, the intrinsic gain in subthreshold region is related with subthreshold slope and the ideality factor n of the Schottky junction.

The expression of the intrinsic gain can be approximated as:

$$A_i = g_m r_o = \frac{\ln 10}{V_A \cdot SS} \tag{B.6}$$

This suggests that intrinsic gain is reverse proportional to the SS of the TFT. By pushing the SS to its theoretical limit (60mV), one could get over 1000 intrinsic gain with even less ideal Schottky-Barrier at source-semiconductor contact (smaller n). The expression also suggests that the value of intrinsic gain is rather independent on the bias of the transistor as long as it is working in subthreshold region.

Ideality factor n contributes to the intrinsic gain of the transistor because it controls the effective Early voltage (V_A) and thus influence the output resistance of the TFT.

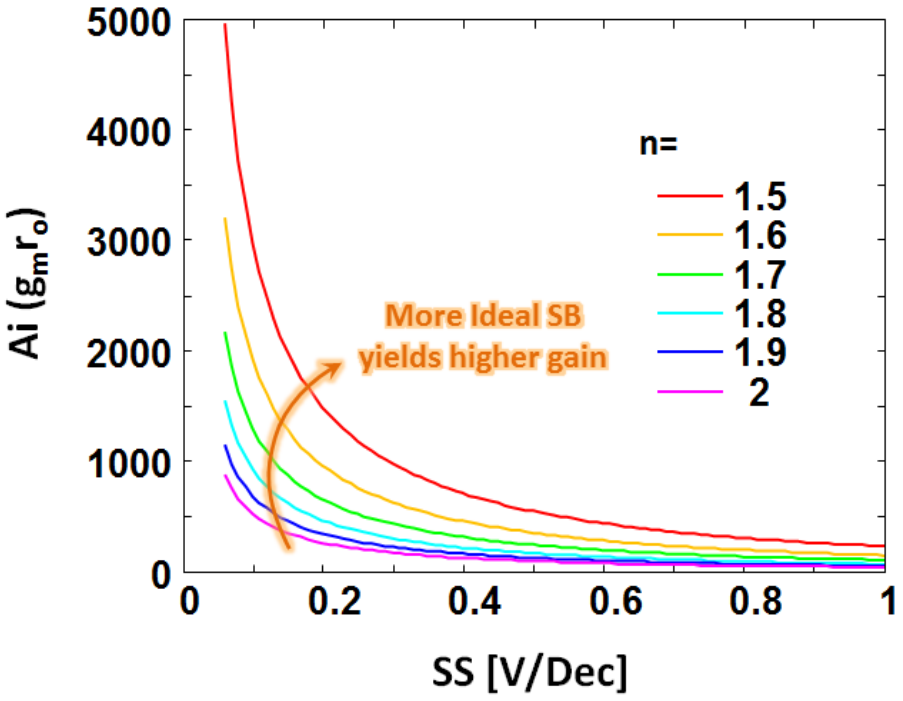


Fig. B.1 Simulation result for the intrinsic gain (A_i) of the Schottky-Barrier IGZO TFT (SB-TFT). The parameter n is the ideality factor of the source-semiconductor junction.

B.3.2 Transconductance Efficiency

Transconductance efficiency (g_m/I_{DS}) is another important figure of merit for electron devices. It represents the efficiency of converting the bias current into an equivalent transconductance. For analogue TFT circuits, as the voltage bias is normally limited by the driving circuitry and the application, reducing the current bias while maintaining a high gm also means reducing the power consumption while keeping the circuit performance.

As can be seen from Fig. B.2, the highest g_m/I_{DS} can be obtained only at deep- subthreshold region for a TFT before it enters a transition region to above-threshold. This value remains a constant at deep-subthreshold due to the exponential nature of the TFT subthreshold behaviour. The simulation result also suggests that this value would increase if the TFT has a steeper subthreshold slope.

The expression of the g_m/I_{DS} value can be estimated as:

$$\frac{g_m}{I_{DS}} = \frac{\ln 10}{SS} \tag{B.7}$$

For above-threshold region, the g_m/I_{DS} value drops as the TFT enters above-threshold region, where the expression is:

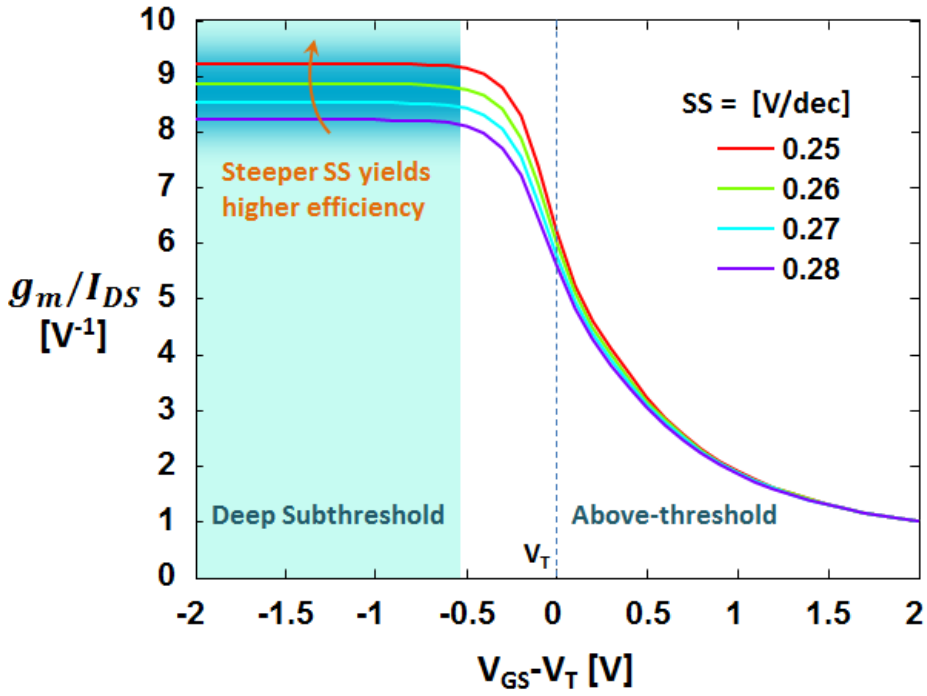


Fig. B.2 g_m/I_{DS} from deep subthreshold to above threshold region. The value reaches maximum at deep subthreshold and increases with steeper SS.

$$\frac{g_m}{I_{DS}} = \frac{2+\alpha}{V_{GS}-V_T} \tag{B.8}$$

where α is the coefficient on the power law of TFT model, α=0 for the case of MOSFET [17]–[19]. Therefore, biasing a TFT at a high gate voltage would result in a less efficient g_m conversion and thus higher power consumption.

B.3.3 Cut-off frequency

Cut-off frequency (f_T) is also considered as the current gain bandwidth product as the current gain at f_T is equal to 1 [17]. This value will limit the actual gain bandwidth product of amplifiers designed by the device. The simulation result of f_T is shown in Fig. B.3. Here f_T is small as the overlap capacitance of the TFT under test is quite big. The overlap length here is 50μm, which is even bigger than the channel length of the device. Practically, this value can be reduced to a few μm or even lower with self-aligned process.

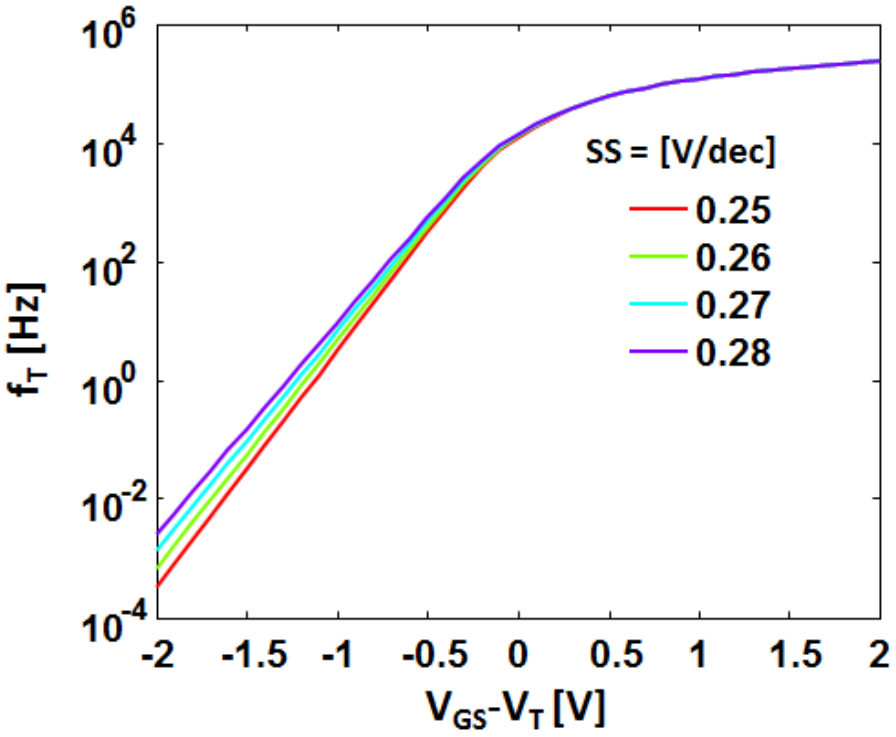


Fig. B.3 Cut-off frequency vs. voltage bias for different SS.

Fig. B.3 suggests that this product rolls off pretty quickly in subthreshold region. The expression of f_T can be derived as follows:

$$f_T = \frac{g_m}{2\pi C_{ov}} = \frac{I_{DS} \cdot \ln 10}{SS \cdot 2\pi C_{ov}} \tag{B.9}$$

The expression shows that the value of f_T is proportional to I_{DS}, thus the quick roll of at subthreshold is explained by the current roll off in subthreshold region. As I_{DS} and C_{ov} are both proportional to the channel width of the TFT, f_T would be independent of channel width. In addition, by reducing the overlap length, one could further reduce the overlap capacitance (C_{ov}) to increase the frequency response.

The expression also suggests that biasing the TFT in a deeper subthreshold region would at the same time pushing the frequency response lower proportionally. Therefore, it's maybe desirable to have a less steep subthreshold slope in terms of speed when considering subthreshold operation.

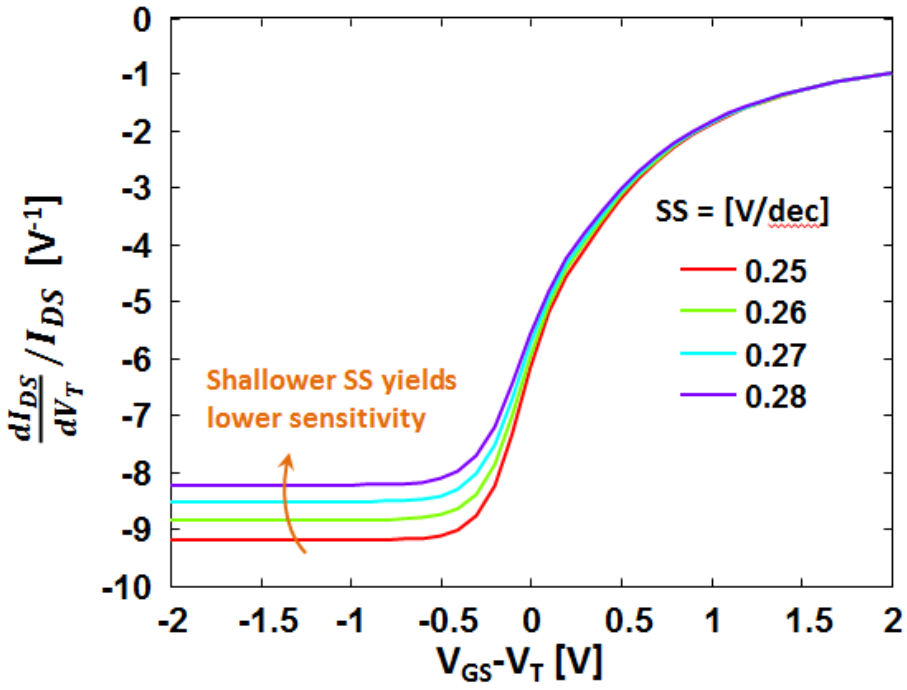


Fig. B.4 Normalized sensitivity to VT shift for different SS

B.4 Sensitivity to Variations and Bias

B.4.1 Current Sensitivity to Variations

Here, we assume the threshold voltage shift is also a uniform shift in subthreshold. A non-uniform shift in subthreshold would mean a change in subthreshold slope, which will be discussed later. Therefore, the V_T shift at abovethreshold is the same as a reference voltage shift at subthreshold. As the reference voltage shift is equivalent to a bias voltage shift. This curve can also be used for testing the sensitivity of bias voltage inaccuracy.

Fig. B.4 shows that at deep subthreshold region the normalized current sensitivity to V_T shift is a constant. The sensitivity becomes lower when the TFT is approaching and enters above threshold region. As V_T shift is equivalent to bias shift, the sensitivity expression can be the same as the g_m/I_{DS} curve (as $g_m = \mathrm{d}I_{DS}/\mathrm{d}V_{GS}$ is also a sensitivity to bias) just with an opposite sign. For deep-subthreshold:

$$\frac{dI_{DS}}{dV_{GS}}/I_{DS} = -\frac{\ln 10}{SS} \tag{B.10}$$

For above-threshold:

$$\frac{dI_{DS}}{dV_{GS}}/I_{DS} = -\frac{2+\alpha}{V_{GS}-V_T} \tag{B.11}$$

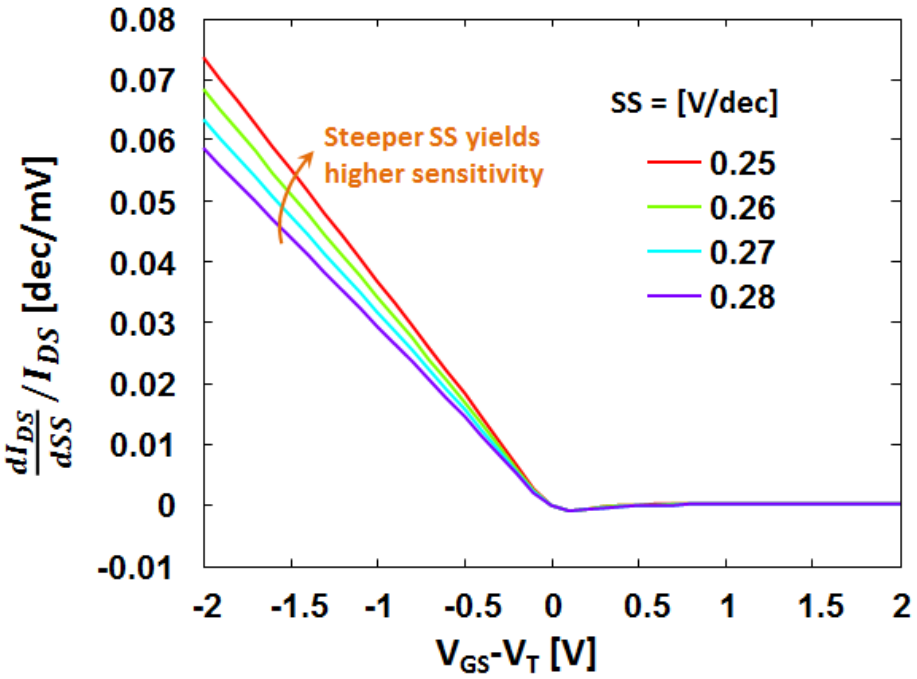


Fig. B.5 Normalized sensitivity to SS variations for different SS mean values

Now we assume the change in SS would not affect V_T of the above threshold region. Therefore, the subthreshold current of different SS would meet at around V_T. This yields the results shown in Fig. B.5, where the normalized current sensitivity would drop when the TFT is biased closer to V_T. In above threshold region, the parameter SS do not contribute to the equation of I_{DS}. The sensitivity is therefore zero. The curve also shows that a steeper SS would increase the current sensitivity.

The expression for the current sensitivity in subthreshold is shown below:

$$\frac{dI_{DS}}{dSS}/I_{DS} = -\frac{(V_{GS}-V_T)\cdot \ln 10}{SS^2} \tag{B.12}$$

The above equation suggests that the sensitivity is reverse proportional to SS^2. Therefore, a steeper SS would yield a high current sensitivity on the variations of SS. In summary, although steeper SS would give rise to g_m/I_{DS} and potentially further reduce the power consumption, the sensitivity on process variations of SS and V_T would increase, possibly narrowing the design window for analog circuits.

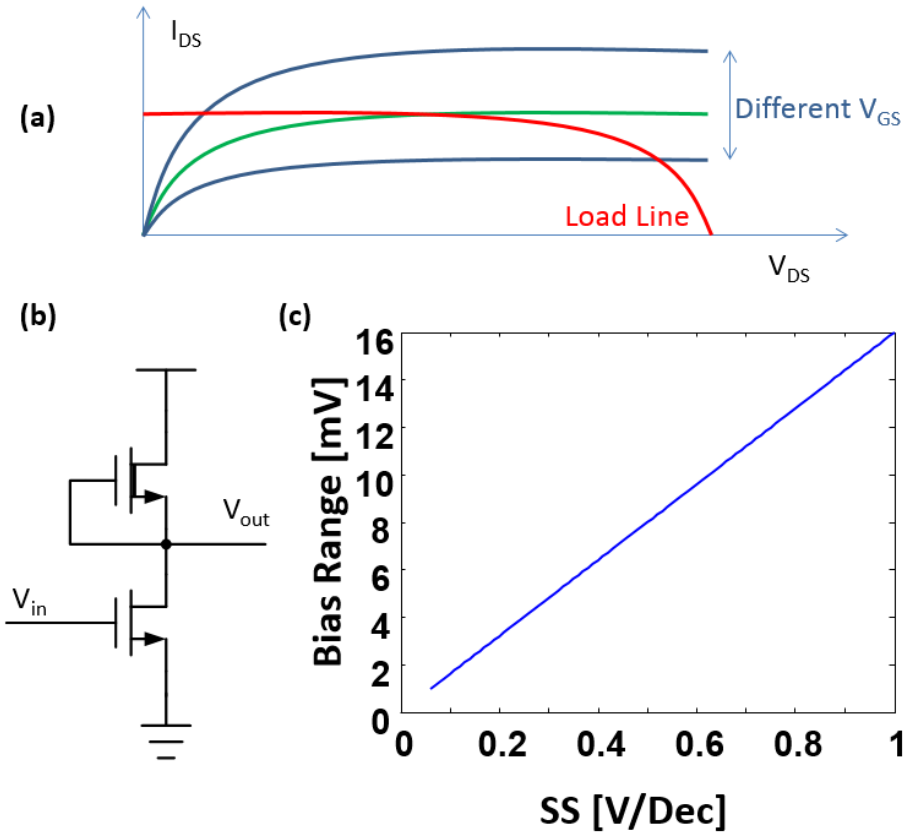


Fig. B.6 The useful bias range for a depletion load common-source amplifier. (a) conceptual figure of the load line and transfer curve of the amplifier, where green curve illustrates the correct bias condition and blue curves illustrates that the amplifying TFT is biased out of useful bias range (b) circuit schematic of the amplifier (c) simulated useful bias range with respect to SS

B.4.2 Accuracy Requirement for Biasing Circuitry

Here, we take a common source amplifier with depletion load as example (Fig. B.6(b)). The load line and bias conditions is shown in Fig. B.6(a). As can be seen, bias conditions should keep both transistors working in saturated region, i.e. the V_{GS} for the green line in Fig. B.6(a). The blue lines show either of the two TFTs is working in a not saturated region.

Therefore, to maintain a high gain, V_{DS} for both TFTs should follow $V_{DS} > v_{sat}$. As the value of v_{sat} for different V_{GS} stays the same in subthreshold, the input voltage range can be calculated as:

$$V_{range} = \frac{2 \cdot SS\,(V_{DD} - 2v_{sat})}{V_A \ln 10} \tag{B.13}$$

B.5 Conclusion

We investigate several figures of merit of TFT's subthreshold operation including A_i, g_m/I_{DS}, f_T and the design sensitivity for biasing circuitry and device variations. The results of this chapter could benefit researchers working in device fabrication and circuit design while considering subthreshold operating TFTs specifically from a device performance perspective to a lower level analogue design. The results suggest that one could get high A_i, g_m/I_{DS} through biasing TFTs in subthreshold region at the cost of reduced f_T and increased sensitivity to bias and process variations. Another interesting conclusion is that TFTs with less steep subthreshold slope can still benefit from a high A_i and g_m/I_{DS}, but with reduced sensitivity to variations and less strict requirement on accuracy of biasing circuitry.