P-type electrical contacts for two-dimensional transition metal dichalcogenides

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Digital logic circuits are based on complementary pairs of n- and p-type field effect transistors (FETs) via complementary metal oxide semiconductor (CMOS) technology. In three dimensional (3D or bulk) semiconductors, substitutional doping of acceptor or donor impurities is used to achieve p- and n-type FETs. However, the controllable p-type doping of low-dimensional semiconductors such as two-dimensional transition metal dichalcogenides (2D TMDs) has proved to be challenging. Although it is possible to achieve high quality, low resistance n-type van der Waals (vdW) contacts on 2D TMDs[1–5], obtaining p-type devices from evaporating high work function metals onto 2D TMDs has not been realised so far. Here we report high-performance p-type devices on single and few-layered molybdenum

disulphide (MoS_2) and tungsten diselenide (WSe_2) based on industry-compatible electron beam evaporation of high work function metals such as Pd and Pt. Using atomic resolution imaging and spectroscopy, we demonstrate near ideal vdW interfaces without chemical interactions between the 2D TMDs and 3D metals. Electronic transport measurements reveal that the Fermi level is unpinned and p-type FETs based on vdW contacts exhibit low contact resistance of 3.3 kΩ·μm, high mobility values of ~ 190 cm^2-$V^{-1}s^{-1}$ at room temperature with saturation currents in excess of > 10^{-5} Amperes per micron (A-μm^{-1}) and on/off ratio of 10^7. We also demonstrate an ultra-thin photovoltaic cell based on n- and p-type vdW contacts with an open circuit voltage of 0.6 V and power conversion efficiency of 0.82%.

Two dimensional semiconductors based on TMD family of materials possess ideal attributes such as atomically thin body and absence of dangling bonds for next generation of electronics[6,7]. However, controllable and reliable substitutional doping of 2D TMDs is challenging – making it difficult to realise purely p- and n-type devices as well as achieving low resistance contacts[8,9]. When metal contacts are evaporated on 2D MoS_2 and other TMDs, interface defects are created that pin the Fermi level near the conduction band and therefore n-type devices are most commonly obtained[10,11]. We[2] and others[1,5,12,13] have recently shown that low contact resistance vdW contacts can unpin the Fermi level so that high performance n-type and ambipolar devices on 2D TMDs can be realised. While p-type devices on multi-layered WSe_2 have been demonstrated using mechanical transfer of metal contacts[3,13], purely p-type FETs based on monolayers have yet to be achieved. P-type devices in monolayer MoS_2 are even more challenging because the valence band energy is located > 6 eV below the vacuum level[14]. The fundamental challenge in achieving ultra-clean p-type vdW contacts by electron beam evaporation – the most commonly used industrial method for deposition of contact metals – on single layer TMDs is that high work function metals

require high energy for sublimation. The transfer of this energy to 2D TMD layers upon deposition of metal atoms leads to formation of defects[15,16].

We have found that clean vdW contacts by evaporation of Pt and Pd (as well as other metals such as Au) onto mono- and multi-layered 2D TMDs such as MoS_2 and WSe_2 can be achieved by minimizing damage at the interface by ensuring that temperature of the devices remains close to room temperature (see Methods). We have characterized the interfaces between the evaporated high work function metals and the 2D TMD semiconductors by annular dark field (ADF) imaging in a scanning transmission electron microscope (STEM), X-ray photoelectron spectroscopy (XPS) and electron energy loss spectroscopy (EELS). This work focuses on realizing p-type FETs with Pd or Pt contacts. We have also demonstrated devices with Au contacts and found that although Au forms clean contacts with MoS_2 and WSe_2, p-type behavior is limited by its relative low work function compared to Pd and Pt[17] (Extended Data Fig. 1). We find that Pd forms clean vdW contacts with few-layered MoS_2 (Fig. 1a). The spacing between the sulfur and Pd atoms at the interface was found to be 2.3 ± 0.1 Å [Fig. 1a (ii)] – slightly smaller than the vdW gap in indium alloy contacts[2]. The interface chemistry was analysed by taking several XPS and EELS spectra at multiple locations on the sample and on several samples to ensure good statistics. Chemical analysis of the Pd-MoS_2 interface with XPS obtained from very thin (< 5 nm) Pd films on MoS_2 revealed that the interface is clean with only pristine Pd $3d_{3/2}$ and Pd $3d_{5/2}$ peaks at ~ 340.3 eV and ~ 335 eV visible and no evidence of Pd_xS_y or PdS_2 was found – as indicated by typical results shown in Fig. 1b. The absence of chemical bonding at the interface is corroborated by EELS analysis (Fig. 1c) using a 0.9 Å electron beam probe focused on the sulfur atom adjacent to the deposited metal. The results show that the $L_{2,3}$ edge of the S atom at the interface is the same as

that of S atoms in the layers away from the interface – suggesting that the electronic structures of the S atoms are the same and no chemical interaction occurs between S and Pd at the interface. In contrast, for Pd deposition on WSe_2 under the same conditions, ADF STEM imaging and XPS analysis indicates chemical interaction between the Pd and Se (Extended Data Fig. 2a and b).

The results from deposition of Pt on multi-layered WSe_2 are shown in Fig. 1d-f. The ADF STEM images of the interface are shown in Fig. 1d (i) and (ii). The spacing between the Pt and Se atoms is also ~ 2.3 ± 0.1 Å [Fig. 1d (ii)]. Absence of chemical interaction between Pt and Se atoms at the interface was confirmed by several XPS scan on < 5 nm Pt films on WSe_2 (Fig. 1e), which show only pristine Pt $4f_{5/2}$ at ~ 74 eV and Pt $4f_{7/2}$ at ~ 71 eV and no evidence for $PtSe_2$ or Pt_xSe_y formation[18]. The EELS data taken from several regions at the interface shown in Fig. 1f also reveals that the electronic structure of the Se atoms at the interface is largely unperturbed.

Electrical measurements on FETs fabricated using high work function metals as contacts and few-layered 2D MoS_2 and WSe_2 as the semiconductor channels are shown in Fig. 2. Remarkably, it can be seen from Fig. 2a, b that the deposition of Pd on few-layered MoS_2 leads to primarily p-type FET transfer and output characteristics with the saturation hole current reaching ~ 4 μA/μm while the saturation electron current remains ~ 0.1 μA/μm. The hole mobility for MoS_2 was found to be 45 ± 5 cm^2-$V^{-1}s^{-1}$. FET characteristics as a function of temperature (Extended Data Fig. 3a,b) were measured to extract the hole Schottky barrier[19], which was found to be 500 ± 50 meV (Extended Data Fig. 3c) for Pd contacts on few-layered MoS_2. For the ambipolar devices, the Schottky barrier height can be extracted by comparing the hole and electron current branches[20]. The hole Schottky barrier extracted using this method was found to be 530 ± 30 meV – consistent

with the low temperature method. The fact p-type operation can be achieved with such a large Schottky barrier via modulation of Fermi level with gate voltage indicates that the Pd/2D MoS_2 interface is clean and the Fermi level is unpinned[21].

We have found that purely p-type FETs with exceptionally high saturation hole currents of 3.07×10^{-4} A (W= 12 μm, L= 4 μm.) and no measurable electron currents can be achieved with Pt contacts on few-layered WSe_2, as observed in the transfer and output characteristics of devices in Fig. 2c and 2d. It can be seen in Extended Data Fig. 3d, e that the purely p-type behavior persists at temperatures down to 70 K. Mobility values of 190 ± 10 cm^2-$V^{-1}s^{-1}$ were obtained with on/off ratios of 10^7 – comparable to those obtained for mechanically transferred Pt contacts[4]. Analysis of the hole Schottky barrier height reveals that it is 200 ± 20 meV (Extended Data Fig. 3f), which leads to efficient injection of holes and acts as significant barrier for injection of electrons. Forward and reverse scans for multi-layer WSe_2 FETs with Pt electrodes are shown in Extended Data Fig. 4. For comparison, damaged interface with ~ 3 nm intermixing layer is clearly seen in cross-sectional STEM image of Pt-WSe_2 interface without optimization of deposition parameters (Extended Data Fig. 5a). The transfer characteristics (Extended Data Fig. 5b) shows poor p-type performance with damaged interface. To demonstrate how the contacts affect the p-type characteristics, the results with Pt contacts on MoS_2 and Pd contacts on WSe_2 are shown in Extended Data Fig. 6. MoS_2 FETs with Pt contacts exhibit lower hole currents compared to Pd contacts due to slightly lower work function of the thin Pt film deposited on TMD (Work function measurement results of Pt and Pd thin films grown on TMDs are shown in Extended Data Fig. 7). Poor p-type characteristics of WSe_2 FETs with Pd contacts are due to chemical interactions between Pd metal and WSe_2. In addition, the influence of substrates (SiO_2, CVD grown hBN on

SiO_2, and PMMA on SiO_2) on hole injection into MoS_2 and WSe_2 with high work function metal contacts is shown in Extended Data Fig. 8 and 9. We have also summarized the electron to hole current ratios of WSe_2 and MoS_2 FETs with different contacts on various substrates (Extended Data Fig. 10). The results show that contacts have dominant influence on the polarity of the devices while the substrates affect the hole current levels. The hole contact resistance of MoS_2 FETs with Pd contacts and WSe_2 FETs with Pt contacts were extracted by transfer length method (TLM) and shown in Fig. 2e,f. Hole contact resistance for multilayer MoS_2 is around 430 kΩ·μm due to the large Schottky barrier. Contact resistance for multilayer WSe_2 is ~ 3.3 kΩ·μm. Analysis of the literature reveals that our high work function metal contacts give comparable device performance to dry transferred metal contacts and are much lower than the reported evaporated contact resistances (Fig. 2g,h, also in Extended data Table 1-3).

In addition to few-layered MoS_2 and WSe_2, we have also realised high work function vdW contacts on single layer TMDs grown by chemical vapor deposition (CVD) (Extended Data Fig. 11). Cross-sectional ADF atomic resolution images of Pt on WSe_2 and Pd on MoS_2 are shown in Fig. 3a and 3e. Typical transfer curve of CVD grown monolayer WSe_2 FETs with Pt electrodes is shown in Fig. 3b. It can be seen that the device shows purely p-type behavior with high saturation hole currents of ~ 7.6 μA/μm. The mobility of monolayer devices was found to range from 10 – 40 of cm^2-$V^{-1}s^{-1}$. The output curves of CVD monolayer WSe_2 FET are shown in Fig. 3c. The TLM results in Fig. 3d show that the contact resistance of monolayer WSe_2 FET is around 229 kΩ·μm. The higher contact resistance compared to multilayer WSe_2 is due to higher valance band edge for hole injection that leads to higher Schottky barrier height (Extended Data Fig. 12). The transfer characteristics of CVD grown monolayer MoS_2 FETs are shown in Fig. 3f. We are able to obtain

p-type behavior with ~ 0.008 μA/μm hole currents. This is consistent with the fact that hole injection into monolayer MoS_2 is exceptionally difficult even with clean contacts of high work function metals because the valence band is located > 6 eV below the vacuum level, which means that there is a significant barrier for hole injection. The fact that we are able to obtain hole currents in monolayer MoS_2 FETs is consistent with realisation of clean vdW contacts and absence of Fermi level pinning. These results suggest that it is possible to fabricate clean vdW contacts using high work function metals on CVD grown monolayers of MoS_2 and WSe_2 to achieve p-type FETs.

We now demonstrate the integration of n- and p-type vdW contacts onto 2D TMDs in ultra-thin photovoltaics and photodiodes. The schematic of the device is shown in Fig. 4a where we utilise our previously reported[2] indium alloy vdW contacts for electron injection (n-type) and high work function vdW contacts based on Pt and Pd reported here for hole injection (p-type). This way, we are able to realize metal-semiconductor-metal (MSM) diode on the same 2D TMD. The FET output curves for In/Au-MoS_2-Pd devices shown in Fig. 4b exhibit diode characteristics at all gate voltages, with a rectification ratio of up to 10^6. The diode properties in dark and under illumination are shown in Fig. 4c. A significant photocurrent is generated under illumination and open circuit voltage of ~ 0.5 ± 0.03 V is obtained. The corresponding power conversion efficiency is calculated to be ~ 0.40 ± 0.02% and the power output of 267 nW is obtained at V_m= 0.3 V (maximum power output point). A similar device consisting of In/Au-WSe_2-Pt also exhibited diode-like behavior at different gate voltages (Fig. 4d) with a rectification ratio of up to 10^7. The current-voltage characteristics under dark and illumination for the In/Au-WSe_2-Pt devices are shown in Fig. 4e. The open circuit voltage measured in these devices is larger (0.6 ± 0.03 V), which results in higher conversion efficiency of 0.82 ± 0.05% with a maximum power output of 572 nW at V_m= 0.35 V.

The responsivity of the photodiodes was found to be 17.6 mA W^{-1} and 33.1 mA W^{-1} with external quantum efficiencies of 4.1% and 7.7% for the In-MoS_2-Pd and In-WSe_2-Pt devices, respectively. The photodiode properties (power output, power conversion efficiency, responsivity and external quantum efficiencies) for MoS_2 and WSe_2 devices are among the highest reported[1,35–37]. We have also measured diode properties at three different laser powers as shown in Fig. 4f. It can be seen that the photocurrent increases with power but the open circuit voltage (defined by the contacts) remains constant.

We have demonstrated clean vdW contacts of high work function metals such as Pd, Pt and Au on few- and single-layered MoS_2 and WSe_2. These contacts lead to p-type characteristics on single layer MoS_2 and purely p-type on WSe_2. The results also suggest that the Fermi level is unpinned and can be modulated with gate voltage. P-N diodes have been achieved with n- and p-type contacts. Our discovery will allow realization of next generation of electronics based on 2D materials under the current complementary p-n FET paradigm.

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Author Contributions MC conceived the idea, supervised the project and wrote the paper with YW. YW synthesized all the samples, measured all devices and analysed the results. JCK, HYJ performed and analysed the STEM and EELS measurements with YW and MC. YL assisted in photoresponse measurements. KYM and SH, HSS performed hBN growth. MK assisted in Raman and PL characterization.

Competing Interests The authors declare no competing interests.

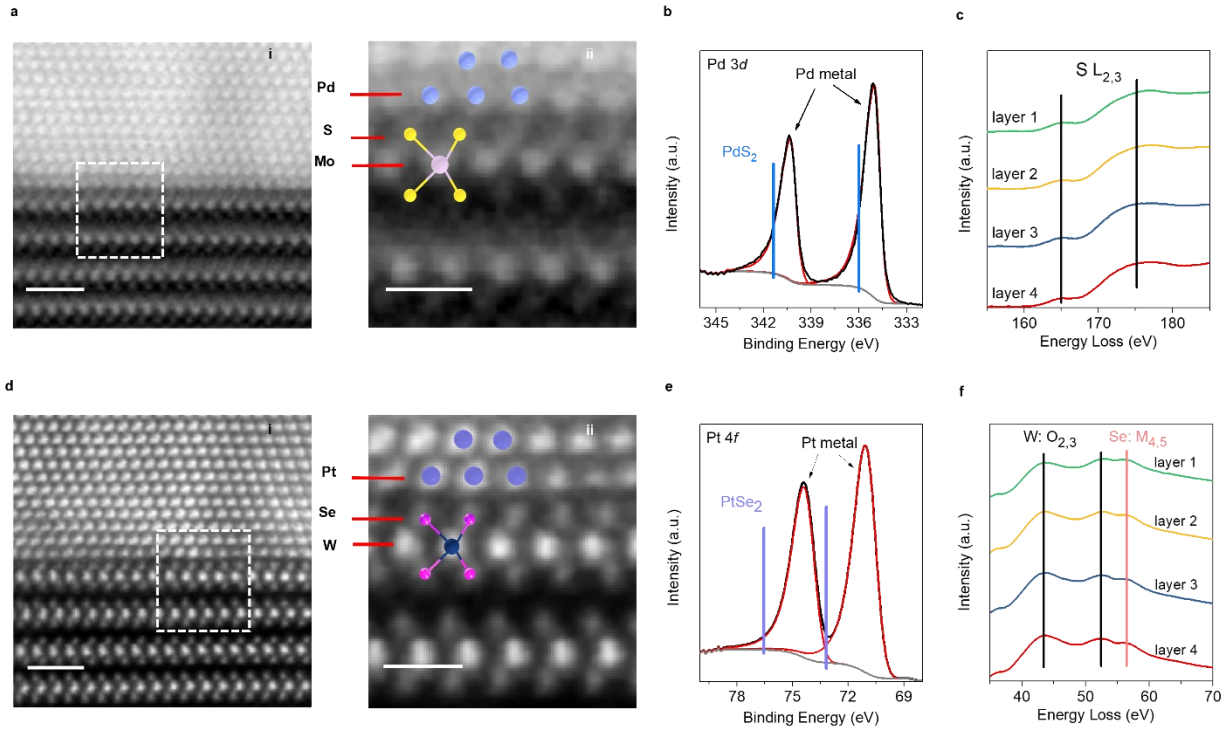

Figure 1 | Atomic resolution imaging and chemical analyses of the metal-semiconductor interface. a, Aomic resolution images of Pd on multilayer MoS_2. (i) Annular dark field (ADF) STEM image showing clean interface between Pd and MoS_2. Scale bar = 1 nm. (ii) Enlarged dashed rectangle region from (i) showing ADF STEM image where Mo, S and Pd atoms are visible. The distacne between Pd and S is 2.3 ± 0.1 Å. Scale bar = 5 Å. **b,** X-ray photoelectron spectrocopy (XPS) of Pd-MoS_2 interface showing only pristine Pd metal peaks with no evidence of PdS_2 or other chemical reactions. **c,** Electron energy loss spectroscopy (EELS) showing that the sulfur atoms at the interface are completely unaffected by the deposition of metal on top. The sulfur peaks of the topmost and the fourth layer are the same within the measurement precision. **d,** Aomic resolution images of Pt on multilayer WSe_2. (i) ADF STEM image of the interface and (ii) enlarged dashed rectangle region from (i). The distacne between Pt and Se is 2.3 ± 0.1 Å. Scale bars = 1 nm in (i) and 5 Å in (ii). **e,** XPS of Pt-WSe_2 interface showing pristine Pt metal peaks. **f,** EELS showing that the electronic structure of the Se atoms in all layers is similar.

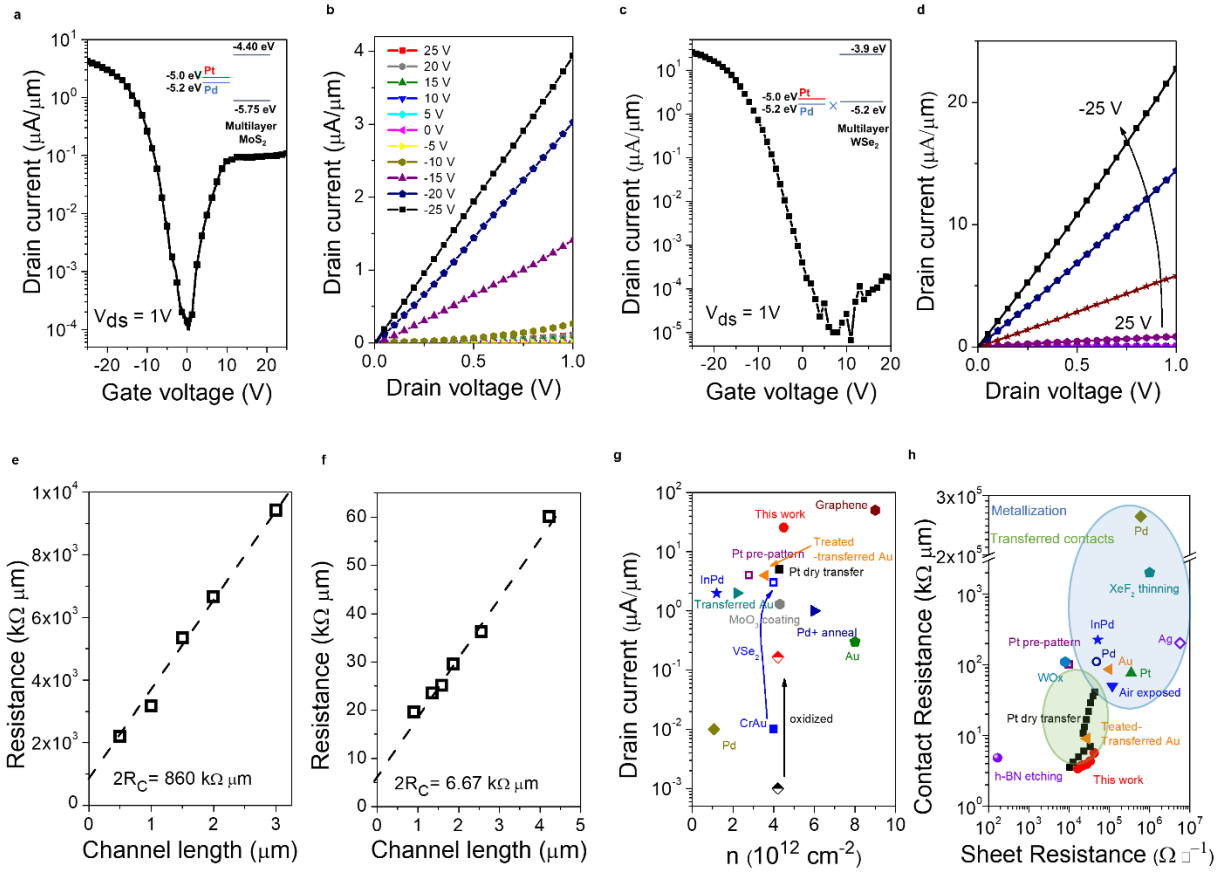

Figure 2 | Multilayer MoS_2 and WSe_2 devices with Pd and Pt contacts. a, Transfer curves of multilayer MoS_2 with Pd contacts showing ambipolar device characteristics with higher hole current branch compared to electron current. W= 5.5 μm, L= 2 μm. **b,** Output curves of multilayer MoS_2 with Pd contacts showing linear current-voltage curves for holes. **c,** Transfer curves of multilayer WSe_2 with Pt contacts showing pure p-type device characteristics. W= 12 μm, L= 4 μm. **d,** Linear output characteristics of multilayer WSe_2 with Pt electrodes. **e,** TLM results of multilayer MoS_2 with Pd electrodes. **f,** TLM results of multilayer WSe_2 with Pt contacts. **g, h,** Comparison of drain current and contact resistance of WSe_2 FETs with values reported in the literature using different methods[2,4,13,22–34].

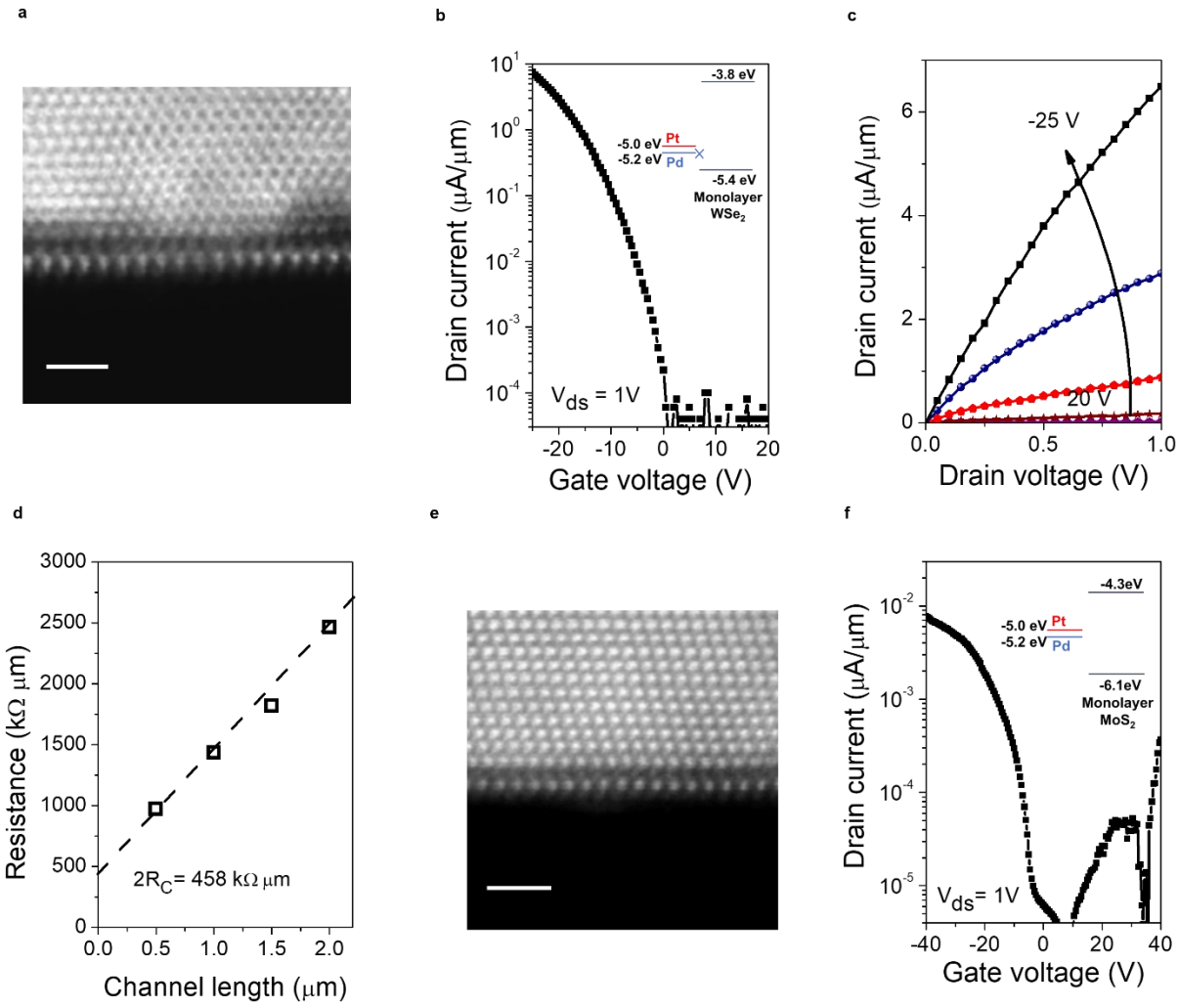

Figure 3 | CVD grown monolayer MoS_2 and WSe_2 with high work function metal contacts. **a,** ADF STEM image showing clean interface between Pt and monolayer WSe_2. Scale bar = 1 nm. **b,** Transfer curve of monolayer WSe_2 with Pt contact showing pure p-type characteristics. W= 4 μm, L= 1.5 μm. **c,** Output curve of monolayer WSe_2 FET with Pt contacts. **d,** TLM result of WSe_2 FET showing contact resistance value around 229 kΩ·μm. **e,** ADF STEM image showing clean interface between Pd and monolayer MoS_2. Scale bar = 1 nm. **f,** Transfer curve of monolayer MoS_2 with Pd contacts showing ambipolar device characteristic with higher hole current branch. W= 5 μm, L= 1 μm. The electron current values are << 1 nA.

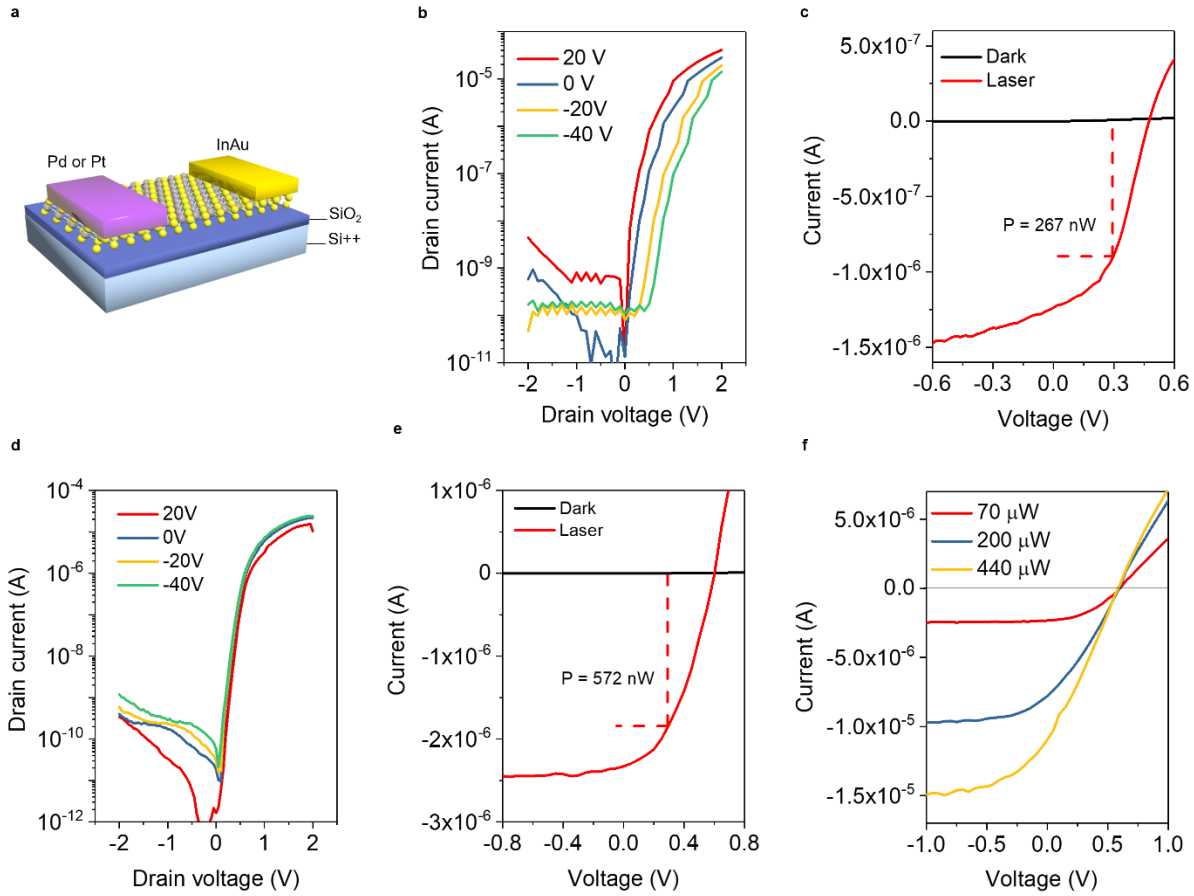

Figure 4 | Metal-semiconductor-metal photodiode with asymmetric electrodes for MoS_2 and WSe_2. a, Schematic illustration of the assymetric contact diode. **b,** Output curves of MoS_2 device with In/Au and Pd contacts showing good rectification behavior. **c,** I-V curves of the diode under dark and illumination (532 nm, 70 μW), demonstrating open circuit voltage of 0.48 V and output power of 267 nW. The red dashed lines show the corresponding power area for maximum power conversion. **d,** Output curves of WSe_2 device with In/Au and Pt contacts showing good rectification behavior. **e,** I-V curves of the diode under dark and illumination (532 nm, 70 μW), demonstrating an open circuit voltage of 0.6 V and output power of 572 nW. **d,** I-V curves under different illumination power showing increasing current and stable open voltage.

Methods:

High work function metal deposition on 2D TMDs for achieving vdW contacts: It has been widely reported that deposition of high work function metals with high melting temperature cause damage to the atomically thin 2D semiconductors[1,13]. We have carefully investigated the influence of a wide range of electron beam evaporation parameters (deposition rate, base vacuum pressure, power, and temperature) on the metal/2D TMD interface. We have found that radiative heating of the 2D materials from the crucible during metal evaporation is a crucial parameter for creation of vdW contacts with high work function metals (See Extended Data Fig. 13). To minimize the damage to the TMDs, we conducted the metal evaporation at a base pressure of $< 10^{-8}$ torr and long working distance of 70 cm. Furthermore, during heating of the crucible to metal sublimation temperature, the crucible and substrate shutters were kept closed to avoid radiative heating of the device. Once the crucible was sufficiently hot for metal sublimation to occur, the deposition was carried out in steps to ensure the device/ sample holder remained at or close to room temperature. For example, a typical process involved multiple steps of 10 nm Pd or Pt depositions at a rate of 2 Å/s. After this initial 50s step, the deposition was paused for one hour to allow the vacuum chamber and substrate holder to cool to room temperature before starting the next deposition step. Extended Data Fig. 13 shows the temperature versus time sketches for deposition of 300 Å Pt in a single step and with multiple steps. The temperature versus time plot on the left (without steps) shows that during deposition the temperature of the holder gradually increases with time. Usually, the substrate temperature increased from 18 °C to 36 °C during 300 Å Pt deposition and the chamber pressure increased from 5×10^{-8} torr to 8×10^{-7} torr. In contrast, the sketch on the right shows the temperature variation during deposition with three steps (100 Å Pt for each step). After each 100 Å of Pt deposition, the chamber and substrate holder were allowed to cool to room temperature

and the chamber pressure returned to the base pressure before running another deposition (red curve region in the plot). As a result, the temperature of the sample holder remained quite low (~24 °C) compared to the deposition without steps. These temperatures were recorded from the thermocouple connected at the bottom of the sample holder (a massive copper block). The real device temperature is likely to be much higher than the temperature of the Cu block. The temperature of the Cu block surface exposed to irradiation where the device is placed is likely to be higher than the back thermocouple reading. This supported by the fact that the PMMA crosslinks (Extended Data Fig. 12) at low deposition rates. We use the values from the thermocouple to compare relative heating of the device during contact evaporation. Typically, 20 nm of Pd capped with 20 nm of Au was used for Pd contacts (all deposited at 2 Å/s in 100 Å steps). For Pt contacts, 10 nm of Pt capped with 30 nm of Au was used. The voltage supplied to the crucible was 10 kV and the current used for the Pd deposition was 60 mA. For Pt deposition, the voltage was 10 kV and the current was 110 mA. For Au deposition, the voltage was 10 kV and the current was 75 mA. Typically, we used 20 nm of Pd and 20 nm of Au for Pd contacts. For Pt contacts, we deposited 10 nm of Pt first then 30 nm Au.

The method and results are reproducible. We have fabricated hundreds of devices with more than 50% showing dominant p-type behavior This is because we did not take any special precautions during device fabrication. For example, all materials and devices were processed in air and the 2D TMDs were transferred via wet chemical processes which can introduce residues. Despite this, we were able to reproduce our results from batch to batch. We fabricated devices at two institutions using completely different electron beam evaporation systems and found similar results. The devices used in this study were fabricated at the University of Cambridge and Ulsan Institute of Science and Technology.

2D TMD materials synthesis: Few-layered (3 - 20 layers, unless otherwise specified) MoS_2 and WSe_2 samples were obtained by mechanical exfoliation of bulk MoS_2 and WSe_2 crystals onto 300 nm or 100 nm of thermally grown SiO_2 on degenerately doped silicon substrates. The silicon substrate was cleaned in the usual way[2] prior to mechanical transfer. This involved washing with acetone, isopropanol and deionized water. After exfoliation, the flakes are identified and devices are patterned by electron beam lithography.

Single-layer MoS_2 and WSe_2 were grown by chemical vapor deposition (CVD). Detailed description of the methods is provided in references [38] and [39]. The as-deposited single layers were confirmed by PL and Raman spectroscopies shown in Extended Data Fig. 11. After growth, the samples were transferred to target substrates by wet transfer.

Role of substrates in devices: To achieve p-type devices, the electron doping from SiO_2 must be suppressed. To this end, it is important to passivate the SiO_2 substrate with self-assembled monolayers (SAMs), or by placing the 2D TMDs on hBN or polymethyl methacrylate (PMMA) substrates. The results in the main paper are based on 2D TMDs on SiO_2 passivated by SAMs. The FET characteristics of Pd and Pt contacts on few-layered MoS_2 and WSe_2 on different substrates (pure SiO_2, hBN/SiO_2, PMMA/SiO_2) are shown in Extended Data Fig. 8 and 9.

SAM treated SiO_2 was obtained by immersing in FOTS (trichloro-(1H,1H,2H,2H-perfluorooctyl) silane, silane/n-hexadecane (1:1000 v:v), purchased from Sigma-Aldrich) for 1 hour to passivate the surface -OH groups. After passivation, the substrate was rinsed with acetone and isopropanol multiple times. The hBN in this work is few-layer hBN grown by CVD. The PMMA substrate was

obtained by spin coating (MicroChem, A6) at 3000 rpm for 1 minute and heating at 180 ºC for 5 minutes. Since the PMMA substrate is not compatible with the ebeam lithography process. TEM grid was used as shadow mask to achieve channel length of around 10 μm.

Measurements: Electrical measurements at room and low temperature were carried using the Keithley 4200 current voltage system. Capacitances of the dielectrics used in this study were measured with Keithley 4200 capacitance-voltage unit. The low temperature measurements were performed in Lakeshore probe station. X-ray photoelectron spectroscopy (XPS) was measured by the Thermo Scientific K-Alpha system. PL and Raman data was collected using a 514-nm laser excitation focused through a × 100 objective lens. The spectra were taken at an incident laser power of 50 μW, which was sufficiently low to avoid any damage to the sample. Photoresponse current-voltage measurements were done using a 532-nm laser excitation focused through a 50× objective lens.

XPS measurements of the metal/semiconductor interface was carried out by depositing 20 nm of the metal on the 2D TMD and then incrementally etching the metal while simultaneously obtaining the spectra. The XPS spectra presented in the main paper were collected when the metal was thin enough (< 5 nm) for the x-rays to penetrate the metal and observe signal from both the contact metal and the TMDs (that is XPS peaks from the chalcogen and transition metal). The interface chemistry was double confirmed by XPS measurements of ~3 nm thin metal deposited on 2D TMDs without any depth profiling. UPS measurements are performed in ultrahigh vacuum using a He discharge UV lamp (He I line at 21.2 eV) to test work function of the thin metal films deposited on TMDs.

Schottky barrier extraction: Schottky barrier height of the contact was extracted using exactly the same methodology as in our previous work[2] by measuring the activation energy in the thermionic emission region. The current density of thermal emission through a metal-semiconductor contact is given by:

$$J = A^{*}T^{\alpha} \exp\left[-\frac{q\Phi_{B0}}{k_B T}\right][1 - \exp\left(-\frac{qV}{k_B T}\right)]$$

Where A* is the Richardson constant, V is the applied voltage, T is the temperature, α is an exponent equal to 2 for bulk semiconductors and 3/2 for 2D semiconductors, and kB is the Boltzmann's constant. Using this equation, the slope of the Richardson plot, $\ln(I/T^{3/2}) \sim 1/T$, yields Φ_{B0} as a function of gate voltage. The gate voltage at which the Schottky barrier height tends to curve away from the linear dependence is where the flat band condition occurs because after the gate voltage reaches this condition carriers are transferred through tunneling as well. To extract Schottky barrier height, we identify the voltage at which Φ_{B0} stops linearly depending on Vg, as shown in Extended Fig. 3c and 3f.

For ambipolar FETs, the Schottky barrier height can also be estimated by comparing the electron and hole branches. Electron and hole currents can be written as:

$$I_n = A^{*}T^{\alpha}e^{-\frac{q\emptyset_{b\_n}}{kT}}$$

$$I_p = A^{*}T^{\alpha}e^{-\frac{q\emptyset_{b\_p}}{kT}}$$

Combining with $E_g = q\emptyset_{b\_n} + q\emptyset_{b\_p}$, both electron and hole barriers can be extracted by comparing the electron and hole current branches.

STEM specimen preparation and acquisition parameters: The cross-sectional TEM specimens were fabricated using the same method described in reference[2]. Briefly, samples were prepared

using a focused ion beam (FEI Helios NanoLab 450). The cross-sectional STEM images were taken at 200 keV using a FEI Titan^3 G2 60-300 with a double-side spherical aberration (Cs) corrector. The probe convergence semi-angle was set to be ~ 26 mrad. ADF STEM images were acquired from 50-200 mrad range. All EELS measurements were collected in dual-mode to enable simultaneous collection of a zero-loss and a core-loss spectrum to compensate for energy drift during specimen acquisition.

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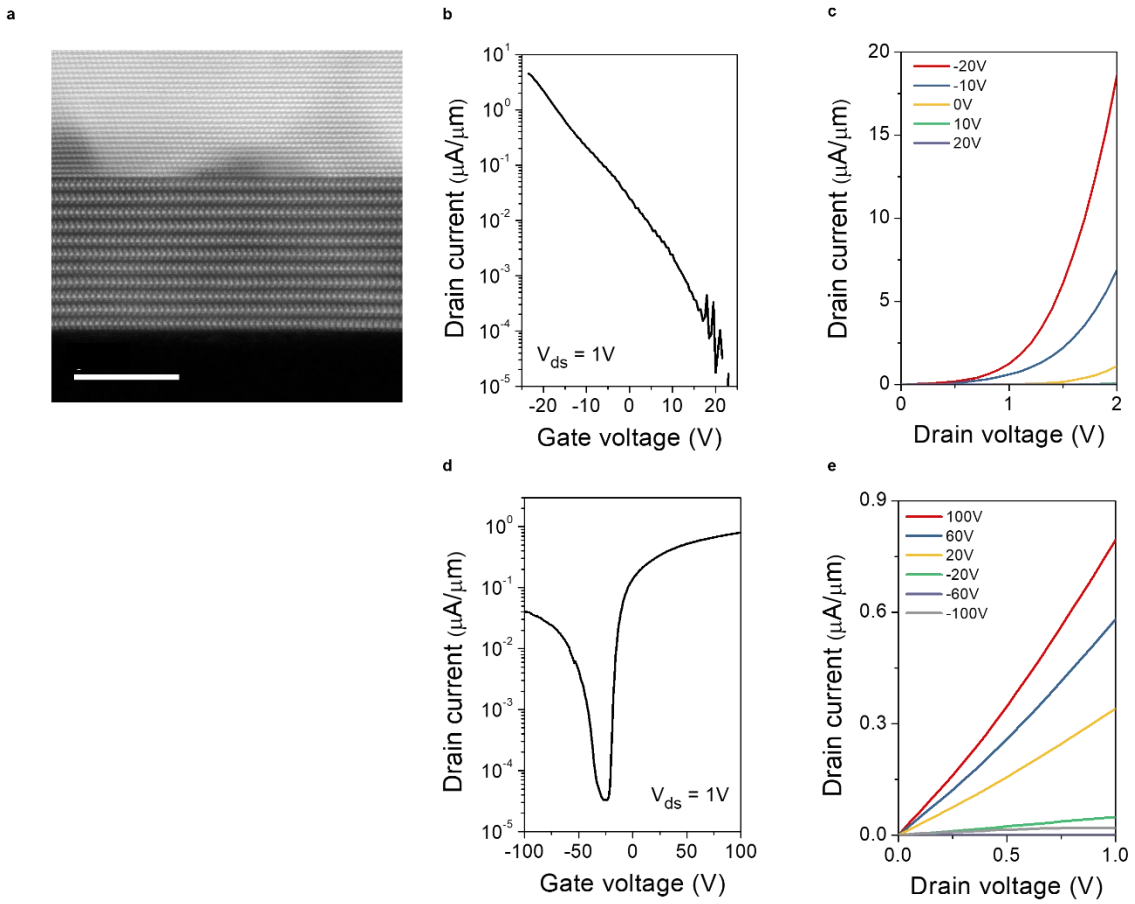
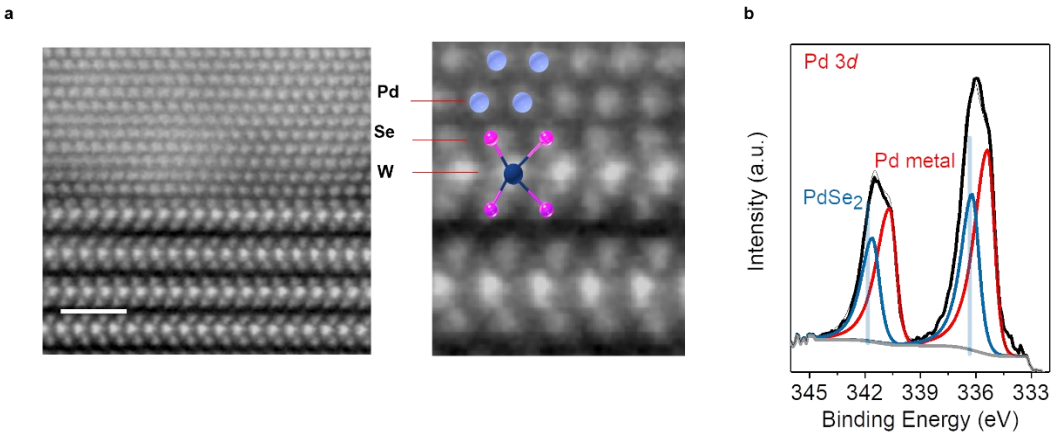
Data availability

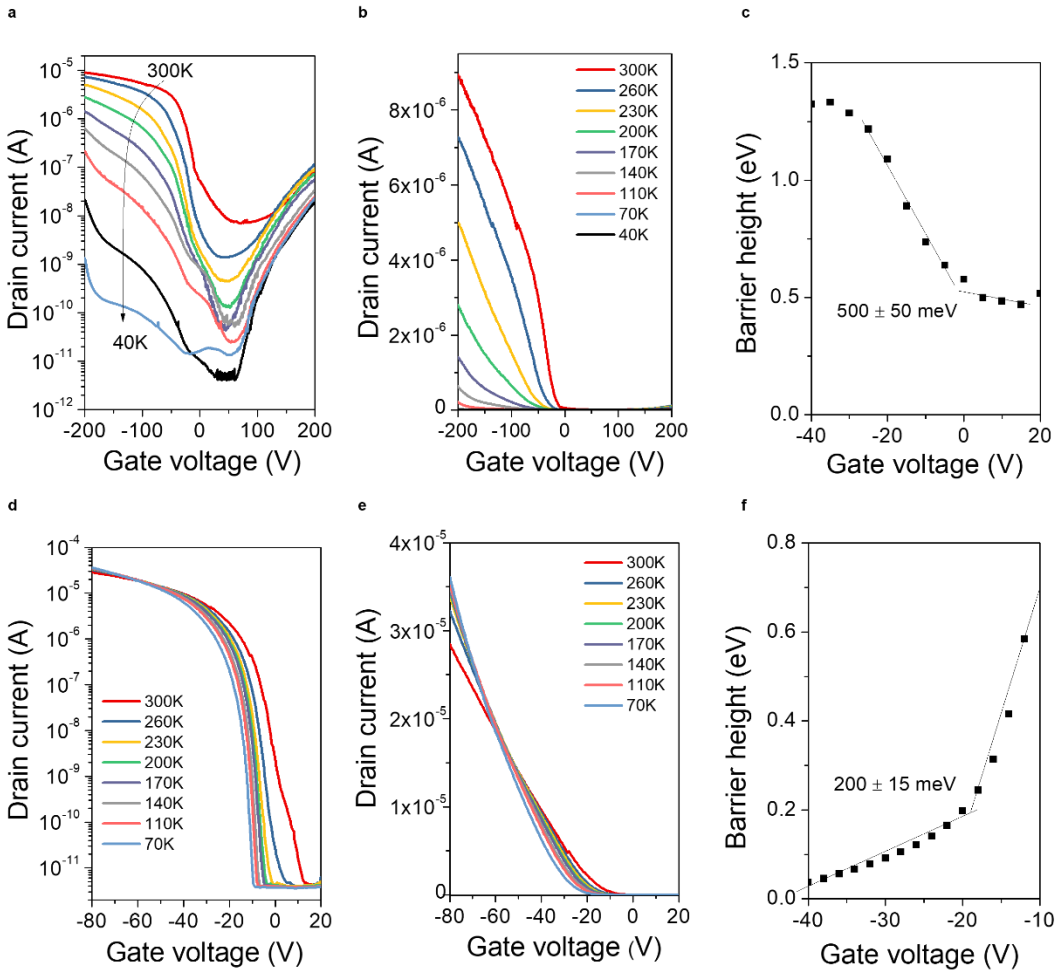
The data that support the findings of this study are available from the corresponding author upon reasonable request.



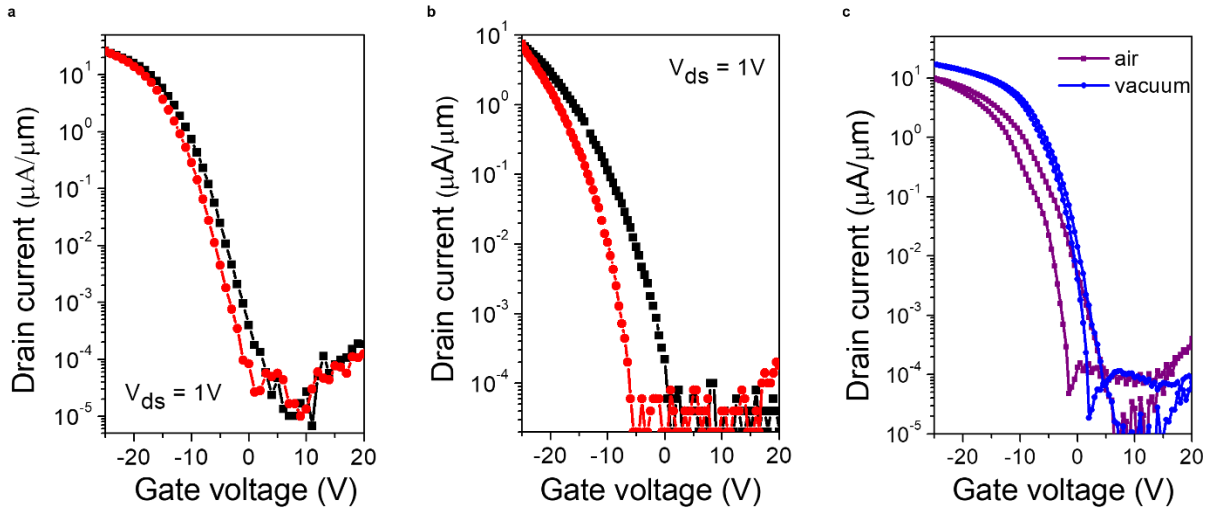
Extended Data Figure 1 | Au contacts on MoS_2 and WSe_2. a, Cross-sectional STEM image of a Au-WSe_2 device showing cleaning van der Waals interface. Scale bar = 5 nm. **b**, Transfer curves of WSe_2 device with Au contact showing p-type results. W= 4 μm, L= 1.5 μm. **c,** Output curves of WSe_2 device with Au contacts. The non-linear I-V curves indicate high Schottky barrier with Au contacts for WSe_2. **d,** Transfer curves of MoS_2 device with Au contacts on PMMA/SiO_2 substrate showing ambipolar behavior with dominant electron current. W= 8 μm, L= 10 μm. **e,** Output curves of MoS_2 device with Au contacts.



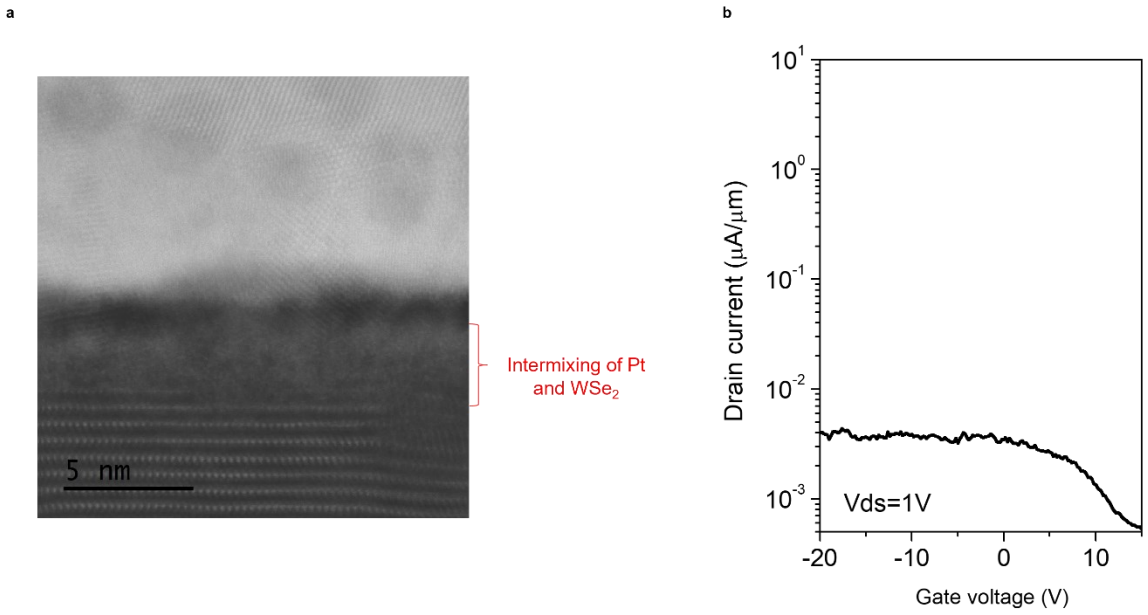
Extended Data Figure 2 | Pd contacts on WSe_2. a (i and ii), Cross-sectional STEM of the Pd-WSe_2 interface. Scale bar = 1 nm. **b**, XPS of Pd-WSe_2 interface showing the presence of $PdSe_2$ peaks, indicating reaction between the deposited metal and the Se atoms.



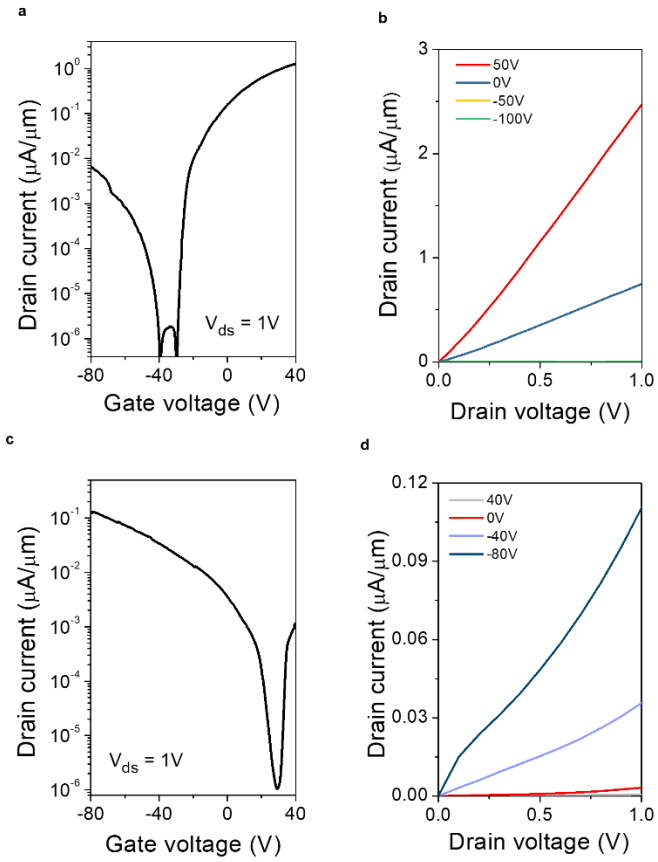
Extended Data Figure 3 | Low temperature measurements. a, Transfer curves of MoS_2 device with Pd contacts on PMMA/SiO_2 substrate at different temperatures. The hole transport part showed a more obvious temperature dependence compared to the electron branch, indicating thermally activated transport for holes and tunnel dominant transport for electrons due to higher Schottky barrier for electrons. **b,** Transfer curves from a plotted linearly. **c,** Schottky barrier extraction for holes in multilayer MoS_2 with Pd contacts. **d,** Transfer curves of WSe_2 device with Pt contacts at different temperatures. **e,** Transfer curves from **d** plotted linearly. **f,** Schottky barrier extraction for holes in multilayer WSe_2 with Pt contacts.



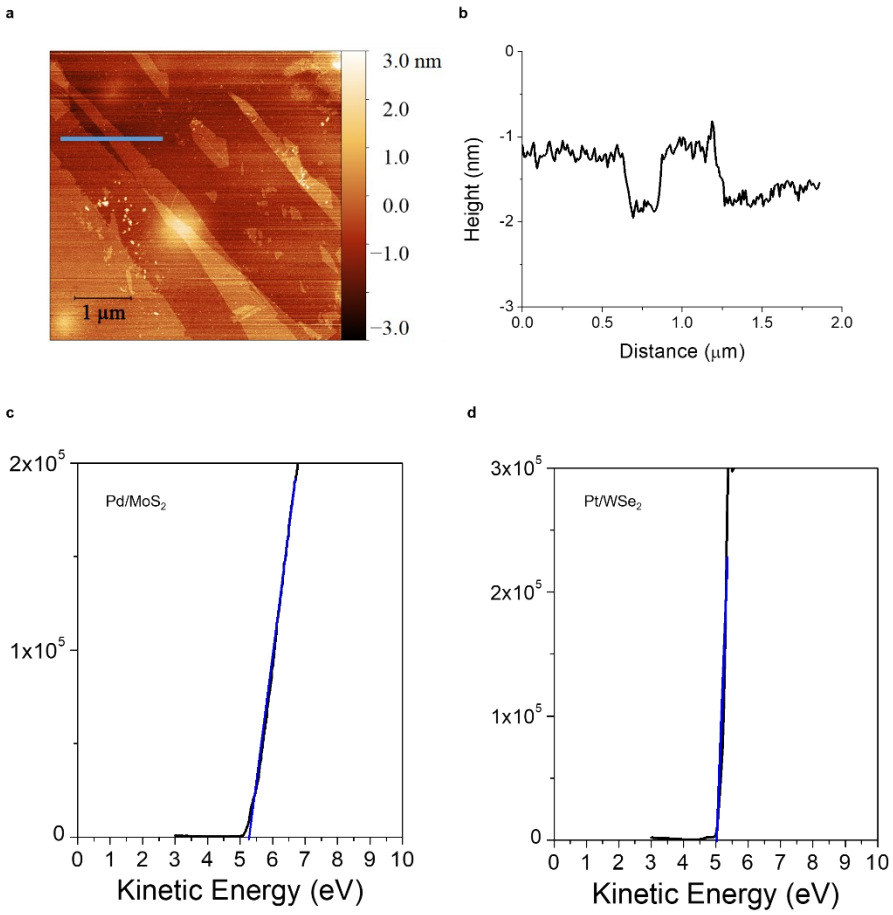
Extended Data Figure 4 | Hysteresis in WSe_2 FETs. Forward (red) and reverse (black) scans for multi-layer (**a**) and monolayer (**b**) WSe_2 FETs with Pt electrodes on SAM treated SiO_2. **c,** Transfer characteristics of the same monolayer WSe_2 FET measured in air and vacuum. It can be clearly seen that the hysteresis decreases in vacuum suggesting it is caused by adsorbates and not any defects at the contacts.



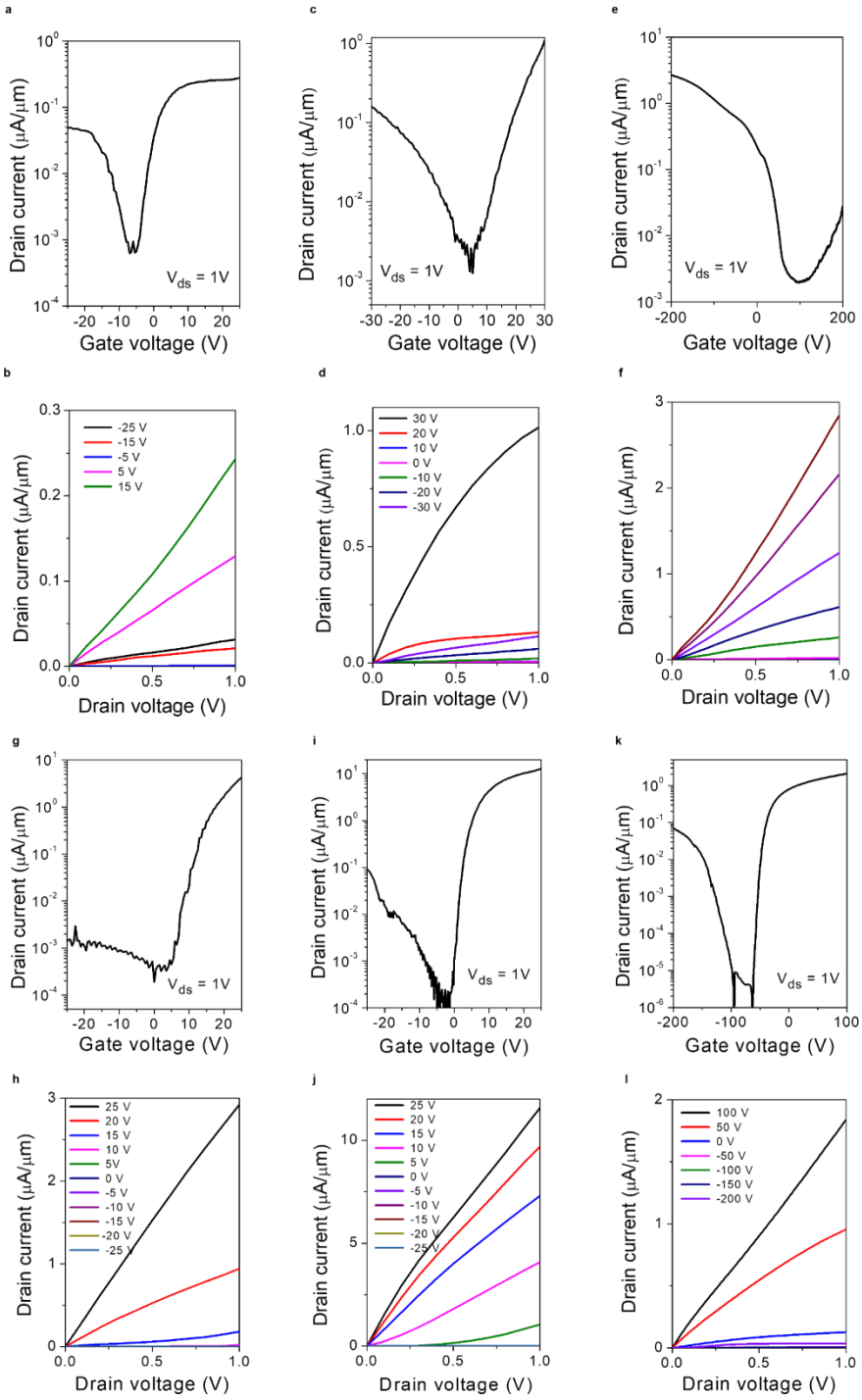
Extended Data Figure 5 | Pt on WSe_2 without optimized deposition parameters. a, Cross-sectional STEM of Pt/WSe_2 interface without optimization of the deposition conditions. **b,** Transfer curve of WSe_2 FET with damaged interface showing very poor p-type characteristics.



Extended Data Figure 6 | Device performance of MoS_2 with Pt contacts and WSe_2 with Pd contacts. a, Transfer curves for MoS_2 device with Pt contacts showing ambipolar characteristics with higher electron branch. W= 4 μm, L= 10 μm. **b**, Output curves of MoS_2 device with Pt contacts. **c**, Transfer curves of WSe_2 device with Pd contacts showing ambipolar characteristics with higher hole branch. W= 38 μm, L= 10 μm. **d**, Output curves of WSe_2 device with Pd contacts showing non-ideal characteristics.

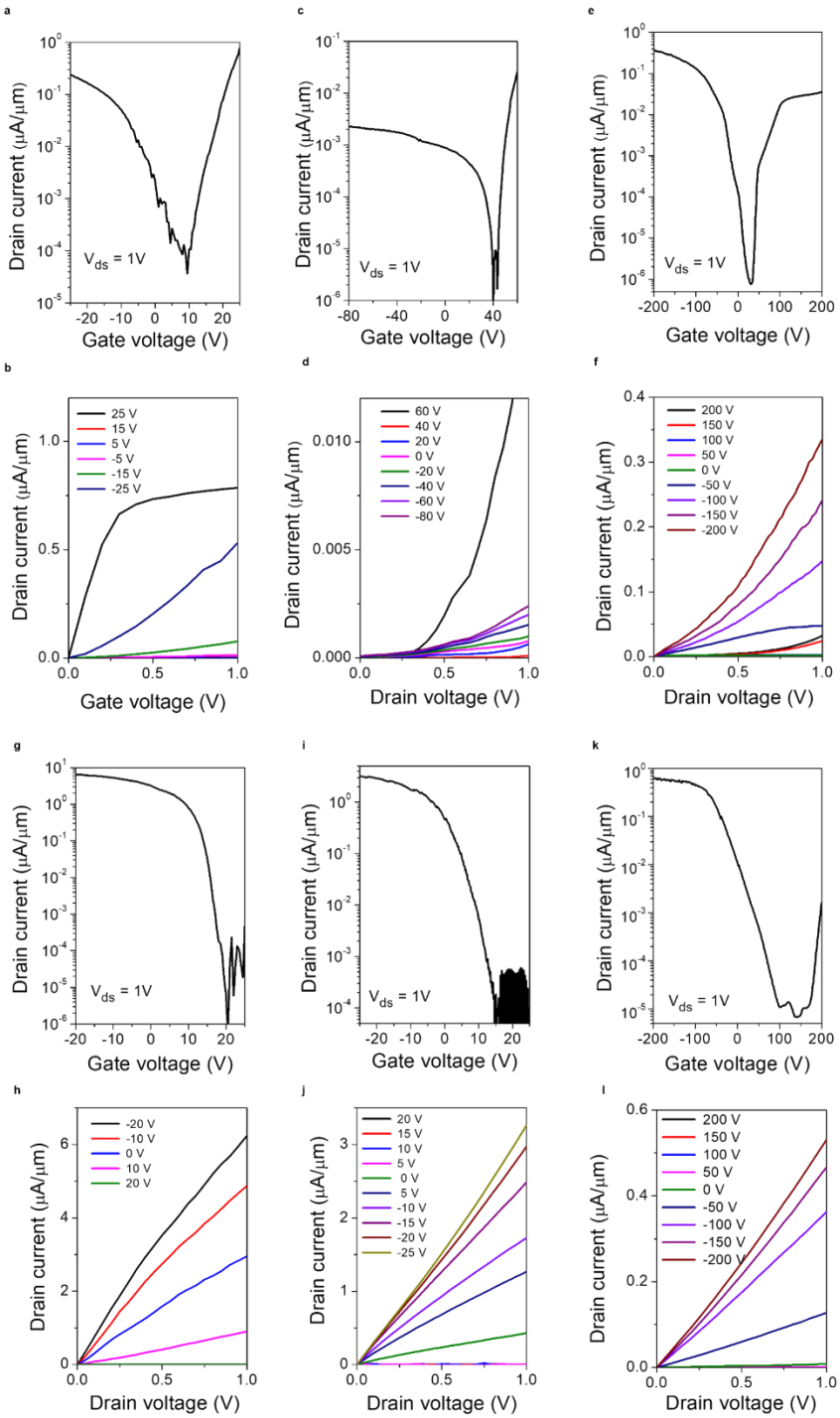


Extended Data Figure 7 | Work function measurements of Pd and Pt thin films on TMDs. **a,** AFM image of ~3 nm Pt deposited on cleaved MoS_2 crystal. **b,** Height profile of the blue line in the AFM image showing uniform growth of Pt on MoS_2. **c**, UPS result of Pd thin film on MoS_2 showing work function ~5.2 eV. **d**, UPS result of Pt thin film on WSe_2 showing work function ~5.0 eV.



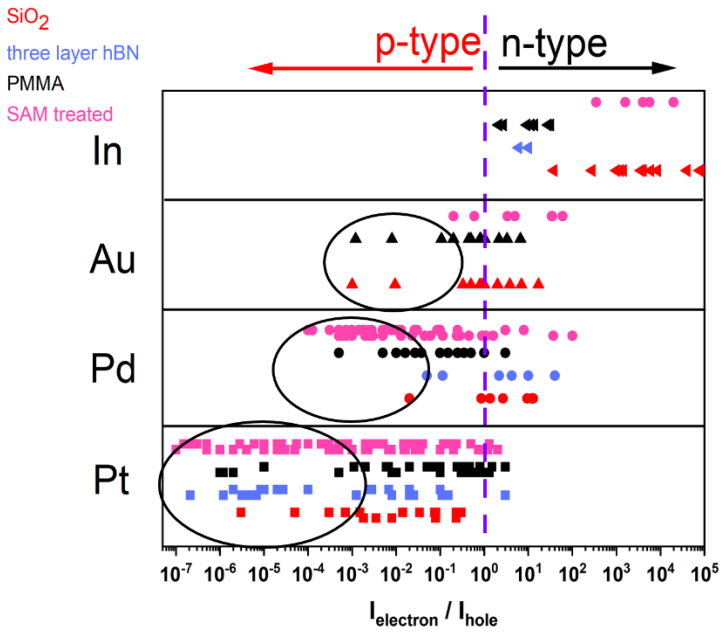
Extended Data Figure 8 | Properties of MoS_2 FETs with Pd (a-f) and Pt (g-l) contacts on different substrates. a,b, Transfer and output curves of MoS_2 FET with Pd contacts on SiO_2. W= 4 μm, L= 1 μm. **c,d,** Transfer curves of MoS_2 FET with Pd contacts on hBN. W= 3 μm, L= 1.5 μm. **e,f,** Transfer and output curves of MoS_2 FETs with Pd contacts on PMMA. W= 16 μm, L= 10

μm. **g,h,** Transfer and output curves of MoS_2 FET with Pt contacts on SiO_2. W= 6 μm, L= 0.8 μm. **i,j,** Transfer and output curves of MoS_2 FET with Pt contacts on hBN. W= 2.5 μm, L= 1 μm. **k,l,** Transfer and output curves of MoS_2 FET with Pt contacts on PMMA. W= 25 μm, L= 10 μm. It can be seen that Pd contacts lead to higher hole current for MoS_2 FETs compared to Pt contacts and the substrates have some influence on the hole injection level.

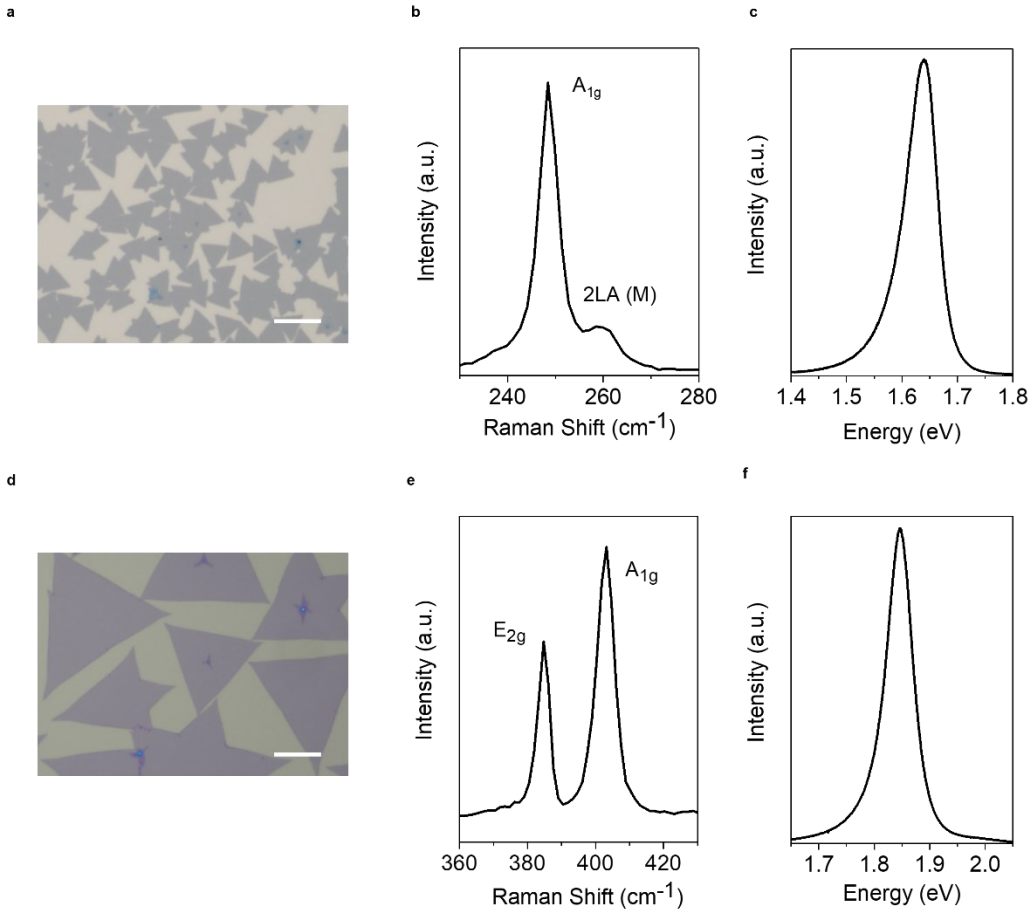


Extended Data Figure 9 | Properties of WSe_2 FETs with Pd (a-f) and Pt (g-l) contacts on different substrates. a,b, Transfer and output curves of WSe_2 FET with Pd contacts on SiO_2. W= 6.5 μm, L= 1 μm. **c,d,** Transfer and output curves of WSe_2 FET with Pd contacts on hBN. W= 6.5 μm, L= 0.8 μm. **e,f,** Transfer and output curves of WSe_2 FET with Pd contacts on PMMA. W= 25

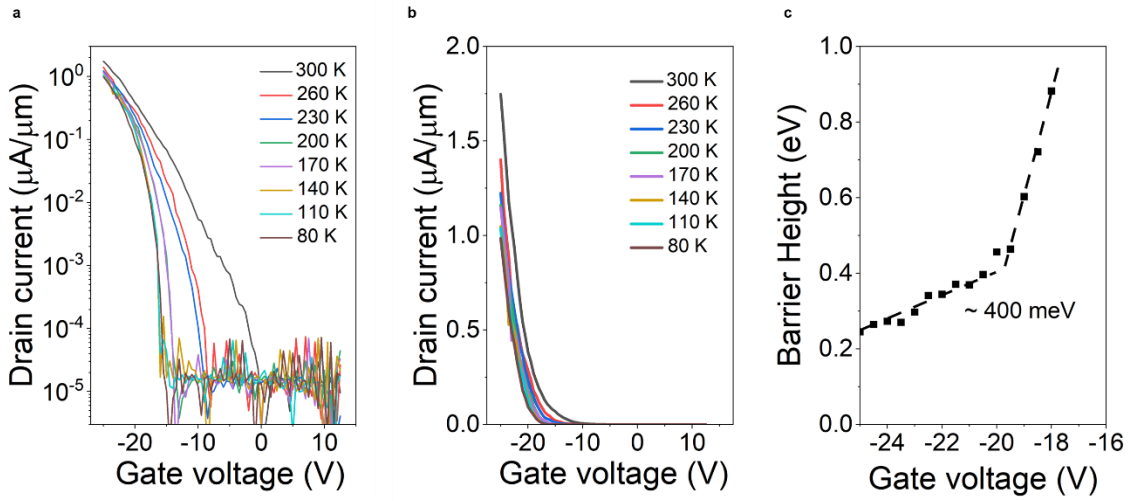
μm, L= 10 μm. **g,h,** Transfer and output curves of WSe_2 FET with Pt contacts on SiO_2. W= 4 μm, L= 0.8 μm. **i,j,** Transfer and output curves of WSe_2 FET with Pt contacts on hBN. W= 1.8 μm, L= 2.5 μm **k,l,** Transfer and output curves of WSe_2 FET with Pt contacts on PMMA. W= 5 μm, L= 10 μm. The results show poor p-type performance of WSe_2 FETs with Pd contacts on all different substrates.



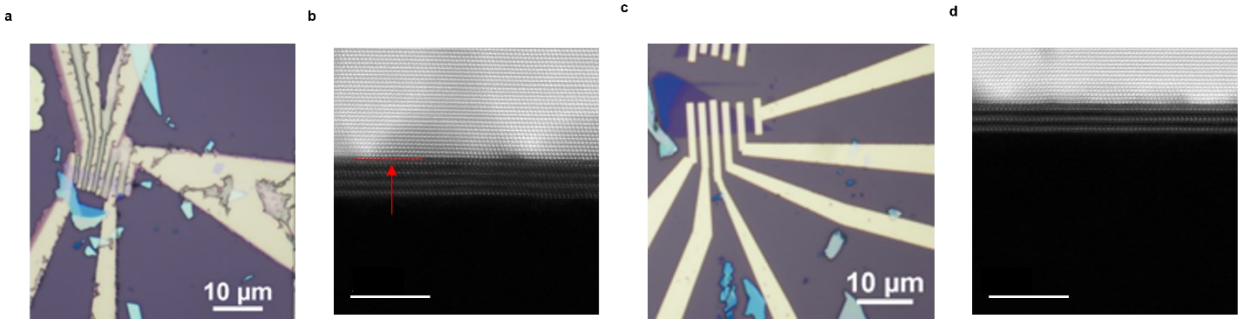
Extended Data Figure 10 | WSe_2 FETs with differnt contacts on different substrates. The scatter plots show the ratio of electron to hole current ($Ie_{lectron}/I_{hole}$) of WSe_2 FETs fabricated on different substrates (SiO_2, hBN, PMMA and SAM treated SiO_2 substrate) using different contacts (In, Au, Pd and Pt). The results excluded the p-type characteristics originate from SAM doping as the trend shows the polarity clearly varies with different contacts.



Extended Data Figure 11 | CVD grown WSe_2 and MoS_2. a, Optical image of CVD grown WSe_2 on SiO_2. Scale bar = 10 μm. **b**, Raman of WSe_2 showing pristine WSe_2. **c**, PL of monolayer WSe_2 showing a peak at ~ 1.65 eV. **d**, Optical image of CVD grown MoS_2 on SiO_2. Scale bar = 20 μm. **e**, Raman of MoS_2 showing pristine MoS_2. **f**, PL of MoS_2 with a peak at ~1.83 eV.



Extended Data Figure 12 | Schottky barrier height for monolayer WSe_2. a, Transfer curves of monolayer WSe_2 FET device with Pt contacts on SAM treated SiO_2 substrate measured at different temperatures. **b,** Transfer curves from **a** plotted linearly. **c,** The extracted Schottky barrier height for the monolayer WSe_2 is ~400 meV, which is 200 meV higher than multilayer WSe_2 FETs due to higher valence band edge of monolayer WSe_2.



Extended Data Figure 13 | The influence of deposition rate on metal/2D TMD interface. a, Optical microscope image of a device where the metal (Au in this case) was deposited at a deposition rate of 0.1 Å/s. To achieve 50 Å, the deposition was conducted for just over eight minutes. The radiative heat emitted from the evaporation crucible causes significant damage to the device. **b,** Cross-sectional atomic resolution ADF STEM image shows that the interface is damaged in this case (arrow indicating mixing of Au atoms with the S atoms of MoS_2. **c, d,** In

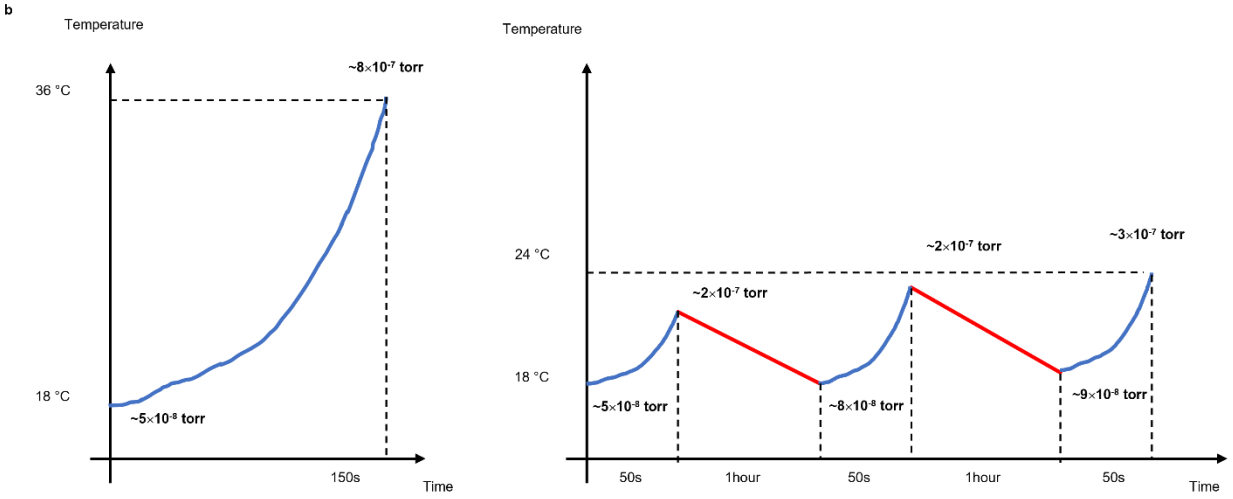
contrast, when the deposition is done quickly (deposition rate = 2 Å/s) and in multiple steps, the device is undamaged and the interface shown in panel **d** is ultra-clean.

a

0.1 Å/s for 100 Å	Current (mA)	Voltage (kV)	Time (s)	Energy (kJ)
Au	80	10	1000	**800**
Pd	85	10	1000	**850**
Pt	130	10	1000	**1300**

2 Å/s for 100 Å	Current (mA)	Voltage (kV)	Time (s)	Energy (kJ)
Au	92	10	50	**46**
Pd	95	10	50	**47.5**
Pt	150	10	50	**75**

b



Extended Data Figure 14 | Evaporation procedures for clean high work function contacts. a, Summary of e-beam evaporation current and voltage applied to deposit Au, Pd and Pt at 0.1 Å/s and 2 Å/s. The irradiation energy supplied to the device for high rate deposition is much lower than for low rate deposition. **b,** Comparison of substrate temperature versus time for 300 Å Pt depositions done in single and multiple steps. The left figure (single step deposition) shows that during deposition, the temperature of the holder gradually increases with time. For deposition with steps, the chamber and substrate holder were allowed to cool to room temperature before running the next deposition. Thus, the temperature of the sample remained lower than deposition without steps.

P-type characteristic of monolayer WSe_2 results								
Method	Channel length (μm)	EOT	Gate voltage (V)	Drain voltage (V)	I_{ON} (μA/um)	Mobility ($cm^2V^{-1}s^{-1}$)	Contact resistance (kΩ·μm)	ref
Clean vdW contacts, Pt	1.5	SiO_2	25	1	7.6	40	229 from TLM	This work
Pd contacts, with/o NO_2 doping	8	SiO_2	10	1	0.005 (undoped) 7 (doped)			[40]
Pt dry transferred contact encapsulated in BN							50 from R_{ON} extraction	[4]
With/o 4-NBD chemical doping						0.005 (undoped) 82 (doped)		[41]
TiPd	3		100	5	0.08			[42]
1T WSe_2 contact, phase transition		SiO_2	100	1	5	66		[43]
WSe_2 grown on hBN	1	hBN/ SiO_2	50	1	1	4.2		[44]
Nb doped WSe_2		SiO_2	80	1	0.79 (undoped) 17.88 (doped)	0.022 (undoped) 27 (doped)	10888 (without) 70.6 (doped)	[45]
V doped WSe_2						0.0005 (undoped) 3.5 (doped)		[46]

Note: 4-NBD is short for 4-nitrobenzenediazonium tetrafluoroborate.

Extended Data Table 1 | P-type characteristics of monolayer WSe_2 FETs

P-type characteristic of multilayer WSe_2 results								
Method	Channel length (μm)	EOT	Gate voltage (V)	Drain voltage (V)	I_{ON} (μA/um)	Mobility ($cm^2V^{-1}s^{-1}$)	Contact resistance (kΩ·μm)	ref
Clean vdW contacts, Pt	4	SiO_2	25	1	25.6	193	3.3	This work
Pt dry transferred contact encapsulated in BN	1		90	0.1	5	195	3.5	[4]
Dry transferred Pt	5	HfO_2/ Al_2O_3	2	1	13			[3]
Dry transferred Au	2	SiO_2	60	1	2	16		[13]
Dry transfer $NbSe_2$	4.5		50	0.6	1	17		[47]
Dry transferred Au contact +in situ defect healing			40	1	3 0.3 (evaporated)	148	9	[25]
Pt deposition		HZO/ Al_2O_3	3	1	0.2 (hole) 10 (electron)			[48]
Pd deposition + forming gas anneal		Al_2O_3	7	1	1			[49]
Edge contact, Pd	0.2	SiO_2	40	3	7			[50]
Pt bottom contacts with UV Ozone treatment			60	2	7	72.9	100	[31]
Pd contacts, O_2 plasma treatment	0.07			1	320 (device couldn't be turned off)		0.528 (four probe)	[51]
MoO_3 doping	5	SiO_2	50	1	1.5			[28]

Extended Data Table 2 | P-type characteristics of multilayer WSe_2 FETs

P-type characteristic of multilayer MoS_2								
Method	Channel length (μm)	EOT	Gate voltage (V)	Drain voltage (V)	I_{ON} (μA/um)	Mobility ($cm^2V^{-1}s^{-1}$)	Contact resistance (kΩ·μm)	ref
Clean vdW contacts, Pd	2	SiO_2	25	1	4.2	44	430	This work
MoOx contacts	8	SiO_2	15	1.5	0.131			[52]
Pt dry transferred contact, encapsulated in PMMA	13.5	PMMA/ SiO_2	60	0.1	0.9	175		[1]
$AuCl_3$ chemical doping		SiO_2	15	1	21	68	2.3	[53]
Plasma doping				5	1			[54]
Nb doped MoS_2					1	5		[55]
Nb doped MoS_2						7 (Hall mobility)		[56]
MoS_2 Fin FET, bottom Si++ contact		Top gate, SiO_2/HfO_2		1	50	10		[57,58]

Extended Data Table 3 | P-type characteristics of multilayer MoS_2 FETs