TFT Compact Modelling

Xiang Cheng, *Student Member*, IEEE, Sungsik Lee, *Member*, IEEE, Guangyu Yao, Arokia Nathan, *Fellow*, IEEE

***Abstract*—This paper reviews the major developments in thin-film transistor (TFT) modeling for the computer aided design (CAD) and simulation of circuits and systems. Following the progress in recent years on oxide TFTs, we have successfully developed a Verilog-AMS model called the CAMCAS model, which supports computer aided circuit simulation of oxide-TFTs, with the potential to be extended to other types of TFT technology families. Also reviewed are the features of SPICE and Verilog-AMS models and their comparison in terms of development complexity and execution speed. This is aimed at providing a guideline for researchers in the CAD area while enabling the choice of platform to implement their models.**

***Index Terms*— TFT compact models, SPICE, Verilog**

I. Introduction

The growing maturity of thin film transistor (TFT) technology coupled with newly emerging materials and processes are enabling integration of circuits and systems for a new family of applications ranging from bio-sensing systems to areas augmenting displays and imaging [1]–[4]. The design of systems places great demand for fast computer aided design (CAD) tools to accurately and reliably predict system behavior.

CAD always requires accuracy, high speed and reliable convergence of device models. In order to achieve high accuracy in all working regions without use of many fitting parameters, good understanding of device physics is needed. However, physical models are not necessarily sufficient for good CAD in the sense that the equations could be complex, which can lead to slow execution or convergence problems. Therefore, simplification of the model equations without sacrificing accuracy is one of the major requirements for a good CAD model. In addition, the model should be adaptive to a wide range of technological/process parameters through simple extraction procedures.

During the past 30 years, a great amount of effort has been made in the TFT modelling area for various semiconductor technologies, including amorphous silicon [5]–[11], polysilicon [10], organics [12]–[16] and metal oxides [17]–[23]. For a-Si TFTs, several SPICE models have been developed. Specifically the model developed by Rensselaer Polytechnic Institute, also known as the RPI model [10], has become a commercial standard supported by many simulation platforms including SmartSpice, HSPICE, Spectre, etc. However, no CAD tool for organic and metal-oxide TFTs has yet become a standard due to the rapid evolution in materials and device structures.

In this paper, we will review the major contributions to the TFT modeling area and compare the differences between Verilog-AMS and SPICE from the standpoint of compact device modelling. Finally, we present the implementation of the Cambridge TFT compact model [21] for oxide TFTs in Verilog-AMS for Spectre simulation. The major goal of this review is to give the reader guidelines for implementing device models for the CAD of circuits and systems.

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X. Cheng, S. Lee, G. Yao and A. Nathan are with Electrical Engineering Division, Department of Engineering, University of Cambridge, Cambridge CB3 0FA, U.K. (correspondence to sl684@cam.ac.uk, an299@eng.cam.ac.uk).

II. Physical and Empirical Modelling

Physical and empirical modelling approaches are generally aimed at providing an accurate model for a given transistor or transistor family, which covers all working regions of the device. While the major consideration is accuracy, the developed model is not necessarily physical. In this sense, it is theoretically possible to use polynomial approximation or other empirical ways to fit any kind of transistor behavior with acceptable accuracy. However, without proper understanding of the underlying device physics, the resulting number of fitting parameters could be large and difficult to extract from measurements since the model should cover a wide range of different bias conditions and transistor scales. Therefore, the transistor models used in a simulator are often a combination of terms and coefficients that are physically and empirically based.

Recent efforts have primarily focused on physically-based approaches in an attempt to develop simple and accurate models. The most well-studied material for TFTs is amorphous silicon (a-Si:H). Several models have been developed based on different distributions of deep states and tail states of the semiconductor to describe static and dynamic behavior for the above and sub-threshold regimes [9]–[11]. Other properties including trap related V_T shift [24] and the off/leakage currents [6]. The RPI model [10] captures most of the device properties leading to satisfactory simulation results, and thus has been widely used.

For organic TFTs, researchers have developed models based on multiple trapping and release (i.e. trap-limited conduction) [25] and variable range hopping (VRH) [13], [26], [27]. However, due to the diverse use of materials in the TFT, the underlying physics differs, and therefore a trend has emerged to develop a model that is unified but less physical [14].

As for metal oxide TFTs, modeling efforts are still in their

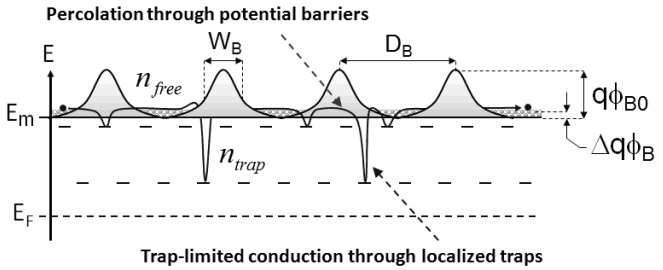


Fig 1 Illustration of carrier transport combining percolation with trap-limited conduction (TLC) for oxide semiconductor TFTs (Here, D_B and W_B denote spatial distance and width of potential barriers, respectively)

infancy, although there is growing interests in the area for implementation of circuits and systems. In what follows, early efforts in compact models for CAD of oxide TFTs are reviewed.

III. Summary of Cambridge's TFT Models

Compared with a-Si TFTs, the oxide system has unique properties, which need to be captured. For example, localized traps or band tail states in oxides do not exist to the same extent as a-Si [20]. Their tail state density is much lower and hence trap-limited conduction is generally insignificant [18], [20]. In addition, more complex systems such as amorphous indium gallium zinc oxide (a-IGZO) can have compositional disorder due to random distribution of metal constituents [18], [28]. This gives rise to potential barriers above the conduction band minima (E_m), suggesting the presence of percolation conduction [18], [20], [28].

In the following, compact models for the terminal current-voltage behavior are presented taking into account the different transport mechanisms in the device for the above- and sub-threshold regimes of TFT operation. The former is based on a mobility model that combines trap-limited conduction (TLC) with percolation conduction. The latter takes into account diffusion and drift current components [19]. A unified model is then presented that covers both regimes based on a single expression that uses a reference voltage V_{FB} rather than V_T [21]. Good agreement with measured terminal characteristics is obtained over the entire range of $V_{GS} > V_{FB}$ for the test TFTs with an a-IGZO channel.

A. Above-Threshold Model

As illustrated in Fig 1, oxide TFTs have potential barriers above E_m due to compositional disorder, suggesting percolation conduction when electrons are released into the conduction band. Moreover, there are localized tail states within the gap states, implying trap-limited conduction. In particular, oxide semiconductors can have a shallow slope of the tail states (kT_t) ~ 20meV, smaller than the thermal energy (kT) at 300K, leading to different mobility behavior. This suggests that the field effect mobility (μ_{FE}) model needs to be modelled based on TLC and percolation conduction, although the former is significant as compared to a-Si.

1) Trap-limited conduction (TLC)

Effect of trap-limited conduction (TLC) can be considered as ratio (γ_{TLC}) of free carrier density (n_{free}) and trapped carrier density (n_{tail}), yielding $\gamma_{TLC} = n_{free}/(n_{free}+n_{tail})$. Here, $n_{free} = N_C\exp[(E_F-E_m)/kT]$, where N_C is effective density of free carriers and kT the thermal energy. And the expression for n_{tail} is approximated with $kT_t < kT$ using exponential distribution of tail states. This yields $n_{tail} = N_{tc}kT_t\exp[(E_F-E_m)/kT]$. Now, we have γ_{TLC} as just a constant,

$$\gamma_{TLC} \equiv \frac{n_{free}}{n_{free}+n_{tail}} \approx \frac{N_C}{N_C + N_{tc}kT_t}. \quad (1)$$

2) Percolation Conduction

Percolation conduction associated with potential barriers above E_m can be considered as mobility scaled from band mobility (μ_0), assuming Gaussian random distribution of potential barriers with mean (ϕ_{B0}) and variance (σ_{B0}). This yields $\mu_0^* = \mu_0\exp[-q\phi_{B0}/kT+(q\sigma_{B0})^2/(kT)^2]$. Here, ϕ_{B0} can be reduced by $\Delta\phi_{B0}$ due to thermally released electrons, depending on Fermi level change (ΔE_F), as described in Fig 1. The thermally reduced barrier height can be expressed as $\phi_{B0}\cdot\exp(-\gamma_B\Delta E_F/kT)$, where $\gamma_B \equiv (D_B-W_B)/D_B$, which can be approximated as $\phi_{B0}(1-\gamma_B\Delta E_F/kT)$ when $\gamma_B\Delta E_F/kT<<1$ by Taylor expansion. Thus, $\Delta\phi_{B0}$ is defined as $\gamma_B\Delta E_F/kT\phi_{B0}$. These conditions yield the percolation mobility (μ_{Per}) as follows,

$$\mu_{Per} \equiv \mu_0 \exp\left(-\frac{q(\phi_{B0}-\Delta\phi_B)}{kT}+\frac{(q\sigma_{B0})^2}{2(kT)^2}\right), \quad (2)$$
$$= \mu_0^* \exp\left(\frac{\gamma_B\Delta E_F}{kT}\phi_{B0}\right)$$

where $\mu_0^* = \mu_0\exp[-q\phi_{B0}/kT+(q\sigma_{B0})^2/2(kT)^2]$ considered as an effective band mobility.

3) Combined Mobility Model with V_{GS} dependence

In Eq.(2), the ΔE_F is controlled by gate voltage (V_{GS}). The relationship between them can be derived by solving Poisson's equation, yielding $\Delta E_F=2(kT/q)\ln[C_{ox}(V_{GS}-V_T)/Q_{ref}]$, where C_{ox} is gate-insulator capacitance, V_T threshold voltage, and $Q_{ref} \equiv [2\varepsilon_S N_C kT\exp[(E_{F0}-E_m)/kT]^{0.5}$. Combining TLC with percolation from Eqs.(1) to (2), we now have the V_{GS} dependent mobility relation,

$$\mu_{FE} \equiv \mu_{Per}\gamma_{TLC}$$
$$= \mu_0^*\left(\frac{N_C}{N_C+N_{tc}kT_t}\right)\left(\frac{C_{ox}}{Q_{ref}}\right)^{\alpha_p}(V_{GS}-V_T)^{\alpha_p} \quad (3)$$

As can be seen, Eq.(3) follows a power law. Here, $\alpha_p \equiv 2q\phi_{B0}\cdot\gamma_B/kT$, related to percolation. In Eq.(3), TLC affects the constant term, while the exponent is determined by percolation.

4) Current-Voltage Relation

With Eq.(3) and the definition of drift current: $I_{DS} = \mu_{FE}C_{ox}(V_{GS}-V_T-V_{ch})dV_{ch}/dx$, current-voltage relation $I_{DS}(V_{GS})$ can be derived with the integral ranges: x=0 to L and channel potential (V_{ch})=0 to V_{DS},

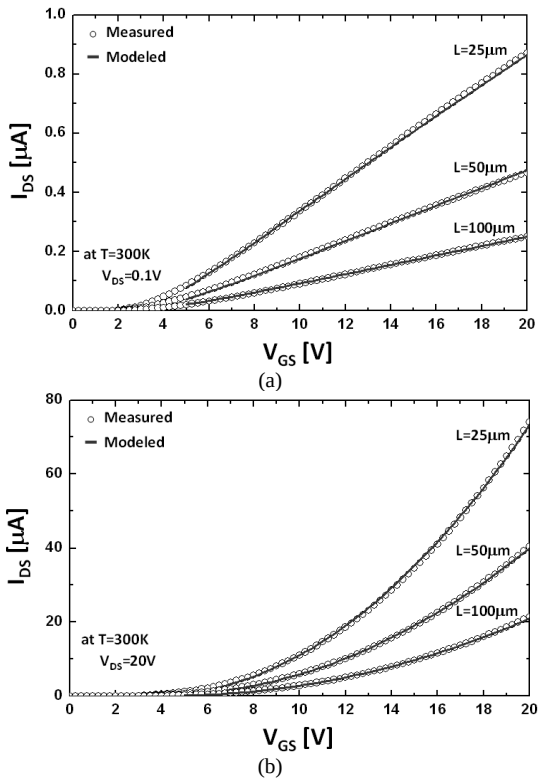


Fig 2 Comparison between measured and modeled transfer characteristics (I_{DS} vs. V_{GS}) for above-threshold regime, (a) linear regime with a small drain voltage (V_{DS}) of 0.1V and (b) saturation regime with a high V_{DS} of 20V, respectively. For each regime, a good agreement between measurement and modeling is achieved.

$$I_{DS} \equiv \mu_0^* \left(\frac{N_C}{N_C + N_{tc} kT_t} \right) \frac{W}{L'} \frac{C_{ox}^{\alpha_p+1}}{Q_{ref}^{\alpha_p}} (V_{GS} - V_T)^{\alpha_p+1} V'_{DS} \cdot \quad (4)$$

In Eq.(4), L' is defined as L-ΔL, where ΔL is channel expansion, and effective drain voltage $V'_{DS} = V_{DS} - 2R_C I_{DS}$, where R_C is contact resistance. For saturation regime expression, Eq.(4) can be reformed with a saturation parameter (β_{sat}), replacing V'_{DS} by $\beta_{sat}(V_{GS}-V_T)$. Fig 2(a) shows a comparison between measured and modeled transfer characteristics (I_{DS} vs. V_{GS}) at V_{DS}= 0.1V, providing a good agreement. The measured saturation characteristics at V_{DS}= 20V is also well matched with the modeled results, as seen in Fig 2(b).

To check the model validity for temperature dependency, we measured and simulated the drain current as a function of gate bias for different temperatures, e.g. 100K, 200K, and 300K, respectively. As seen in Fig.3(a), there is good agreement between the measurements and the model, Eq.(4). For purposes of validation, the modeled values of exponent (α_p) in the power-law, Eq.(4), are compared with the extracted values from the best fit since it has a unique signature of percolation conduction, i.e. $a = \alpha_p + 1 \equiv 2q\phi_{B0}\cdot\gamma_B/kT + 1$). As seen in Fig.3(b), the proposed percolation model for $\phi_{B0}\cdot\gamma_B$ = 2.5 meV shows better agreement compared to the conventional model (e.g. trap-limited conduction model with $a = 2kT_t/kT - 1$ for kT_t = 30 meV).

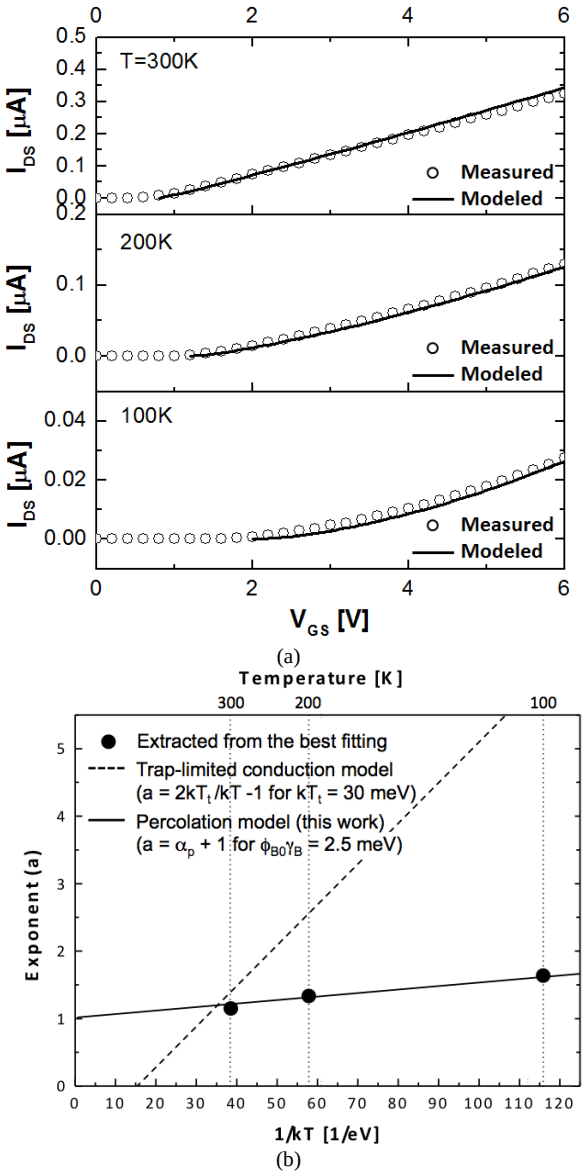


Fig. 3 (a) Measured and modeled I_{DS}-V_{GS} for above-threshold regime at V_{DS} =0.1V for different temperatures (100K, 200K, 300K, respectively). (b) Retrieved exponent (a) vs. temperature. Here, the proposed model shows a better agreement compared to the conventional model (e.g. trap-limited conduction model).

B. Sub-Threshold Model

The sub-threshold current in the limit of low V_{GS} shows a linear dependence on V_{GS} in a semi-log plot, as illustrated in Fig 4, suggesting diffusion current, as follows,

$$I_{Diff} \approx \mu_0 \frac{kT}{q} \frac{W}{L'} Q_{fi} \exp\left(\frac{q}{kT} \left(\frac{V_{GS} - V_{FB}}{1 + q^2 D_{it} / C_{ox}} \right) \right) \left(1 - \exp\left(-\frac{qV'_{DS}}{kT} \right) \right), \quad (5)$$

where μ_0 is the band mobility for electrons. Note that the sub-threshold slope (S) can be derived from Eq.(5) with the definition $dV_{GS}/d\log I_{DS}$,

$$S \equiv \ln 10 \frac{kT}{q} \left(1 + \frac{q^2 D_{it}}{C_{ox}} \right). \quad (6)$$

As described in Fig 4, interface states are occupied first, followed by filling deep states located in the bulk at higher V_{GS}.

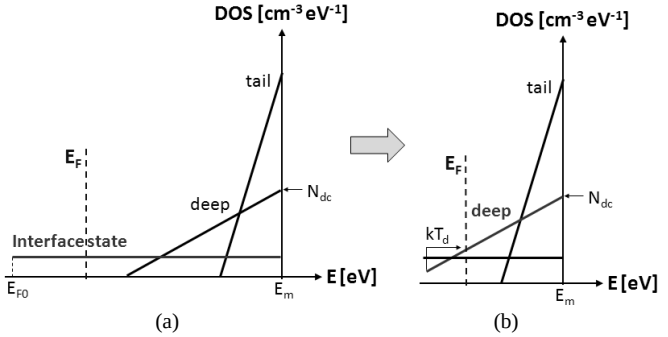


Fig 4 Density of states profile with (a) Fermi level within interface states at low gate voltage, and (b) the case of deep states dominant with increasing gate voltage corresponding Fermi level now within deep states.

Table I Extracted Sub-Threshold Parameters at T=300K

Parameters	Value
S	0.19 V/dec
D_{it}	$1.64\text{x}10^{11}$ $cm^{-2}eV^{-1}$
I_{off}	$2\text{x}10^{-14}$ A
Q_{fi}	$7.05\text{x}10^{-14}$ C/cm^2
α_d	2.26
T_d	639K
Q_d	$7.8\text{x}10^{-8}$ C/cm^2

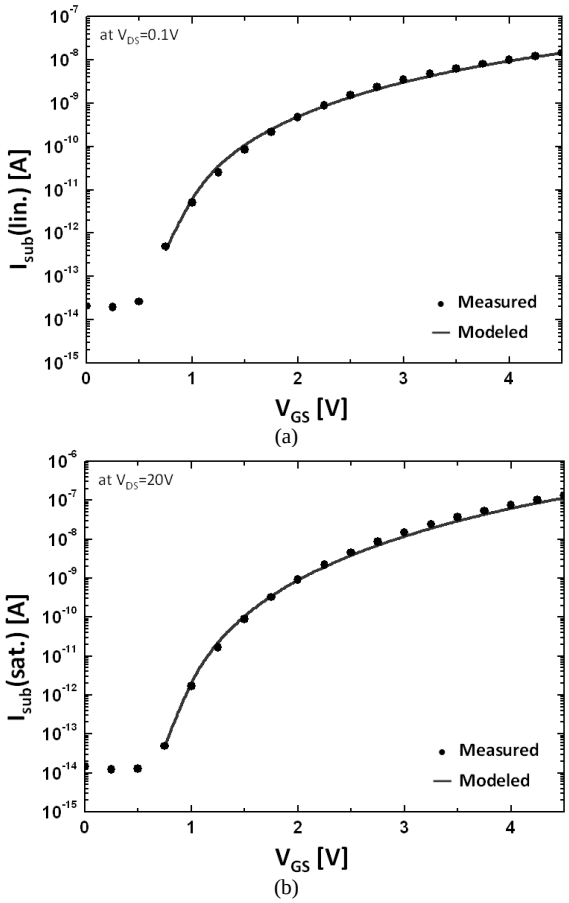


Fig 5 Measured and modeled sub-threshold current (I_{sub}) as a function of V_{GS} for (a) linear regime with V_{DS}=0.1V and (b) saturation regime with V_{DS}=20V

So, As the E_F moves to the location of deep states for increasing V_{GS}, the drain current can be defined as a drift current (I_{Drift}),

$$I_{Drift} \approx \mu_0 \frac{W}{L'} \frac{C_{ox}^{\alpha_d+1}}{Q_d^{\alpha_d}} (V_{GS} - V_{FB})^{(\alpha_d+1)} V'_{DS}, \qquad (7)$$

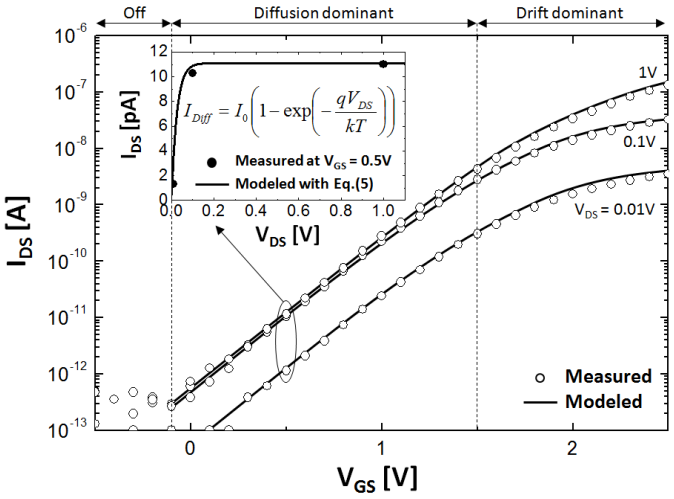


Fig. 6. Measured and modeled I_{DS} vs. V_{GS} at sub-threshold regime for a different V_{DS}. Inset: Measured and modeled I_{DS} vs. V_{DS} for V_{GS} = 0.5V. Here, the equation is simplified from Eq. (5) introducing the pre-constant I_0 which is around 10pA at V_{GS} = 0.5V.

where Q_d is a reference charge density associated with deep states, α_d is power-law exponent defined as $2(T_d/T-1)$, and T_d is the characteristic temperature of deep states.

We now have the current-voltage relations for both diffusion and drift components as given by Eqs.(6) & (7). These equations can be combined as a total drain current (I_{sub}) in the sub-threshold regime using a harmonic average,

$$I_{sub} \equiv (I_{Diff}^{-m} + I_{Drift}^{-m})^{-1/m}, \qquad (8)$$

The examined TFT to verify this model, which is the same as that used in the previous sections, has the following geometrical and physical parameters (extracted in the previous sections): W=100μm, L=100μm, channel thickness t_S=40nm, channel permittivity $\varepsilon_S = 11.5\varepsilon_0$ (where ε_0 is vacuum permittivity), V_{FB} ~0.6V, V_T ~4V, C_{ox} = 11.5 nF/cm^2, μ_0 = 15 cm^2/V-s, and $N_C=5\text{x}10^{18}$ cm^{-3} at 300K. As we extracted in the previous section 5.1, $2R_C \equiv R_{SD}$ = 9637 Ω for W = 100 μm (equivalent to $R_{SD}W$ = 96.37 Ω-cm) and ΔL=-3.5μm (L'=L-ΔL=L+3.5μm). Other extracted model parameters are summarized in Table I. Fig 5 shows the measured sub-threshold characteristics for a different V_{DS}, providing a good agreement with each other.

To validate the sub-threshold model in terms of the diffusion component in the examined transistors, we measured the drain current for small V_{DS}=0.01, 0.1, and 1V. Comparing to the model, we get good agreement as seen in Fig.6. In particular, as shown in the inset of Fig.6, the measured I_{DS} vs. V_{DS} at the diffusion dominant regime of V_{GS} (e.g. V_{GS} = 0.5V) is compared with the Eq.(5). Here, the dependence of the drain current on V_{DS} is found to follow the law of $(1-\exp(-qV_{DS}/kT))$ of Eq.(5) which is a signature of the presence of the diffusion current.

Regarding continuity and symmetry of the compact model where above- and sub-threshold models are combined, the model was subject to the Gummel symmetry test (GST) [22], [29]. As seen in the inset of Fig.7(a), V_X represents a symmetrical voltage applied on source and drain sides, respectively. Fig.7 demonstrates perfect continuity and

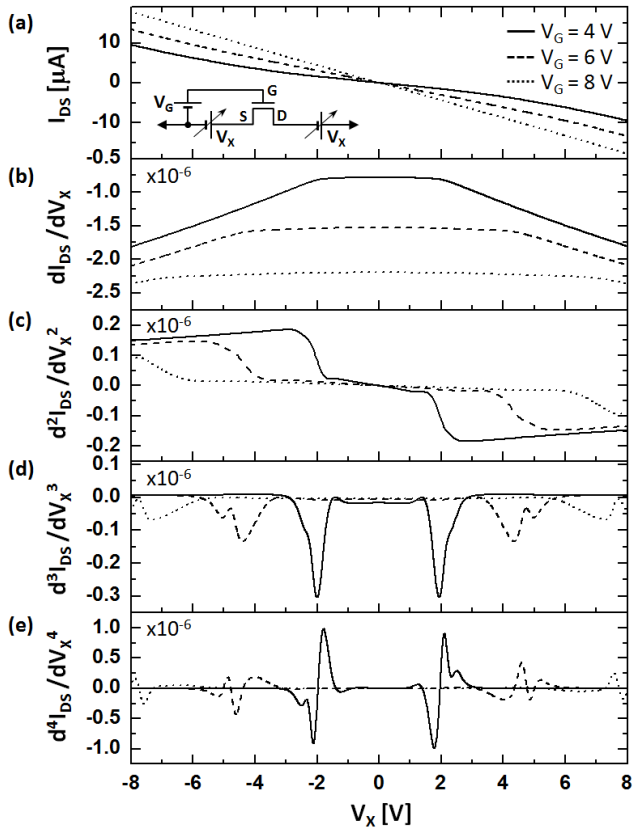


Fig.7. (a) Calculated I_{DS} vs. V_X of the combined above- and sub-threshold model for different V_G (4, 6, 8V). (b) First, (c) second, (d) third, and (e) fourth derivatives of I_{DS} with respect to V_X. The inset of (a): test circuit configuration of the GST.

symmetry as a function of V_X even for the 4th derivative of I_{DS} with respect to V_X, suggesting it has successfully passed the GST. For this, we employed smoothness and continuity functions for the effective drain voltage and threshold voltage terms [30].

C. Unified Model

As seen in the previous sections II & III, the current-voltage relation needs to be derived separately to describe the sub-threshold and above-threshold characteristics. Here, we need separate expressions for the sub-threshold and above-threshold regimes, implying two different equation systems to describe total current (see Fig. 8Fig). Moreover, in this case, threshold voltage (V_T) is not immediately apparent from the I-V plot and needs to be extracted from above-threshold region of the characteristic as a fitting parameter. However, the extracted value of V_T can be quite different depending on extraction method and the I-V data range chosen for the fit. In contrast, turn-on- voltage (V_{FB}) is the gate voltage (V_{GS}) at which drain current (I_{DS}) starts increasing rapidly, thus it is easy to identify V_{FB} on a semi-log plot of I_{DS} vs. V_{GS}.

We can unify this to cover both sub-threshold and above-threshold characteristics. The proposed unified model is a single expression with a reference voltage level V_{FB} rather than V_T, providing good agreement with measured terminal characteristics over the entire range of $V_{GS} > V_{FB}$ for the test TFTs with an amorphous InGaZnO (a-IGZO) channel, which is the same TFT used in the previous sections. The derived

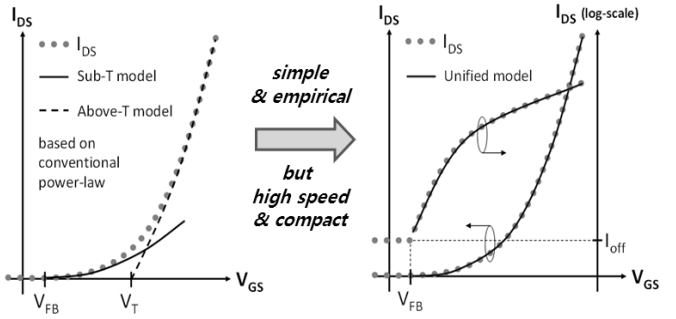


Fig.8. (a) Schematic I_{DS} vs. V_{GS} curves (gray circles) with the conventional power-law models for sub-threshold (Sub-T, solid line) and above-threshold (Above-T, dot line) characteristics. In this case, we need two models for these two different operational regimes. Here, V_{FB} and V_T are on-voltage and threshold voltage, respectively. (b) Schematic I_{DS}-V_{GS} curves (gray circles) with only one model: unified model which can cover sub-threshold as well as above-threshold regimes at the same time.

Table II Extracted Parameters for Unified Model at T=300K

Parameters	Value
G_0	2.34x10^{-5}ohm^{-1}
κ	-10.812 V$^{-\alpha}$
α	-0.675

equation for this model is as follows,

$$I_{DS} = G_0\left(\frac{W}{L'}\right)\exp\left(\kappa(V_{GS}-V_{FB})^{\alpha}\right)V'_{DS} + I_{off}, \qquad (9)$$

where $G_0 = \mu_0(\varepsilon_S kTN_C)^{1/2}$, $\kappa = \zeta/2kT$, and ζ & α are related to trap states. The extracted model parameters are summarized in Table II.

Fig 9 shows modeled results for different L (=25, 50, and 100μm), providing good agreements with the measured characteristics. Also, they exhibit small average errors < 5% over a wide range of V_{GS} from 5 to 20V. Interestingly, the proposed model using only one equation covers both the sub- and above-threshold regimes at the same time. This is mainly due to a combination of the exponential function and power-law. Additional advantage of this unified model is that it just needs a few model parameters to be implemented in model code description, e.g. Veriog-A, thus providing a higher-speed simulation.

IV. Computer Interpretation of Device Model

After having established an accurate analytical model for the TFT, computer implementation for circuit simulation is not always easy. Several considerations including speed, convergence and even the way of translating different form of equations into computer language should be taken into consideration in this step.

For a-Si TFTs, several SPICE models have been developed. Specifically the model developed by Rensselaer Polytechnic Institute, also known as the RPI model [10], has become a commercialized standard supported by many simulation platforms including SmartSpice, HSPICE and Spectre, etc.

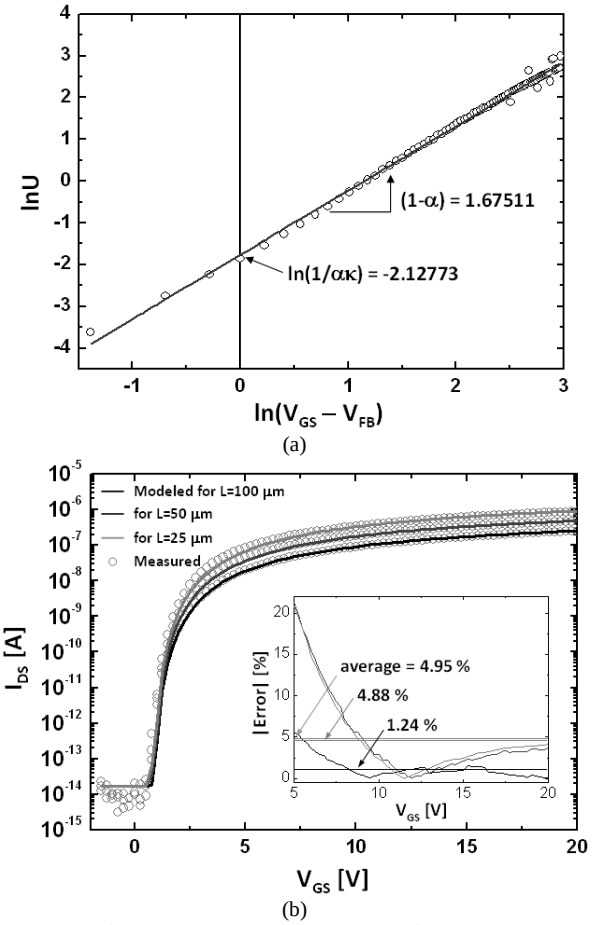


Fig. 9 (a) Plots of lnU vs. ln(V_{GS}-Von). Here, linear fitting is applied over the entire range of ln(V_{GS}-V_{FB}). (b) Modeled results for different L in comparison with the measured curves using a unified model, showing average error less than 5%.

However, CAD of organic and metal-oxide TFTs is yet to become a standard due to the rapid and ongoing evolution in materials and device structures. In fact, and as mentioned previously, there is a quest for unifying the TFT model to meet simulation requirements of TFTs with ever changing structures and materials.

It is important to understand the benefits and drawbacks of SPICE and Verilog-A, while developing a device model to be used in further circuit simulation and system design.

A. SPICE

SPICE is an open source analogue circuit simulation software firstly developed at the University of California, Berkeley [31]. The first two versions of this simulator was written in Fortran. SPICE2 included several elements widely used in circuit simulation at that time, including the diode, MOSFET, JFET and BJT, etc. In 1989, a version of the simulator SPICE3 was re-written in C. This version includes the well-known BSIM model [32].

Many commercial circuit simulators today are based on the aforementioned software including PSPICE, HSPICE, SmartSpice, Spectre, etc. The fast simulation speed, high accuracy and ease of use make the SPICE simulator extremely popular in the area of circuit design. However, SPICE is written in a low level computer language (Fortran or C) and so are the models used in it. Therefore, researchers should not only have a good understanding of device physics but also need enough knowledge of the algorithms and limitations of the simulator. The procedure for developing a stand-alone SPICE model (not by combining existing elements) always takes time and resources. Due to the complexity of model development in SPICE, currently only well developed and widely used devices are having SPICE models.

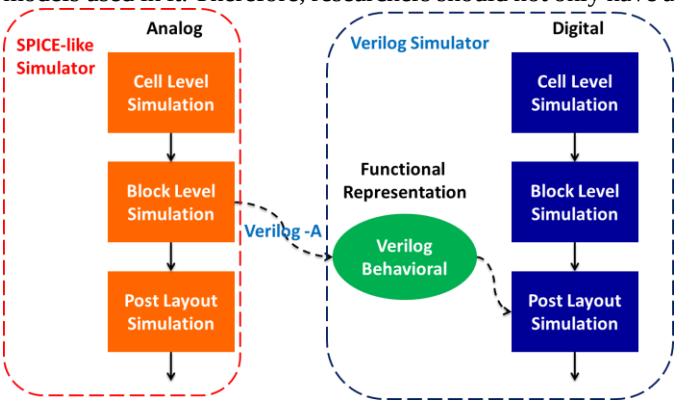


Fig.10 Verilog-A behaviour model in early mixed signal simulation environment

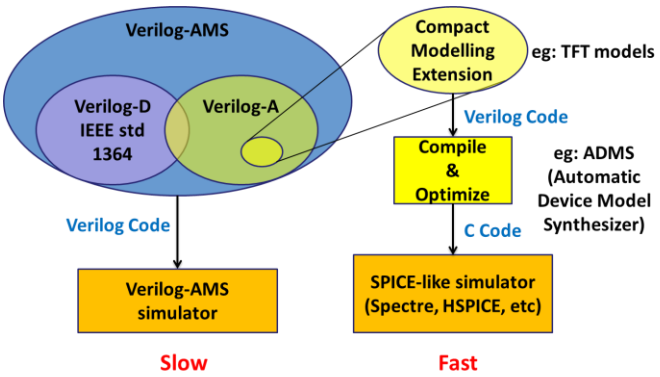


Fig.11 Verilog-A(MS) extension for compact modelling with SPICE like simulator integration

It is worth noting that modern circuit simulators use a heavily modified original SPICE model but they separate as much as possible the simulation algorithm from the device model. For example, the Spectre simulator provides a Spectre Compiled Model Interface (CMI) for Spectre developers and others to use C code directly for device modelling.

B. Verilog

The Verilog Hardware Description Language (Verilog HDL) was designed in 1984 to meet the design demands of VLSI engineers working in the higher abstractive level to increase the number of transistors in simulating digital circuits. Subsequently adopted by Cadence Design Systems and Open Verilog International, VHDL has become an IEEE standard in 1995, i.e. IEEE Std 1364-1995 [33].

Since the original Verilog language did not support analogue systems, the extensive use of HDL languages led to a growing

Table III Comparison between different model languages

	SPICE	Spectre CMI	Verilog-AMS
Language	C/Fortran	C	Verilog
Language level	Low	Low	High
Easy to use	No	No	Yes
Efficiency & Speed	High	High	Low
Complexity	High	High	Low
Simulator information needed for developers	Simulation algorithm & limitations	Simulator limitation on equations	None
Users	SPICE developers	CAD engineers, Cadence programmers	End users

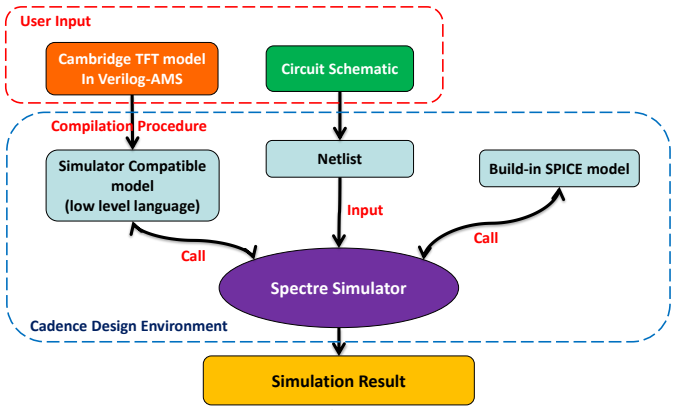


Fig. 12 Circuit design and simulation flow using CAMCAS model in Cadence Design Environment

demand for high-level behavioral model for systems and components for use in analogue and mixed signal system design. Thus, Verilog-AMS standard was then developed by Accellera to include Verilog-A, a previously standalone behavioral language used for analogue modeling in Spectre, and extending both the digital part of the IEEE Std 1364 and the analogue part of Verilog-A [34].

In the early days of Verilog-A and Verilog-AMS, the behavior model was limited in terms of accuracy for analogue devices. The language was first developed for design of systems and thus the behavioral language was at that time not intended for complex physical equations at the device level. Fig. 10 illustrates the mixed signal simulation environment in early days. In addition, device modelling often led to long execution times compared with SPICE models. Even so, the capability of behavioral modelling started to attract the attention of device modelers struggling with low level implementation.

In 2002, the open-source tool supporting automatic conversion [35] of Verilog-AMS models to C codes was introduced. Since then, several proposals have been made to use Verilog-AMS to efficiently develop compact device models [36], [37] to integrate with SPICE like simulators. The report in 2010 [38] showed comparable performance of their Verilog-AMS device model against SPICE. The language has

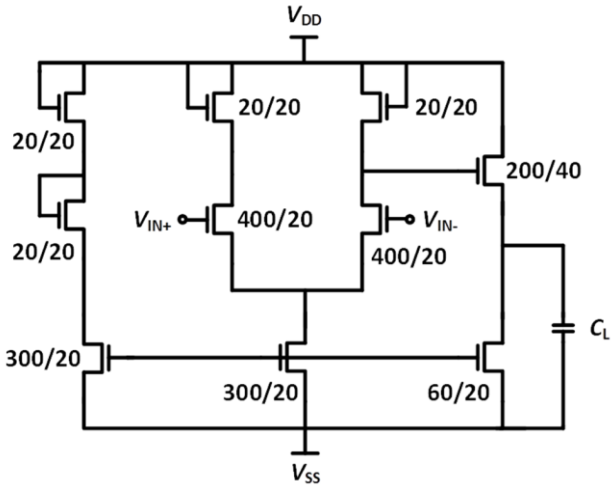


Fig. 13 A voltage amplifier used in simulation with CAMCAS model

now become a major tool for device model developers. Fig. 10 illustrates the relation between different Verilog languages and the simulation flow in two types of simulators.

C. *Short Summary of Comparison*

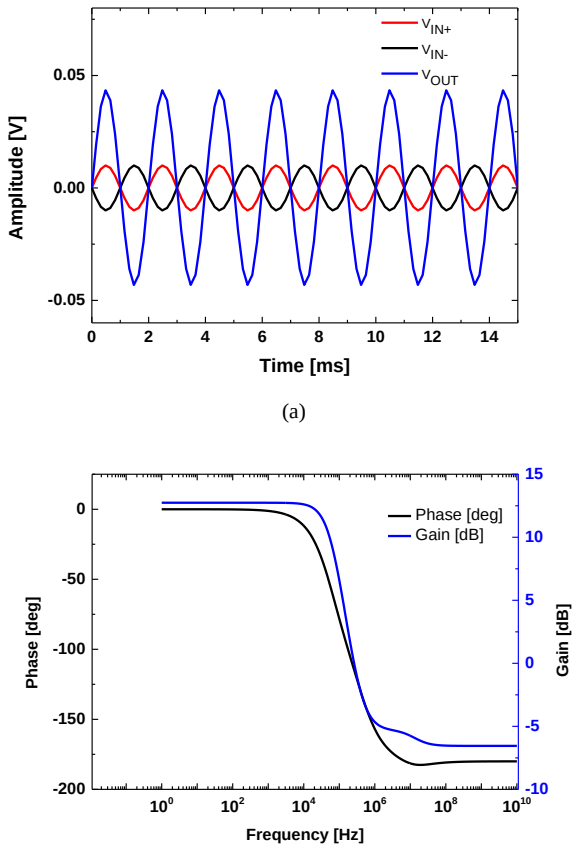
Table III summarizes the comparison of different model languages. The SPICE model development based on a low level language is only used by model developers of components, which are not likely to change (due to heavy usage or technology maturity) in view of resource requirements.

In the meantime, the Verilog approach is ideally suited to meet the modelling demands of ever-changing TFT or other device structures without requiring a mature physical understanding of the devices or underlying material system. The direct implementation of physical equations in Verilog-AMS will dramatically reduce the time between development of new devices and subsequent circuit simulation.

Despite all the benefits of Verilog-AMS, the model is still slower and less efficient than a well-developed SPICE model, due to the fact that the Verilog-AMS model should be converted to a lower level language form. The converted form although automatically optimized by the synthesizer (e.g. ADMS [35]) cannot be as efficient as a SPICE model because the latter is optimized directly in a lower level language. Therefore, it is recommended to use SPICE for circuit simulation whenever it could offer sufficient accuracy. On the other hand, Verilog-AMS is suited for devices that are new or under-development.

V. THE CAMCAS MODEL IN SIMULATION ENVIRONMENT

As discussed before, we implement the Cambridge's TFT compact model (i.e. CAMCAS model) directly into Verilog-A language for use in a Cadence Design Environment so as to focus on developing a more accurate model for circuit simulations. The simulation flow in the Cadence Design



(a)

(b)

Fig. 14 Simulation results of the voltage amplifier (a) Transient analysis for small signal amplitude at input and output (b) ac analysis for gain and phase

Environment is shown as Fig.12.

The user extracts processing parameters based on the measurement results of their own devices and incorporates them into the CAMCAS Verilog-AMS model. In addition, the user can change the form of equations for better fitting to measurement results. Thus circuit designers can use the usual route of circuit design by simulating their TFT circuits before fabrication analogous to using the SPICE model in Cadence Spectre.

Fig.13 shows an example of an IGZO TFT circuit simulated using the CAMCAS model in Cadence Spectre. The simulation results show a voltage gain of 12dB in both transient and ac simulation as shown in Fig.14(a) and (b), respectively.

VI. Conclusion

Physically-based compact models play an important role in computer-aided circuit design and simulation. This paper reviews the major contributions in TFT analytical modelling and compares the pros and cons of SPICE and Verilog-AMS from the standpoint of device model development. Brief guidelines are provided to decide on choice of modelling language for implementation of models and to understand how models work within the simulator.

Regarding the device models, oxide TFTs are considered and two different approaches are reviewed. While considering physical and material properties of oxide semiconductors, both above- and sub-threshold models have been presented. In particular, the above-threshold model uniquely addresses carrier transport properties in oxide TFTs, such as percolation conduction along with trap-limited conduction. Thus it is a fully-physical model. Also, using a harmonic average technique, diffusion and drift current components have been seamlessly combined to describe sub-threshold current behavior, providing good agreement with measurements. Using a different, more empirical-based approach, a unified model is discussed that covers both sub- and above-threshold regimes with a single expression. This model provides higher speed circuit simulation since it has only a few number of parameters. The results presented here are essential for oxide circuit design and simulation, providing designers with a preference for fully physical but slower simulations on the one hand, and higher speed but less model complexity on the other.

The CAMCAS model described above is implemented in Verilog-AMS, and the validity of the approach is demonstrated by way of a voltage amplifier circuit simulation.

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References

[1] R. Chaji and A. Nathan, *Thin Film Transistor Circuits and Systems*. Cambridge University Press, 2013.

[2] S. Lee, S. Jeon, R. Chaji, and A. Nathan, "Transparent semiconducting oxide technology for touch free interactive flexible displays," *Proc. IEEE*, vol. 103, no. 4, pp. 644–664, 2015.

[3] S. Jeon, I. Song, S. Lee, B. Ryu, S. E. Ahn, E. Lee, Y. Kim, A. Nathan, J. Robertson, and U. I. Chung, "Origin of high photoconductive gain in fully transparent heterojunction nanocrystalline oxide image sensors and interconnects," *Adv. Mater.*, vol. 26, no. 41, pp. 7102–7109, 2014.

[4] A. Nathan, S. Lee, S. Jeon, I. Song, and U. Chung, "Amorphous Oxide TFTs: Progress and Issues," *SID Symp. Dig. Tech. Pap. Inf. Disp.*, vol. 43, no. 1, pp. 1–4, 2012.

[5] H. Aoki, "Dynamic characterization of a-Si TFT-LCD pixels," *IEEE Trans. Electron Devices*, vol. 43, no. 1, pp. 31–39, 1996.

[6] K. S. Karim, P. Servati, N. Mohan, A. Nathan, and J. A. Rowlands, "VHDL-AMS modeling and simulation of a passive pixel sensor in a-Si:H technology for medical imaging," in *ISCAS 2001. The 2001 IEEE International Symposium on Circuits and Systems (Cat. No.01CH37196)*, vol. 5, pp. 479–482.

[7] K. Khakzar and E. H. Lueder, "Modeling of amorphous-silicon thin-film transistors for circuit simulations with SPICE," *IEEE Trans. Electron Devices*, vol. 39, no. 6, pp. 1428–1434, Jun. 1992.

[8] L. Resendiz, B. Iniguez, a. Estrada, and a. Cerdeira, "Modification of amorphous level 15 AIM SPICE model to include new subthreshold model," *2004 24th Int. Conf. Microelectron. (IEEE Cat. No.04TH8716)*, vol. 1, pp. 16–19, 2004.

[9] T. Leroux, "Static and dynamic analysis of amorphous-silicon field-effect transistors," *Solid. State. Electron.*, vol. 29, no. 1, pp. 47–58, Jan. 1986.

[10] M. S. Shur, "SPICE Models for Amorphous Silicon and Polysilicon Thin Film Transistors," *J. Electrochem. Soc.*, vol. 144, no. 8, p. 2833, 1997.

[11] M. Shur, M. Hack, and J. G. Shaw, "A new analytic model for amorphous silicon thin-film transistors," *J. Appl. Phys.*, vol. 66, no. 7, p. 3371, 1989.

[12] G. Horowitz and P. Delannoy, “An analytical model for organic-based thin-film transistors,” *J. Appl. Phys.*, vol. 70, no. 1, p. 469, 1991.
[13] M. C. J. M. Vissenberg and M. Matters, “Theory of the field-effect mobility in amorphous organic transistors,” vol. 57, no. 20, p. 13, 1998.
[14] M. Estrada, A. Cerdeira, J. Puigdollers, L. Reséndiz, J. Pallares, L. F. Marsal, C. Voz, and B. Iñiguez, “Accurate modeling and parameter extraction method for organic TFTs,” *Solid. State. Electron.*, vol. 49, no. 6, pp. 1009–1016, Jun. 2005.
[15] M. Fadlallah, W. Benzarti, G. Billiot, W. Eccleston, and D. Barclay, “Modeling and characterization of organic thin film transistors for circuit design,” *J. Appl. Phys.*, vol. 99, no. 10, p. 104504, 2006.
[16] A. Valletta, A. S. Demirkol, G. Maira, M. Frasca, V. Vinciguerra, L. G. Occhipinti, L. Fortuna, L. Mariucci, and G. Fortunato, “A compact Spice model for organic TFTs and applications to logic circuit design,” in *2015 IEEE 15th International Conference on Nanotechnology (IEEE-NANO)*, 2015, pp. 1434–1437.
[17] H.-H. Hsieh, T. Kamiya, K. Nomura, H. Hosono, and C.-C. Wu, “Modeling of amorphous InGaZnO[sub 4] thin film transistors and their subgap density of states,” *Appl. Phys. Lett.*, vol. 92, no. 13, p. 133503, 2008.
[18] S. Lee, K. Ghaffarzadeh, A. Nathan, J. Robertson, S. Jeon, C. Kim, I. H. Song, and U. I. Chung, “Trap-limited and percolation conduction mechanisms in amorphous oxide semiconductor thin film transistors,” *Appl. Phys. Lett.*, vol. 98, 2011.
[19] S. Lee, S. Jeon, and A. Nathan, “Modeling Sub-Threshold Current–Voltage Characteristics in Thin Film Transistors,” *J. Disp. Technol.*, vol. 9, no. 11, pp. 883–889, Nov. 2013.
[20] S. Lee and A. Nathan, “Localized tail state distribution in amorphous oxide transistors deduced from low temperature measurements,” *Appl. Phys. Lett.*, vol. 101, 2012.
[21] S. Lee, D. Striakhilev, S. Jeon, and A. Nathan, “Unified Analytic Model for Current–Voltage Behavior in Amorphous Oxide Semiconductor TFTs,” *IEEE Electron Device Lett.*, vol. 35, no. 1, pp. 84–86, Jan. 2014.
[22] Z. Zong, L. Li, J. Jang, N. Lu, and M. Liu, “Analytical surface-potential compact model for amorphous-IGZO thin-film transistors,” *J. Appl. Phys.*, vol. 117, no. 21, p. 215705, 2015.
[23] C. Perumal, K. Ishida, R. Shabanpour, B. K. Boroujeni, L. Petti, N. S. Munzenrieder, G. A. Salvatore, C. Carta, G. Troster, and F. Ellinger, “A compact a-IGZO TFT model based on MOSFET SPICE Level=3 template for Analog/RF circuit designs,” *IEEE Electron Device Lett.*, vol. 34, no. 11, pp. 1391–1393, 2013.
[24] A. a. Fomani and A. Nathan, “Metastability mechanisms in thin film transistors quantitatively resolved using post-stress relaxation of threshold voltage,” *J. Appl. Phys.*, vol. 109, no. 8, p. 084521, 2011.
[25] B. G. Horowitz, “Organic Field-Effect Transistors,” no. 5, pp. 365–377, 1998.
[26] C. H. Kim, A. Castro-Carranza, M. Estrada, A. Estrada, Y. Horowitz, G. Horowitz, and B. Iniguez, “A compact model for organic field-effect transistors with improved output asymptotic behaviors,” *IEEE Trans. Electron Devices*, vol. 60, no. 3, pp. 1136–1141, 2013.
[27] L. L. L. Li, H. Marien, J. Genoe, M. Steyaert, and P. Heremans, “Compact Model for Organic Thin-Film Transistor,” *IEEE Electron Device Lett.*, vol. 31, no. 3, pp. 210–212, 2010.
[28] S. Lee, Y. Yang, and A. Nathan, “Modeling Above-Threshold Current-Voltage Characteristics in Oxide TFTs for Display Pixel Circuits,” *Dig. Tech. Pap. Int. Symp. Disp. Week 2013, SID (Society Inf. Display) Symp.*, vol. 44, no. 1, pp. 22–25, 2013.
[29] “IEEE Recommended Practices #P1485 on: Test Procedures for Micro-electronic MOSFET Circuit Simulator Model Validation,” 1997. [Online]. Available: http://electronica.ugr.es/~amroldan/modulos/investiga/material_restringido/estandar_medida_mos.pdf.
[30] G. H. See, X. Zhou, K. Chandrasekaran, S. Ben Chiah, Z. Zhu, C. Wei, S. Lin, G. Zhu, and G. H. Lim, “A compact model satisfying Gummel symmetry in higher order derivatives and applicable to asymmetric MOSFETs,” *IEEE Trans. Electron Devices*, vol. 55, no. 2, pp. 624–631, 2008.
[31] L. W. Nagel and D. O. Pederson, “SPICE (Simulation Program with Integrated Circuit Emphasis),” *No ERLM382Electronic Res. Lab.*, vol. Memorandum, pp. 1–4, 1973.
[32] B. J. Sheu, D. L. Scharfetter, P.-K. Ko, and M.-C. Jeng, “BSIM: Berkeley short-channel IGFET model for MOS transistors,” *IEEE Journal of Solid-State Circuits*, vol. 22. pp. 558–566, 1987.
[33] IEEE, *Verilog IEEE Std 1364-1995*. 1996.
[34] H. Verilog, “Verilog-AMS Language Reference Manual,” *Eda-Stds.Org*, 2014.
[35] L. Lemaitre, C. McAndrew, and S. Hamm, “ADMS-automatic device model synthesizer,” *Proc. IEEE 2002 Cust. Integr. Circuits Conf. (Cat. No.02CH37285)*, pp. 27–30, 2002.
[36] L. Lemaitre, G. Coram, C. McAndrew, and K. Kundert, “Extensions to Verilog-A to support compact device modeling,” *Proc. 2003 IEEE Int. Work. Behav. Model. Simul.*, 2003.
[37] M. A. Chalkiadaki, C. Valla, F. Poullet, and M. Bucher, “Why- and how- to integrate Verilog-A compact models in SPICE simulators,” *Int. J. Circuit Theory Appl.*, vol. 41, no. July 2012, pp. 1203–1211, 2013.
[38] G. Depeyrot, “Verilog-A Compact Model Coding Whitepaper,” *Memory*, vol. 2, no. June, pp. 821– 824, 2010.