Supplementary Materials

for

Sub-threshold Schottky-barrier thin film transistors with ultralow power and high intrinsic gain

Sungsik Lee and Arokia Nathan*

Electrical Engineering Division, Department of Engineering, University of Cambridge, 9 JJ Thomson Avenue, Cambridge CB3 0FA, UK

*Corresponding author. Email: an299@cam.ac.uk

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Materials and Methods

MM1. Overall TFT Fabrication Procedure
The fabrication process of the TFTs reported here is as follows. Starting with the glass wafer, RF-sputtering is performed for molybdenum (Mo) deposition to be used as the gate electrode. Here, the work-function of Mo is assumed to be 5eV (25). This is followed by wet etching to pattern it for the desired geometry. Then SiOx and SiNx were layered using plasma enhanced chemical vapor deposition (PECVD). The total film thickness is 350nm and is used as the gate insulator. The TFT semiconducting channel was a 50nm-thick IGZO deposited using RF-sputtering with an IGZO ceramic target (Fig.S1A), subsequently patterned by RIE. In the sputter deposition, the oxygen-gas partial pressure against Ar, i.e. O2/(O2+Ar) was 4% and 15% to realize two test TFT structures, in which each was annealed at 250 °C, and 450 °C, respectively. Then an etch-stop layer (ESL) is formed using SiOx to protect the IGZO, followed by dry etching to define source/drain contact area. As the final metallization, 150nm-thick molybdenum is deposited with RF sputtering, and patterned with wet etching. The device is then passivated with a 200nm-thick SiNx/SiOx, and patterned by wet etching to define the via holes. This is followed by another thermal annealing at 450 °C for all the samples (26). The detailed processing steps on IGZO and Mo are discussed in the following sections. Electrical characteristics were measured using a standard semiconductor analyzer – KEITHLEY.

MM2. Detailed IGZO Film Deposition Procedure and Its Large Area Processability
Detailed procedure of the IGZO deposition is as follows:
1) Starting with an IGZO ceramic target, RF sputtering with Ar plasma was performed to get a 50nm-thick IGZO. The IGZO ceramic target used has a composition - In2O3:Ga2O3:ZnO=1:1:2, and its equivalent atomic composition is In:Ga:Zn:O = 1:1:1:4 (27), as seen in Fig.S1A.
2) During the sputtering, the vacuum level in the chamber was kept at about 6 mTorr while supplying oxygen flow, i.e. oxygen partial pressure, Pox = O2/(O2+Ar) with fixed Ar flow at 50 sccm. Here, we varied Pox for two cases: 4% and 15%.
3) Then the samples were thermally annealed (at 250°C and 450°C) for an hour in oxygen ambient followed by patterning, S/D metallization, and passivation steps. The S/D metallization process is detailed in section MM7.

Note that the IGZO TFT process used is applicable to a variety of large area applications, such as displays (27).

MM3. Oxygen Partial Pressure Effect on Microstructure and Electrical Performance
The target used here is for an amorphous phase IGZO film formation, and its composition riches in ZnO (28). And the ZnO-rich IGZO film is usually having a high reactivity with oxygen, hence the sputtering performed here is a reactive process (Fig.S1A) (28,29). Thus, the IGZO films would react well at higher oxygen partial pressure, leading to a less disordered film in terms of defects, e.g. oxygen vacancies (Vox), as seen in the inset of Fig.S1A (7,28). As mentioned in MM2, thermal annealing in oxygen ambient was performed to further stabilize the film structure. The oxygen ambient helps suppress
possible oxygen reduction during the thermal annealing (29). These processes affect the electrical properties such as carrier density and mobility. As seen in Fig.S1B, the electron concentration was reduced by almost an order of magnitude when $P_{\text{oxy}}$ was increased from 4% to 15%. This can be explained with the reduction of $V_{\text{oxy}}$ states which act as electron donors (Fig.S1A) (19,20). At the same time, the electron mobility (from Hall measurements) was decreased. Note that, for the case of conducting oxides, e.g. IGZO, it is known that the carrier mobility is proportional to carrier density (27) hence influencing the ON-state current in the I-V characteristics (Fig.S3A).

**MM4. Our IGZO TFT Process Window**
From our experimental results and analysis discussed in section MM3, the process window for an IGZO TFT (as labeled in a red shade within Fig.S1B), may be wide enough to include the two cases for 4% and 15% the oxygen partial pressure. As seen in Fig.S1B, the carrier density is changed from $\sim5\times10^{18}$ to $\sim5\times10^{17}\text{cm}^{-3}$. These levels are reasonable for the active layer in a FET structure. In other words, this range is amenable to be modulated by gate bias. However, if $P_{\text{oxy}}$ is too low or too high, the film’s conductivity would be too high (very conductive, even degenerate) or too low (i.e. very resistive) to be used as an active layer in FETs. Note that this window would be varied depending on the IGZO target specification.

**MM5. Discussions on a Stoichiometric Behaviour of LC- and MC-IGZO Films**
In general, a sputtered IGZO film would have an oxygen reduction issue during sputtering (1-7,27-30). This suggests oxygen composition would be less than ideal while oxygen vacancies are generated (30). In order to minimize this, a high oxygen-gas flow (i.e. oxygen partial pressure, $P_{\text{oxy}}$) would be employed (31). Here, we believe that this oxygen-gas flow would help to approach the desired stoichiometric composition ($\text{In:Ga:Zn:O = 1:1:1:4}$) given from our target specification ($\text{In}_2\text{O}_3:Ga_2\text{O}_3:ZnO=1:1:2$). An important consideration for $P_{\text{oxy}}$ is its level/range needs to be determined for optimal electrical performance as discussed in the previous section MM4. We used 4% and 15% as representatives for less compensated (LC) and more compensated (MC) characteristics, respectively. The corresponding carrier density for each $P_{\text{oxy}}$ was reasonable and sufficient for the FETs’ active layer, as discussed in the section MM3 and MM4. Since $P_{\text{oxy}}$ is compensating the $V_{\text{oxy}}$ states which are electron donors, as discussed in the previous section MM3 and Fig.S1A, the $V_{\text{oxy}}$ states are reduced according to the oxygen 1s peaks, confirming their correlation with the reduction of electron density (Fig.S1C).

**MM6. Process Window / Transition from LC to MC**
Within the process window of the IGZO TFT (seen in Fig.S1B), a demarcation level of $P_{\text{oxy}}$ between LC and MC needs to be determined, and this depends on the electrical performance discussed in section MM4. In other words, if $P_{\text{oxy}}$ is very low, the film is much less compensated, but too conductive to be a semiconductor. And if $P_{\text{oxy}}$ is very high, the film would be very much compensated, but too resistive to be a semiconductor either. In this respect, we defined the transition from LC to MC with the observation of an order change in electron density. Based on this, as seen in Fig.S1C, we proposed that the range
at around 4% is for LC-IGZO while that at around 15% is for MC-IGZO, as discussed in section MM5.

**MM7. Detailed Source / Drain Metal Deposition Procedure and Contact Properties**

As seen in Figs. S2A-S2D, we tested four different samples as discussed in MM2: (A) 4% P\textsubscript{ox} and 250°C annealing, (B) 4% P\textsubscript{ox} and 450°C annealing, (C) 15% P\textsubscript{ox} and 250°C annealing, and (D) 15% P\textsubscript{ox} and 450°C annealing, respectively. These conditions were applied before the Molybdenum (Mo) metallization. The detailed procedure for the Mo metallization by RF sputtering is as follows:

1) The Mo target used here was >99% purity, which was loaded in the chamber vacuum with ~10 mTorr vacuum. The deposited thickness of the Mo film was 150nm.
2) Photo-lithographic patterning with wet etching followed.
3) The device was then encapsulated with SiO\textsubscript{x}, followed by another thermal annealing step at 450°C for 20 min. This additional annealing was commonly used across all four samples. This post-metallization annealing helps with achieving a more reliable contact property (26).

These processes with conditions as listed in A to D determine whether the device is Schottky or ohmic. Sample ‘A’ shows the best ohmic characteristics among all samples albeit with the poorest SS as seen in Fig.S2E and S2F, respectively (see also Table S1). As described in Fig.S2A, the carrier density is high due to the reduced compensation of V\textsubscript{ox}, thus making a narrower SB narrower while reducing E\textsubscript{C}-E\textsubscript{F}. In addition, a higher trap density at the semiconductor surface and/or at the interface between Mo and IGZO is expected because of the lower annealing temperature, confirming its larger SS in Fig.S2E and Table S1. This suggests that trap-assisted tunneling played a key role in achieving a more reliable ohmic contact as seen in Fig.S2F (31). Case ‘B’ is in a similar situation in terms of the V\textsubscript{ox} compensation and carrier density, but less defective at the surface / interface since it was annealed at higher temperature. This is consistent with the results in Fig.S2E and Table S1. This suggests that device ‘B’ would still have an ohmic contact (weakly Schottky) although it was annealed at a higher temperature (Fig.S2F). Device ‘C’ was subject to the same annealing temperature as ‘A’, but yielded a better SS (Fig.S2E and Table S1). This can be attributed to the higher P\textsubscript{ox} and its role in reducing interfacial states. At the same time, its conductivity is less due to the higher P\textsubscript{ox} (15%) because of the higher compensation of V\textsubscript{ox}, leading to a wider SB (yielding a Schottky contact) compared to cases A and B. However, there may be interfacial traps thus introducing weak quasi-ohmic characteristics. These results are consistent with the observations presented in Fig.S2G. Case ‘D’ shows clear Schottky contact characteristics (Fig.S2G), and concurrently providing a steeper SS than any of the other test devices. Again, this can be attributed to the high P\textsubscript{ox} as well as the high temperature annealing. These results go to show that the P\textsubscript{ox}, rather than thermal annealing, determines the overall contact property.
**Supplementary Text**

**ST1. TFT Technologies and their OFF-State Characteristics / Power Consumption**

Existing TFT technologies are unlikely to meet the low power and high intrinsic gain requirements because of the typically high bias current (micro-ampere) and limited signal amplification (i.e. intrinsic gain of a few tens), which is insufficient to process weak signals at the nano-ampere level (13-16). Moreover, the OFF-current of other TFT technologies is higher due to their narrower band-gap compared to IGZO, thus producing a higher power consumption in their OFF-state. Indeed, according to the literature (1-8, 13-16), LTPS, a-Si, organics, and oxides (e.g. IGZO) technologies have > 10^{-12}, ~10^{-12}, ~10^{-12}, and <10^{-13} amperes as their OFF-current, respectively (Table S2). Clearly the IGZO TFT’s OFF-current is the lowest (8). For an estimation of power consumption ($P_{out}$), the theoretically-achievable minimum $P_{out}$ would be $I_{OFF}V_{DD}$, where $V_{DD}$ is the supply voltage and $I_{OFF}$ is the OFF-current. As reported in this paper, the Schottky barrier can also be incorporated with other semiconductor families for a high performance (e.g. high gain) in spite of operating in the deep sub-T regime where their OFF-current level (determined by their band-gap), would eventually determine the minimum achievable power consumption.

**ST2. Detailed Performance Comparison between LC and MC IGZO TFTs**

The IGZO-based SB-TFTs were fabricated using different oxygen gas partial pressure against argon gas, i.e. $P_{ox} = O_2/(O_2 + Ar)$ of 4% and 15% for the LC and MC IGZO, respectively. Fig.S3A shows transfer characteristics where the sub-threshold slope (SS) of the MC-IGZO TFT (~0.28 V/dec) was lower than that of the LC-IGZO TFT (~0.34 V/dec). This result suggests that defects in the IGZO film were reduced with the higher $P_{ox}$. This can be explained with the following empirical relation (22),

\[ SS = \ln(10) \frac{kT}{q} \left( 1 + \frac{q^2 D_t}{C_{ox}} \right), \]  

where $kT$ is the thermal energy, $q$ the elementary charge, $C_{ox}$ the gate insulator capacitance per cm$^2$, and $D_t$ the defect density per eV and cm$^2$. Indeed, the $D_t$ value of the MC IGZO is found to be $4.7 \times 10^{12}$ cm$^2$eV$^{-1}$, which is more than 30% reduced compared to $6.8 \times 10^{12}$ cm$^2$eV$^{-1}$ of the LC device. In addition, both $V_{ref}$ and $V_T$ of the MC IGZO TFT were positive and greater than those of the LC device, suggesting a decrease of the film conductivity. Here, the threshold voltage ($V_T$) for each device was extracted using the linear extrapolation method (Fig.S3B) (32). These findings confirm that the $V_{ox}$ states, acting as electron donors, were reduced (1-7, 19, 20). Thus, the MC device appeared to be operating in the enhancement mode, and its operating current, especially in its deep sub-T regime, ranges from pico- to nano-ampere levels within a small voltage range < 1 volt associated with the smaller SS, as shown in blue shade in Fig.1C. This smaller SS leads to the higher $g_m$ (Eq.S2, Fig.1D) (21,22), which is important to achieve high amplification factor. The intrinsic gain ($A_i$) of the transistor $A_i = g_m r_o$, where $r_o$ is output resistance at the saturation regime (16-18) and is the other important parameter to achieve high $A_i$. In the measured output current-voltage characteristics (i.e. $I_{DS}$ vs.$V_{DS}$), as seen in Fig.1B, the MC-IGZO TFT shows nonlinear characteristics at a low $V_{DS}$ whereas the LC device shows the usual ohmic characteristics.
ST3. Effect of Schottky Contact on Above-Threshold Operation in TFTs

As discussed in the sections MM3 - MM5 under the ‘Materials and Methods’, the film’s conductivity was reduced by a higher $P_{ox}$ to get Schottky characteristics. As a result, the electron mobility has also been reduced, as seen in Fig.S1B. Although the mobility concept is not a matter for the sub-T regime operation, it leads to lower current when $V_{GS}$ is increased. Indeed, as seen in Fig.1D, this was observed in the MC-IGZO device. Although the MC device has steeper SS compare to the LC device in the deep sub-T regime, the current level and SS more rapidly degrades when $V_{GS}$ approaches $V_T$ and is even more in the ON-state. This can be explained with the reduced electron mobility.

ST4. Relationship between SS and $g_m$

From a simple exponential current-voltage relation, the following empirical relation can be stated for $g_m$ in the sub-threshold regime (22),

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{I_0 \ln(10)}{SS} \exp \left( \frac{V_{GS} - V_{ref}}{SS \ln(10)} \right), \quad (S2)$$

where $I_0$ is the reference current at $V_{GS}=V_{ref}$. As seen in Eq.S2, $g_m$ is increased with decreasing SS. This is consistent with the results in Figs.1D and 1E.

ST5. Modeling of Ohmic Device and Related Analysis and Discussions

The output current of the ohmic device has much higher dependency on $V_{DS}$ through a channel length modulation ($\delta L$) since it follows drift-diffusion transport where $L-\delta L$ comes in at saturation (Eq.S3) (21). In shorter channel-length ($L$) devices, this effect is more visible. Indeed, the ohmic device with $L=10 \mu m$ shows a smaller $r_o$ compared to the device with $L=20 \mu m$ whereas the $r_o$ of the SB-TFT is found to be almost independent on $L$ as shown in Fig.1B. The current-voltage relation in the saturation regime of the ohmic device is represented as,

$$I_{sat}(Ohmic) = \frac{W}{L-\delta L(V_{DS})} I_{sat0} \exp \left( \frac{V_{GS} - V_{ref}}{SS \ln(10)} \right), \quad (S3)$$

where $I_{sat0}$ is a reference saturation current normalized with $W/L$, and $\delta L$ is a channel length modulation factor as a function of $V_{DS}$. In Eq.S2, $\delta L$ is extended with increasing $V_{DS}$ while increasing with the current as $\delta L=A^*V_{DS}^{0.5}$. This is derived from the depletion width of a reverse-biased diode. Here, $A^*$ is a constant. This gives the equation for $r_o$ as a function of $V_{DS}$ and $L$,

$$r_o(Ohmic) \approx \frac{L}{L + A^* \sqrt{V_{DS}}} r_o(ideal), \quad (S4)$$

where $r_{o(ideal)}$ is the ideal output resistance without $V_{DS}$ and $L$ dependency. Indeed, the ohmic contact has a much higher $L$-dependency as seen in Fig.1D. This mainly originates from the diffusion current dominant ohmic device since diffusion is related to the distance ($L$) through $qD_n dn/dx$ (21). Based on Eqs.S2-S3, the LC-IGZO TFT and Fig.S4C shows the modeling results of the ohmic TFT. Here, we confirms that the ohmic device has a higher $V_{DS}$ dependence at the saturation regime compared to the MC (Schottky) device, providing a smaller $r_o$ and lower $A_i$. A comparison with SB-TFT is also shown in Table S3. This poorer performance of the ohmic device is mainly related to weak electrical isolation of the source side from the drain bias whereas the source side Schottky barrier in the SB-TFT structure is helping to electrically isolate the source.
barrier from the drain bias. So, for the ohmic device, it is generally treated as drain-induced barrier lowering, which a sort of short channel effect (33,34). These effects are generally not present when the channel length is in tens of microns. However, when the gate insulator thickness is too thick, it comes into the picture. This is because the gradual channel approximation is not well satisfied. It means that the (vertical) gate E-field is not large enough compared to the (lateral) drain-source field. TFT are generally processed at low temperatures to be compatible to glass and plastic substrates. So, we have to grow a thicker gate insulator to guarantee low gate leakage current. Indeed, it is well accepted that a typical ohmic contact TFT usually suffers from short channel effects when L becomes less than \(~10\ \mu m\) (33,34). Here, the source side Schottky barrier in the SB-TFT structure helps to electrically isolate the source barrier from drain bias.

**ST6.** 1-V relation for forward bias in SB-TFT  
The following relation from TE theory is used to explain the non-linear behaviour of the SB-TFT,

\[
J_{\text{FWD}}(V_{GS}, V_{DS}) = J_0 \exp \left( -\frac{\phi_{B0} - \Delta \phi_{BD} (V_{GS})}{V_{th}} \right) \left( \exp \left( \frac{V_{DS}}{n V_{th}} \right) - 1 \right) \quad \text{for } V_{DS} \ll V_{\text{tran}}, \quad (S5)
\]

Here, \(J_0\) is associated with Richardson constant (21,35,36). This is an effective way to account for TFE responsible for quantum mechanical tunneling. In Eq.S4, the last term on \(V_{DS}\) explains the non-linear behaviour seen in Fig.1D. This happens when \(V_{DS} \ll V_{\text{tran}}\). As for gate bias-dependency, more electrons are induced in the channel with increasing \(V_{GS}\), making the \(\phi_{B0}\) lower (i.e. bigger \(\Delta \phi_{BD}\)) while providing a higher current through TFE, as shown in Fig.2B. From Eq.S4, Eq.1 is derived for a negative \(V_{DS}\).

**ST7.** Reverse-biased SB-TFT and gate bias dependency  
When \(V_{DS} \gg V_{\text{tran}}\), the drain current becomes firmly saturated. This is explained with the reverse-biased Schottky diode at the source junction as illustrated in Fig.2C. Here, \(V_{DS}\)-induced SB lowering due to the image charge effect is negligible because the \(V_{DS}\)-induced lateral field is very weak in low voltage (< 1V) operation. Thus, this regime satisfies the condition \(L > W_D\) seen in Fig.S5A, meaning that the SB lowering at the source side \((\Delta \phi_{BS})\) is a function of \(V_{GS}\) modulating the saturated current density. This behaviour is simulated with MATLAB as seen in Fig.S5B. While considering the initial lowering, the results are consistent with the retrieved values shown in Fig.2D. For this computation with MATLAB, we used the following set of equations to relate the microscopic parameters (such as surface potential (\(\phi_S\)) and carrier density) and macroscopic parameters (such as current and bias),

\[
C_{\text{st}}(V_{GS} - V_{\text{ref}} - \phi_S) = q^2 D \phi_S. \quad (S6)
\]

Besides this, the induced electron density \((n_{\text{induced}})\) is,

\[
n_{\text{induced}} = n_i \exp(q \phi_0 / kT), \quad (S7)
\]

and the intrinsic carrier density \((n_0)\) is calculated as,

\[
n_i = N_c \exp((E_{\text{fo}} - E_c) / kT), \quad (S8)
\]
where $N_C$ is the effective density of states, $E_{F0}$ the Fermi energy at flat-band, and $E_C$ the conduction band energy. From Eqs.S6-S8, the built-in potential ($V_{bi}$) is computed as a function of initial value ($V_{bi0}$) and surface potential ($\phi_S$) as,

$$V_{bi} = V_{bi0} + \phi_S.$$  \hfill (S9)

With Eq.S9, the Schottky barrier width at the source side ($W_S$) is written as,

$$W_S = \frac{2E_{IGZO}(V_{bi0} + \phi_S)}{q\xi_{induced}}.$$  \hfill (S10)

In Eq.S10, we ignore the drain bias-induced image-charge effect since we found that $W_D$ ~ 1.3 $\mu$m is much less than $L$ of 10 and 20 $\mu$m (see Fig.S5A). This is calculated with the following equation as,

$$W_D = \frac{2E_{IGZO}(V_{bi0} + V_{DS})}{q\xi_0}.$$  \hfill (S11)

Note that the effect of drain bias on the source side is negligible as long as the channel length ($L$) is much longer than $W_D$. In other words, when $L < W_D$, the image-charge effect (i.e. DIBL as the drain-induced barrier lowering) will be visible, leading to smaller $r_o$ as a function of $L$ and $V_{DS}$. As seen in Fig.S5A, indeed, $W_D$ should be even less than 1.3$\mu$m in the operational conditions, thus the condition, $L < W_D$, is satisfied. From Eqs.S6-S11, the following equations are derived as a function of distance ($x$),

$$E_S = q(\phi_{bs} - V_{gs}) + q\phi_S + V_{bi0} - V_{bi}(\phi_S),$$  \hfill (S12)

$$E_D = q\phi_{bs} - q\phi_S - E_S - \frac{1}{2}W_S^2,$$  \hfill (S13)

$$\Delta E_S = E_S(V_{gs0}) - E_S(V_{gs}),$$  \hfill (S14)

$$E_S(V_{gs0}) = q\phi_{bs} + V_{bi0} - V_{bi}(\phi_S).$$  \hfill (S15)

$$q\Delta \phi_{bs} = E_s(V_{gs}) + \Delta E_S.$$  \hfill (S16)

Using Eqs.S12-S16, the band diagram to show the SB lowering for difference gate biases are calculated and plotted in MATLAB, as seen in Figs.S5A and S5B.

**ST8. Relationship between SB Height and Width**

Since the image charge effect is negligible at a low bias condition, and interface property at the contact is fixed with process, the SB height as the difference between the Mo work-function and electron affinity of IGZO is not changed physically. In contrast, the SB width is physically changed and electrically modulated with the gate-source field / bias. When the SB width is reduced more, electrons’ emission is expected to be increased more. This is not a typical thermionic emission (TE), but a thermionic field-emission (TFE) (23). The TFE property is mainly related to the quantum mechanical tunneling which usually yields a numerical form or complicated equation of current-voltage relation rather than an analytical equation (36). So, in this work, we employed the effective SB height-lowering (e.g. $\Delta \phi_{bs}$) as an effective and more analytical way to account for narrowing of the SB-width ($W_S$) and respective tunneling effect to explain the TFE (Fig.S5C) (23).

**ST9. Equations for $r_o$ and $g_m$ for SB-TFTs**

The saturation current is described as,
\[ I_{sat} = A_s J_{sat}(V_{GS}) \exp \left( \frac{\varphi_{B0}}{v_{th}} \right) \left[ 1 - \exp \left( -\frac{V_{DS}}{nv_{th}} \right) \right], \quad (S17) \]

where \( n \) is the ideality factor (\( \sim 1.7 \) of the examined device), \( A_s \) the Schottky contact area where electrons are emitted through the TE-TFE rather than drift-diffusion process, \( v_{th} \) thermal voltage (i.e. \( kT/q \)), and \( J_{sat} \) the saturation current density as a function of \( \varphi_{B0} \) and \( V_{GS} \). Note that \( I_{sat} \) is linearly proportional to \( A_s \) defined as \( W \ell \), where \( \ell \) is a specific contact length. So \( I_{sat} \) is scalable only by \( W \). In other words, as seen in Eq.S17, the saturation current of the SB-TFT is not dependent on \( L \) but \( W \). In addition, the term, \( 1 - \exp(-V_{DS}/nv_{th}) \), is almost unity in the saturation regime since \( V_{DS} \gg nv_{th} \) at 300K, and thus independent of \( V_{DS} \). These are consistent with the results in Fig.1B. In Eq.S17, the current density term can be written as,

\[ J_{sat}(V_{GS}) = J_0 \exp \left( \frac{\Delta \varphi_{BS}(V_{GS})}{v_{th}} \right). \quad (S18) \]

Here, \( J_0 \) is a reference current density and the barrier lowering term (\( \Delta \varphi_{BS} \)) is where the TFE is taken into account effectively as a function of \( V_{GS} \) in the same way as Eq.S5. As seen in Fig.2D, it is noticed that there is an intercept (\( \Delta \varphi_0 \) \( \sim 0.165V \) which can be considered as an initial SB lowering corresponding to the reference current of 1 pA at \( V_{GS} = V_{ref} \). Here, \( \Delta \varphi_{BS}(V_{GS}) = \zeta_0(V_{GS} - V_{ref}) + \Delta \varphi_0 \). With Eqs.S17 and S18, the intrinsic gain is given as,

\[ A_i = \zeta_0 n \exp \left( \frac{v_{sat}}{nv_{th}} \right), \quad (S21) \]

As seen in Eq.S21, \( A_i \) is not a function of either bias (e.g. \( V_{GS}, V_{DS} \)) or geometry (e.g. \( W, L \)), but a function of intrinsic parameters (e.g. \( \zeta_0, n, v_{th}, \) and a saturation voltage \( v_{sat} \)). So, it is just a constant unlike the ohmic device. With Eq.5, \( A_i \) is calculated as \( \sim 450 \) for \( \zeta_0 = 0.19, n = 1.7, v_{th} \sim 25.6mV, \) and \( v_{sat} = 0.315V \) (see the section ST10). And \( g_m \) and \( r_o \) of the ohmic device are also extracted as \( 5 \times 10^{-12} \) S and \( 8 \times 10^{12} \) Ohm, respectively, giving \( A_i = 40 \) (Table S3). This clearly indicates that the SB device has an order of magnitude higher amplification factor compared to the ohmic device. In Eq.S16, \( \zeta_0 \) can be written as \( \ln(10)v_{th}/SS \) where \( SS \) is \( \ln(10)v_{th}n \). Thus, \( \zeta_0 = 1/n, \) where \( n \) is \((1+q^2D/c_{ox})\) from Eq.S1. From this Eq.S16 is rewritten as follows,

\[ A_i = \frac{n}{n_i} \exp \left( \frac{v_{sat}}{nv_{th}} \right). \quad (S22) \]

Here, we can further reduce Eq.S22 with the Early voltage (\( V_A \)) concept as,

\[ A_i = \frac{V}{V_{th}}. \quad (S23) \]
As seen in Eq. S24, the $V_A$ of the SB-TFT is huge due to the exponential term where $v_{sat} \gg n v_{th}$. This is the main origin of a high intrinsic gain associated with the almost infinite output resistance which is also related to this exponential term seen in Eq. S19. A comparison with BJT and Si-MOSFET is shown in Table S4.

ST10. Extraction of Intrinsic Parameters for $A_i$

For the calculation of $A_i$, the values of the intrinsic parameters ($\zeta_0$, $n$, $v_{th}$, and $v_{sat}$), which compose $A_i$, need to be extracted. The extraction methodology for each parameter is described in Fig. S6. For $v_{sat}$, both $V_{\text{tran}}$ and $V_0$ are needed to be extracted since $v_{sat} = V_{\text{tran}} - V_0$. In Fig. S6A, $I_{DS}$ vs. $V_{DS}$ plot is used for retrieving the values of $V_{\text{tran}}$ and $V_0$, where a linear extrapolation was applied. The extrapolation line met the bottom and top reference levels for zero and saturation, respectively. This method gave $V_{\text{tran}} = 0.48V$ and $V_0 = 0.165V$, thus $v_{sat} = 0.315V$. The second parameter is the ideality factor ($n$) of the Schottky diode of the source/drain side. To get this, we used the log-scale plot of $I_{DS}$ vs. $V_{DS}$, as seen in Fig. S6B (i.e. typical method used for a diode evaluation) (21,36). From the slope, we now got $n = 1.7$, as seen in Fig. S7B. The third one is $\zeta_0$ which was extracted as 0.19, as shown in Fig. S7C (see also Fig. 2D). This is based on the simulation results in Fig. S6B. Empirically, $\zeta_0$ can also be extracted from the SS value ~ 0.28V/dec, which is explained in the following section (ST11) along with Eq. S25. Lastly, $v_{th}$ was given as 25.6mV at 300K (RT), which is from the calculation with $k_B T/q$, where $k_B = 1.38 \times 10^{-23}$ J/K, $T=300$ K, and $q = 1.6 \times 10^{-19}$ C.

ST11. Empirical and Physical Meaning of $\zeta_0$

As seen in Eq. S21, i.e. $A_i = \zeta_0 n \exp(v_{sat}/nv_{th})$, the intrinsic gain ($A_i$) can be higher with a larger $\zeta_0$. This is one of the device’s intrinsic parameters which related to interface quality through the following relation connected with SS empirically,

$$\zeta_0 = \frac{C_{ox}}{C_{ox} + q^2 D_t} = \frac{\ln(10)}{SS} v_{th}.$$  

(S25)

This suggests that the steeper (smaller) SS due to better interface quality/film quality will help to get a bigger $\zeta_0$ for a given gate-insulator capacitance ($C_{ox}$). In other words, a bigger $C_{ox}$ can yield a bigger $\zeta_0$ for a given $D_t$. Here, $D_t$ is considered as the interface state density in the conventional theory for ohmic devices. This suggests that a Schottky device may have a different physical meaning although it may be fine empirically to be treated as is. So, $\zeta_0$ is physically and more correctly to be considered as a parameter to describe how the gate field is efficiently modulating the SB shape. This efficiency may be increased with a larger $C_{ox}$, thus empirically same observation as the earlier discussion with SS. This suggests that an actual physical meaning of $\zeta_0$ in the SB-TFT is not entirely related to the interface quality between the semiconductor and gate-insulator, but it is related to an electrostatic sensitivity to the Schottky-barrier modulation mainly at the source side where the electrons’ emission is determined. In other words, if a certain SB-TFT got a bigger $\zeta_0$, it means that the SB shape at the source is more easily modulated even with smaller gate-source field/bias. At the same time, once electrons have been
emitted into the channel, they will still suffer from the trapping at the interface traps which reside at the interface between the semiconductor, i.e. active layer, and gate insulator. Thus, $\zeta_0$ is a combinational parameter of the SB modulation efficiency by gate bias, and the typical interface states which usually determine the SS in a typical ohmic device.

**ST12. Electrical Stability**

Since the presented transistor operates at a low voltage and low current, it is also electrically stable for a long time. Indeed, the measured instability data, seen in Fig. S7, confirms this. Here, we used the real operating bias conditions: $V_{GS}=0.5V$ and $V_{DS}=1V$. It is found that the drain current is found to be very stable for a long time of 10000sec. This implies that the low operating voltages ($V_{GS}=0.5V$ and $V_{DS}=1V$) and corresponding drain current are too low to get either a charge trapping or a defect creation (37,38).

**ST13. Circuit Demonstration**

Using the presented SB IGZO TFTs, a common source amplifier was demonstrated in Fig.4 and Fig.S9. Initially in Fig.S9A and S9B, TFT-2, which has a larger $W$, is used as a depletion load for an extremely low bias-current of ~ 2 pA. Indeed, the bias current ($I_B$) and voltage ($V_{B}$) are ~2 pA and ~0.1 V, respectively. This suggests that the current can be scaled with $W$. So, it is expected that the peak gain happens at ~0.1V input. Indeed, as seen in Fig.S9E and S9H, the peak voltage gain of 230 happens at ~0.1V of $V_{in}$, and power consumption is ~3pW only. Thus, this approach would be useful for extremely low power applications where requiring simply a picowatt power source. In the second example, which is also shown in Fig.4, TFT-2 is another type of depletion load (Fig.S8), as seen in Figs.S9C and S9D. The TFT-2 has a negative $V_{ref}$ of -0.51V, which stems from light stress (under conditions of $V_{GS}=0V$ and $V_{DS}=0.5V$ with 1mW/cm$^2$ blue light for 1000sec) (Fig.S8A). This negative shift of I-V curves are due to either ionized oxygen vacancies and/or hole trapping, and persistent photoconductivity (PPC) (19, 20, 24). As seen in Fig.S9G, the bias current ($I_B$) is ~ 90pA since TFT-2 has it at $V_{GS}=0V$. And it is matched with the current level of TFT-1 at $V_{GS}=0.5V$. So, it is expected that the peak gain happens at 0.5V input. At $V_{in} = 0.5V$, it is found that the voltage gain ($A_V$) for each example circuit is peaked to be about 220, as seen in Fig.S9E. This is explained with $A_V = 0.5A_t$, where $A_t$ is ~450 of each TFT’s intrinsic gain. Figs.S9G and S9H show the measured $I_{out}$ and $P_{out}$. In particular, output-power consumption ($P_{out}$) is found to be very low < 150 pW (Fig.S9H). Thus, it can even be driven by a nano-watt power source.

**ST14. Importance of Ultra Low Power TFTs**

Thin film transistors (TFTs) based on amorphous oxide semiconductors (AOSs), such as In-Ga-Zn-O (IGZO), have been shown to be one of the most promising candidates for large-area electronic applications, including wearable systems. However, another key requirement is still missing particularly for a wearable application, which is a low power consumption capability, since a wearable system is portable along with a limited battery life-time and/or only micro-watt-level power harvesting technique with a battery-less. To meet this requirement, we report on a Schottky-barrier (SB) IGZO TFT operating in the sub-threshold (sub-T) regime to meet ultra low power and high gain performances. In this regime, transistors are almost switched off, but working on with a leakage / standby...
signal while turning it into a useful signal (Fig.S10). This brings a new concept as a near-OFF-state TFT circuit design (Fig.S11).

**ST15. Guidance for Device-Level Optimization for High Performance Circuits**

As seen in Eq.S25, the steeper (smaller) SS due to either a better interface quality/film quality (i.e. smaller $D_t$) or a larger $C_{ox}$ will help to get a bigger $\zeta_0$ and $A_i$. Another way is to get a smaller ideality factor (n) which associated with the Schottky diode characteristics in association with metal-semiconductor interface quality and work-function of the metal for source and drain electrodes. This also leads to a higher $r_o$. Similarly, as seen in Eq.S20, transconductance ($g_m$) can be higher with a larger $\zeta_0$ for a given geometry ($A_i$). In addition, $g_m$ can also be increased with $A_j$ through increasing W. For output driving capability (i.e. fan-out), the followings needs to be satisfied (17, 18),

$$R_{intrinsic} = \frac{1}{g_m} < R_{Load}$$  \hspace{1cm} (S26)

where 

$$1 = \frac{1}{g_m} = \frac{v_{th}}{\zeta_0 A_j J_{th0}} \exp \left( -\frac{\zeta_0 (V_{GS} - V_{ref}) - \Delta \phi_0}{v_{th}} \right),$$  \hspace{1cm} (S27)

$$A_j \equiv W/e,$$  \hspace{1cm} (S28)

$$\zeta_0 = \frac{\ln(10)}{SS} V_{th}.$$  \hspace{1cm} (S29)

If the (capacitive or high impedance) load (i.e. $R_{Load}$) is big enough, it would be fine to satisfy Eq.S26 as is. Otherwise, we can still tune $g_m$ by tuning W as reflected in Eqs.S27 and S28. In addition, as mentioned earlier, the SS can be smaller with improvement of interface and Schottky contact quality, leading to a larger $\zeta_0$. This would also lead to a higher $g_m$ even at the same bias current, as seen in Eqs.S27 and S29. In addition, the smaller SS would help for the further scaling-down of voltage range much less than 1V while maintaining the level of current, thus further low power can be achieved. Besides, if the drain-side contact becomes ohmic while keeping the source contact as Schottky, $V_0$ would be zero helping to get a smaller $V_{tran}$ in the output characteristics. These are summarized in Fig.S12, along with other diagnostic points. Here, we believe that this would be useful for engineers and scientists who are following up this work for a circuit design consideration in near future.
Fig.S1. IGZO target specification drawn on its possible stoichiometries and process windows. (A) Reaction rate and respective reduction of oxygen vacancies. Inset: Reconstructed oxygen 1s peaks (XPS) for 4% and 15% $P_{ox}$ devices. (B) Measured electron concentration and mobility vs. $P_{ox}$. Inset: Micro-photos of the fabricated LC- and MC-IGZO TFTs. (C) Electron density and oxygen vacancy density as a function of $P_{ox}$. 
Fig. S2. Conceptual band-diagram of 4 Schottky contact cases for 4 different samples and respective sub-threshold characteristics. Band diagrams in (A) to (D) are for the cases of 4\% P_{ox} and 250 °C annealing, 4\% P_{ox} and 450 °C annealing, 15\% P_{ox} and 250 °C annealing, and 15\% P_{ox} and 250 °C annealing, respectively. Here, the LC-IGZO and MC-IGZO devices mentioned in the main text are the diagrams (A) and (D), respectively. (E) I_{DS} vs. V_{GS}, (F) I_{DS} vs V_{DS} for A and B, and (G) I_{DS} vs V_{DS} for C and D, respectively.
Fig. S3. Input characteristics and basic parameter extractions of MC- and LC-IGZO TFTs. (A) Log-scale $I_{DS}$ vs. $V_{GS}$ in the deep sub-T regime, where SS of each device is indicated. (B) Linear-scale $I_{DS}$ vs. $V_{GS}$, where $V_T$ is extracted using a typical linear-extrapolation method.

Fig. S4. Modeling results of ohmic TFT (i.e. LC-IGZO TFT). (A) $I_{DS}$ vs. $V_{GS}$ in log-scale, where $V_{ref}$ is indicated. (B) Log-scale $I_{DS}$ vs. $V_{GS}$ where the deep sub-T regime is zoomed in along with the calibrated gate bias (i.e. $V_{GS}-V_{ref}$). Here, modeled result (dot line) agrees well with the experiment. (C) Experimental and modeled output characteristics for a different $V_{GS}$, showing a good agreement with each other.
Fig. S5. MATLAB simulation results on bias-dependent SB. (A) Depletion width at drain side (W_D) vs. V_DS for a different gate bias. (B) Schottky barrier lowering vs. distance from the source side for different gate biases. Here, the initial barrier height ($q\phi_{B0}$) is to be 0.67eV = $q\phi_m$(Mo) - qX(IGZO). The work-function of Mo ($q\phi_m$) and electron affinity of IGZO (qX) is to be 5eV (25) and 4.33eV (26). In addition, SB width at source (W_S) is indicated as well. (C) The deduced relationship between $\Delta \phi_{BS}$ and W_S.
Fig. S6. Extraction of intrinsic parameter values for an estimation of $A_i$. (A) Normalized $I_{DS}$ vs. $V_{DS}$ measured at $V_{GS} = 1V$, where $V_{sat}$ and $V_{tran}$ are retrieved. (B) Extraction of ideality factor ($n$) in the log-scale. (C) Extraction of $\zeta_0$ as the slope on the plot of $\Delta \phi_{BS}$ vs. $V_{GS}$, where each value is from the MATLAB simulation (Fig.S5B).

Fig. S7. Electrical stability under dark. Effect of bias stress on drain current under dark. Here, we used the actual operating bias conditions: $V_{GS} = 0.5V$ and $V_{DS} = 1V$. It is found that the drain current is found to be very stable for 10000sec. Inset: conceptual cross-section of the device where gate-source field and drain-gate field are balanced to be cancelled since they are the same in the amplitude but the opposite direction each other. So, even if there is a charge trapping process under this low bias condition, it is expected to be cancelled, suggesting a long-term electrical stability / reliability.
Fig. S8. Light induced conversion from enhancement mode to depletion mode. (A) Light stress induced drain current increase vs. time. Here, the stress condition is as follows: $V_{GS}=0\, \text{V}$, $V_{DS}=0.5\, \text{V}$, and light intensity (blue) = 1mW/cm$^2$ (Inset: drain current vs. gate bias before and after the light stress) (B) Conceptual diagram before light stress. (C) Diagram to describe the oxygen vacancy ionization under light, and its persistency due to its lattice relaxation (19,20,24). (D) Diagram after removal of light. Here, the increased conductivity and current can be maintained since ionized $V_{Ox}$ are holding electrons as donors (19,20).
Fig. S9. Circuit level demonstrations with different types of depletion loads. (A) Measured $I_{DS}$ vs. $V_{GS}$ for driver (TFT-1) and depletion load (TFT-2). Here, TFT-2 has a factor of 2 larger $W$, acting as a depletion load with providing an extremely low bias current $\sim 2pA$. (B) Common-source circuit diagram and its 3-D view. (C) Measured $I_{DS}$ vs. $V_{GS}$ for driver (TFT-1) and another type of depletion load (TFT-2). Here, TFT-2 has an identical geometry as TFT-1, but has a negative $V_{ref}$ after light stress (Fig.S9A), acting as a depletion load. Note that this particular case also provides an optical tenability. (D) Respective circuit diagram. (E) $V_{out}$ vs. $V_{in}$, (F) $A_{V}$ vs. $V_{in}$, (G) $I_{out}$ vs. $V_{in}$, and (H) $P_{out}$ vs. $V_{in}$ for those two cases, respectively.
Fig. S10. Motivation figure -1: TFT power consumption per 1V with state diagram ranging from the OFF- to ON-states. Here, the values are calculated as an absolute value with $W = 50 \mu m$. The deep sub-T regime, where transistors are almost switched off, is operated only with sub-nano Watts. And this regime helps to stay at a cold state (blue colour) in terms of its power density for a given transistor area (i.e. $W \times L$). In contrast, the typical on-regime, i.e. above-T regime, consumes a high power > 1mW. It suggests a high power density, thus a hot state (red colour). The power level labeled in blue, which is below the threshold (green), should be the target for TFT-based wearable systems, especially in a battery-less energy harvesting.

Fig. S11. Motivation figure-2: Conceptual illustration with Y-shape highway between TFT's ON- and Near-OFF-states. Here, the two extreme applications are sitting at the end of each avenue. This figure is a highway-concept version converted from the version seen in Fig.S10.
Fig. S12. Flow chart of a technical guidance to improve performances of the sub-threshold SB-TFTs for higher performance circuits. Here, the relationship between device level optimization and microscopic parameters is also shown relating to the final performances in macroscopic.
Table S1. TFT sample sprit from A to D and sub-threshold slope (SS) of each one.

<table>
<thead>
<tr>
<th>$P_{OX}$</th>
<th>4%</th>
<th>15%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Annealing Temperature</td>
<td>250 °C</td>
<td>450 °C</td>
</tr>
<tr>
<td>Sample Labels</td>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>Sub-threshold Slope (SS)</td>
<td>0.34 V/dec</td>
<td>0.33 V/dec</td>
</tr>
</tbody>
</table>

Table S2. OFF-Current and Standby Power for TFT Technologies (1-8, 13-16).

<table>
<thead>
<tr>
<th>TFT Technologies</th>
<th>LTPS</th>
<th>a-Si</th>
<th>Organics</th>
<th>IGZO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Band-gap</td>
<td>~ 1.1 eV</td>
<td>1.7 ~ 1.8 eV</td>
<td>1 ~ 2 eV</td>
<td>&gt; 3eV</td>
</tr>
<tr>
<td>OFF-current</td>
<td>&gt; $10^{-12}$ A</td>
<td>~ $10^{-12}$ A</td>
<td>~ $10^{-12}$ A</td>
<td>&lt; $10^{-13}$ A</td>
</tr>
<tr>
<td>Minimum Standby Power (for $V_{DD} = 1$V)</td>
<td>&gt; $10^{-12}$ W</td>
<td>~ $10^{-12}$ W</td>
<td>~ $10^{-12}$ W</td>
<td>&lt; $10^{-13}$ W</td>
</tr>
</tbody>
</table>

Table S3. Basic performance comparison between Schottky and ohmic S/D TFTs.

<table>
<thead>
<tr>
<th>TFT Types</th>
<th>Schottky-Barrier TFTs (this work)</th>
<th>Ohmic S/D TFTs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sub-threshold Slope (SS)</td>
<td>~ 0.28 V/dec</td>
<td>~ 0.34 V/dec</td>
</tr>
<tr>
<td>$r_0$ ((\propto 1/SS))</td>
<td>~ 0.19</td>
<td>~ 0.17</td>
</tr>
<tr>
<td>Intrinsic Gain</td>
<td>~ 450</td>
<td>~ 40</td>
</tr>
<tr>
<td>Output resistance at $V_{GS} - V_{ref} = 0$V</td>
<td>~ $5 \times 10^{13}$ Ω</td>
<td>~ $8 \times 10^{12}$ Ω</td>
</tr>
<tr>
<td>Transconductance at $V_{GS} - V_{ref} = 0$V</td>
<td>~ $9 \times 10^{-12}$ S</td>
<td>~ $5 \times 10^{-12}$ S</td>
</tr>
</tbody>
</table>
Table S4. Features of the sub-T SB-TFT in comparison with BJT and Si-MOSFET.

<table>
<thead>
<tr>
<th>Transistors Families</th>
<th>Sub-threshold SB-TFT (this work)</th>
<th>BJT</th>
<th>Si-MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Saturation Current / Transconductance</td>
<td>Exponential / Exponential</td>
<td>Exponential / Exponential</td>
<td>Square-law / Linear</td>
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<tr>
<td>Output Resistance</td>
<td>Huge</td>
<td>Huge</td>
<td>Low</td>
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<tr>
<td>Intrinsic Gain</td>
<td>$\frac{V_A}{V_{th}}$ (Constant)</td>
<td>$\frac{V_A}{V_{th}}$ (Constant)</td>
<td>$\frac{2V_A}{V_{GS} - V_T}$ (Bias dependent)</td>
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<tr>
<td>Input Current</td>
<td>None</td>
<td>High</td>
<td>None</td>
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<tr>
<td>Input Impedance</td>
<td>Huge</td>
<td>$\beta/\beta_n$</td>
<td>Huge</td>
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<tr>
<td>Design Parameter</td>
<td>$A_s$ (source contact area)</td>
<td>$A_e$ (emitter area)</td>
<td>W/L</td>
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<tr>
<td>Operating Voltage</td>
<td>0.5V ~ 2V</td>
<td>0.5V ~ 2V</td>
<td>0.5V ~ 2V</td>
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<tr>
<td>Operating Current</td>
<td>&lt; 1mA</td>
<td>~ mA</td>
<td>~ μA</td>
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