Mono-Type TFT Logic Architectures for Low Power Systems on Panel Applications

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***Abstract*—This paper introduces novel 7-T pseudo-CMOS for enhancement mode and 6-T pseudo-CMOS for depletion mode inverter circuit architectures. The designs are built around mono-type of TFTs and consume less power consumption than existing 4-T pseudo-CMOS circuits. In addition, they provide steep transfer curves, along with embedded control for compensation of device parameter variations. Analysis of the transient behavior for the various circuit architectures is presented, providing quantitative insight into capacitive loading taking into account the effects of overlap capacitances.**

***Index Terms*—pseudo-CMOS, thin film logic circuits, ring oscillator, circuit CAD,**

I. Introduction

System on panel (SOP) integration is gaining significant interest in displays and other large area applications. This is driven by the need to further reduce cost margins, along with the added benefits of increased compaction [1]-[12]. The quest for higher on-panel integration density is strongly motivated by advances in thin film transistor (TFT) technology, which have enabled realization of complex pixel circuits with analog-digital functionality [13] for switching and stability compensation in active matrix arrays. In addition, digital circuits such as shift registers and other logic forms are now commonly used for the gate driver electronics [14], [15]. Unlike the ubiquitous CMOS technology, TFTs (with the exception of polysilicon) are generally monotype (i.e. either n- or p-channel). A summary of key properties of two monotype large area TFT technology families is given in Table 1. Note the stark contrast in carrier mobilities of the monotype channel rendering poor circuit performance in terms of switching behavior and power consumption.

Recently, Huang *et al*. introduced a high performance 4-T pseudo-CMOS inverter circuit with monotype transistors [16]-[19], however, with static power consumption much higher than the conventional CMOS [20] or the dual-V_T [21] counterpart. Alternate TFT structures based on the dual-gate configuration have been proposed [22]-[24] so as to provide better control of threshold voltage and improvement in noise margin, power consumption and circuit delay. But this comes at the cost of fabrication complexity and cost, depending on the material system and associated processing [20]-[24]. In addition, control signals are required for circuit operation.

However, in this paper, the author has provided an ultra low-power logic styles for non-complementary logic applications by transistor feedback effect. The paper is organized as follows. Section II introduces previous reported works followed by Section III, which describes the static CAD model, used for simulation of the circuits presented in this paper. Novel inverter circuits are presented in Section IV and circuit performance discussed in Section V and Section VI. Section VII presents impact of overlap capacitance on circuit performance. Finally, a five-stage 7-T pseudo-CMOS ring oscillator is presented in Section VIII followed by conclusions.

TABLE 1
COMPARISON OF OXIDE AND ORGANIC TFT TECHNOLOGY

TFT Technology	Oxide		Organic	
Device Type	N	P	N	P
Device Materials	IGZO	Copper Oxide	PTCDI – $C_{13}H_{27}$	Pentacene
Mobility (cm^2/Vs)	1.58	0.0022	0.09	0.71
Threshold Voltage	5.77	-4.75	49	-22
Reference	[25]	[25]	[26]	[26]
Device Type	N	P	N	P
Device Materials	SnO_2	SnO	$F_{16}CuPc$	Pentacene
Mobility (cm^2/Vs)	-	0.24	0.02	0.06
Threshold Voltage	-	30	-	-
Reference	[27]	[27]	[20]	[20]

II. Inverter Circuit Configurations

There have been a number of inverter circuit types introduced and these include, as examples, saturated/unsaturated load, level-shifted diode-load, depletion load, CMOS [28], and 4-T pseudo-CMOS [17].

In this paper, these three types of circuits are taken into consideration – CMOS, saturated load, and 4-T pseudo-CMOS – as shown in Fig. 1.

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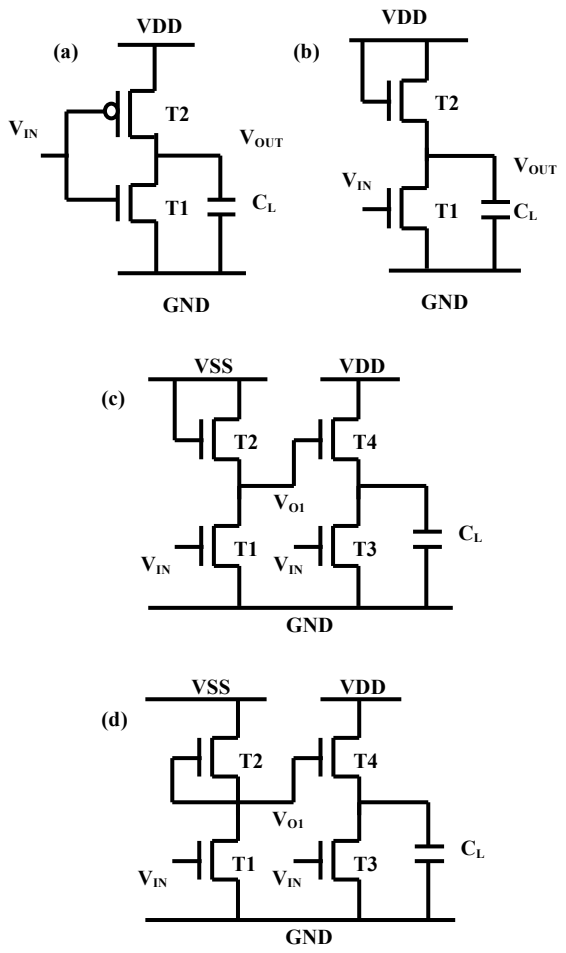


Fig. 1. Different inverter configurations; (a) CMOS p-channel load (b) diode-connected load (c) enhancement mode 4-T pseudo-CMOS and (d) depletion mode 4-T pseudo-CMOS. The enhancement and depletion mode have different aspect ratio TFTs.

The CMOS configuration is believed to be the most efficient circuit especially for digital circuits. It has negligible static power consumption along with a full voltage swing, and a perfect transfer curve. However, for most TFT technologies, with relative low mobility for one type of material, the corresponding transistor has a much larger size to have a comparable drivability. In addition, because of its staggered structure, the parasitic capacitances resulting from the overlap of electrodes, which are proportional to the device channel width, cannot be avoided [12],[29]. This results in increased power consumption and time delay. The saturated load inverter, with its ratioed design, consumes high static power with a large pull down device to maintain low logic level. In contrast, the recent 4-T pseudo-CMOS configuration has the advantage of better noise margin and a large voltage swing. However, the first stage of the 4-T pseudo-CMOS with its diode-connected architecture, cannot limit the current, which results in relative high power consumption [17]-[19].

III. Thin Film Transistor Logic Design

The model used for design and analysis of the logic configurations has been reported earlier by Lee *et al.* [30]- [34] and is summarized below. More details about the models has been described in Appendix C.

1) Static Model:

Linear Regime: $(V_{GS}-V_T)>V_{DS}$

$$I_{lin}=\mu_0^*\left(\frac{N_C}{N_C+N_{tc}kT_t}\right)\frac{W}{L-\Delta L}\frac{C_{ox}^{\alpha_p+1}}{Q_{ref}^{\alpha_p}}(V_{GS}-V_T)^{\alpha_p+1}V_{DS}', \quad (1)$$

Saturated Regime: $(V_{GS}-V_T)\le V_{DS}$

$$I_{sat}=\frac{1}{2}\mu_0^*\left(\frac{N_C}{N_C+N_{tc}kT_t}\right)\frac{W}{L-\Delta L}\frac{C_{ox}^{\alpha_p+1}}{Q_{ref}^{\alpha_p}}(V_{GS}-V_T)^{\alpha_p+2}\beta_{sat}. \quad (2)$$

Here, W is the channel width, L the channel length, a_p the power law exponent, β_{sat} the pinch off coefficient $\beta_{sat}=1+V_{DS}/V_A$, where V_{DS} is a constant and V_A the early voltage.

2) Dynamic Model:

The dynamic model is illustrated in Fig. 2, where the various symbols and expressions are summarized in Table 2. The key simulation parameters are shown in Table 3.

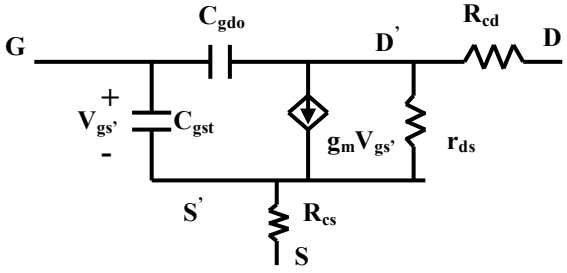


Fig. 2. Dynamic model of TFT. C_{gst} is the sum of gate insulator capacitance and the gate source overlap capacitance, and C_{gdo} gate drain overlap capacitance

IV. Proposed Logic Circuits

A. Enhancement-Mode 7-T Pseudo-CMOS Inverter

Fig. 3 shows circuit schematics of the proposed enhancement-mode 7-T pseudo-CMOS inverter designs. While enhancement-mode designs generally provide small power consumption for the second stage, the first stage of the circuit is diode connected, which results in a relative large power consumption. Hence, the motivation of the proposed circuits is to limit the power consumption by altering its design through adding an extra stage. As shown in the Fig. 3(a) and (b), the pull down transistors T1, T3, and T6 are connected to the input. Transistor T2 is connected to the source of T5 and T4 is connected to the source of T2. T5 is diode connected and T7 connected to the source of T4. With input voltage low, T1, T3 and T6 are off, transistor T5 conducts and V_{O1} is set to be V_{SS}-V_T. Hence, T2 conducts and V_{O2} is V_{SS}-2V_T and T4 conducts and V_{O3} is V_{SS}-3V_T. Therefore, the load voltage is high. When input is high, T1, T3, and T6 conduct. The static

TABLE 2
DYNAMIC MODEL SYMBOLS AND EXPRESSIONS

Symbol	Quantity	Expressions
g_m	transconductance	$g_m = (2+\alpha_p)K(V_{GS}-V_T)^{\alpha_p+1}\beta_{sat}$
r_{ds}	output resistance	$1/r_{ds} = 1/V_A K(V_{GS}-V_T)^{\alpha_p+2}$
C_{gst}	total gate to source capacitance	$C_{gst} = C_{gs} + C_{gso} = \left.\frac{\partial Q_G}{\partial V_{GS}}\right\|_{V_{GD}} + 1/2WC_{ov}$
C_{gdo}	gate to drain overlap capacitance	$C_{gdo} = 1/2WC_{ov}$
R_{cs}	source contact resistance	$R_{cs} = 1/2R_{cw}/W$
R_{cd}	drain contact resistance	$R_{cd} = 1/2R_{cw}/W$

where K is the conductance parameter: $K = \mu_0^*\left(\frac{N_C}{N_C + N_{tc}kT_t}\right)\frac{W}{L-\Delta L}\frac{C_{ox}^{\alpha_p+1}}{Q_{ref}^{\alpha_p}}$,

C_{ov} the overlap capacitance per unit width, R_{CW} the contact resistance parameters, $Q_G = \frac{\alpha_p+2}{\alpha_p+3}C_{ox}\frac{(V_{GS}-V_T)^{\alpha_p+3}-(V_{GD}-V_T)^{\alpha_p+3}}{(V_{GS}-V_T)^{\alpha_p+2}-(V_{GD}-V_T)^{\alpha_p+2}}$

TABLE 3
KEY PARAMETERS FOR SIMULATION

Symbol	Quantity	Simulation value
μ_n	effective mobility of n type transistor	15 cm^2/Vs
μ_p	effective mobility of p type transistor	2 cm^2/Vs
L_{min}	minimum channel width	10 µm
ΔL	electrical channel length expansion	-3 µm
V_T	threshold voltage	2 V
C_{ox}	gate capacitance unit area	12n F/cm^2
C_{ov}	overlap capacitance unit length	10p F/cm
α_p	power-law exponent,	0.2
Q_{ref}	reference charge of tail states	100n C/cm^2
V_{A0}	absolute value of early voltage at L_m=10 µm	200 V

current though T5 should be the same as the current through T3, so the voltage V_{O1} reduces. With T1 conducting, the voltage V_{O2} drops. Hence, both the gate voltage of T2 and T4 decrease and the current though the first and second stage can be limited. With the input voltage high, transistor T2 and T4 work as a feedback system. Transistors T2, T4 and T5 are operated in saturation regime. Hence, Vss – V_{O1} = V_{O2} – V_{O3}. It increases the resistance of the pull up system and provides a lower V_{O3} than the 4-T pseudo-CMOS. Compared with the design of previously reported 4-T pseudo-CMOS designs, the proposed 7-T pseudo CMOS inverter requires seven TFTs instead of four. In addition, the vertical multi-stage architecture may require a higher V_{DD} to drive the circuit. However, the circuit operating principle is based on a complementary switching technique across each stage, thus low power consumption has been achieved although the circuit speed may be influenced. There is no need to add more transistors because the current has been already limited. If more transistors are added, the transfer curve shifts to a more negative level resulting in large noise margin. This can be adjusted with voltage tuning but at the cost of increased power consumption. Additionally a transistor number in general increases parasitics resulting in increased power consumption and a lowering of circuit speed.

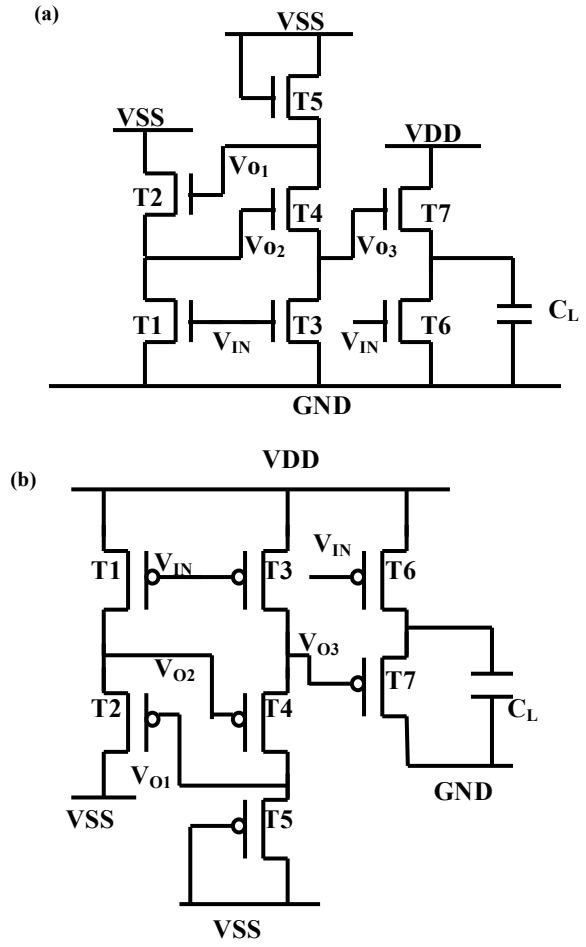


Fig. 3. Schematics of enhancement mode (a) n-type 7-T pseudo-CMOS inverter (b) p-type 7-T pseudo-CMOS inverter.

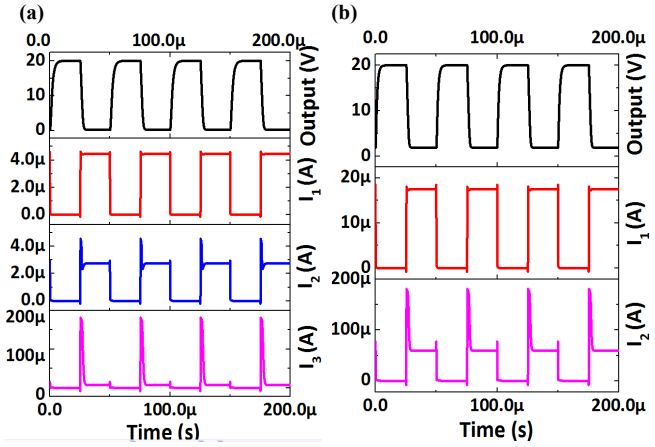


Fig. 4. Dynamic output and current for the (a) enhancement mode 7-T pseudo-CMOS inverter (b) enhancement mode 4-T pseudo-CMOS inverter as shown in Fig. 1. (c).

TABLE 4
TRANSISTOR SIZE OF ENHANCEMENT MODE FOR SIMULATION

TFTs		Channel width (μm)	Channel length (μm)
7-T pseudo-CMOS	*T1*	10	10
	T2	10	10
	T3	10	10
	T4	10	10
	T5	10	10
	T6	400	10
	T7	200	10
4-T pseudo-CMOS	*T1*	40	10
	T2	10	10
	T3	400	10
	T4	200	10

The results shown in Fig. 4 are based on the transistor size as indicated in Table 4.

For fair comparison, the total area of the 7-T pseudo-CMOS circuit is equal to that of the pseudo-CMOS and the final stage transistors have the same size to keep the same parasitics since these affect circuit performance as discussed in Section VI. As shown in Fig. 4 (a) and (b), the sum of the on currents I_1 (4.5 μA) and I_2 (2.8 μA) in proposed circuit is less than half that of the first stage of 4-T pseudo-CMOS: I_1 (18 μA). In addition, the minimum output voltage (0.22V compared to 1.9V) is also much lower. Thus the on current of the 7-T pseudo-CMOS circuit in the final stage is one fifth that of 4-T pseudo-CMOS, which implies a higher power efficiency and smaller voltage for logic low.

B. *Depletion-Mode 6-T Pseudo-CMOS Inverter*

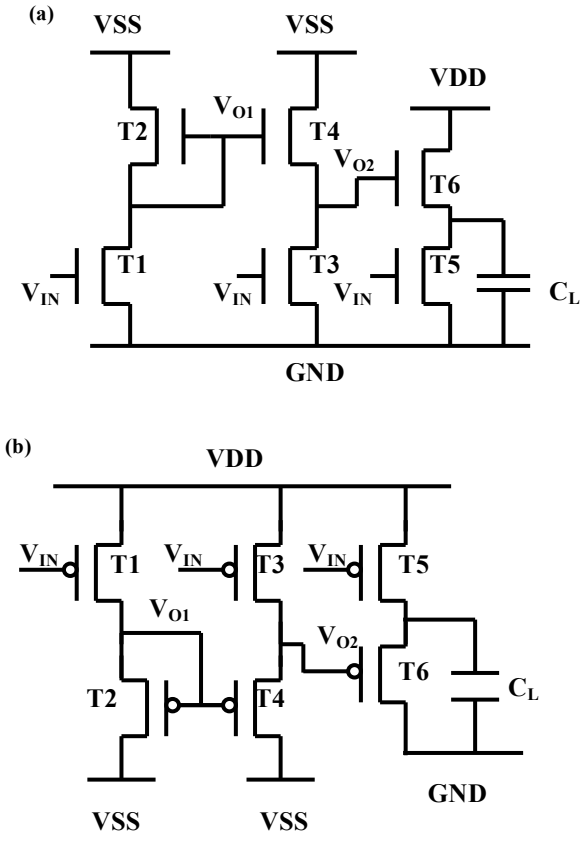


Fig. 5. Schematics of the depletion mode (a) n-type 6-T pseudo-CMOS inverter (b) p-type 6-T pseudo-CMOS inverter.

Figure 5 shows the schematics of the depletion-mode 6-T pseudo-CMOS inverter circuits, in which the first stage is a zero gate voltage transistor. The second stage is a buffer where the gate of T4 is connected with the source of T2. In the last or output stage, the gate of T6 connects with the source of T4. As shown in Fig. 5(a), a negative threshold voltage provides constant current flow by T2. When T1 is on, the zero gate voltage current is much smaller than the pull down current, and thus limits the static current in Stage 1 resulting in a low V_{O1}. When T1 turns on, the current from T2 charges the gate voltage of T4. In conventional 4-T pseudo-CMOS designs, a large channel width is required for the push up transistor in the final stage to drive the load. Hence, the rise time to charge the push up transistor could be long, resulting in a slow response and higher power consumption. Nevertheless, the 6-T pseudo-CMOS design, has a buffer stage containing T3 and T4, which can provide a smaller charging time. The channel width of transistor T4 can be minimum feature size, so that V_{O1} can rise up faster and the larger source voltage of T4 can charge the pull-up transistor T6 quicker, contributing to an improved transient time as well as power efficiency. The depletion mode inverters could be realized using the same technology as the enhancement mode counterpart. According to Chiang *et al.*, the threshold voltage of amorphous semiconductors has a strong dependence on channel length, where a short channel is typically used for depletion mode operation and equivalently, a long channel for enhancement mode [35].

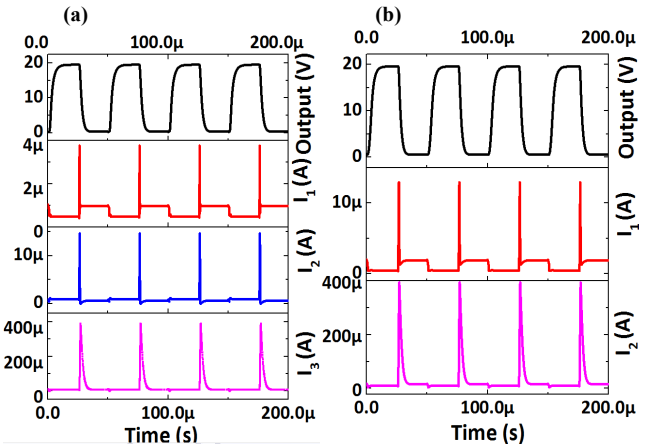


Fig. 6. Dynamic output and current for the (a) depletion mode 6-T pseudo-CMOS inverter (b) depletion mode 4-T pseudo-CMOS inverter.

The results shown in Fig. 6 are based on the transistor size as indicated in Table 5. For fair comparison, the total area of the 6-T pseudo-CMOS circuit is equal to that of the 4-T pseudo-CMOS counterpart and the final stage transistors have the same sizes. As shown in Fig. 6(a) and (b), the addition of the turn on current I_1 = 0.96 μA and I_2 = 0.64 μA is less than the on current in the first stage of the 4-T pseudo-CMOS circuit, I_1 = 1.9 μA. In addition, the on current of the last stage is 8.7 μA, compared to 16.7 μA of the 4-T pseudo-CMOS, which is a 50% improvement in power efficiency.

V. Voltage Transfer Characteristics

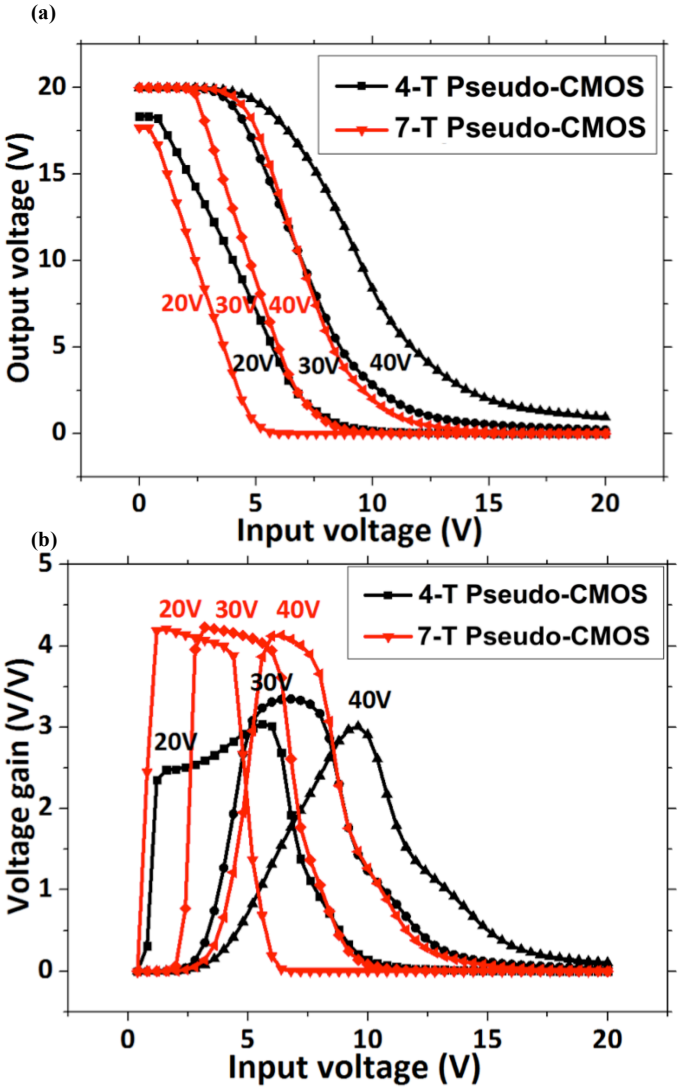


Fig. 7. Enhancement mode inverter (a) VTC and (b) gain for the 7-T pseudo-CMOS (red line) and the 4-T pseudo-CMOS (black line) at different tuning voltages 20V, 30V and 40V.

Fig. 7 shows the enhancement mode transfer characteristics and voltage gain of 7-T pseudo-CMOS and the 4-T pseudo-CMOS. The V_{DD} used for the simulation is 20V. The different curves reflect the different VTCs and gain under different tuning voltages V_{SS}. The 7-T pseudo-CMOS provides a larger voltage gain and steeper VTCs than that of the 4-T pseudo-CMOS. The maximum gain of the 7-T pseudo-CMOS is 4.3, while the maximum gain of 4-T pseudo-CMOS is around 3. The larger gain can be contributed to the feedback effect of transistor T2 and T4. The adjustable post-fabrication tuning voltage can be applied to compensate device variations due to processing and bias-induced instability [12], [36]-[38].

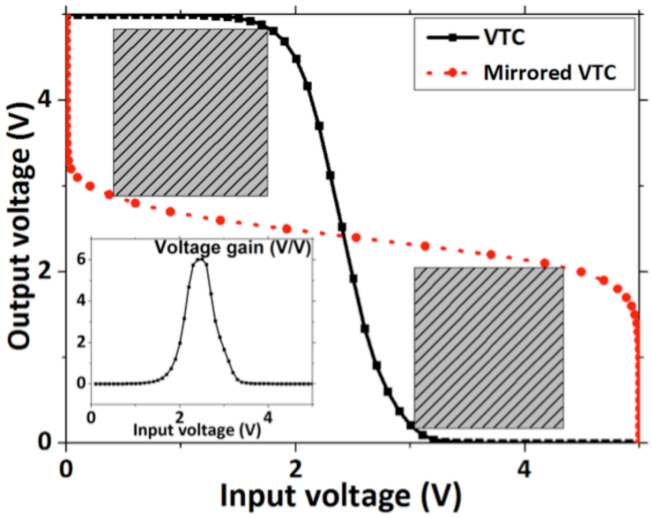


Fig. 8. VTC of the 7-T pseudo-CMOS (black line) and mirrored VTC (red line). Insert: Gain plot derived from the VTC.

Fig. 8 shows the voltage transfer curve of the enhancement 7-T pseudo-COMS with V_{DD} = 5 V, V_{SS} = 15 V and V_T = 2 V. The maximum gain is round 6 when the input voltage is 2.4 V. The noise margin is normalized with V_{DD}: $NM_H=V_{OH}-V_{IH}=0.0915$ V/V and $NM_L=V_{IL}-V_{OL}=0.0875$ V/V, which implies the proposed circuit is a robust design from the standpoint of noise margin.

Fig. 9 shows the transfer characteristics and voltage gain of 6-T pseudo-CMOS and the 4-T pseudo-CMOS with depletion mode. The curves reflect VTCs and gain for different threshold voltages V_T. The 6-T pseudo-CMOS provides a larger voltage gain and steeper VTCs than that of the 4-T pseudo-CMOS. The maximum gain of the proposed inverter is larger than eighty. The larger gain can be attributed to its cascade structure. In addition, with the increase of V_T, the VTC becomes more positive and the gain decreases. This could be explained by the reduction of current flowing through the circuit.

TABLE 5
Transistor Size Of Depletion Mode For Simulation

TFTs		Channel width (μm)	Channel length (μm)
6-T pseudo-CMOS	*T1*	10	10
	T2	10	10
	T3	10	10
	T4	10	10
	T5	200	10
	T6	200	10
4-T pseudo-CMOS	*T1*	40	10
	T2	10	10
	T3	200	10
	T4	200	10

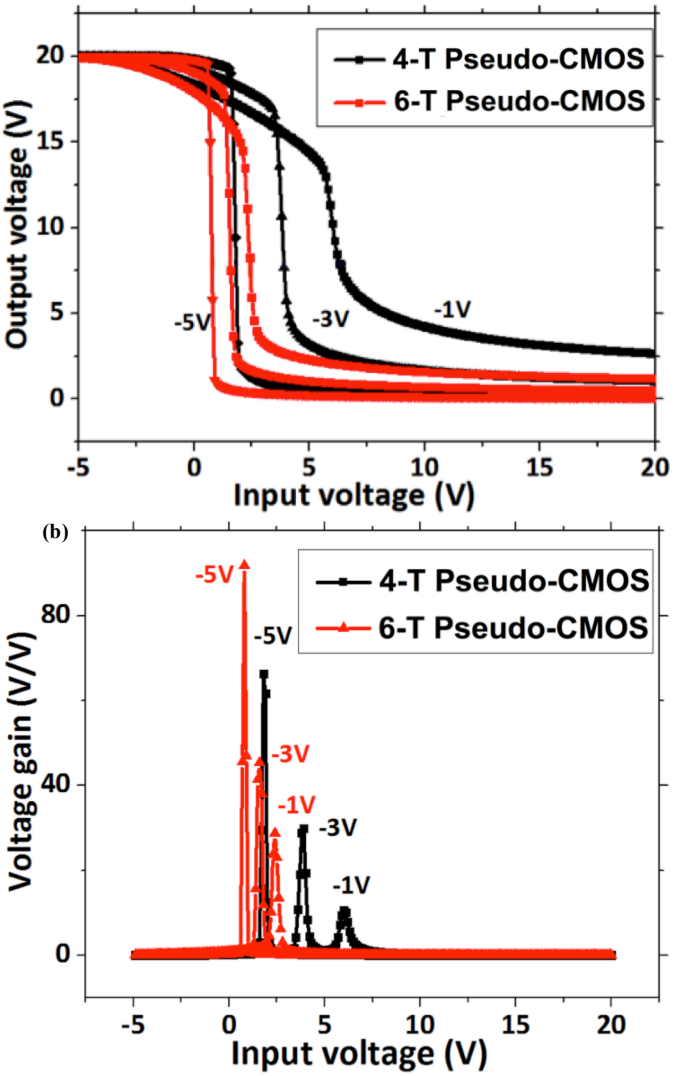
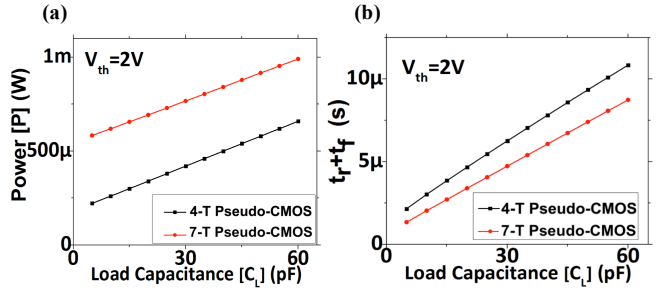


Fig. 9. Depletion mode inverter (a) VTCs and (b) gain for 6-T pseudo-CMOS (red line) and 4-T pseudo-CMOS (black line) with different threshold voltages -1V, -3V and -5V.

Fig. 10 provides the power consumption and the total rise and fall times with respect to load capacitance.



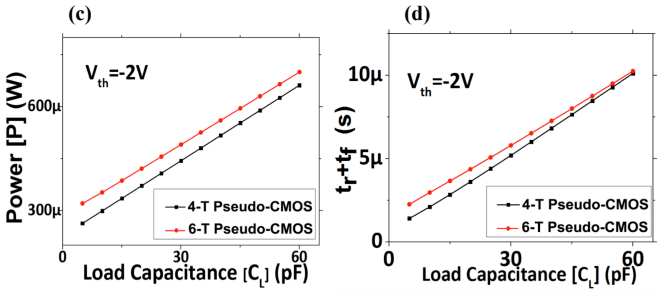


Fig. 10. Power consumption for (a) enhancement mode operation (b) corresponding delay time (c) depletion mode operation and (d) corresponding delay time. The tuning voltage is V_{SS}=30 V at 20 kHz frequency. For fair comparison, the total area of proposed circuit is equal to that of 4-T pseudo-CMOS and the final stage transistors have the same size.

As presented in Fig. 10. (a), the 7-T pseudo-CMOS provides smaller power consumption than the 4-T pseudo-CMOS in enhancement mode. For a 5 pF capacitive load, the 7-T pseudo-CMOS saves 61.33% of total power compared with the 4-T pseudo-CMOS, while for a 60pF load, it uses 67% less power. On the other hand, the 7-T pseudo-CMOS has slightly larger rise and fall time for the same tuning voltage of 4-T pseudo-CMOS. This is due to the reduction of the V_{O3} (V_{SS}-3V_t). V_{O3} in the 7-T pseudo-CMOS is V_{SS}-3V_T when the input is low while V_{O1} in the 4-T pseudo-CMOS circuit is V_{SS}-V_T. Here they are both charging the load capacitance. Hence, the charging current of the 7-T pseudo-CMOS is smaller than that of 4-T pseudo-CMOS, resulting in an increase of the rise time. In terms of fall time, V_{O3} of the 7-T pseudo-CMOS is smaller than V_{O1} of the 4-T pseudo-CMOS, which on the other hand reduce the discharging time. For n-type non-complementary circuits in general, the rise time dominates the total delay time and fall time is negligible. Hence, the delay time of proposed circuits is longer. In addition, relative large overlap capacitance, which is comparable with gate capacitance (C_{ox} = 12 nF/cm^2, C_{ox} = 15.6 pF/cm with L' = 13 um and C_{ov} = 10 pF/cm), cause the incensement of transient time of 7-T pseudo-CMOS, which is discussed in section VI. For C_L = 5 pF, the 7-T pseudo-CMOS spends 0.81 µs more than 4-T pseudo-CMOS and this increases to 2.10 µs with C_L = 60 pF. This is also quantified in sections VI. The power-delay product of the 7-T pseudo-CMOS is 40%, i.e. 18% less than that of the 4-T pseudo-CMOS for 5 pF and 60 pF capacitive loads, respectively, as shown in Figure D1 (a). Improvement in circuit speed can be achieved by decreasing the overlap capacitance. Fig. 10 (c) and (d) show the performance of the 6-T pseudo-CMOS of depletion mode and 4-T pseudo-CMOS of depletion mode. The results indicate that the 6-T pseudo-CMOS provides better power consumption along with less delay time. It consumes 17.92% and 6% less power than the 4-T pseudo-CMOS circuit with C_L = 5 pF and C_L = 60 pF. The rising and falling times of the 6-T pseudo-CMOS is 62.3% that of the 4-T pseudo-CMOS for C_L=5 pF. In terms of power delay product, the 6-T pseudo-CMOS saves 50% and 7% that of the 4-T pseudo-CMOS with C_L = 5 pF and C_L = 60 pF, as shown in Fig. D1 (b).

Because the mobility, operating voltage, threshold voltage and oxide capacitance are all different, it is not possible to conduct a fair comparison between the circuits proposed here and that of conventional CMOS, unless normalization is considered, which is presented in Appendix A.

The normalized power consumption and transient time of MOSFET circuit and TFT circuit are shown in Fig. 11.

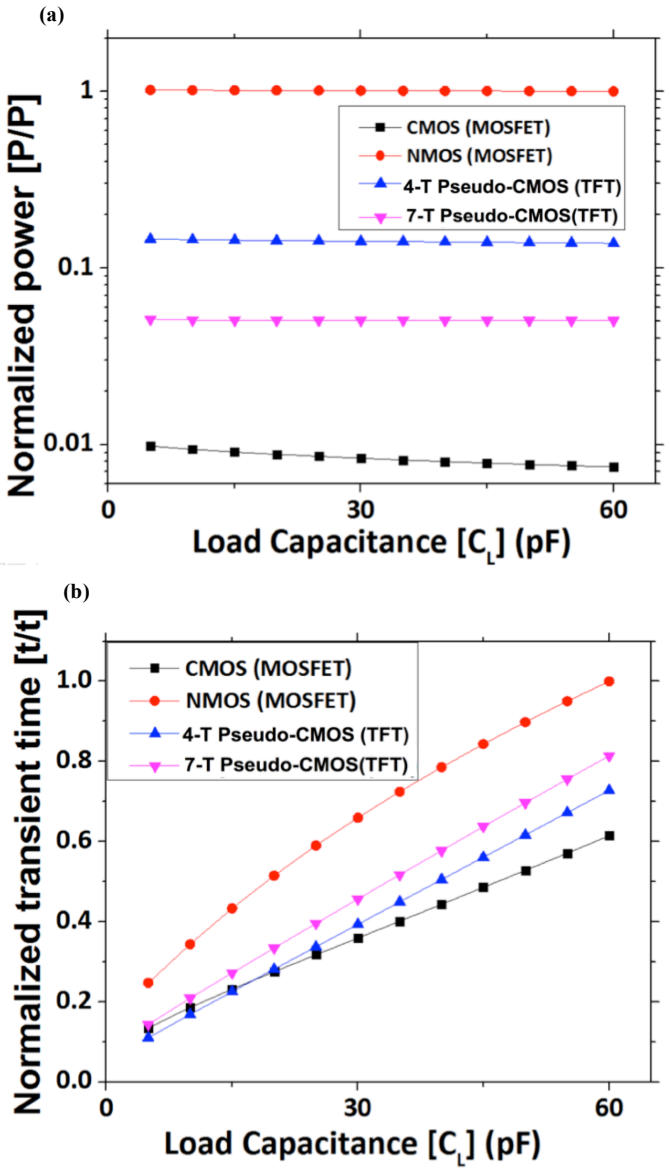


Fig. 11. Normalized (a) power consumption and (b) delay time for the 7-T pseudo-CMOS, 4-T pseudo-CMOS, CMOS, and diode connected inverter configurations,

As indicated in Fig. 11 (a) the normalized power consumption derived form Eq. A7 shows that the NMOS circuit, 4-T pseudo-CMOS circuit and the 7-T pseudo-CMOS circuit are independent of load capacitance. However, normalized power of the CMOS circuit decreases with the increase of load capacitance, which is due to the insufficient charge for load capacitance with large load. We conclude that the normalized CMOS circuit consumes less power than the other three circuits. In average it is more than one order of magnitude less than the 4-T pseudo-CMOS circuit. The 7-T pseudo-CMOS circuit consumes one third of the power consumed by the 4-T pseudo-CMOS circuit and 5% of that consumed by the NMOS circuit, which indicates its high power efficiency among the family of non-complementary inverters. The normalized transient time as derived form Eq. A9 is shown in Fig. 11 (b). It indicates that the CMOS circuit provides the smallest transient time, which contributes to its complementary nature and its low overlap capacitance. However, the pseudo-CMOS circuits show no major difference with CMOS, which indicates that for the same driving current, the delay of the 7-T pseudo-CMOS is comparable with that of CMOS.

VI. Impact of Overlap Capacitance on Circuit Performance

The overlap capacitances for the circuits considered are illustrated in Fig. 12. The total overlap capacitance (C_{ovs}+C_{ovd}) is assumed to be around 2/3 of the gate capacitance in the analysis.

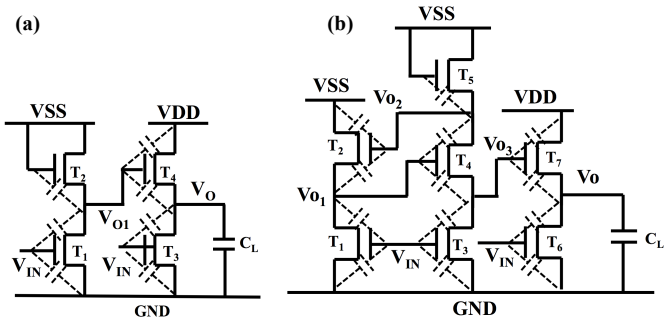


Fig. 12. (a) Enhancement mode 4-T pseudo-CMOS and (b) Enhancement mode 7-T pseudo-CMOS with overlap capacitance

As shown in Fig. 13, with the reduction of overlap capacitance, the 7-T pseudo-CMOS and the 4-T pseudo-CMOS circuits improve their performance in terms of both energy efficiency and delay time. The 7-T pseudo-CMOS consumes 222 µW compared with 584 µW for the 4-T pseudo-CMOS with 10 pF/cm, which is 0.65 pF for the total overlap capacitance. If the overlap capacitance reduces to 32.5 fF, the power consumption of 7-T pseudo-CMOS reduces into 218 µW while that of 4-T pseudo-CMOS is 583 µW. The power consumed due to parasitic capacitance can be divided into two parts: 1) charging of the parasitic capacitance; 2) increasing of the short circuit power consumption due to the rising of charging time (rise time/ fall time). For both the 7-T and 4-T pseudo-CMOS circuits, the first part is the same due to the same total size of transistors. The power reduction can be estimated as:

$$P_{reduce} = \frac{1}{2}\left(t_r + t_f\right)_{reduce} V_{DD} I_{short} f \ . \qquad (3)$$

The difference between the 7-T and 4-T pseudo-CMOS circuits could be estimated as:

$$P_{reduce\_proposed} - P_{reduce\_pseudo}$$
$$= 0.5 \times 0.957\mu s \times 20V \times 25\mu A \times 20Hz$$
$$-0.5 \times 0.197\mu s \times 20V \times 42\mu A \times 20Hz$$
$$= 3.13\mu W$$

which is consistence with the difference of power reduction 3.29 μW as indicated in Fig. 13(a).

As shown in Fig 13 (b), the circuit delay time reduces with decrease in overlap capacitance. Under the condition C_{ov}= 10 pF/cm, the t_r+t_f of the 7-T pseudo-CMOS is 1.6 times that of 4-T pseudo-CMOS. However, the difference decreases with reduction of the overlap capacitance. In the ideal case, with no overlap capacitance, the 7-T pseudo-CMOS uses less time for charging/discharging than 4-T pseudo-CMOS. Thus, with the reduction of overlap capacitance by future proposed new TFT devices structures or fabrication processes, the 7-T pseudo-CMOS can achieve similar speeds. The reason for this is explained by transient analysis. For both circuits, the final stage is the same. Hence, the transient response can be estimated through V_{O1} and V_{O3} respectively as presented in Appendix B.

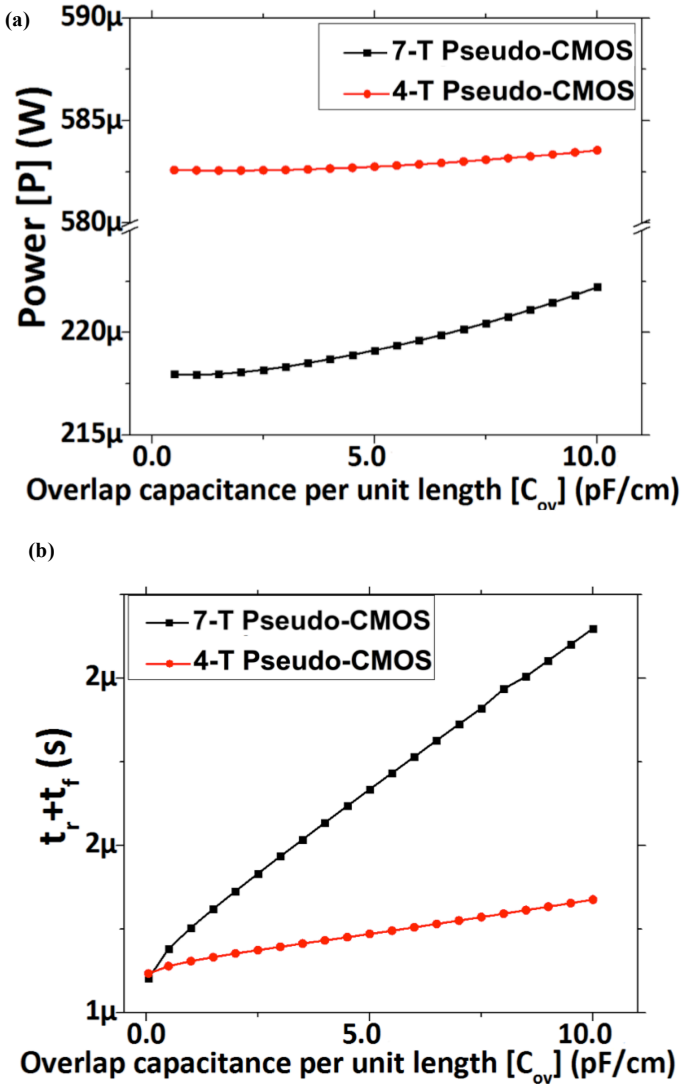


Fig. 13. (a) Power consumption (b) delay time as a function of overlap capacitance per unit length with load capacitance C_L=5pF.

The transient response of 4-T pseudo-CMOS is derived in Eq. (B1). The C' dominates the V_{O1} response, since the size of T4 is five times larger than T1, so the response time decrease with the reduction of overlap capacitance. On the other hand, for the 7-T pseudo-CMOS, as shown in Eq. (B6), the denominators of I_2, I_4, and I_5 has the coefficients K_1+1, K_2+1, K_3+1, which are overlap capacitance dependent. With decreasing C_{ov}, the denominators decrease and if the overlap capacitance equals to 0, Eq. (B6) gets simplified to:

$$\frac{dV_{O3}}{dt} = \frac{I_2}{C_{gs7}} + \frac{I_5}{C_{gs7}}, \qquad (4)$$

Eq. (4) indicates that both I_2 and I_5 charge the gate of T7, so V_{O3} in the 7-T pseudo-CMOS may rise faster than V_{O1} in 4-T pseudo-CMOS. Hence, with decrease of overlap capacitance, the transient time of 7-T pseudo-CMOS decrease faster than that of 4-T pseudo-CMOS. In addition, as shown in Eq. (B6), with the increase of load capacitance, C' increases, so with the (1+K_n) factor, therefore the increase in response time is faster than with 4-T pseudo-CMOS as indicated in Fig.10 (b).

VII. Ring Oscillator

Using the enhancement and depletion mode inverter circuit configurations discussed above, the output of a 5-stage ring oscillator is shown in Fig. 14,

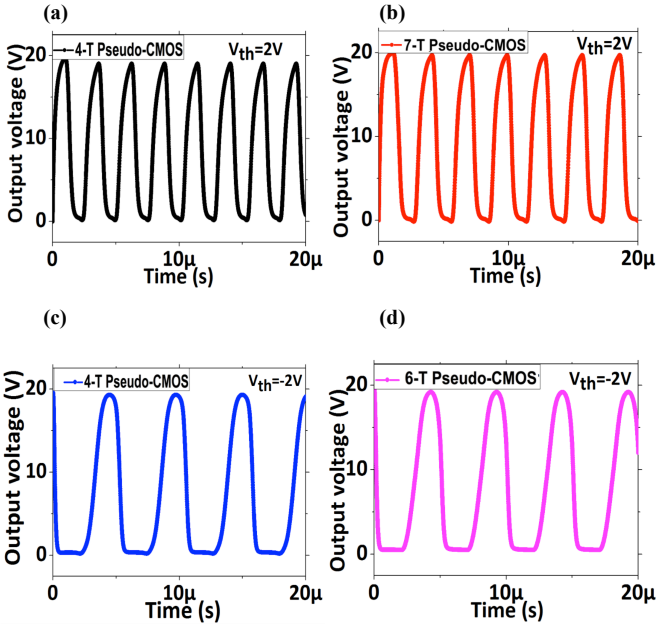


Fig. 14. Voltage output from 5 stage ring oscillator constructed by (a) enhancement mode 4-T pseudo-CMOS with V_{SS} = 30V, (b) enhancement mode 7-T pseudo-CMOS with V_{SS} = 30V (c) depletion mode 4-T pseudo-CMOS with V_{SS} = 30V, (d) depletion mode 6-T pseudo-CMOS with V_{SS} = 30V

for which the frequency is given by [39]:

$$f = \frac{1}{2Nt_d}. \quad (5)$$

Here N is the number of stages and t_d the delay of each inverter circuit. The operation frequency of the five stage ring oscillators and delay of the circuit calculated from Fig. 14. is summarized in Table 6.

TABLE 6
DELAY TIME OF INVERTER CIRCUITS

TFT Mode	Enhancement		Depletion	
Inverter type	4-T Pseudo -CMOS	7-T Pseudo -CMOS	4-T Pseudo -CMOS	6-T Pseudo -CMOS
Frequency	386 kHz	348 kHz	182 kHz	204 kHz
Delay time (ns)	259	287	549	490

From Eq. (5), the operating frequency of the ring oscillator is inversely proportional with the delay of a single stage. The time delay of the 7-T pseudo-CMOS with positive V_T is 28 ns larger than that of the 4-T pseudo-CMOS, as discussed earlier. .In contrast, in depletion mode configuration, the 6-T pseudo-CMOS has a shorter delay time, confirming the states in Section V. The propagation delay of inverter is:

$$t \sim \frac{V_{DD}C_L}{I(V_{DD})}. \quad (6)$$

With the same V_{DD}, the pull-down transistor of the enhancment mode circuit is double that of the depletion mode circuit, which provides a larger $I(V_{DD})$. Hence, the operating frequency of the enhancement mode inverter is larger than that of the depletion mode.

VIII. CONCLUSION

This paper addressed the design challenges associated with TFT-based digital circuits. Novel pseud-CMOS circuit architectures operating in both enhancement and depletion modes with monotype of transistors are presented. The proposed circuit architectures provide low-power consumption, large noise margin and rail-to-rail output performance. In addition, the author presents a method of normalization complementary logics (CMOS) and non-complementary logics. The result indicates that the proposed inverter circuit reduces power consumption by 95% compared with diode-connected inverter circuits. In addition, the author conducted analysis of overlap capacitance on circuit performance, the results indicate with the reduction of overlap capacitance by future proposed new TFT devices structures or fabrication processes, the 7-T pseudo-CMOS can achieve fastest speeds among non-complementary architecture. Thus, the proposed circuits provide a desirable solution for robust flexible electronics and displays, where power consumption is critical.

APPENDIX A

NORMALIZATION OF POWER CONSUMPTION AND TRANSIENT TIME

To conduct a fair comparison, we consider the general transistor model applicable for both CMOS and TFT, which is a simplification of Eq. 1:

$$I_{lin} = \mu_{eff} C_{ox} \frac{W}{L'}(V_{GS} - V_T)V_{DS}$$
$$I_{sat} = \frac{1}{2}\mu_{eff} C_{ox} \frac{W}{L'}(V_{GS} - V_T)^2. \quad (A1)$$

with $\mu_{eff} = \mu_0^* \left(\frac{N_C}{N_C + N_{tc} k T_t} \right) \frac{C_{ox}^{\alpha_p}}{Q_{ref}^{\alpha_p}}$, $L' = L - \Delta L$ and $\alpha_p = 0$.

If normalized with transistor property, Eq. A1 can be recast as:

$$\frac{I_{lin}}{\mu_{eff} C_{ox} \frac{W}{L'} V_{GS}^2} = \left(1 - \frac{V_T}{V_{GS}}\right)\frac{V_{DS}}{V_{GS}}$$
$$\frac{I_{sat}}{\mu_{eff} C_{ox} \frac{W}{L'} V_{GS}^2} = \frac{1}{2}\left(1 - \frac{V_T}{V_{GS}}\right)^2. \quad (A2)$$

If the ratio of the operating voltage and threshold voltage of TFT and MOSFET are set to be the same, i.e.:

$$\frac{V_{GS\_TFT}}{V_{GS\_MOSFET}} = \frac{V_{DS\_TFT}}{V_{DS\_MOSFET}} = \frac{V_{T\_TFT}}{V_{T\_MOSFET}} = \frac{V_{DD\_TFT}}{V_{DD\_MOSFET}}. \quad (A3)$$

the gate voltage and drain voltage could also be set to have the same ratio of drive voltage. Hence, from Eq. A2 and A3, the current can be normalized between TFT and MOSFET.

The total power consumption could be expressed as:

$$P_{total} = P_{dynamic} + P_{short} + P_{static} \quad (A4)$$

where the dynamic power consumption is:

$$P_{dynamic} = C_L V_{DD}^2 f, \quad (A5)$$

which reflects the power required by load and does not reflect circuit property. Only the short circuit power and static power is proportional to the driving voltage and current:

$$\left(P_{total} - P_{dynamic}\right) \sim V_{DD} I. \quad (A6)$$

Thus the normalized power could be expressed as:

$$P' = \frac{P_{total} - P_{dynamic}}{\mu_{eff} C_{ox} \frac{W}{L} V_{DD}^3} \quad \text{(A7)}$$

and the transient time of the circuit as:

$$t \sim \frac{V_{DD} C_L}{I(V_{DD})} \quad \text{(A8)}$$

which can be normalized as:

$$t' = t \frac{\mu_{eff} C_{ox} \frac{W}{L} V_{DD}^2}{V_{DD} C_L} = t \frac{\mu_{eff} C_{ox} \frac{W}{L} V_{DD}}{C_L}. \quad \text{(A9)}$$

APPENDIX B

TRANSIENT TIME ANALYSIS

As shown in Fig. 12 (a) for a falling input, V_{O1} of the 4-T pseudo-CMOS is:

$$\frac{dV_{O1}}{dt} = \frac{I_2}{C' + C_{ovd1} + C_{ovs2}}, \quad \text{(B1)}$$

where I_2 the current through T2, C' the equivalent capacitance seen from the final stage:

$$C' = C_{ovd4} + \frac{(C_{gs4} + C_{ovs4})(C_L + C_{ovd3})}{C_{gs4} + C_{ovs4} + C_L + C_{ovd3}}, \quad \text{(B2)}$$
$$\simeq C_{ovd4} + C_{gs4} + C_{ovs4}$$

For a falling input, the respective V_{O3} of the 7-T pseudo-CMOS at points 1, 2 and 3 are:

$$\left(C_{gs2} + C_{ovs2} + C_{gs4} + C_{ovs4} + C_{ovd4}\right)\frac{dV_{O1}}{dt} = I_2 + \left(C_{gs2} + C_{ovs2}\right)\frac{dV_{O2}}{dt} + \left(C_{gs4} + C_{ov4}\right)\frac{dV_{O4}}{dt}, \quad \text{(B3)}$$

$$\left(C_{gs2} + C_{ovs2} + C_{ovd4} + C_{ovs5} + C_{ovd2}\right)\frac{dV_{O2}}{dt} + I_4 = I_5 + \left(C_{gs2} + C_{ovs2} + C_{ovd4}\right)\frac{dV_{O1}}{dt}, \quad \text{(B4)}$$

$$\left(C_{gs4} + C_{ovs4} + C_{ovd3} + C'\right)\frac{dV_{O3}}{dt} = I_4 + \left(C_{gs4} + C_{ovs4}\right)\frac{dV_{O1}}{dt}, \quad \text{(B5)}$$

From Eq. (B3) (B4) (B5),

$$\frac{dV_{O3}}{dt} = \frac{I_2}{(1+K_1)(C' + C_{ovd3}) + C_1} + \frac{I_4}{(1+K_2)(C' + C_{ovd3}) + C_2}, + \frac{I_5}{(1+K_3)(C' + C_{ovd3}) + C_3} \quad \text{(B6)}$$

where, I_2, I_4, I_5 are the currents through T2, T4, T5, and C' the equivalent capacitance seen from the final stage is:

$$C' = C_{ovd7} + \frac{(C_{gs7} + C_{ovs7})(C_L + C_{ovd6})}{C_{gs7} + C_{ovs7} + C_L + C_{ovd6}} \cdot \quad \text{(B7)}$$
$$\simeq C_{ovd7} + C_{gs7} + C_{ovs7}$$

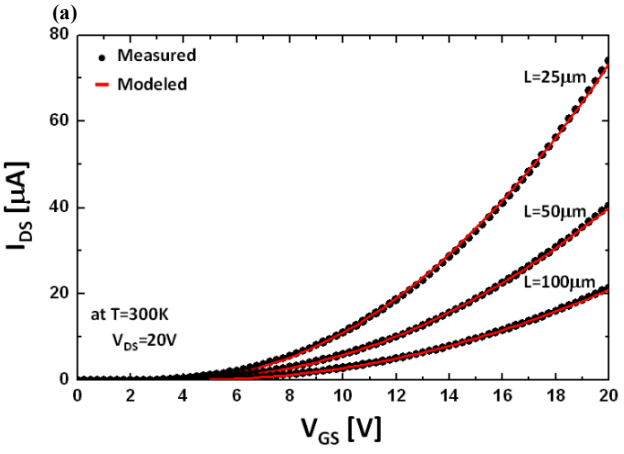
The other parameters are summarized as:

$$K_1 = \frac{C_1}{C_{gs4} + C_{ovs4}}, \; C_1 = (C_{ovs5} + C_{ovd2}) // (C_{gs2} + C_{ovs2} + C_{ovd4}),$$
$$K_2 = \frac{C_2}{C_{ovs5} + C_{ovd2}}, \; C_2 = (C_{gs4} + C_{ovs4}) // (C_{gs2} + C_{ovs2} + C_{ovd4}),$$
$$K_3 = \frac{C_{ovs5} + C_{ovd2}}{C_2}, \; C_3 = C_{ovs5} + C_{ovd2}.$$

APPENDIX C

TRAP-LIMITED CONDUCTION AND PERCOLATION MODELS FOR TFT

The developed trap-limited conduction and percolation models provide good agreement with the measured transistor characteristics as shown in C1.



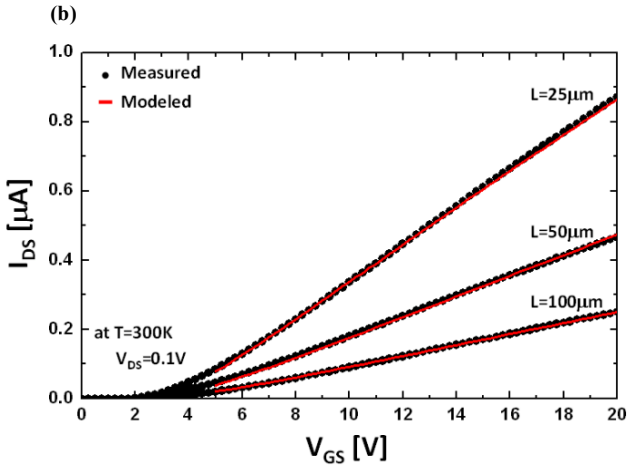


Fig. C1. Comparison between measured and modeled transfer characteristics (I_{DS} vs. V_{GS}) at (a) linear regime with a small drain voltage (V_{DS}) of 0.1V and (b) saturation regime with a high V_{DS} of 20V, respectively. For each regime, a good agreement between measurement and modeling is achieved [30]-[34]

APPENDIX D

POWER DELAY PRODUCT

The power delay product of enhancement mode operation and depletion mode operation are illustrated in Fig. A1.

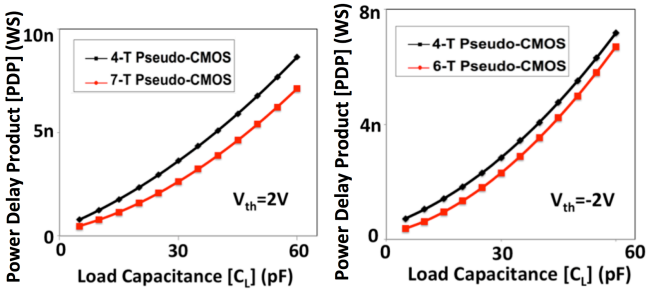


Fig. D1. Power delay product of (a) enhancement mode and (b) depletion mode operation The tuning voltage is V_{SS}=30 V at 20 kHz frequency. For fair comparison, the total area of the proposed circuit is equal to that of 4-T pseudo-CMOS and the final stage transistors have the same size

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REFERENCES

[1] H. Kawaguchi, T. Someya, T. Sekitani and T. Sakurai, "Cut-and-paste customization of organic FET integrated circuit and its application to electronic artificial skin," *IEEE J. Solid-State Circuits*, vol. 40, pp. 177-185, Jan. 2005.

[2] M. Takamiya *et al.*, "Design solutions for a multi-object wireless power transmission sheet based on plastic switches," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, pp. 362–363, Feb. 2007.

[3] T. Sekitani, K. Zaitsu, Y. Noguchi, K. Ishibe, M. Takamiya, T. Sakurai, and T. Someya, "Printed nonvolatile memory for a sheet-type communication system," *IEEE Trans. Electron Devices*, vol. 56, no. 5, pp. 1027-1035, May 2009

[4] E. Cantatore, T. C. T. Geuns, G. H. Gelinck, E. van Veenendaal, A. F. A. Gruijthuijsen, L. Schrijnemakers, S. Drews, and D. M. de Leeuw, "A 13.56-mhz RFID system based on organic transponders," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pp. 84-92, Jan. 2007.

[5] Y. Kurokawa, T. Ikeda, M. Endo, H. Dembo, D. Kawae, T. Inoue, M. Kozuma *et al.*, "UHF RFCPUS on Flexible and Glass Substrates for Secure RFID Systems," in *Proc. IEEE Int. Solid- State Circuits Conf. (ISSCC)*, vol. 43 no. 1, pp. 292-299, Jan. 2008

[6] H. Dembo *et al.,* "RFCPUs on glass and plastic substrates fabricated by TFT transfer technology," in *IEDM Tech. Dig.*, 2005, pp. 1067-1069

[7] R. Rotzoll , S. Mohapatra , V. Olariu , R. Wenz , M. Grigas , K. Dimmler , O. Shchekin and A. Dodabalapur "Radio frequency rectifiers based on organic thin-film transistors," *Appl. Phys. Lett.*, vol. 88, no. 12, pp. 123-502, 2006

[8] H. Klauk, D. J. Gundlach, and T. N. Jackson, "Fast organic thin-film transistor circuits," *IEEE Electron Device Lett.*, vol. 20, pp. 289-291, 1999.

[9] A. Nathan, L. Sungsik, J. Sanghun, and J. Robertson, "Amorphous oxide semiconductor TFTs for displays and imaging," *J. Display Technol.*, vol. 10, no. 11, pp. 917-927, Nov. 2013.

[10] A. Nathan *et al.*, "Flexible electronics: the next ubiquitous platform," *Proc. IEEE,* vol. 100, no. Special Centennial Issue, pp. 1486-1517, 2012

[11] S. Lee, S. Jeon, R. Chaji, and A. Nathan, "Transparent Semiconducting Oxide Technology for Touch Free Interactive Flexible Displays," *Proc. IEEE*, vol. 103, No. 4, pp. 644-664, April 2015.

[12] R. Chaji and A. Nathan, Thin Film Transistor Circuits and Systems. Cambridge, U.K.: Cambridge Univ. Press, 2013.

[13] T. Kamiya and H. Hosono, "Material characteristics and applications of transparent amorphous semiconductors," *NPG Asia Mater.*, vol. 2, no. 1, pp. 15-22, Jan. 2010.

[14] G. H. Gelinck, H. E. A. Huitema, E. van Veenendaal, E. Cantatore, L. Schrijnemakers, J. B. P. H. van der Putten, T. C. T. Geuns, M. Beenhakkers, J. B. Giesbers, B. H. Huisman, E. J. Meijer, E. M. Benito, F. J. Touwslager, A. W. Marsman, B. J. E. van Rens, and D. M. de Leeuw, "Flexible active-matrix displays and shift registers based on solution-processed organic transistors," *Nature Materials*, vol. 3, pp. 106-110, Feb. 2004.

[15] P. van Lieshout, E. van Veenendaal, L. Schrijnemakers, G. Gelinck, F. Touwslager, and E. Huitema, "A flexible 240×320-pixel display with integrated row drivers manufactured in organic electronics," in *IEEE ISSCC Dig. Tech. Papers*, 2005, pp. 578-618.

[16] K. Fukuda, T. Sekitani, T. Yokota, K. Kuribara, T. C. Huang, T. Sakurai, U. Zschieschang, H. Klauk, M. Ikeda, H. Kuwabara, T. Yamamoto, K. Takimiya, K. T. Cheng, and T. Someya, "Organic pseudo-CMOS circuits for low-voltage large-gain high-speed operation," *IEEE Electron Device Lett.*, vol. 32, no. 10, pp. 1448-1450, Oct. 2011

[17] T. C. Huang, K. Fukuda, C. M. Lo, Y. H. Yeh, T. Sekitani, T. Someya, and K. T. Cheng, "Pseudo-CMOS: A design style for low-cost and robust flexible electronics," *IEEE Trans. Electron Devices*, vol. 58, no. 1, pp. 141-150, Jan. 2011.

[18] T. C. Huang, K. Fukuda, C.-M. Lo, Y.-H. Yeh, T. Sekitani, T. Someya, and K.-T. Cheng, "Pseudo-CMOS: A novel design style for flexible electronics," in *Proc. DATE*, 2010, pp. 154-159.

[19] T. C. Huang and K. T. Cheng, "Design for low power and reliable flexible electronics: Self-tunable cell-library design," *J. Display Technol.*, vol. 5, no. 6, pp. 206-215, Jun. 2009.

[20] H. Klauk, U. Zschieschang, J. Pflaum, and M. Halik, "Ultralow- power organic complemetary circuits," *Nature*, vol. 445, pp. 745-748, 2007.

[21] I. Nausieda, K. Ryu, D. He, A. Akinwande, V. Bulovic, and C. Sodini, "Dual threshold voltage integrated organic technology for ultralow-power circuits," in *IEDM Tech. Dig.*, 2009, pp. 1-4. DOI: 10.1109/IEDM.2009.5424345.

[22] P. Servati, K. S. Karim, and A. Nathan, "Static characteristics of a-Si:H dual-gate TFTs," *IEEE Trans. Electron Devices*, vol. 50, pp. 926-932, 2003.

[23] F. M. Li, Y. Vygranenko, S. Koul, and A. Nathan. "Photolithographically defined polythiophene organic thin-film transistors." *J. Vac. Sci. Technol. A*, vol. 24, no. 3, pp. 657-662, 2006.

[24] K. Myny, M. J. Beenhakkers, N. A. J. M. van Aerle, G. H. Gelinck, J. Genoe, W. Dehaene, and P. Heremans, "Unipolar organic transistor circuits made robust by dual-gate technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 1223-1230, May 2011.

[25] A. Dindar , "Metal-oxide complementary inverters with a vertical geometry fabricated on flexible substrates", *Appl. Phys. Lett.*, vol. 99, no. 17, pp. 172104-1-172104-3, 2011.

[26] H. Yabuta, N. Kaji, R. Hayashi, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano and H. Hosono "Sputtering formation of p-type SnO thin-film transistors on glass toward oxide complimentary circuits", *Appl. Phys. Lett.*, vol. 97, pp. 072111-1-072111-3, 2010.
[27] D. J. Gundlach, K. P. Pernstich, G. Wilckens, M. Grüter, S. Haas, and B. Batlogg, "High mobility n-channel organic thin-film transistors and complementary inverters," *J. Appl. Phys.*, vol. 98, no. 6, p. 064502, Sep. 2005.
[28] E. Striter and T. Gunther, "A microprocessor architecture for a changing world: The Motorola 68000," Computer, vol.12, no. 2, pp. 43-52, Feb. 1979.
[29] A. Nathan, A. Kumar, K. Sakariya, P. Servati, S. Sambandan, and D. Striakhilev, "Amorphous silicon thin film transistor circuit integration for organic LED displays on glass and plastic," *IEEE J. Solid-State*
[30] S. Lee, A. Ahnood, S. Sambandan, A. Madan, and A. Nathan, "Analytical field-effect method for extraction of subgap states in thin-film transistors," *IEEE Electron Device Lett.,* vol. 33, no. 7, pp. 1006-1008, Jul. 2012.
[31] S. Lee and A. Nathan, "Localized tail state distribution in amorphous oxide transistors deduced from low temperature measurements," *Appl. Phys. Lett*., vol. 101, Sep. 2012, Art. ID 113502.
[32] S. Lee, D. Striakhilev, S. Jeon, and A. Nathan, "Unified analytic model for current-voltage behavior in amorphous oxide semiconductor TFTs," *IEEE Electron Device Lett*., vol. 35, no. 1, pp. 84-86, Jan. 2014.
[33] S. Lee, Y. Yang, and A. Nathan, "Modeling Current-Voltage Behaviour in Oxide TFTs Combining Trap-limited Conduction with Percolation," Digest of Technical papers, *International Symposium, Display Week 2013*, vol. 44, no. 1, pp. 22-25, June 2013.
[34] S. Lee, A. Nathan, Y. Ye, Y. Guo, and J. Robertson, "Localized States and Electron Mobility in Amorphous ZnON Thin Film Transistors," *Sci. Rep.*, vol. 5, pp.13467, 2015.
[35] C. S. Chiang, C. Y. Chen, J. Kanicki, and K. Takechi, "Investigation of intrinsic channel characteristics of hydrogenated amorphous silicon thin-film transistors by gated-four-probe method," *Appl. Phys. Lett.*, vol. 72, no. 22, pp. 2874–2876, Jun. 1998.
[36] K. Jeong, H. W. Yang, J. H. Jeong, Y.-G. Mo, and H. D. Kim, "Origin of threshold voltage instability in indium-gallium-zinc oxide thin film transistors," *Appl. Phys. Lett.*, vol. 93, pp. 123508-1-123508-3, 2008.
[37] T. Kamiya, K. Nomura, and H. Hosono, "Origins of high mobility and low operation voltage of amorphous oxide TFTs: Electronic structure, electron transport, defects and doping," *J. Display Technol.*, vol. 5, no. 7, pp. 273-288, Jul. 2009.
[38] W. T. Chen, S. Y. Lo, S. C. Kao, H. W. Zan, C. C. Tsai, J. H. Lin, C. H. Fang, and C. C. Lee, "Oxygen-dependent instability and annealing/ passivation effects in amorphous In–Ga–Zn–O thin-film transistors," *IEEE Electron Device Lett.*, vol. 32, no. 11, pp. 1552-1554, Nov. 2011.
[39] S. Docking and M. Sachdev, "An analytical equation for the oscillation frequency of high-frequency ring oscillators," *IEEE J. Solid-State Circuits*, vol. 39, no. 3, pp. 533-537, Mar. 2004.

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