Instability Mechanisms in Amorphous Oxide Semiconductors Leading to a Threshold Voltage Shift in Thin Film Transistors

A. Flewitt and K. M. Niang

Department of Engineering, Cambridge University, Cambridge, CB3 0FA, UK

Amorphous indium gallium zinc oxide (a-IGZO) has been successfully employed commercially as the channel layer in thin film transistors (TFTs) for active-matrix flat panel displays. However, these TFTs are known to suffer from a threshold voltage shift upon application of a gate bias. The threshold voltage shift is reversible through annealing. A similar phenomenon is observed in other TFTs with an amorphous oxide semiconductor channel. The migration of oxygen vacancies is proposed as being the microscopic mechanism causing this effect as it can lead to a change in the equilibrium distribution of defect states in the band gap of the semiconductor. This would manifest itself as a reversible threshold voltage shift in the TFT transfer characteristics, as observed experimentally.

Introduction

Amorphous oxide semiconductors (AOSs) have emerged as the leading alternative to silicon thin film materials for the channel layer in thin film transistors (TFTs) (1, 2). A key reason for this is that TFTs fabricated using AOSs, such as amorphous indium gallium zinc oxide (a-IGZO) or amorphous zinc tin oxide (a-ZTO), have a much higher field-effect mobility than amorphous silicon. However, like amorphous silicon, under some circumstances AOS TFTs suffer from a threshold voltage shift upon application of a gate bias (3, 4). This is a significant problem if the devices are to be used to control active matrix displays, such as those based on organic light emitting diodes where it is desired to accurately control the current through the diode using the gate voltage applied to a TFT, or in logic circuits.

In this paper, the underlying mechanisms leading to a threshold voltage shift in TFTs is reviewed. The method of quantitatively measuring the threshold voltage shift process is then discussed before a summary of previously-published data on the measurement of the threshold voltage shift in AOS TFTs is presented. This leads to a set of requirements that any microscopic model for the underlying mechanism for the threshold voltage shift proves must satisfy. Finally, a model based on the migration of oxygen vacancies is discussed with consequent approaches for engineering more stable AOS TFTs.

Generic Mechanisms for Threshold Voltage Shift

The TFT is an insulated-gate field-effect transistor in which a dielectric thin film (commonly either silicon dioxide or silicon nitride) separates a metal gate from the semiconductor channel. It should be noted that most of the AOSs, including a-IGZO, have a charge neutrality level that sits close to the conduction band, and therefore these

materials are naturally n-type (5). Furthermore, the disordered nature of these materials means that there are a significant number of states within the band gap. Therefore, AOS TFTs are normally operated as n-channel accumulation-mode or depletion-mode devices.

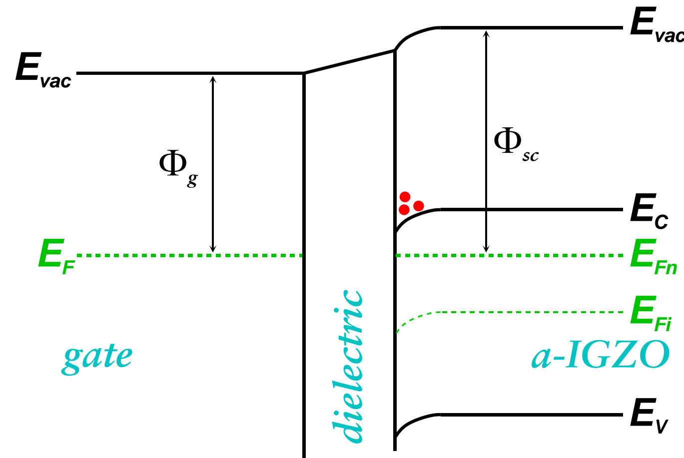


Figure 1. The band diagram of a metal gate – dielectric – AOS semiconductor structure. The Fermi energy level in both the metal gate, E_F, and the semiconductor, E_{Fn}, is shown. For the semiconductor, the middle of the band gap is indicated by E_{Fi} as a guide to the eye. Downward band bending at the semiconductor/dielectric interface means that charge is accumulated here in the conduction band (indicated by the dots).

From the generic energy level diagram of this type of structure in Figure 1, it is clear that the difference in the work function between the metal gate material, Φ_g, and the semiconductor, Φ_{sc}, has a significant influence on the degree of band bending when the gate-source voltage, V_{gs}, and the drain-source voltage, V_{ds}, are both 0 V. This also affects the threshold voltage, V_{th}, as a consequence. For example, under the situation shown where $\Phi_{sc} > \Phi_g$ there is significant downward band bending in the semiconductor at the dielectric interface, resulting in charge accumulation. The TFT will therefore be 'on' in this situation, and will require the application of a negative V_{gs} in order to turn it 'off' (i.e. it is operating as a depletion-mode device with a negative V_{th}). The presence of other charge, either trapped in the dielectric, Q_i, or in defects in the semiconductor at the interface with the dielectric, Q_t, will also affect V_{th}.

These different influences on V_{th} may be combined into a single expression

$$V_{th} = \frac{\Phi_g - \Phi_{sc}}{e} - \frac{Q_i}{C_i} - \frac{Q_t}{C_i} \qquad [1]$$

where e is the electronic charge and C_i is the capacitance per unit area of the dielectric. For a change in the threshold voltage of a TFT to occur as a result of the application of a gate bias, at least one of the terms in equation (1) must be changing. One possibility is that charge is being trapped or released either in the dielectric or at the semiconductor/dielectric interface, affecting Q_i or Q_t respectively. The only other realistic possibility is that Φ_{sc} is changing and this must be driven by some change in the density of states in the band gap of the semiconductor.

There have been many experimental studies of the threshold voltage shift in AOS TFTs, and all of these mechanisms have been observed in different devices for particular stressing conditions (6). It is possible to engineer the dielectric material and its interface with the semiconductor to eliminate charge trapping effects for typical stressing conditions, and when this is done, the experimental situation simplifies as only the processes affecting the AOS itself remain, and this is the subject of the rest of this work.

Measurement of the Threshold Voltage Shift

Quantitative measurement of the threshold voltage shift in TFTs requires the initial threshold voltage of the device under test to be known (at time $t = 0$) and then as a function of time thereafter for a particular gate bias stress condition.

The first point to address is the appropriate selection of the bias stress conditions. It is a change in the Fermi energy in the AOS which drives the threshold voltage shift process as this moves the semiconductor out of its initial equilibrium state. In order to be able to quantitatively compare bias stressing on different devices (and even in different materials) it is critical that the semiconductor always experiences the same stressing conditions. In practice, this means that there should always be the same electric field at the semiconductor-dielectric interface, and this field should be perpendicular to the plane of the interface. To achieve this, the threshold voltage must first be measured, and then a stressing gate-source voltage calculated to always give the same electric field above the threshold voltage at the semiconductor-dielectric interface. For the work published by the authors, the stressing gate-source voltage is always chosen to give an electric field at the interface of 1 MV cm^{-1} above the threshold voltage.

The second point is to determine a method for measuring the threshold voltage as a function of time during the bias stressing process. A simple way of achieving this is to perform a gate transfer measurement (i.e. a sweep of V_{gs} for a constant V_{ds} whilst measuring the drain-source current, I_{ds}). However, whilst this measurement is being performed, the device is no longer being subjected to the stress condition and the threshold voltage may start to recover. As the threshold voltage needs to be measured many times in order to be able to perform a quantitative analysis, there is a cumulative effect of performing the multiple gate transfer measurements that are required, and this can become very significant. For negative bias stress (NBS) measurements, there is little alternative but to accept this effect. However, for the more common positive bias stress (PBS) an alternative approach is to apply a small V_{ds} at the same time as applying the stressing gate-source voltage. It is important that the application of V_{ds} does not significantly change the electric field at the semiconductor-dielectric interface, and so it should be chosen to be just sufficient to yield a measurable I_{ds}. Under these conditions, the device is operating in the linear regime where

$$I_{ds} = \frac{C_i \mu_{FE} W}{L}\left[\left(V_{gs} - V_{th}\right)V_{ds} - \frac{V_{ds}^2}{2}\right] \qquad [2]$$

where μ_{FE} is the field-effect mobility, and W and L are the channel width and length respectively. Therefore, if the bias stressing process does not cause the field-effect

mobility to change, the threshold voltage shift, ΔV_{th}, may simply be determined from equation (2) by measuring the change in I_{ds} with time according to

$$\Delta V_{th} = V_{th}(t) - V_{th}(0) = \frac{L}{C_i \mu_{FE} W V_{ds}} \left[I_{ds}(0) - I_{ds}(t) \right] \qquad [3]$$

where $I_{ds}(0)$ and $I_{ds}(t)$ are the drain-source current initially and after a stressing time t respectively. This method allows continuous measurement of the threshold voltage shift without perturbing the bias stressing conditions themselves. A typical bias stress curve that results from this measurement is shown in Figure 2.

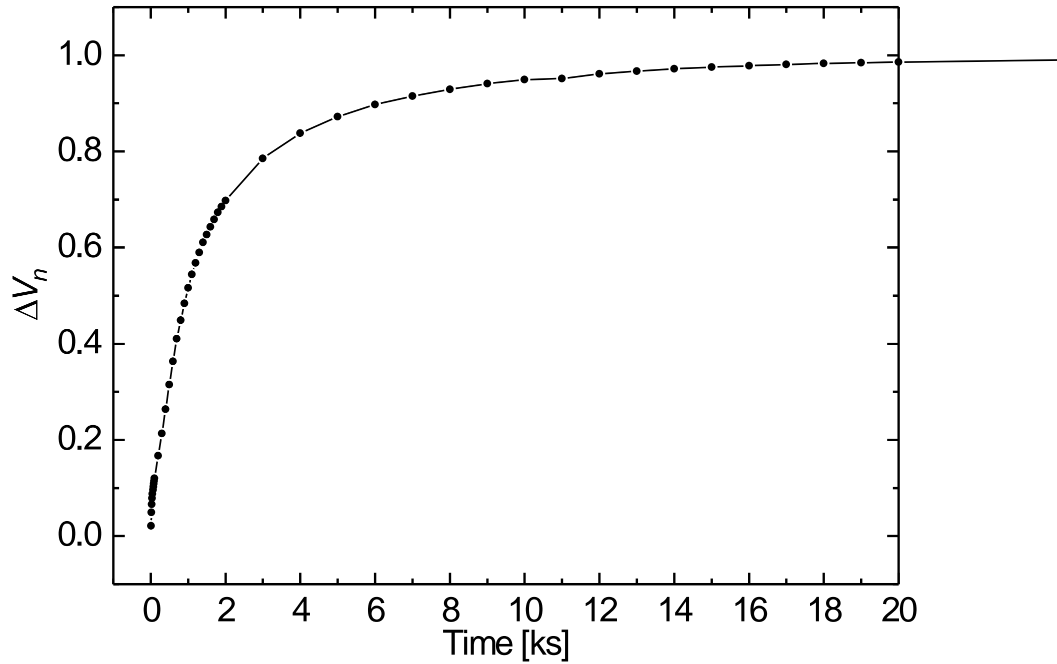


Figure 2. The normalized threshold voltage shift, ΔV_n, as a function of time for an a-IGZO TFT measured at 105 °C (3). The normalized threshold voltage shift is defined as $\Delta V_n = V_{th}(t = \infty) - V_{th}(0)$.

The third point is to determine the total length of time for which the bias stress should be measured. Upon application of the stressing voltage, the sudden change in operating conditions from the initial equilibrium will result in the most rapid rate of change in V_{th}; thereafter, the rate of change will decrease until a new equilibrium is established, as shown in Figure 2. In order to carry out a quantitative extraction of information from the measurement, it is important that the new equilibrium V_{th} to which the measurement is tending can be established with accuracy. If the measurement is performed at room temperature, this may require the measurement to be carried out for a period of several weeks. However, by increasing the temperature, the measurement period can be significantly reduced. The temperature should not be sufficiently high to cause annealing

effects, but even measurement in the range of 60 °C to 120 °C can reduce the time required to a few days and even less than 24 hours.

Thermalisation Energy Analysis of the Threshold Voltage Shift

Having obtained continuous data on the threshold voltage shift as a function of time, it is possible to perform a quantitative energetic analysis using the thermalization energy concept. Assuming that the TFT under test has a high quality dielectric and dielectric-semiconductor interface (as discussed previously) then the threshold voltage shift is caused by some microscopic process occurring in the AOS. Figure 2 shows that it takes a finite time for the TFT to respond to a change in the electric field at the dielectric-semiconductor interface and establish a new equilibrium. Therefore, some energy barrier must exist to this microscopic process occurring. The greater the energy barrier, then statistically it should take a longer time for the process to occur. This can be expressed as a thermalization energy, E_{th}, where

$$E_{th} = kT \ln(\nu t) \quad [4]$$

with k being the Boltzmann constant, T being the temperature and ν being the attempt-to-escape frequency (the number of times per second that the system locally attempts to overcome the energy barrier)(7). Therefore, the threshold voltage shift as a function of time can be converted into a threshold voltage shift as a function of energy as long as ν is known. This can be achieved by performing the threshold voltage shift measurement at several temperatures and replotting the data for different 'guessed' values of ν. When the correct value of ν is chosen, the data from the measurements performed at different temperatures will all lie on the same universal curve. For a-IGZO TFTs, ν is found to be 10^7 Hz (3), and this allows the data in Figure 2 to be replotted as a function of energy as shown in Figure 3. The differential of this curve (also shown in Figure 3) is therefore the distribution of energy barriers to the microscopic mechanism causing the threshold voltage shift.

The authors have previously published the results of positive bias stress analysis on bottom gate a-IGZO TFTs (3), and on bottom gate amorphous zinc tin oxide (a-ZTO) TFTs (4). The authors have also previously re-analyzed data on negative bias stressing of bottom gate a-IGZO TFTs published by Chowdhury et al. (8, 9). In all cases, an attempt-to-escape frequency ~10^7 Hz and an energy barrier of ~0.75 eV is extracted. This suggests that the same basic microscopic process is occurring in all of these cases.

Microscopic Mechanism for the Threshold Voltage Shift Process

Based on the results from the thermalization energy analysis of the threshold voltage shift in a-IGZO and a-ZTO TFTs, the authors have previously suggested five requirements that any microscopic model for the mechanism causing this process must satisfy (3):

1. a negative shift in the threshold voltage occurs for negative gate bias and a positive shift occurs for positive gate bias;
2. illumination with light is required to induce a negative threshold voltage shift, whereas positive threshold voltage shifts occur both with and without illumination;

3. the threshold voltage shift is metastable, and the rate of shift is strongly temperature-dependent in the range from room temperature up to ~400 K when structural changes are not occurring;

4. the energy barrier to the instability mechanism is ~0.75 eV; and

5. there is an attempt-to-escape frequency of ~10^7 s^{-1} associated with the instability process.

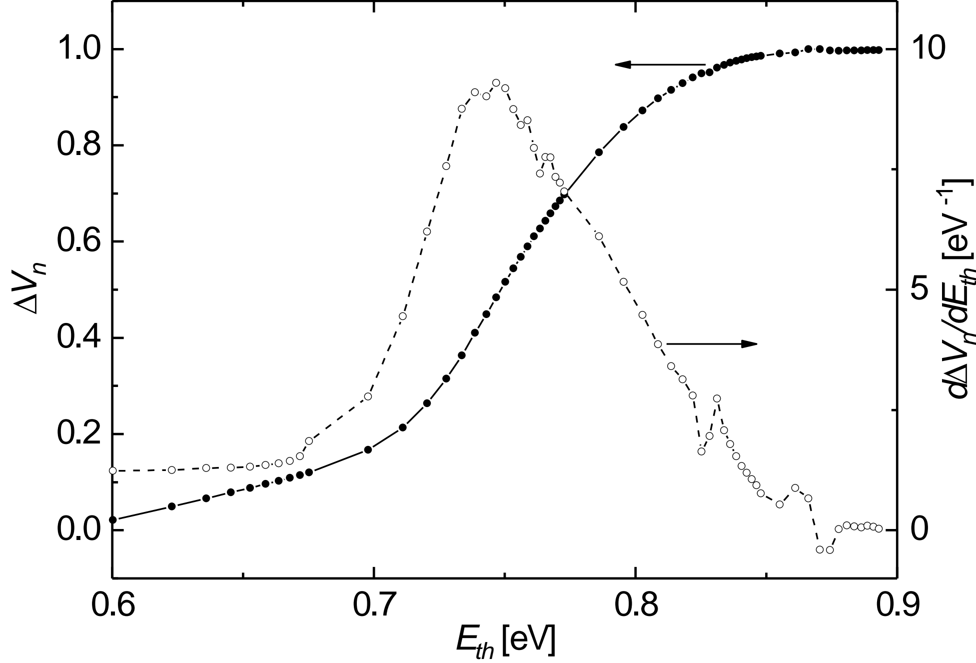
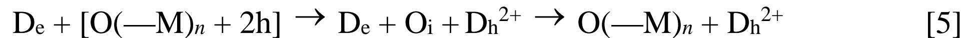


Figure 3. The normalized threshold voltage shift, ΔV_n, as a function of thermalization energy for an a-IGZO TFT measured at 105 °C (3) (solid black circles ●) and the first differential with respect to energy showing the distribution of energy barriers to the threshold voltage shift process (open circles ○).

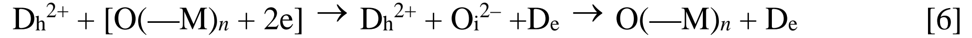
Based on these requirements, the authors have proposed a microscopic mechanism for the threshold voltage shift process that is based on the migration of oxygen vacancies (9). It uses the fact that AOSs all suffer from oxygen vacancies and these produce states which lie in the band gap. For the case of zinc-based AOSs, oxygen vacancy states may either be uncharged (V_O) or 2+ charged (V_O^{2+}). By definition, the V_O^{2+} states must lie higher in the band gap than V_O states as the former are unoccupied by electrons. Therefore, oxygen vacancy defects that are formed in the V_O state are called D_e states and those formed in the V_O^{2+} state are called D_h states. As discussed earlier, a change in the density of states of a semiconductor will lead to a threshold voltage shift. Therefore, a process that converts D_e states to D_h states or vice versa will yield a threshold voltage shift. In this model, it is proposed that the migration of oxygen vacancies can mediate these transitions. For example, a D_e state may be converted to a D_h state by the migration of an oxygen vacancy as follows:



$$D_e + [O(\text{—}M)_n + 2h] \rightarrow D_e + O_i + D_h^{2+} \rightarrow O(\text{—}M)_n + D_h^{2+} \qquad [5]$$

where $O(\text{—}M)_n$ is an n-coordinated oxygen atom neighboring the D_e site, $[O(\text{—}M)_n + 2h]$ represents -hole localization close to such a site, and O_i is the oxygen atom migrating in

the opposite direction to the movement of the oxygen vacancy. Likewise, the reverse process for converting D_h states to D_e states is:



$$D_h^{2+} + [O(—M)_n + 2e] \rightarrow D_h^{2+} + O_i^{2-} + D_e \rightarrow O(—M)_n + D_e \qquad [6]$$

In this case O_i^{2-} is a negatively-charged oxygen ion.

In practice, both of the processes represented by equations (5) and (6) will be taking place all the time. However, if the system is in equilibrium, then there will be no overall change in the mid-gap density of states. However, if the Fermi level is changed, then this will favor one reaction over the other with a consequent change in the density of states until a new equilibrium is established. Positive bias stress results in the Fermi energy being raised towards the conduction band edge. Conduction band tail states become occupied with localized electrons. This is the condition represented by $[O(—M)_n + 2e]$. Therefore, equation (6) is favored and the number of D_e states is increased at the expense of the number of D_h states being reduced. The Fermi level is then forced to a lower energy, and a higher threshold voltage results, as observed experimentally.

This process is consistent with the attempt-to-escape frequency of ~10^7 Hz. It is normally expected that the attempt-to-escape frequency will be of the order of phonon frequencies as this is the oscillation frequency of bonds in a solid, and a simple view of a defect creation process is that an attempt is made to break a bond every time it oscillates. However, for equation (6) to occur, electrons must be localized close to the vacancy migration site. Only if the electrons are always localized close to this site would the attempt-to-escape frequency be 10^{13} Hz. The actual frequency of 10^7 Hz is therefore a reflection that the electrons are localized over a much larger distance (10 to 20 nm) around the migration site (9, 10). Furthermore, the energy barrier of ~0.75 eV therefore represents the energy barrier to vacancy migration.

This insight allows us to consider how the stability of AOSs might be improved. One possibility would be to increase the barrier to vacancy migration. This might be achieved either by changing the stoichiometry of the AOS significantly. Both the a-IGZO and a-ZTO materials measured to date are significantly zinc-based, and therefore it is unsurprising that the oxygen vacancy migration energy is similar in both cases. However, materials which are not zinc-based may have a higher energy barrier. There may also be ways of increasing the stability of oxygen vacancies through the addition of impurities which remove the less stable oxygen vacancies. The other possibility is to reduce the attempt-to-escape frequency by increasing the localization length of electrons. This will be related to the medium-range order in the AOS, and it is possible that this could be influenced by using alternative deposition techniques which reduce the amount of disorder that is present.

Conclusions

All semiconductors are unstable to some degree (even silicon) and AOSs are no exception. However, the question is whether it is possible to engineer a specific semiconductor so that the instability is sufficiently small to enable its use in given applications. For AOSs, oxygen vacancy migration is a possible microscopic process that may lead to bias stress instability in TFTs. This cannot be completely eliminated, but it may be mitigated by engineering materials with a high oxygen vacancy migration energy

or by increasing the localization length of carriers through control of the medium-range order in the material.

Acknowledgments

The support of this work by the Engineering and Physical Sciences Research Council (EPSRC) through project EP/M013650/1 is acknowledged. Additional data related to this publication is available at the DSpace@Cambridge data repository (www.repository.cam.ac.uk).

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