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Supporting Information

A Vertical Organic Transistor Architecture for Fast Nonvolatile Memory

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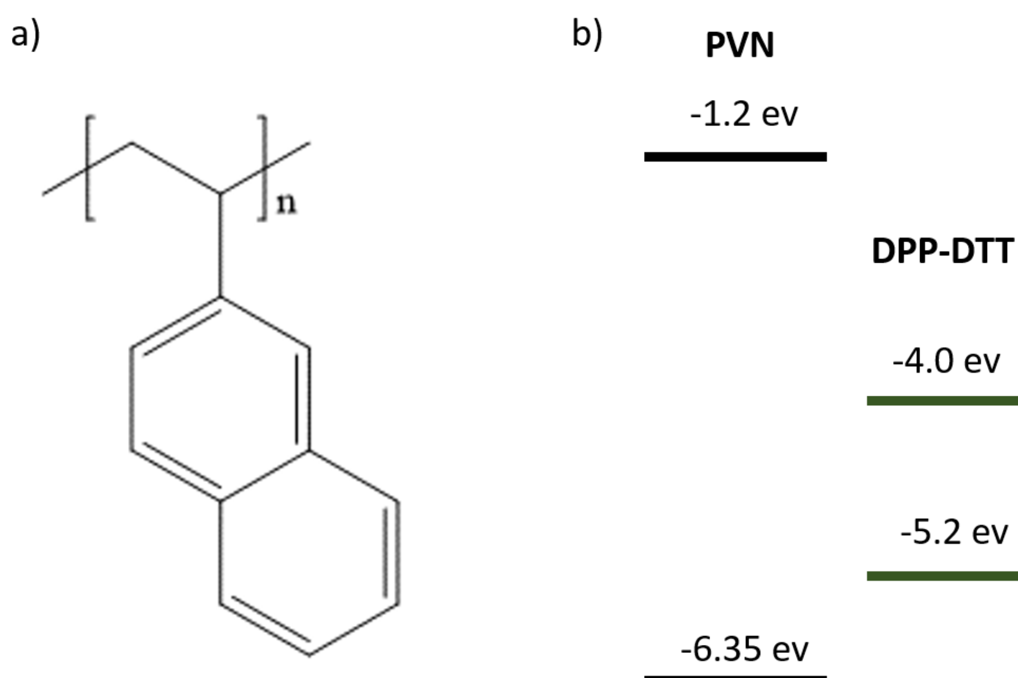

Figure. S1. (a) Chemical structure of PVN, (b) energy diagram of PVN [45] and DPP-DTT.

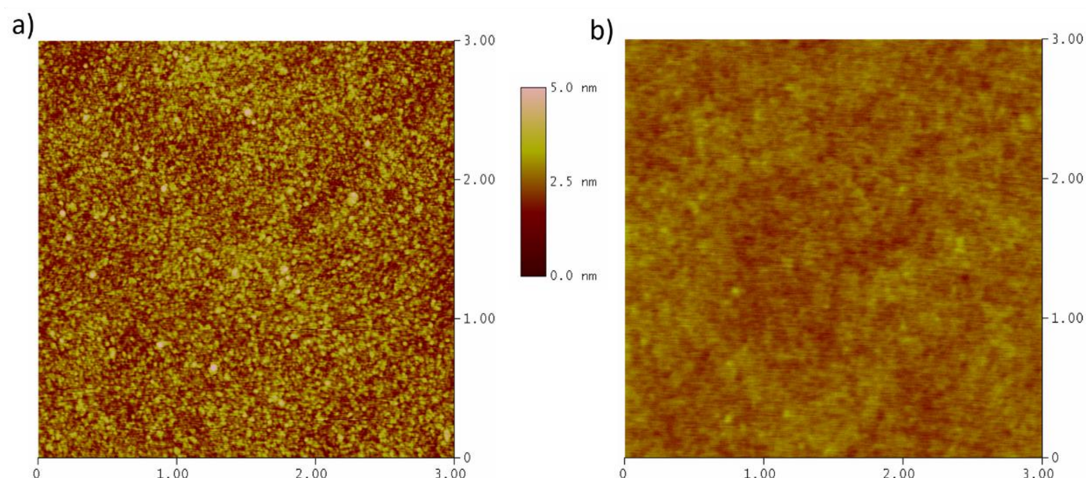

Figure. S2. AFM images of (a) AlOx, and (b) PVN. The rms roughness (*Rq*) is 0.57 nm for AlOx and 0.209 nm for PVN.

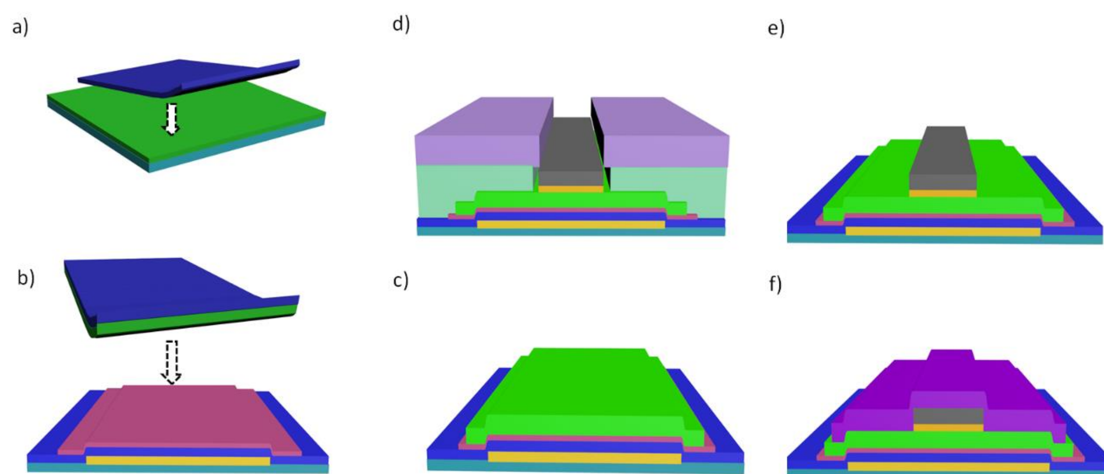

Figure. S3. Schematic illustration of process sequence for device fabrication (a) Transfer of DPP-DTT from silicon substrate onto PDMS stamp; (b) printing of DPP-DTT onto PVN/AlO_x/Au substrate to produce structure in (c). (d) Precise patterning of Cu/LiF by photolithography on top of DPP-DTT to produce (e), (f) subsequent deposition of pentacene.

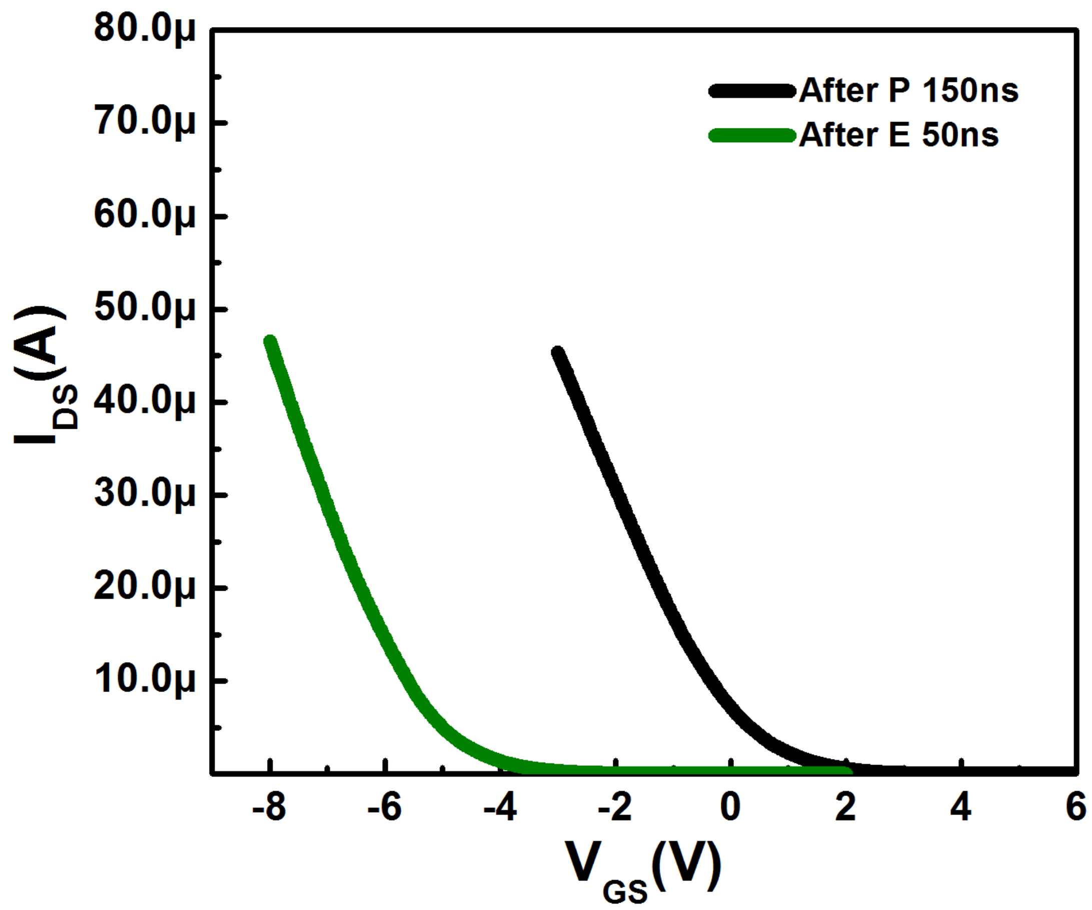

Figure. S4. Transfer curve shifts of AVM after programming for 150ns at V_{GS} = 35V and erasing for 50ns at V_{GS} = -35V. In these measurement the drain is set floating during programming and erasing.

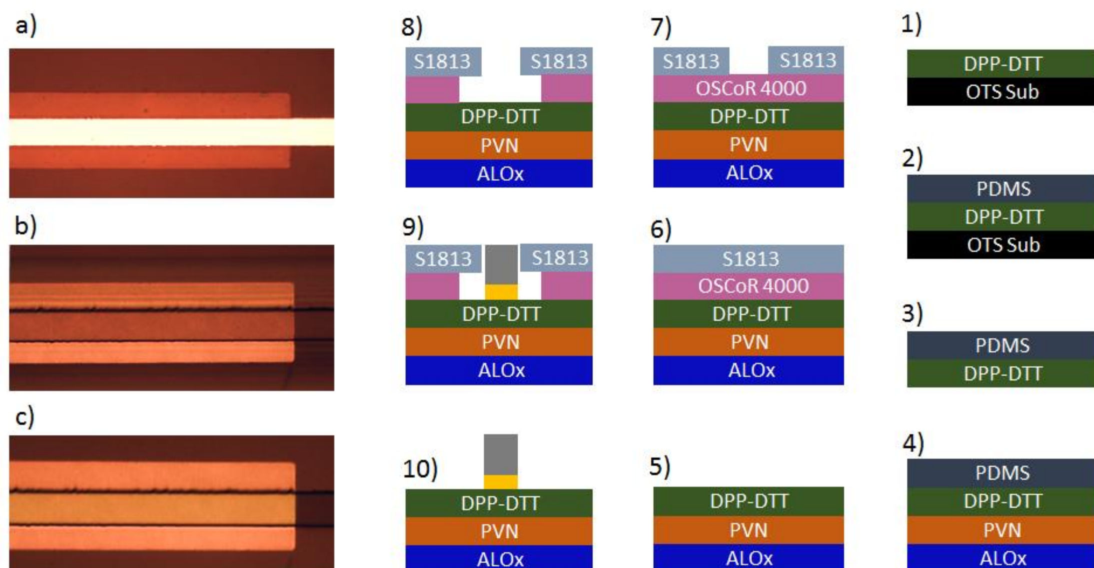

Figure. S5. Detailed illustration of photolithographic source patterning process. 1) Spin coating of DPP-DTT onto OTS-substrate, 2-3) Transfer of DPP-DTT film from OTS-substrate to PDMS stamp, 4-5) transfer of DPP-DTT onto PVN substrate by heating at 75 degree for 5 minutes, 6) spin coating OsCoR 4000 and S1813 onto DPP-DTT; before the second spin coating step the first layer was annealed and dried in vacuum; 7) UV exposure of S1813 through a lithography mask and development in MF319 developer; 8) transfer the pattern by developing OsCoR 4000 in HFE for 1~1.5 minutes; 9) deposition of Cu and LiF; 10) lift-off of the bilayer resist by immersing in HFE for 3 hours. (a), (b), (c) photography taken in microscopy corresponding to steps 10, 8, 7).

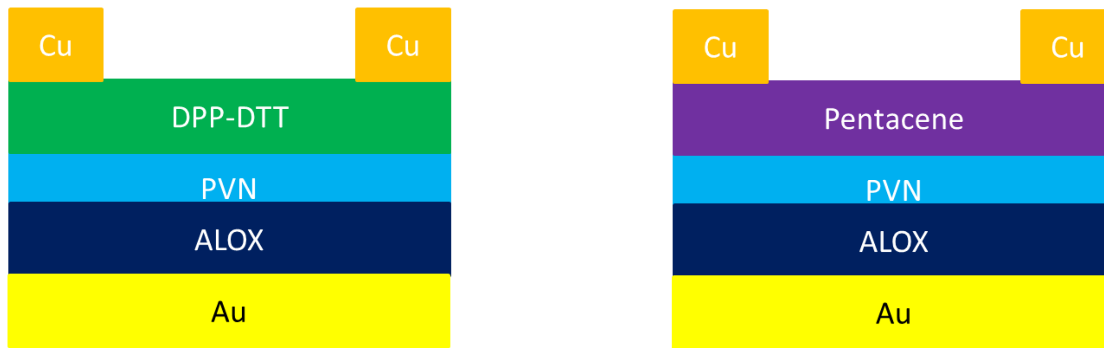

Figure. S6. The left and right correspond to the device structure of ALM and ULM.

FETs	Figure 2f (DPP-DTT)	Figure 3c (DPP-DTT)	Figure 3d (DPP-DTT)	Figure 3e (Pentacene)
Hole mobility μ_H	0.58 cm^2/Vs	0.33 cm^2/Vs	0.63 cm^2/Vs	0.87 cm^2/Vs
Electron mobility μ_E	0.31 cm^2/Vs	0.15 cm^2/Vs	0.41 cm^2/Vs	

Table. S1. Mobility of transistors.

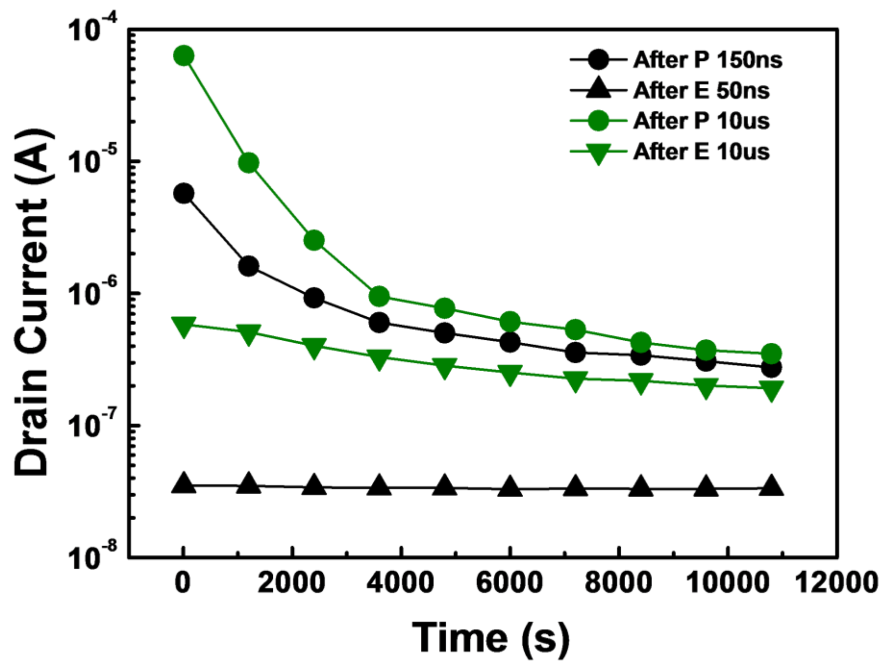

Figure. S7. The retention characteristic in the form of read-out current.