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Investigation of gate drive strategies for high voltage GaN HEMTs

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Abstract

Gallium Nitride (GaN) devices due to its excellent material properties has the potential to significantly impact the power electronics industry. With the 600 V devices getting commercialised, there is an increasing demand to accelerate the adoption of these devices in power applications which requires know-how on dealing with these novel devices in real circuits. This paper studies the basic driving requirements of GaN switches when operated in half-bridge configuration. The stringent gate drive margin, instability issues due to high dv/dt and di/dt, cross talk due to parasitics, voltage overshoot and oscillations are analysed in detail using different gate drive circuits. This work will discuss the impact of the different gate drive strategies on the GaN switching performance. These findings are experimentally validated by designing, demonstrating and comparing 1 kW, 500 KHz GaN half bridge prototypes using three different types of gate drives.

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Keywords: Gallium Nitride, Gate Drives, Half-bridges
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1. Introduction

Gallium Nitride (GaN) devices are continuously evolving in the market with 600 V devices getting commercialized and manufacturers releasing different variants of normally-off devices to exploit the superior properties of this novel material compared to silicon. The growing acceptability of these devices has seen a strong interest in the different varieties of GaN structures [1]. Cascodes are preferred in certain applications due to its conventional packaging and drive requirements, whereas most of the high-power density applications have been focused on normally-off single device GaN HEMTs.

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There is good literature on understanding the driving requirements for GaN HEMTs and designing novel gate drives for these devices [2-4]. But most of them are focused on certain aspects of GaN drive issues and do not always cater to the commercial feasibility of these drives. This paper investigates the driving requirements of GaN HEMTs when used in half-bridge circuits. Issues of instability when working at high-switching frequencies are discussed based on using off-the-shelf drivers. Section I brief the structure and packaging of commercial GaN devices in both cascodes and HEMTs. Section II reviews the gate drive challenges, section III analyses the instability issues using three different off-the shelf gate drives. Section IV proposes a customized gate drive with clean switching waveforms. Conclusions and scope for future work are discussed in section V.

I **Structure and Working of GaN HEMTs**

The basic GaN device is normally-on type, which are not preferred in power applications due to safety and acceptability considerations. So the industry has come up with various variants of normally-off devices as shown in figure 1-5 .

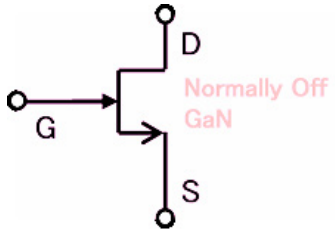

Figure 1: Normally-off single device GaN

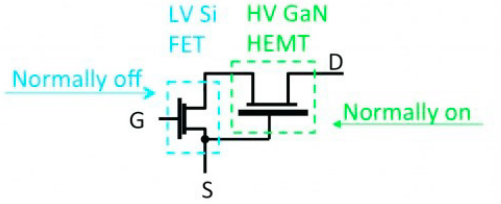

Figure 2: Normally off- GaN Cascode

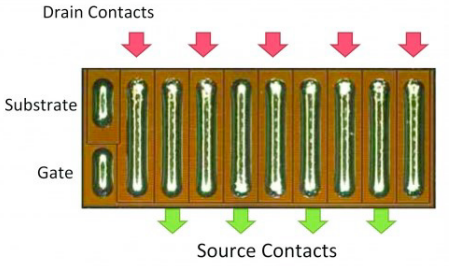

Figure 3: EPC LGA package

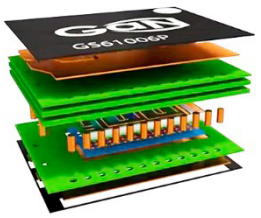

Figure 4: GaN Systems Kelvin package

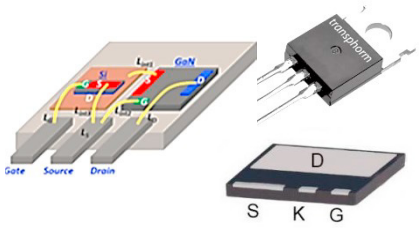

Figure 5: Transphorm TO & SMD

Figure 1 shows normally-off single device GaN HEMTs which is commercially available from EPC (20-200 V), GaNSystems (650 V) and Panasonic (650 V) all of which have different package structures . The cascode configuration, as shown in figure 2, is a normally-off low-voltage Si FET (typically 30 V) connected to a normally-on high-voltage GaN HEMT (600 V) in series while the gate of the GaN HEMT is connected to the source of the Si FET. A normally-off power electronics device is thus achieved by this two-device series configuration. Motivated by the reasonably high –threshold gate voltage, normally-off structure, very low reverse recovery charge, small output capacitance, conventional TO package and ease of use, GaN cascode devices have generated a lot of hype and enthusiasm in the market [5]. But cascodes compromise the GaN device's superior properties leading to internal switching losses which makes the cascode GaN suitable for certain topologies and applications [6-8]

The different structures and packages for GaN devices demand customised drive circuitry to maximise the benefits from different GaN devices. The gate drive design must tolerate different characteristics caused by variation in structures and packaging. For sensitive non-packaged devices like EPC LGA GaN, the soldering and the placement of peripheral components makes a huge difference to its behaviour in the circuit [9]. GaNSystems has a special

kelvin package which enables top and bottom sided cooling and the layout is critical to its working [10]. In case of Transphorm, the TO packaged cascode devices enables it to work with Si device drivers but the package parasitic acts as a barrier in its reliable working in a half-bridge [11]. The next session will consider the different driving requirements of GaN demonstrating the challenges during operation with the designed prototypes.

2.Gate Drive Requirements and Challenges for GaN circuits

For both e-mode and cascode GaN devices, control of the device is achieved by supplying or removing the gate charge from the gate electrode. Gate drive design for cascode device is identical to the Si devices. However, driving e-mode devices is complex and needs special considerations. Main issues of driving high speed e-mode GaN devices are:

1.Low gate threshold voltage
2.Very small margin of allowable gate voltage
3. dv/dt and di/dt constraints
4. Parasitic issues
5. Layout considerations

For e-mode devices, the maximum Gate to Source voltage V_{GS} is normally less than 6 Volts but the devices normally require 3 to 4 Volts to fully switch on, resulting in a small margin. In contrast, the Silicon MOSFETs has much higher maximum V_{GS} voltage about 20 Volts. The threshold voltage, V_{GSTH} of GaN is very low, 1 to 2 V, causing incident switch-on when the device is used in high dV/dt applications [12] The gate drive for GaN is therefore stringent due to the low V_{GS} margin and low V_{GSTH}. These gate voltage requirements can be achieved by critical damping of the gate -drive turn-on switching power loop. In addition, the turn-on and turn-off damping requirements are different which necessitates the use of independent gate resistors to adjust the turn-on and turn-off gate-loop damping.

The limited gate drive voltage range impacts the high-side supply for half-bridges. In this work, a bootstrap circuit is used in the first design to mitigate the issue of limited drive voltage range but the dead-time had to be decreased to 50ns, which caused frequent failures. So, the deadtime was increased to 100ns and a high-side supply regulated by a discrete IC voltage regulator which solved the bootstrapping issue had to be used.

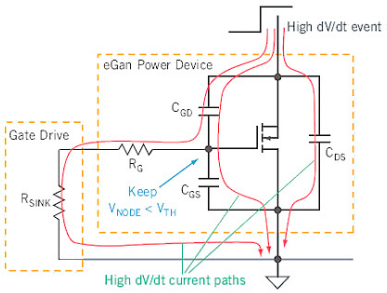

Figure 6 : Effect of dv/dt on switching[12]

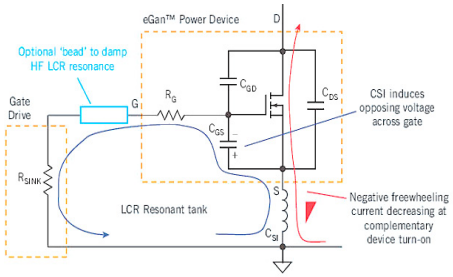

Figure 7 : Effect of di/dt leading to shorting of bridge leg [12]

Another major constraint in driving GaN high speed switches is the dv/dt and di/dt effects. In a MOS gated power switching device, the voltage slew rate (dV/dt) is determined by the charge / discharge rate of the miller capacitance. From figure 7, gate resistors can be increased to slow down dv/dt but it negates the purpose of using the high-speed switches. So an optimisation of gate resistance selection is required. Simulation results show that a gate-pull down resistor less than 0.5ohm is optimal as shown in figure 8.

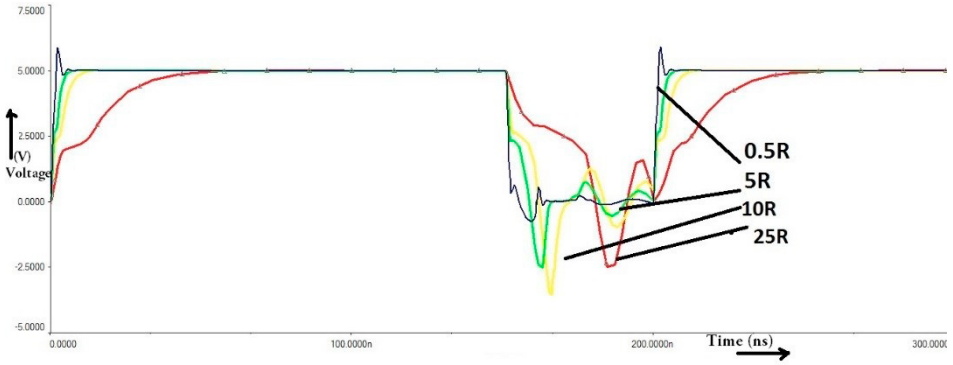

Figure 8: Variation of gate voltage with gate resistor

3. Gate Drive Design and Experimental Results

Based on these gate drive requirements, three different off the shelf gate drivers were used to analyse GaN switching 1) LM5114 2) UCC27611 3) ADuM3221 - all microcontroller driven and based on these findings a customised gate drive circuitry was designed and demonstrated to mitigate the effects of voltage overshoot and oscillations.

Specifications	Drivers		
	LM51114 (low side)	UCC27611 (high-side)	ADuM3221
Peak Output Current (A)	7.6	6	4
Prop Delay (ns)	12	14	60
Output Impedance(Ω)	0.23	0.35	-
Package	SOT	SON	SOIC

Table 1 : Gate drive specifications

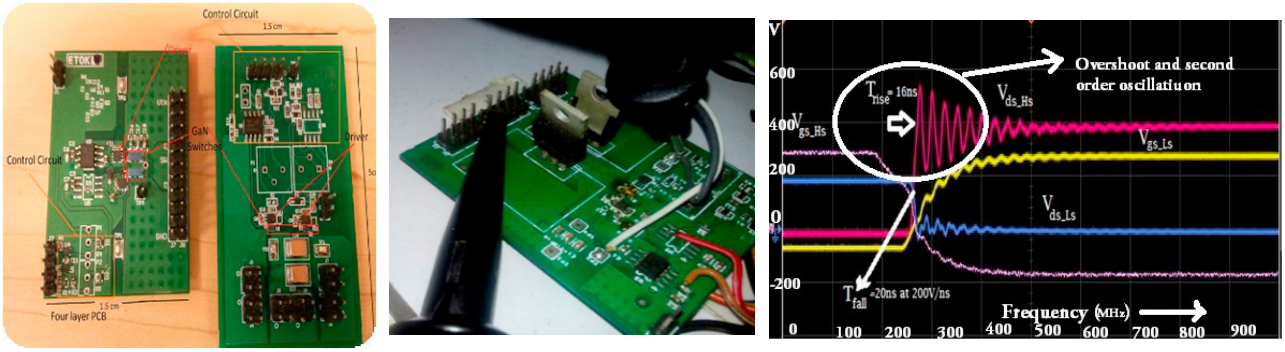

Figure 10: Prototype of GaN Half-bridge circuits and switching waveforms of high & Low side switches with LM5114 & UCC27611 driver with oscillations

The following GaN devices were used to build prototypes: Transphorm : TPH3206PD(600 V, 17 A) , TPH3202PS (600 V, 17 A) and EPC : EPC2027 (450 V, 5 A). LM5114 was used as low-side drive and UCC27611 as high side drive due to the driving specifications of the driver as tabulated in table 1.

With drivers LM5114 and UCC27611 typical voltage and current traces after the switching point show significant ringing oscillation with a long decay time. This oscillation causes additional switching losses and EMI. At switch-off, excessive voltage over-shoot can cause device failure. The voltage overshoot is mainly due to the parasitic inductances of the device package and circuit layout which have been explored in details in [14-16].

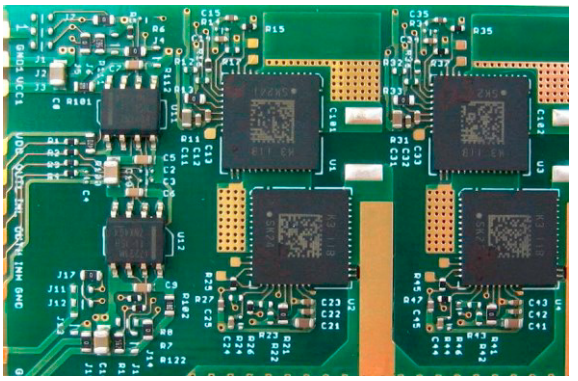

Figure 11: Prototype using ADuM3221

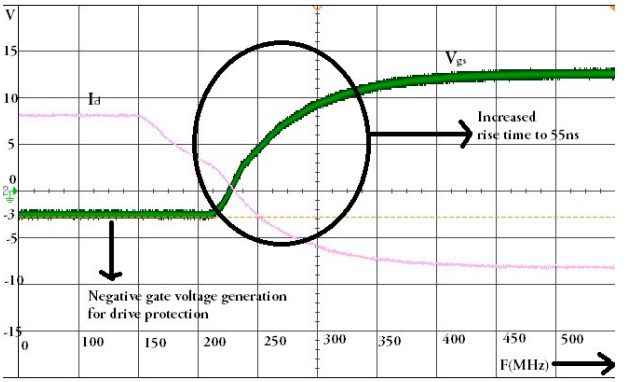

Figure 12: Gate drive voltage and current with ADuM3221

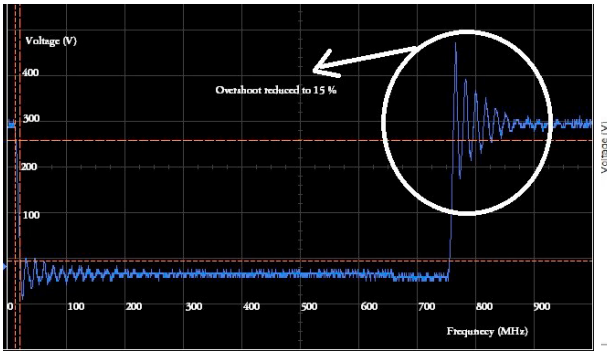

Figure 13 : Switching voltage with AduM3221 driver

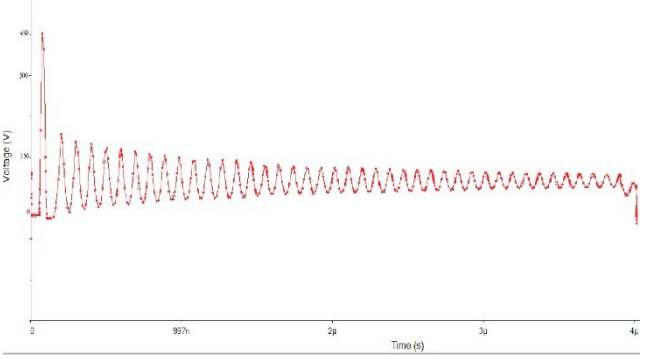

Figure 14 : Second order response (transient analysis)

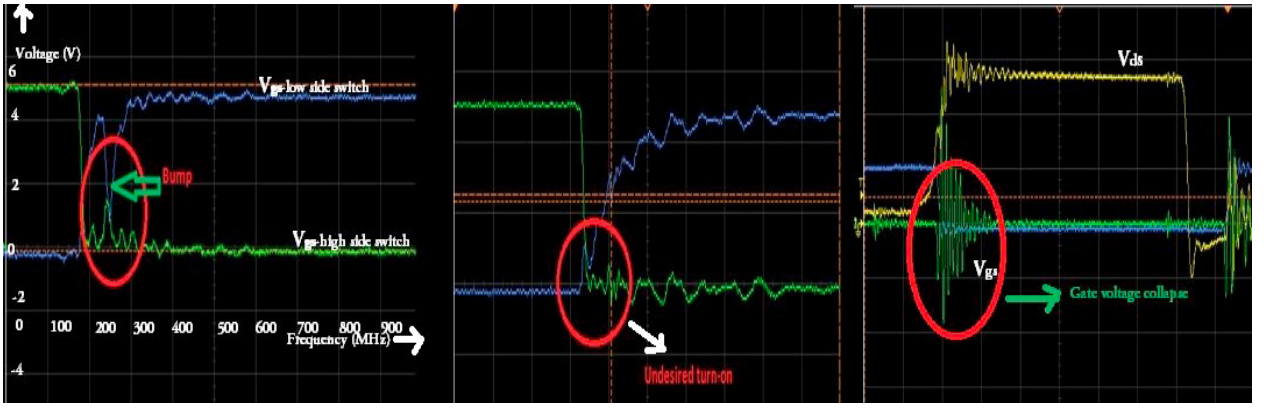

Figure 15: Shorting of legs due to cross talk and gate turn-on leading to shorting of leg and gate drive collapse(LM5114 driver)

The results of the study suggest that the gate driver based on the GaN specific ICs-LM5114 & UCC27611, gave rise

and fall times around 5ns and hence worked per device specifications. The overshoot and ringing was within 5-10 % of the Vds as the input voltage was increased from a few volts to 400 V but was sensitive to voltage disturbances and noise. As noticed in analysis the turn-on spikes and oscillations are higher than during turn-off (figure 10). Thus, these devices gave excellent switching performance till a few MHz but requires stringent RF based PCB design considerations and gate voltage stabilisation for reliable working which is explored by the author as future work.

The second gate driver was built using commercial Si driver- ADuM3221 with a negative drive voltage circuitry to avoid spurious turn-on as in figure 12. This system was more robust with increased rise and fall times around 50ns; the switching performance was compromised due to slow drive characteristics and more ringing due to the CSI of the Transphorm TO package which required damping components (figure 13-15). This drive worked reliably in the frequency range of 10 KHz to 500 KHz but the system complexity and cost is increased due to the negative drive voltage generation circuity.

Based on these findings, the preferred driver characteristics can be summarised as follows:

*Low inductance package
*Peak output current of min 4A
*Low output impedance <2ohm
*Small gate drive loop
*Stringent PCB layout

With these findings in hand, a customised open-loop gate drive using high-bandwidth op-amps was designed with the following specifications:

- 650MHz bandwidth.
- 1p sec propagation delay (for real-time control).
- +/- 400mA drive.
- Gate voltage: +8V to -3V (specifically for driving eHEMT GaN).

The PCBs have been designed in Orcad and a four-layer configuration is used (figure 16). The PCB is made as small as possible (2.5 x 1.5cm and 4.5 x 3 cm) with a tight layout with the driver circuit placed very near to the gate to avoid loop inductances. Decoupling capacitors are placed as close as possible to the devices for reducing unwanted losses.

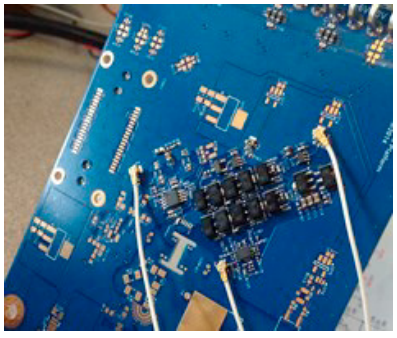

Figure 16: Prototype using 4-layer PCB

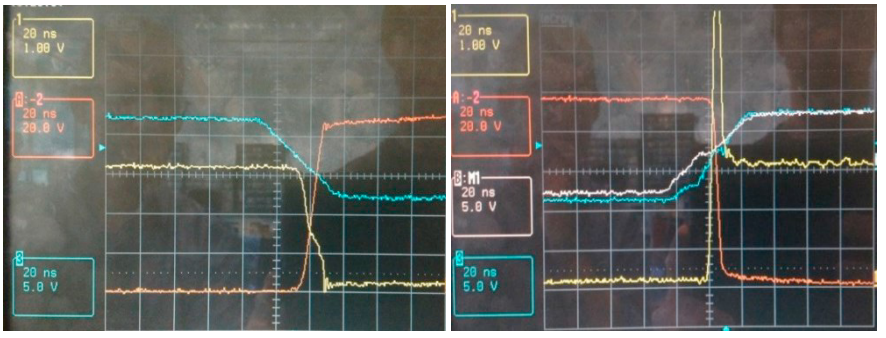

Figure 17: Turn off (left) & turn-on waveforms(right)(Red =V_{ds}, Yellow = I_s, Blue=V_{gs})

For measurements, 700MHz high voltage measurement using RC potential divider chain scalable to 3kV and beyond is used with buffered 50- Ω) output. 1GHz current measurement using 10 mΩ resistive shunt (approx. 100 mV at 10A), with inductance compensation with buffered 50- Ω) output to scope is utilized. The use of four-layer PCB with tight layout and reduced power switching loop using intermediate return path and use of customised

voltage and current measurement circuitry gives clean switching waveforms as shown in figure 17.

For turn off, there is no voltage over-shoot, dI/dt 'hesitation' due to switch device capacitance is due to charging by load current. This system is very robust with clean switching waveforms though at turn-on, there is a current spike during dV/dt due to output capacitance of GaN switch devices (normally masked by ringing). Efforts to mitigate this is an on-going work of the author.

4. Discussions and Future Work

Open-loop resistive gate drives as reported above has shown less competence in driving GaN devices at high frequencies. The common problems associated with conventional resistive gate drives used in the study are:

1. The dV/dt is dependent upon the load current because the voltage across the gate resistor varies during the miller plateau region. The degree of dependency depends on the device type.
2. The dV/dt changes with junction and gate drive temperatures.
3. The relationships between these variable factors, gate resistor values and device switch timing have not been thoroughly understood.
4. In practice, all gate drives are generally 'current drive' because the gate of the device is capacitive thus a standard resistive drive without current regulation cannot fully control the switching behaviour.

To design reliable and rugged gate drives, current drives are a better option for GaN circuits and will be explored by author as future work with emphasis on customised current measurement circuitry for accurate feedback control.

5. Conclusions

The main objective of this research work was to investigate different gate driver issues for GaN HEMTs to enable better design of circuits using these devices. Towards achieving this goal, a thorough study of available off-the shelf gate drives were built and experimental demonstration has been performed to discuss issues of using conventional off-the-shelf gate drivers.

The available gate drivers for GaN HEMT are targeted at e-mode devices. GaN specific driver used in this work has proved useful at high-performance related applications. The possibility of a gate feedback control to stabilise the gate voltage oscillations which can lead to more reliable working will be pursued by author as future work. The IGBT based drive can be used for GaN cascodes, but for optimum performance, transient voltage supressing diodes and decoupling capacitors are required for damping oscillations and limiting overshoots which increases complexity and cost. Overall, the PCB layout based on RF techniques for low -level parasitic reduction with power switching loop minimisation and high bandwidth customised drive circuitry will enable reliable working of GaN devices in half-bridge circuits.

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