

On the Reproducibility of CMOS Plasmonic Mid-IR Thermal Emitters

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Abstract—In this paper we report about the reproducibility of CMOS plasmonic mid-IR thermal emitters. The electro-thermal transduction efficiency of the devices is shown not to depend on the plasmonic structure geometry and to be extremely reproducible from device to device, wafer to wafer and lot to lot. The small variation in terms of optical performance is investigated through numerical simulation and attributed to variations in planar and cross sectional dimensions of the fabricated structures.

Keywords—Thermal emitter, plasmonic, CMOS, mid-IR.

1. Introduction

Surface plasmons (SP) [1] are coherent oscillations of free electrons excited by an electromagnetic field at the interface between two materials with permittivities (real part) of opposite sign (e.g. metal/dielectric interface). This charge motion is responsible for the generation of an electromagnetic wave (namely surface plasmon polariton, SPP) which propagates along the interface until its energy is lost, either due to absorption or scattering into other directions. When the frequency of the light impinging on the interface matches the natural oscillation frequency of the delocalized electrons, surface plasmon resonance (SPR) occurs. This phenomenon is elegantly predicted by the Maxwell theory, by “simply” considering each medium described by a complex frequency-dependent dielectric function and applying proper boundary conditions. Surface plasmons can highly enhance light/matter interactions, with two main consequences: (i) sub-diffraction limit light confinement and (ii) local electromagnetic field intensity enhancement. The latter phenomenon is the one exploited in IR emitters/detectors to artificially engineer their emissivity/absorptivity properties [2].

Our group is very active in the field of CMOS IR devices [3-10] and has been investigating, for a few years now, techniques to improve their performance. For example in [9], we designed a plasmonic crystal and, exploiting a slow-wave lattice resonance and spontaneous thermal plasmon emission, engineered a CMOS tungsten-based thermal emitter. This device, in comparison to its non-plasmonic counterpart, was shown to improve the sensitivity towards CO₂ of a prototype NDIR-based capnometer by almost 4 times.

Hereafter follows a brief description of the IR thermal emitters and an experimental study on their reproducibility supported by numerical simulations.

2. Experimental

The IR thermal sources were designed using the CADENCE Virtuoso layout editor and fabricated in 6” wafer SOI CMOS technology, in a commercial foundry. **Fig. 1** shows an optical micrograph of the developed IR thermal sources. A schematic cross section of the technology is depicted in **Fig. 2**. High temperature tungsten metallization was used as the resistive material for the micro-heater, the plasmonic pattern and the interconnects. Tungsten was chosen due to its very high melting point (> 3400 °C) and lower susceptibility to electromigration when compared to aluminium or polysilicon. The micro-heater has a circular multi-ring structure with a diameter of 600 μm, embedded within a ~5 μm thick, 800 μm diameter dielectric membrane released by a post-CMOS DRIE process. During this fabrication step, the buried oxide layer acts as an effective etch-stop. The DRIE process allows for the realization of nearly vertical side-walls, thus permitting aggressive miniaturization. The membrane thermally isolates the micro-heater

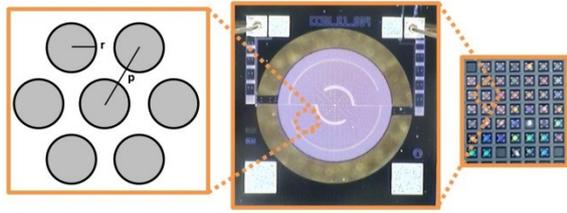


Fig. 1. (left hand-side) Schematic depiction of hexagonal plasmonic structure comprising tungsten cylinders having radius r and cylinder-to-cylinder distance (pitch) p . (centre) Optical micrograph of SOI CMOS MEMS plasmonic IR source (chip size: $1\text{ mm} \times 1\text{ mm}$), (right hand-side) Optical photograph of plasmonic IR sources with different plasmonic patterns. Note the different reflections resulting from different plasmonic pattern geometries.

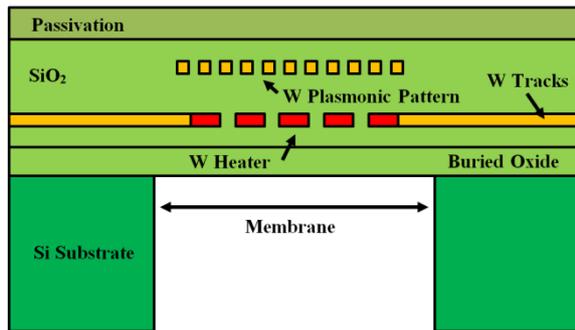


Fig. 2. Plasmonic IR thermal emitter cross sectional view (not to scale).

from the substrate, allowing temperatures in excess of $600\text{ }^\circ\text{C}$ to be reached in the heater area. Si_3N_4 is used as passivation layer. The wafers were laser diced into $1\text{ mm} \times 1\text{ mm}$ dies in a commercial dicing house, and subsequently wedge-bonded onto TO5 packages.

A number of thermal emitters were designed, fabricated and diced, differing from each other only in terms of plasmonic layer design (r and p). The emitters were then first characterised in a basic NDIR system in air. A pair of LabView controlled Keithley 2401 were used (*i*) to drive the micro-heater, injecting different current values, (*ii*) to measure the voltage across the micro-heater for each current value, and (*iii*) to measure the output of a commercial thermopile with CO_2 filter (HMSJ21F4.26/90) after a delay time of 1 s . This testing set-up allowed emitters characterisation in terms of DC power consumption and thermopile voltage response simultaneously. Among all the designed devices, the one coded as n.er 04, having $r=0.8\text{ }\mu\text{m}$ and $p=2.6\text{ }\mu\text{m}$ (more details can be found in [9]), was found to be the one with higher optical output, thus some of the results presented in this paper focus on this design.

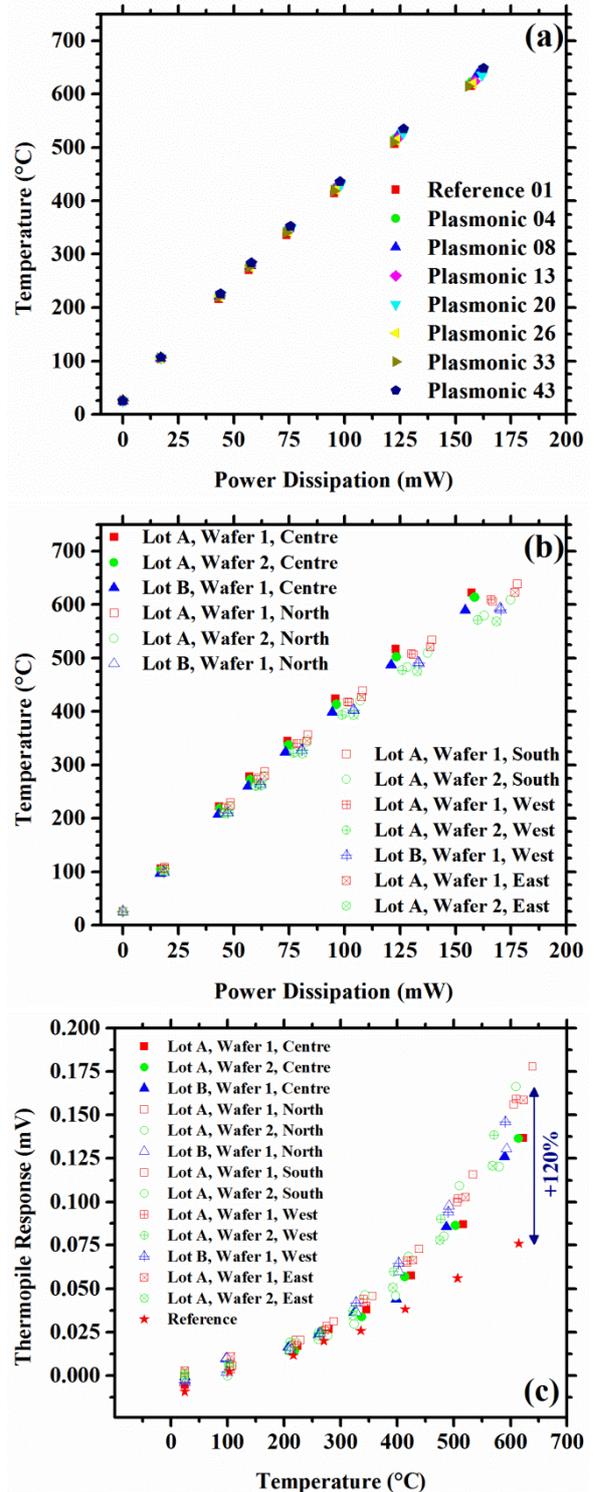


Fig. 3. (a) Emitter temperature as a function of DC power consumption, for different devices. (b) Emitter temperature as a function of DC power consumption, for plasmonic design 04, with devices coming from different position within the same wafer, from different wafers and from different lots. (c) Thermopile response as a function of emitter temperature for plasmonic design 04, with devices coming from different position within the same wafer, from different wafers and from different lots.

In **Fig. 3a** and **Fig. 3b** the electro-thermal behaviour of some of the plasmonic emitters is plotted and compared to a reference, non-plasmonic device. It was found that the presence of the plasmonic pattern does not affect the device electro-thermal conversion efficiency, which is also highly reproducible from device to device within the same wafer, from wafer to wafer and from lot to lot. In **Fig. 3c** the thermopile response is plotted as a function of the emitter temperature for devices coming from different areas of the same wafer, from different wafers and different lots. The plasmonic emitter (design n.er 04) is consistently more efficient (up to 120 %) than a typical non-plasmonic counterpart, proving the employed fully-CMOS MEMS technology to be extremely highly reproducible and thus suitable for high volume cost efficient mass production. This is undoubtedly the prime advantage of using plasmonic phenomena for engineering the spectrum of the spontaneous thermal emissions of IR sources in contrast to the methods [3, 5].

3. Discussion

To gain insight into the physical phenomena and in particular to understand which technological parameters govern the emission at different wavelengths, 3D finite element modelling (FEM) of the plasmonic IR emitters was carried out. The devices spectral behaviour was investigated with the RF Module of COMSOL Multiphysics. In **Fig. 4** typical spatial electric field intensity distributions are presented at the plasmonic resonance frequency, corresponding to the wavelength where the emissivity peaks reach their highest values. At this wavelength, a localized enhancement of the electric field in the proximity of the metal dots forming the plasmonic structure is present, resulting in an increase of the resistive losses within the metal and, thus, an increase in emissivity. The amplitude of the simulated peaks is very close to the experimental one (more details in [9]), but the wavelength of the peaks is slightly red-shifted. Such discrepancies might stem from (i) the use of material properties taken from literature – which might not be entirely appropriate since these are strongly dependent on the fabrication process – (ii) the assumption of planarization in the simulated structure, and (iii) the employment of a typical thickness value for the layers forming the membrane. The latter is indeed critical for the optical behaviour of the structures. In **Fig. 5**, a numerical evaluation of the

effect of layers' thickness variation (within the tolerances of our process) is reported. Among all of them, the thickness of the SiO₂ layer between the heater and the plasmonic pattern is shown to affect the most the plasmonic resonance frequency. Variations (within the process tolerances) in the planar and cross sectional dimensions of the structures are thus shown to be a possible cause for the small optical performance variation shown in **Fig 3c**.

4. Conclusion

A number of devices comprising plasmonic patterns with different geometries were designed, fabricated, experimentally characterised and numerically investigated. The addition of the plasmonic layer was found not to degrade the electro-thermal conversion efficiency of the devices. Dependency of the resonant frequency on the geometry of the plasmonic pattern was experimentally investigated. A high degree of reproducibility was observed for devices coming from the different areas of the same wafer, from different wafers and from different lots. Three dimensional FEM modelling was also employed to theoretically investigate the IR plasmonic source spectral behaviour. The model was found to qualitatively capture the position, the amplitude and the geometry dependency of the plasmonic resonant frequency. Additionally the discrepancies between experimental and simulated results were mainly attributed to the slight variation in the layer thicknesses (especially that of the SiO₂), the non-planarised process and the slight difference in the optical properties of the materials, which are process dependent. Additionally the small differences in optical performance between same devices were attributed to concurrent variations of the geometric process parameters.

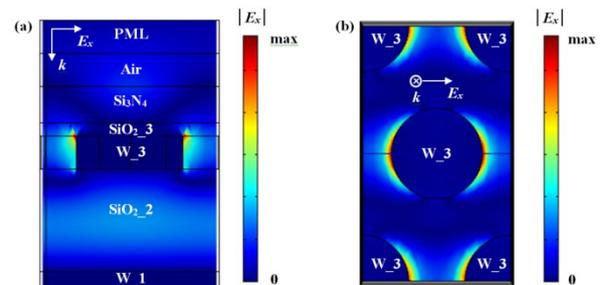


Fig. 4. (a) Cross sectional view and (b) top view of a typical electric field intensity ($|E_x|$) distribution at plasmon resonance frequency. Pitch and radius for the simulated structure are equal to 2.6 μm and 0.8 μm , respectively.

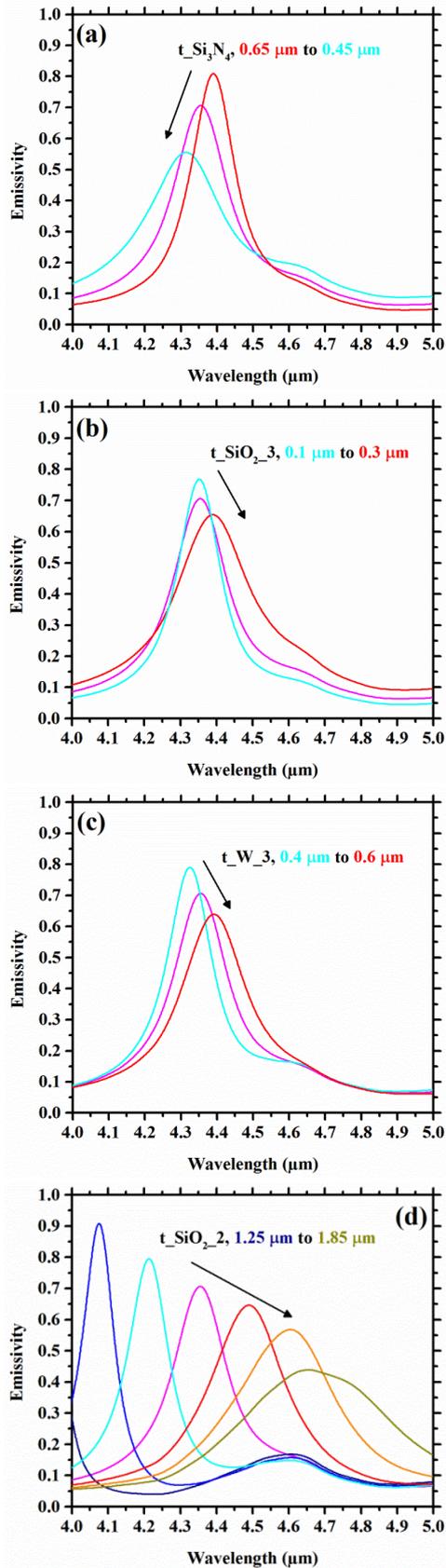


Fig. 5. Simulated effect of process tolerances on layers' thickness, respectively for (a) Si_3N_4 , (b) SiO_2_3 , (c) W_3 and (d) SiO_2_2 .

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