Low Inductance Switching for Wide Band Gap Device Based Power Circuit

1. Introduction

Wide Band Gap (WBG) materials such as Gallium Nitride (GaN) and Silicon Carbide (SiC) offer superior electrical and thermal properties, e.g. higher critical electric field and thermal conductivity, over conventional Silicon (Si) devices. For the same voltage and current rating, a WBG power semiconductor device offers smaller die area, providing higher operating temperature, higher operating frequency with lower switching losses and part-load conduction losses compared to an equivalent Si power device [1]. As an example, SiC MOSFET power devices only require a thin but highly doped drift layer to withstand a high blocking voltage. By this mechanism a unipolar WBG device can be competitive against a bipolar Si device in terms of electrical performance, whilst offering greater benefits at high switching frequencies when compared to conventional Si IGBTs. The increased operating frequency reduces the requirements for filter capacitors and inductors, and the reduced switching losses improve overall efficiency.

SiC MOSFETs and GaN HEMTs are two of the most popular WBG power semiconductor devices available today. Operating such FET-type WBG devices at high switching frequency imposes significant challenges: (1) The high $dv/dt$ and high $di/dt$ generated by the FET-type devices cause significant ringing issues with parasitic inductance and capacitance in the switching loop, (2) accurate measurements of the switching behaviours with low phase lag are required by feedback control and status monitoring, without degrading the performance of the power circuit being measured, (3) stringent power circuit layout and gate-drive design are required to reduce the effects of parasitic inductances in order to approach ideal switching waveforms.

This paper presents a prototype low inductance PCB design for SiC MOSFET based switching circuit. In addition, a high bandwidth linear gate drive circuit for SiC MOSFETs and a high bandwidth on-board measurement system are developed together with the low inductance PCB to demonstrate the reliable use of WBG devices in high frequency switching circuits. The design procedure and the PCB layout requirements for low switch-commutation and gate-drive loop inductances are discussed. The design methodology and test procedure are presented along with experimental test results for the gate drive and measurement systems. The stringent PCB layout, specialised gate-drive design and built-in measurement systems all contribute to improving the usability of SiC power MOSFETs. The potential benefits of this gate drive-circuit for WBG power device based applications are discussed.

2. Parasitics and PCB Design

Parasitics in device packaging and application circuit remain significant barriers to the wider adoption of WBG devices in power converter applications. At high switching frequencies, a successful converter design using these WBG power devices needs to involve considerations from both power electronics and RF design, with techniques from both fields being used to first understand and then eliminate the effect of parasitics. The main parasitic elements are:

1) Common source inductance (CSI), the inductance shared between the gate-drive and power circuit, both inside the device package and the external connectivity on the PCB. This can be extremely detrimental, since adding as little as 1 nH of CSI, can increase losses 50% over an ideal case [2]. It is dependent on both the circuit layout and package inductance.

2) Gate loop inductance (GLI), the area enclosed by the gate-drive current path to the switching die and the return path from the source connection back to the gate-drive 0 V. It can be reduced by tight PCB layout, with careful consideration given to cancellation of the magnetic field generated by this loop. A GLI above 5 nH can decrease the switching efficiency significantly and cause localised overshoot of the gate voltage at the switching die [2], [3]. If the GLI is too high then critical damping may not be achieved, resulting in switching instability and device failure [4].

Switched current commutation loop inductance (SCCLI), caused by the magnetic field generated by switching the load current from the top device to bottom device (or vice-versa) in a half-bridge switching topology. A SCCLI of 2 nH has been achieved in this work through careful PCB layout, the results of which are shown in Fig. 2. It has been found in literature of previous work that loop inductances beyond 5 nH can be extremely detrimental to the circuit operation, causing voltage overshoot spikes and subsequent oscillations at the mid-point voltage during fast switching transitions.

![Fig.1 SiC Development Platform (left), and Test-Rig set up with Network analyser (right)](Image)

The gate- and power-loop inductances have been measured using an Agilent E5061B Network Analyzer. The test-set up is shown in Fig. 1.

The loop inductance has been optimised using magnetic field cancellation in a multi-layer PCB structure with currents flowing along the top-side of the board and returning through a mid-layer, as shown in Fig. 2.
3. On-board Measurement System

There are limited choices of commercially available test equipment that are capable of accurately measuring the switching currents without significantly degrading the performance of the circuit under test. Also, measuring the gate voltage of a high-side switching device can present significant problems, since such a small differential signal is difficult to extract from a large common-mode voltage that intermittently slews very quickly. On-board measurement circuits have been developed here as solutions to these problems and are explored in this paper, as follows:

1) Very low inductance resistive-shunt circuit for high bandwidth current measurement and minimal insertion losses or switching performance degradation.
2) $V_{DS}$ measurement circuitry using a resistor-capacitor array to achieve high bandwidth and high precision with minimum propagation delay.

All measurement signals are buffered and compatible with $50\Omega$ terminated scope inputs.

3.1 Current Measurement Circuit

Measuring the current in the commutation loop without introducing undesirable loop inductance is a challenging problem. There are many methods explored in literature to deal with these issues [5]. Most of these rely on measuring magnetic flux as a proxy for current, which introduces inductance as a by-product [6]. For WBG devices, where the current slew rate can be in the order of $100\ \text{A/\mu s}$, the inductance created by any practical magnetic flux measurement system will have a detrimental effect on the efficient and reliable operation of the switching circuit.

One solution to overcome these limitations is a resistive shunt. The problems encountered by a practical implementation of such a circuit are the inductance of the resistors and power dissipation. The solution used in this paper to mitigate these issues is as follows:

1) The resistance is made as small as practicably possible, whilst still giving a reliable signal. A good target value in this study has been found to be $100\ \text{mV}$ at full current.

2) The inductance of the resistive shunt has been reduced by paralleling small SMD resistors, with the return current path run directly underneath with a very thin dielectric insulator material (approx $100\ \mu\text{m}$ thick) between. This gives an insertion inductance in the region of $300\ \text{pH}$.

3) The increase in measurement gain at high frequencies (>1 MHz) due to the small amount of remaining inductance is compensated for with a filter incorporated into the amplifier circuit.

The initial tests show a relatively flat gain up to $200\text{MHz}$, though there is still some more work to do in flattening some unwanted out-of-band parasitic effects.

3.2 $V_{DS}$ Measurement Circuit

The $V_{DS}$ voltage measurement in a typical half-bridge switched inductive load test setup can present significant challenges such as:

1) High bandwidth is necessary to capture the fast slew rates and overshoot ringing of WBG switching devices.
2) The V_{DS} measurement circuit as a part of a feedback control loop will need to exhibit extraordinarily low propagation delay to be stable under all operating conditions whilst still having sufficient gain to be useful.

The measurement circuitry presented in this paper is capable of achieving both of the above requirements. It is based on a potential divider buffered by a high impedance input op-amp. Due to practical limitations, the capacitive effects of the op-amp, passive components and PCB become significant at high frequency requiring low impedance. However, the impedance needs to be high at low frequency in order to minimize the power dissipation. The solution presented here is a high resistance potential divider with a capacitor-resistor network connected in parallel. As the capacitors decrease in impedance with increasing frequency, there remains some series resistance to limit the minimum impedance and dampen any effects due to the inductance of the capacitors. The test results from this circuit show a flat response up to 500MHz.

3.3 Gate Drive Circuit

The most common problems associated with conventional resistive gate drives are:

1. The gate voltage during the miller plateau region will vary with load current, so the voltage across the gate resistor, and therefore the gate current, will be dependent on load current. Thus \( \frac{dv}{dt} \) will also vary with load current, and this effect can be noticeable depending on the device type and design.
2. This miller voltage also varies with power device junction temperature and gate drive temperature.
3. There is a complex relationship between these variable factors, gate resistor and device switch timing.

The solution to these issues is to drive the gate with a controllable current source. Thus, the gate current during the miller plateau becomes independent of gate voltage and therefore load current. A further improvement on this is to make the current drive controllable. This offers the possibility to vary the gate drive current according to a pre-set signal profile during the switching event or a feedback control signal. Such a feedback mechanism could be used to limit over voltage transients or over-current during short-circuit current conditions.

The gate drive circuit presented here can achieve a constant gate current. The test results show that this circuit offers a significant level of performance, and is capable of driving a current into a capacitive gate load with a bandwidth in excess of 150 MHz. These tests were carried out at varying values of gate voltage to show that the drive current remains unaffected by gate voltage.
3.4 Hard Switching Tests under Inductive Load Condition

The high performance switching and measurement circuits described in this paper have been built according to the layout techniques described herein. The test results achieved from switching this circuit at high-voltage and high-current are presented in this section.

The test set-up is as follows:

1) Switched inductive load of 100 µH, with a 50 Ω series resistor to dissipate the stored energy after each switch cycle. The test cycle is a double-pulse at low duty to remove the need for thermal management of the power components.

2) 500 V DC bus provided by a DC power supply, with sufficient de-coupling capacitance to ensure that the power supply is buffered from the high peak demand of 25 A and instead is only required to supply a low average current.

3) Outputs from the various on-board measurement circuits, along with external measurement probes included for comparison, are connected to a 500 MHz LeCroy oscilloscope. The drive reference signal is provided by an arbitrary waveform generator.

The turn-off waveforms are presented in Fig. 10. Ch. 1 shows the \( V_{DS} \) measurement by a high voltage probe, and Ch. 2 shows that by the on-board system. The \( I_D \) shown is measured by the calibrated on-board system.

After the initial rise, the main \( V_{DS} \) rising remains smooth, and the \( V_{DS} \) over-shoot after the DC level is very small with an absence of noticeable ringing as a result of the low parasitic inductances. The rapid increase in \( V_{DS} \) caused a drop in the device current \( I_D \) due to the resulting voltage change across the freewheeling diode. After the \( V_{DS} \) reached DC level, the \( I_D \) regained a little amplitude, which is also due to the rapid rising of the \( V_{DS} \). This suggests that the on-board measurement may have superior bandwidth than the external current probe, considering the effect of series parasitic inductance. Ringing in \( I_D \) is detected, but the amplitude is small.

Similarly, the turn-on waveforms are shown in Fig. 11. The initial current rising is smooth, followed by ringing in small amplitude after it reached the load level. The \( V_{DS} \) fall remained smooth in the entire turn-on process, with no obvious ringing in \( V_{DS} \).

The on-board \( V_{DS} \) measurement showed good agreement with the external high voltage probe. Further waveforms and a detailed analysis of these results will be included in the full paper submission.

At zero load current, Fig. 13 shows there is a bump in current associated with charging the drain-source capacitance of the other device in the bridge leg. This effect is seen superimposed on the switching waveforms.
4. Discussion

WBG power devices offer more benefits over Si power devices at higher switching frequencies. At high switching frequencies, the rapid transient processes require the PCB design to have minimal inductance for the switching loop, gate drive and common source. This work presents techniques for reducing the critical parasitic inductances in the circuit through careful component selection and optimised PCB layout. This is achieved by cancelling magnetic fields resulting from looped current paths in the gate-drive and switched-current-commutation circuits, though the underlying mechanism is to minimise the contained area of these current loops.

Reduced ringing in current and voltage mitigates the EMI and the stress on the insulation. The work reported here represents a practical implementation to such requirements for SiC MOSFETs. The same methodology can also be applied for GaN devices. This high performance switching circuit is coupled with non-intrusive measurement techniques that do not adversely affect the performance of the switching circuit, and thus near-ideal switching waveforms can be demonstrated in the switching tests in 3.4. The on-board measurement system showed good agreement with the external measurements and may have even superior bandwidth. The on-board current measurement may be subject to internal ringing, and the parasitic capacitance may be from multiple sources, which added to the detected ringing in the test waveforms. Further studies into these issues will be included in the full paper.

This paper also presents a high-performance linear current source gate drive circuit that offers a high level of controllability over the SiC MOSFETs tested. The tests shown in this paper have been initially carried out with a fixed drive amplitude, but it is anticipated that future work will demonstrate the benefits that can be achieved with a profiled gate drive signal with active feedback control. The latter control scheme can potentially reduce the effects of EMI or improve parallel current sharing. The use of digital systems to control the drive circuitry is capable to enable increased accuracy, flexibility and scalability.

The integration of the reported on-board measurement system with the stringent PCB layout and the customised gate-drive design forms the foundation for a SiC device development platform for realistic application environments. Similarly, this principle can be adapted to GaN devices. This platform enables the testing of feedback control scheme, protection systems and status monitoring, all of which will be crucial to maximise the advantages, usability and reliability of WBG devices in realistic conditions.

5. Conclusions

The benefits of using WBG power semiconductor devices can only be realised when the power circuit, gate-drive and PCB layout are all properly optimised for fast switching. In this paper, the performance of such an optimised circuit is successfully demonstrated. A set of circuits and PCB layout considerations are provided and have been implemented and tested. The circuits have been designed after extensive studies focusing on minimising the impact of parasitics, with Spice simulations to model their effects.

Further to this, the circuit design for a linear current source gate drive is presented and the benefits are discussed. It is also anticipated that more sophisticated profiled drive strategies, closed-loop control and digital control systems, enabled by the fundamental work presented here, will yield further benefits in the future, for improved performance, EMI and circuit protection.

In addition, a high performance embedded non-intrusive measurement system is presented. This system showed good agreement with the external probe measurements, with even superior bandwidth.

The combination of the on-board measurement system, current source gate drive and the low inductance PCB layout presented in this paper demonstrates a practical implementation for high frequency power circuit basics, which can serve as the foundation for a WBG device development platform with considerable potential for high frequency power applications.

References