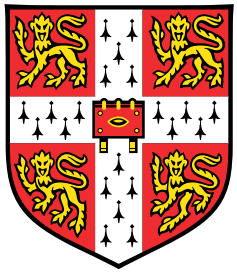
High Efficiency IGBTs through Novel Three-Dimensional Modelling and New Architectures



Emma Mae Findlay

Jesus College

University of Cambridge

This thesis is submitted for the degree of
Doctor of Philosophy

January 2020

Declaration

This thesis is the result of my own work and includes nothing which is the outcome of work done in collaboration except as declared in the Preface and specified in the text.

It is not substantially the same as any that I have submitted, or, is being concurrently submitted for a degree, diploma or other qualification at the University of Cambridge or any other University or similar institution except as declared in the Preface and specified in the text. I further state that no substantial part of my dissertation has already been submitted, or, is being concurrently submitted for any such degree, diploma or other qualification at the University of Cambridge or any other University of similar institution except as declared in the Preface and specified in the text.

It does not exceed the prescribed word limit for the Engineering Degree Committee. This thesis contains approximately 48,000 words (excluding references) and has 125 figures.

Emma Mae Findlay

January 2020

High Efficiency IGBTs through Novel Three-Dimensional Modelling and New Architectures

Emma Mae Findlay

Abstract

New Insulated Gate Bipolar Transistor (IGBT) designs are reliant on simulation tools, such as Sentaurus technology computer-aided design (TCAD) models, which allow for rapid device development that could not be achieved by manufacturing prototypes due to the cost and time associated with fabrication. These simulations are, though, computationally expensive and typically most design engineers develop these TCAD models only in two dimensions. This leads to inaccuracies in the model output since manufactured transistors are inherently three-dimensional (3D).

Based upon a commercial IGBT, this thesis begins by outlining the development of a 3D TCAD model using design details provided by the manufacturer. Large variations between the experimental data from the manufactured device and the simulation model lead to the discovery of widespread birds-beaking within the IGBT – an uncontrollable processing defect that the manufacturer was unaware of. This thesis presents a new simulation technique to account for this processing error while minimising computational effort and investigates the consequence of this birds-beak on the reliability of the device. The verified 3D IGBT model was also used to determine an optimum cell design that considered critical 3D effects omitted from previous studies.

An extensive literature review for the Reverse-Conducting IGBT (RC-IGBT) is provided. It is shown that despite the benefits of the RC-IGBT, the device suffers from many undesirable design trade-offs that have prevented its widespread use. The RC-IGBT designs that have currently been proposed in literature, either present a trade-off in performance, an inability to be manufactured, or a requirement for a custom gate drive. This thesis presents a new RC-IGBT concept, the 'Dual Implant SuperJunction (SJ) RC-IGBT' that addresses these concerns and is manufacturable using current state of the art techniques. The concept and proposed manufacturing method enables, for the first time, a full SuperJunction structure to be achieved in a 1.2kV device.

In addition, an investigation into a coordinated switching scheme using both a silicon IGBT and silicon-carbide MOSFET was undertaken, which aimed to improve turn-off

losses within the IGBT without sacrificing on-state losses. Thermal modelling of the power devices switching under inductive load was explored as the system was optimised to use a SiC MOSFET in excess of its nominal ratings, reducing the overall system cost.

"Pooh began to feel a little more comfortable, because when you are a Bear of Very Little Brain, and you Think of Things, you find sometimes that a Thing which seemed very Thingish inside you is quite different when it gets out into the open and has other people looking at it"

A.A. Milne, The House at Pooh Corner (1928), Chapter 6

Acknowledgements

I would first like to acknowledge the EPSRC Doctoral Training Partnership scheme (grant RG75686) for supporting me financially during this PhD.

A special thanks goes to my supervisor, Prof. Florin Udrea, for his unwavering support, critical eye, and for having the confidence in me to allow me to explore my own ideas. His advice and knowledge have been invaluable.

To Dr Marina Antoniou, thank you for all your advice, good humour and support over the past three years; I have learnt so much from you. To Prof. Patrick Palmer, I am grateful for your continued encouragement and support, and it has been wonderful to collaborate with you (again!) during this PhD.

I would like to acknowledge the support of Dynex Semiconductor Ltd. and CRRC Corporation Ltd, in particular Lee Coulbeck, Dr Ian Deviny and Chunlin Zhu, for providing me with IGBT modules, sharing commercially sensitive information, and for assisting me in taking measurements.

I would also like to thank my colleagues in the High Voltage Microelectronics and Sensors Group for creating a friendly and enjoyable environment in the lab. In particular, my thanks go to Dr Nishad Udugampola who always went out of his way to assist me in taking the experimental measurements for this PhD thesis.

A special mention to Prof. Tim Wilkinson for his friendship and timely dinner invitations at Jesus College.

Finally, I would like to thank my friends and family; Sunil and John thank you for being so supportive. To my father, William Findlay, you inspire me every day and my passion for power electronics comes from you. Thank you for sharing your knowledge with me and challenging my thoughts. To my mother, Janet Findlay, you are my best friend and your unwavering support has encouraged me throughout my whole life. Thank you for helping me proofread this thesis and for always motivating me to keep going.

List of Contents

List of Publications

- E. M. Findlay, F. Udrea, and M. Antoniou, “Investigation of the Dual Implant Reverse-Conducting SuperJunction Insulated-Gate Bipolar Transistor,” IEEE Electron Device Lett., vol. 40, no. 6, pp. 862–865, 2019, doi:10.1109/LED.2019.2911994.
- E. M. Findlay and F. Udrea, “Modeling of Large Area Trench IGBTs: The Effect of Birds-Beak,” IEEE Trans. Electron Devices, vol. 40, no. 6, pp. 2686–2691, 2019, doi:10.1109/TED.2019.2911020.
- E. M. Findlay and F. Udrea, “Reverse-Conducting Insulated Gate Bipolar Transistor: A Review of Current Technologies,” IEEE Trans. Electron Devices, vol. 66, no. 1, pp. 219–231, Jan. 2019, doi:10.1109/TED.2018.2882687
- P. Palmer, X. Zhang, J. Zhang, E. Findlay, T. Zhang, and E. Shelton, “Coordinated Switching with SiC MOSFET for Increasing Turn-off dV / dt of Si IGBT,” 2018 IEEE Energy Convers. Congr. Expo., pp. 3517–3521, 2018
- E. M. Findlay and F. Udrea, “Investigation into the Effect of Emitter Geometry on the Performance of 3D Trench Insulated Gate Bipolar Transistor Structures,” IEEE Trans. Electron Devices, under review.
- E. M. Findlay, X. Zhang, E. Shelton, F. Udrea, and P. Palmer, “Optimisation of Coordinated Switching Scheme for SiC MOSFET and Si IGBT with Increased IGBT Turn Off dV/dt” [to be submitted in due course].

List of Figures

List of Equations

List of Tables

Chapter 1

Introduction

It is estimated that at least 50% of the electricity used worldwide is controlled by power transistors, with widespread use of these devices in the consumer, industrial, medical and transportation sectors [1]. Power semiconductors have been evolving since their invention in the late 1940's but with the move towards greater electrification for transportation, renewable energy sources, and industrial applications the demand for efficient power semiconductors is increasing. Given the number of these devices used worldwide, even a small increase in efficiency has the potential to have a significant impact upon global energy consumption, and so there is a need for the research activity in this field to intensify to meet this need. This chapter introduces the Insulated Gate Bipolar Transistor, the dominant power device in the 600V to 4.5kV range [2], within the context of the wider power semiconductor device market, detailing its invention, major development milestones, and performance characteristics. In conclusion, an outline for this thesis is provided.

1.1 The History of the Power Device

The invention of the bipolar transistor in 1947 was the first reported semiconductor power device [3]. Initial devices used germanium, which in 1952 was used to develop a 200V/25A power rectifier [4], however, by the end of the decade silicon (Si) had become the dominant material for power devices as it was more suitable for the diffused deep junctions that are required for high voltage blocking.

By 1956, the thyristor concept was proposed [5], and was the first example of a power device suitable for conducting both high current and high voltage. Initially, thyristors did not have gate control (they needed to be commutated off), but by 1961 the Gate-Turn-Off (GTO) thyristor was developed [6]. Further development of the GTO thyristor continued for a number of decades, as the devices were used extensively in traction and energy recovery circuits [7], [8].

The power Metal Oxide Field Effect Transistor (MOSFET) was developed throughout the 1970's [9]–[12] and culminated in a 600V power MOSFET by the end of the decade [13]. The power MOSFET, shown in Figure 1, is a voltage controlled device (with high input impedance on the gate) and therefore has much simpler gate drive requirements than thyristors, which reduces the cost and complexity of the control circuitry. However, compared to the bipolar action of the thyristors and power bipolar transistors, the power MOSFET, as a majority carrier device, has relatively poor on-state performance and limited blocking capability, which is governed solely by the thickness and doping of the drift region.

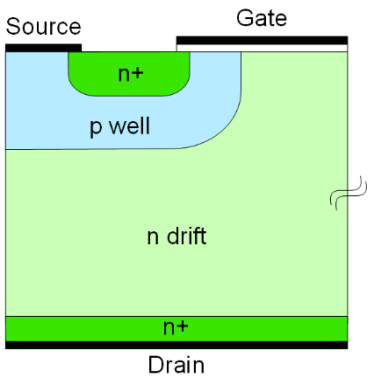


Figure 1 - Power MOSFET structure

The next logical step in device development was to combine the benefits of the earlier bipolar devices (low conduction losses) with the voltage, high impedance, gate control characteristic of the power MOSFET. The Insulated Gate Bipolar Transistor (IGBT) addressed these issues, and its invention is discussed further in Section 1.2. Today, the IGBT is considered to be one of the primary power devices on the market; currently IGBTs and IGBT modules account for 28% of the $17.5 billion power semiconductor industry ($4.8 billion market share), and in the next 5 years the IGBT market is set to increase in value to $6.18 billion [14].

Similar developments in lateral devices have been made, with the Lateral Double-diffused Metal-Oxide- Semiconductor (LDMOS) for low power applications and the lateral IGBT (LIGBT) [15] for relatively higher power. Both of these are suitable for use within power integrated circuits.

One of the major developments in the power semiconductor device was the invention of the superjunction concept in the late 1990's [16]–[18], which is widely considered the most innovative concept since the invention of the IGBT. The concept enables the device to surpass the limit of silicon, which is defined as the trade-off between on-state resistance and breakdown voltage as expressed in Equation 1. The application of highly n-doped and p-doped pillars to the drift region enables a more optimised distribution of electric field within the drift region compared to conventional power devices. The superjunction IGBT is explored in more detail in Section 1.5.1.

$$R_{specific-drift} = \frac{4BV^2}{\varepsilon_0 \varepsilon_r \mu_n \xi_{critical}^3} \approx 8.3 \times 10^{-9} V_{BR}^{2.5}\Big|_{silicon}$$

Equation 1 - Relationship between the specific drift resistance ($R_{specific-drift}$) and the breakdown voltage (BV) of the device, with the specific approximation for silicon. ε_0 is the permittivity of free space, ε_r is the permittivity the semiconductor material, μ_n the mobility of electrons, $\xi_{critical}$ is the critical electric field for the semiconductor material [1]

Since the 1990's work has also focussed on the use of wide bandgap materials, or materials with a larger bandgap energy compared to silicon [19], [20]. The primary materials of interest are silicon-carbide (SiC), gallium nitride (GaN) and, more recently, diamond. The first commercially available wide bandgap power device was a SiC Schottky diode introduced by Infineon in 2001 [21]. Since the development of the first

SiC MOSFET [22], several generations of devices have been developed and are commercially available in the 650V – 1.7kV range with current ratings in the region of hundreds of amps [23]. GaN devices are also emerging into the market, with high electron mobility transistors (HEMTs), metal-insulator-semiconductor FETs (MISFETs) and hetero-junction lateral Schottky diodes. However, the cost per amp of SiC and GaN is still significantly higher than Si since both the material and processing costs are greater [24], [25]. Diamond based devices, such as the vertical FET structure [26], are able to be produced in laboratory conditions, but given the processing requirements these devices are not yet close to commercialisation.

Figure 2 shows the suitable applications of the modern silicon power devices that are commercially available, in terms of their most efficient voltage rating and frequency of operation. It can be seen that the IGBT sits in between the thyristor and the power MOSFET, competing with both devices at the extreme of their respective operating windows.

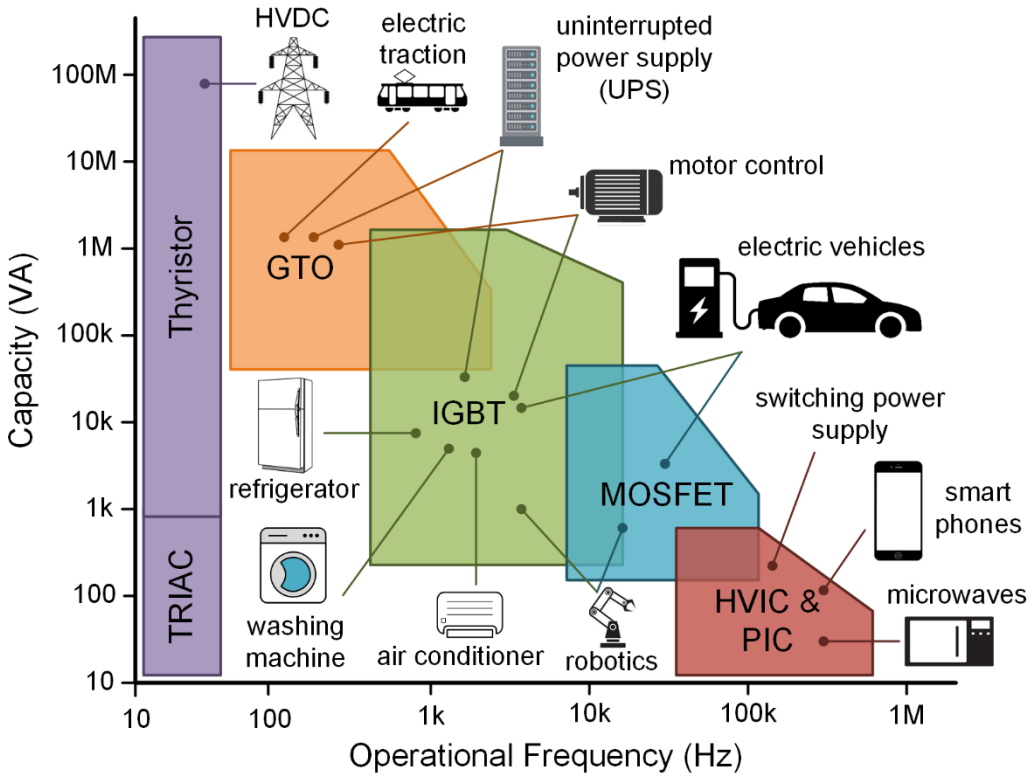


Figure 2 - Operational frequency and capacity of typical power devices with suitable applications marked [27]

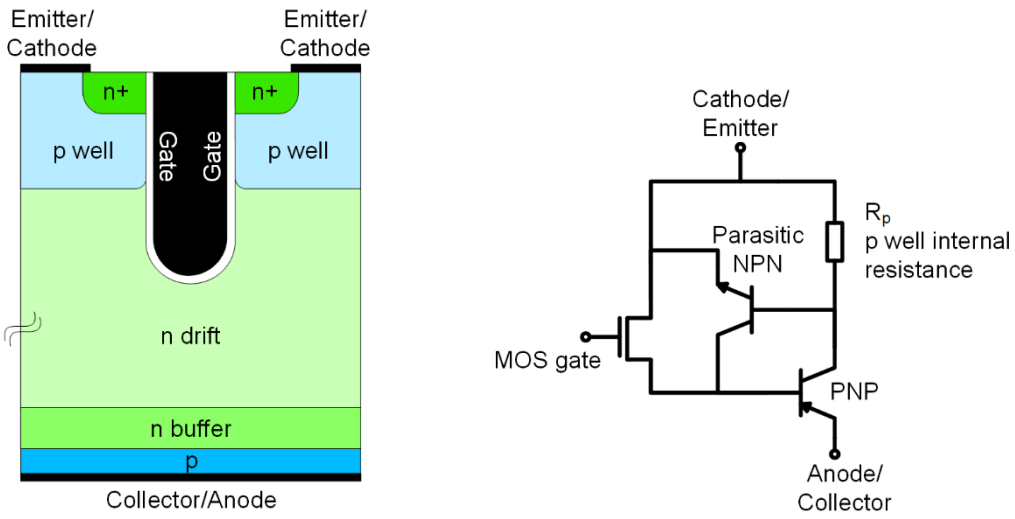
1.2 IGBT Invention

The attribution of the invention of the IGBT has been much disputed. It has often been claimed that several papers between 1979 and 1980 present the invention of the IGBT such as Baliga [28], Plummer [29], Leipold [30] and Tihanyi [31], but the structures described do not exactly emulate the IGBT behaviour. In the case of [28], [30], [31] the proposed device is described as a Metal Oxide Semiconductor (MOS) controlled turn-on thyristor, and [29] describes series connected bipolar transistors (or thyristors) with a MOSFET. [32]–[34] correctly describes an IGBT as a pnp transistor driven by a base current supplied via a MOS gate, and these references fall between 1982 to 1984. However, the first example of a bipolar structure driven by a MOS gate actually dates to 1968 from a patent by Mitsubishi [35], which also shows a structure almost identical to the modern IGBT and correctly describes the principle of operation. This structure was, though, not conceived for power applications, and was in fact designed for use within radio frequency (RF) circuits.

The name of the IGBT was derived from the Insulated Gate Transistor (IGT) and the Conductivity Modulated Field Effect Transistor (COMFET). Throughout the 1980's the original commercial devices could block only about 600V and a few amperes but today modern IGBTs can be rated in excess of 6.5kV and 3600A (when packaged in high-power modules) [36].

1.3 Structure of the IGBT

Figure 3 (a) shows the current commercial IGBT design. It consists of several regions; a trench MOS gate for high impedance voltage control and a bipolar pnp element formed form the p+ collector/n-buffer and n-drift/p-well which reduces the drift region resistance through conductivity modulation. The device is often viewed as the combination between a Power MOSFET and a bipolar transistor, as shown by the equivalent circuit in Figure 3 (b).



(a) (b)

Figure 3 - (a) Schematic of modern trench IGBT structure, (b) Equivalent circuit schematic of IGBT

1.3.1 Development of Trench Structure

The introduction of the trench gate was one of the major developments of the IGBT. Figure 4 shows a planar variant for comparison with Figure 3 (a). The trench design was first reported in 1986 [37] and demonstrated in 1989 [38] with the intention of increasing the MOS channel density and reducing latch-up susceptibility. Theoretically, a 30-40% overall loss advantage with no serious penalties in safe operating area (SOA) can be achieved [39]–[41]. Advanced trench structures have been developed by numerous manufacturers [42]–[45] despite initial reservations as to whether it would lead to any performance benefits [46], because direct experimental measurements were difficult due to issues with manufacturing of the trench. Improvements in etch quality and surface roughness through a combination of wet and dry etching or using a sacrificial oxidation [47], [48] helped overcome these issues. Fabrication of the trench is still, however, complex and defects such as birds-beak at the top of the trench still occur due to processing variations [49], [50].

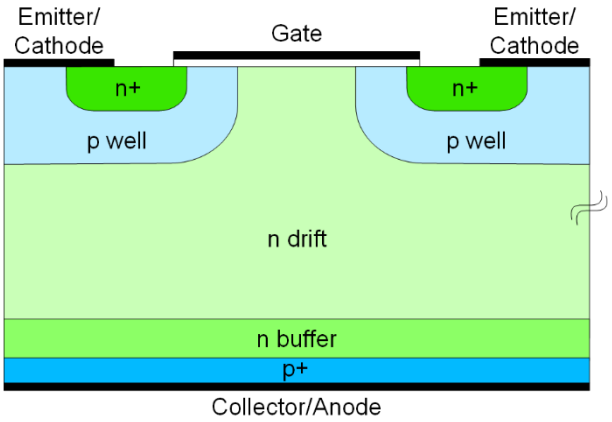


Figure 4 - Planar IGBT structure

The trench IGBT does offer a number of advantages compared to the planar variant [1], [38], [51].

- Higher channel density

  Trench cells are smaller than planar cells and therefore a greater number of MOS channels can be formed within a given area. This in turn reduces the channel resistance of the IGBT.

- Enhanced PIN diode effect

  The trench gate increases plasma injection, and hence conductivity modulation within the drift region. Electrons accumulate at the bottom of the trench effectively forming a thin n+ emitter layer for the PIN diode (which is formed with the p+ collector/ n-buffer and n-drift regions). Given this region under the gate is traditionally the weakest modulated region, the PIN diode effect can be significant. This enhanced conductivity modulation reduces on-state losses, but does not affect the turn-off, in particular the tail current, which is primarily governed by charge at the collector.

- No parasitic JFET effect

  Planar IGBTs can suffer from electron current crowding due to the depletion region formed between the p-well n-drift region. The trench structure effectively eliminates this effect (it is possible for this effect to remerge for very dense structures but in most cases, it is negligible).

- Reduced latch-up susceptibility

  The parasitic thyristor structure formed via the n+ emitter/p-well/n-drift and n-buffer/p+ collector is supressed as the n+ emitter implantation can be reduced in size as a result of the trench structure. This reduction in size reduces the lateral resistance under the n+ implant, reducing the likelihood of triggering the thyristor structure and the IGBT latching.

- Improved gate contact

  The thickness of polysilicon is larger for the trench IGBT which improves the gate contact and reduces the resistance, which results in a faster turn-on of the IGBT.

1.3.2 Emitter Design

The emitter design, including the trench gate placement and n+ and p+ implants can be varied to provide a trade-off between on state and short circuit performance.

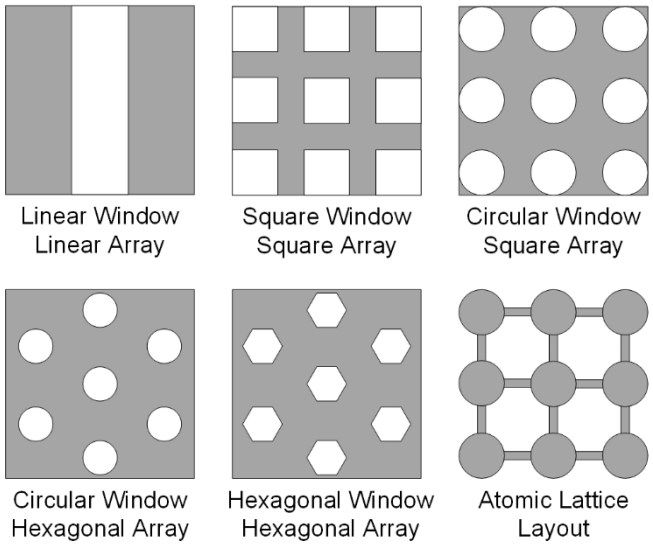


Figure 5 - Cell topologies for the IGBT [1]

The layout of the polysilicon gate on the top surface of the IGBT can follow many different geometries as shown in Figure 5. The linear window is actually the preferred design, with the other arrays suffering from either increased latch-up susceptibility or difficulty in producing an accurate mask [52]. Only the atomic lattice layout has improved

latch-up susceptibility [53] and has been used to produce an IGBT that does not latch even when operating in the saturation region at 200ºC [54]. Despite these benefits, the fabrication is still more complex and the linear gate layout has become the dominant design.

Using the linear gate layout, minimising the saturation current ($I_{c(sat)}$) and therefore improving the short circuit safe operating area (SCSOA), is typically achieved by increasing the number of dummy trenches (increasing the silicon area per cell) or reducing the channel size for a given cell area by alternating the n+ implant with the p-well under the emitter in the z dimension (hole bypassing the emitter). Hole bypassing the emitter was first proposed in 1994 [42] with the aim of increasing the channel resistance. A limited number of devices were fabricated, but measurements were not able to fully quantify the device behaviour [42]. A further study was conducted, implementing 2D simulation techniques with some experimental measurements, however this was unable to quantify all 3D effects within the IGBT due to modelling limitations [55]. The effect of hole current within the IGBT, and in particular its effect on the channel inversion, has also been considered but the study was limited to a 2D device model [39].

1.3.3 Drift, P+ Region and Plasma Distribution

The original IGBT designs were based upon a punch through (PT) concept (Figure 6 (a)), which uses a highly doped p+ substrate as a base material with the n+ and n- epitaxially grown on top. In the forward blocking state the entire n-region, which is made as short as possible to minimise on-state losses and tail current during turn-off, is depleted. Therefore, the electric field is terminated by the highly doped and relatively thick buffer. The main disadvantage for this structure is that the p+ anode is the substrate wafer and thus is required to be highly doped to avoid a high series voltage drop across this region. Consequently, the collector doping cannot be varied to control the injection and as such the n-buffer layer is required to be highly doped to control the amount of holes injected into the drift (the base transport factor), and often a further reduction of charge carrier lifetime is required using gold doping or electron beam irradiation. Lifetime killing methods require further fabrication steps and leads to a poor trade-off between on-state and transient losses. For a PT device the hole current accounts for 40-45% of the total current. [1], [56].

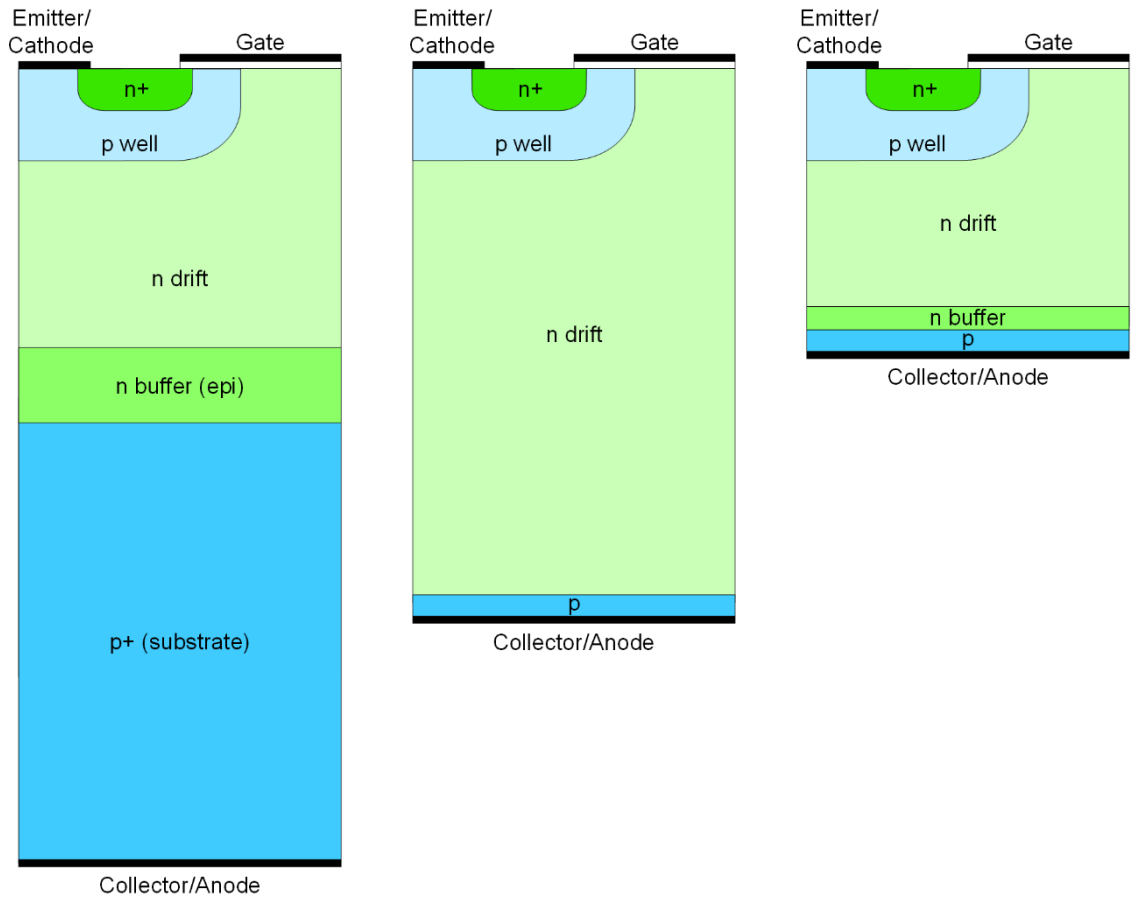


Figure 6 - Various collector designs for the IGBT, (a) punch though (PT), (b) non-punch through (NPT), (c) soft punch through (SPT) [57]

The alternate Non-Punch Through (NPT) concept (Figure 6 (b)) does not contain a buffer region as the n-drift is made longer such that, when blocking voltage, the depletion region does not reach the p+ collector, hence avoiding punch through. Unlike the PT device, the p+ collector implant is formed at the end of the fabrication process through back implantation and thus can be made relatively thin and the doping changed to modify the injection efficiency. Given this, the charge distribution for the NPT is more uniform and with a lower peak value at the collector. For a NPT device the hole current accounts for 20-25% of the total current. [1], [56].

The SPT [57], fieldstop (FS) [58] or light punch-through (LPT) [59] design (Figure 6 (c)) offers a compromise between the PT and NPT IGBT structures. It has a short punch-through type drift region (similar to the PT design), but also includes a buffer region and lightly doped p collector (characteristic of the NPT). The concept controls hole injection by changing the efficiency of the emitter junction, and as such the buffer is more lightly

doped than a traditional NPT IGBT; low enough to not influence hole injection but sufficiently high to prevent the depletion region reaching the collector contact. This results in a device with an initial fast turn-off typical of a NPT but eliminates the long tail [36], [57]. Compared to the PT design, the SPT has a soft turn-off behaviour reducing noise, overshoot and electromagnetic interference (EMI) issues [57], and a positive coefficient of temperature with resistance, making it suitable for paralleling devices for use in higher power applications [36], [57].

The three concepts are compared in Table 1, but given the performance and manufacturing benefits, the Trench SPT IGBT is the leading IGBT design.

Feature	PT IGBT	NPT IGBT	SPT IGBT
Drift layer thickness	Thin	Thick	Thin
Wafer type used for fabrication	Epitaxial	Float Zone	Float Zone
Buffer layer	Thick and highly doped	N/A	Thin and lowly doped
P+ collector implant	Thick and highly doped (substrate)	Thin and relatively lowly doped	Thin and relatively lowly doped
Bipolar gain control method	Lifetime killing	Injection efficiency	Injection efficiency
Relative on-state losses	Low	Medium	Low
Relative switching losses	High	Low	Low
Relative turn-off current tail duration	Short	Long	Short
Relative voltage overshoot (inductive applications only)	High	Low	Low
Temperature coefficient	Negative (under majority of conditions)	Positive	Positive

Short Circuit Safe Operating Area	Medium	Large	Large
Reverse Bias Safe Operating Area	Narrow	Large	Large

Table 1 - Comparison of PT, NPT and SPT IGBT structure and behaviour [1], [36], [56], [57]

1.4 Manufacture of the IGBT

Fabrication of the trench IGBT begins either on epitaxial wafers (PT IGBT) or float zone wafers (NPT and SPT IGBT). Firstly, the device termination is formed around the outside of the cell, followed by the diffusion of the p-well. In the case of SPT and NPT devices, the p+ collector implant is formed on the backside of the wafer and annealed. For all wafers, the n+ source is formed and the trench is etched through a multilayer mask using a combination of wet and dry etching or using a sacrificial oxidation [47], [48]. Following this, gate oxidation, polysilicon filling and etch-back, and polysilicon oxidation with further thickening with deposited oxide is undertaken. Contacts are made via metal deposition and patterning, passivation and pad opening. [44].

1.5 Alternate IGBT-Based Structures

There are a range of IGBT variants that have been proposed in literature, the most significant of which have been summarised below.

1.5.1 Superjunction IGBT

The superjunction (SJ) IGBT, based upon the CoolMOS concept [16], [18], [60], was first reported in [61] with further development in [62]–[65]. In this device the drift region has n and p pillars which are more highly doped than the typical IGBT n-drift, as shown in Figure 7. These pillars are doped to meet charge balance requirements [66]. Under forward blocking, the pillars deplete laterally at a lower voltage compared to a traditional constant drift region implant, resulting in a uniform potential distribution (approaching a square electric field along the drift region compared to a triangular distribution for NPT

and trapezoidal for PT), which maximises the breakdown of the device per drift unit length. However, compared to the SPT IGBT, the superjunction IGBT only offers a marginal improvement in drift region length as the SPT cell has already been optimised to approach a square electric field distribution.

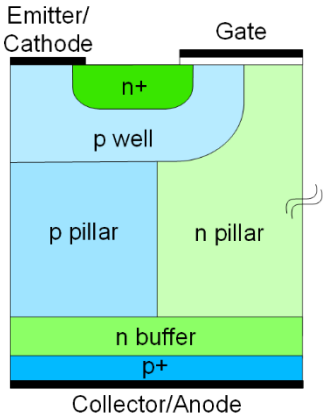


Figure 7 - Superjunction IGBT structure [61]–[65]

The on-state and transient performance of the superjunction IGBT offers several benefits compared to the traditional IGBT structure. The n/p pillars result in plasma clustering in the middle of the device towards the anode [62], whereas in an ordinary IGBT this plasma is at the cathode. Typically an absence of plasma at the cathode would significantly increase the drift resistance of the IGBT (as there is no conductivity modulation in this region), but in the superjunction structure the doping of the pillars in the drift region can be increased by at least one order of magnitude compared to an ordinary drift region. Therefore, this unipolar conduction through the pillars does not result in excessive resistive losses at the cathode side of the drift region [62]. This behaviour applies similarly to lateral bipolar superjuntion devices [67]. Due to this reduced plasma formation in the superjunction IGBT, the switching speed is significantly improved as the device does not suffer from the long tail that is characteristic of the IGBT. It is also worth noting that the SJ IGBT will only be suitable for lower breakdown voltages (<1.7kV) as to achieve a higher blocking voltage the n/p pillar doping must be increased. To compensate for this the anode injection efficiency must also be significantly increased, which results in a non-uniform plasma distribution and excess charge at the anode side that, in turn, limits the performance benefit offered by the SJ IGBT at these higher breakdown voltages.

Fabrication of the full superjunction is, however, complex. State of the art fabrication techniques limits a pillar length to 65µm [68] as there is a concern regarding the creation of voids within the structure [69]. Therefore it is not possible to produce a full superjunction structure in a 1.2kV IGBT and hence the semi-superjunction IGBT (Figure 8) has been proposed, which offers some, if not all of the benefits of the full SJ IGBT [66]. A variation with the superjunction implant applied from the anode-side has also shown similar benefits [70]. Experimental results for the SJ-SPT-IGBT and SJ-NPT-IGBT were reported at 650V validating the simulation models and indicating that the switching losses of the SJ-NPT were lower than the SJ-SPT-IGBT. The SJ-NPT device had better short circuit ruggedness than the SJ-SPT, but both exhibited superior on-state and switching performance compared to a traditional SPT-IGBT [69]. The results highlight that the trade-off between the forward and reverse conduction capabilities in the superjunction design is difficult to optimise [71].

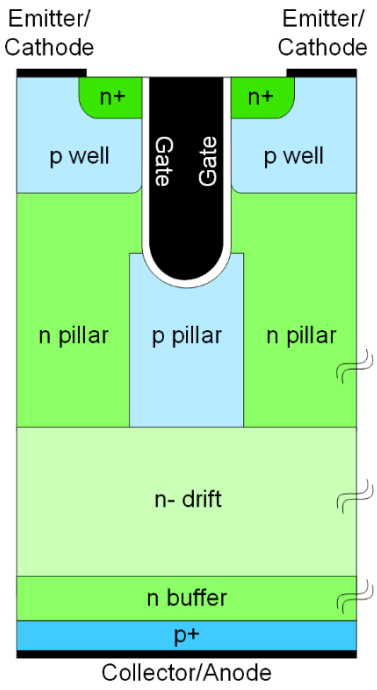


Figure 8 - Semi-SJ IGBT structure [66]

1.5.2 Injection Enhanced Gate Transistor

The Injection Enhanced Gate Transistor (IEGT) shown in Figure 9, is a trench IGBT with a reduced n+ emitter contact area. It features unconnected cells that reduces hole injection since holes are required to travel along long resistive paths to reach the cathode shorts [43], [72]. This concept is similar to the dummy p-well regions and dummy trenches used in modern IGBT designs (as discussed in Chapter 3), but here the trenches are much deeper and wider than in a standard IGBT. This results in enhanced electron injection at the cathode side of the drift region, in a similar way to the PIN diode effect as discussed in Section 1.3.1, and these dummy trenches act as field plates when the device is blocking forward voltage. The device offers a low on-state voltage drop without a significant effect on the switching losses [73]. The IEGT cell has been optimised for 3.3kV and 4.5kV [72].

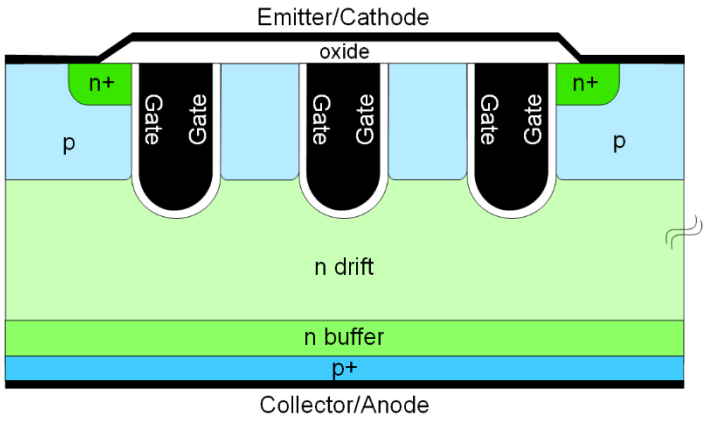


Figure 9 - Injection Enhanced Gate Transistor (IEGT) structure [43]

1.5.3 Carrier Store Trench Bipolar Transistor

The Carrier Store Trench Bipolar Transistor (CSTBT) features a PIN diode structure within the IGBT as a n+ layer (denoted as n-injector) is placed under the p-well as shown in Figure 10 [74]. The device is produced by Mitsubishi [75]. The placement of the n+ layer weakens the pnp bipolar transistor within the device, instead creating a PIN diode (p+ collector/n-buffer, n-drift/n-injector) which acts in parallel with the PIN diode effect formed under the trench gate (Section 1.3.1). Similar to the IEGT concept (Section 1.5.2), the CSTBT has increased conductivity modulation at the top side of the drift region, but this n-injector can be difficult to optimise as it can degrade the breakdown performance.

If the n-injector doping is too high, it can inhibit depletion region growth into the drift region, which can result in premature avalanche of the device, but it must be sufficiently high otherwise the benefit of the PIN diode is supressed.

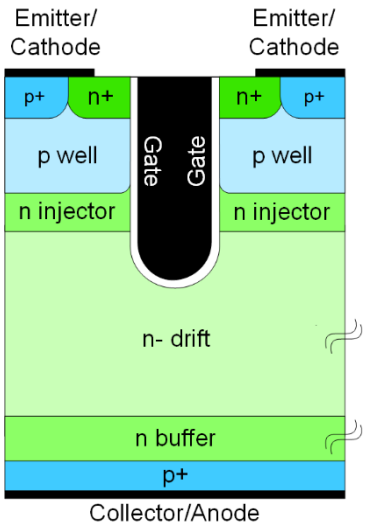


Figure 10 - Carrier Store Trench Bipolar Transistor [74]

A variant of the CSTBT is the Trench Emitter Switched Thyristor (Trench EST), which includes an additional second p-well below the n-injector, creating a thyristor structure (rather than a PIN diode) [76]. Again, this variant increases plasma formation at the top of the drift region, but it is important that the n+ injector is discontinuous in the third dimension (into the page) to enable safe removal of holes during switching. Fabrication is also difficult as stacks of doping layers must be produced under the p-well, and it is this that has prevented the concept becoming a commercial product.

1.5.4 High Conductivity IGBT

The High Conductivity IGBT (HiGT) is another variant on the IEGT and CSTBT concepts, produced by Hitachi [77]–[79]. In this case, to enhance electron injection at the top of the device a n layer is placed around the p-well to prevent holes from reaching the cathode short (p+ implant under cathode). A trench and SPT variant has also been produced [78]. Its operation, and issues, are almost identical to the CSTBT cell (Section 1.5.3).

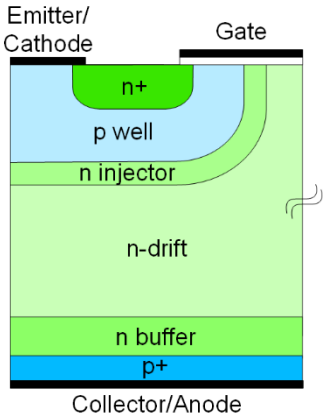


Figure 11 - High conductivity IGBT structure (HiGT) [77]

1.5.5 Reverse-Conducting IGBT

A full review of the Reverse-Conducting IGBT is given in Chapter 5.

The Reverse-Conducting IGBT (RC-IGBT) structure was first proposed in 1987 with a collector shorted, p-channel IGBT [80] building upon the concept suggested by Ueda et al. [37]. The concept is to integrate a reverse conducting diode within the IGBT, in a similar fashion to an inherent body diode within a power MOSFET, for use within applications which require a free-wheeling diode. Figure 12 shows the RC-IGBT structure, which differs from a traditional IGBT due to the inclusion of n+ regions (anode shorts) into the p-collector (p-anode) [71], [81]. When a reverse voltage is applied to the device, electrons are provided by the n+ anode short and holes are injected from the p+ emitter (p+ cathode), resulting in the device behaving similar to a PIN diode. The RC-IGBT has several benefits over a separate IGBT and diode solution and has the potential to become the dominant device within many power electronic applications. However, the device suffers from many undesirable design trade-offs that have prevented its widespread use, most prominently a snapback in the on-state characteristic that can lead to overheating and ultimately the destructive failure of the device [82]. These issues with the RC-IGBT are discussed further in Section 5.2.

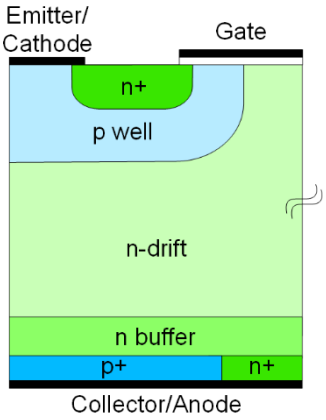


Figure 12 - Reverse conducting IGBT structure [83]

1.6 Modes of Operation

The IGBT operates in four modes;

- Off state

  The reverse-biased PIN junction (formed from the p-well/n-drift/n-buffer) supports the voltage applied to the device between the collector and emitter. The drift region doping and length is optimised such that the main mechanism for breakdown is avalanche at the p-well/n-drift boundary.

- Turn-on

  Application of a positive gate voltage with respect to the emitter (for n-channel) causes inversion of the p-well under the gate and the formation of a MOS channel between the n+ emitter implant and n-drift, enabling the flow of electrons towards the collector. This electron current serves as the base current of the pnp transistor (p+ collector/n-buffer, n-drift/p-well), which when triggered injects holes into the drift region. The conductivity of the n-drift layer increases rapidly as plasma is formed.

- On-state

  The total current flowing in the on-state is equivalent to the sum of the electron current flowing through the MOS channel and the hole current from the collector to the emitter. Typically, the static gain of the pnp transistor within the IGBT is between 0.2 and 0.5.

- Turn-off

  The IGBT is turned off by reducing the gate-emitter voltage, typically reduced to -15V to increase the speed of turn-off. This removes the MOS channel, which removes the base current to the pnp element of the IGBT. The turn-off speed is determined by the open base current decay of this pnp transistor and the time taken to remove the excess plasma within the drift region. These features result in the long tail in the current during turn-off which is characteristic of the IGBT.

In the following sections, some of these operational cases are expanded in more detail.

1.6.1 On-state

On-state characteristics of an IGBT, shown in Figure 13, are very similar to those of a MOSFET, except that conduction begins at a collector-emitter voltage (V_{ce}) of 0.7V, and not 0V as for a MOSFET. This is because the p+ collector/n-buffer junction must be forward biased for hole injection, which for silicon requires 0.7V to be applied. Despite showing linear and saturation regions similar to that of a MOSFET, just after turn-on the IGBT exhibits a slight superlinear region where there is a rapid decrease in the on-resistance as conductivity modulation occurs within the device. Saturation of the IGBT is caused by the same mechanism as for the MOSFET – pinch off of the channel. Current densities of the IGBT are also higher than a typical MOSFET (100-200A/cm^2 compared to 30A/cm^2 respectively).

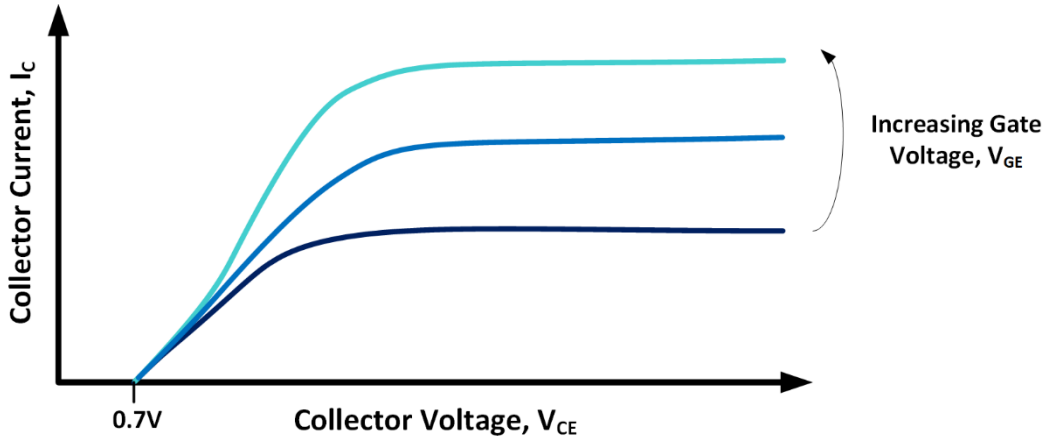


Figure 13 - Schematic representation of IGBT on-state characteristics

1.6.2 Turn-Off

Typically, IGBT turn-off events occur under inductive load conditions using a circuit similar to that shown in Figure 14. The IGBT switching characteristics are similar to those of a power MOSFET, and a typical turn-off waveform is shown in Figure 15 [1], [84]–[86].

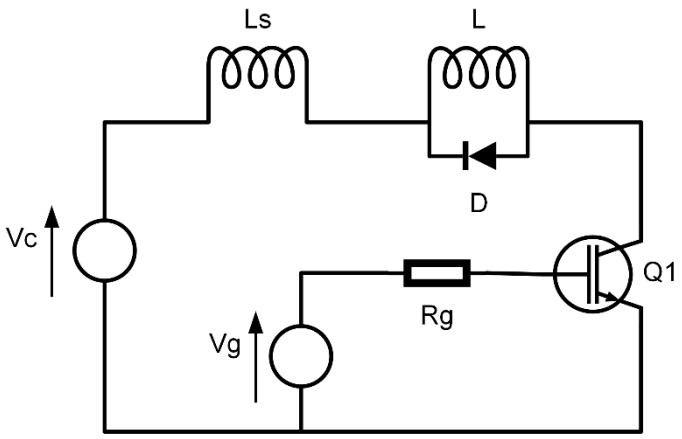


Figure 14 - Schematic of IGBT inductive load transient test circuit [87]

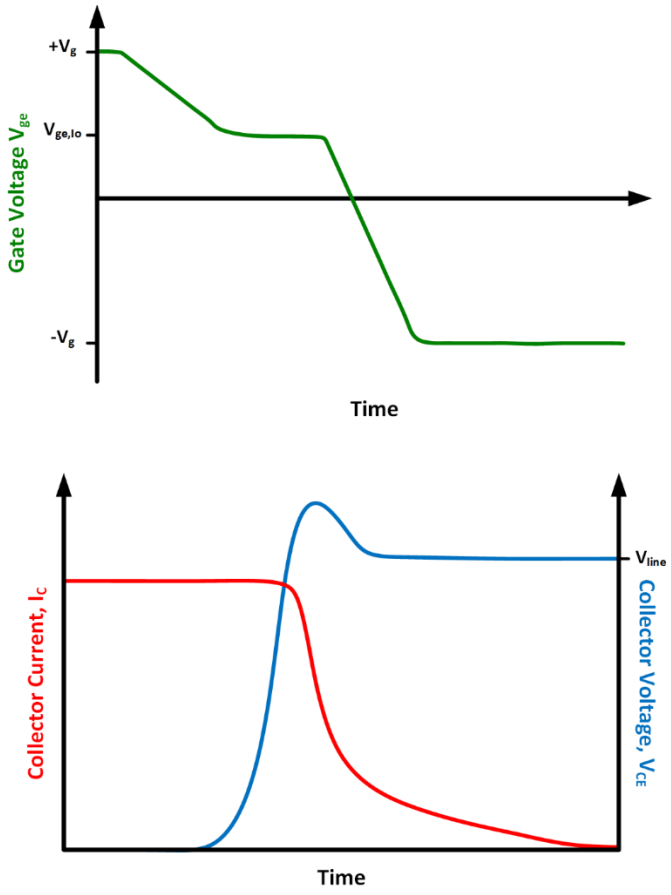


Figure 15 - Schematic representation of IGBT turn-off characteristics under inductive load conditions

At the point at which the gate-emitter signal voltage is driven low (typically -15V), the voltage at the gate of the IGBT (V_{ge}) falls slightly to reach the initial plateau ($V_{ge,Io}$) with no change in collector current or voltage, and this is the source of the majority of the turn-off delay for an IGBT. $V_{ge,Io}$ is the local threshold voltage and at this gate voltage the Miller capacitances are being discharged such that the MOS channel can be removed and there is no further injection of electrons into the n-drift. The collector voltage increases from this point as the depletion region begins to form within the device at a rate limited by the gate resistance as defined in Equation 2.

$$\frac{dV_{ce}}{dt} = \frac{\mathrm{V_{ge,Io}}}{C_{gc}R_g}$$

Equation 2 - Rate of increase of collector voltage (V_{ce}) at turn-off of IGBT where $V_{ge,Io}$ is the gate voltage at full-load collector current I_o at turn-off, C_{gc} parasitic gate-collector capacitance, R_g is the gate resistance [85]

At the point at which the collector-emitter voltage reaches the supply rail voltage, the free-wheeling diode takes over the current through the inductor such that the IGBT current is allowed to fall. Typically, there is also an overvoltage spike in the collector voltage above the supply voltage induced by the stray inductance in series with the IGBT and the collector current reducing (negative $\frac{di}{dt}$). The rate of decrease of collector current is limited by the gate resistance as shown in Equation 3;

$$\frac{di_C}{dt} = g_{fe}\frac{\mathrm{V_{ge,Io}}}{(C_{ge} + C_{gc})R_g}$$

Equation 3 - Rate of decrease of collector current (i_c) at turn-off of IGBT where g_{fe} is the device transconductance, $V_{ge,Io}$ is the gate voltage at full-load collector current I_o at turn-off, C_{ge} the parasitic gate-emitter capacitance, C_{gc} the parasitic gate-collector capacitance and R_g is the gate resistance [85]

As the collector current decreases, there are two sections to this curve. Initially there is a rapid decrease in collector current which is due to the removal of the fraction of the electron current (MOS current) at the cathode terminal. This is followed by the long 'tail' caused by the bipolar current from the internal pnp transistor structure. It is this long 'tail' that is responsible for the majority of IGBT turn-off losses and which also limits the

maximum switching frequency. Stored charge remains in the n-drift region which can only be eliminated through recombination (carrier sweep out is not possible as the MOSFET portion of the device is off and there is no negative voltage applied to the IGBT to produce a negative drain current). It is typically desirable for the carrier lifetime in this region to be high to reduce the on-state voltage drop, but this, in turn, worsens the switching performance.

1.6.3 Safe Operating Area

The safe operating area (SOA) is defined as the boundary of voltage and current which a power device can be operated in without destructive failure [1]. For an IGBT the maximum collector current at low V_{ce} is limited by the on-set of thyristor latch up (triggering of the parasitic thyristor formed by n+ emitter/p-well/n-drift, n-buffer/p+ collector). At high collector-emitter voltages and low current the maximum voltage is constrained by breakdown of the device. It is worth noting that during switching events, there are instances when the IGBT must be able to conduct high current under high voltage conditions. During this time the device can be susceptible to avalanche-induced secondary breakdown, which would result in the destructive failure of the device; during turn-on this phenomenon limits the forward-biased safe operating area (FBSOA) and during turn-off the reverse-biased safe operating area (RBSOA).

The short-circuit safe operating area is another key parameter for the IGBT. There are occasions when an IGBT may experience a short circuit event (due to failure or an event in the surrounding circuitry) [1]. Industry standards state that the IGBT must be able to withstand this high current flow under short-circuit conditions for 10μs under elevated ambient temperatures (150ºC) [87] as this represents the worst-case time taken for gate drivers to detect the event and turn off the IGBT. Typically though, to improve the reliability of the device, most commercial IGBTs are designed to withstand short circuit conditions far in excess of this 10μs minimum. The time that the IGBT survives under these conditions is known as the short circuit endurance time of the device and the capability of the IGBT to withstand this particular high voltage, high current condition is referred to as the short circuit safe operating area (SCSOA).

1.6.4 High Temperature Operation

IGBTs often operate at high temperatures, typically 125ºC but often 150ºC and sometimes 175ºC. The bipolar and MOS elements have opposite behaviours for increasing temperatures so the IGBT has competing effects making its behaviour more complex to predict. The MOS proportion of the device has a positive relationship between temperature and on-state losses (as the temperature increases so does the voltage drop across the device), but the bipolar element has the opposite relationship. In general, with elevated temperature, the mobility degrades significantly in the MOS channel (reduction in transconductance). In the drift, this reduction in mobility with temperature is still present, but the hole injection efficiency and lifetime compete against this effect and increase with temperature. Overall, the threshold voltage of the IGBT typically reduces with temperature, since the voltage drop across the anode junction reduces (at a rate of 2mV/ºC), and it is this property which governs much of the IGBT behaviour, such as an increase in saturation current with temperature and transient losses. [1], [88]–[91].

1.7 Overview of the Thesis

This thesis will deal with a variety of topics concerning the design and optimisation of the IGBT. The discussion will cover several areas including device-based, and circuit level investigations, using both experimental data and advanced 3D modelling techniques.

- Chapter 2 will introduce the simulation techniques used throughout this thesis. The discussion will focus on the necessary considerations that must be made to develop a verified model that emulates the behaviours of manufactured devices.
- Chapter 3 uses these simulation techniques and focusses on the development of the 3D IGBT model based upon a commercial device. This model is verified using experimentally gathered data. It is shown that a single accurate model could not be produced due to widespread birds-beaking across the IGBT die area. Instead a two-device model is proposed to fully characterise the behaviour of the device in all modes of operations, including static and dynamic as well

as during fault modes such as short-circuit. It is demonstrated that this birds-beaking significantly reduces the reliability of the device.

- Chapter 4 uses this fully verified 3D IGBT model to determine an optimum design for the IGBT emitter geometry that considers critical 3D effects omitted from previous studies. In particular the effect of varying the n+ emitter implant depth in the third dimension is investigated and it is revealed that there are competing effects within the IGBT.
- Chapter 5 presents an extensive review and critical analysis of current reverse-conducting IGBT concepts. The chapter presents the most promising RC-IGBT concepts, which have been simulated under the same conditions such that they can be directly compared. The limitations of each design is evaluated and reveals that all concepts either present a trade-off in performance characteristics, an inability to be manufactured, or a requirement for a custom gate drive.
- Chapter 6 introduces the new novel RC-IGBT concept; the Dual Implant SuperJunction Reverse-Conducting IGBT. The device is fully characterised, in terms of its blocking, on-state and transient performance and compared to a traditional RC-IGBT structure to highlight the performance benefits of the new structure.
- Chapter 7 utilises the verified IGBT model alongside a SiC MOSFET simulation model to investigate the use of a circuit-based solution to produce a novel low-cost solution to improve the IGBT dV_{ce}/dt without affecting the on-state performance. Thermal analysis is undertaken to determine the suitability of the concept and it is shown that a SiC MOSFET can be safely used in this topology while exceeding its device current rating by a factor of three.
- Chapter 8 summarises the conclusions made in the thesis and discusses the potential for future research in light of these results.

Chapter 2

Sentaurus TCAD Simulation Methods

It is commonplace to use simulation tools to predict the behaviour of circuits prior to manufacture, enabling the optimisation of designs at minimal cost. Circuit level simulations, such as Simulation Program with Integrated Circuit Emphasis (SPICE), use compact models for transistors, which require little computational effort but yield less accurate results. To improve the accuracy of the simulation output, finite element modelling software, such as Sentaurus technology computer-aided design (TCAD), allows the physical interactions within the device to be modelled, but at the expense of computational effort.

The simulation work conducted in this thesis has been completed in Sentaurus TCAD, with a particular focus on simulations in three-dimensions. This chapter provides an overview of the physical models used in these simulations, and specific techniques for modelling these structures.

2.1 Introduction

Sentaurus TCAD is an electrothermal, mixed-mode device and circuit simulator for one-dimensional, two-dimensional, and three-dimensional semiconductor devices. It solves coupled, non-linear partial differential equations, using advanced physical models derived from experimental measurements. The physical models describe the carrier distribution and conduction mechanisms within the device. By combining these models with user defined set-up parameters (such as terminal voltages and ambient temperature), currents, voltages, and charges are computed. The simulation software is capable of simulating most types of semiconductor device, in silicon as well as silicon-carbide (SiC) and III–V compound homostructure and heterostructure devices. Typically, most TCAD simulations used for power device development are completed in two-dimensions, however with the improvement and reduction in cost of computational power three-dimensional models are becoming increasingly prominent. [92]

This chapter outlines the critical physical models activated within Sentaurus TCAD when simulating silicon-based power semiconductors and explains some of the techniques implemented to achieve accurate results while minimising computation effort. Given Chapter 7 introduces a SiC MOSFET model, a wide bandgap material, a brief description of specific SiC models have also been included.

2.2 Physical Models

Physical models applied to silicon devices include mobility models, a definition for the bandgap and the intrinsic carrier concentration, as well as any other effects which need to be considered such as impact ionisation (avalanche breakdown). Details about the main models used in this thesis are given in the sub-sections below. Unless otherwise stated, the Sentaurus default parameters were used as defined in [92]. Appendix A.1 lists any alternate parameter values used, which are particularly applicable to 3D Si IGBT models, and Appendix A.2 provides the simulation parameters used for SiC models.

2.2.1 Bandgap Modelling

There are two models primarily used to model the bandgap (and therefore, the intrinsic carrier density) in silicon; Slotboom bandgap narrowing and the old model for Slotboom

bandgap narrowing. These two models are fundamentally the same but have different default parameters.

The Sentaurus bandgap model follows the empirical formula given in Equation 9 [92], [93];

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta}$$

Equation 4 - Lattice temperature-dependence of bandgap where $E_g(0)$ is defined as the bandgap energy at 0K (1.1648eV for Slotboom and 1.1537 for Old Slotboom), T is the temperature of the lattice and α and β are material parameters, which for silicon are 4.73e-4 eV/K and 636K respectively [92], [93]

Equation 5 describes how Sentaurus calculates effective bandgap having considered the effect of bandgap narrowing, where ΔE_g^0 varies between different bandgap models. Equation 6 provides the specific equation for ΔE_g^0 for the Slotboom models, where the only difference between the Slotboom bandgap narrowing model and the old model for Slotboom bandgap narrowing are the specific values for the parameters. Note that ΔE_g^{Fermi} in Equation 5 is an optional correction to account for carrier statistics and is applied to all models for bandgap narrowing within Sentaurus. The model is based upon the measurements of the material parameter $\mu_n n_i^2$ for npn bipolar devices and $\mu_p n_i^2$ for pnp bipolar devices (where is μ_n is the mobility of electrons, μ_p the mobility of holes and n_i the intrinsic carrier density) from silicon bipolar transistors and a 1D model for collector current [94]–[97].

$$E_{g,eff}(T) = E_g(T) - \left(\Delta E_g^0 + \Delta E_g^{Fermi}\right)$$

Equation 5 - Effective temperature dependent bandgap of a material $E_{g,eff}(T)$, where $E_g(T)$ is defined in Equation 4, ΔE_g^0 describes the bandgap narrowing at 0K and is dependent on the model of bandgap narrowing used, ΔE_g^{Fermi} is an optional correction to account for carrier statistics

$$\Delta E_g^0 = E_{ref}\left[\ln\left(\frac{N_{tot}}{N_{ref}}\right) + \sqrt{\left(\ln\left(\frac{N_{tot}}{N_{ref}}\right)\right)^2 + 0.5}\right]$$

Equation 6 - Bandgap narrowing for the Slotboom and Old Slotboom model where E_{ref} and N_{ref} are material defined parameters and N_{tot} is the total doping concentration. For Slotboom model, E_{ref} is 6.92e-3eV and N_{ref} is 1.3e17cm-3. For old model for Slotboom, E_{ref} is 9.0e-3eV and Nref is 1.0e17cm-3.

Although both models are suitable for use within vertical silicon power devices, the old model for Slotboom bandgap narrowing has been shown to be more physically realistic in certain circumstances [98].

2.2.2 Mobility Models

The mobility of a carrier, either electron or hole, is defined as the proportionality contestant that relates the average carrier velocity and the electric field [1];

$$\upsilon = \mu E$$

Equation 7 - Average carrier velocity (υ) as a function of the mobility of the carrier (μ) and the applied electric field (E) [1]

Free carriers, travelling in the direction of the electric field, undergo scattering events, which can occur due to a number of different reasons. In the bulk, scattering can occur either due to an interaction with the lattice (dependent on temperature) or with ionised donor/acceptor atoms (dependent on the concentration of ionised impurities). Additional scattering near semiconductor surfaces also occurs, and in bipolar devices the high concentration of electrons and holes being simultaneously injected increases the probability of mutual scattering and, hence reducing the effective mobility. [1].

To account for all these effects, different mobility models are used within Sentaurus which can be combined using Matthiessen's rule [92]:

$$\frac{1}{\mu} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + \frac{1}{\mu_3} + \cdots$$

Equation 8 - Overall mobility of carriers (μ) defined as an average of mobilities derived from individual models (numbered 1,2,3…) [1]

The following mobility models were implemented within Sentaurus for device simulations detailed within this thesis [92];

- Doping dependent Masetti model

  Mobility degradation due to impurity scattering (primarily used for 2D models only)

- Doping dependent Philips Unified Mobility Model

  A well calibrated model, which describes both majority and minority carrier bulk mobilities. The model accounts for the temperature dependence of mobility, electron-hole scattering, screening of ionised impurities by charge carriers and clustering of impurities.

- Enhanced Lombardi Model

  Particularly applicable to MOS channels, this model accounts for mobility degradation at interfaces, which for MOS channels is caused by the high transverse electric field that forces carriers to interact strongly with the semiconductor-insulator interface. This model account for the surface contribution due acoustic phonon scattering as well as surface roughness.

- Canali Model for High-Field Saturation

  In high electric fields, the relationship given in Equation 7 no longer applies and the velocity of carriers saturates to a finite speed. This model is temperature dependent, and the output depends on the other mobility models that have been activated for the simulation. This can be calculated either parallel or perpendicular to the interface.

For all these mobility models, the parameters used are the default silicon parameters as defined by Sentaurus [92]. These parameters have been derived from extensive simulations, experimental results, and values published in literature. If desired, specific silicon crystallographic lattice orientation values are available for some of these models which can be used instead. This is discussed further in Chapter 3, and these parameter values are given in Appendix A.1.

2.2.3 Generation-Recombination Models

Generation-recombination models describe the processes that exchange carriers between the conduction and valence band, which are particularly significant for bipolar devices. There are three main models implemented [92];

- Shockley-Read-Hall Recombination

  This model describes recombination through deep defect levels in the gap between the conduction and valence bands. It can account for lifetimes which are a function of doping, electric field and temperature, but typically only doping and temperature dependence is used in power device models.

- Auger Recombination

  Auger recombination is the process in which an electron and a hole recombine in a band-to-band transition, and the resulting energy produced by this recombination passes to another electron or hole. This model is temperature dependent and accounts for the decrease of the Auger coefficients at high injection levels [99].

- Avalanche Generation (van Overstraeten – de Man Model)

  Electron-hole pair production due to avalanche generation (impact ionisation) only occurs once an electric field threshold has been met, and if there is a possibility of acceleration of these carriers (wide space charge regions). Temperature dependence is accounted for and the coefficients of this model are derived from experimental results [100]. *Avalanche is typically only applied in breakdown simulations to avoid unnecessary computational effort.*

2.2.4 Temperature Dependence

Calculation of the lattice temperature is required to describe self-heating within the device, which is critical for some simulations such as short-circuit fault conditions. This is typically calculated using the thermodynamic model, which implements drift-diffusion models to calculate a spatially dependent lattice temperature during a standard circuit simulation. The effect of heatsinks and packaging can also be accounted for by defining thermal resistance on contacts. [92].

2.2.5 SiC Specific Models

Silicon can typically be considered to be fully ionised at room temperature, however, for aluminium acceptors in silicon carbide it is no longer safe to make this assumption, and hence the incomplete ionisation model must be activated. The incomplete ionisation

model is probability based, using the activation energy of the dopants and the temperature to calculate the likelihood of ionisation.

Traps also need to be considered at the SiC/oxide interface. These traps account for a defect in the crystallographic structure that can capture a carrier, and a large density of traps, which is characteristics of a SiC/oxide interface, can prevent the formation of high conductivity inversion layers [1], [101]. Within Sentaurus TCAD the concentration of these traps within a region can be specified, as well as the energy distribution within the bandgap. For the SiC model used in Chapter 7, the most simplistic approach is taken whereby the concentration is modelled as a fixed charge at the interface, which is, by default, taken to be distributed over 13 energy levels in the bandgap [92].

Also, for SiC devices Fermi statistics are activated. For silicon devices, Boltzmann statistics are used to describe the behaviour of electrons or holes. Fermi, or Fermi-Dirac, statistics are physically more correct, but computationally more expensive, however they are important to use for high carrier densities in excess of $n>1e19cm^{-3}$. Given the SiC device studied in this thesis is only modelled in 2D, it was acceptable to activate this more complex model. [92].

An alternate parameter set for the SiC models is given in Appendix A.2, which accounts for the material variation compared to silicon, and also the additional models activated.

2.3 Contact

Sentaurus TCAD enables contacts to be specified as electrodes, which mark an electrical boundary condition. These regions are not included in the simulation (are not meshed, see Section 2.4) and are therefore typically removed. It is possible to define a specific work function at an electrode to emulate a metal-semiconductor interface if a pre-defined metal or material is not specified. Lump or distributed contact resistance can also be specified at any contact as required, and is implemented in Chapter 3, Section 3.3.2.3.3, [92].

2.4 Meshing of Structures

Meshing in finite element software defines the points at which calculations are made to determine the behaviour of the item. It is critical that the mesh itself is optimised,

particularly for 3D structures. Under meshing can result in convergence issues, but over-meshing can result in an over constrained problem that requires significant, unnecessary, computational effort. Given 3D structures are significantly larger than 2D variants, care and attention must be made in defining the mesh. At interfaces, regions where doping varies significantly and other areas of interest (e.g. the channel region on an IGBT), a much finer mesh is used compared to the bulk to ensure that the charges are properly evaluated. Typically, the mesh size gradually increases away from these regions and ultimately matches the coarser bulk regions. Figure 16 shows the typical meshing of an IGBT around the emitter and gate, showing a refinement of the mesh in these regions of interest.

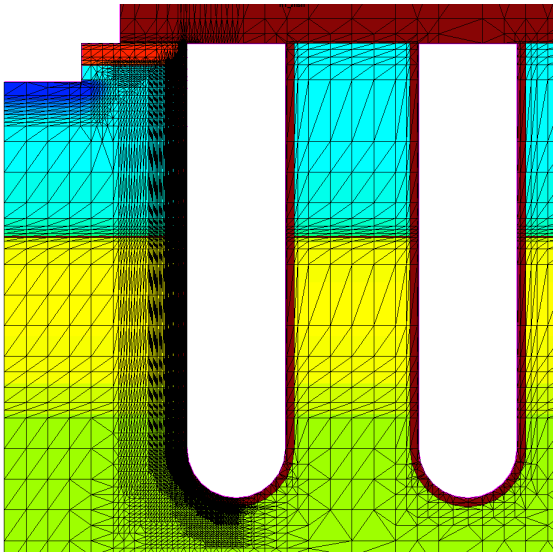


Figure 16 - Meshing structure around a trench IGBT gate and emitter; brown region oxide, red region n+ doping, dark blue region p+, light blue region p-well, yellow region n-enhancement, green region n-drift

2.5 Mixed Mode Simulations

Mixed mode simulations enable circuit simulations of one or more TCAD models alongside other components based upon compact SPICE models. Despite being computationally more demanding than a full compact circuit model, by using the TCAD model in this way, accurate results for the power device behaviour in various applications can be achieved. Lattice heating effects can also be included in these simulations (Section 2.2.4). This mode is typically used to model transient events such as turn-off behaviour and short-circuit events.

2.6 Conclusion

This chapter has outlined the relevant simulation techniques implemented in Sentaurus TCAD, for both 3D silicon power semiconductors as well as some additional considerations for SiC, a wide bandgap material. The techniques discussed in this chapter have been applied to the TCAD simulations presented in this thesis.

Chapter 3

3D Modelling of Large Area IGBTs

New IGBT designs are becoming increasingly reliant on simulation tools that enable rapid device development which, due to the cost and time associated with fabrication, could not be achieved by manufacturing prototypes. Using finite element modelling software, Sentaurus TCAD, allows the physical interactions within the device to be modelled more accurately than an equivalent compact circuit model. These simulations are computationally expensive and typically most design engineers develop TCAD models only in two dimensions. However, modern transistor designs are inherently 3D, and thus to ensure that the device performs as expected when manufactured, it is critical that models are accurate and account for the effects resulting from the 3D structure. Therefore, it was necessary to produce a fully verified 3D model which could be used to characterise and understand all device phenomena, particularly in this third dimension which has historically been overlooked.

This chapter considers a commercial Insulated Gate Bipolar Transistor (IGBT) and details the development of a 3D model using commercially sensitive data obtained from the manufacturer. It is shown that despite having all this information about the device, a single accurate model could not be produced due to processing uncertainty across the IGBT die area. Not only did this processing uncertainty, known as birds-beak, have a strong effect on the accuracy of the TCAD simulations but it had the consequential effect of reducing the reliability of the device. [1]

[1] The material in this chapter has been taken from the following publication:
E. M. Findlay and F. Udrea, "Modeling of Large Area Trench IGBTs: The Effect of Birds-Beak," IEEE Trans. Electron Devices, vol. 66, no. 6, pp. 2686–2691, 2019, doi:10.1109/TED.2019.2911020

3.1 Introduction

The trench IGBT design was first reported in 1986 [37] and demonstrated in 1989 [38] with the intention of increasing the MOS channel density and reducing latch-up susceptibility. Theoretically, a 30-40% overall loss advantage with no serious penalties in safe operating area (SOA) can be achieved [39]–[41], and advanced trench structures have been developed by numerous manufacturers [42]–[45]. However, fabrication of the trench is complex and defects such as birds-break at the top of the trench occur due to processing variations [49], [50].

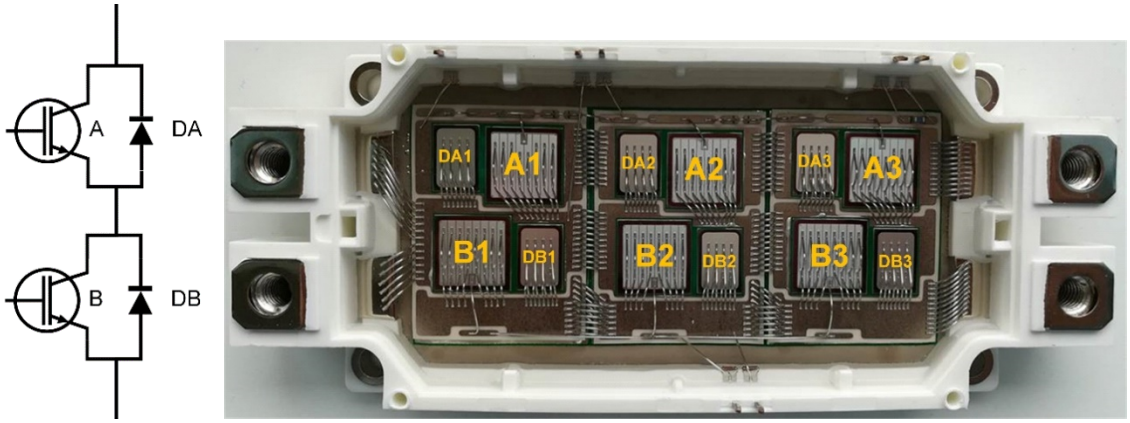
Development of new IGBT designs are becoming increasingly reliant on simulation tools, which allow for rapid device development that could not be achieved by manufacturing prototypes due to the cost and time of fabrication. However, to ensure that the device performs as expected when manufactured, it is critical that the models are accurate. Three-dimensional models enable more complex and realistic structures to be emulated and 3D modelling is becoming increasingly prevalent as processing power becomes more readily available. However, the high computational demands mean that designers are restricted to model only a very small proportion of the total device active area, which can have negative consequences. In the case of large area high power devices, processing variations across the chip can become significant, particularly for trench designs, and the simulation model becomes inaccurate as these deviations from the ideal structure are difficult to account for.

This chapter details the development a 3D Sentaurus TCAD model to simulate the behaviour of a 1.7kV 150A Trench IGBT. The effect of process variations across the chip area on the device characteristics are investigated, and simulation techniques to account for this are proposed. The practical implications on device performance as a result of these processing defects are also demonstrated and, to minimise their effects, a new n+ emitter implantation design is given.

3.2 IGBT Device Structure

Investigations were conducted using a CRRC TG450HF17M1-S300 Half Bridge IGBT module, rated for 1.7kV and 450A. The module circuit configuration is given schematically in Figure 17 (a), where 3 IGBT and 3 diode die are connected in parallel to

form a single switch (each individual die is rated to 150A). An image showing the inside of the module is given in Figure 17 (b). Given that a single IGBT die was modelled in the simulation, all currents derived experimentally were divided by three such that they became comparable with the simulation output.



(a) (b)

Figure 17 - Module layout of TG450HF17M1-S300 Half Bridge IGBT, (a) schematic connections (b) image of module connections with 6 IGBT die and 6 diodes (A1, A2, A3 forms IGBT A; DA1, DA2, DA3 form diode DA; B1, B2, B3 forms IGBT B and DB1, DB2, DB3 form diode DB as defined in (a))

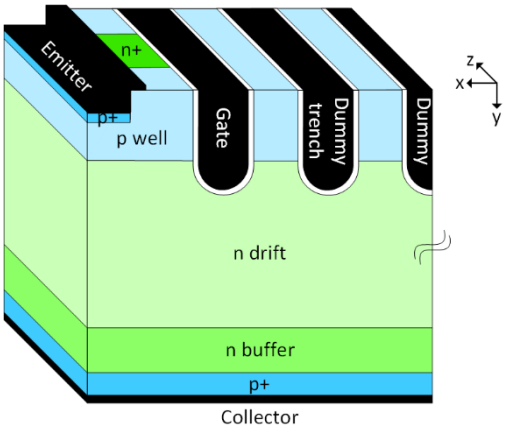


Figure 18 - Schematic of full IGBT cell simulated

Figure 18 is a schematic representation of the 3-D TCAD IGBT model developed in Sentaurus. A 3-D model was necessary since the n+ doped region under the emitter was not continuous throughout the whole depth of the device; the n+ implant alternates with regions of p-well (in z-dimension, into the page on Figure 18). This structure repeats

throughout the whole depth of the device. A 2-D variant with modified area scaling factor was explored in Section 3.4 but was found to be inaccurate.

Doping profiles were taken from commercially sensitive spreading resistance profiling (SRP) plots provided by CRRC. Due to the nature of the measurement for a SRP plot, it is not always representative of the true doping level. For example, if the probes are not correctly contacted to the bevelled surface, then there will be an error in the resistance measurement. Also, if the angle of the bevel is too steep, or the distance between the probes too wide, there will be an error in the concentration, especially as the probe nears the junction. The measurement only takes account of a very specific point on the silicon surface and does not account for variation across the profile of the implant; the effect of sintering of the aluminium on the collector contact causes a local increase in p++ doping at the contact [102] which cannot be seen in the SRP plot as the resolution is too course for this measurement. Therefore, it is important that these measurements are used as a guideline, and a small amount of adjustment is made to match the simulation device output to the experimental results. Further details are given in Section 3.3.

To minimise the simulation time, the cell structure is simplified to the smallest possible replicating cell. As such, an area scaling factor is applied to the simulation results so that the output emulates the behaviour of the whole die. To account for all fringing effects (at a n+/p-well boundary the effective channel area increases due local depletion regions), the n+ emitter implant should be located centrally and the overall cell depth (z-dimension) increased. However, by neglecting some of these fringing effects, the cell size could be reduced significantly giving the structure in Figure 19 (equivalent to 0.000166% of the device active area). By using the reduced cell size, the number of node points and therefore computational time, is reduced by 74% and 93% respectively. The penalty for using the smaller cell is the accuracy of the simulation output; the saturation current at a gate-emitter voltage (V_{ge}) of 9V is 8% higher for the larger cell in Figure 18 compared to the result using the Figure 19 structure . This discrepancy in the real channel length due to the additional fringing effects can be accounted for by increasing the area factor of the smaller model. Therefore, the benefit of faster simulations offsets this slight reduction in accuracy and thus the simulations conducted in the remainder of this chapter use the smaller model as shown in Figure 19.

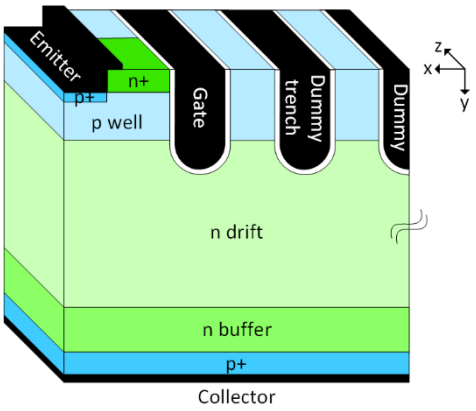


Figure 19 - Schematic IGBT cell simulated with reduction in the size in z-dimension

The parameter file for silicon used default values provided by Sentaurus. Both simulation and experimental measurements were conducted at 298K, unless otherwise stated, and were measured in accordance with the IEC standard [87].

3.3 Development of 3D Simulation Model

Development of an accurate model, validated by the experimental data, was achieved through an iterative process as illustrated in the flowchart given in Figure 20. Further details about each measurement is given in the subsequent sections.

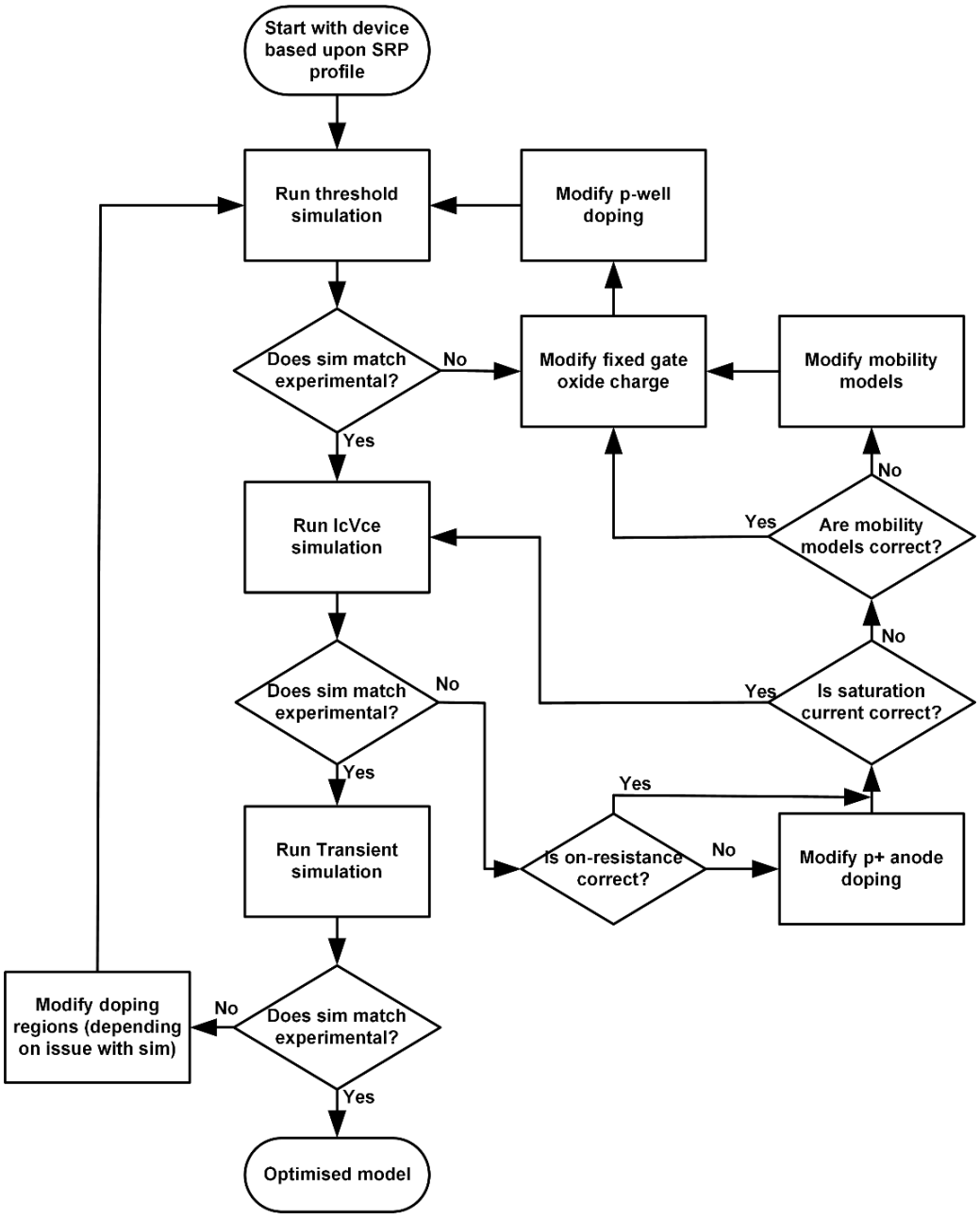


Figure 20 - Flowchart of model validation process

3.3.1 IGBT Threshold Measurement

Threshold measurements were taken in accordance with the IEC standard and in line with the conditions outlined on the CRRC datasheet [87], [103]. The test circuit is shown in Figure 21, and threshold is achieved when the collector current for the module is 15mA, therefore per cell it is 5mA.

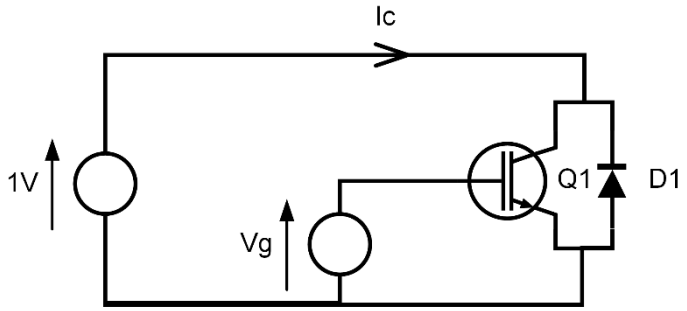
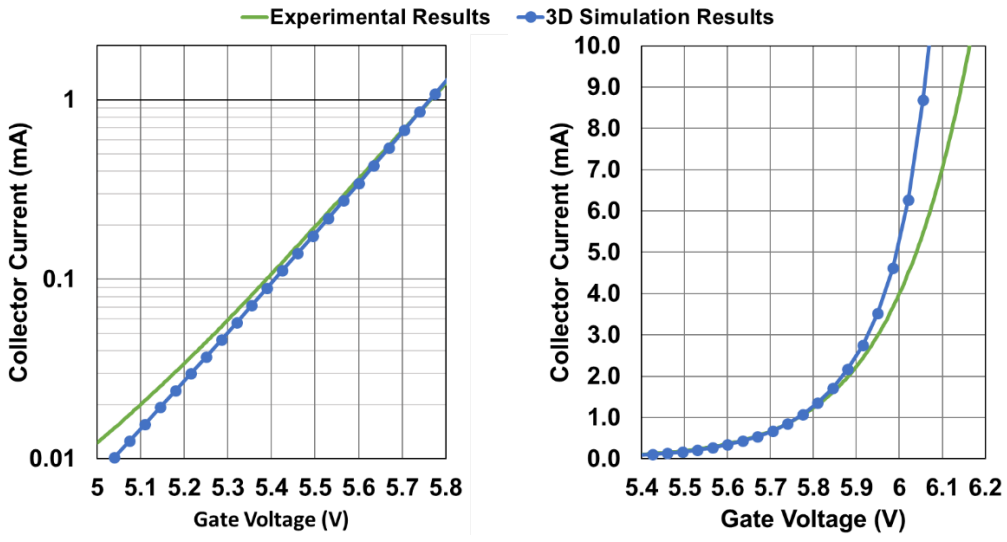


Figure 21 - Schematic of threshold measurement test circuit [87]

To match the threshold voltage, the p-well doping by the gate is adjusted along with the fixed charge within the gate oxide. Increasing the p-well doping increases the threshold voltage, whereas increasing the fixed gate oxide charge decreases the threshold. To be physically realistic of a typical device, the fixed charge within the oxide should be within the range 1e10cm^{-3} and 3e11cm^{-3}. For the results in Figure 22, the peak p-well doping is set to 2.39e17 cm^{-3} and the gate oxide is fixed at 8.25e10cm^{-3}. Both numbers can be adjusted at the designer's discretion, and their relationship for a fixed threshold voltage is illustrated in Figure 23. Note that Figure 23 uses p-well doping value at the n+/p-well interface, not the peak p-well doping as discussed for Figure 22.



(a) (b)

Figure 22 - Gate threshold measurement of original 3D model, Collector-Emitter Voltage (V_{ce})=1V, ambient temperature 298K (a) sub-threshold (b) at threshold, experimental V_{th}=6.04V, simulation V_{th}=5.99V at I_c=5mA

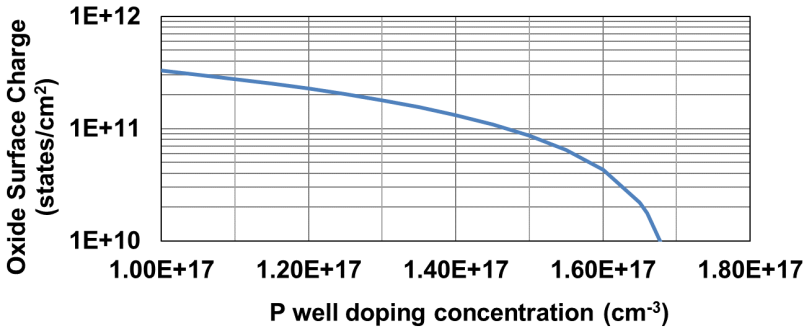


Figure 23 - Dependence of gate oxide charge on p-well doping for fixed threshold voltage (V_{th} = 6.1V)

The simulation results in Figure 22 have excellent matching at the sub-threshold level (Figure 22 (a)), with the curve diverging at higher currents (Figure 22 (b)).

A few conclusions can be inferred from the results;

- In the simulation the injection of carriers is too high as the gate voltage increases. 10mA through the device corresponds approximately to 8mA/cm^2 where the excess charge in the device is lower than the n-drift doping. Therefore, at this low collector current, this discrepancy cannot be attributed to the IGBT pnp transistor gain; removing the p+ emitter (to produce a MOSFET) still exhibits too high an injection as shown in Figure 24.
- The divergence at higher gate voltages suggests that the mobility of the majority carriers within the channel is slightly high and may need to be reduced for future simulations.

Although the simulation model did not match the experimental data exactly, there was sufficient agreement to justify running further simulations.

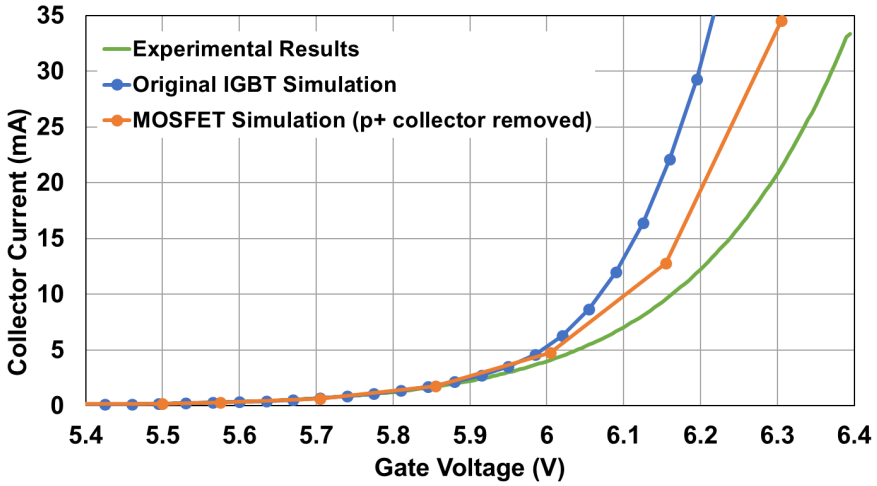


Figure 24 - Gate threshold measurement of original 3D model and equivalent MOSFET structure highlighting the effect of hole injection from anode, Collector-Emitter Voltage (V_{ce})=1V, ambient temperature 298K

3.3.2 IGBT On-State Characteristics

The IGBT output characteristics (I_c V_{ce} curve) were run for several gate voltages, in line with those specified on the datasheet so that both the simulation and experimentally gathered results could be directly compared to the manufacturer's expectations. Again, the measurement was taken in accordance with the IEC standard [87]. The test circuit is shown in Figure 25, with the collector and gate continually pulsed to ensure there were minimal self-heating effects within the device. A small gate resistor (not shown) was attached to provide stability. The measurement was recorded when the gate was fully charged and the collector current stable.

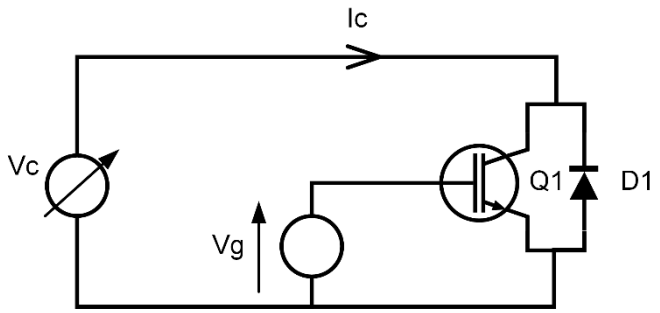


Figure 25 - Schematic of IGBT output characteristic measurement test circuit [87]

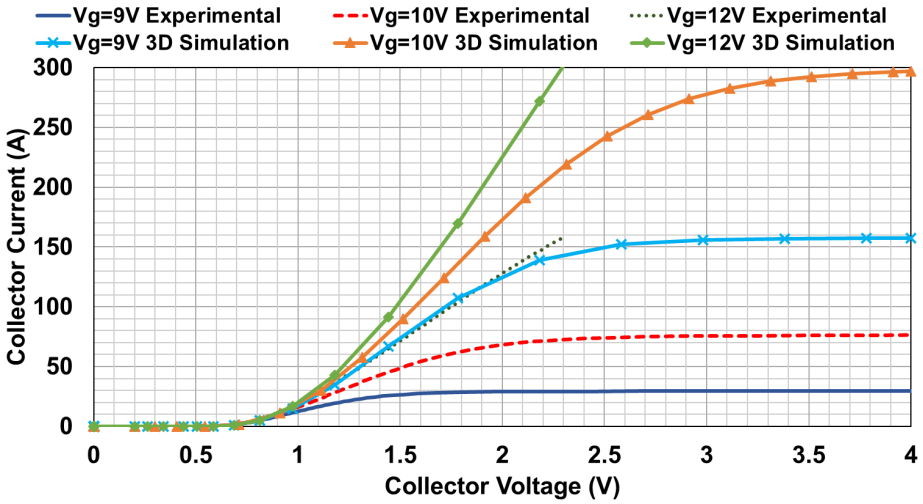


Figure 26 - On-state characteristics, original 3D model using default silicon parameter file as defined by Sentaurus, ambient temperature 298K

Using the device model in Section 3.3.1, the IGBT output characteristic is shown in Figure 26. The simulated device shows very poor on-state matching, both in terms of the gradient of the IcVce curve in the linear region and the saturation current; the saturation current exceeds the experimental results by over 5 times at Vg = 9V.

The saturation current ($I_{C(sat)}$) can be defined as;

$$I_{c(sat)} = \frac{\mu_{ni} C_{ox} Z}{2L_{ch}(1-\alpha_{pnp})}(V_g - V_{th})^2$$

Equation 9 - Saturation collector current, where L_{ch} is the channel length, μ_{ni} is the inversion layer mobility, α_{pnp} is the gain of the pnp structure within the IGBT, C_{ox} is the specific capacitance of the gate oxide, Z is the length of the IGBT in the z-plane (into the page on Figure 18) , V_g is the gate voltage bias and V_{th} the threshold voltage. [1]

Looking at each variable in turn;

- Typically, α_{pnp} can be expected to vary between 0.15 to 0.4, with the most common values being in the range 0.2-0.3. Therefore, the bipolar action of the IGBT $[(1-\alpha_{pnp})^{-1}]$ increases the saturation current for a given gate voltage by a factor of 1.6 compared to a MOSFET of the same geometry. Consequently, the discrepancy in Figure 26 cannot be attributed to the hole injection efficiency alone. Note: α_{pnp} has been defined as $I_{emitter} = I_{electron} + I_{hole}$ where $I_{electron} = I_{emitter}(1- \alpha_{pnp})$ and $I_{hole} = I_{emitter}\alpha_{pnp}$

- Threshold voltage is in line with the experimental results as determined in Section 3.3.1 and shows acceptable agreement.
- The experimental measurement was taken in a quasistationary state such that there was no gate current when the collector current was recorded and therefore there cannot be an error in the recorded gate voltage.
- Both Z and L_{ch}, which are dependent solely on the device geometry, were known to be correct in this instance given that the device dimensions and layout had been provided by CRRC (the area scaling factor can account for, at most, a 15% discrepancy which is insufficient to account for this error, nor does the shape of the I_c V_{ce} trace indicate a simple scaling issue).

The two remaining variables, the gate oxide capacitance and the mobility of the inversion layer, were investigated in turn to determine their influence on the saturation current.

3.3.2.1 Gate Oxide Capacitance

The gate oxide capacitance is fixed by the material (silicon dioxide), the geometry and the thickness of the gate oxide trench. In recent years there have been improvements in the processing of trench devices and therefore it is not unreasonable to assume that the oxide thickness is uniform down the length of the trench. The manufacturer stated that the gate oxide thickness was 0.11µm, but there may be some small variations. Therefore, the effect of the oxide capacitance was investigated numerically using Equation 9 by uniformly changing the thickness of the oxide down the length of the trench. At a thickness of 0.11µm (at value 1 on Figure 27 x-axis) the change in saturation current for small variations in thickness is minimal; increasing the thickness by 0.01µm only decreases the saturation current by 9%, partly due to the dependence of the gate oxide capacitance on the device threshold voltage.

It was therefore concluded that the global thickness of the gate oxide capacitance was not the principle source of the simulation error.

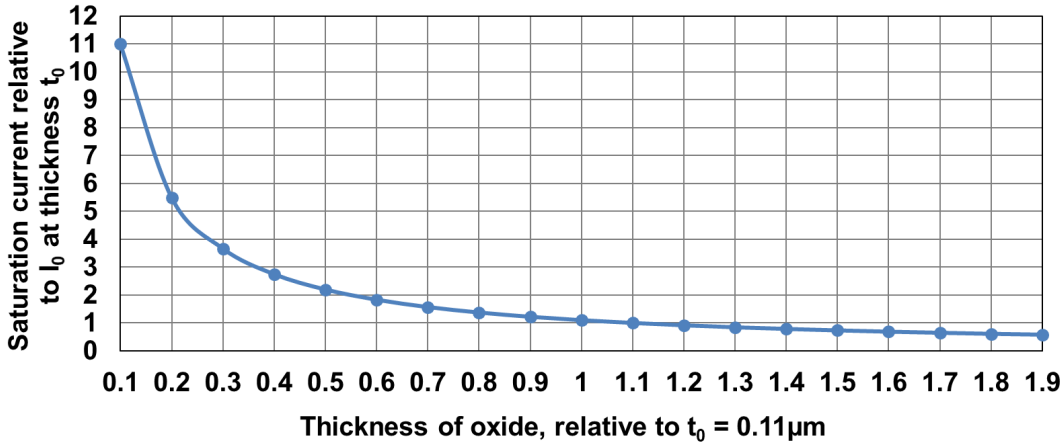


Figure 27 - Relationship between saturation current and the thickness of gate oxide measured relative to values at oxide thickness 0.11µm, for fixed n+/p-well doping, ambient temperature 298K

3.3.2.2 Mobility of Carriers

Mobility models were modified, particularly since the threshold measurement indicated that the mobility of majority carriers within the channel was slightly high.

The High Field Saturation model (when the drift velocity of carriers is no longer proportional to the electric field) was instead calculated parallel to the semiconductor–insulator interface, which has been shown to be a more accurate model to represent the MOSFET channel behaviour [92]. The old model for Slotboom bandgap narrowing was also used since it has been shown to be more physically realistic [98]. In addition, specific silicon parameter values based upon crystallographic lattice orientations were used, rather than the default Sentaurus general silicon values. These more specific silicon values were taken from the standard Sentaurus parameter file which have been experimentally determined and validated by Sentaurus. Given the wealth of research conducted into silicon, it is reasonable to expect that these values are accurate. These values are given in Appendix A.1.

The effect of these modifications can be seen in Figure 28 where using these models resulted in a 43% reduction in saturation current compared to the results in Figure 26. The gradient of the I_cV_{ce} curve in the linear region, particularly at higher gate voltages, also had much improved matching to the experimental results. However, the saturation current still exceeded the experimental values by over 200% (V_g = 9V) and, particularly at lower

gate voltages, the collector current-collector voltage trace shape still differed significantly from the experimental results.

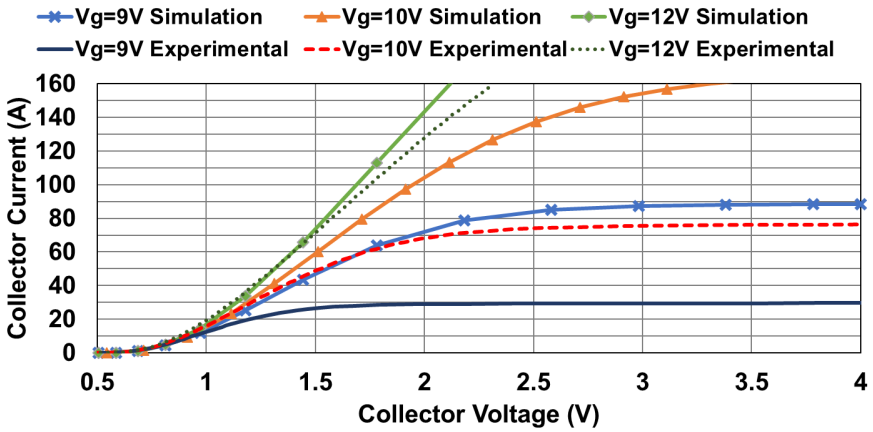


Figure 28 - On-state characteristics, using 3D model with optimised physical models, ambient temperature 298K

3.3.2.3 Further Considerations

Various other aspects of the IGBT geometry and behaviour were investigated to determine if they were the cause of the errors in the simulation model. These have been explained in more detail in the sections below.

3.3.2.3.1 Emitter Shorting Dummy p-well Connections

The effect of emitter shorting the dummy p-well regions (p-well adjacent to the dummy trenches in Figure 19) was also considered, which in previous simulations had been left floating as CRRC maintained that there were no connections. These dummy p-well regions provide a secondary avenue for hole extraction and therefore reduce the number of electrons injected at the emitter and hence reduce plasma formation at the top of the device. Figure 29 shows that this emitter shorted device has a 34% decrease in the gradient of the I_cV_{ce} curve in the linear region compared an equivalent device with floating dummy p-well regions, but the saturation current remains unchanged. This therefore provides further evidence that the MOSFET channel is dominating the error in the saturation current shown in Figure 28.

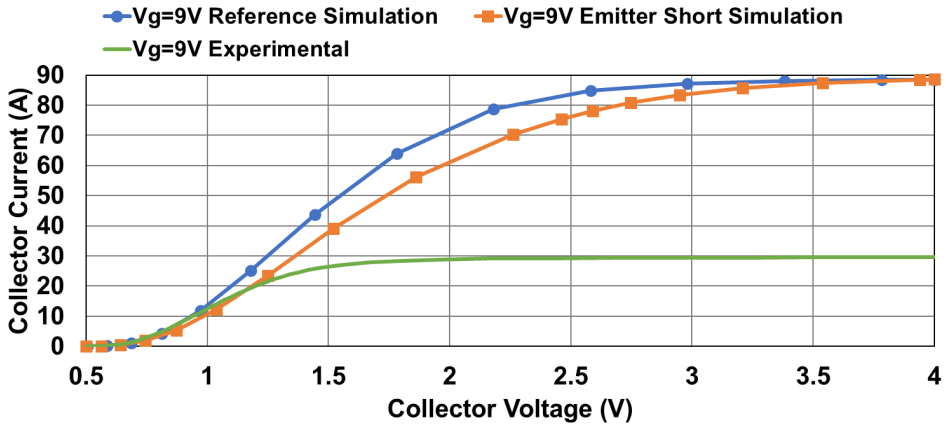


Figure 29 - On-state characteristics comparing 3D model with optimised physical models and dummy p-well regions either floating or emitter shorted, ambient temperature 298K

3.3.2.3.2 Self-Heating Effects

Self-heating effects were also considered using the thermode command within Sentaurus as significant self-heating in the channel region would reduce mobility and therefore reduce the saturation current. Simulations were conducted assuming only the backside of the wafer provided an avenue for thermal extraction (the thermal resistance of this contact was derived from the device datasheet). There are, however, competing effects within the device as the threshold voltage decreases with temperature and saturation current is proportional to $(V_g - V_{th})^2$ as shown in Equation 9. Overall, the saturation current only increased by 0.5% compared to the non-thermal model. Although this is more realistic of the device conditions, to include lattice heating the computational time increased by over 5 times. Therefore, self-heating effects were not considered in subsequent simulations of on-state or transient switching behaviour.

3.3.2.3.3 Parasitic Resistance

Modules have a series parasitic resistance caused by bond wires and connections which can result in the applied gate emitter voltage across the device contact not being equal to that made at the external module connections. This parasitic resistance is shown schematically in Figure 30. Either all the resistance can be modelled on the emitter (Figure 30 (a), denoted model A) or it can be distributed with the collector (Figure 30 (b), denoted model B), but the former has the greatest impact on the gate-emitter voltage.

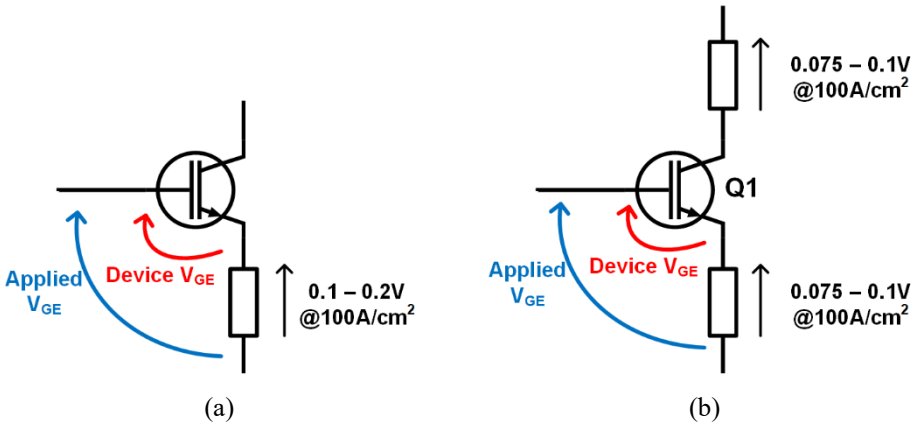


Figure 30 - Schematic showing parasitic impedances that typically present on an IGBT module with a) all distributed resistance shown on the emitter and b) resistance distributed between collector and emitter

The modelled IGBT has a total active area of 1.305cm^2, which equates to a series resistance of between 0.767mΩ and 1.534mΩ for the parasitic impedance in model A. A 1.534mΩ resistance in series with the emitter was introduced to the model and the effect on the simulated characteristics is shown in Figure 31 and Figure 32. Although there is an improvement in the gate threshold characteristic, the collector current-voltage waveform is still a poor match.

Investigations were conducted into the effect of increasing the emitter resistance further, but it was found to distort the overall shape of the waveform, such that matching the experimental results was untenable.

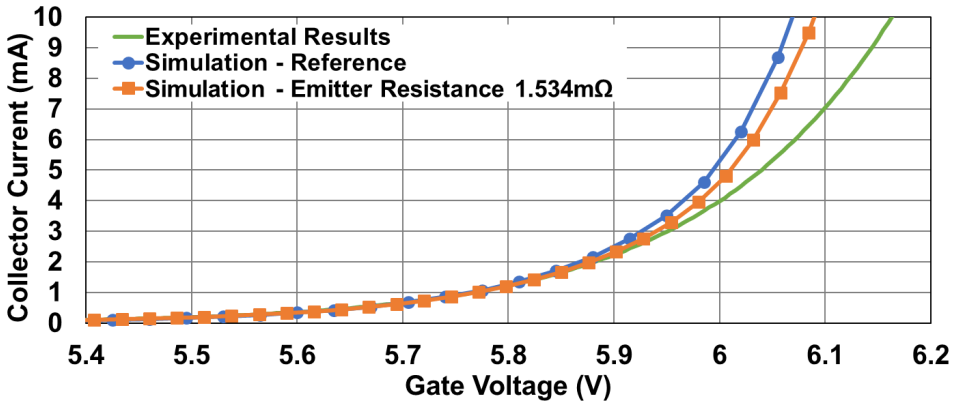


Figure 31 - Gate threshold measurement comparing original 3D model with optimised physical models with and without a 1.534mΩ resistance connected to the emitter, Collector-Emitter Voltage (V_{ce})=1V, ambient temperature 298K

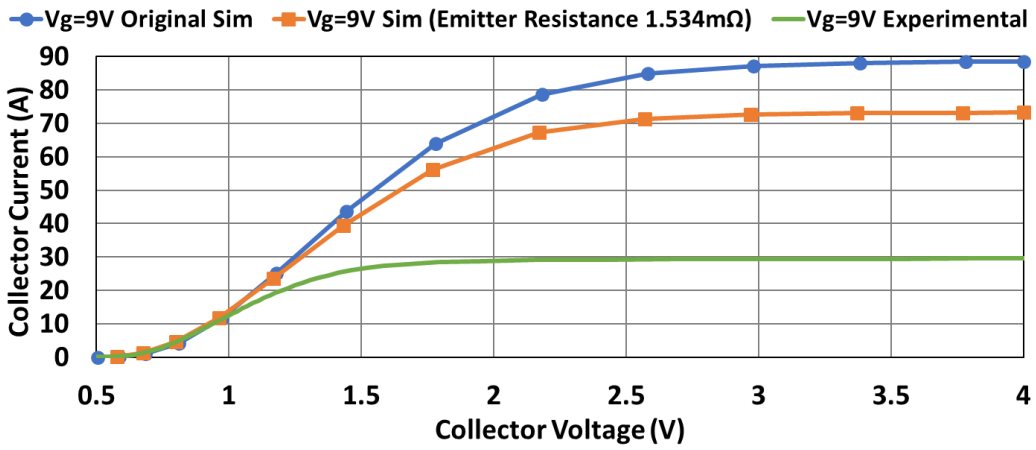


Figure 32 - On-state characteristics comparing original 3D model with optimised physical models with and without a 1.534mΩ resistance, ambient temperature 298K

3.3.2.4 Determining the Source of the Error

It has been the assumption thus far, due to the matching work as detailed in Section 3.3.1, that the threshold of the simulation was correct and therefore the error must exist in the multiplying terms of Equation 9. However, having considered the value of each of these other parameters, it now seems unlikely that these are the cause of the issue. Further experimental data was therefore taken to plot the relationship between saturation current and gate voltage. The experimental procedure was identical to that used in Figure 21, except that the collector voltage was increased to 4V to ensure the device was in saturation.

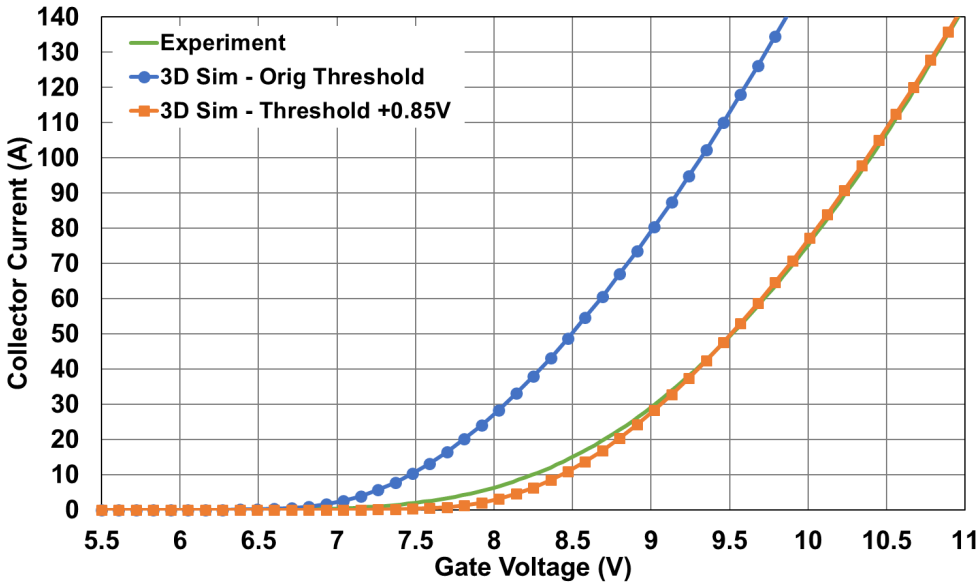


Figure 33 - Saturation current for increasing gate voltage comparing original 3D model with optimised physical models and the same model with the threshold voltage increased by 0.85V, V_{ce}=4V, ambient temperature 298K

Figure 33 shows the relationship between saturation current and gate voltage of the device, using the modified mobility model as detailed in Section 3.3.2.2. The overall shape of the curve for the 3D simulation results matches the experimental curve well, which indicates that the multiplying terms of Equation 9 are correct, however, the simulated results are 0.85V too close to the y axis. Consequently, it can be concluded that either the applied gate voltage or the device threshold in the simulation model is incorrect. Since the measurement was taken at zero gate current, the discrepancy is therefore with the device threshold voltage. Increasing the threshold voltage of the simulated device by 0.85V (by increasing the p-well doping) produces the on-state characteristics shown in Figure 34, with Figure 35 providing a zoomed in view at turn on. This simplistic modification to the simulation model results in good matching for large currents, however it is physically unrealistic as the simulation model turns on at a much higher gate voltage than experimental results have shown, so further investigation was required.

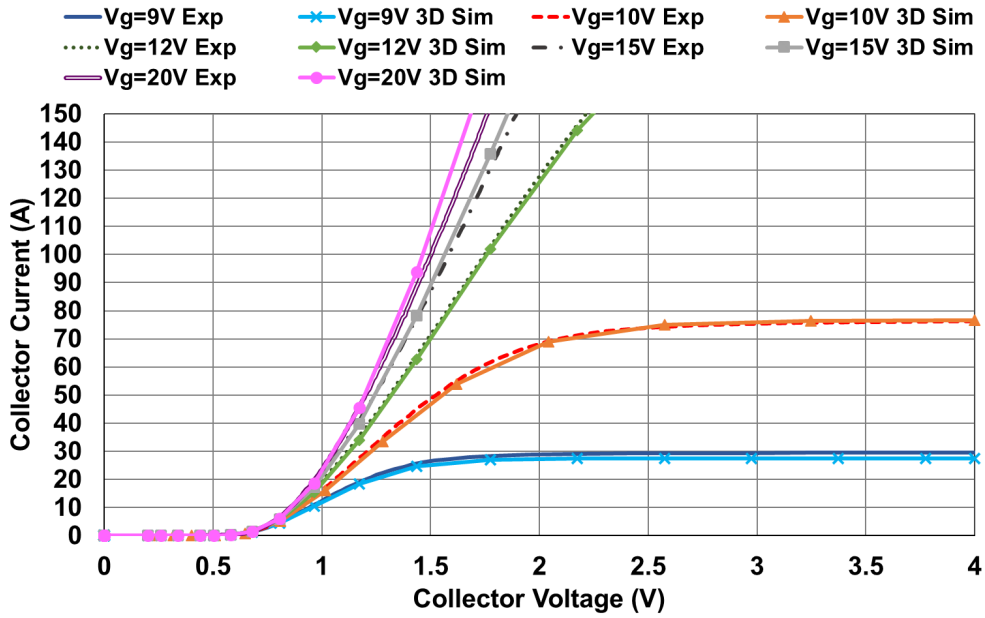


Figure 34 - On-state characteristics of 3D simulation model with optimised physical models and threshold voltage increased by 0.85V, ambient temperature 298K

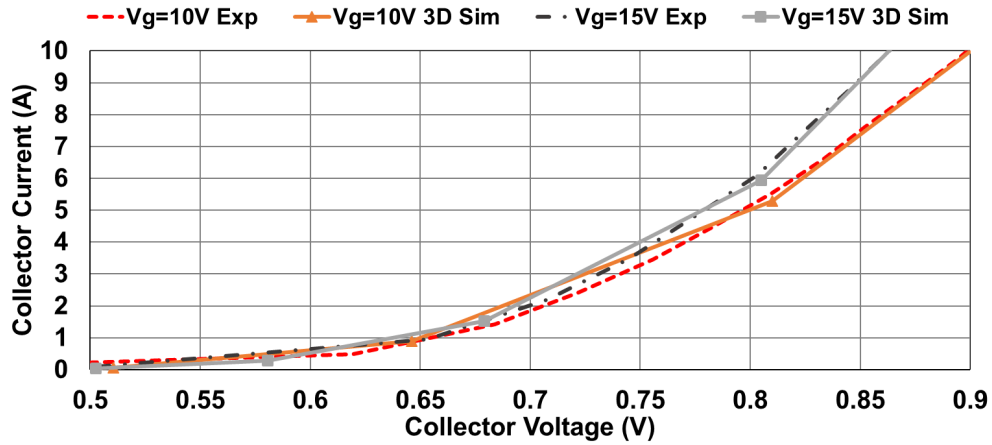


Figure 35 - Zoom of on-state characteristics at the point of turn-on for 3D simulation model with optimised physical models and threshold voltage increased by 0.85V, ambient temperature 298K

3.4 2D Simulation v 3D Simulation

A 2D simulation model, using the same doping, gate charge and mobility models was also run for comparison. Despite matching the gate threshold (Figure 36), the 2D model still suffers from the same voltage offset as seen for the 3D model (Figure 37), providing further evidence that this offset is not a modelling issue. As a result, the threshold voltage of the 2D model also needs to be increased by 0.85V for the on-state current to match. Figure 37 also shows that, for the 2D model, the gradient of the curve is too steep; the 2D

model does not account for fringing effects at the n+/p-well boundary along the gate and therefore an error in Z is expected. The 3D simulation output shows that fringing increases the length of the IGBT channel in the z plane by 2.5%, which, if included in the 2D model, would increase the saturation current further. As it stands, there is a 35% discrepancy between the gradient of the 2D results and the experimental curve, which therefore indicates that this is not caused by fringing effects alone and that the 2D model does not fully account for the carrier mobility nor the gain of the bipolar element of the IGBT.

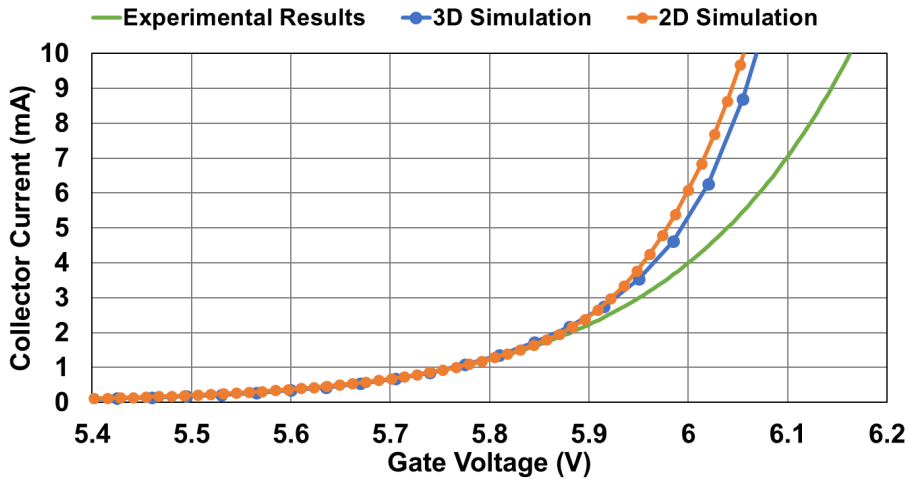


Figure 36 - Gate threshold measurement comparing 3D and 2D model using same physical models, Collector-Emitter Voltage (Vce)=1V, ambient temperature 298K

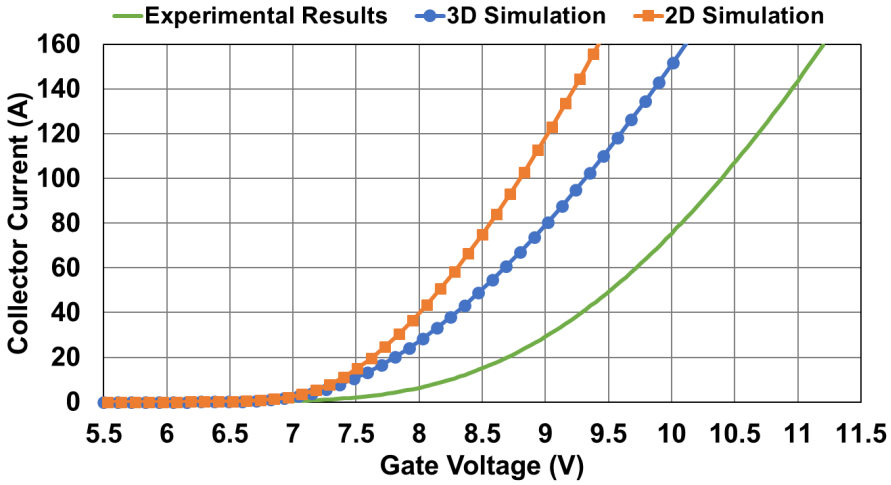


Figure 37 - Saturation current for increasing gate voltage comparing original 3D model with optimised physical models and the equivalent 2D model, V_{ce}=4V, ambient temperature 298K

Improved matching could be achieved for the 2D model by replacing the Philips unified mobility model used in the 3D simulation with the doping dependent Masetti model. Both

models account for doping-dependent scattering in the device, but the Philips unified mobility model also accounts for other effects such as electron-hole scattering [92]. Implementing this more simplistic Masetti model in the 2D simulation results in the saturation current having only a 2.5% error in the on-state, which can be attributed to the unaccounted fringing effects, and overall, it has a good on-state curve matching (Figure 38).

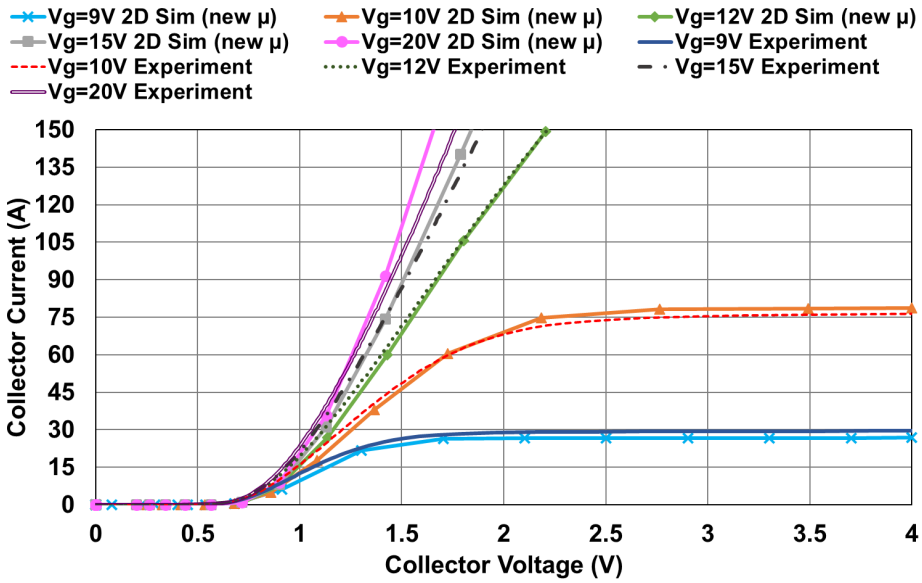
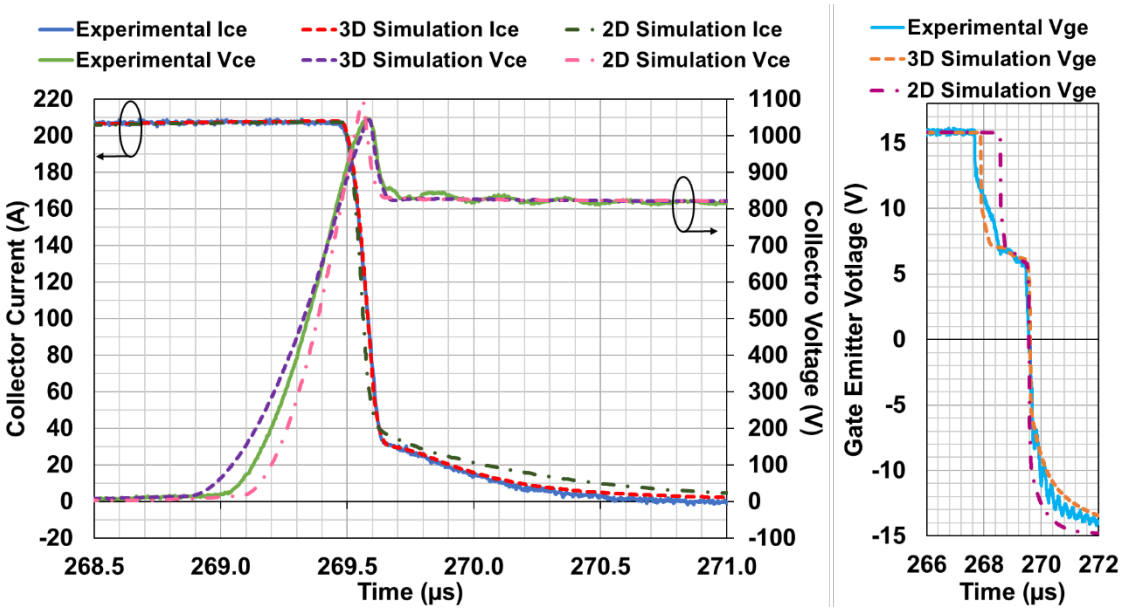


Figure 38 - On-state characteristics of 2D simulation model with doping dependent Masetti model and threshold voltage increased by 0.85V, ambient temperature 298K

Yet despite this improvement in the on-state matching, the transient simulation is a relatively poor match. Details about the inductive load turn-off measurement can be found in Section 3.5.1. When a transient simulation is run with the same conditions, the 2D simulation with the Masetti doping dependent mobility has too large a tail current compared to both the 3D model and the experimental data, indicating that plasma formation within the 2D device model is too high. The gate charge is also much reduced resulting in a significantly shorter Miller plateau time (39% reduction compared to the equivalent 3D model), signifying that the gate-collector Miller capacitance is too low in the case of the 2D model. By reintroducing the Philips unified mobility model improvements in the transient output are seen (shown in Figure 39), however the 2D model output is still a significantly worse match to the experimental data compared to the 3D output. Given that the 2D model cannot provide consistent matching for all of the

measurements for a specific set of mobility models, it demonstrates the need for a 3D model in this instance. The 2D model (excluding fringing effects) assumes that all holes are extracted via the p+ under the emitter contact, but the 3D model accounts for a small amount of hole extraction via the p-well emitter contact (behind n+ region in z plane). This three-dimensional effect impacts the behaviour of the device and, as a result, a full 3D IGBT model is required to accurately model the device behaviour.



(a) (b)

Figure 39 - Transient measurement comparing simulation results with both models' threshold voltage increased by 0.85V: 2D with doping dependent Masetti model and 3D model from section 3.3, ambient temperature 298K (a) collector-emitter voltage and current (b) gate-emitter voltage

3.5 Effect of Processing Errors: Birds-Beak Effect

Using the relationship in Equation 9, for a threshold voltage of 6.04V (collector current 5mA, in agreement with CRRC datasheet values) and the other defined device parameters, the theoretical saturation currents are significantly higher than the experimentally measured values. Therefore, to explain this behaviour, it is proposed that a processing defect across the chip area results in a small proportion of the IGBT active area having a threshold voltage of 6.04V and the remainder of the device's active area having a higher threshold voltage. The proportion of the chip area that turns on at the higher gate voltages dominates the large current measurements and thus the theoretical relationship described in Equation 9 is still observed.

The most likely cause of this threshold variation across the device is a birds-beak effect. Bird-beaking is a defect within trench formation that is difficult to control during device processing. The deep trench oxide structure of this device is prone to the bird-beak effect as the oxide width does not remain constant due to processing variations [49], [50]. The device used for this investigation also has an arsenic implanted n+ source: arsenic implants are much more highly doped compared to phosphorous, resulting in a shallower implant, but lower contact resistance, which is beneficial for the on-state performance. Typically, birds-beaking can be neglected as it is assumed that the oxide width is constant over the depth of the implant; but the combination of trench technology, shallow arsenic implants and large device area brings this effect into consideration.

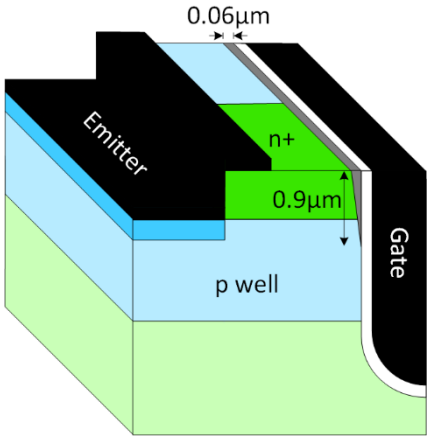


Figure 40 - Zoom of 3D TCAD model of the gate with bird-breaking (highlighted in grey)

To test this hypothesis, a new simulation model was developed to account for this birds-beak effect, as shown in Figure 40. It is likely that a range of birds-beak sizes will be present across the chip area following a normal distribution, however, to reduce the computational effort, the device was modelled as two 3D structures in parallel: one 3D model (as shown in Figure 19) which turns on at 6.04V (collector current 5mA) and represents 8% of the total active area, and the remaining active area by a 3D model which has a birds-beak applied at the channel (Figure 40). The applied bird beak is modelled as a triangular structure which extends 0.06µm in the channel and is 0.9µm deep. The threshold of the birds-beak model is set at 6.62V (collector current 5mA).

Figure 41 shows the threshold measurement from the dual birds-beak 3D model, which now has good agreement with the experimental results, compared to the original 3D

model shown in Figure 22. This threshold measurement is dominated by the behaviour of the 8% (non-birds-beak) device area model cell and the reduced active area turning on at this gate voltage diminishes the number of injected carriers, resulting in good matching to the experimental data. Figure 42 shows the on-state characteristics which are dominated by the behaviour of the birds-beak model cell. These are slightly worse than those provided in Figure 34, but are still in good agreement (4.4% error in the saturation current at Vg=10V). Introducing the birds-beak structure does significantly reduce the saturation current but the device on-resistance increases as the injection efficiency for the channel worsens. Increasing the IGBT pnp transistor gain (by slightly increasing the p+ collector doping) can counteract this without affecting the saturation current but results in too large a tail current during turn-off. The simulation model could be made more accurate by modelling a range of birds-beaks structures to account for more of the process variation across the chip area, however, the computational effort would be significant.

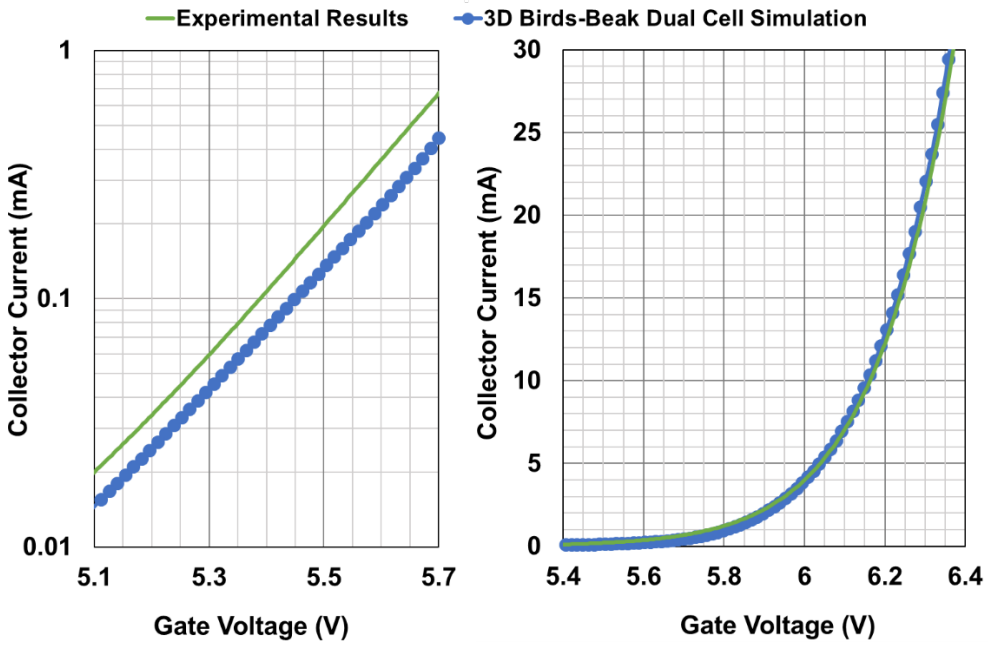


Figure 41 - Gate threshold measurement of the dual device 3Dmodel with birds-beak, Collector-Emitter Voltage (V_{ce})=1V, ambient temperature 298K (a) sub-threshold (b) at threshold, experimental V_{th}=6.04V, simulation V_{th}=6.04V at I_c=5mA

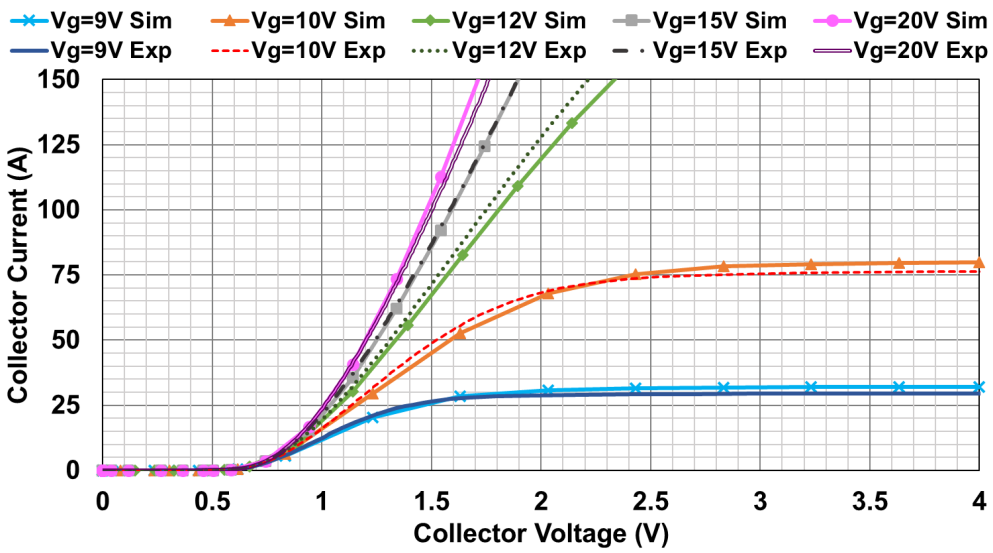


Figure 42 - On-state characteristics of dual device 3D model with birds-beak, ambient temperature 298K

3.5.1 Inductive load turn-off of dual 3D model

The IGBT switching characteristics were measured experimentally and compared to the output from the birds-beak dual model simulation output, using an inductive load as shown in Figure 43. Only turn-off was considered as the turn-on of the IGBT waveform is characterised by the reverse recovery of the diode (across the load inductor L) which was not included in the simulation model. The gate resistance Rg includes the on-chip resistance. In this simulation and experimental measurements L=455µH and Ls=120nH.

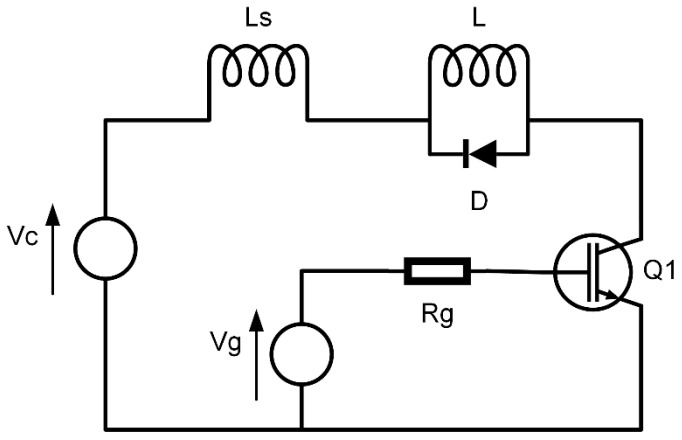
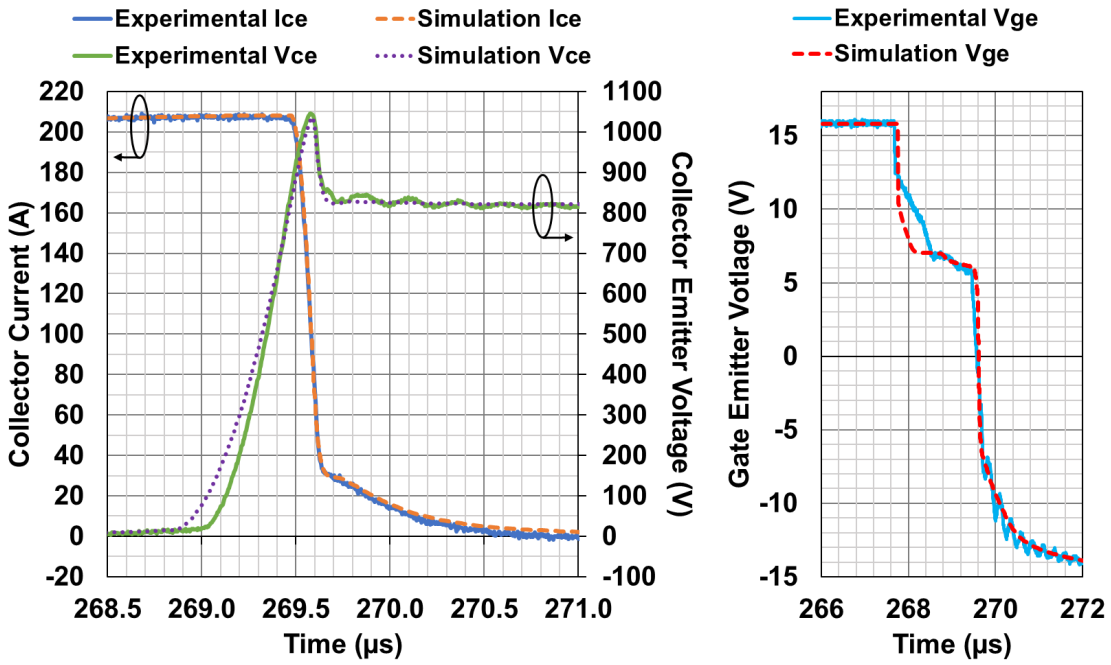


Figure 43 - Schematic of IGBT inductive load transient test circuit [87]



(a) (b)

Figure 44 - Transient measurement of dual device 3D model with birds-beak, ambient temperature 298K (a) collector-emitter voltage and current (b) gate-emitter voltage

The dual 3D simulation model and the experimental results at turn-off are particularly well matched. Figure 44 (a) shows that the collector current and voltage traces have excellent agreement, with the tail current in particular being very well matched. The collector-emitter voltage trace indicates that C_{gc} is slightly high in the simulation model since the voltage increases a little earlier than the real device, however this model does not account for all the parasitics within the module (such as the effect of bond wires, busbars etc.), which would lower the C_{gc} value if included. The tail current matches particularly well, which signifies that the plasma formation within the IGBT is correct.

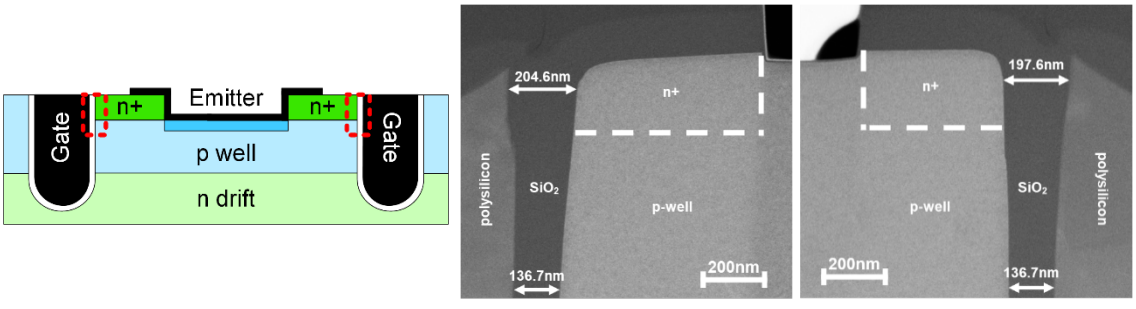
The gate-emitter voltage trace shown in Figure 44 (b) has a well-matched Miller plateau voltage (equivalent to the device threshold voltage at this specific collector current) indicating that the saturation current of this model accurately replicates the real device. Prior to the Miller plateau, the initial fall of the gate voltage is slightly delayed and much faster than the shallower trace measured experimentally. The time taken for the device gate voltage to fall rapidly is dependent upon C_{ge}, and to a certain extent C_{gc} and V_{ce}. V_{ce} must reach the line voltage before the gate voltage can fall, but the dV_{ce}/dt from Figure 44 (a) matches well so this effect is minor compared to the difference in C_{ge}. This therefore indicates that C_{ge} is too low in the simulation model compared to the real device,

which is again indicative of only modelling the active area of the cells and not accounting for additional parasitics such as the effect of the busbar. In particular, the gate busbar adds in extra capacitance which would take longer to discharge before the threshold voltage is reached and the gate regains control of the current. Despite this, the turn-off plots demonstrate that this dual cell modelling technique is a reliable method for a device designer to use.

3.5.2 Imaging of the Birds-Beak Structure

To confirm the presence of birds-beak, the emitter region was observed in cross-section by high angle annular dark field scanning transmission electron microscopy (HAADF-STEM) in a FEI Tecnai Osiris microscope operated at 200kV. The sample was prepared by focused ion beam. The images in Figure 45 show two adjacent gate trenches either side of the emitter contact. Not only is birds-beaking present in the sample, but the amount of birds-beaking varies significantly between the two trenches. For this device, the n+ emitter implantation extends ~0.25µm into the silicon area, which coincides with the thicker oxide regions in the images. The increase in thickness of the oxide is also in line with that included in the simulation model with birds-beak, which is directly compared in Figure 46. There is a normal distribution of birds-beak sizes across the device area, which can be simplified to a single 'average' birds-beak size. The size of birds-beak used for this simulation model was determined empirically.

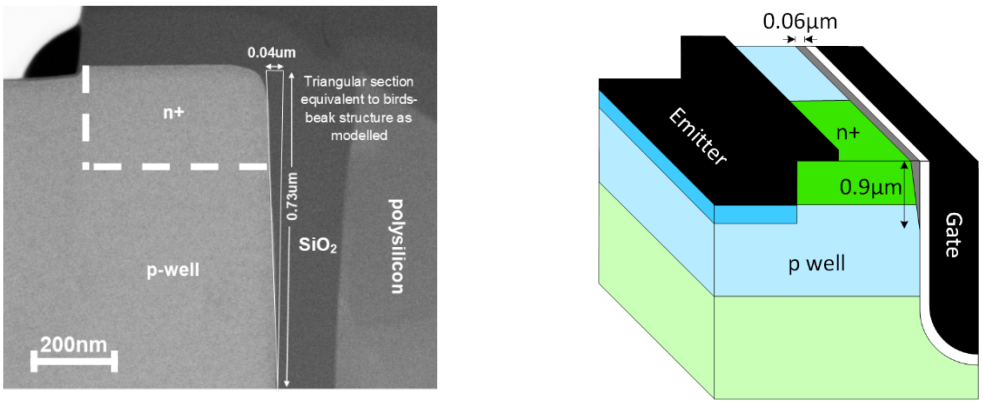
These images confirm that birds-beak is the cause of the threshold variation seen in the device behaviour.



(a) (b) (c)

Figure 45 - Cross-sectional HAADF-STEM images of the gate regions showing the presence of birds-beak; (b) and (c) are taken from the regions indicated by the rectangles in the schematic image in (a) [1].

[1] Acknowledgement is made to Dr F. C-P. Massabuau from the Material Science Department, University of Cambridge for his assistance taking the HAADF-STEM images



(a) (b)

Figure 46 - (a) Cross-sectional HAADF-STEM images of the gate region showing the dimensions of a single birds-beak as imaged (b) 3D TCAD model with bird-beaking (highlighted in grey) as shown in Figure 40.

3.5.3 Implications of Birds-Beak Structure on Device Performance

The effect of the birds-beak on the device short circuit endurance time was investigated using the dual threshold model developed in Section 3.5. The short circuit simulation followed the IEC standard using the circuit schematic shown in Figure 47 [87]. The gate resistance Rg includes the on-chip resistance. In this simulation Ls=100nH.

Self-heating effects were included in this simulation assuming only the backside of the wafer provided an avenue for thermal extraction; a heat loss of 0.6K/W was included at the collector in accordance with the manufacturer's recommended heatsink (0.2K/W thermal resistance of junction to module package, 0.1K/W thermal resistance module package to heatsink, 0.3K/W thermal resistance of heatsink).

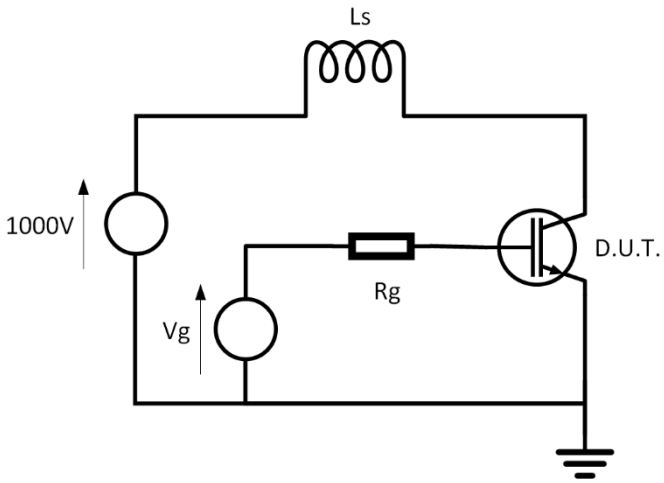


Figure 47 - Schematic of IGBT inductive load transient test circuit [87]

Model Description	Endurance Time
Single model (birds-beak higher threshold cell only)	26.02µs
Dual model (non-birds-beak lower threshold 8% active area, paralleled with birds-beak cell)	21.36µs
Dual model (non-birds-beak and birds-beak in same silicon bulk, 16% active area, paralleled with birds-beak cell)	17.71µs

Table 2 - Summary of endurance time for 3D simulations models including lattice heating and heatsink at collector (heat loss of 0.6K/W)

A summary of the simulation results is given in Table 2. Under short circuit conditions the dual 3D model exhibits an endurance time of 21.36µs; the current density of the lower threshold model (non-birds beak cell with 8% active area) is 0.179mA/cm^2 and the higher threshold model (birds-beak applied) is 0.143mA/cm^2. As a result, thermal breakdown occurs in the region with the lower threshold due to this higher current density. When the birds-beak is applied across the whole of the device active area, the endurance time increases by 21.8%. Therefore, it can be concluded that the lower threshold regions are causing local hotspot formation across the chip area, which will reduce reliability and ultimately cause premature failure of the device.

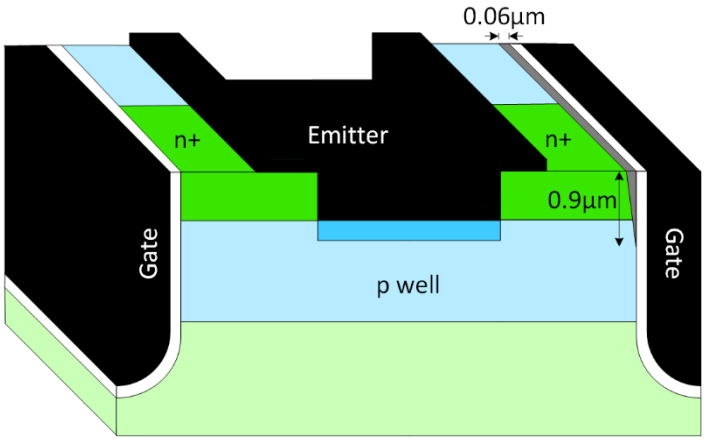


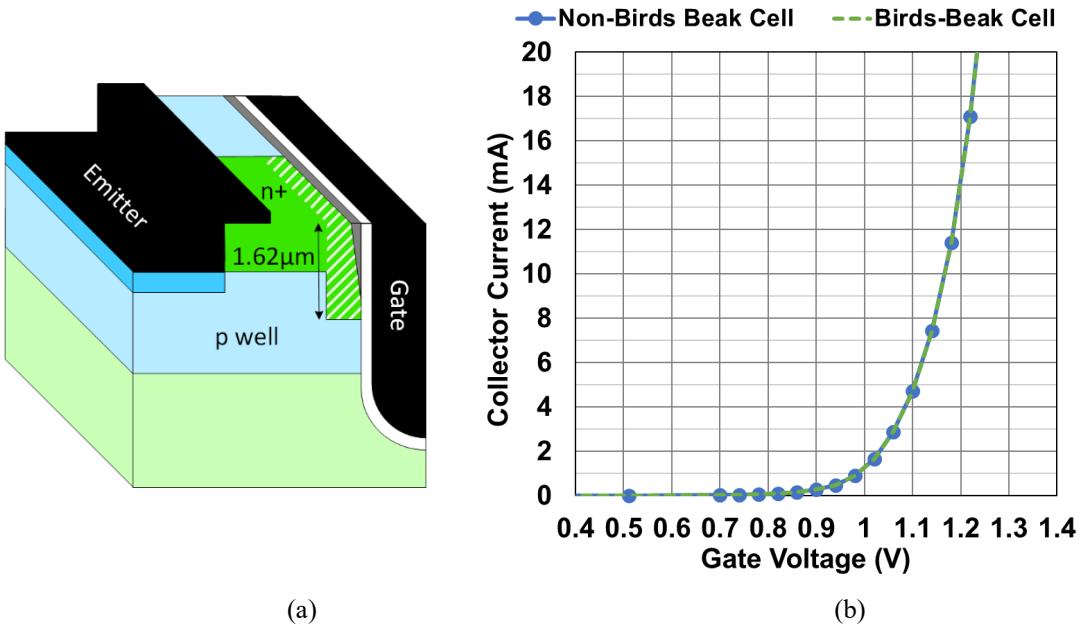
Figure 48 - Schematic of 3D simulation model with birds-beak cell (right) adjacent to non-birds-beak cell (left) with same emitter and collector (not shown)

However, this dual model is a simplification of the device heating as, in reality, the lower threshold regions (non-birds-beak) are dispersed across the device active area and are adjacent to other active regions which contain birds-beak. It is expected that there will be an interaction within the silicon bulk for these two regions, which is not considered in the current separate two cell simulation model. To address this, a further simulation model was developed where a non-birds-beak cell was situated adjacent to a birds-beak cell with a common collector and emitter as one model (Figure 48). This accounts for 16% of the active area and the remaining active area is formed from another cell with birds-beak, connected in parallel as before. This more complex model exhibits an endurance time of 17.71μs; a 17% reduction from the original dual model simulation result. Despite the IGBT having a positive temperature coefficient of resistance which will cause a redistribution of the charge away from the hotter non-birds-beak channel region to the birds-beak channel region, the interaction in the silicon bulk means that the overall temperature of both channel regions will be slightly higher than in the original separated dual model, thus causing a faster rate of heating and a lower endurance time than was previously accounted for.

3.5.4 Eliminating the Effect of Birds-Beak in Trench Devices

To overcome this reduction in endurance time, an additional phosphorus n+ emitter implant is proposed, as shown in Figure 49 (a). A shallow, highly doped arsenic implant is often preferred in power devices as it provides a low contact resistance to the emitter metal which reduces the on-state losses of the device and its susceptibility to thyristor latch up compared to a deeper traditional phosphorus implant. The study has demonstrated, however, that in trench devices the arsenic implant is susceptible to the effects of birds-beaking. As a result, an arsenic phosphorus co-implantation is proposed; a technique commonly implemented in CMOS design [104]. By combining the arsenic and phosphorus implants to form the n+ emitter, a low contact resistance can be achieved while removing the threshold variation across the chip induced by the birds-beaking. The phosphorus implant was applied locally along the gate to the simulation model. The same gaussian implant was applied to the cells with and without the birds-beak, with a peak concentration of $1e20cm^{-3}$ at the emitter metal and the implantation extending to a depth of 1.62μm. Figure 49 (b) shows the threshold voltages of the two simulated cells, demonstrating that this co-implantation strategy removes the effect of the birds-beak

entirely. The threshold of the device is reduced compared to the original model as the p-well doping is lower at the n+ emitter/p-well interface, but designers can compensate for this by increasing the p-well doping concentration, which will also help prevent thyristor latch-up and punch-though under breakdown conditions.



(a) (b)

Figure 49 - (a) Zoomed-in view of 3D TCAD model at the gate with birds-beak structure highlighted in grey and the additional phosphorus co-implant for n+ source shown in striped green. (b) Threshold measurement of TCAD model with additional phosphorus co-implantation, comparing cells with and without birds-beak for same active area, V_{ce}=1V, ambient temperature 298K

3.6 Conclusion

Large variations between the experimental data from the manufactured device and the simulation model lead to the discovery of widespread birds-beaking within the IGBT – an uncontrollable processing defect that the manufacturer was unaware of. This chapter presents the importance of accounting for this in large area devices, and shows that 3D modelling techniques alone do not guarantee an accurate device model. In practical terms, this results in the designer struggling to validate models and underappreciating the true behaviour of the device. The birds-beak phenomenon has been successfully imaged and it has been demonstrated that this effect can be accommodated by using a simple two-device simulation model to account for the variation in threshold voltages across the chip area. This two-model technique reduces computational effort for designers while producing accurate results. The birds-beak phenomenon has been shown to reduce the

short-circuit endurance time of the chip by 31.9% as the areas of lower threshold conduct 25.2% higher current density compared to regions of the device which suffer from birds-beak. To overcome this, an arsenic phosphorus co-implantation technique was demonstrated in simulation where it was shown that there was no variation in device threshold even with the presence of the birds-beak and/or variations across the device area.

Chapter 4

Effect of Emitter Geometry on the Performance of a 3D Trench IGBT

Having developed the verified IGBT model in the previous chapter, it was used to determine an optimum cell design that considered critical 3D effects omitted from previous studies. Currently no study has evaluated all the possible variations that can be made to the IGBT emitter geometry to minimise on-state losses and saturation current. The former is minimised to reduce energy losses and the latter is reduced to increase the reliability of the power semiconductor.

This chapter includes extensive 3D TCAD simulations which have been undertaken to investigate the effect of varying the n+ channel implantation in the z-dimension. The results demonstrate that there are competing effects within the device; for small cells, or cells with a limited channel depth size, the hole current modulation of the channel dominates the device behaviour, resulting in a significant increase in V_{on} and lower $I_{c(sat)}$. For larger cells or cells with an extensive channel depth, it is possible to partially trigger the parasitic thyristor structure, resulting in an increased susceptibility to latch up under short circuit conditions and at high temperatures, which reduces the reliability of the device.[1] This chapter presents the designer with an optimum cell geometry and a set of rules highlighting the limits within which they should work to produce a reliable device.

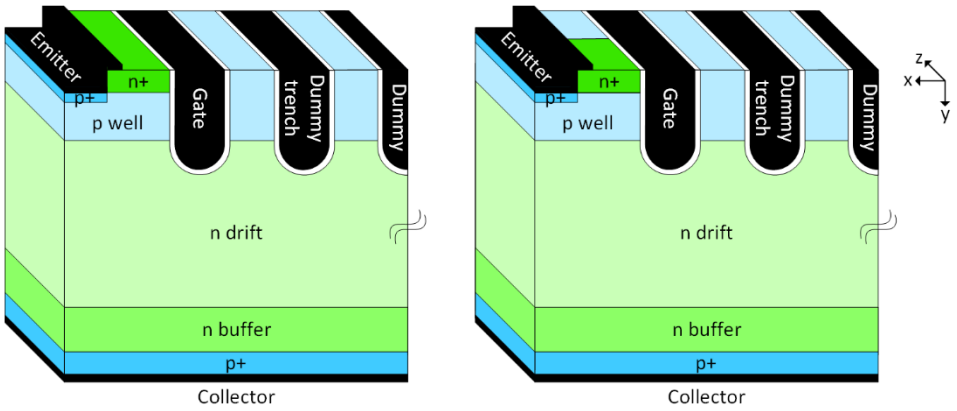
[1] The material in this chapter has been taken from the following publication:
E. M. Findlay and F. Udrea, "Investigation into the Effect of Emitter Geometry on the Performance of 3D Trench Insulated Gate Bipolar Transistor Structures,", IEEE Trans. Electron Devices, under review.

4.1 Introduction

The Trench IGBT has become the dominant IGBT device design compared to the planar cell due to its increased MOS channel density and reduced latch-up susceptibility [55]. Theoretically, a 30-40% overall loss advantage with no serious penalties in safe operating area (SOA) can be achieved [39]–[41]. However, the short circuit capability of the trench device is poorer than the planar variant as the short circuit current is significantly higher due to the reduced voltage drop across the channel [55]. Short circuit destruction of the IGBT can be classified into four modes [105];

1. During device turn on, a large increase in current (di/dt) induces latch-up in the device (by triggering the parasitic thyristor structure within the IGBT) resulting in thermal runaway.
2. During device turn on dynamic avalanche occurs as the critical power of the device has been exceeded due to plasma injection that results in a shorter depletion region.
3. Thermal runaway of the device due to heating effects.
4. During turn off under short circuit conditions a rapid increase in hole current can cause device failure due to latch-up.

Minimising the saturation current ($I_{c(sat)}$), and therefore improving the short circuit safe operating area (SCSOA) is typically achieved by increasing the number of dummy trenches (increasing the silicon area per cell) as explored in [43], or reducing the channel size for a given cell area by alternating the n+ implant with the p-well under the emitter in the z dimension. This is known as hole bypassing the emitter and is shown schematically in Figure 50. Hole bypassing the emitter was first proposed in 1994 [42] with the aim of increasing the channel resistance. A limited number of devices were fabricated, but measurements were not able to fully quantify the device behaviour [42]. A further study was conducted, implementing 2D simulation techniques with some experimental measurements, however this was unable to quantify all 3D effects within the IGBT due to modelling limitations [55]. The effect of hole current within the IGBT, and in particular its effect on the channel inversion, has also been considered, but the study was again limited to a 2D device model [39].



(a) (b)

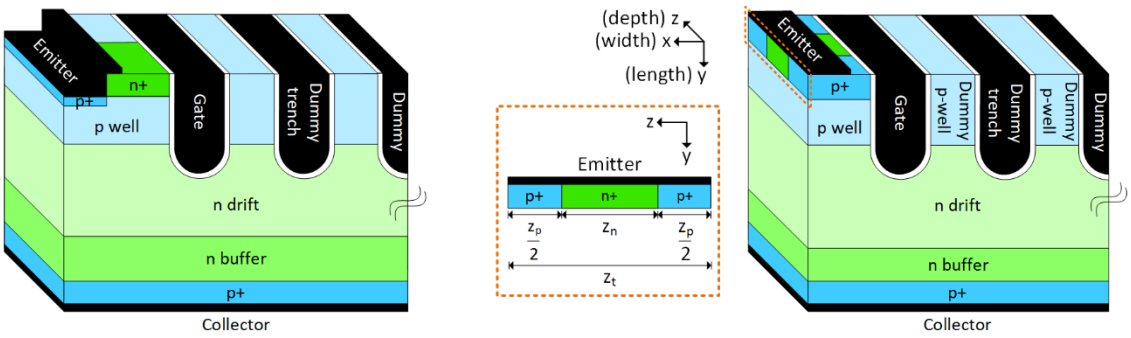
Figure 50 - Schematic of IGBT with (a) continuous n+ implant in z-dimension, (b) hole bypassing the emitter with p-well

All of the previous studies, such as those in [39], [42], [43], [55] have investigated the effect of varying one emitter geometric property independently on IGBT device performance, but no previous study has modelled all variations in a comparative fashion to determine the overall optimum design. [106] studies the effect of the 3D current flow on the accuracy of TCAD simulations and does an initial analysis on the effect of hole bypassing the emitter on saturation current, however the study is limited to an overall fixed cell depth, and no consideration is made to the effect of dummy trenches. The study outlined in this chapter develops this research further by comparing the effect of hole bypassing the emitter and increasing the number of dummy trenches, for varying cell depths, to determine the overall optimum method to minimise the saturation current within a device. The effect that these geometric properties has on the on-state voltage (V_{on}) is also considered. The impact of these modifications on the transient (turn-off) behaviour of the IGBT was investigated but shown to have no effect.

4.2 Device Structure

Figure 51 (b) is a schematic representation of the 3D TCAD IGBT model developed for this investigation, based upon the previously calibrated simulation set-up as discussed in Chapter 3 [107]. As highlighted by Figure 51 (a), which shows the original 3D IGBT cell discussed in Chapter 3, there were a few modifications to the basic 3D structure. To account for all fringing effects in the unit cell (the smallest replicating structure) the n+

emitter implant was moved to be centrally located. The emitter connection also varies slightly from the model developed in Chapter 3 as it was found that, for that original structure, the emitter short to the p-well region was dominated by the p+ contact to the side of the emitter n+ implant and therefore no variation in saturation current with p-well depth was observed. As a result, for this study, the p+ region was moved to be adjacent to the n+ channel implant so the effect of varying Z_p (Figure 51 (b)) could be explored. This modification does not inherently affect the IGBT behaviour but does exaggerate the physical effects of the geometry change enabling a detailed investigation of this feature.



(a) (b)

Figure 51 - 3D IGBT cell structure (not to scale) (a) original 3D IGBT model (b) modified model for this study with inset showing zoom of emitter n^+/p^+ implantation in z plane.

Simulations were conducted for a variety of scenarios: with a fixed cell size (Z_t, Figure 51 (b)), the depth of the n+ channel implantation (Z_n, Figure 51 (b)) was varied. In addition, for a fixed proportion of n+ channel implantation with respect to the overall cell size (Z_n/Z_t constant), the effect of varying the depth of the cell (Z_t) was explored. The number of dummy trenches were also varied, but through all modifications the total active area of the IGBT was kept constant such that all results could be directly compared. All dummy trenches and dummy p-well regions were left floating unless otherwise stated.

4.3 Device Short Circuit Performance

The short circuit simulations were completed in accordance with the IEC standard measurement [87] and followed the procedure outlined in Chapter 3, Section 3.5.3.

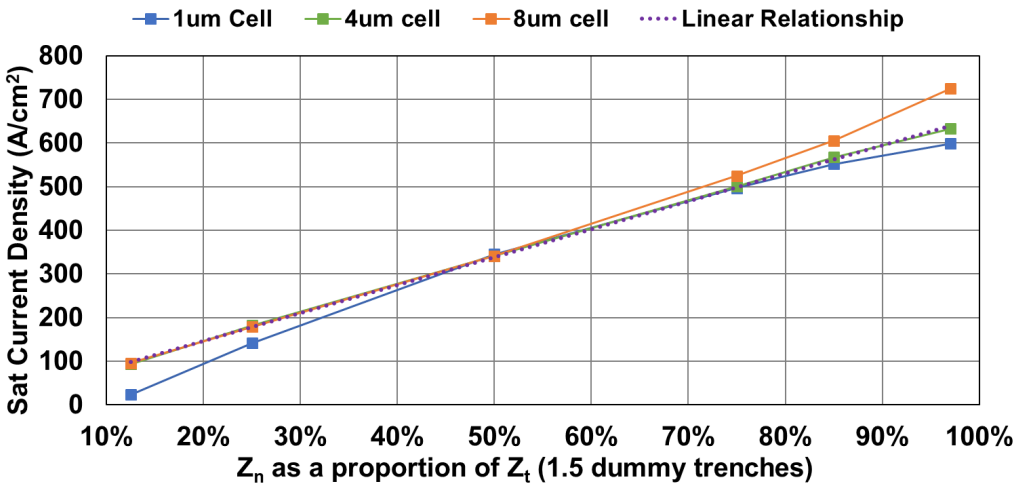


Figure 52 - Short circuit saturation current for Z_t 1µm, 4µm and 8µm with varying depth of n+ implant (Z_n), ambient temperature 423K. Total device area remained constant.

Figure 52 shows the variation in the saturation current for different n+ channel depths (Z_n) and for cell sizes (Z_t) 1µm, 4µm and 8µm. Theoretically, four effects within the IGBT are expected to be seen when modifying Z_n for a given Z_t, which can be identified and related to the equivalent schematic of the IGBT shown in Figure 53;

1. A linear variation of saturation current with channel depth (MOSFET behaviour)
2. Second order fringing effects adding an additional Δz to the effective channel depth
3. Modulation of the channel through the flow of hole current; higher hole current reduces the channel resistance and increases $I_{c(sat)}$ [39]
4. Inducing a partial latch up of the IGBT (partially triggering the thyristor structure: n+ emitter, p-well, n-drift/n-buffer, p+ collector)

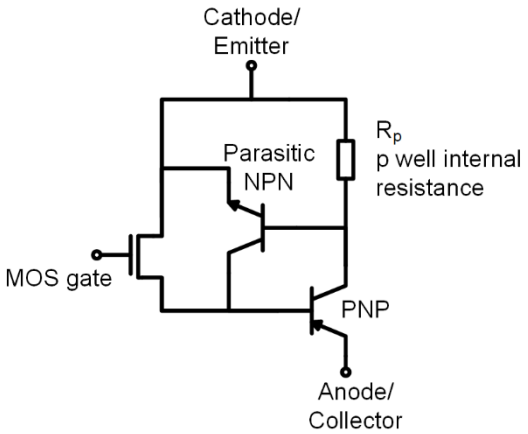


Figure 53 - Equivalent circuit schematic of IGBT

Each of these effects can be seen in the results presented in Figure 52. The 4µm cell follows a linear relationship between n+ channel depth and saturation current, indicating that, for this size of device, the MOSFET channel behaviour dominates. By increasing the hole bypass area (Z_p) or reducing the n+ channel depth (Z_n), there is an increased voltage drop across the channel and the electric field becomes more concentrated at the n+ emitter/p+ emitter junction. It is this higher electric field concentration that causes the saturation of the carrier velocity at a lower collector-emitter voltage, thus reducing the short circuit saturation current [55].

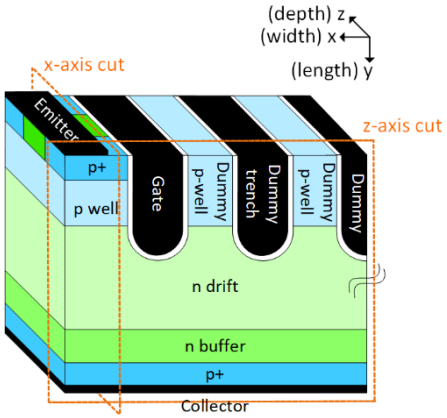


Figure 54 - Schematic of IGBT cell, showing cutline for Figure 55 (z-axis cut only) and Figure 56 (intersection of x-axis and z-axis cut)

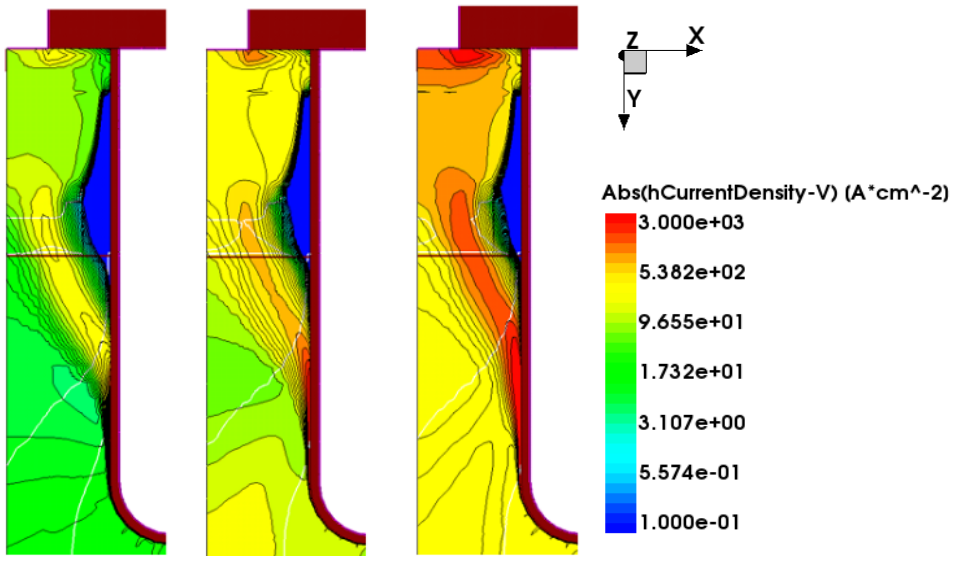


Figure 55 - Hole current density at emitter of device with Z_t=1µm under p+ implant as shown in Figure 54 z-axis cutline, (a) Z_n 0.125µm (Z_n/Z_t 0.125), (b) Z_n 0.25µm (Z_n/Z_t 0.25), (c) Z_n 0.5µm (Z_n/Z_t 0.5), ambient temperature 298K

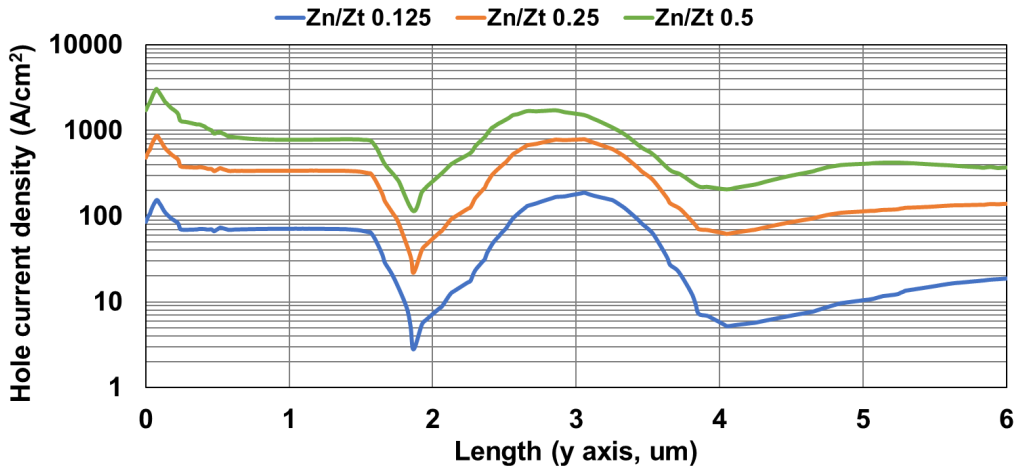


Figure 56 - Hole current density in the p-well with Z_t=1µm (plot taken from the emitter contact to the bottom of the gate trench) at the intersection of the z-axis and x-axis cutlines as shown in Figure 54, Z_n 0.125µm (Z_n/Z_t 0.125), Z_n 0.25µm (Z_n/Z_t 0.25) and Z_n 0.5µm (Z_n/Z_t 0.5), ambient temperature 298K

For small n+ channel depths (Z_n/Z_t<50%), the 4µm and 8µm cells have the same saturation current, indicating that for these larger cells, fringing effects are minimal. Whereas for the 1µm cell, the saturation current exhibits a sub-linear behaviour caused by the modulation of the channel by the flow of hole current. A significantly reduced hole current flows through the 1µm cell with Z_n/Z_t=12.5% compared to Z_n/Z_t=50% (as highlighted by the hole density plots given in Figure 55 and Figure 56). The consequence of this is a significantly larger depletion region adjacent to the channel (shown in blue, Figure 55), which, in turn, induces a larger channel resistance. This is caused by a lower distributed substrate (n-drift) potential, which supresses enhancement of the channel region and thus increases the tendency of the device to saturate [39]. At greater n+ channel depths (Z_n/Z_t>75%), the 1µm cell again exhibits a sub-linear behaviour, this time caused by pinch-off of the device; after accounting for fringing effects which increase Z_n further, the remaining p+ area under the emitter contact is too small and therefore inhibits the extraction of holes, which causes the device to saturate prematurely.

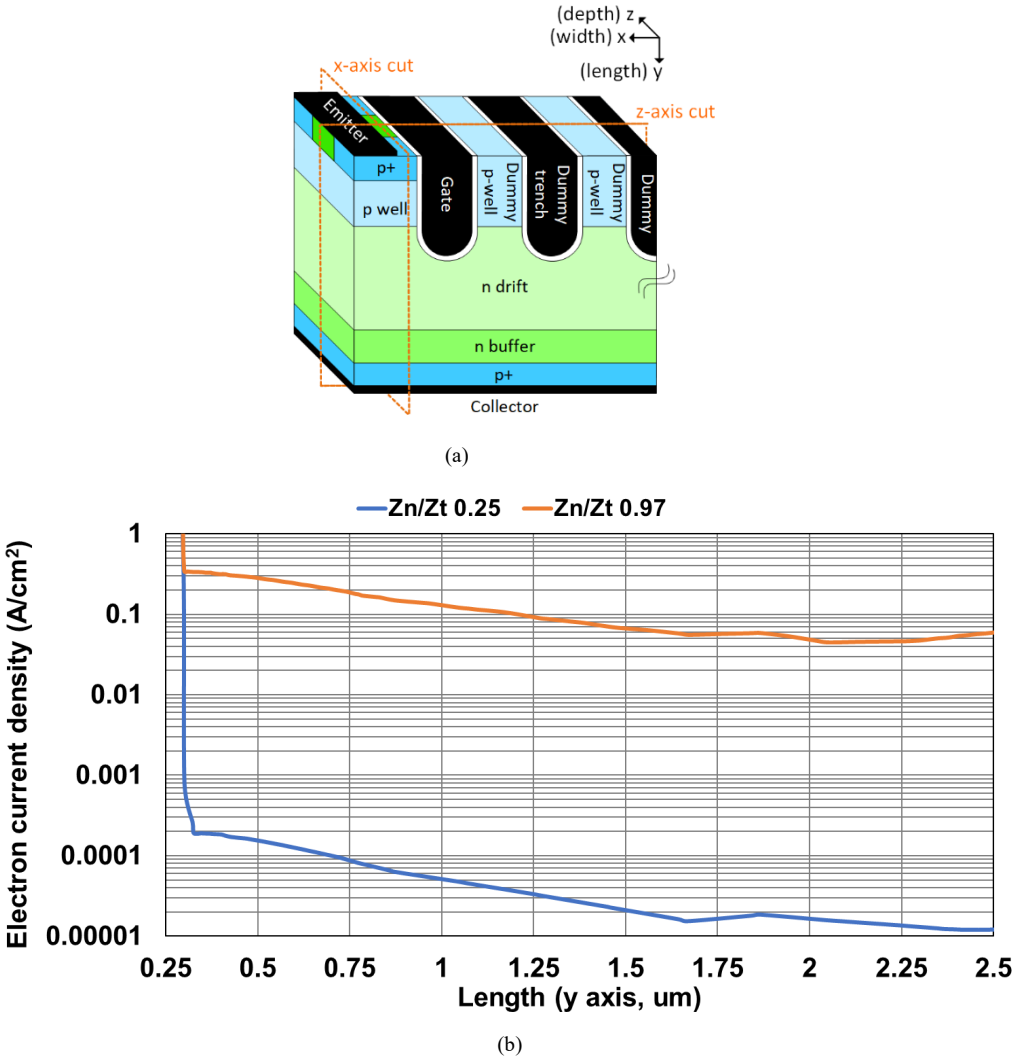


Figure 57 - (a) Schematic of IGBT cell, showing cutlines, (b) Electron current density in the p-well of device (taken at the intersection of cutlines as shown in (a)) with Z_t 8µm, for Z_n 2µm (Z_n/Z_t 0.25) and Z_n 7.76µm (Z_n/Z_t 0.97), ambient temperature 298K

For the 8µm cell at large channel depths (Z_n/Z_t>75%), a super-linear behaviour is exhibited due to a partial latch up of the IGBT. In this case, the physical size of Z_n increases to such an extent that the n+/p-well boundary becomes forward biased due to the concentration of holes running under the n+ implant (the hole current tends to flow near the electron supply to satisfy the condition for charge neutrality [1]). This results in the partial turn-on of the parasitic thyristor structure within the IGBT, as demonstrated in Figure 57 by the increased electron density in the p-well for the cell with larger channel depths (an increase of several orders of magnitude).

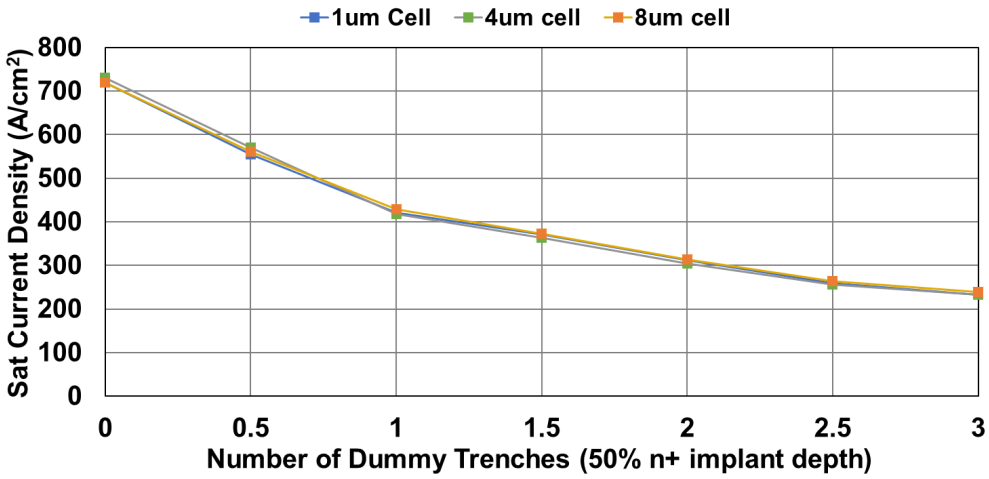


Figure 58 - Short circuit saturation current for Z_t 1µm, 4µm and 8µm with varying number of dummy trenches, ambient temperature 423K. Total device area remained constant and $Z_n/Z_t = 0.5$.

Increasing the number of dummy trenches within the device reduces the saturation current, as shown Figure 58. Since the total device active area remained constant for these simulations, as the cell width increased (due to more dummy trenches), the channel density reduced. As a consequence, fewer carriers are injected per unit area causing a reduction in saturation current. This reduction does not follow a linear trend; these trenches influence the flow of hole current and the modulation of the channel, but their effect becomes diminished for increasing number of trenches. As expected, Z_t had no effect on the saturation current when varying the number of dummy trenches. Comparing Figure 52 and Figure 58 it can be seen that having zero dummy trenches is of comparable saturation current density to the cells with large channel depths (Z_n/Z_t>75%), however, for larger numbers of dummy trenches, the reduction in saturation current is smaller compared to the effect of reducing the channel depths to Z_n/Z_t<25%.

4.4 Short Circuit Current Versus On-State Voltage

The relationship between saturation current and on-state voltage is given in Figure 59 for cells with a 50% channel depth (Z_n/Z_t) and 1.5 dummy trenches. On-state voltage was measured at 100A/cm^2 for a gate-emitter voltage of 15V, using the procedure for on-state measurements as outlined in Chapter 3, Section 3.3.2.

The full expression for the on-state voltage drop of an IGBT structure is given as [1];

$$V_{on} = V_{P+N} + V_{NB} + V_{MOSFET}$$

Equation 10 - On-state voltage drop for an IGBT where V_{P+N} is the voltage drop across the p+ collector/n-base junction, V_{NB} the voltage drop across the n-drift region once conductivity modulation has been accounted for due to high-level injection conditions, and V_{MOSFET} is the voltage drop across the MOSFET portion. [1]

In this analysis V_{P+N} was unchanged as there were no modifications made to the collector geometry or doping throughout the study. It was therefore expected that, for a fixed Z_n/Z_t, V_{on} would increase with increasing Z_t as the voltage drop across the channel becomes greater: for larger devices, the effective channel area is reduced since the impact of the fringing effects becomes increasingly negligible (the fringing depth remains a fixed length because the n+ emitter and p+ emitter doping is unchanged). Figure 59 shows, however, that cells with Z_t in the range of 0.25µm to 1µm have an inverse linear relationship between on-state voltage and saturation current. At these small dimensions the effect of modulation of the channel due to the hole current becomes dominant; this hole current reduces the tendency of the device to saturate as well as modulating the MOS component (reducing V_{on} as the variation in V_{NB} becomes significant). For all other cells in Figure 59, this modulation of the channel (V_{NB}) becomes less significant and as such the V_{MOSFET} term increases with channel depth and dominates the expression for the on-state voltage (Equation 10).

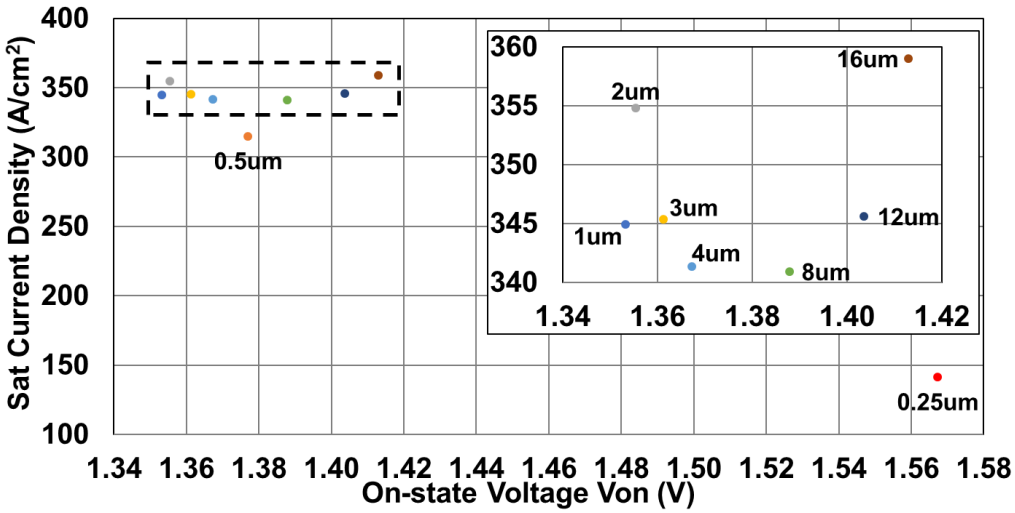


Figure 59 - Relationship between short circuit saturation current (423K ambient) and on-state voltage (100A/cm², V_{ge} = 15V, 298K ambient) for varying Z_t with 50% channel depth (Z_n/Z_t) and 1.5 dummy trenches.

Despite this, the saturation current does not always reduce as a result of this larger on-state voltage, which would be expected for a MOSFET, due to the conflicting effects as discussed in Section 4.3. Only cells with Z_t in the range of 2µm to 4µm follow this expected trend. For Z_t in the range of 1µm to 2µm the saturation current behaviour is still dominated by the hole current modulation of the channel; the 2µm cell has higher distributed drift potential, increasing channel injection and therefore increasing $I_{c(sat)}$. For cells in the range Z_t = 8µm - 16µm, the saturation current also increases with increasing Z_t but, at these dimensions, the partial latch up of the IGBT begins to be induced, to such an extent that the 16µm cell has been shown to latch after only 2µs under short circuit conditions. This simulation included self-heating effects (following the procedure outlined in Chapter 3, Section 3.5.3). As a consequence of this latching, thermal run-away of the device results in the 16µm cell design failing to meet the basic requirement that IGBTs should be able to withstand short-circuit conditions for a minimum of 10µs [87].

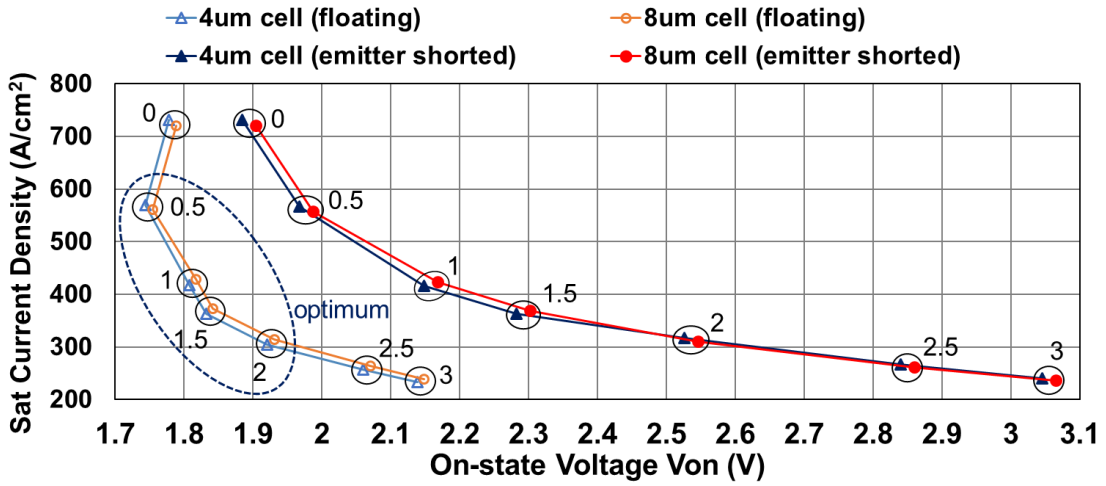


Figure 60 - Relationship between short circuit saturation current (423K ambient) and on-state voltage (200A/cm^2, 298K ambient) for the dummy p-well and dummy trenches both either emitter shorted or floating, with varying numbers of dummy trenches (0 to 3) for Z_t 4µm and 8µm and 50% channel depth (Z_n/Z_t). Total area factor remained constant.

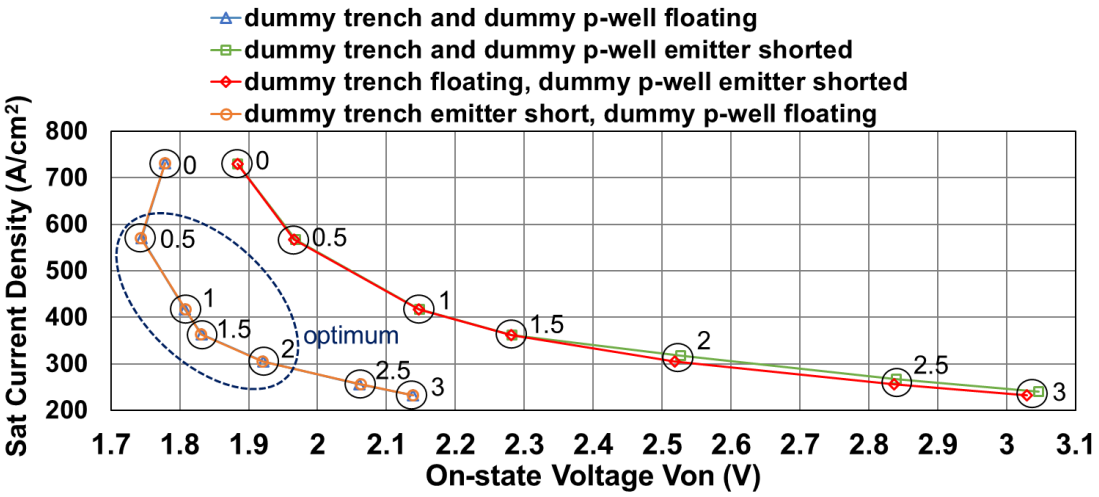


Figure 61 - Relationship between short circuit saturation current density (423K ambient) and on-state voltage (200A/cm^2, 298K ambient) for emitter shorted or floating p-well regions and (varying numbers of) dummy trenches (0 to 3) for Z_t 4µm with 50% channel depth (Z_n/Z_t). Total area factor remained constant.

Figure 60 and Figure 61 investigate the effect of the dummy p-well regions and dummy trenches on the performance of the IGBT. In Figure 60, for a 4µm and 8µm cell (Z_t) with 50% channel depth (Z_n/Z_t), these dummy regions were either both left floating or both emitter shorted. The results indicate that varying the number of dummy trenches to increase the width of the cell reduces the saturation current and typically increases the on-state voltage as expected, due to the reduction in channel density. Figure 60 highlights that the size of the cell (Z_t) has no effect on the saturation current. Z_t has minimal effect on V_{on}, but V_{on} is dependent on the electrical connections made to the dummy p-well/dummy trenches; floating connections have a reduced V_{on} compared to emitter shorting. This is in line with the results in Figure 58 and Figure 59.

Figure 61 investigates the effect of varying the electrical connections made to the dummy p-well and dummy trenches independently. A 4µm cell with 50% channel depth (Z_n/Z_t) was chosen for this investigation and all four combinations of electrical connections for the dummy p-well and dummy trenches were evaluated. The results in Figure 61 indicate that having the dummy p-well regions and the dummy trenches independently either floating or emitter shorted has little effect on the saturation current, but the type of connection to the dummy p-well significantly impacts V_{on}. Emitter shorting the dummy p-well regions results in an appreciably larger on-state voltage because this connection provides an avenue for hole extraction away from the channel that, in turn, reduces the

modulation of the channel by the hole current. By also emitter shorting the dummy trenches, V_{on} varies slightly for larger devices (larger number of dummy trenches) as the field applied to these trenches further supresses the hole current flow parallel to the gate. For the device with floating dummy p-well regions, as shown in Figure 61, V_{on} reduces from 0 dummy trenches to 0.5 (with the dummy trench either floating or emitter shorted). This result is also evident in Figure 60. The presence of the dummy trench controls the hole current flow at the top of the device, and, in this instance, increases the hole current flow parallel to the channel significantly. This effect offsets the reduction in the channel density caused by introducing this dummy trench, and hence reduces the on-state voltage. It is therefore beneficial to have a dummy trench structure as part of the overall cell design, and 0.5 dummy trenches is sufficient to achieve the performance benefit. From the results in Figure 61 an optimum range of between 0.5 and 2 dummy trenches is ideal, allowing a trade-off to be made between V_{on} and saturation current at the designer's discretion depending on the application for the IGBT; an effect similar to adjusting the p+ collector implantation. Further increases beyond 2 dummy trenches does continue to reduce the saturation current but with the penalty of significantly increasing the on-state voltage.

4.5 Transient Performance at Turn-Off

Figure 62 considers the relationship between on-state voltage and turn-off energy (E_{off}) for varying cell size (Z_t). The turn-off energy losses were calculated from an inductive load turn-off test using the same conditions as stated in Chapter 3, Section 3.5.1.

Given that the turn-off energy only varies from 38.7mJ/cm^2 to 37.8mJ/cm^2 (2% variation) and there is no clear trend, it can be concluded that E_{off} is essentially unaffected by the cell size.

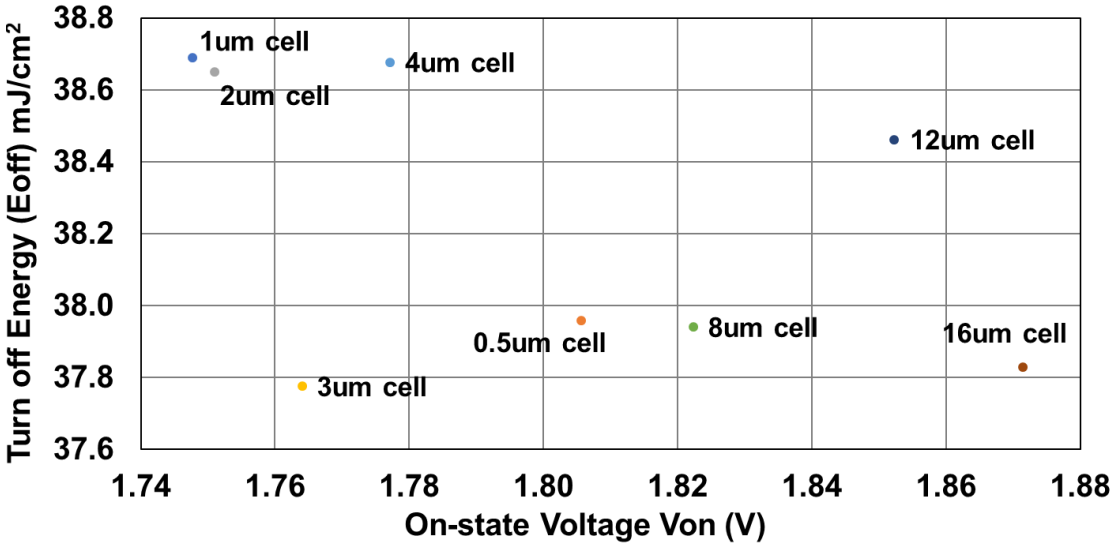


Figure 62 - Relationship between inductive load turn-off energy loss (E_{off}) (298K ambient) and on-state voltage (200A/cm^2, 298K ambient) for varying Z_t with 50% channel depth (Z_n/Z_t) and 1.5 dummy trenches. Total area factor remained constant.

4.6 Conclusion

This chapter presents an investigation into the effect of geometric properties of a trench IGBT cell, in particular comparing the effect of hole bypassing the emitter with the introduction of dummy trench structures, on the saturation current and on-state voltage. The results have demonstrated that there are competing effects within the device that determine the overall behaviour. From the results, the optimum device is shown to be Z_t = 1µm, Z_n = 0.5µm with at least 0.5 dummy trenches, and the dummy p-well regions should be left floating. Reducing Z_t or Z_n further results in a reduction of the channel modulation by hole current which significantly increases V_{on}. Dummy trenches are necessary to control the hole current flow at the top of the device, however increasing the number of dummy trenches beyond 0.5 to reduce channel density and thus the saturation current is at the designer's discretion and provides a trade-off with the on-state voltage. It has been shown, though, that increasing the number of dummy trenches beyond two is undesirable as it results in a significant increase in on-state losses with only a minimal reduction in saturation current. The effect of hole modulation of the channel has a larger impact on saturation current than increasing the number of dummy trenches. In particular, for larger geometries (Z_t > 8µm and Z_n > 6µm) it has been demonstrated that it is possible to partially trigger the parasitic thyristor structure, resulting in an increased susceptibility

to latch up under short circuit conditions. It has also been shown that the emitter geometry has no effect on IGBT turn-off losses.

Chapter 5

Reverse-Conducting IGBT: A review of current technologies

This chapter presents the Reverse-Conducting IGBT (RC-IGBT) which integrates an antiparallel diode structure within the IGBT, in a similar fashion to the inherit body diode within a Power MOSFET structure. The RC-IGBT has several benefits over a separate IGBT and diode solution and has the potential to become the dominant device within many power electronic applications; including, but not limited to, motor control, resonant converters, and switch mode power supplies. However, the device inherently suffers from many undesirable design trade-offs which have prevented its widespread use. One of the most critical issues is the snapback seen in the forward conduction characteristic which can prevent full turn-on of the device and result in the device becoming unsuitable for parallel operation (required in many high voltage modules). This phenomenon can be suppressed but at the expense of the reverse conduction performance.

This chapter provides an overview of the technical design challenges presented by the RC-IGBT structure and reviews the alternative device concepts which have been proposed in literature, while discussing the challenges in commercialisation. For the first time, the most promising concepts have been simulated under the same conditions such that they can be directly compared. Analysis shows that these alternate concepts either present a trade-off in performance characteristics, an inability to be manufactured, or a requirement for a custom gate drive. [1]

[1] The material in this chapter has been taken from the following publication:
E. M. Findlay and F. Udrea, "Reverse-Conducting Insulated Gate Bipolar Transistor: A Review of Current Technologies," IEEE Trans. Electron Devices, vol. 66, no. 1, pp. 219–231, Jan. 2019, doi:10.1109/TED.2018.2882687

5.1 Introduction

In recent years, the IGBT has replaced the silicon MOSFET in certain applications because the IGBT has a lower on-state voltage for the same voltage blocking rating due to the bipolar injection mechanism within the device [36], [84]. Compared to MOSFETs, IGBTs can operate at higher power densities due to lower on-state losses [84], but power MOSFETs have an intrinsic anti-parallel (body) diode providing a reverse conduction path which is not present in the structure of a traditional IGBT [108]. For most power electronic applications, including but not limited to motor control, resonant converters and high switch mode power supplies, the IGBT is utilised in conjunction with a free-wheeling diode (FWD) connected in anti-parallel, typically fabricated in either separate packages or as connected die within a module [108].

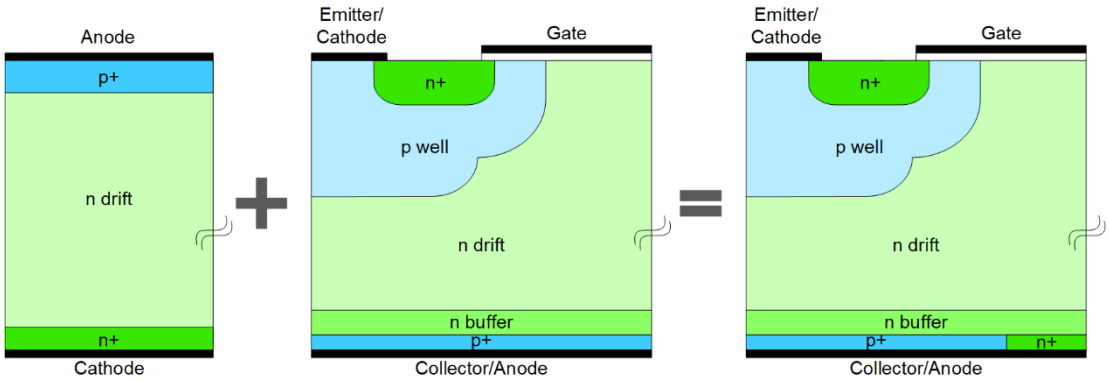
The FWD performance is critical during both normal switching and under surge conditions [36]. Separate connections introduce additional costs (bonding, packaging and silicon) [36], [108]. Furthermore, these bond wires can introduce parasitic oscillations under switching conditions, which can lead to additional die losses. By integrating the switch and the anti-parallel diode into a single structure, the Reverse-Conducting IGBT (RC-IGBT) enables a higher power per package footprint to be achieved [36]. However the traditional RC-IGBT cannot be used in high power applications as the device is not suitable for parallel operation due to the negative resistance characteristic exhibited in the on-state (forward conduction) [109]. Limitations in fabrication technologies have also hampered the development of the RC-IGBT concept, however with the emergence of thin-wafer processing (and alternative techniques such as reactive ion etching [110]) more device concepts are being realised and it has become an active area of research [108].

This chapter provides a review of the RC-IGBT concepts, highlighting the advantages and disadvantages of each design and discussing the challenges in commercialisation.

5.2 Traditional RC-IGBT structure

The RC-IGBT structure was first proposed in 1987 with a collector shorted, p-channel IGBT [80] building upon the concept suggested by Ueda et al. [37]. A commercially available soft punch through (SPT) n-channel RC-IGBT is given in Figure 63. In order to integrate the diode structure within the IGBT to enable a reverse-conducting capability,

n+ regions (anode shorts) are implanted into the p-collector (p-anode) [71], [81]. When a reverse voltage is applied to the device, electrons are provided by the n+ anode short and holes are injected from the p+ emitter (p+ cathode), resulting in the device behaving in a similar manner to a PIN diode. It has been reported that the doping profile of the field stop (FS) layer can be optimised to improve turn-off losses by modifying the injection efficiency of the anode (emitter) [81].



(a) (b) (c)

Figure 63 - Vertical Cross Section of Infineon IHW20N120R3 RC-IGBT (c), highlighting the construction with the anti-parallel diode (a) and the IGBT structure (b) [83]

The RC-IGBT presents several advantages:

1. A RC-IGBT uses less area than an equivalent IGBT and diode (>30% size reduction, Figure 64)
2. Reduction in assembly cost (bonding, packaging and less silicon area)
3. Reduction in wafer processing and testing cost
4. Lower thermal resistance and reduced temperature ripple as the same silicon volume is used during both diode and IGBT conduction modes
5. More degrees of freedom in package layout
6. Improved reliability due to fewer bond wires within a module (bond wires induce parasitic (inductive) effects)
7. More suitable for high junction temperature operation as the leakage current in IGBT mode is lower due to the presence of the anode shorts (reduced pnp transistor gain).

8. Possibility of using a suitable gate signal to allow better trade-off between the on-state voltage drop and the reverse recovery losses of the diode.

[108], [111], [112]

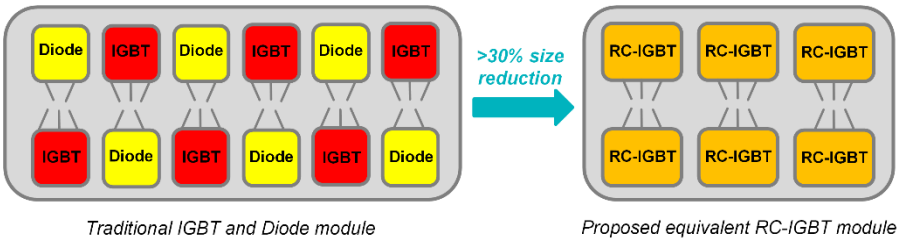


Figure 64 - Schematic representation of module size reduction of a standard IGBT/diode module (3 IGBT/diode die per switch position in half bridge configuration), compared to an equivalent RC-IGBT module

It has also been shown that the performance and design trade-offs associated with the SPT design are strongly minimised by the introduction of these anode shorts [111]. However, the RC-IGBT structure within high voltage, hard switching application suffers from a number of undesirable characteristics;

- Snapback in the current-voltage characteristics is present (MOSFET shorting effect)

  Anode shorts provide a MOSFET structure within the IGBT such that at initial turn-on of the device, unipolar conduction occurs (current flow through the anode short) until the n buffer/p+ anode region becomes forward biased so that hole injection from the p+ collector begins and conductivity modulation occurs in the drift region. This results in a rapid decrease in the on-state resistance causing the snapback exhibited in the I-V characteristic. This snapback, shown in Figure 65, is more prevalent at lower temperatures, as the voltage drop needed to forward bias the p+ collector/n buffer junction increases at lower temperature at a rate of approximately 2mV/ºC. As a consequence, at low ambient temperatures the device can fail to fully turn-on. Reduction in the density of n+ shorts within the device area can reduce the snapback voltage but at the expense of the anti-parallel diode performance. [36], [71], [108], [111], [113], [114]

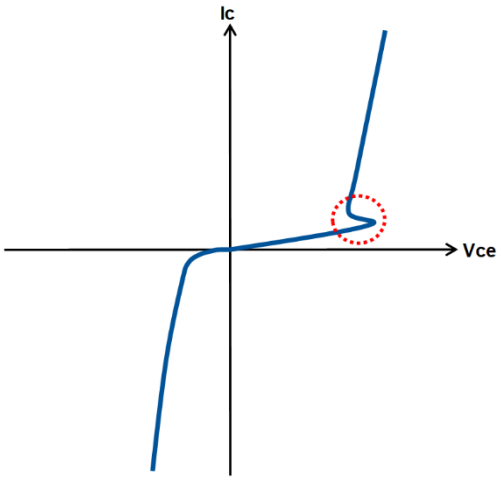


Figure 65 - Typical RC-IGBT on-state characteristics, with the snapback region highlighted in red

- A trade-off between the IGBT on-state losses and the diode reverse recovery losses (plasma shaping effect)

  Plasma distribution affects both the on-state and switching losses. Moreover, the collector p-wells in forward conduction (IGBT mode) are also the anode of the device in reverse conduction (diode mode). It is desirable to have a high plasma concentration in the upper part of the drift region (closer to the gate) to reduce the on-state losses in IGBT mode, but in order to minimise the reverse recovery losses of the diode, a low plasma concentration is desirable. These contradictory aims are difficult to optimise, but typically local lifetime control helps to achieve selective plasma reduction [115], [116]

- Reduction in Safe Operating Area (SOA) (the charge uniformity effect)

  Non-uniform current distribution occurs in RC-IGBTs due to the relatively large p+ collector (anode) implant, compared to the n+ anode short. Current crowding can occur at the p+ collector/n+ anode short boundary when the RC-IGBT conducts in diode mode. This can result in the device overheating and the local hotspot formation can ultimately lead to the destructive failure of the device. [117].

- A trade-off between the IGBT and diode softness (drift layer effect)

  It is desirable for the RC-IGBT to have a thin n-drift layer to minimise on-state losses in IGBT mode. However, this low resistance induces a high di/dt during the reverse recovery of the diode which causes it to exhibit snappy behaviour. The

diode is therefore prone to hard reverse recovery which increases electromagnetic interference [111], [118].

There have been many reported optimisations of the traditional RC-IGBT structure to overcome these trade-offs, all with varying success. Several papers have investigated the use of a dedicated gate drive scheme in order to reduce losses by varying the p-collector (p-anode) efficiency [119], [120]. In terms of static loss during diode conduction mode, a low (negative) gate voltage is required, but this increases the dynamic losses as the carrier density within the device is higher, therefore complex gate drive schemes have been developed to optimise these losses [120]. In the case of the Reverse Conducting IGBT with Diode Control (RCDC), the addition of continuous p-anode areas on the backside of the device suppresses the snapback behaviour, but does not remove it entirely. Although the devices with this additional gate control enable the user to vary the on-state voltage for the diode, the complicated nature of the gate control (the requirement for a dedicated current direction detection during inverter operation) makes it unsuitable for the majority of applications [119], [120]. An alternative variation is the introduction of an oxide trench between the anode short and the p+ anode which increases the resistance of the short such that the snapback characteristic is suppressed, but the device suffers from non-uniform current flow and poor switching performance [121]. In addition, the processing of the oxide trench on the back of the wafer is challenging and the effect of phenomena such as hot carrier injection still needs to be examined.

Research has also been conducted into improving the junction terminations to improve the safe operating area of the RC-IGBT [122] as well as optimising the dimensions and structure of the FWD within the RC-IGBT to minimise losses without lifetime control in order to minimise process steps [123].

5.3 Alternative RC-IGBT Structures

Several approaches have been proposed to improve the electrical performance of the RC-IGBT. The concepts can be grouped into four classifications, which are explored in more detail in the following sections;

1. Thyristor based structures
2. Complex backside processing

3. Pilot structures
4. Other concepts

A summary of these structures' advantages and disadvantages can be found in Appendix A.3. 2D simulations of some of these concepts have also been undertaken; modelled using a comparable cell to enable a direct performance comparison (Section 5.4).

5.3.1 Thyristor Based Structures

5.3.1.1 RC-IGBT with anti-parallel thyristor

A proposed RC-IGBT which utilises a thyristor to enable conduction in the reverse direction is given in Figure 66. The NPT variation of this concept has also been reported as the RC-Trench Clustered IGBT (RC-TCIGBT) [124]. Within the p+ anode region an n+ column is present leaving a narrow p- layer before the n+ buffer region; the p base, n- drift/n buffer, p- layer, n+ column form the thyristor structure. It is reported that the thyristor has a comparable on-state voltage to an anti-parallel PIN diode, but the thyristor structure is not immediately triggered when a 0.7V forward bias is applied, instead triggering when the current gain of the npn and pnp transistors equal 1 or when either the npn or pnp is operating in punch through mode (either the n- drift/n buffer or the p- layer is depleted). [113]

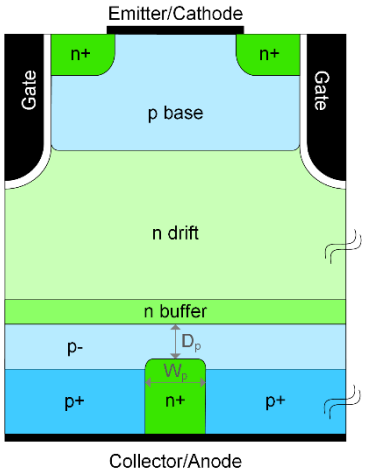


Figure 66 - Device structure of the RC-IGBT with anti-parallel thyristor [113]

The narrow p- layer present in this design forms a barrier to electrons when conducting in IGBT mode, thus avoiding the snapback phenomenon, assuming that D_p (Figure 66) is of sufficient size. As D_P is reduced, the gain of the npn transistor increases such that electrons are no longer confined to the n buffer layer and the snapback characteristic in the I-V characteristic re-emerges [113]. In the extreme (when $D_P = 0$) this results in the traditional RC-IGBT structure with anode shorts given in Figure 63. To minimise the snapback phenomenon in the forward conduction direction it is important that the pnp transistor is turned on quickly which can be achieved by;

1. Increasing the channel density
2. Increasing $R_{n\text{- buffer}}$
3. Reducing the current gain of the npn transistor to facilitate turn-on of the pnp

[113]

2D simulations showed that by increasing the channel density, a snapback characteristic in the reverse conduction state emerges (the α_{pnp} is reduced to such an extent that it is difficult to turn on the thyristor) [113]. A similar snapback occurs in the reverse conducting characteristic when the carrier lifetime is decreased, despite the overall improvement to the switching performance [113]. To eliminate this snapback in the reverse conduction characteristic, the addition of floating n+ dots to restrict hole injection was proposed such that carrier lifetime could remain high without affecting switching performance (Figure 67) [113]. A number of dots were removed above the n+ column to reduce the turn-over voltage in the forward conduction without affecting the turn-off time [113]. Simulation results have indicated several trade-offs with this proposed solution;

- Snapback in the forward conduction mode was not eliminated, but the effect was less pronounced with the removal of more n+ dots above the n+ column (Figure 68)
- Turn-off time for the IGBT increased as more n+ dots were removed (Figure 69)

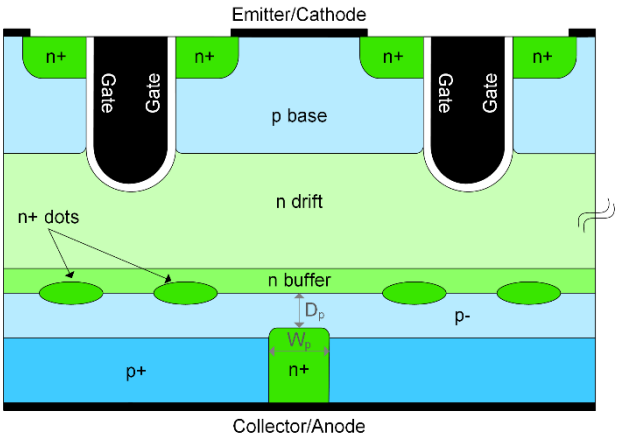


Figure 67 - Device structure of the RC-IGBT with anti-parallel thyristor and n+ dots [113]

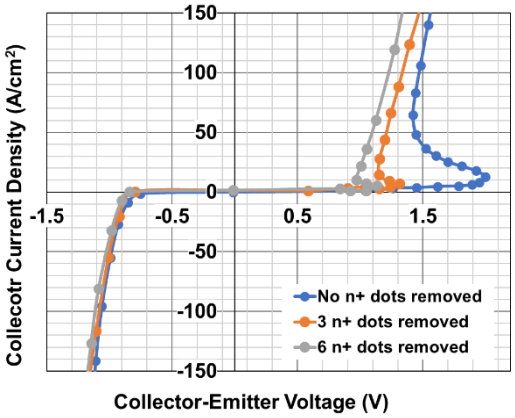


Figure 68 - Simulated output characteristics of the RC-IGBT with different numbers of N+ dots removed from the top of N+ column [113]

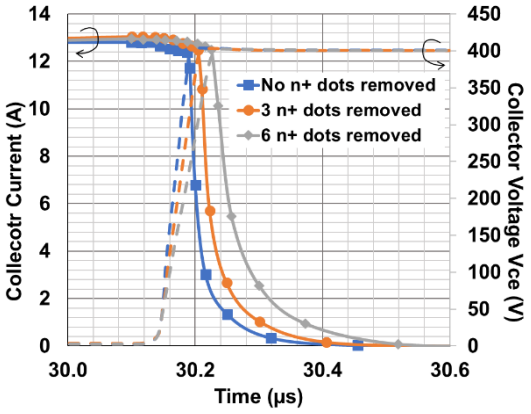


Figure 69 - Simulated turn-off waveforms in IGBT mode with different numbers of N+ dots removed from the top of N+ column [113]

A variation on the above design involves the addition of dielectric (oxide) trenches either side of the n+ column, instead of using n+ dots. Simulation results have reported that this technique also suppresses the snapback phenomenon and by increasing the number of parallel thyristor structures within a single device (by reducing the n+ column and p+ anode widths) a more uniform current density distribution can be achieved in both the forward and reverse conduction direction for a given device area, but this in turn results in a reduction in the on-state characteristics in both modes. [125]

Experimental data to support the simulation results have yet to be reported for the RC-IGBTs with anti-parallel thyristor structures. Both of these papers indicate that the trade-

off between forward and reverse conduction capabilities is difficult to optimise for this structure [71].

5.3.1.2 RC-IGBT with anti-parallel Shockley diode

The RC-IGBT with anti-parallel Shockley diode (SH-RC-IGBT) is shown in Figure 70. The device is very similar to that shown in Figure 66, containing an n+ short, which is instead isolated by an oxide trench. The reverse conduction FWD is achieved through a Shockley diode formed by the p-base, the n-drift, the p2-base and the n+ short. In the forward conduction state (Figure 71), the anode-short effect is suppressed as only a small amount of current can flow through the npn transistor (n-buffer, p2-base, n+ short) thus making the anode short inactive during initial forward conduction of the device. [126]

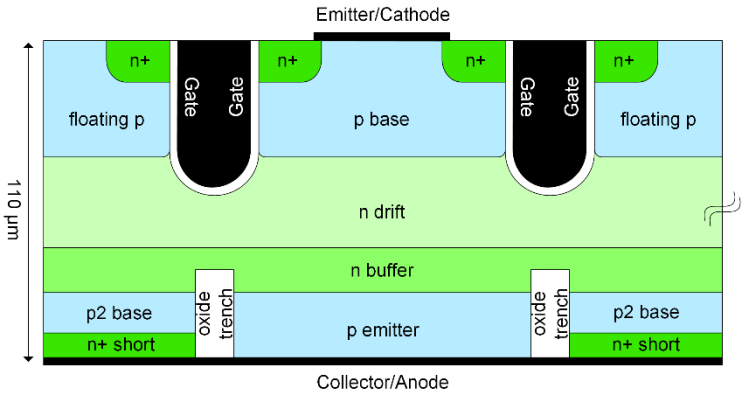


Figure 70 - Device structure of SH-RC-IGBT [126]

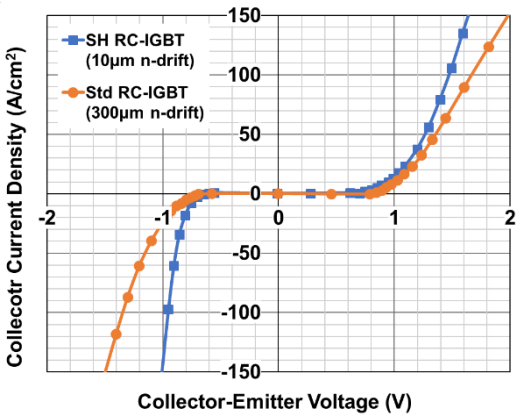


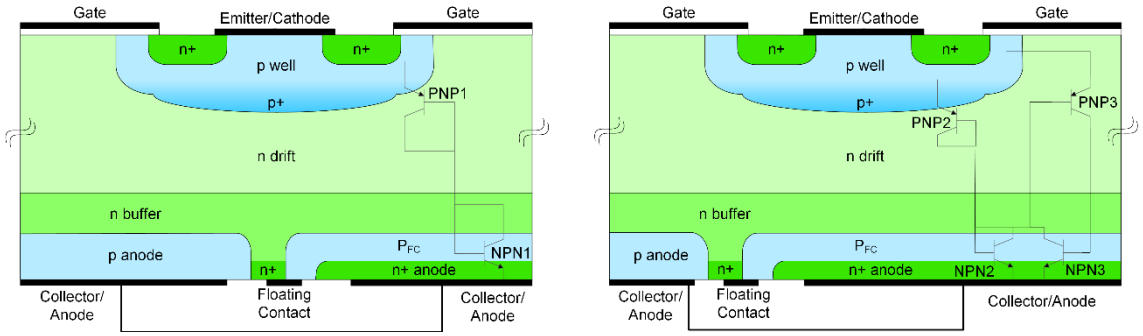
Figure 71 - Comparison of output I-V characteristics for SH-RC-IGBT and a conventional RC-IGBT [126]

During the reverse conduction state (Figure 71), the Shockley diode is easily triggered for low leakage current as the p2-base is lightly doped and has narrow width compared to the heavily doped n+ region. This therefore makes the current gain of the npn in diode mode close to 1. The simulated SH-RC-IGBT on-state characteristics in both conduction modes is better than the conventional RC-IGBT; in the forward and reverse direction on-state voltages reduced by 25% and 50% respectively. This is attributed to the SH-RC-IGBT eliminating the effect of the anode shorts in IGBT mode and therefore it has a significantly higher injection efficiency, whereas in diode mode, the device utilises the bottom chip area better. To eliminate the snapback characteristic, the SH-RC-IGBT requires a carrier lifetime less than 0.5μs and a 10μm wide drift region (300μm for a conventional RC-IGBT). As a result of the former, the Shockley diode requires a much higher current to be triggered, although the impact of this can be reduced by reducing the doping concentration of the p2-base. The device also has an improved current distribution which increases the SOA of the SH-RC-IGBT, but it suffers from a higher reverse-recovery charge (Q_{rr}) and longer delay in turn-off due to the higher injection efficiency which makes it unsuitable for higher frequency applications. Overall, however, the turn-off losses are expected to be less than a comparable RC-IGBT. Results are limited to simulation only. [126].

5.3.1.3 Pseudo-double anode RC-IGBT

A further variation upon the RC-IGBT with anti-parallel thyristor, the Pseudo-double anode (PDA-RC-IGBT) structure is shown in Figure 72, with two variations to provide diode and thyristor conduction. The P_{FC} region is short-connected with the n-buffer through a floating contact. Snapback is suppressed as, under forward conduction, the n+ anode and P_{FC} region are reverse biased and therefore make no contribution to current flow. When the structure is reverse biased ($V_{CE}<0$) the floating contact ensures that both bipolar transistors (pnp_1 and npn_1) are in a collector-base short-circuited configuration, such that electrically the device behaves as two series connected diodes under this condition. This does, however, result in a higher reverse voltage drop compared to a traditional RC-IGBT. For larger current density applications, the device can be modified to trigger the parasitic thyristor formed by pnp_3 and npn_3. Compared to the diode version, the thyristor has lower on-state voltage drop but has a negative resistance characteristic. The PDA-RC-IGBT has a recombination current in the forward conduction state which

reduces the overall injection efficiency of the device, but has a significantly more uniform current distribution for both diode and thyristor versions which increases the SOA of the device. [127].



(a) (b)

Figure 72 - PDA-RC-IGBT structure. (a) Diode version. (b) Thyristor version. [127]

5.3.2 Complex Backside Processing

5.3.2.1 RC-IGBT with floating p-region

Figure 73 shows a schematic cross-section of the RC-IGBT with floating p-region structure. An oxide trench is present at the collector/anode of the device, with a floating p doped region, p-float, located between the n-collector and the n-drift. The p-float region begins at a distance L_g from the edge to the device. The FWD structure is achieved via p-body, n-drift, n-buffer and n-collector on the extreme left of the schematic. At large currents, the npn transistor, formed by n-collector, p-float, n-drift, can become activated to provide a low-impedance current path (the emitter for the forward and reverse conduction is the n-drift and n-collector respectively). For small currents, the p-float acts as a barrier to electrons, which together with the oxide trench forms a high-resistance collector short path suppressing the snapback characteristic. The turn-over voltage for the snapback is given by Equation 11, showing that increasing the collector-short resistance reduces the effect of snapback. [121].

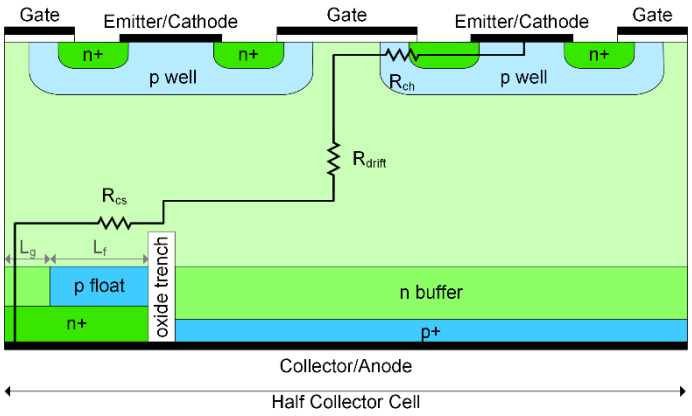


Figure 73 - RC-IGBT with floating p-region device structure [121]

$$V_{SB} = \left(1 + \frac{R_{drift} + R_{ch}}{R_{CS}}\right) V_{cr}$$

Equation 11 - Snapback turnover voltage, terms referenced to Figure 73 (V_{cr} voltage drop across p-collector/n-buffer junction when bipolar conduction begins, R_{CS} collector short resistance, R_{drift} drift region resistance, R_{ch} resistance of MOSFET channels) [121]

Simulation results have shown that by increasing L_F the snapback can be reduced and ultimately eliminated under certain conditions even at -40°C. In practice, however, L_F is reduced to achieve a better trade off in performance; smaller L_F has lower turn-off losses but increased forward voltage drop. With this optimisation, it is reported that the proposed RC-IGBT turn-off time is reduced by 21% compared to a conventional RC-IGBT or 27% compared to a Soft Punch Through or Field Stop IGBT (SPT-IGBT/FS-IGBT), which is attributed to the small collector cell length and the action of the npn transistor. [121].

A similar structure utilising the p-plug concept has been proposed (Figure 74). This device has an improved current distribution but suffers from the snapback effect. By reducing the non-uniform current distribution typically found in RC-IGBTs, the likelihood of local hotspot formation (and ultimately the destructive failure of the device) is lowered. The introduction of the p-plug in the n-buffer layer above the oxide trench, means that the electron path in the n-buffer is blocked (in the x direction, Figure 74), such that the device can be split into two discrete parts (IGBT and diode) unlike a conventional RC-IGBT. The device can be optimised to maximise the conduction volume in each mode, with simulations reporting 90% utilisation in IGBT mode (75% for a standard RC-IGBT and 35% for bi-mode insulated gate transistor (BIGT)) and 60% in diode mode

(30% for a standard RC-IGBT and 27% for BIGT). This increased the reliability of the proposed device, but, in turn, did induce a larger snapback characteristic [117].

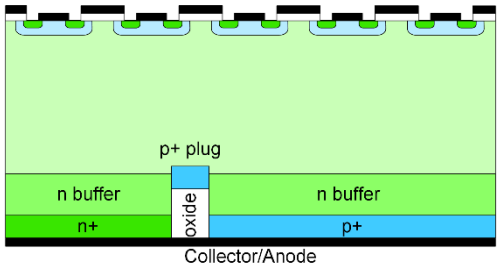


Figure 74 - RC-IGBT with floating p-plug situated on top of an oxide trench in the n-buffer layer [117]

Figure 75 shows the Carrier Stored Floating P-region Reverse Conducting IGBT (CSFP-RC-IGBT). This device contains a n doped charge stored (CS) layer between the p-well and the n-drift region, which is comparatively more doped than the drift region. The addition of this layer reduces the on-state voltage drop in IGBT mode and, with increased doping density, reduces the on-state resistance compared to a standard RC-IGBT with p-float but increases the turn-off losses slightly. The concept of CS was also described in the HiGT structure from Hitachi [77] and the SPT+ structure from ABB [128] (Section 1.5.4). For increasing carrier concentration in the CS layer, the I-V characteristic tends towards a PIN diode, however the breakdown voltage of the device is reduced. There were no reported results regarding the performance of the reverse conducting diode, however, given the increase in carriers at the cathode, the performance is expected to worsen. [129].

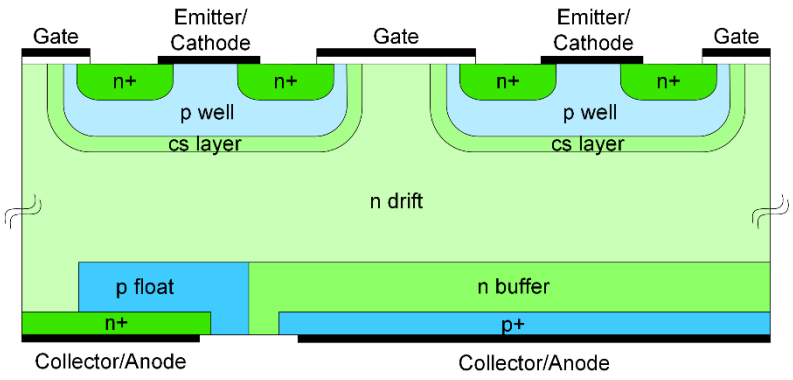


Figure 75 - CSFP-RC-IGBT structure [129]

Fabrication of these structures are complex and costly due to the requirement for backside photolithography and the non-uniform current distribution in both conduction states. As a consequence, these results are limited to simulation only [118].

5.3.2.2 RC-IGBT with Alternating N/P Buffers (AB RC-IGBT)

The Alternating Buffer Reverse Conducting IGBT (AB RC-IGBT), shown in Figure 76, has a similar structure to a conventional RC-IGBT with the addition of a buffer layer with alternating n and p implants. These implantations are several micrometres above the collector. In this device, the p buffer acts as an electron barrier, forcing the electrons to flow through the high resistance n-drift region between the buffer and collector. Figure 77 compares the on-state performance of the AB RC-IGBT to the RC-IGBT with floating p-region (Figure 73) and a conventional RC-IGBT. For a collector length (L_C) 30µm, the AB RC-IGBT can eliminate snapback entirely, whereas a collector length of 80 µm is required for the RC-IGBT with floating p-region to eliminate snapback: shorter devices are more desirable to reduce the current crowding at the anode short during reverse conduction. [130].

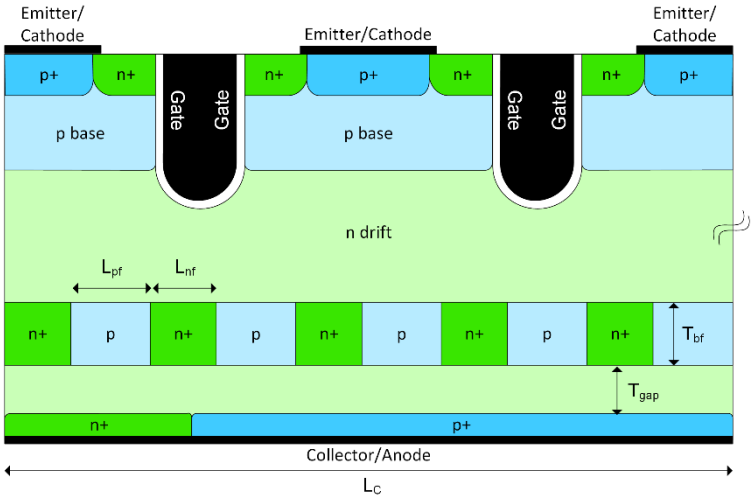


Figure 76 - Alternating Buffer (AB) RC-IGBT [130]

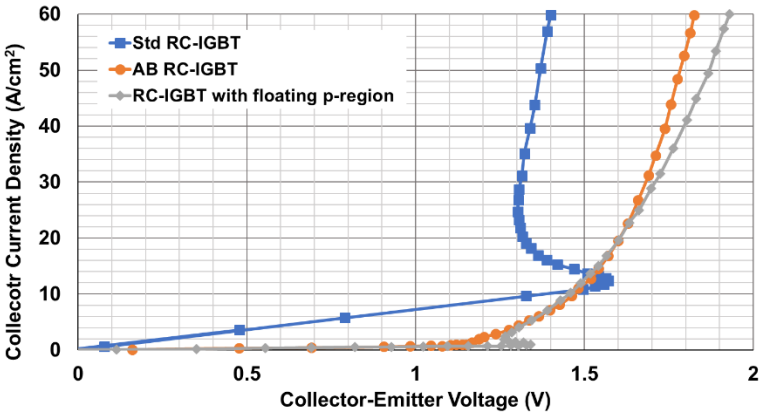


Figure 77 - I-V characteristic of AB RC-IGBT (L_C (collector length)=30µm, L_P (p+ length)=25µm), RC-IGBT with floating p-region (L_C=30µm, L_P=25µm) and a conventional RC-IGBT (L_C=300µm, L_P=295µm) [130].

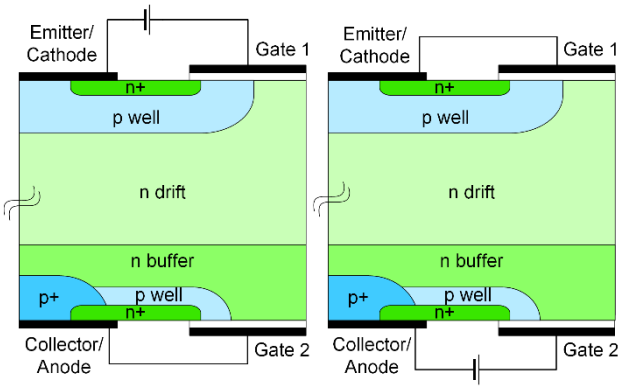
This snapback suppression is achieved by increasing the relative implant width of the p buffer region (L_{pf}) compared to the n+ buffer (L_{nf}) to increase the barrier to electron flow. However, the AB RC-IGBT structure has a parasitic pnp transistor, formed between the p+ collector/n-drift/p buffer. Base punch through of this parasitic transistor compromises the blocking capabilities of the device which becomes increasingly significant for wider p buffer implants. Wider p buffer regions also result in larger switching losses as the p buffers obstruct extraction of excess carriers in the drift region during turn-off. However, the AB RC-IGBT is still a 20% improvement on a conventional RC-IGBT for a device with the same IGBT on-state voltage. Increasing the thickness of the buffer layer (T_{bf}) also helps supress snapback by shielding electrons in unipolar mode, but this in turn reduces injection efficiency and increases the on-state losses during IGBT conduction. [130].

5.3.2.3 RC-IGBT with double gate structure

The Dual-Gate Bidirectional IGBT (BD-IGBT or DGIGBT) was first proposed by Nakagawa in 1988, demonstrating the device's potential using simulation results [131]. Fabrication techniques to realise this structure have followed and in 2014 a 1200V 25A single-chip dual-gate BD-IGBT was manufactured with a fusion wafer bonding process [132]. However fabrication of IGBTs with lower breakdown voltages using this method have resulted in less than ideal electrical performance [132].

The structure of the BD-IGBT is shown in Figure 78. This structure inherently has a reverse conducting diode: in the forward conduction mode, with gate 2 shorted and gate

1 positively biased, normal IGBT conduction occurs, whereas with gate 2 forward biased and gate 1 shorted a forward voltage blocking state is provided alongside a reverse conduction path, thus serving the same function as a FWD [131]. Turn-off losses are smaller than a standard FS-IGBT as an anode short is effectively realised when an n-channel is formed underneath a positively biased gate, resulting in a shorter turn-off irrespective of carrier lifetime within the device [131], [133]. Due to the structural symmetry, the forward and reverse conduction behaviour is the same, with the I-V characteristic 180° symmetric about the origin [133].



(a) (b)

Figure 78 - BD-IGBT device structure. (a) Forward conduction mode. (b) Reverse conduction mode [131]

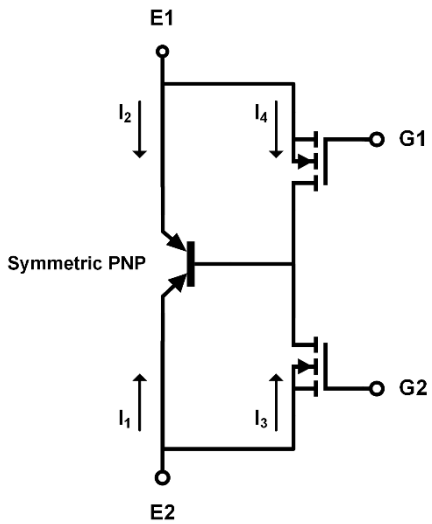


Figure 79 - Equivalent circuit of BD-IGBT [133]

Operation of this device is, however, complicated. There are four modes of operation, with their conditions summarised in Table 3 in relation to the equivalent circuit shown in Figure 79. A quasi-IGBT mode can be achieved when both gates are positive, as the hole injection efficiency of the backside p-well (in either conduction direction) is reduced by the presence of the parallel MOS channel [133]. It is also possible to exhibit MOSFET behaviour when the current is lower than a threshold value I_H (typically ~4A/cm^2) such that the backside p-well is biased by <0.7V so hole injection does not occur. It is this transition from MOSFET mode to quasi-IGBT mode which exhibits the snapback characteristic in the I-V curve, however, in this quasi-IGBT mode much higher switching speeds can be achieved than in the IGBT mode [133] and higher back-gate voltage reduces the susceptibility of the breakdown voltage and leakage currents with temperature [132]. It has been reported that multifaceted gate driving schemes can be implemented to optimise the switching and on-state losses of the device for various applications [133]. However, this makes it undesirable for use within the majority of commercial circuits due to the increased cost and complexity of driving two gates for a single switch.

Mode	Gate Biasing	I_E	
		Component	Range
I: IGBT	$V_{G1E1} > V_T$, $V_{G2E2} = 0$	$I_E = I_1$	$I_E > 0$
	$V_{G1E1} = 0$, $V_{G2E2} > V_T$	$I_E = I_2$	$I_E < 0$
II: Quasi-IGBT	$V_{G1E1} > V_T$, $V_{G2E2} > V_T$	$I_E = I_1 + I_3$	$I_E > I_H$
	$V_{G1E1} > V_T$, $V_{G2E2} > V_T$	$I_E = I_2 + I_4$	$I_E < -I_H$
III: MOSFET	$V_{G1E1} > V_T$, $V_{G2E2} > V_T$	$I_E = I_3$	$0 < I_E < I_H$
	$V_{G1E1} > V_T$, $V_{G2E2} > V_T$	$I_E = I_4$	$-I_H < I_E < 0$
IV: Blocking	$V_{G1E1} < V_T$, $V_{G2E2} < V_T$	$I_E = 0$	$I_E = 0$

Table 3 - Operation modes of BD-IGBT [133]

To be more favourable to a larger range of applications, the Automatically Controlled Gate RC-IGBT (AG-RC-IGBT, Figure 80) has been proposed [71]. The structure is similar to that given in Figure 78 except that the anode gate (gate 2) is connected to the n+ region within the n-buffer through an ohmic contact. In this device, the voltage of gate 2 is lower than that of the anode in forward conduction mode and therefore snapback does not occur [71]. In reverse conduction mode, when a voltage is applied to the anode, the capacitance of gate 2 is charged through the floating n+ region (that the gate has an ohmic contact with) until the threshold voltage is achieved and a reverse conduction path is provided. The device suffers from a higher on-state resistance compared to a conventional RC-IGBT [71]. The doping of the p2 base is reduced for faster charging of the gate and to enable the device to operate at higher switching speeds and lower anode voltages, however, this in turn reduces the injection efficiency of the anode in the forward conduction state [71]. With some optimisation, it is possible to trigger the thyristor structure (p+ region (top), n-drift/n-buffer, p2-base, n+-region) to form a MOS-controlled thyristor (MCT) in the reverse direction. This structure has a lower on-state resistance making it more suitable for higher current densities, but the snapback phenomenon re-emerges in both conduction directions, presenting an issue if the device is paralleled [71]. In both variations of the AG-RC-IGBT, the non-uniformity of current distribution in the volume of silicon can lead to localised hot-spots, limiting both the current capability and reliability of the device [125]. There has been no reported experimental data for the AG-RC-IGBT.

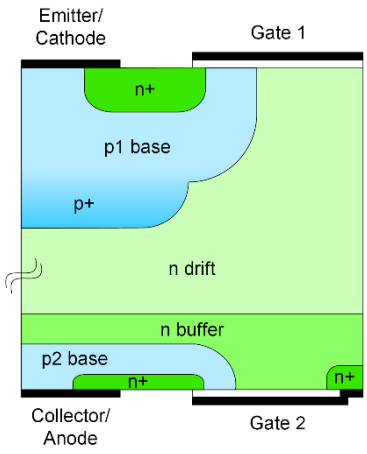


Figure 80 - AG-RC-IGBT structure [71]

5.3.2.4 Tunnelling injection IGBT (TIGBT)

An alternative concept for the RC-IGBT is the Tunnelling Injection IGBT (TIGBT), shown in Figure 81, which uses band-to-band tunnelling to overcome the known issues with the traditional RC-IGBT. A highly doped (10^{19} cm^{-3}) n-tunnel layer is sandwiched between the p++ collector and the n-buffer. The band diagrams of these layers under a range of conditions is shown in Figure 81. For forward conduction, the collector (anode) and the gate are positively biased, and there exists a common band of energies such that electrons can tunnel from the n-tunnel into the p++ collector. The device exhibits a snapback characteristic since for increasing collector voltage the tunnelling current decreases after reaching a peak value. This peak current exponentially increases with the decrease in the barrier width which is dependent upon the doping concentrations. It is possible to remove this snapback by increasing the doping concentration of the n-tunnel and p++ collector but at the expense of the diode mode conduction losses. [118].

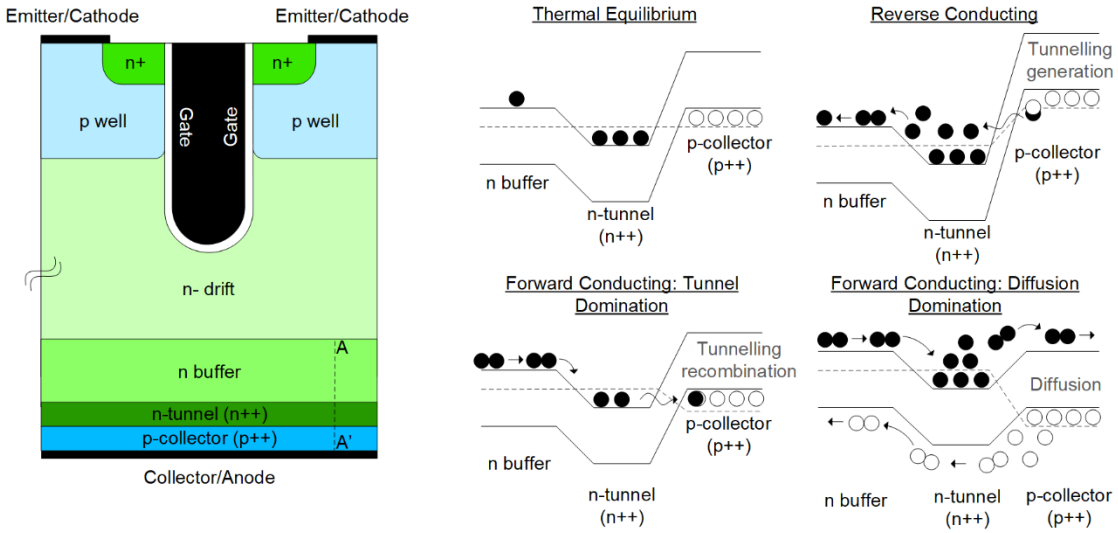


Figure 81 - TIGBT structure (left) with energy band diagram taken along cutline A-A' at thermal equilibrium, reverse conducting (gate zero biased and collector positively biased), and forward conducting (gate biased to 15 V and collector negatively biased) [118]

In the reverse direction, the device is equivalent to a PIN diode in series with a backward tunnel injection; with the collector negatively biased and the gate zero biased, electrons can inject via band-to-band tunnelling from the p-collector into the n-tunnel layer. In diode mode, the TIGBT exhibits a soft recovery as electrons extracted through tunnelling across the n-tunnel/p++ collector junction induces hole injection into the n-drift which

results in a small reverse recovery and minimal voltage overshoot. However, these injected holes attract electrons to maintain charge neutrally in the drift region which need to be extracted from the p-body to the emitter. This induces a relatively long current tail in the turn-off which is undesirable in high frequency applications. The TIGBT conducts uniformly across the device region (unlike a standard RC-IGBT) and therefore the device has a smaller turn-on voltage at low currents and the reverse recovery peak currents are reduced. The device also has the advantage over the other concepts that the fabrication method does not need to allow for non-uniform current distribution nor require backside photolithography, which is a complex and expensive fabrication process. However it is very difficult to produce a very thin n-tunnel layer with such high doping as required for the TIGBT. [118].

5.3.3 Pilot Structures

5.3.3.1 BIGT (Bi-mode Insulated Gate Transistor)

The BIGT was first proposed in 2009 by ABB Semiconductors, and consists of a hybrid structure of an IGBT (referred to as a pilot-IGBT) and RC-IGBT integrated into a single device as shown in Figure 82 [115]. The initial prototype device was a 3300V module, but in 2013 a 6500V HiPak module was produced [109]. The overall module performance (output current) of the BIGT compared to a separate IGBT/diode solution is up to 15% higher [134].

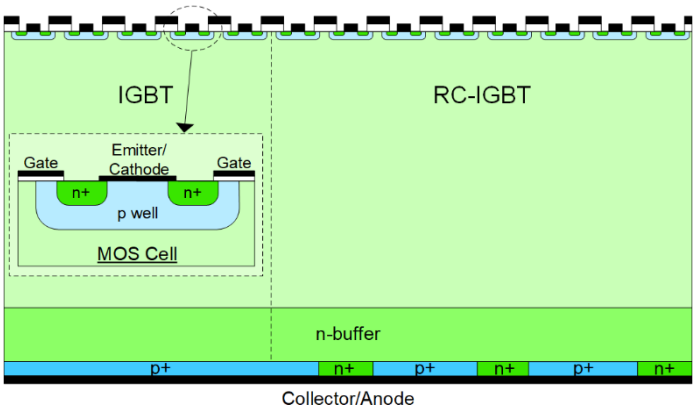


Figure 82 - BIGT structure [115]

The pilot-IGBT is sized to reduce the snapback in the forward conduction mode at low temperatures [115]. The device has, however, suffered from secondary snapbacks due to plasma formation primarily limited to the IGBT region with only a small section of the RC-IGBT area being conductivity modulated [135]. In order to utilise the full device area through the lateral expansion of the plasma area towards the RC-IGBT area, a radial layout of the anode shorts is used. This achieves the optimum trade-off in diode and IGBT conduction losses while eliminating this secondary snapback [135]. It also results in the on-state characteristics being less sensitive to the n buffer doping, therefore providing another degree of freedom to optimise the device for high temperature operation [135].

Reduction in the reverse recovery losses in the diode while minimising the impact on the on-state performance in the forward direction is achieved by;

1. Finite control of the doping profile of the cathode (emitter) p-well and the cathode (collector) p+/n+ regions
2. Local p-well Lifetime (LpL) control through particle implantation
3. Uniform local lifetime control through proton irradiation [115]

The impact of these steps is shown in Figure 83. The finite control of the p-well results in a worsening of performance of the individual device under surge, however in typical applications where multiple devices are paralleled into a single BIGT module, this is compensated by the increased silicon area such that the overall surge capability remains constant [109]. It was reported that as a result of performing the uniform local lifetime control, the forward conduction mode on-state voltage increased by 300mV to 3.3V at 125°C [115]. However, a 10% reduction in the diode mode reverse recovery and IGBT mode turn-on losses are obtained when MOS Control Diode function is utilised [115], [116]. This increase in the conduction losses limits the output current capability of the device at low frequencies [109], and the on-state voltage drop in diode mode (reverse conduction) is relatively high at 3.0V at 125°C [115].

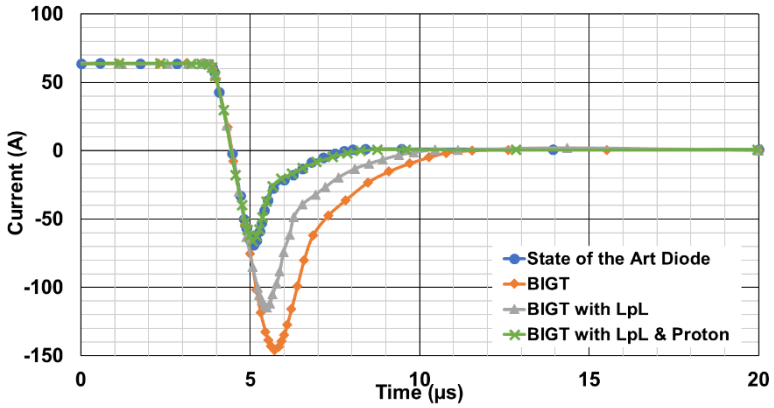


Figure 83 - Nominal reverse recovery currents for 3.3kV/62.5A BIGT operating in diode mode, showing reverse recovery at 1800V, 62.5A (150A/µs), 125°C [115]

The gate voltage has a strong influence on the reverse conduction losses during diode mode, as it affects the plasma shape near the emitter by causing the shorting of the RC-IGBT/BIGT MOS cells p-wells which are functioning as the anode regions of the diode [109], [136]. As a result, the gate voltage is required to be below the MOS channel threshold so that p-well injection remains high [109], [136]. The optimum control has the channel off during diode conduction mode, with it turned on towards the end of the diode conduction time, before being turned-off again prior to diode reverse recovery to prevent a short circuit [134]. As a consequence of this complex gate drive scheme to prevent unnecessarily high conduction losses and to optimise switching performance, operation of the device is more complex, making it less attractive to application circuit designers [109]. It has been acknowledged that it is this requirement for a custom gate drive scheme that is one of main obstacles preventing the BIGT from being adopted in mainstream applications [136].

The device exhibits a strong positive temperature coefficient in both modes thus making it suitable for paralleling in modules to achieve higher operating powers [115]. The SOA of the BIGT is not compromised but the temperature ripple is reduced as the same volume of silicon is heated during both IGBT and diode mode, therefore increasing the reliability of the device [109], [115]. Switching losses are comparable to SPT IGBT/diode modules but the BIGT does not show oscillations or voltage overshoot caused by current tail snap-off [109], [115]. The BIGT has softer turn-off behaviour in both conduction modes compared to state of the art IGBT and diode modules due to the presence of injected holes and charge extraction (Figure 84) [115].

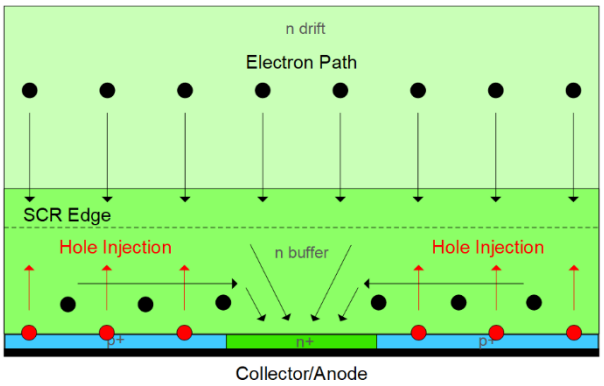


Figure 84 - BIGT anode (collector) charge extraction concept [115]

The Enhanced Trench Bi-mode Insulated Gate Transistor (ET-BIGT) is a further development of the BIGT concept. The enhanced trench (ET) structure, shown in Figure 85, reduces conduction losses in the IGBT mode (Figure 86) by enhancing the excess carrier concentration at the MOS cell structure [137]. It also provides improved controllability while extending the maximum junction temperature rating [137]. The ET-BIGT addresses the requirement on the BIGT that the gate voltage should be less than a threshold during diode conduction to reduce on-state losses [109]; the ET design was optimised for reverse mode conduction losses under positive gate biasing conditions for ease of control and to maintain good surge capability [137]. Initial results have shown that without MOS gate control the ET-BIGT can achieve lower switching losses compared to the Enhanced Planar BIGT, but the trench cell does suffer from a higher diode on-state forward voltage when a positive gate emitter bias is applied [137].

Figure 87 shows the introduction of a pilot diode perpendicular to the gate/emitter trenches. Trench cell concepts in RC-IGBTs have a stronger gate shorting effect compared to the lateral gate on a planar cell; in the case of the latter, there is a relatively high diode hole injection at the centre of the p-well under the contact [137]. Therefore, to implement an enhanced trench structure within an RC-IGBT, a pilot diode is required to achieve low conduction losses under positive gate bias [137]. Results have indicated that the pilot diode region does not affect the performance of the ET cell if the dimensions between the repetitive pilot diode regions are large, however it does give a higher forward voltage drop in diode mode [137].

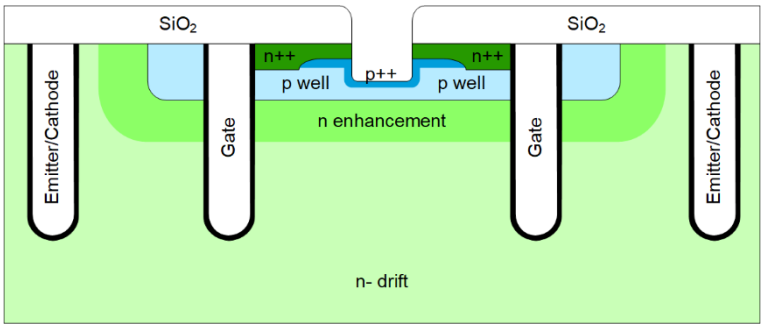


Figure 85 - Enhanced Trench MOS cell structure [137]

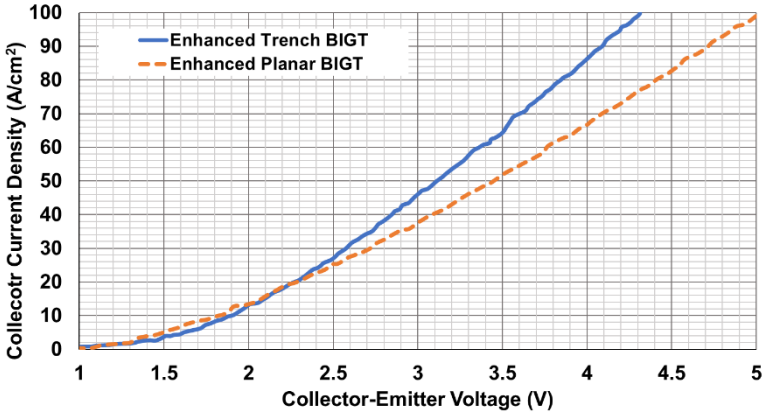


Figure 86 - Comparison of on-state voltage drop for Enhanced planar BIGT and Enhanced Trench BIGT [134]

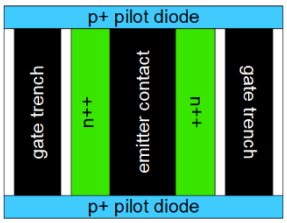


Figure 87 - ET-BIGT showing pilot diode position [137]

Further research has focussed on optimising the ET-BIGT with pilot diode to eliminate the need for complex gate drive schemes: the on-state losses while operating in diode mode under positive gate bias, are significant [136]. Three main approaches were taken [136];

1. Use of a period n+ source region to minimise the gate shorting effect (Figure 88)
2. Increasing the p+ pilot diode implantation dose
3. Optimising the n+ anode shorts by high temperature annealing to increase injection efficiency

Despite the improved diode on-state performance, the use of a periodic n+ source region results in a slight increase in V_{CE} due to the larger cell pitch, which becomes increasingly prominent in high voltage devices [136]. Increasing the p+ pilot anode dose increases the reverse recovery losses and optimising the anode short presents the classic trade-off between diode mode on-state performance and reverse recovery losses [136]. Despite

reducing the forward voltage drop of the diode by 1.2V compared to the reference BIGT under +15V gate bias condition, the new BIGT suffers from a 21% increase in diode recovery losses and an 11% increase in IGBT mode turn-on losses at 150°C [136]. This indicates that this optimised version of the device is only suitable at low switching frequencies (<500Hz) and that different design trade-offs should be chosen for applications where the BIGT is required to switch faster [136].

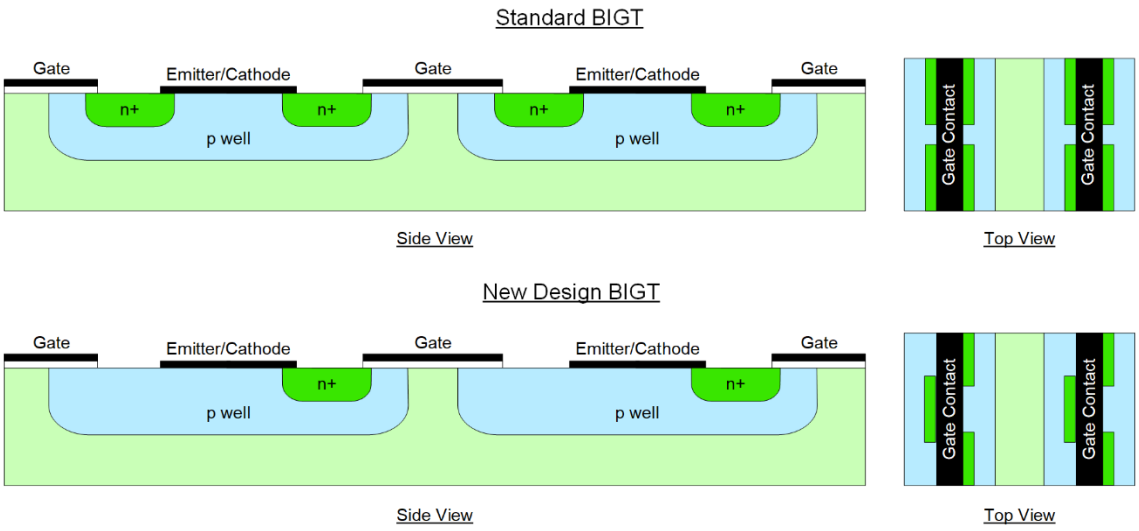


Figure 88 - BIGT n+ source adaptations comparing standard symmetric MOS cell and new periodic MOS cell design [136]

5.3.4 Other Concepts

5.3.4.1 RC-IGBT with superjunction structure

The majority of RC-IGBT development has focussed on the anode structure, however, the Trench Field Stop Superjunction RC-IGBT (TFS-SJ-RC-IGBT) (Figure 89) instead employs a superjunction structure at the cathode and utilises traditional anode shorts to provide the reverse conduction path [66], [108]. It should be noted that the length of the p-pillars in the superjunction structure do not extend all the way through the device; the p-pillar length (Ymid) is considerably smaller than the total length of the drift region, resulting in the device often being referred to as a semi-superjunction structure.

In the conventional RC-IGBT structure (and ordinary IGBT), the resistance of the n−drift region ($R_{n\text{-}drift}$) is determined by the thickness and doping of the region, which is limited

by the breakdown rating of the device. Employing the superjunction structure within the RC-IGBT allows the n-drift doping to be increased by several orders to magnitude without impacting the breakdown voltage, thus reducing the drift region resistance significantly. In fact, in the SJ structure the drift region resistance is dependent on the length of the pillar Ymid as it is the sum of the n-pillar resistance and the remaining drift region resistance. By increasing Ymid, the snapback voltage is reduced and is eliminated at 360µm even at low temperatures (Figure 90). For a TFS-SJ-RC-IGBT, which is comparable with a CoolMOS structure (3 x 10^{15} cm^{-3} p-pillar doping and Ymid=70µm), the switching losses of the proposed device are lower than a standard RC-IGBT, however a snapback is present in the I-V characteristic. Increasing Ymid to achieve a deep superjunction results in an initial increased gate capacitance, which decreases rapidly, and therefore enhanced ringing is present in the switching waveforms, which can result in worse switch-off losses compared to a NPT-IGBT [66], [69]. Increasing the doping concentration of the pillars is also detrimental to turn-off of the device as the depletion region expansion is slower [138]. The diode reverse recovery characteristic is, however, unaffected by the superjunction structure [138].

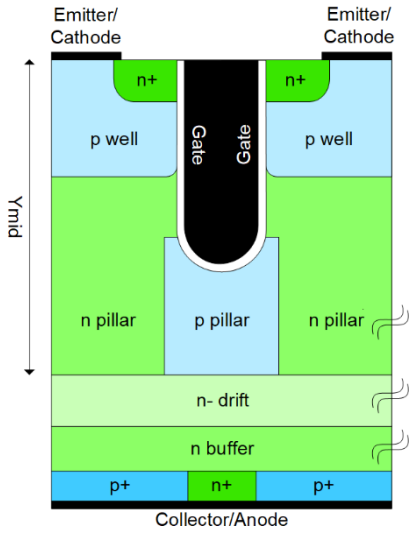


Figure 89 - TFS SJ RC IGBT [66]

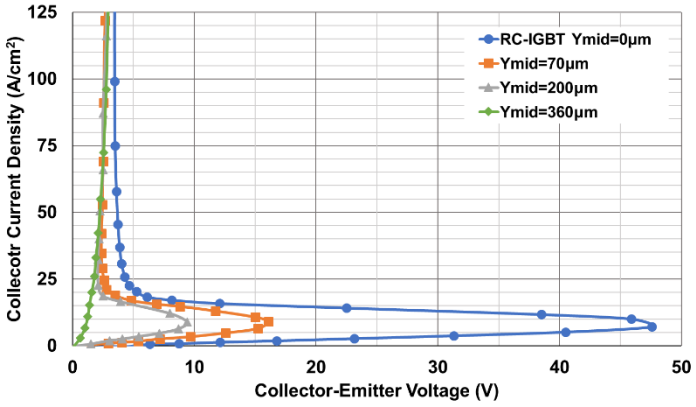


Figure 90 - ON-state characteristics for a 3.3-kV TFS RC SJ IGBT p-pillar, doping concentration 3×10^{15} cm^{-3} for Ycell equal to 370 µm for varying Ymid (0–360µm) [66]

More recent studies have focussed on the possibility of applying the superjunction to the anode side [70], similar to the Alternating Buffer Reverse Conducting IGBT concept [130], as discussed in Section 5.3.2.2. In this alternative SJ device, it was shown that pillar location is independent of the features of the cathode, thus making processing simpler as there is no need for alignment [70]. It also decouples the anode design from the cathode enabling the designer to better control the saturation current and short circuit capability [70], and has the advantage over the AB RC-IGBT that the n/p pillars in the SJ device do not also need to be optimised for breakdown capability [82]. Similar improvements in snapback was reported for this anode SJ implantation, but, as for the cathode-side SJ device, to remove the snapback entirely the SJ implant has to extend through the entire drift region, which cannot be manufactured using current techniques [70]. For the superjunction devices, state of the art fabrication techniques limits a pillar length to 65µm [68], so from a single deep SJ trench it is not possible to achieve a full SJ structure in the drift region of a 1.2kV IGBT.

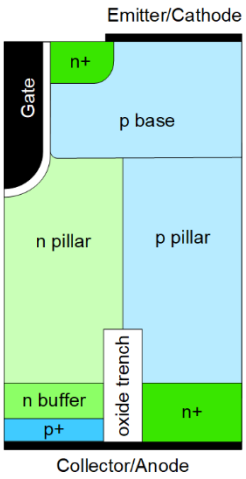


Figure 91 - SJ RC IGBT with trench oxide [139]

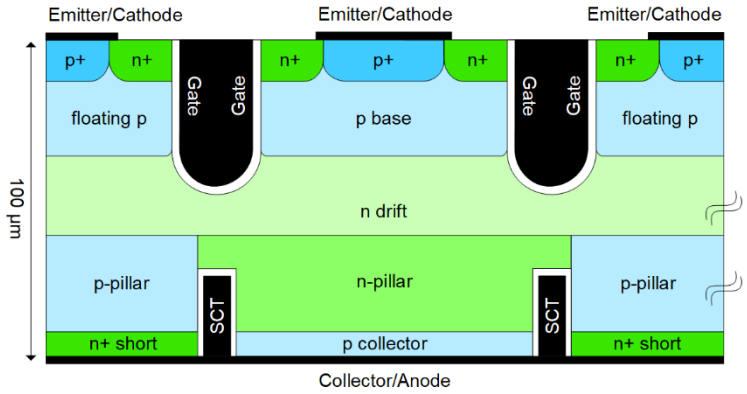


Figure 92 - RC-IGBT concept with anode-side SJ trenches and shorted collector trenches (SCT) [140]

A further adaptation of the structure given in Figure 89 is shown in Figure 91. The paper reports simulation results showing the improved performance of the SJ-RC-IGBT compared to the two-device alternative, however there is no data comparing it to the TFS-SJ-RC-IGBT [139] and this alternative structure suffers from the same manufacturing issues.

Most recently the anode-side SJ concept has also been proposed with the integration of shorted collector trenches [140], resembling Figure 91 and is very similar in structure and operation to the RC-IGBT with anti-parallel Shockley diode (Section 5.3.1.2), but with the oxide trenches at the bottom shorted to the collector (shorted collector trench, SCT). This device is shown schematically in Figure 92. This concept achieved snapback free operation with a cell pitch of 8µm, compared to 160µm for the RC-IGBT with floating p-region (Section 5.3.2.1) and 800µm for the conventional RC-IGBT [140]. Improvements in turn-off losses compared to these two other concepts were demonstrated, however, there was a significant increase in the delay before turn off of the device (before V_{ce} increased), which would limit the maximum frequency of operation of the device, and the high di/dt makes the device susceptible to ringing with any stray inductance. Also, like all the concepts discussed in Section 5.3.2, this new RC-IGBT concept has very complex fabrication requirements; the SJ structure is limited to 65µm deep [68], there is a need for a trench on both the front and the backside, and a high alignment precision is necessary between the trench and the superjunction pillar to avoid re-emergence of the snapback characteristic.

The majority of investigations for the SJ-RC-IGBT structure have been simulation based due to the nature of manufacturing IGBTs using Field Zone (FZ) wafers and the concern regarding the creation of voids within the structure [69]. Experimental results for the SJ-SPT IGBT and SJ NPT IGBT were reported validating the simulation models and indicating that the switching losses of the SJ NPT IGBT were lower than the SJ SPT IGBT. The SJ NPT has better short circuit ruggedness, but both exhibit superior on-state and switching performance compared to a traditional SPT IGBT [69]. The results highlight that the trade-off between the forward and reverse conduction capabilities in the superjunction design is difficult to optimise [71].

5.3.4.2 Schottky Controlled Diode within RC-IGBT

The introduction of the Schottky controlled (SC) injection concept to the diode within the RC-IGBT was reported in 2016. The device structure is given in Figure 93, where the p+ base and p- anode are formed separately to reduce reverse recovery loss by suppressing carrier injection from the surface while the patterned cathode suppresses carrier injection from the backside. The partially formed p+ ohmic areas on the anode are based upon the SC concept and high dynamic ruggedness is achieved by connecting the internal electrode of the trench at the diode area to the emitter electrode. The peak reverse recovery current was reduced by 49% due to the introduction of the anode structure compared to a conventional RC-IGBT, and the cathode structure reduced the tail current, but there was increased ringing in the reverse recovery waveforms. The paper focuses on the diode performance and does not comment on the overall performance of the RC-IGBT. [141].

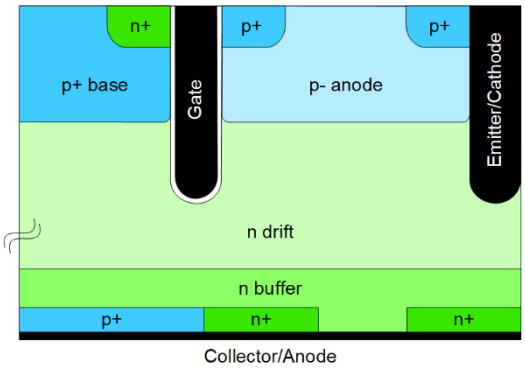


Figure 93 - Schottky Controlled RC-IGBT structure [141]

5.4 Comparison of RC-IGBT Concepts

2D simulations were undertaken in order to directly compare some of the RC-IGBT concepts. A 1.7kV 150A trench SPT IGBT structure was used for this analysis, based upon the structure developed in Section 3.4. The structure was modified to include an n+ anode short implant which covered 10% of the total collector area. This RC-IGBT structure has not been optimised but provides a benchmark for comparison. This device had a snapback voltage of 79.5V and a reverse conduction voltage drop of 3.66V at 50A.

Given the BIGT and RC-IGBT with double gate structure have been manufactured and experimental results have been published, they were not included in this simulation analysis. For this investigation the basic geometry of the IGBT cell and n+ implant was not modified, and the concepts were implemented in line with the original study. The RC-IGBT concepts which were considered are;

1. RC-IGBT with thyristor structure (thyristor based structure)
2. AB RC-IGBT (complex backside processing)
3. Tunnelling IGBT (complex backside processing)
4. TFS SJ RC-IGBT (other concepts)

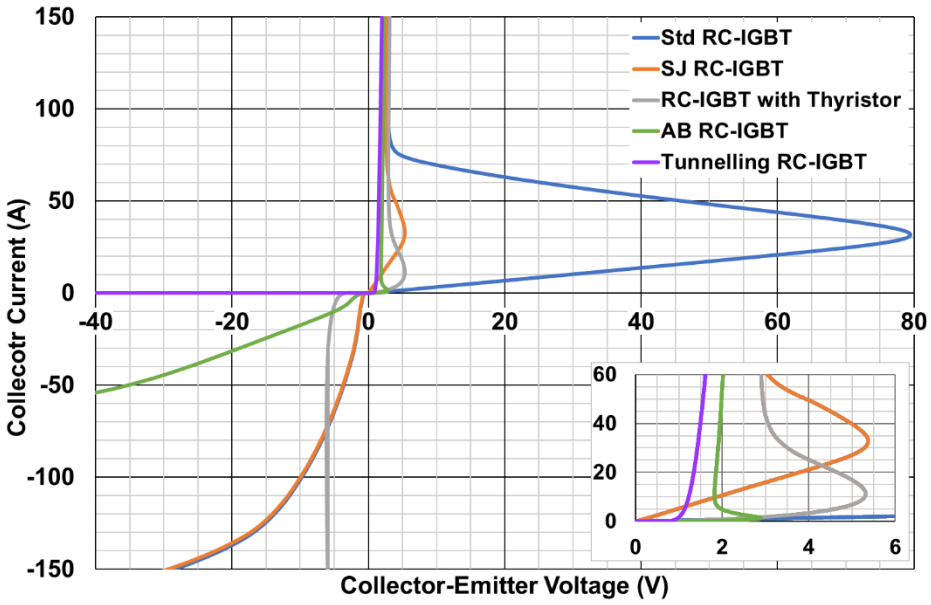


Figure 94 - Simulated on-state characteristics for RC-IGBT concepts, ambient temperature 298K

Figure 94 compares these concepts to the reference RC-IGBT. All concepts show considerable improvement to the snapback characteristic, but with varying impact on the reverse conduction performance.

The thyristor structure could have been optimised further to eliminate the snapback by reducing the depth of the p+ collector implants (4µm in Figure 94, with Dp=7µm), however this resulted in the device being unable to conduct in the reverse direction. In fact, the reverse conduction was very difficult to design and optimise, either introducing a secondary snapback as reported in the original study, or even a negative resistance characteristic as shown in Figure 94.

For the Tunnelling RC-IGBT, the n++ region was doped in line with [118] to 7e19cm^{-3}. For tunnelling to occur, the n++ depth could not exceed 0.28µm (Figure 94), which is unrealistic to manufacture given current fabrication techniques. For this IGBT cell geometry, the device showed minimal conduction in the reverse direction. Optimisation of this device is exceedingly difficult and, if it could be produced, would require a fabrication processes with very small tolerances.

The Alternating Buffer was designed with L_p=2µm, L_n=1µm, T_{gap}=8µm. The ratio of L_p/L_n was fixed at 2 in accordance with the study in [130]. This geometry produced minimal snapback in the forward conduction, but in the reverse direction the on-state losses increased by 91%. Figure 95 investigates the behaviour of the AB RC-IGBT with different features. Once again the ratio of L_p/L_n was fixed at 2 in accordance with the study in [130]. Figure 95 shows that doubling the number of buffer implants across the width of the device (L_p/L_n=2) reduced the snapback by 17% but increased the on-resistance in the reverse conduction by over 6 times. In addition, reducing the gap between the buffer layer and the p+ collector implant (T_{gap}) to 2µm eliminated the snapback in the forward direction but induced a large snapback in the reverse characteristic. The placement of the anode shorts is also critical to the success of this design; by moving the anode short from the centre of the cell to the edge, the snapback shown in Figure 95 is removed entirely as the lateral resistance along the p+ collector is increased, but this further increases reverse conduction losses, rendering the diode portion of the device unsuitable for use within typical application circuits. The AB structure replaces the traditional SPT buffer layer, and the design of this AB layer also needs to be optimised for the breakdown capability of the device. The complex requirements of this device makes the design and fabrication challenging.

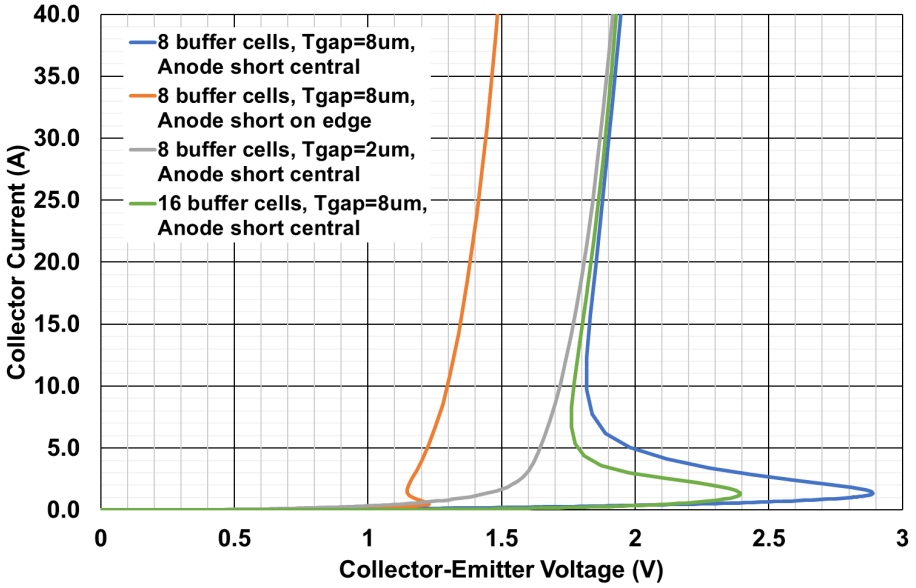


Figure 95 - AB RC-IGBT cell geometry comparison, Vg=15V, ambient temperature 298K

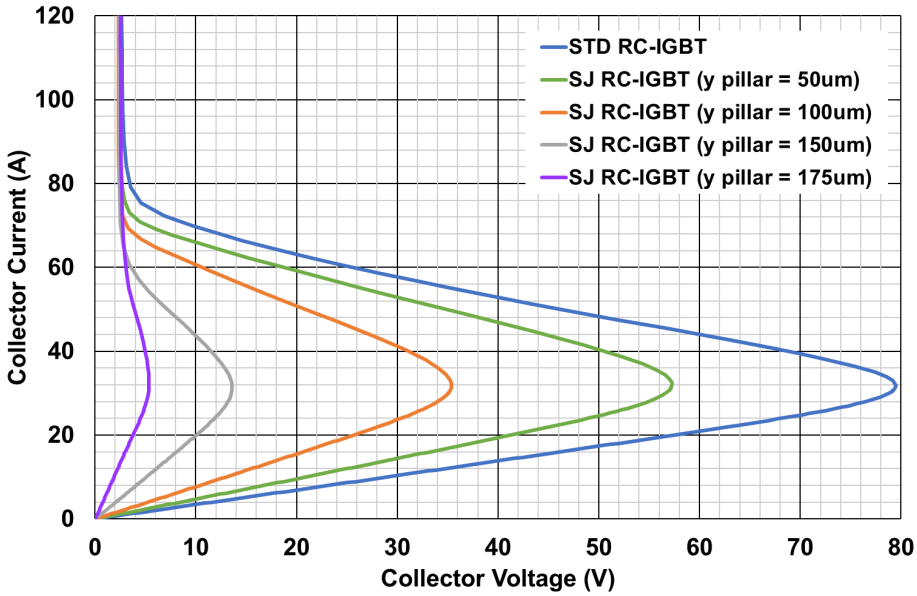


Figure 96 - Simulated on-state for TFS SJ RC-IGBT with varying pillar depth, ambient temperature 298K

For the SJ RC-IGBT, p-pillars were implanted under the gate trenches to emulate a more realistic fabrication. For increasing pillar depth, a reduction in the snapback occurs (Figure 96), with no effect on the reverse conduction performance as reported in [66], [108]. For the 1.7kV IGBT cell, the snapback could not be removed in its entirety due to the buffer design which limited the maximum pillar length to 87.5% of the total device

thickness (y pillar = 175μm, Figure 96). The original study in [108] reported elimination of the snapback but, to achieve this, had a buffer design which enabled the superjunction pillars to extend to 97.3% of the total device thickness. The buffer design is therefore critical to the performance of the SJ RC-IGBT, however the length of the required SJ pillars means that at present, this device would be very difficult to fabricate.

5.5 Conclusion

This chapter presents a review of the recent advancements of the RC-IGBT structure, outlining new concepts developed to overcome some of the technical design challenges of the traditional device. The RC-IGBT features an anti-parallel diode integrated within the same chip area which, at a module level, reduces the bill of materials, is a more compact design and ultimately has a lower cost. The first RC-IGBT structure introduced collector shorts, but optimisation of this implantation to give a good trade-off between the forward snapback and the reverse conducting characteristics is extremely challenging. The introduction of a pilot IGBT has been one of the most pragmatic solutions to resolve the snapback issue, whist still offering good reverse characteristics. Double gate structures have been hampered by the complicated gate drive requirements which have prevented their widespread use. Other solutions such as the trench oxide barriers, tunnelling devices, and complex buffer structures have also been proposed but at present have only been validated through simulations. Such structures may be too complex to be practical as they require advanced back-side processing of the silicon wafers. The SJ RC-IGBT concept also suffers with processing issues as the superjunction structure needs to extend deep into the drift region to give favourable trade-off characteristics. Nevertheless, it is one of the most promising solutions as it alleviates the snapback issue whilst also offering low switching losses both during forward and reverse recovery. Another promising concept to alleviate the snapback is to use a thyristor with very low breakover voltage instead of an anti-parallel diode. Whilst this eliminates the snapback in the forward mode it introduces a snapback in the reverse conduction mode which is difficult to control.

Despite these advancements, the RC-IGBT still has dynamic limitations particularly for high power applications, as there are conflicting requirements for the diode and IGBT in terms of their plasma distribution at the collector: high plasma concentration at the top of

the drift region (p-well) reduces the on-state losses in IGBT mode, but to minimise the reverse recovery losses and prevent EMC issues, a low plasma concentration is required during diode mode. The snappy behaviour of the diode can be controlled by a low circuit stray inductance or by reducing the IGBT turn-on di/dt, but this increases the IGBT turn-on losses. Local lifetime killing in the diode regions can improve performance, but for electron irradiation it is difficult to mask and therefore degrades the performance of adjacent IGBT cells. Separate diode and IGBT chips allow optimisation of each device independently, but the RC-IGBT offers improved utilisation of silicon area. The RC-IGBT may also have an advantage in terms of the IGBT leakage current; the leakage current amplification due to the pnp transistor gain is smaller as a result of the presence of anode shorts. This can result in lower off-state losses especially at high junction temperatures. No single solution to optimise all the static and dynamic trade-offs has emerged for the RC-IGBT but it is an active area of current research.

Chapter 6

Dual Implant SuperJunction Reverse-Conducting IGBT

It has been shown in the previous chapter that the RC-IGBT has the potential to become the dominant power device in a range of applications, which traditionally use a separate IGBT and diode co-packaged. However, as discussed earlier, the traditional RC-IGBT suffers from several undesirable characteristics and the various proposed concepts designed to alleviate these issues either present a trade-off in performance characteristics, an inability to be manufactured, or a requirement for a custom gate drive, which makes it undesirable to application engineers.

The superjunction (SJ) RC-IGBT is one of the most promising concepts, but to achieve the full performance benefits a deep SJ structure is required, which currently cannot be manufactured. This chapter presents a new novel device, the Dual Implant SJ RC-IGBT, that addresses these performance concerns associated with the traditional RC-IGBT but, critically, is manufacturable using current state of the art techniques. This new concept, for the first time enables a full SuperJunction structure to be achieved in a 1.2kV device.[1]

[1] The material in this chapter has been taken from the following publication:
E. M. Findlay, F. Udrea, and M. Antoniou, "Investigation of the Dual Implant Reverse-Conducting SuperJunction Insulated-Gate Bipolar Transistor," IEEE Electron Device Lett., vol. 40, no. 6, pp. 862–865, 2019, doi:10.1109/LED.2019.2911994

6.1 Introduction

In Chapter 5 it has been shown that the RC-IGBT structure, which integrates the diode structure within the IGBT by the addition of anode shorts (n+ regions) [71], [81], presents a number of advantages [82], [108], [111], [112];

1. An RC-IGBT uses less area than an equivalent IGBT and separate diode (>30% size reduction)
2. Reduction in assembly cost (bonding, packaging and less silicon area)
3. Reduction in wafer processing and testing cost
4. Lower thermal resistance and reduced temperature ripple as the same silicon volume is used during both diode and IGBT conduction modes
5. More degrees of freedom in package layout
6. Improvement in reliability due to fewer bond wires within a module (bond wires induce parasitic (inductive) effects)
7. More suitable for high junction temperature operation as the leakage current in IGBT mode is lower due to the presence of the anode shorts (reduced pnp transistor gain).
8. Possibility of using a suitable gate signal to allow better trade-off between the on-state voltage drop and the reverse recovery losses of the diode.

However, the RC-IGBT structure within high voltage, hard switching application suffers from several undesirable characteristics [82];

1. Snapback in the current-voltage characteristics is present (MOSFET shorting effect)
2. A trade-off between the IGBT on-state losses and the diode reverse recovery losses (plasma shaping effect)
3. Reduction in safe operating area (SOA) (charge uniformity effect)
4. A trade-off between the IGBT and the diode softness (drift layer effect)

To overcome these issues, the majority of RC-IGBT development has focussed on the anode structure, however, the Trench Field Stop Superjunction RC-IGBT (TFS-SJ-RC-IGBT) instead employs a superjunction structure at the cathode and utilises traditional anode shorts to provide the reverse conduction path [66], [108]. In the original study, the

p-pillars in the superjunction structure did not extend all the way through the drift region; the p-pillar length is considerably smaller than the total length of the drift region, resulting in the device often being referred to as a semi-superjunction structure [66]. For a TFS-SJ-RC-IGBT, which is comparable with a CoolMOS structure (3e15cm^3 p-pillar doping and pillar length = 70μm), the switching losses of the proposed device are lower than a standard RC-IGBT, however, a snapback is present in the I-V characteristic. By increasing the pillar length, the snapback voltage was shown to reduce and ultimately be eliminated at a pillar length of 360μm even at low temperatures [66], [108]. However, this deep superjunction structure results in an initial increased gate capacitance which decreases rapidly, and hence enhanced ringing is present in the switching waveforms, which can result in worse switch-off losses compared to a NPT-IGBT and also increased electromagnetic interference (EMI) [66], [69], [70]. Increasing the doping concentration of the pillars is also detrimental to turn-off of the device as the depletion region expansion is slower [138]. The diode reverse recovery characteristic is, however, unaffected by the SJ structure [138]. As reported in literature and the results in Chapter 5, Section 5.4, simulations have demonstrated the benefit of extending the SJ pillars further into the drift region to remove the snapback, but this device is not currently manufacturable.

More recent studies have focussed on the possibility of applying the superjunction structure to the anode side [70], similar to the Alternating Buffer Reverse Conducting IGBT (AB RC-IGBT) concept [130]. In this alternative SJ device, it was shown that pillar location is independent of the features of the cathode, thus making processing simpler as there is no need for alignment during processing [70]. It also decouples the anode design from the cathode enabling the designer to better control the saturation current and short circuit capability [70], and has the advantage over the AB RC-IGBT that the n/p pillars in the SJ device do not also need to be optimised for breakdown capability [82]. However, the presence of the pillars at the buffer resulted in an increase in the electric field at this boundary which resulted in punch-though the of the device. To counteract this the buffer doping needs to be increased which reduces the injection efficiency of the p-anode, which also needs to be compensated for. Similar improvements in snapback has been reported for this anode SJ implantation, but, as for the cathode-side SJ device, to remove the snapback entirely the SJ implant had to extend through the entire drift region, which cannot be manufactured [70]. For the AB RC-IGBT the snapback can also be supressed by increasing the relative implant width of the p buffer region compared

to the n+ buffer, but this significantly compromises the blocking capabilities of the device and increases switching losses. This makes the buffer design particularly hard to optimise, as discussed in Chapter 5.

In the case of the superjunction devices, current state of the art fabrication techniques limits the pillar length to 65µm, so from a single implantation it is therefore not possible to achieve a superjunction structure throughout the drift region of a 1.2kV IGBT. This chapter proposes applying two superjunction implants; one from the cathode side and a second one from the anode side, and investigates the requirement for alignment of these pillars. This work builds upon the concepts and results as given in [66], [70], specifically for an RC-IGBT structure. Although demonstrated on the RC-IGBT the concept could be applied equally to any power device structure (such as an IGBT or MOSFET) with a drift region thickness less than 130µm.

6.2 Device Structure

Figure 97 is a schematic representation of the 1.2kV dual implant SJ RC-IGBT. It is based upon the standard RC-IGBT structure with anode shorts [82], but the drift region contains two separate regions of SJ pillars, one from the cathode side and a second from the anode side. The 2D 1.2kV model used was based upon the verified 2D 1.7kV model developed in Chapter 3. At this lower breakdown voltage, the total length of silicon is reduced (y dimension) from 200µm to 135µm. 135µm represents a standard length for a 1.2kV IGBT, and although 120µm is the leading industry standard, by demonstrating the suitability of the dual implant technique on this slightly longer device, it could easily be applied to a shorter, or lower voltage class variant.

No changes were made to the geometry or the doping at the cathode. The n+ emitter, p+ emitter, p-well and n-enhancement layer doping remains unchanged from the 1.7kV model but the n-drift region doping was reduced slightly to 4e13 cm^{-3}. The majority of changes are situated at the anode, where a new, higher doped but less deep buffer was used (gaussian implant, 3e16cm^{-3} peak concentration, and 7e15cm^{-3} at 1µm depth) with a significantly larger p+ anode implant (gaussian implant, 1e18 cm^{-3} peak concentration, extending 3µm). To enable reverse conducting behaviour the n+ anode short covers 10% of the anode area. The area factor was set so that the total device area simulated is 1cm^2.

Superjunction p-pillars were initially added with a width of 1.5µm and doping 1e16cm^{-3}. The n-pillar doping was calculated to achieve charge balance [66]. For any given depth of superjunction pillar, three offsets were also modelled; full alignment (Figure 97 (a)), 50% offset, full misalignment (Figure 97 (b)).

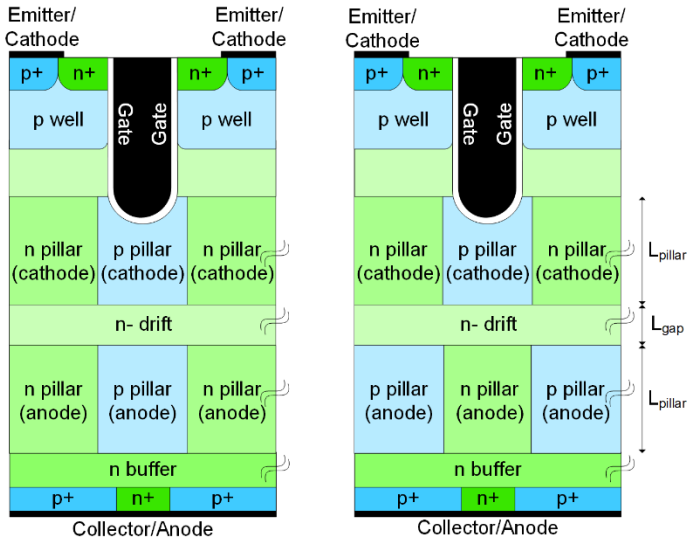


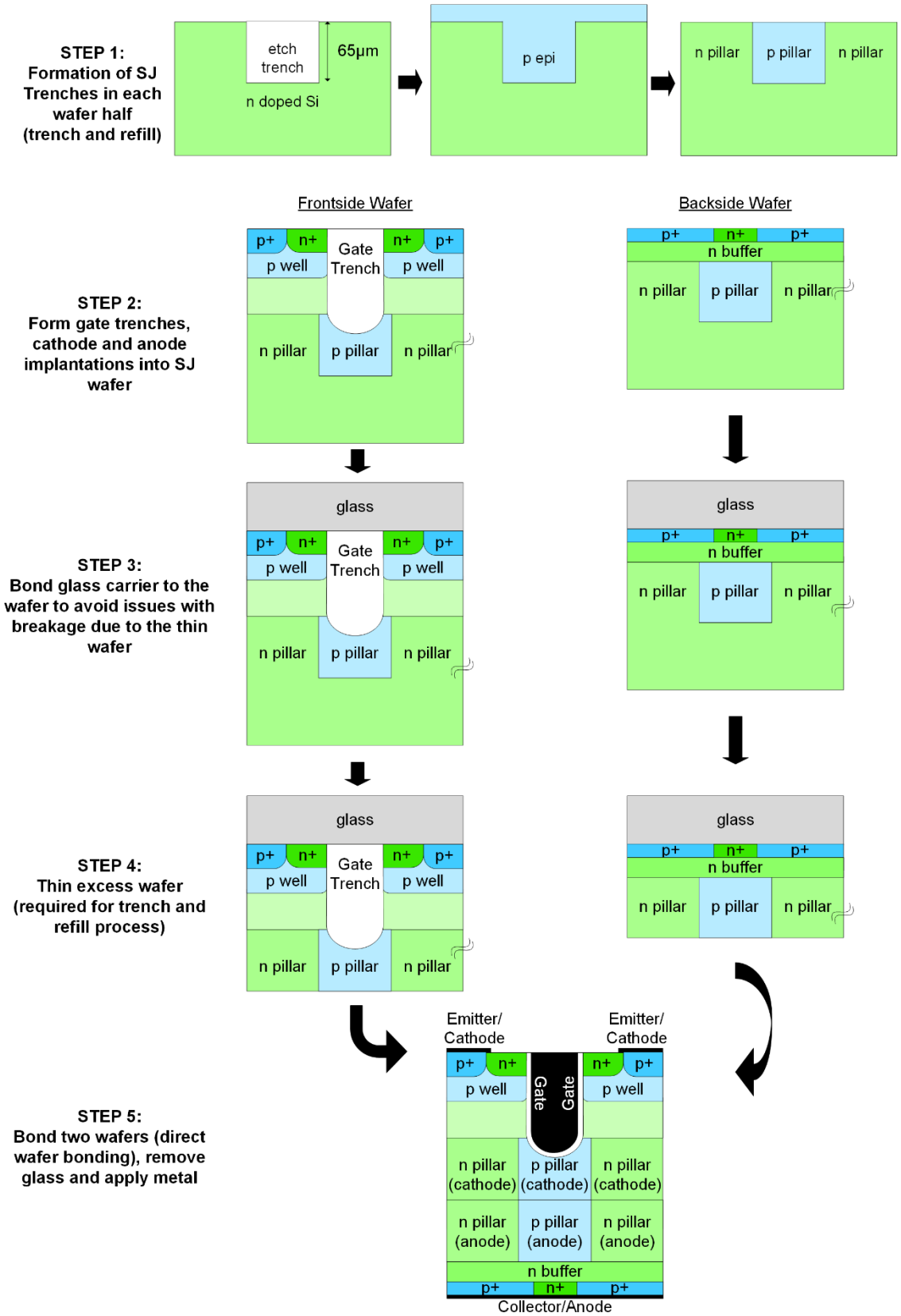
Figure 97 - Dual Implant SJ RC-IGBT structure (not to scale) (a) anode and cathode pillars with no offset, (b) anode and cathode pillars with full offset.

6.3 Device Manufacture

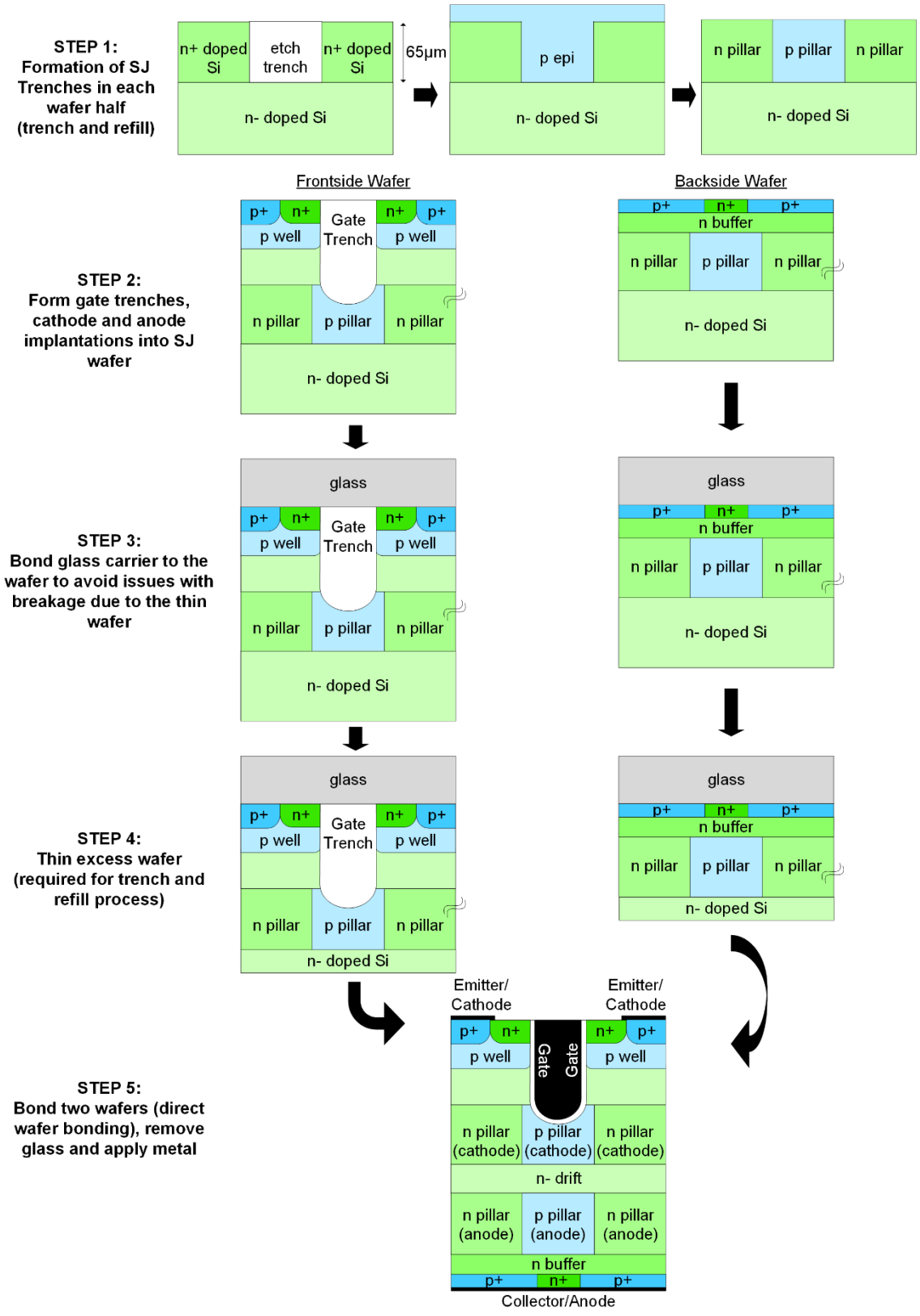
Fabrication of the proposed device is difficult, however, use of a direct wafer bonding technique to produce a full superjunction device (by applying the SJ structure to both the frontside and backside of the wafer) is comparatively easier than attempting to produce a deep superjunction trench from a single etch (which is currently limited to 65µm in length using state of the art fabrication techniques).

A proposed process flow is given in Figure 98. The SJ pillars can be formed either by using a trench and refill technique [68] or by other demonstrated techniques such as that reported in [69]. The proposed fabrication would require the front and backside wafers to be formed separately, with a SJ implant applied to both wafers. Additional wafer thickness is required to avoid damage during the SJ trench formation, which can later be removed prior to the wafer bonding. If this additional wafer thickness is entirely removed, the anode-side and cathode-side superjunction pillars could be directly bonded with no drift region in between (as shown in Figure 98 (a)). The n-buffer, p+ anode and remaining

cathode and gate structures can be formed subsequently. The processing requirements for the backside are not as stringent as for the frontside since there are no cathode or gate structures. The two halves would first be bonded to glass carriers [132] and then etched to remove the excess wafer required for the SJ trench formation. The wafers would then be bonded using a wafer bonding process as demonstrated in [132], [142]–[144]. These studies have shown that the IGBT performance does not degrade using this technique. The results in Section 6.5 demonstrate that there is no requirement for lateral alignment between these two wafers (frontside and backside).


STEP 1:
Formation of SJ Trenches in each wafer half (trench and refill)
etch trench
65µm
n doped Si
p epi
n pillar
p pillar
n pillar
Frontside Wafer
Backside Wafer
STEP 2:
Form gate trenches, cathode and anode implantations into SJ wafer
p+
n+
p well
Gate Trench
n buffer
STEP 3:
Bond glass carrier to the wafer to avoid issues with breakage due to the thin wafer
glass
STEP 4:
Thin excess wafer (required for trench and refill process)
STEP 5:
Bond two wafers (direct wafer bonding), remove glass and apply metal
Emitter/ Cathode
Gate
n pillar (cathode)
p pillar (cathode)
n pillar (anode)
p pillar (anode)
Collector/Anode

(a)



(b)

Figure 98 - Process flow for manufacture of Dual Implant SJ RC-IGBT showing two variants, (a) direct bonding of anode-side and cathode-side SJ regions, and (b) inclusion of n-drift region between SJ pillars

6.4 Device Breakdown

Figure 99 shows the breakdown characteristics of the Dual Implant SJ-RC-IGBT alongside the RC-IGBT and the IGBT using the same device geometry and buffer/drift region doping profiles. As expected, the superjunction RC-IGBT offers improved breakdown capabilities for a given drift length compared to the standard IGBT, and also a small improvement over a traditional RC-IGBT. The presence of the anode short increases the breakdown capability of the standard RC-IGBT compared to the standard IGBT. Application of the superjunction structure to the RC-IGBT results in a further increase in the breakdown voltage, but not as significant as reported for the application of the superjunction structure to the traditional IGBT [66], [70].

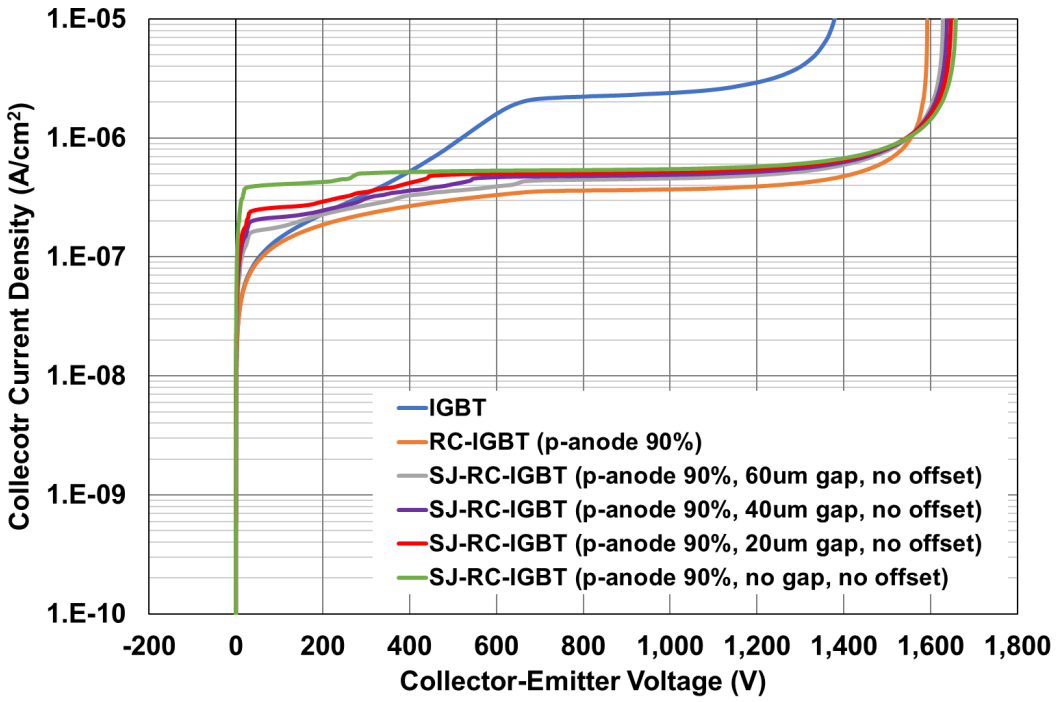


Figure 99 - Simulated breakdown characteristics for the IGBT, RC-IGBT and Dual Implant SJ RC-IGBT with varying L_{gap}, ambient temperature 298K

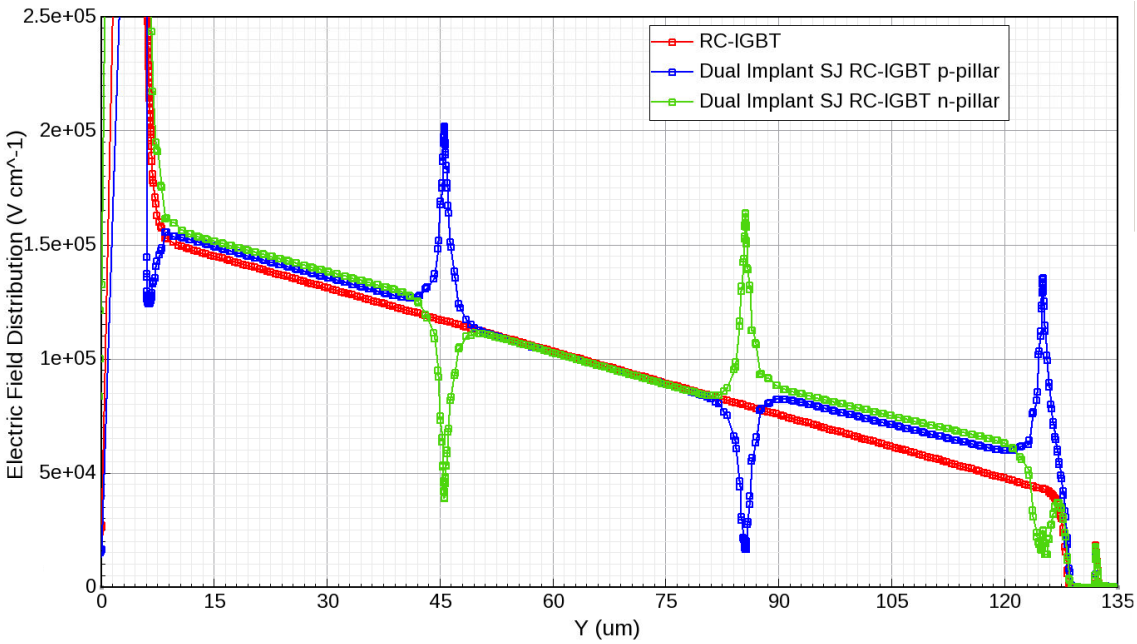


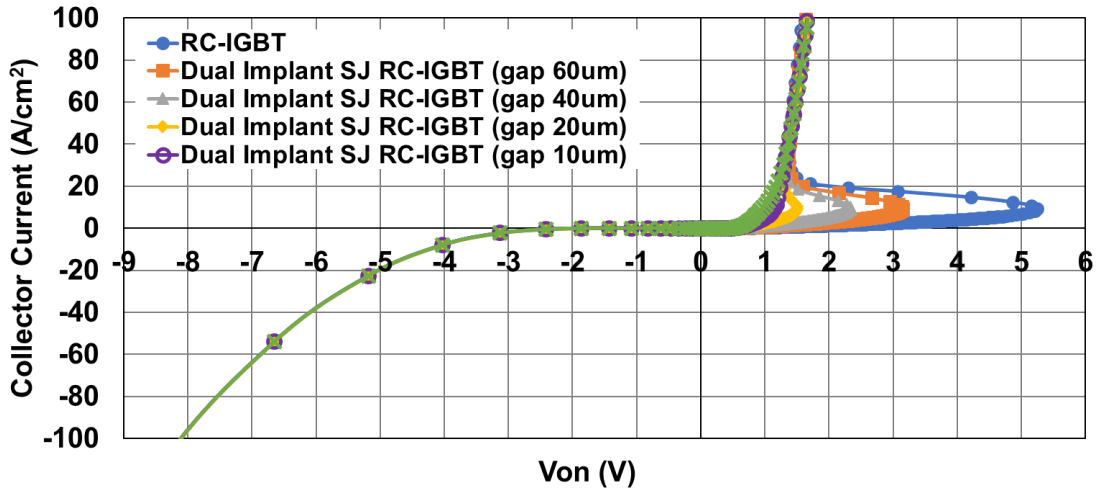
Figure 100 - Electric field distribution under blocking conditions (1.2kV) of the RC-IGBT and Dual Implant SJ RC-IGBT, thickness 135µm, ambient temperature 298K

Figure 100 shows the electric field distributions under blocking conditions (1.2kV), for the standard RC-IGBT and Dual Implant SJ RC-IGBT with L_{gap}=40µm. The SJ pillars meet the condition for charge balance, such that the total charge in the n-doped and p-doped pillars are equal and deplete fully prior to device breakdown [145]. For both devices, breakdown occurs at the n+ injector layer at the cathode, but the presence of the SJ pillars alters the electric field distribution such that a larger voltage can be supported for a given device thickness. As a result, a SJ device can be made thinner for the same breakdown voltage to improve on-state performance, in line with previous studies [17], [66], [70] and the results in Figure 99.

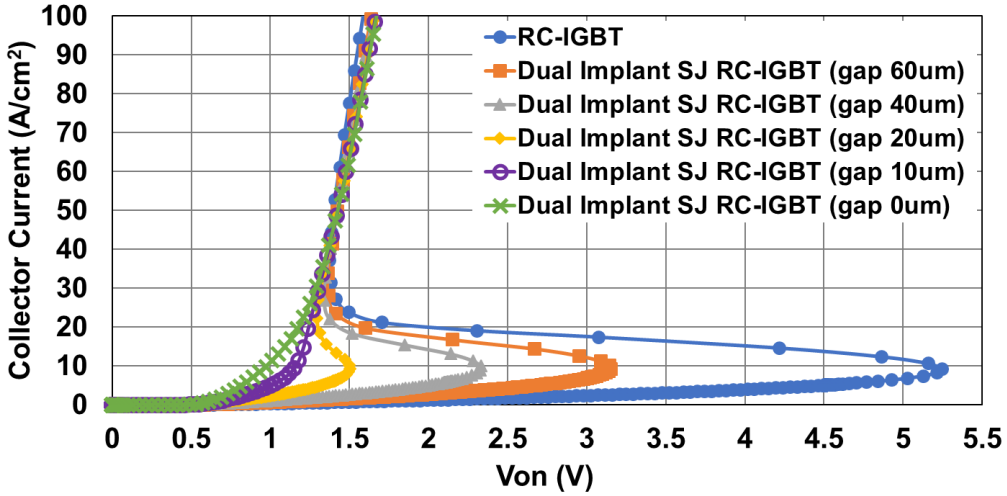
Figure 100 also shows three distinctive electric peaks in the drift region at 45µm, 85µm and 125µm which occur at the junctions between the superjunction pillars and the n-drift regions (n-buffer at 125µm). At each of these points the peak electric field is lower than the critical electric field and therefore does not affect the device operation. However, as reported in [70], this peak electric field at the p-pillar/n-buffer junction (125µm) meant that the n-buffer doping had to be increased to prevent punch-through of the device. This increase in the buffer doping reduces the injection efficiency of the p+ anode, which can be compensated for by increasing the p+ anode doping concentration.

6.5 Device On-State Performance

Application of the dual implanted SJ structure to the RC-IGBT supresses snapback in the forward direction while not affecting the reverse conduction. Figure 101 shows the on-state characteristics where the cathode and anode SJ implants are aligned for varying L_{gap}. It was demonstrated in simulation that a deep SJ device (L_{gap}<10µm or L_{pillar}>54µm) either completely removes the snapback (L_{gap}<5µm) or it is very limited (L_{gap}=10µm). This is in line with the studies in [66], [108], however in this device each SJ implantation (L_{pillar}) needed to produce the full SJ device is 59µm; less than the 65µm limit imposed by current fabrication techniques.



(a)



(b)

Figure 101 - On-state characteristics of Dual Implant SJ RC-IGBT, ambient temperature 298K, SJ pillars have no offset between anode and cathode side (a) forward and reverse conduction, (b) zoom of forward conduction

Figure 102 shows the effect of SJ pillar alignment in the x-direction, with the anode pillars misaligned fully (Figure 97 (b)) and by 50%. The on-state characteristics show minimal variation; at 20A/cm^2 the on-state voltage varies by 0.03V between the half-offset and the fully aligned cells. This shows there is no requirement for alignment between the SJ pillars making this proposed device relatively easy to fabricate.

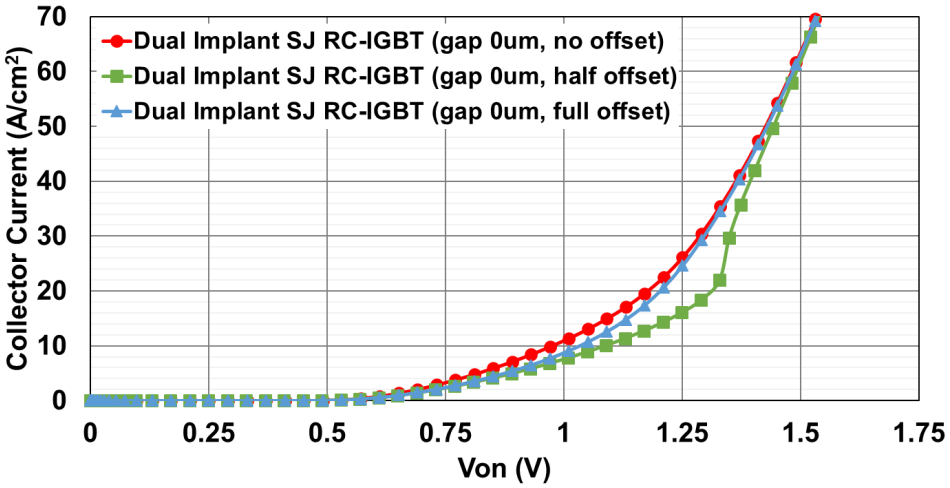


Figure 102 - On-state characteristics of Dual Implant Full SJ RC-IGBT with varying offset between anode and cathode SJ implants, ambient temperature 298K

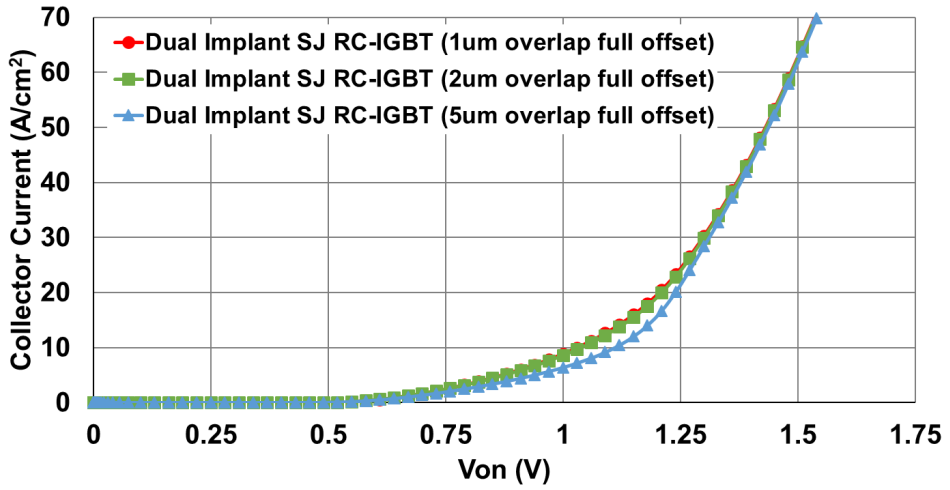


Figure 103 - On-state characteristics of Dual Implant SJ RC-IGBT with different amounts of overlap for full offset between anode and cathode SJ implants, ambient temperature 298K

The effect of overlapping of the SJ pillars (y-direction) was also investigated. The on-state plots for varying amount of overlap (Figure 103) shows minimal variation in the characteristic compared to the full SJ structure (Figure 102) which is to be expected given

the bipolar action of the IGBT. Figure 103 shows the full offset device, but the result applies equally to the half offset and no offset cells.

With a 5µm overlap between pillars, for both full and half misalignment, the breakdown capabilities are unchanged. However, with full alignment between anode and cathode pillars (shown in Figure 104 (a)) the breakdown capabilities begin to degrade significantly as the overlap increases. In the region where the pillars overlap, the SJ charges add. For the fully misaligned cell (shown in Figure 104 (b)), the charge from the p-doped pillars is cancelled out by the n-doped pillars resulting in a lowly doped region in the centre of the device (original n-drift doping concentration). For the no offset cell, SJ pillars are aligned and therefore in the overlapping region the pillar doping increases by a factor of two. Hence, under blocking conditions the overlapping area is unable to fully deplete as the conditions for charge balance are no longer met. With partial misalignment (half offset) the SJ pillars are able to compensate for the regions of charge imbalance, but with full alignment, a high electric field is produced in this highly doped central section of the drift region, resulting in premature breakdown. Therefore, to guarantee the performance of the device without the requirement for alignment between the SJ pillars, at most a 2µm overlap can occur, to ensure full drift layer depletion.

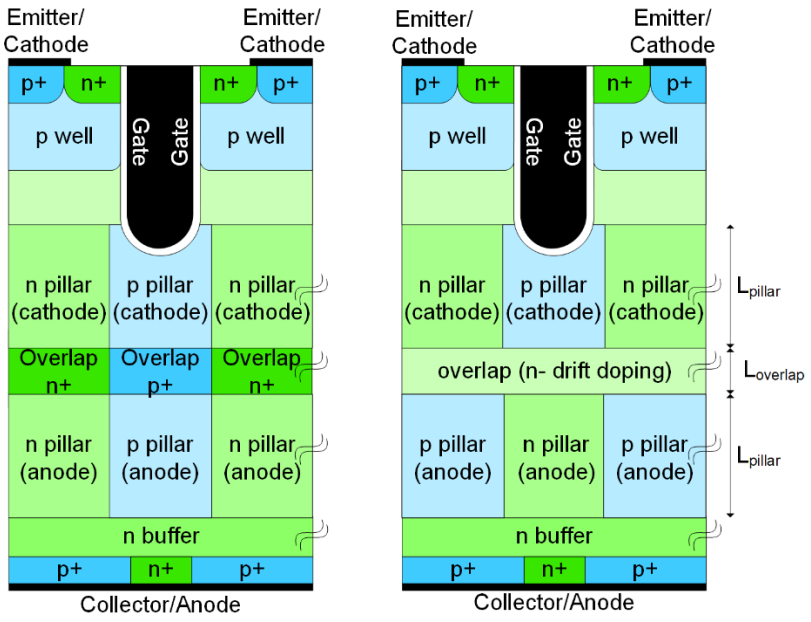
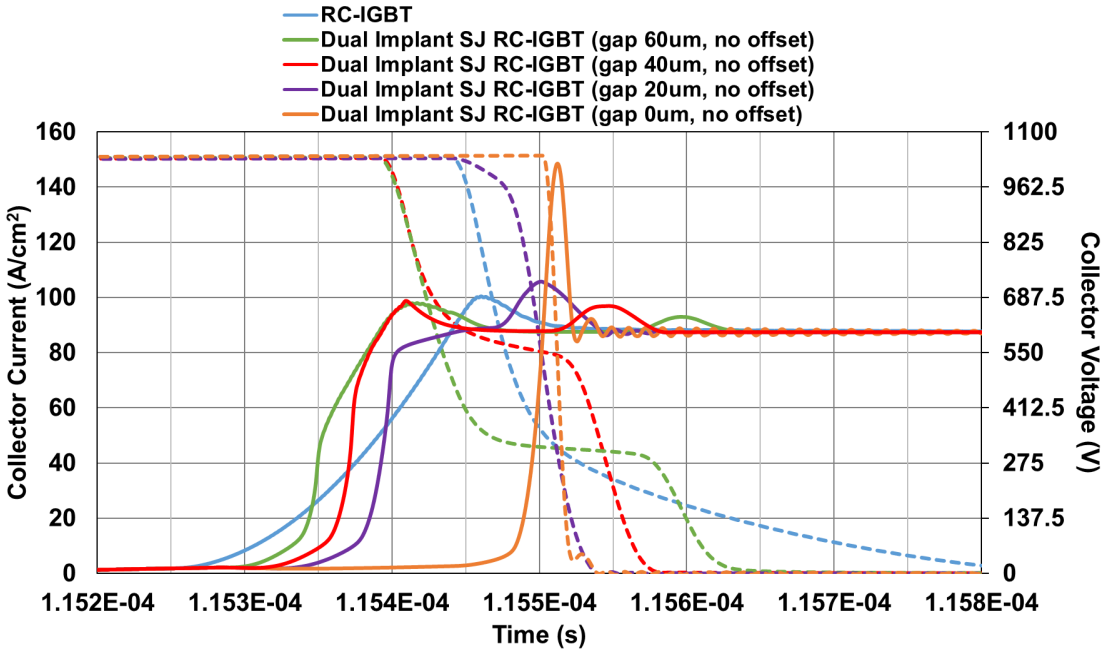


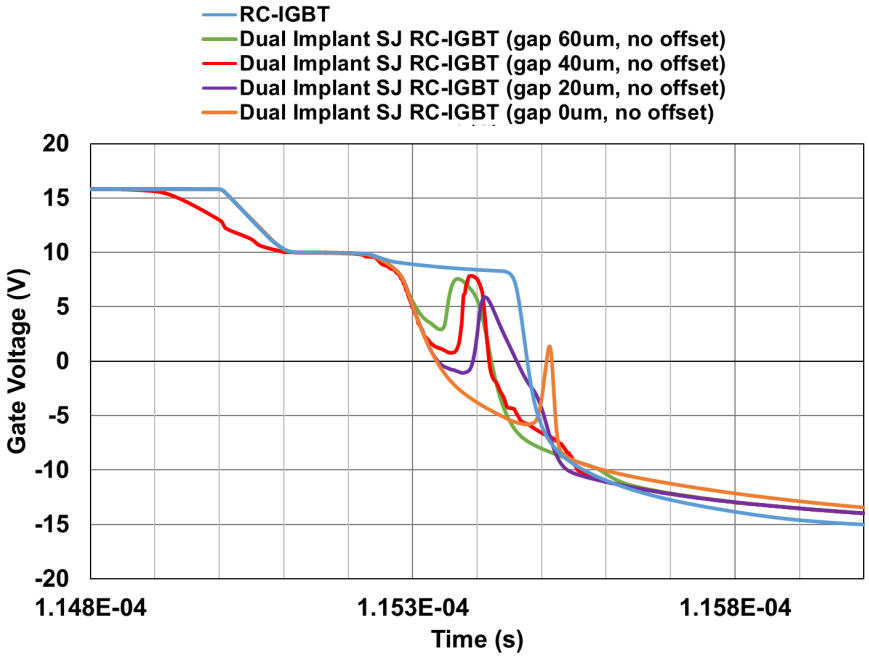
Figure 104 - Dual Implant SJ RC-IGBT structure with SJ pillar overlapping (not to scale) (a) anode and cathode pillars with no offset, (b) anode and cathode pillars with full offset.

6.6 Transient Performance

Transient simulations were run in accordance with IEC standard at a line voltage of 600V, using the same circuit as in Chapter 3, Section 3.5.1 [87]. Initial simulations exhibited significant ringing through the collector at turn off. The high doping of the superjunction sections within the device drift region and the interaction of the depletion region with the buffer resulted in high frequency ringing with the stray inductance Ls. To suppress this, the stray inductance was reduced to 35nH/cm^2 of device area in line with industry-leading module packaging designs, which have been optimised for SiC devices that exhibit similar behaviour [146], [147]. A Zener diode clamp with breakdown voltage 1500V was also included for protection.

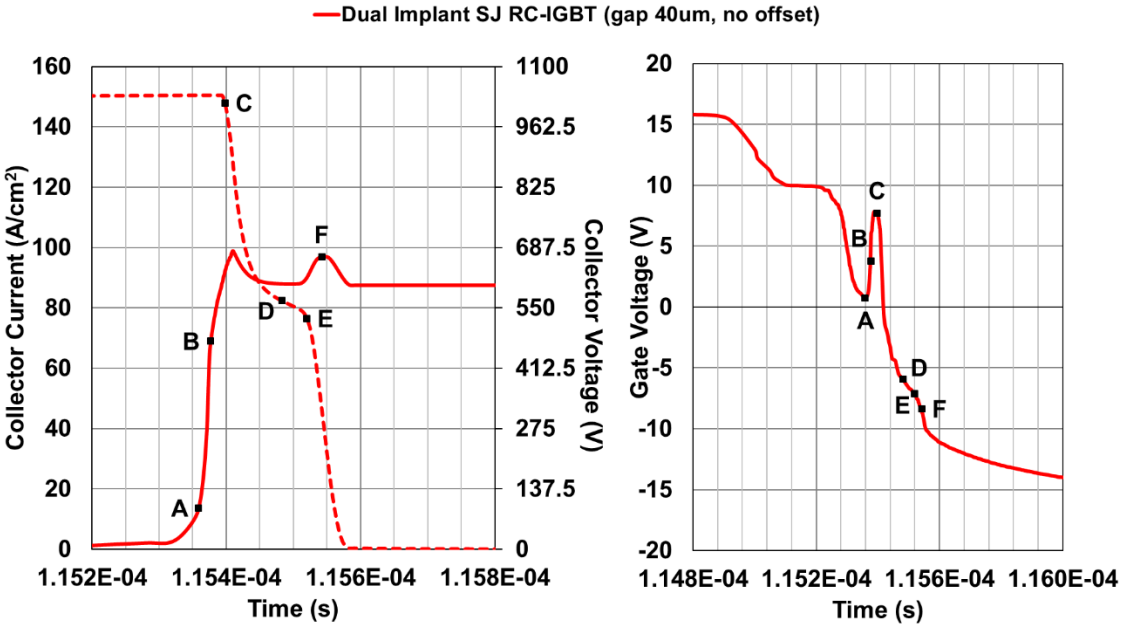


(a)



(b)

Figure 105 - Inductive load turn-off waveform for the Trench RC-IGBT and Trench Dual Implant SJ RC-IGBT with L_{gap}=60µm, 40µm, 20µm and 0µm (no offset), ambient temperature = 298K. (a) Dashed lines collector current; solid line collector-emitter voltage, (b) gate-emitter voltage



(a) (b)

Figure 106 - Inductive load turn-off waveform for the Trench Dual Implant SJ RC-IGBT with L_{gap}=40µm, (no offset), ambient temperature = 298K, as shown in Figure 105 but with significant points marked A to D. (a) Dashed lines collector current; solid line collector-emitter voltage, (b) gate-emitter voltage

Figure 105 shows the turn-off waveforms for the RC-IGBT and the dual implant SJ RC-IGBT with L_{gap} of 0µm, 20µm, 40µm and 60µm (dual implant SJ RC-IGBT with L_{gap} 20µm is shown alone in Figure 106 with key points marked A to D for ease of viewing). During turn-off, voltage is supported across the p-well/n-drift junction and the depletion extends down through the device (y-direction) towards the anode. The presence of the SJ structure induces a secondary lateral (x-direction) expansion of the depletion region which causes the higher breakdown capability (Figure 99, Figure 100). In this dual implant device, the gate-emitter voltage falls sharply during what would typically be the Miller plateau region (point A, Figure 106). For normal IGBTs under inductive load conditions, during the Miller plateau, all gate current is used to discharge the parasitic capacitance C_{gc}, where C_{gc} is a function of the collector-emitter voltage. Typically, C_{gc} is initially large resulting in a low dV_{ce}/dt at the start of the turn-off event, but, after this, the depletion region does not change significantly with applied voltage (for reasonable collector voltages for the given device's rating) so C_{gc} can be considered almost constant and hence the dV_{ce}/dt can be approximated to be linear. However, in superjunction devices, it is known that C_{gc} changes dynamically with increasing V_{ce}, with the capacitance initially falling then recovering to a higher value [148]. This effect is particularly pronounced for the dual implant device as the cathode side SJ implant is being completely depleted, with partial depletion of the drift region in between, to support the line voltage across the device, but leaving the anode side superjunction completely un-depleted at this line voltage. This is characterised by the initial plateau on the gate-emitter waveform followed by the sharp fall and then recovery, as shown in Figure 106 (b). During this time, the C_{gc} rapidly decreases and then begins to recover as the depletion region moves into the anode side superjunction causing a slowing in the dV_{ce}/dt (point B, Figure 106). At point C, Figure 106, I_c falls at a high dI/dt as the depletion region extends towards the anode through the lowly doped n-drift region, and as it encounters the second superjunction structure (anode side) the collector current plateaus due to this secondary lateral expansion of the depletion region in the anode SJ pillars (point D, Figure 106). This high voltage high current event could cause significant heating within the device; however, this plateau is eliminated for L_{gap}<20µm. Once the SJ pillars have been fully depleted, the collector current begins to fall rapidly (point E, Figure 106) as the remaining excess charge is swept out of the device. This coincides with a small increase in collector voltage (point F, Figure 106); this is an inductive load test and this second fast dI/dt event causes an increase in voltage across the inductor as seen in the waveform.

Figure 105 shows that reducing L_{gap} reduces the tail current but increases the likelihood of high frequency ringing. The gate capacitance is non-constant during turn-off as explained above and previously reported in [69], [148], but there is no ringing on the gate waveform (Figure 105 (b)), indicating this is not the source of the ringing. The depletion region at the line voltage extends further into the buffer regions for deep SJ structures. The buffer region has a reduced carrier lifetime due to the higher doping used compared to the drift region and therefore, the capacitive structure C_{gc} is more likely to ring with the stray inductance. Misalignment between the anode-side and cathode-side pillars also increases this ringing; a 50% offset generates the greatest amount of ringing, followed by no offset, and full-offset showing the least. This was the case for all depths of superjunction implant. There is no clear reason for this, but from studying the breakdown plots at 600V and 700V, it appears that the depletion region spreads the furthest into the buffer region for the 50% offset, and least for full offset. This could be associated with the position of the n+ anode short, which at present is situated centrally within the cell. Further evidence to support this conclusion is given by increasing the p-width for fixed p-pillar doping (while also increasing n-pillar doping for charge balance to hold), which suppresses the ringing as the depletion region does not spread as far through the device, and hence does not reach the buffer. It has been demonstrated that for a full SJ structure with 2.5µm p-width there is no ringing present on the waveforms irrespective of the SJ pillar alignment, but there is a small amount of ringing present with a p-width of 1.8µm at 50% offset. It should be noted that by increasing the p-pillar width the breakdown capabilities of the device worsened, although all were still above the target voltage of 1.2kV. Some structures also exhibited some Plasma Extraction Transit Time (PETT) oscillations [149], but investigations have highlighted that careful optimisation of the buffer can eliminate all of these different oscillations present at turn-off.

The device has been optimised for 600V operation, which constitutes the normal application range for a 1.2kV device. At this switching voltage the device shows good turn-off ruggedness (three times nominal current, 350A/cm^2). Although the device is rugged up to 900V, at this switching voltage some unwanted oscillations are introduced. This occurs because the transient voltage generated via L_{stray} pushes the depletion region into the buffer region (which due to the higher doping has a reduced carrier lifetime), so there is less excess charge in the open pnp transistor. Hence there is minimal tail current for the dual implant SJ RC-IGBT and this is the cause of the ringing. To address this

issue, a simple re-optimisation of the n-buffer doping profile supresses this oscillation at 900V; achieving similar turn-off ruggedness without compromising the breakdown performance.

6.7 Technology Curve

The technology curve given in Figure 107 shows the advantage in removing the snapback; devices where L_{gap}<10µm exhibited negligible snapback and have significantly reduced turn-off losses. Compared to the traditional RC-IGBT, the full dual implant SJ RC-IGBT provides up to a 77% reduction in switching losses, and with L_{gap}=10µm a 39% reduction (V_{on} = 1.515V at 100A/cm^2). The manufacturing requirements for the dual implant SJ RC-IGBT are therefore less restrictive, and a full SJ structure is not required to achieve significant improvements in performance; alleviating concerns regarding the overlapping of the anode and cathode SJ pillars during processing. To warrant the additional processing expense to implant the dual SJ structure, Figure 107 shows that a deep SJ structure is required as there is little benefit in a partial implant.

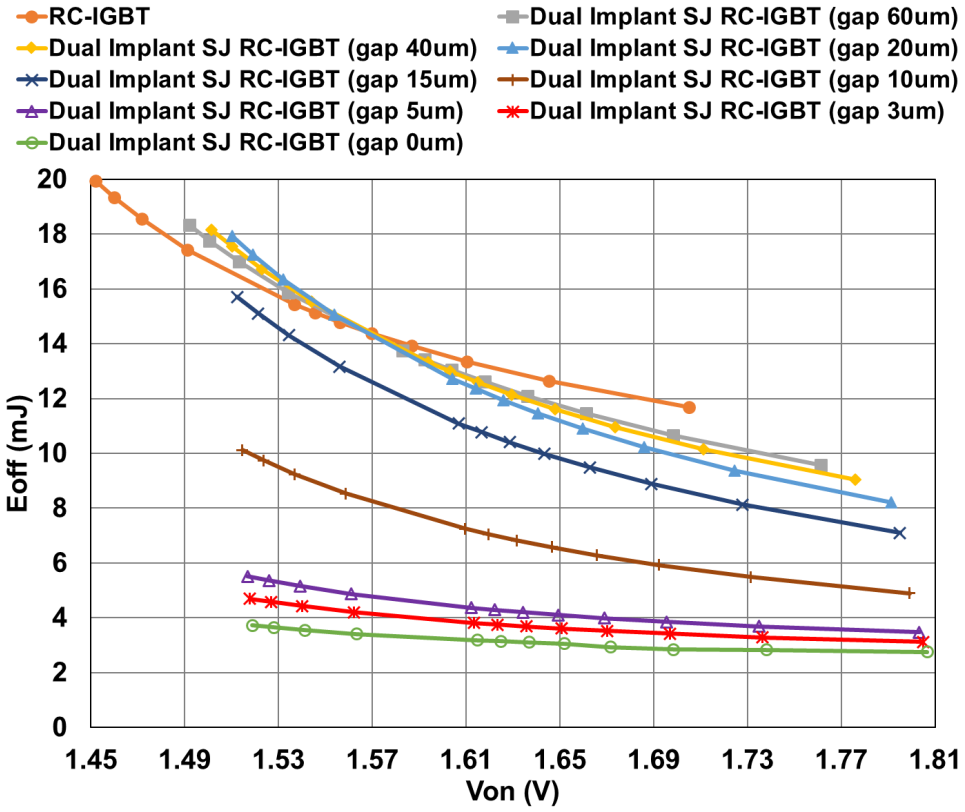


Figure 107 - Technology curves of Trench RC-IGBT and Dual Implant SJ RC-IGBT with varying L_{gap}, no offset, V_{on} at 100A/cm^2, ambient temperature 298K

6.8 Conclusions

This chapter presents the Dual Implant SJ RC-IGBT and describes how a full superjunction structure can be manufactured within a 1.2kV device. Two separate SJ implantations are applied to the device one from the anode side and the other from the cathode side and it has been demonstrated that there is no requirement for the pillars to be aligned. It has also been shown that for significant improvement in turn-off losses compared to a traditional RC-IGBT, a deep SJ device must be manufactured. To achieve the performance benefits, the maximum permissible gap between the anode and cathode SJ pillars is 10μm such that there is negligible snapback in the on-state, and a maximum pillar overlap of 2μm can be tolerated without degradation in the breakdown capabilities. It has been shown that at most this Dual Implant SJ RC-IGBT can achieve a 77% reduction in turn-off losses compared to the conventional RC-IGBT.

Chapter 7

Si IGBT and SiC MOSFET Coordinated Switching Scheme

As has been shown in the previous chapters, the IGBT has excellent on-state performance due to the bipolar action of the device. However, this property restricts the IGBT dV_{ce}/dt at turn-off, which increases turn-off losses compared to an equivalent metal-oxide semiconductor field effect transistor (MOSFET). It is not possible to improve the inherent dV_{ce}/dt of the IGBT without sacrificing the on-state behaviour, and therefore an alternative approach was investigated.

Silicon-carbide (SiC) MOSFETs are emerging into the market as SiC has higher mobility and increased thermal stability compared to silicon (Si), but the on-state losses of these devices are still higher than the Si IGBT and the cost per amp of SiC is larger due to increased material and processing costs. Therefore, this chapter presents a coordinated switching scheme using both a Si IGBT and a SiC MOSFET, which aims to improve the turn-off losses within the IGBT without sacrificing on-state losses and minimise the overall system cost. The system was optimised to use a SiC MOSFET in excess of its nominal ratings, reducing the cost of the device, and thermal simulations included in this chapter show that the SiC MOSFET can be operated safely under these conditions.[1]

[1] Excerpts of the material in this chapter has been taken from the following publication:
P. Palmer, X. Zhang, J. Zhang, E. Findlay, T. Zhang, and E. Shelton, "Coordinated Switching with SiC MOSFET for Increasing Turn-off dV / dt of Si IGBT," 2018 IEEE Energy Convers. Congr. Expo., pp. 3517–3521, 2018

7.1 Introduction

Multilevel inverter topologies are becoming increasingly popular in modern drive systems and for HVDC applications [150]–[155]. Despite using a larger number of power transistor switches compared to a more traditional topology, there is an overall efficiency benefit in terms of filtering requirements and a reduction in the voltage rating of each individual transistor; multiple transistors are connected in series between the voltage rails such that each single transistor can have a lower voltage rating compared to the overall voltage rating of the system [150], [154]. This has the advantage that smaller, more cost-effective transistors can be used in larger higher-powered applications, but it is critical that the switching event is as efficient as possible.

The IGBT has a lower on-state voltage for the same voltage blocking rating compared to a silicon power metal–oxide–semiconductor field-effect transistor (MOSFET) due to the bipolar injection mechanism within the IGBT, which causes conductivity modulation within the drift region [36], [84], making it attractive for use within multilevel inverters. However, this plasma formation within the IGBT results in increased switching losses and limits the maximum switching frequency due to the concentration of excess carriers that restrict the voltage rise (dV_{ce}/dt) during turn-off [1], [156]. The development of the soft punch through (SPT) [57], fieldstop (FS) [58] or light punch-through (LPT) [59] designs reduced the IGBT switching losses by providing an initial fast turn-off typical of a non-punch through (NPT) design but eliminating the long tail [36], [57]. Compared to the punch through (PT) design, the SPT IGBT has a linear dV_{ce}/dt with minimal overshoot [57]. Despite these developments in performance, the bipolar characteristics of the IGBT inherently restrict the rate of voltage rise during turn-off, and therefore in future only limited, incremental improvements are expected for Si IGBT technologies [24], [157].

In contrast, MOSFETs are capable of high switching speeds (fast rise of dV_{ds}/dt at turn off) as the device is solely controlled by the MOS gate [1]. Silicon-carbide, a wide bandgap semiconductor material, offers a more than eight times higher electric field breakdown capability compared to Si [158] and higher saturation drift velocity [25], [159]. SiC also offers improved thermal properties and has been demonstrated to operate reliably with a junction temperature in excess of 200°C for a SiC MOSFET [160], [161]. The specific on-resistance of the drift region is also greatly reduced for SiC compared to Si since the drift region can be more highly doped and significantly thinner without compromising breakdown capabilities [1], [24], [158]. As a consequence, for devices in

the range of 1.2–1.7 kV, a SiC MOSFET offers the best compromise compared to existing silicon devices: Si MOSFETs have much higher conduction losses compared to the Si IGBT but the Si IGBT suffers from high dynamic losses limiting its switching capabilities [25]. SiC IGBTs are, however, not suitable for high power applications as the inbuilt potential of a SiC p/n junction is 2.7V, negating the other material benefits offered by SiC.

Since the development of the first SiC MOSFET [22], several generations of devices have been developed and are commercially available in the 650V – 1.7kV range with current ratings in the region of hundreds of amps [23]. However, the cost per amp of SiC is still significantly higher than Si since both the material and processing costs are greater [24]. It is expected that, over time, the cost of production will reduce due to greater volumes, improved manufacturing techniques and larger SiC wafers, but not to the level of silicon [21], [24], [25]. Despite the performance benefits, this additional expense currently prevents the use of SiC MOSFETs within many applications.

It is therefore proposed in this chapter to employ a coordinated switching scheme using a bipolar Si IGBT and a unipolar SiC MOSFET to achieve improved switching performance, without sacrificing on-state losses or incurring a significant increase in device cost. Many Si based hybrid IGBT and MOSFET solutions have been proposed previously [162]–[165], and more recently a SiC MOSFET and Si IGBT co-packaged hybrid device concept has been demonstrated in [166], [167]. However, unlike previous studies, the concept proposed in this chapter only switches the SiC MOSFET for a short period of time at the end of the IGBT duty cycle, saving the thermal allowance of the SiC MOSFET for a more extensive and cost-effective use of its device ratings. In this study co-packaging is avoided to take advantage of commercially competitively priced devices.

This concept was developed in collaboration with Patrick Palmer, Xueqiang Zhang, Jin Zhang, Tianqi Zhang, Edward Shelton [156].

7.2 IGBT Turn-Off Mechanism and the Reduction of Excess Carriers

The explanation included in this section was developed by the author of this thesis in collaboration with Patrick Palmer and Xueqiang Zhang.

To turn-on an IGBT, the p-well must be inverted to form a MOS channel through the application of a positive gate-emitter voltage (V_{ge}), causing the flow of electrons into the n-drift from the n+ emitter implantation. This electron current serves as the base current for the bipolar pnp transistor within the IGBT (formed by the p+ collector, n-buffer/n-drift, p-well structure). Once this bipolar structure is turned on, holes are injected into the n-drift region and the excess carrier concentration (plasma) increases. The resulting conductivity modulation accounts for the relatively low on-state voltage (V_{on}) of the IGBT, however this plasma limits the dynamic performance. For inductive loads, to turn off the device, the Miller capacitances and accumulation layer formed under the gate must be discharged and the line voltage must first be supported across the device by the growth of the depletion region from the emitter towards the collector. The MOS channel is contracted to restrict the injection of electrons into the base of the pnp transistor, which allows the depletion region to form. It is the rate of the growth of this depletion region that determines the dV_{ce}/dt in the turn-off waveforms, but the maximum dV_{ce}/dt is limited by the rate of removal of the stored charge. After this, the speed of turn-off (dI_{ce}/dt) is determined by the open base current decay of the pnp transistor which is, in turn, dependent on the remaining excess carrier charge (plasma) stored in the n-drift region. Controlling the plasma level, as part of the device design, is therefore essential to achieve a favourable trade-off between on-state and turn-off losses. As a result, for a given IGBT design, multiple devices are manufactured at various points along the turn-off loss (E_{off}) and on-state voltage (V_{on}) trade-off curve, such that the power device can be optimised for various applications.

As a mature technology, step changes in IGBT design will be limited, and hence alternative methods are required to improve performance. The switching scheme proposed aims to reduce the excess plasma within the IGBT at the point of turn-off, without modifying the IGBT device design or compromising the on-state performance. The premise of the switching scheme is to turn on a parallel SiC MOSFET towards the end of the IGBT duty cycle. At this point, the MOS channel of the IGBT is turned off and further current is prevented from entering the IGBT as the SiC MOSFET provides an alternative route for the load current. While the MOSFET is conducting, the excess carriers (plasma) in the IGBT drift region begin the slow processes of recombination and diffusion. The reduction in plasma will depend on the length of time the MOSFET conducts for, however this reduction of charge within the IGBT drift region should result

in an increased IGBT dV_{ce}/dt when the MOSFET is turned off, as the depletion region is able to form more quickly. The excess carrier charge in the IGBT cannot be reduced indefinitely by such recombination and diffusion, and therefore a limit in the increase of dV_{ce}/dt is expected. There is also a trade-off with MOSFET losses, which is explored in Section 7.4, however, an overall reduction in switching losses is seen compared to a single Si IGBT solution.

For this switching scheme, it is also advantageous to minimise the size of the SiC MOSFET used in order to reduce the overall cost of the hybrid solution and maximise efficiency. Since the mobility of carriers in SiC is higher than in Si, a much smaller SiC MOSFET can be employed compared to an equivalent silicon device. According to this scheme, the SiC MOSFET turns-on under Zero Voltage Switching (ZVS) and/or Zero Current Switching (ZCS), minimising turn-on losses. This retains the thermal capacity of the SiC MOSFET for the short period of time when it conducts the full load current. The SiC MOSFET can therefore be chosen to be undersized and operated it in excess of its nominal ratings. This results in the device temporarily conducting current beyond its specified DC current rating. Section 7.4.3 considers the implications of these conditions on the thermal behaviour of the SiC MOSFET, noting that the active volume of the device sits on a SiC substrate. It has been shown to be an effective solution since the SiC MOSFET has low switching losses and conducts for only a fraction of the overall system duty cycle.

7.3 Experimental Verification of Switching Scheme

The experimental measurements were undertaken by Patrick Palmer and Edward Shelton. Interpretation of these results were completed by the author of this thesis in collaboration with Patrick Palmer, Xueqiang Zhang.

Figure 108 shows the control strategy for the coordinated IGBT/MOSFET switching scheme. The effect of varying the length of time that the MOSFET conducts for, with the IGBT MOS channel off, is investigated in this study. Experimental verification of the scheme was conducted using a Fuji Electric V series 1.7kV 650A Si IGBT module with a Wolfspeed C2M series 1.2kV 36A (80mΩ) SiC MOSFET connected in a voltage clamp circuit which effectively behaves as an inductive load test, as shown in Figure 109. A

double pulse test was conducted with a line voltage of 400V and a maximum load current of 20A at turn-off. The transistors were controlled using two in-house programmable gate drivers and the integrated antiparallel diodes within the IGBT module were used as the free-wheeling diode (D1). Despite only switching a relatively low current, as found in pulse-width modulation (PWM) circuits, this test set-up demonstrates the capabilities of the switching scheme, and in particular the ability to use a significantly lower rated SiC MOSFET compared to the Si IGBT.

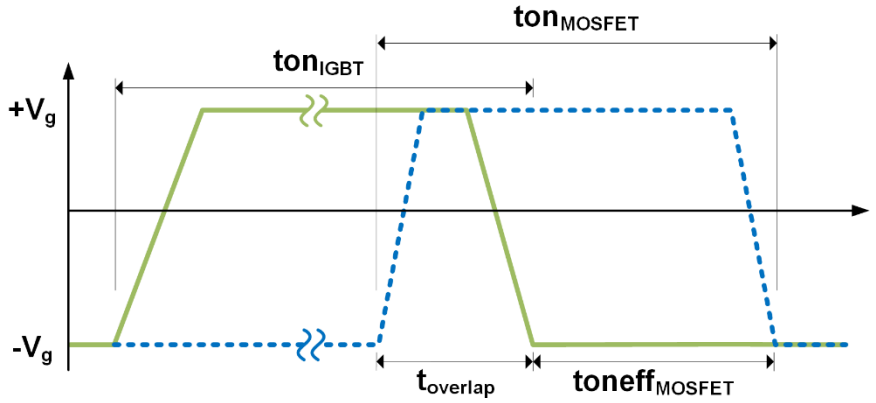


Figure 108 - Gate drive timing diagram, IGBT solid green line, MOSFET dashed blue line. $toneff_{MOSFET}$ is varied throughout the investigation.

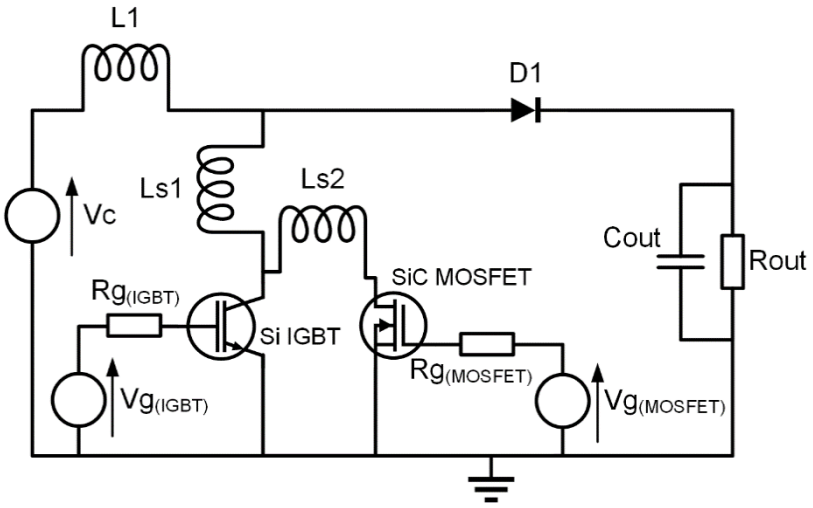


Figure 109 - Schematic diagram of experimental voltage clamp circuit (effective inductive load test) for coordinated SiC MOSFET and Si IGBT switching scheme

Figure 110 shows the conventional turn-off of the IGBT in isolation which can be compared with the coordinated MOSFET/IGBT solution shown in Figure 111. Given that, in both cases, the switching current is significantly lower than the IGBT device

rating, the bipolar current is a significant proportion of the overall collector current. This results in the tail current becoming particularly pronounced and the rate of increase of collector voltage lower than for the datasheet performance of the IGBT at turn-off. Despite this, the coordinated switching solution (Figure 111) exhibits a much higher dV_{ce}/dt; 807 V/µs compared to the single IGBT solution (Figure 110) at 520 V/µs. The coordinated switching solution also exhibits lower tail current indicating that there has been a significant reduction in plasma in the drift region at the point of turn-off compared to the reference IGBT.

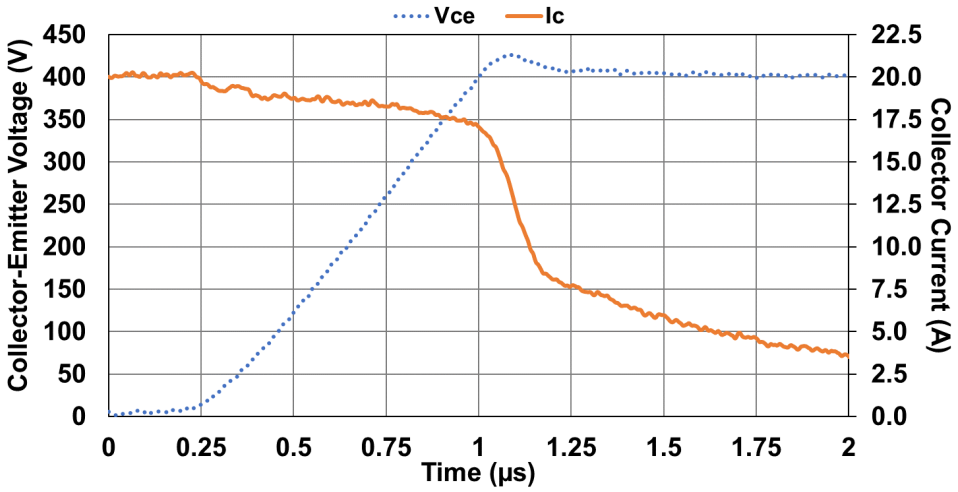


Figure 110 - Turn-off waveform of Si IGBT, without SiC MOSFET, in inductive load test as given in Figure 109, ambient temperature 298K

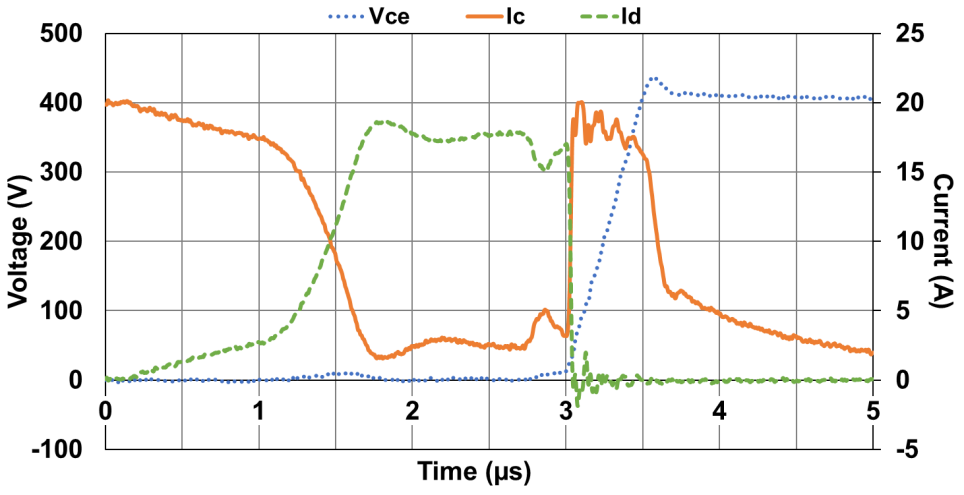


Figure 111 - Turn-off waveform showing the Si IGBT collector-emitter voltage (V_{CE}) and collector current (I_C) with SiC MOSFET drain current (I_D) in the coordinated switching scheme operating in the test circuit as given in Figure 109, ton_{MOSFET} = 3µs, ambient temperature 298K

The waveform in Figure 111 can be split into three phases. During the first phase ($t<1.7\mu s$), the SiC MOSFET is switched on under ZVS condition and subsequently the IGBT MOS gate is turned off. As a result, the majority of load current is transferred from the IGBT to the MOSFET. This commutation takes approximately 1.7μs to complete but the small bipolar element of the IGBT current (tail current) remains in the IGBT due to the plasma stored in the drift region. During the second phase ($1.7\mu s<t<3\mu s$), the majority of the load current is maintained in the MOSFET, giving time for the open base current decay of the pnp transistor within the IGBT to occur through diffusion and recombination of carriers while V_{ce} remains low. In the third phase ($t>3\mu s$), the MOSFET is switched off, the load current is commutated back to the IGBT, and a linear rise in V_{ce} is seen. As with a conventional IGBT turn-off under inductive load, once V_{ce} has reached the line voltage (400V) the collector current falls rapidly, leaving only the remaining tail current caused by the bipolar action of the device, which is significantly reduced compared to the IGBT only turn-off in Figure 110.

Figure 112 provides the relationship between the measured dV_{ce}/dt and the effective on-time for the SiC MOSFET ($toneff_{MOSFET}$) while the IGBT MOS gate is off. During these measurements $t_{overlap}$ was set to 1μs. This time accounts for the delay to turn on the SiC MOSFET, a safety margin to ensure that the SiC MOSFET is fully on before the IGBT gate is turned off, and the time taken for the IGBT gate voltage to fall. Figure 112 shows that for low MOSFET on-time ($toneff_{MOSFET}<9\mu s$) there is a linear increase in dV_{ce}/dt, however beyond this, the rate of increase of collector emitter voltage begins to slow and a saturation effect is exhibited: from Figure 113 it can be seen that there is negligible tail current for ton_{MOSFET} at 20μs showing that there is a limit to the reduction in excess carrier charge in the IGBT. Figure 113 shows overshoot and ringing in the waveforms as ton_{MOSFET} increases. This occurs because there has been a significant reduction of plasma within the drift, such that when the depletion region forms due to the reapplication of the line voltage across the collector-emitter, it spreads further into the device and hence the parasitic C_{gc} rapidly reduces. As a consequence of this and the stray inductance in the circuit, it results in the device "snapping" and ringing occurs. This therefore presents a limit to the effectiveness of reducing the stored plasma and the tail current. Despite this, the experimental results demonstrate an increase in dV_{ce}/dt by over four times when $toneff_{MOSFET} = 9\mu s$ ($ton_{MOSFET} = 10\mu s$) and the reduction in tail current lowers the IGBT turn-off losses considerably.

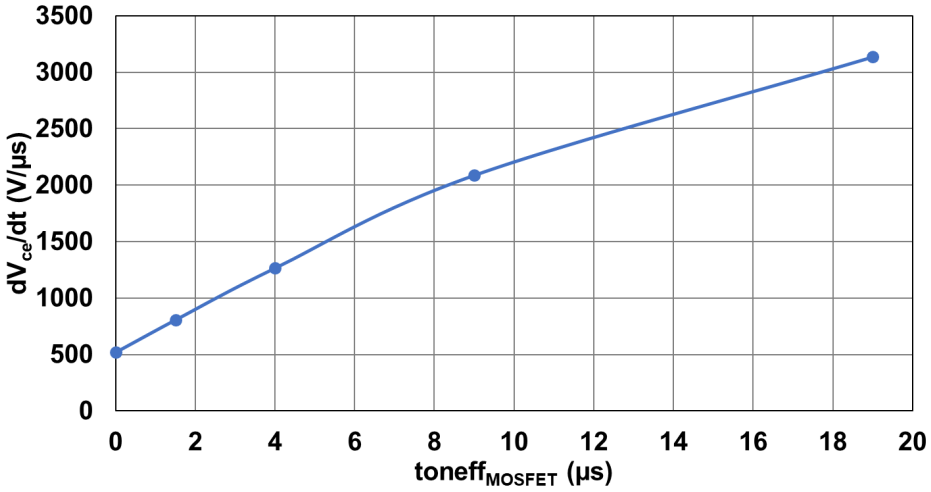


Figure 112 - Experimentally measured rate of change of collector-emitter voltage (measured at 10%-90% V_{ce}) against the effective on-time of the SiC MOSFET ($toneff_{MOSFET}$), switching 20A in the circuit as given in Figure 109, ambient temperature 298K

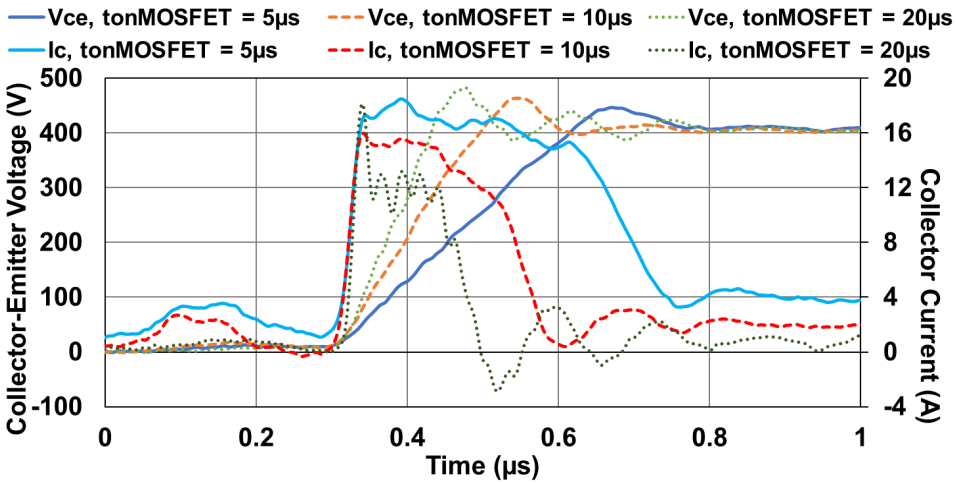


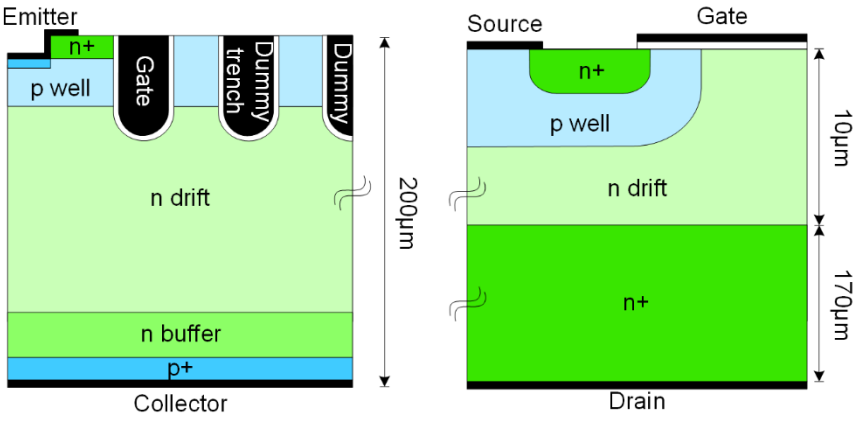
Figure 113 - Turn-off waveforms with false origin of the Si IGBT/SiC MOSFET with varying ton_{MOSFET} for coordinated switching scheme operating in the circuit as given in Figure 109, ambient temperature 298K. Note current and voltage waveforms have been overlaid for ease of comparison

7.4 Simulation Investigation

The material presented in this section has been undertaken solely by the author of this thesis.

2D TCAD Si IGBT and SiC MOSFET models were developed in Sentaurus to further investigate the coordinated switching strategy, without the constraints of the hardware in the experimental rig that limited both the maximum switching current and also ton_{MOSFET}

to 20µs. The 2D IGBT model used (Figure 114 (a)) was the same as that developed in Chapter 3, Section 3.4, with the area factor scaled such that the full 450A module was simulated [107].



(a) (b)

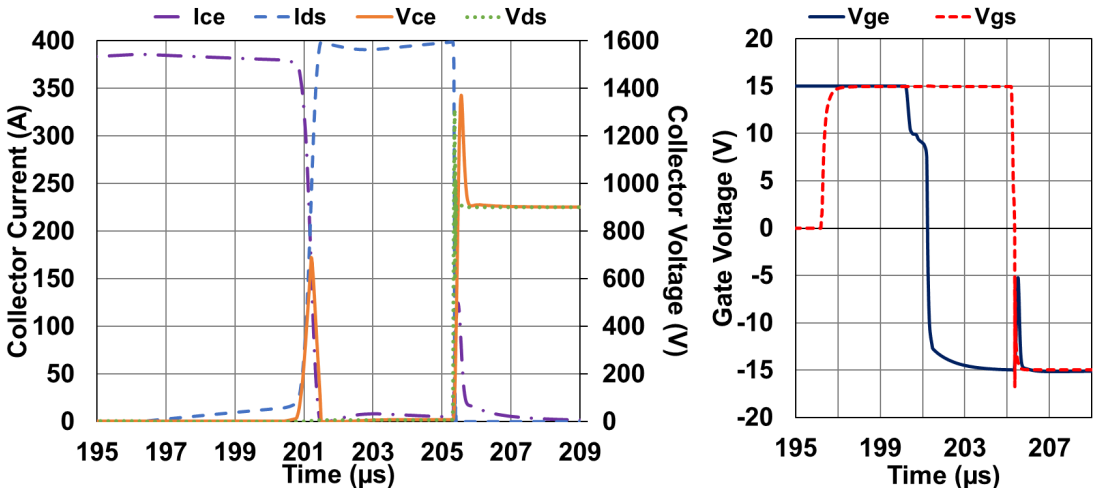
Figure 114 - Schematic of simulated device structures (a) 2D 1.7kV IGBT, (b) 2D SiC MOSFET model with substrate included

The SiC MOSFET model (Figure 114 (b)) has been developed specifically for this study, using a planar gate configuration and an active area of 0.25cm^2 for a device current rating of 150A. To be representative of industry standard devices, the substrate was increased to 170µm, which provides a worst case for the heating conditions discussed in Section 7.4.3. This could be removed by manufacturers if desired to produce a thinner device, which would cool the device faster due to a smaller thermal mass. Section 7.4.4 investigates the effect of reducing the current rating of the SiC MOSFET further, to 45A and 22.5A, representing a 1:10 and 1:20 ratio respectively with the IGBT rated current.

The two models have been simulated using mixed-mode simulations. The SiC MOSFET and IGBT were connected in parallel in a standard inductive load test configuration (as shown in Chapter 3, Section 3.5), switching a 455µH load at 400A and 900V line voltage. A stray inductance of 300nH was accounted for in line with the load inductance, and a further 300nH between the IGBT and MOSFET connections. For both the IGBT module and MOSFET module a 10Ω gate resistor was applied.

7.4.1 Effect of SiC MOSFET on IGBT dV/dt and Switching Losses

Figure 115 provides the simulated turn-off waveforms with $toneff_{MOSFET}$ = 4µs. In this simulation $t_{overlap}$ = 5µs; 4µs was set by the gate drive scheme to ensure that the SiC MOSFET is fully on before turning off the Si IGBT and a further 1µs accounts for the IGBT gate voltage to fall as shown in Figure 115 (b). Throughout the simulations $t_{overlap}$ remains constant and only $toneff_{MOSFET}$ is varied as shown in Figure 108.



(a) (b)

Figure 115 - Simulated turn-off waveform of the Si IGBT/SiC MOSFET coordinated switching scheme in inductive load test, $toneff_{MOSFET}$ = 4µs, ambient temperature 298K, (a) IGBT V_{ce} and I_c with MOSFET V_{ds} and I_d, (b) IGBT and MOSFET gate voltages

Figure 115 displays the same characteristics as shown in the experimental results in Figure 111. For this simulation, $toneff_{MOSFET}$ was 4µs and Figure 115 shows a tail current within the IGBT at the end of the coordinated turn-off event as a result of remaining excess carriers within the device drift region. At ~203µs, the IGBT collector current slightly increases while the MOSFET is conducting. During this time, despite the IGBT gate signal having been driven to -15V, the parasitic capacitances have not discharged because, unlike a normal inductive load turn-off event, the collector-emitter voltage has not increased to the line voltage as it is clamped by the on voltage of the SiC MOSFET. As a consequence, this parasitic capacitance partially discharges, resulting in a temporary increase of electrons in the p-well, increasing the collector current. The full discharge of the IGBT parasitic capacitances occurs at the point of turn off of the MOSFET, as shown by the spike in the collector current and gate-emitter voltage. Due to the presence of stray

inductance, at the point the MOSFET is turned off there is also a collector-emitter voltage spike across the IGBT as a result of the high rate of change of collector current.

A comparison of the collector-emitter voltage for varying MOSFET on-time is given in Figure 116. A false origin has been used in this figure, where t=0µs is equivalent to the point at which all gate signals are low. As shown in the experimental results (Figure 113), increasing the MOSFET on-time increases dV_{ce}/dt, but it also increases the overshoot (at $toneff_{MOSFET}$ = 39µs, $V_{overshoot}$ = 1657V). Unlike the experimental results there is not, however, significant ringing: as the simulation is switching significantly higher currents compared to the experimental data, there are still sufficient carriers within the IGBT at the point of turn-off to prevent the depletion region spreading too far and too quickly through the device, and therefore C_{gc} remains sufficiently large to not induce high frequency oscillations. Figure 116 also shows a significantly larger delay in the collector-emitter voltage rising for the IGBT switching alone compared to the coordinated switching solution. This due to the effective remaining parasitic capacitance in the IGBT when turned off in the coordinated scheme being significantly reduced compared to the IGBT switching alone. The coordinated scheme provides time for a partial discharge of these parasitic capacitances, the removal of some of the accumulation layer charge, and the recombination and diffusion of some of the excess carriers within the drift, thus reducing the delay in the voltage rise V_{ce}.

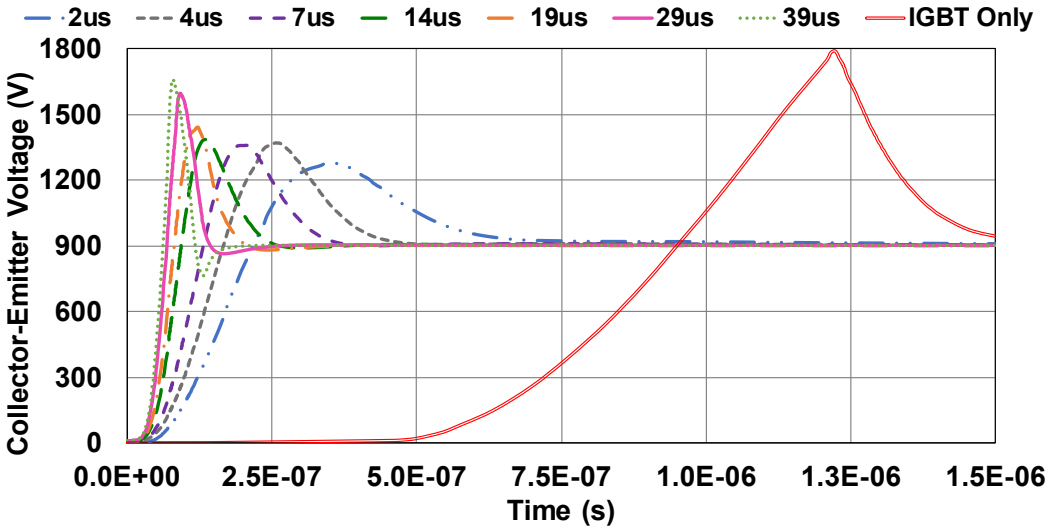


Figure 116 - Comparison of simulated IGBT collector-emitter voltage for varying MOSFET on time ($toneff_{MOSFET}$), ambient temperature 298K. A false origin has been used, where t=0µs is equivalent to the point at which the all gate signals are low.

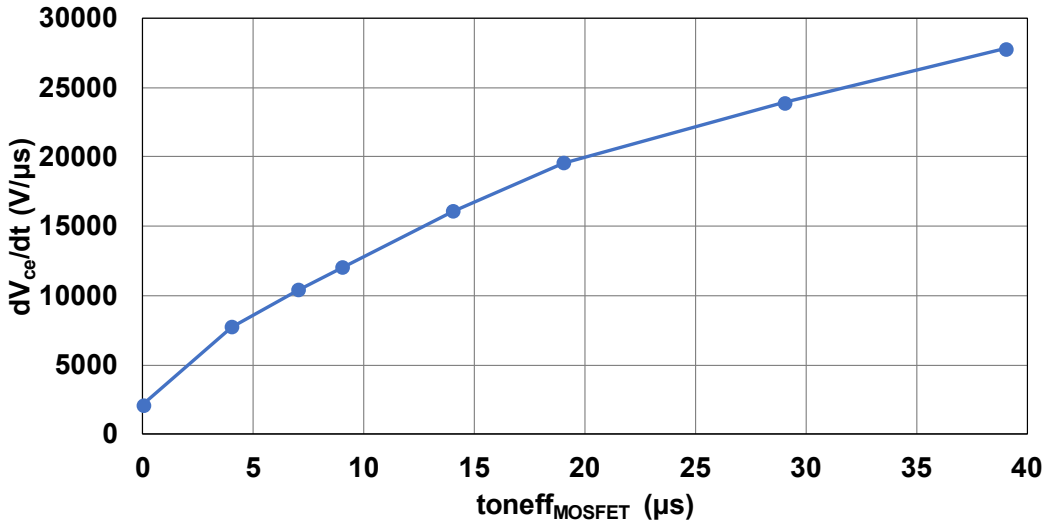


Figure 117 - Relationship between simulated rate of increase of IGBT collector-emitter voltage at turn-off (measured at 10%-90% V_{ce}) and $toneff_{MOSFET}$ for inductive load switching at 400A, ambient temperature 298K

The relationship between dV_{ce}/dt and MOSFET on-time is explored further in Figure 117. For increasing $toneff_{MOSFET}$, the rate of increase of dV_{ce}/dt slows and ultimately begins to saturate. The point at which dV_{ce}/dt begins to saturate is heavily dependent on the carrier lifetime within the IGBT. In the TCAD model, carrier lifetimes are calculated locally and dependent on multiple recombination mechanisms, however a simple MATLAB model allows a carrier lifetime to be easily specified. A MATLAB model of a Si IGBT [168] with a reduced low-level carrier lifetime set to 1µs and a SiC MOSFET model based on that proposed by McNutt [169], demonstrates saturation in the dV_{ce}/dt for $toneff_{MOSFET} >$ 5µs [156]. This therefore suggests the possibility of further optimisation of the switching scheme through localised lifetime control within the IGBT. It is worth noting that the results in Figure 117 show a significantly higher dV_{ce}/dt than given experimentally in Figure 112. Despite both using a 450A rated IGBT module, experimentally only 20A was switched, compared to the 400A as simulated. In the case of the lower current, full conductivity modulation of the drift is still achieved [170] and hence the bipolar element of the IGBT dominates the behaviour, giving an artificially low dV_{ce}/dt.

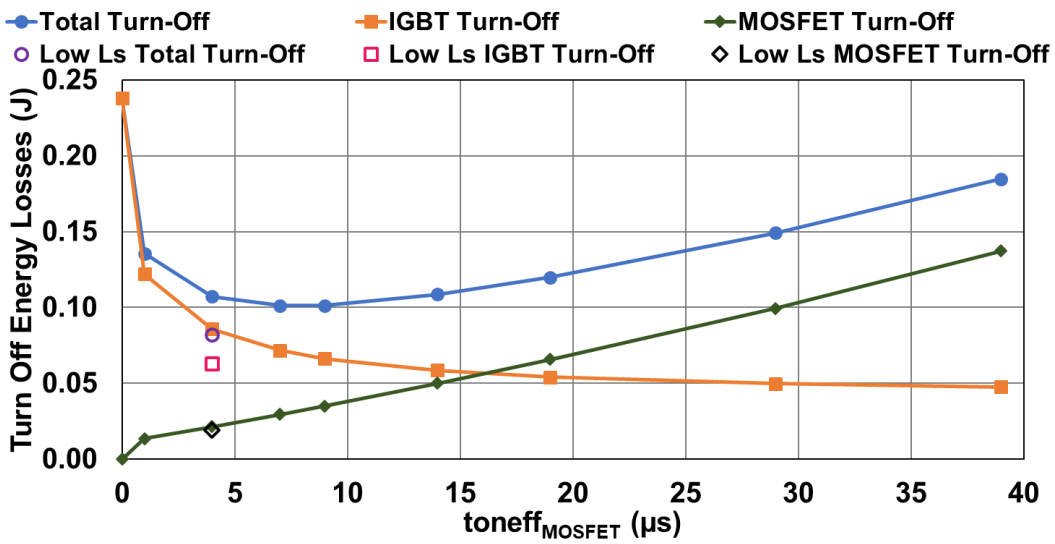


Figure 118 - Relationship between simulated turn-off losses and toneff$_{MOSFET}$ for inductive load switching, ambient temperature 298K

Increasing the dV_{ce}/dt of the IGBT does not reduce the overall turn-off losses indefinitely as MOSFET losses increase with duty cycle. This trade-off is shown in Figure 118, where turn-off losses are calculated from the point in time where the IGBT gate signal falls (including some of $t_{overlap}$ and all of toneff$_{MOSFET}$ as defined in Figure 108). This therefore includes the MOSFET on-state losses, as well as the IGBT and MOSFET turn-off losses. In these simulations the SiC MOSFET has been operated in excess of its nominal device ratings, such that the drain current is significantly higher than the DC rated value. This is acceptable given the relatively short duty cycle of the MOSFET, and the low loss ZVS/ZCS condition at turn-on. It does, however, result in a slightly higher on-state voltage drop across the MOSFET than would traditionally be expected. Despite this, the coordinated switching scheme significantly reduces the overall switching losses compared to the single IGBT device. At most, a 57.5% reduction in turn-off losses is achieved (toneff$_{MOSFET}$ = 9µs). For toneff$_{MOSFET}$ > 15µs, the MOSFET on-state losses begin to dominate, and there is no further benefit in increasing dV_{ce}/dt of the IGBT.

7.4.2 Effect of Stray Inductance on Switching Losses

Further investigations were conducted to discover the effect of stray inductance on the circuit performance. Industry-leading module packaging designs, created specifically for SiC MOSFET modules, have reduced the stray inductance to 35nH/cm^2 [146], [147]. Using these parameters provides an upper bound for the maximum improvement in

performance that could be achieved if, for example, the Si IGBT and SiC MOSFET were co-packaged.

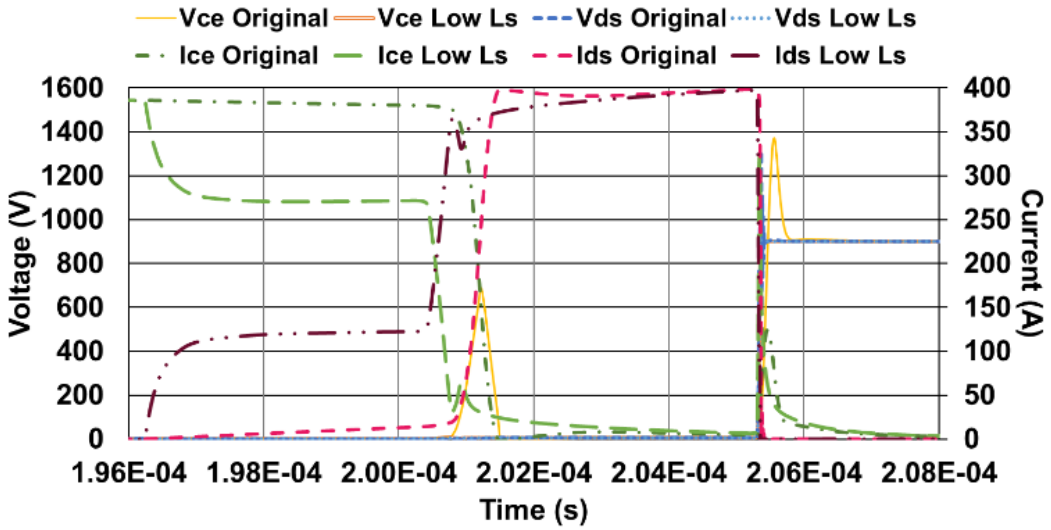


Figure 119 - Simulated turn-off waveform of the Si IGBT/SiC MOSFET coordinated switching scheme in inductive load test, $toneff_{MOSFET}$ = 4µs, ambient temperature 298K, for original and low stray circuit inductance

Figure 118 shows a further reduction in the total power losses of 23.7% compared to the original coordinated switching scheme layout (at $toneff_{MOSFET}$ = 4µs, close to the minimum loss condition), mainly due to an improvement in the stray inductance for the IGBT packaging. Figure 119 compares the two transient waveforms at turn-off. The high stray inductance (original conditions) causes a delay in the rise of the collector voltage and significant overshoot. However, this is not the most dominant effect in terms of power losses. For the original circuit, when the MOSFET is initially switched on, it is unable to efficiently take over the IGBT conduction current due to the large stray line inductance. As a result, there is less time for the recombination process within the IGBT to occur and therefore there is more stored charge within the device when the MOSFET is eventually switched off. The larger stray inductance also resists rapid changes in the current, which contributes further to the overall switching loss. It should be noted that at ~201µs, there is a small spike in the collector current for the low inductance waveform. This is caused by the accumulation charge dissipating away from the gate, causing a localised increase in current. This effect could not be seen in the previous simulation waveforms due to the larger inductance between the IGBT and MOSFET.

7.4.3 Thermal Effects within the Si IGBT and SiC MOSFET

The coordinated switching scheme has been designed to minimise the size of the SiC MOSFET by operating the device in excess of its nominal ratings to reduce the overall cost of the hybrid solution and maximise efficiency. Therefore, it is critical that self-heating effects are considered to determine if it is safe to use the proposed SiC MOSFET under these conditions. To assess this, simulations were conducted at ambient temperatures of 298K and 423K with self-heating for both the IGBT and MOSFET considered, allowing for a heatsink in line with manufacturer's recommendations; a heatsink with 0.6K/W was applied to both the IGBT collector and MOSFET drain, and it was assumed that there was minimal heat loss from the other contacts. It should be noted that the SiC MOSFET is constructed on a SiC substrate (170µm), which is many times the thickness of the active region, and as such acts as a thermally conductive mass. Including self-heating effects did not lead to significant changes in the switching waveform as originally shown in Figure 115.

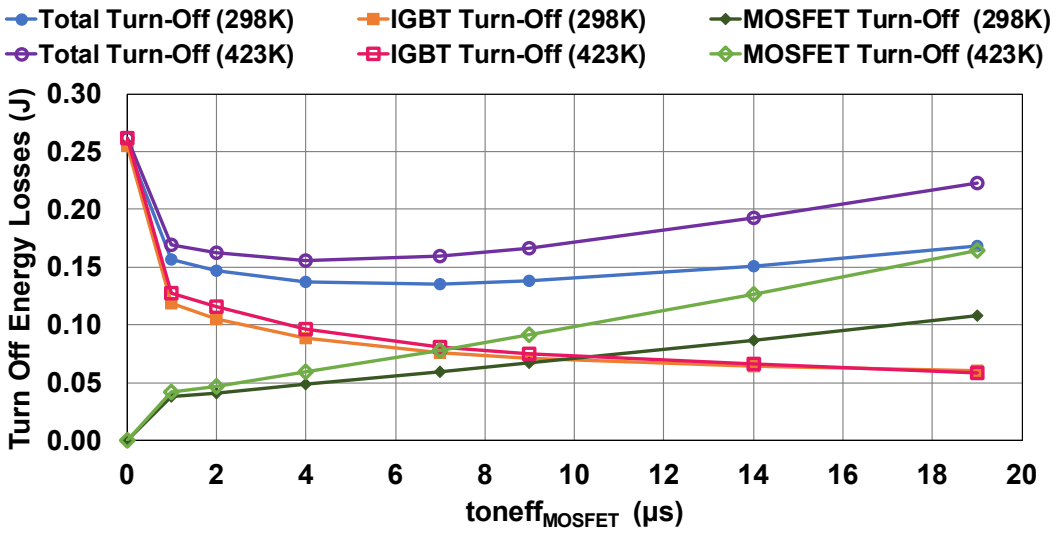


Figure 120 - Relationship between simulated turn-off losses and toneff$_{MOSFET}$ for inductive load switching with device self-heating considered and collector/drain heatsink of 0.6K/W, ambient temperature 298K and 423K

Figure 120 shows the energy losses for different MOSFET duty cycles at both 298K and 423K. At toneff$_{MOSFET}$ = 9µs losses increase by 36% compared to the non-thermal simulations; with the increased losses dominated by the MOSFET heating. This results in a new minimum total loss condition at 298K ambient where toneff$_{MOSFET}$ = 7µs, which

represents a 46.8% reduction compared to the turn-off losses for the IGBT switched alone. For an ambient temperature of 423K, the $toneff_{MOSFET}$ optimum point is reduced further to 4µs since the MOSFET losses have increased, but this is still a 40.3% reduction compared to the single IGBT turn-off under the same conditions. It was found that, for the coordinated scheme, the maximum lattice temperature within the IGBT during turn-off was largely independent of the MOSFET on-time and slightly reduced compared to the IGBT only turn off: at ambient 298K, the IGBT only turn-off maximum lattice temperature was 311K whereas for the coordinated switching IGBT the maximum lattice temperature was 303K, and at 423K ambient, at most a 6K increase in maximum IGBT lattice temperature was measured during the coordinated turn-off event.

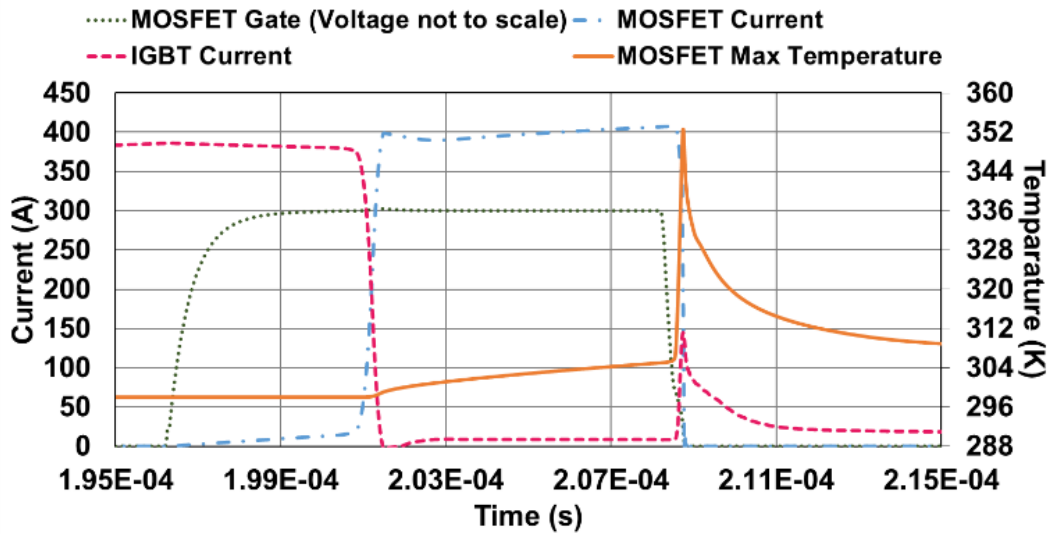
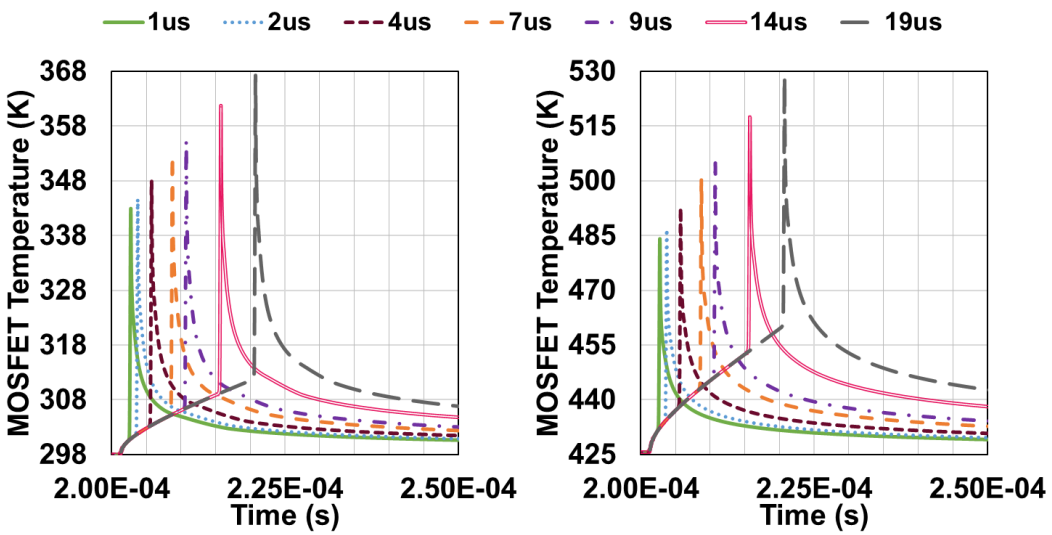
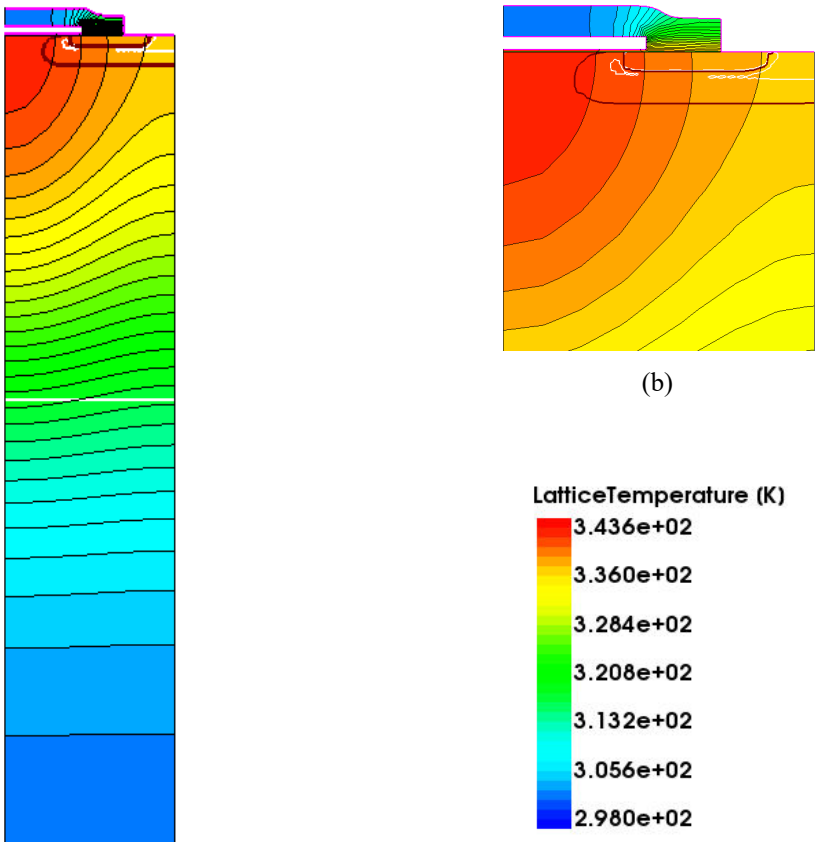


Figure 121 - Simulated turn-off waveform of the Si IGBT/SiC MOSFET coordinated switching scheme in inductive load test with device self-heating effects considered, $toneff_{MOSFET}$ = 7µs, ambient temperature 298K



(a) (b)

Figure 122 - Simulated SiC maximum lattice temperature with time for varying $toneff_{MOSFET}$, (a) ambient temperature 298K, (b) ambient temperature 423K



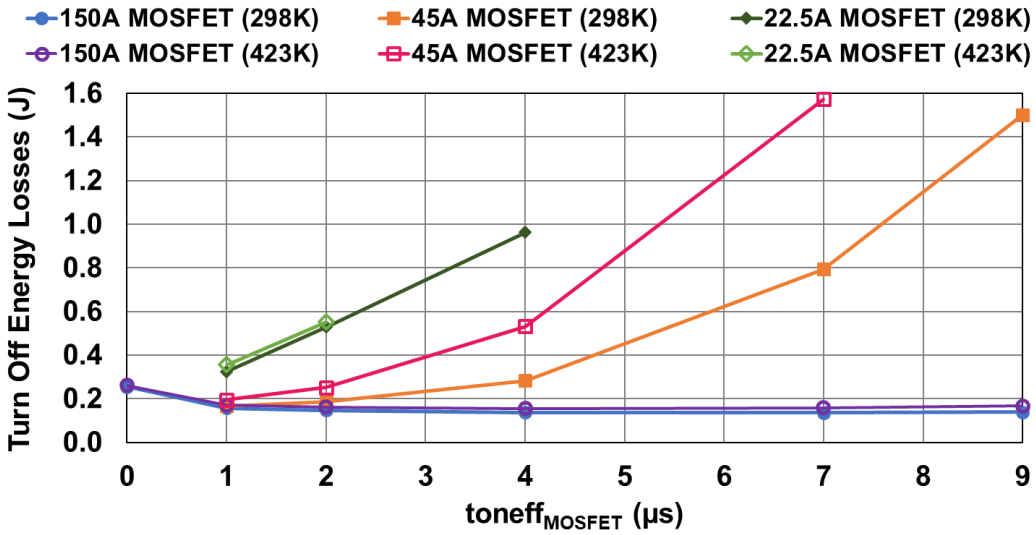
(a)

Figure 123 - Simulated SiC lattice temperature at 208.8µs in Figure 122 for $toneff_{MOSFET}$ = 7µs, ambient temperature 298K, (a) gate and source region of MOSFET (b) zoomed view at gate

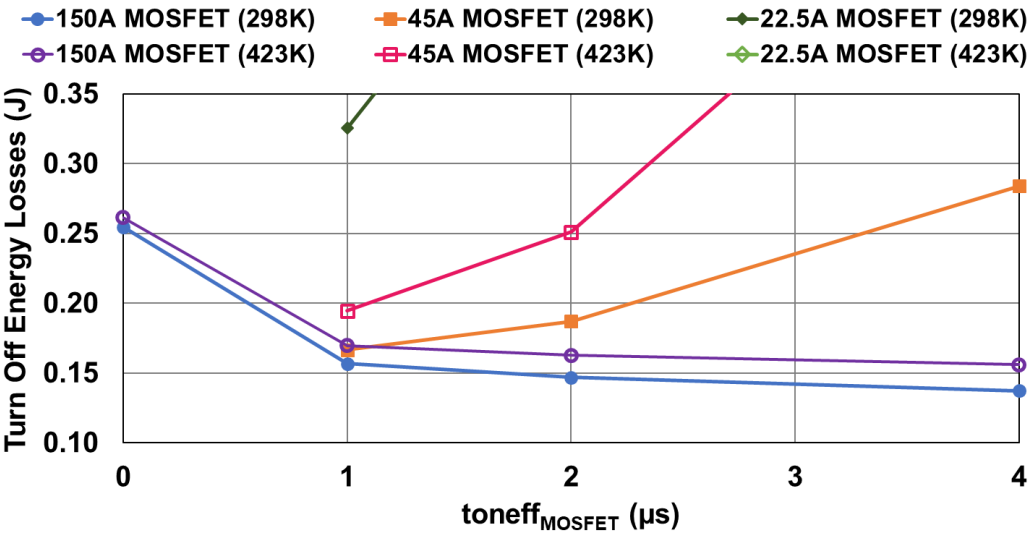
The MOSFET heating was explored in relation to the transient waveforms in Figure 121. Self-heating effects cause a rise in the temperature when the MOSFET is in the on-state and conducting the load current. However, the sharp increase in the maximum lattice temperature of the MOSFET coincidences with the device turning off and the small current spike in the IGBT, caused by excess carriers that have yet to recombine. This is expected given the hard turn-off of the MOSFET. The MOSFET lattice is hottest under the gate at the top of the device as shown in Figure 123, but it rapidly dissipates into the bulk of the device. Figure 122 shows the relationship between the maximum lattice temperature within the MOSFET and the device duty cycle for different ambient temperatures. Despite the increasing temperature with duty cycle, in all cases it takes approximately 16μs for the lattice temperature to recover from the sharp increase caused by the hard switching event and return to the temperature at just prior to turn-off. From Figure 122 (a), at $toneff_{MOSFET}$ = 7μs, it takes 10μs for the lattice temperature to return to within 5% of the device ambient, meaning that a switching frequency in excess of 90kHz is easily achievable for this topology. It is possible that with improved heatsinking and forced air cooling this switching frequency could be increased further.

7.4.4 Minimising the Current Rating of SiC MOSFET

Given the increased manufacturing expense of SiC devices compared to Si, it would be advantageous to minimise the size of the MOSFET to reduce overall costs. In previous simulations the MOSFET was sized to be one third of the IGBT current rating (150A), but a more aggressive ratio is investigated here; 1:10 ratio (45A MOSFET rating) and 1:20 ratio (22.5A MOSFET rating). The ability of the undersized MOSFET to conduct current far in excess of its device ratings will be limited by the heating of the device and the speed at which this heat can be dissipated. As a result, the same simulation conditions as discussed in Section 7.4.3 were used for this analysis.



(a)



(b)

Figure 124 - Relationship between simulated turn-off losses and toneff$_{MOSFET}$ for varying size of SiC MOSFET under inductive load switching with device self-heating considered and collector/drain heatsink of 0.6K/W, ambient temperature 298K and 423K; (a) full graph, (b) zoom toneff$_{MOSFET}$ 0 to 4µs

Figure 124 compares the total turn-off losses for the coordinated switching scheme with the various sizes of MOSFET. It should be noted that there was no significant change to the IGBT turn-off losses (Figure 120) or the current voltage waveform (Figure 121) when using the smaller MOSFETs. It can be seen from Figure 124 that using the 22.5A MOSFET (1:20 ratio) presents no advantage compared to the single IGBT turn-off under the same conditions, whereas using the 45A MOSFET (1:10 ratio), under certain conditions, does reduce overall turn-off losses. When toneff$_{MOSFET}$ ≤ 2µs, for both ambient temperatures, the 45A MOSFET scheme has reduced turn-off losses compared

to the single IGBT turn-off. In particular at 298K for $toneff_{MOSFET}$ = 1µs, losses are only slightly increased compared to using the 150A MOSFET. However, the significant heating of the 45A SiC MOSFET limits the benefits of the coordinated switching scheme, and despite reducing the excess carriers in the IGBT drift region, the overall switching losses increase due to the large on-state losses of the MOSFET.

Temperature	MOSFET Current Rating		
	150A	45A	22.5A
298K	Did not fail	9µs	4µs
423K	Did not fail	7µs	2µs

Table 4 - Maximum permitted $toneff_{MOSFET}$ to prevent breakdown of SiC MOSFET for varying SiC MOSFET current ratings, under inductive load switching with device self-heating considered and collector/drain heatsink of 0.6K/W

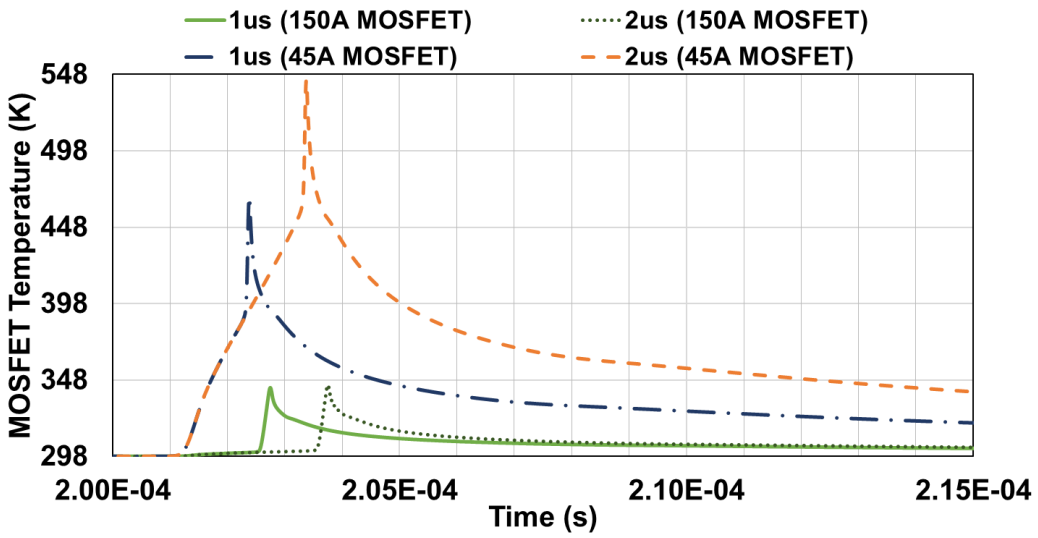


Figure 125 - Simulated SiC maximum lattice temperature with time for varying $toneff_{MOSFET}$ and MOSFET current rating, ambient temperature 298K

This heating of the SiC MOSFET often resulted in the destructive failure of the device if $toneff_{MOSFET}$ was too large; Table 4 summaries the maximum permissiable $toneff_{MOSFET}$ for the simulated heatsink conditions. It would be possible to extend the MOSFET on-time further if more aggressive cooling conditions were implemented, such as forced air

or water cooling, however, this would significantly increase the overall cost of the system. Figure 125 shows the relationship between the maximum lattice temperature within the MOSFET for the 150A and 45A devices, and the device duty cycle for an ambient temperature of 298K. Only the data for $toneff_{MOSFET}$ of 1µs and 2µs was considered as a longer MOSFET on-time did not result in an efficiency saving when using the 45A SiC MOSFET in this scheme. Both sizes of MOSFET exhibit a rapid temperature increase which coincidences with the device turning off, however, the 45A MOSFET also has significant heating during conduction. This consequently increases the maximum lattice temperature by almost 60% compared to the 150A rated device ($toneff_{MOSFET}$ = 2µs) and hence severely limits the maximum switching frequency of the scheme: for the lattice temperature to return within 5% of the ambient temperature takes 29µs for the 45A MOSFET with $toneff_{MOSFET}$ = 1µs and 95µs for the 45A MOSFET with $toneff_{MOSFET}$ = 2µs, which for the 150A MOSFET takes only 2µs and 3µs respectively. This results in a maximum switching frequency of 34kHz for the 45A MOSFET (with $toneff_{MOSFET}$ = 1µs), however this still presents a 34.6% improvement in turn-off losses. Therefore, for low cost, relatively low switching frequency applications, it is advantageous to reduce the size of the SiC MOSFET to this more extreme level, however, careful consideration must be given to the cooling conditions for the SiC device.

7.5 Conclusion

This chapter presents a coordinated switching scheme using a SiC MOSFET in parallel with a Si IGBT to achieve a higher dV_{ce}/dt and lower losses at turn-off compared to a stand-alone IGBT switch. By switching the SiC MOSFET on towards the end of the IGBT duty cycle under ZVS/ZCS condition, it has been demonstrated that the MOSFET is able to act as a bypass route for the load current. This enables the IGBT MOS channel to be switched off while the MOSFET is conducting, providing time for the excess carriers within the IGBT to recombine, reducing the tail current, and greatly increasing the IGBT dV_{ce}/dt when the MOSFET is subsequently turned off. This switching scheme has been demonstrated experimentally and extensive simulations have been conducted to investigate the optimum switching conditions. TCAD simulations have established that there is an optimum condition and that, after a relatively short MOSFET on-time, overall system losses are significantly reduced. Increasing the MOSFET on time beyond this

time, and hence increasing the dV_{ce}/dt of the IGBT further does not improve the overall performance since the MOSFET on-state losses begin to dominate. Despite operating the SiC MOSFET in excess of its nominal ratings, in order to reduce the overall cost of the hybrid solution and maximise efficiency, simulations of the lattice heating have shown that the SiC MOSFET cools sufficiently quickly to support an overall switching frequency for this topology in excess of 90kHz for a 450A IGBT module and 150A rated MOSFET module (33% of IGBT current rating). It has been demonstrated that, after accounting for self-heating within the devices, a 46.8% reduction in turn-off losses can be achieved using this 150A SiC MOSFET, compared to a single IGBT turn-off under the same conditions. If the MOSFET size is reduced further to a 45A rated device (10% of IGBT current rating), to minimise the overall system cost, it has been shown that, after accounting for self-heating within the devices, a 34kHz switching frequency can be supported while still improving the switching losses by 34.6% compared to a single IGBT turn-off under the same conditions.

Chapter 8

Conclusions and Future Work

Power semiconductor devices, estimated to control 50% of the electricity used worldwide [1], are at the heart of all power electronics systems. With the move towards electrification for transportation, renewable energy sources, and industrial applications, demand for efficient IGBT modules is increasing: at the time of writing, IGBTs and IGBT modules account for 28% of the $17.5 billion power semiconductor industry ($4.8 billion market share), and in the next 5 years the IGBT market is set to increase in value to $6.18 billion [14]. *Optimisation of the IGBT to produce even a small increase in efficiency therefore has the potential to have a significant impact upon global energy consumption. Meeting these applications and new end-user demands requires development of highly reliable and efficient modules. This thesis outlines work towards this objective.*

8.1 Conclusions of the Thesis

Despite the emergence of wide bandgap materials, silicon is still the primary material for power semiconductor devices as material and processing costs of silicon are significantly lower compared for these emerging materials. Particularly for power IGBTs, both GaN and SiC are not suitable; GaN is only suitable for lateral devices and with the inbuilt potential of a SiC p/n junction being 2.7V, this negates the other material benefits offered by SiC.

The IGBT itself is often viewed as the combination of a power MOSFET and a bipolar transistor. It therefore offers a compromise between on-state and switching performance making it the dominant power device in the 600V to 4.5kV range [2], although Si IGBTs are commonly produced up to 6.5kV. Amongst numerous other applications, these devices are used in charging electric vehicles, feeding the power generated by wind turbines or solar cells into the national grid, controlling motors in electric cars and powering the electric train network. Any energy consumed by power transistors in these applications is wasted energy. With global warming becoming a critical issue, there is an immediate need to reduce our carbon footprint and one way to achieve this is to improve the efficiency of the power transistor itself. Given the number of power devices used around the world, even a fractional reduction in their losses could have a global impact on total energy consumption.

Improving the efficiency of the IGBT has been addressed throughout this thesis, by undertaking extensive 3D TCAD simulations and, where possible, obtaining experimental verification. This has been approached in several different ways; optimising existing designs to increase reliability, developing novel switching schemes to reduce losses, combining device structures to improve performance and designing a new novel device to address operational issues.

These findings are summarised in more detail below.

- New IGBT designs are becoming increasingly reliant on simulation tools that allow for rapid device development which, due to the cost and time associated with fabrication, could not be achieved by manufacturing prototypes. TCAD simulations enables the physical interactions within the device to be modelled more accurately than an equivalent compact circuit model, but these simulations are computationally expensive and typically most design engineers develop these TCAD models only in

2D. The results in Chapter 3 highlighted the inaccuracies of a 2D model and justified the benefit of developing these transistor models in 3D to ensure that the device performs as expected when manufactured.

- Based upon a commercial IGBT, Chapter 3 detailed the development of a leading TCAD simulation model of the IGBT using novel 3D modelling techniques, which works in all modes of operation including static and dynamic as well as during fault conditions such as short-circuit events. To minimise computational effort, the simulated cell represented the smallest possible replicating structure; equivalent to 0.000166% of the device active area. However, using this model it was found that processing variations across the die became significant. Large variations between the experimental data from the manufactured device and the simulation model lead to the discovery of widespread birds-beaking within the IGBT – an uncontrollable processing defect that the manufacturer was unaware of. The birds-beak phenomenon was imaged using a scanning electron microscope and the results in Chapter 3 highlighted how this processing uncertainty has a strong effect on the accuracy of simulations. It was demonstrated that the birds-beak effect can be accounted for in simulation by a two-device model, which allows for small-scale and large-scale device behaviours to be matched while limiting the computational effort.
- The effect of this birds-beaking was investigated further in Chapter 3. In practical terms, this phenomenon results in the designer struggling to validate models and underappreciating the true behaviour of the device. In terms of device performance, birds-beaking caused a 32% reduction in short-circuit endurance time for the device as the areas of lower threshold (non birds-beak) conduct 25.2% higher current density compared to regions of the device which suffer from birds-beak.
- Current processing limitations mean that the birds-beak cannot be eliminated directly when using the existing n+ implant. Therefore, to overcome this issue, an alternative n+ emitter implantation was proposed, using a combination of arsenic and phosphorus, so that the device performance is unaffected by the presence of birds-beaking. This modification requires minimal extra fabrication steps. Although the additional phosphorus implant reduces the threshold of the device compared to the original model designers can compensate for this by increasing the p-well doping concentration, which will also help prevent thyristor latch-up and punch-though under breakdown conditions.

- Chapter 4 used the verified 3D IGBT model to determine an optimum cell design that considered critical 3D effects, and compared different methods to modify the emitter geometry, which had previously not been investigated in literature. In particular, the effect of the geometric properties of a trench IGBT cell on the saturation current and on-state voltage was studied to produce a set of design rules. Previous studies had only investigated one variation of the emitter geometry. Extensive simulations revealed that there are competing effects within the device as the emitter geometry is varied. For small cells, or cells with a limited channel depth (z-dimension), the reliability improves (reducing saturation current) but at the expense of on-state losses. This is attributed to hole current modulation of the channel; whereby the bipolar action of the IGBT is limited and the behaviour becomes more like that of a power MOSFET. For larger cells or cells with an extensive channel depth, it is possible to partially trigger the parasitic thyristor structure, resulting in an increased susceptibility to latch up under short circuit conditions. Dummy trenches are necessary to control the hole current flow at the top of the device, however increasing the number of dummy trenches beyond 0.5 to reduce channel density and thus the saturation current is at the designer's discretion and provides a trade-off with the on-state voltage. However, increasing the number of dummy trenches beyond two is undesirable as it results in a significant increase in on-state losses but only a minimal reduction in saturation current. It was also shown that the emitter geometry has no effect on IGBT turn-off losses.
- The module used for the 3D simulation study in Chapter 3 contained both IGBTs and diodes co-packaged, as both an anti-parallel diode and power device are required together for most power electronic applications. The Reverse-Conducting IGBT (RC-IGBT) concept integrates this antiparallel diode structure within the IGBT itself, in a similar fashion to the inherent body diode within a power MOSFET. The RC-IGBT has several benefits over a separate IGBT and diode solution and has the potential to become the dominant device within these power electronic applications. However, the device suffers from many undesirable design trade-offs that have prevented its widespread use, most prominently a snapback in the on-state characteristic that can lead to overheating and ultimately destructive failure of the device. To overcome these issues, many variations of the RC-IGBT have been proposed in literature, the most promising of which were simulated under the same conditions such that they could be directly compared. The results, given in Chapter

5, showed that these various concepts either present a trade-off in performance, an inability to be manufactured, or a requirement for a custom gate drive, which significantly increases the cost and complexity of the system.

- Following this critical review of existing RC-IGBT structures, Chapter 6 proposed a new RC-IGBT device that is manufacturable using current state of the art techniques, does not suffer from snapback and is compatible with a standard gate drive. This new 'Dual Implant SuperJunction RC-IGBT' for the first time enables a full SuperJunction (SJ) structure to be achieved in a 1.2kV device using current fabrication techniques, by applying two separate SJ implantations; one from the anode side and the other from the cathode side. It was demonstrated that there is no requirement for the pillars to be aligned, but to achieve the performance benefits, the maximum permissible gap between the anode and cathode SJ pillars is 10μm such that there is negligible snapback in the on-state, and a maximum pillar overlap of 2μm can be tolerated without degradation in the breakdown capabilities. It was shown in simulation that the new Dual Implant SJ RC-IGBT can result in a 77% reduction in turn-off losses compared to a conventional RC-IGBT.
- The IGBT has excellent on-state performance due to the bipolar action of the device, however, this property restricts the IGBT dV_{ce}/dt at turn-off. It is not possible to improve the dV_{ce}/dt of the IGBT without sacrificing the on-state behaviour, and therefore an alternative approach was investigated in Chapter 7. Silicon-carbide MOSFETs are emerging into the market as SiC has higher mobility and increased thermal stability compared to silicon, but the on-state losses are still higher than the Si IGBT and the cost per amp of SiC is larger due to increased material and processing costs. Therefore, a novel coordinated switching scheme using both a Si IGBT and SiC MOSFET was proposed, which aimed to improve turn-off losses within the IGBT without sacrificing on-state losses while minimising the overall system cost.
- In this new switching scheme, the SiC MOSFET was turned-on towards the end of the IGBT duty cycle, under a ZVS/ZCS condition, to act as a bypass route for the load current, giving time for charge within the IGBT to recombine and hence improve the dV_{ce}/dt. The system was optimised to use a SiC MOSFET in excess of its nominal ratings, reducing the cost of the device, and, to ensure it could be operated safely under these conditions, extensive simulations to model the heating of the semiconductor lattice were conducted. These simulations showed that the SiC

MOSFET cools sufficiently quickly to support an overall switching frequency for the topology in excess of 90kHz, and a 46.8% reduction in turn-off losses was achieved compared to a single IGBT turn-off under the same conditions. If the MOSFET size is reduced further to a 45A rated device, to minimise the overall system cost, it has been shown that, after accounting for self-heating within the devices, a 35kHz switching frequency can be supported while still improving the switching losses by 34.6% compared to a single IGBT turn-off under the same conditions.

8.2 Future Work

The work, detailed in this thesis, can be extended in several directions.

- Manufacture of the modified IGBT design with the arsenic phosphorus co-implantation technique to eliminate the effects of birds-beak would be the next logical step to improve the trench IGBT performance. A future study could be conducted alongside a commercial partner to verify the simulation model results, with the intention of developing the device for mass manufacture.
- The Dual Implant SJ RC-IGBT concept should also be manufactured to verify the simulation results. In particular, future work should focus on refining the suggested process flow, presented in Chapter 6, as although the current suggested method is possible (and comparatively significantly easier than a deep SJ trench from a single etch), it still presents numerous technical challenges. Work could also be performed to optimise the diode performance, which was not considered in detail in the original study. A further development could investigate the possibility of commercialisation of the device as it has the potential to be a disruptive technology within the RC-IGBT market. In particular, efforts could concentrate on the optimisation of the device within typical applications to ensure maximum efficiency in these situations.
- The SiC MOSFET/Si IGBT switching scheme has been successfully demonstrated experimentally at lower powers and extensive simulations have shown its suitability at higher currents. However, to progress this research, the technology should be demonstrated experimentally in a multilevel converter suitable for HVDC applications. Particular attention should be given to the gate drivers, and optimising the switching scheme, without significantly increasing the overall cost and complexity of the system. Further work studying the effects of stray inductance on

the system could also be explored by co-packaging the SiC MOSFET die and Si IGBT die within the same module (but still with separate gate control). The possibility of a further reduction in the SiC MOSFET size could be investigated, either by optimising the heatsink (forced air or water cooling) or by using multiple, significantly smaller, SiC MOSFET die per Si IGBT switch, as there may be a cost benefit.

- Future research could also focus on designing a new and novel IGBT that integrates monitoring sensors directly onto the IGBT die, with the intention to detect degradation in the lifetime of IGBT modules while in service. Degradation is usually caused either by fluctuating environmental conditions or by manufacturing imperfections, such as the birds-beak effect. It is known that there are three main indicators that an IGBT is degrading and is susceptible to failure; for all ambient temperatures, threshold voltage increases, transconductance increases and the collector-emitter on-voltage reduces. This study could investigate the use of silicon sensors to directly measure these IGBT parameters, rather than inferring them from the converter performance, which is typically the method used. Beginning with simulations based on the techniques developed in this thesis, the suitability of the 'smart IGBT' concept could be demonstrated and ultimately the design could progress to prototype development and experimental verification.

Appendix

A.1. 3D Simulation Parameters for Mobility Models in Silicon

The simulation parameters, for the mobility models when simulating silicon IGBT structures in 3D, were used as listed below. 2D simulation models used the default silicon values as provided in [92].

Enhanced Lombardi Model (parameter set EnormalDependence):

B = 1.805e+07, 3.02e+07 [cm/s]

C = 5.1e+03, 8.36e+03 [$cm^{5/3}/(V^{2/3}s)$]

N0 = 1, 1 [cm^{-3}]

lambda = 0.0233, 0.0119

k = 1, 1

delta = 1.79e+18, 4.1000e+15 [V/s]

A = 2.688, 2.18

alpha = 2.74e-20, 3.13e-20

aother = 0.0000e+00, 0.0000e+00

N1 = 1, 1 [cm^{-3}]

nu = 0.0767, 0.123

eta = 1.0e+300, 1.0e+300 [$V^2/(cm \cdot s)$]

l_crit = 1.0000e-06, 1.0000e-06 [cm]

Canali Model for High-Field Saturation (parameter set HighFieldDependence):

beta0 = 1.109, 1.213

betaexp = 0.66, 0.17

alpha = 0.0000e+00, 0.0000e+00

K_dT = 0.2, 0.2

E0_TrEf = 4.0000e+03, 4.0000e+03

Vsat_Formula = 1 , 1

vsat0 = 1.0700e+07, 8.3700e+06

vsatexp = 0.87, 0.52

Philips Unified Mobility Model (parameter set PhuMob):

mumax_As = 1.4170e+03 [cm^2/Vs]

umin_As = 52.2 [cm^2/Vs]

theta_As = 2.285

n_ref_As = 9.6800e+16 [cm^{-3}]

alpha_As = 0.68

mumax_P = 1.4140e+03 [cm^2/Vs]

mumin_P = 68.5 [cm^2/Vs]

theta_P = 2.285

n_ref_P = 9.2000e+16 [cm^{-3}]

alpha_P = 0.711

mumax_B = 4.7050e+02 [cm^2/Vs]

mumin_B = 44.9 [cm^2/Vs]

theta_B = 2.247

n_ref_B = 2.2300e+17 [cm^{-3}]

alpha_B = 0.719

nref_D = 4.0000e+20 [cm^{-3}]

nref_A = 7.2000e+20 [cm^{-3}]

cref_D = 0.21

cref_A = 0.5

me_over_m0 = 1

mh_over_m0 = 1.258

f_CW = 2.459

f_BH = 3.828

f_e = 1

f_h = 1

alpha1_g_k = -7.2169e-01

alpha1_g_m = -1.5952e+00

A.2. Simulation Parameters for SiC Models

The simulation parameters, for the models when simulating SiC MOSFET structures in 2D, were used as listed below. A full list of the models that these parameters apply to is given in [92].

Relative permittivity (parameter set Epsilon):

epsilon = 9.66

Specific heat capacity (parameter set LatticeHeatCapacity):

cv = -2.139

cv_b = 2.242e-2

cv_c = -3.130e-5

cv_d = 1.546e-8

Incomplete Ionisation (parameter set Ionization):

For 4H-SiC Nitrogen hexagonal site;

E_0 = 0.0709

alpha = 3.3800e-08

g = 2.0

Xsec = 1.0000e-12

For 4H-SiC Nitrogen cubic site;

E_0 = 0.1237

alpha = 4.6500e-08

g = 2.0

Xsec = 1.0000e-12

For 4H-SiC Boron;

E_0 = 0.293

alpha = 0

g = 4.0

Xsec = 1.0000e-12

For 4H-SiC Al;

E_0 = 0.265

alpha = 3.60e-08

g = 4.0

Xsec = 1.0000e-12

4H-SiC Phosphorus hexagonal site;

E_0 = 0.055

alpha = 6.386e-9

g = 2.0

Xsec = 1.0000e-12

Bandgap narrowing, Slotboom model (parameter set Slotboom):

Chi0 = 3.24

Bgn2Chi = 0.5

Eg0 = 3.285

alpha = 0.033

beta = 1.0e5

Nref = 1.e+17

Ebgn = 0.009

Isotropic density of states mass for electrons (parameter set eDOSMass):

Formula = 1

a = 0.95481

ml = 0.95481

mm = -2.3367

Doping Dependent Masetti Model (parameter set DopingDependence):

formula = 1, 1

mumin1 = 40, 15.9

mumin2 = 40, 15.9

Pc = 0, 0

Cr = 1.94e17, 1.76e19

alpha = 0.61, 0.34

mu1 = 0, 0

Cs = 3.43e20, 6.1000e20

beta = 2, 2

Enhanced Lombardi Model (parameter set EnormaDependencel):

B = 1e6, 9.92e06

C = 280, 2.95e03

N0 = 1, 1

lambda = 0.125, 0.0317

k = 1, 1

delta = 5.82e14,2.0546e14

A = 2, 2

alpha = 0.0, 0.0

N1 = 1, 1

nu = 1, 1

eta = 5.82e30, 2.055e+30

l_crit = 1.0e-06, 1.0e-06

Isotropic density of states mass for holes (parameter set hDOSMass):

Formula = 1

a = 1

b = 6.92e-2

c = 0

d = 0

e = 1.88e-6

f = 0

g = 6.58e-4

h = 0

i = 4.32e-7

mm = 0

Canali Model for High-Field Satruation (parameter set HighFieldDependence):

beta0 = 1.2, 1.2

betaexp = 1.0000e+00, 1.0000e+00

alpha = 0.0000e+00, 0.0000e+00

K_dT = 0.2, 0.2

E0_TrEf = 4.0000e+03, 4.0000e+03

Ksmooth_TrEf = 1, 1

Vsat_Formula = 1, 1

vsat0 = 2.2e+07, 2.2e+07

vsatexp = 0.44, 0.44

Avalanche Generation Okuto–Crowell model (parameter set OkutoCrowell):

a = 2.10e07, 2.96e07

b = 1.70e07, 1.60e07

c = 0.0, 7.511e-3

d = 0.0, 1.381e-3

gamma = 0.0, 0.0

delta = 1.0, 1.0

Auger recombination (parameter set Auger):

A = 5e-31, 2e-31

B = 0.0, 0.0

C = 0.0, 0.0

H = 0.0, 0.0

N0 = 1.0e+18, 1.0e+18

Shockley-Read Hall Recombination (parameter set Scharfetter):

taumin = 0.0, 0.0

taumax = 2.50e-6, 0.5e-6

Nref = 3.0e17, 3.0e17

gamma = 0.3, 0.3

Talpha = 1.72, 1.72

Etrap = 0.0000e+00

A.3. Summary Table of RC-IGBT Concepts

Concept	Advantages	Disadvantages
RC-IGBT with anti-parallel thyristor [113], [125], [126]	Narrow p-layer (depth Dp) acts as a barrier to electrons to minimise snapback effect. Introduction of floating n-dots in the n-buffer improved switching characteristics and snapback became less pronounced as more n-dots were removed. Addition of a dielectric trench either side of n+ column suppressed snapback and resulted in a more uniform current distribution by paralleling multiple thyristor structures in the device.	Minimising snapback in the forward conduction (triggering pnp faster) induces snapback in the reverse characteristic. There is a trade-off between snapback and switching characteristics. Removal of n-dots increased turn-off time. Addition of a dielectric trench either side of n+ column worsened on-state characteristics. Device has not been manufactured.
Pseudo-double anode RC-IGBT (PDS-RC-IGBT) [127]	Snapback can be supressed as diode/thyristor structure makes no contribution to current flow. Reverse conduction is achieved by the floating contact ensuring the bipolar structure is in a collector-base short-circuited configuration. Device has uniform current distribution compared to a conventional RC-IGBT and has an	Higher on-state losses in reverse conduction due to two series connected diode structures. In forward conduction the device has reduced injection efficiency compared to a conventional RC-IGBT structure. Under high current applications when the parasitic thyristor structure is used, in reverse conduction the device exhibits a negative resistance

	increased SOA. Structures can be modified for larger current density applications by triggering parasitic thyristor structure which presents lower on-state losses in the forward conduction mode.	characteristic. Device has not been manufactured.
RC-IGBT with floating p-region [117], [121], [129]	For large currents, the npn transistor (n-collector, p-float, n-drift) can provide a low-impedance current path. For small currents, the p-float acts as a barrier to electrons with the oxide trench, and forms a high-resistance collector short path, suppressing snapback. As the length of the p-float is increased, on-state voltage drop is reduced, and snapback is reduced (can be removed). Structure of p-plug on top of oxide trench improves current distribution, thus increasing reliability (reduced likelihood of hotspots).	Increasing the length of p-float increases turn-off losses. Structure of p-plug on top of oxide trench suffers from snapback characteristics. Fabrication of structures are complex and costly due to the requirement for backside photolithography. There is nonuniform current distribution in both conduction modes. Device has not been manufactured.
Alternating Buffer (AB) RC-IGBT [130]	The floating p buffer implants act as an electron barrier which, with certain geometry, eliminates snapback. Increasing both the width and length of the p buffer implant suppresses snapback. Snapback is suppressed for a much narrower device width compared to both the conventional RC-IGBT and the RC-IGBT with floating p-region. 20% reduction in switching losses compared to a conventional RC-IGBT.	Base punch through of the parasitic pnp transistor (p+ collector/n-drift/p buffer) reduces blocking capability of the device. Increasing the width of the p buffer implant increases switching losses. Increasing the length of the p buffer reduces injection efficiency and increases IGBT on-state losses. Device has not been manufactured.
RC-IGBT with double gate structure [71], [131]	Device has structural symmetry in the forward and reverse direction and inherently has a reverse conduction path to serve as a FWD. Turn-off loss is minimised when operating in quasi-IGBT and MOSFET mode.	Complicated gate drive requirements as device has 2 gates and 4 modes of operation. [IGBT (single gate positive), Quasi-IGBT (both gates positive), MOSFET (current lower than threshold), Blocking mode]. Transition

	Automatically-Controlled Gate RC-IGBT (AC-RC-IGBT) shorts the second gate to the n-buffer region such that only single gate control is required. No snapback occurs and structure can be modified to trigger MCT for higher currents. Device has been manufactured.	from Quasi-IGBT to MOSFET mode exhibits snapback. AC-RC-IGBT has higher on-state resistance compared to RC-IGBT, suffers from localised hotspots and in MCT mode snapback occurs in the reverse characteristic.
Tunnelling IGBT [118]	Reverse conduction achieved by electrons tunnelling from p-collector to n-tunnel. Snapback can be suppressed by increasing the doping of p-collector and n-tunnel. Exhibits soft turn-off characteristics with small reverse recovery and minimal voltage overshoot. Fabrication does not require backside photolithography or need to account for nonuniform current distribution.	Trade-off between snapback characteristics and diode mode conduction losses. Relatively long current tail in the turn-off making it unsuitable for high frequency applications. Difficult to manufacture a very thin tunnel layer with such high doping. Device has not been manufactured.
BIGT (Bi-mode Integrated Gate Transistor) [109], [115], [136], [137]	Pilot IGBT sized to reduce snapback, with radial layout of anode shorts removing secondary snapback in the on-state. Turn-off losses minimised when operating in quasi-IGBT and MOSFET mode. Suitable for paralleling multiple devices as there is a strong positive temperature coefficient. Soft turn-off behaviour in both conduction modes. Reduced temperature ripple for same area of silicon compared to a separate IGBT/diode. Device has been manufactured.	Radial layout of anode shorts presents a trade-off between conduction losses in the IGBT and diode modes. Optimising the trade-off in reverse recovery losses in diode mode and on-state losses in IGBT mode worsens the performance of the device under surge and increases conduction losses which limits device capability at low frequencies. Complex gate drive schemes are required to optimise switching and on-state performance.
RC-IGBT with superjunction structure [66]	Trench Field Stop (TFS) Superjunction (SJ) RC IGBT removes snapback using superjunction structure at cathode. Anode short provides reverse	For a structure comparable with commercially available COOLMOS, snapback is present in the waveform. Increasing length of p-pillar (Ymid) can

	conduction path. Increasing doping concentration of pillars reduces on-state losses for a given breakdown voltage. Increasing length of p-pillar (Ymid) reduces snapback (can be eliminated). Diode characteristic unaffected by superjunction structure.	increase switching losses due to an oscillatory gate voltage. Increasing doping concentration of pillars increases turn-off time. Device has not been manufactured, but a SJ SPT IGBT has been reported [69].
Schottky Controlled Diode within RC-IGBT [141]	Peak diode reverse recovery current was reduced by 49% compared to a conventional RC-IGBT. Reduced tail current in transient waveforms.	Increased ringing in the diode reverse recovery waveforms. The study did not comment on the overall performance of the RC-IGBT, particularly in reference to the behaviour in IGBT mode. Device has not been manufactured.

Table 5 - Advantages and disadvantages of RC-IGBT concepts proposed in literature

References

[1] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. 2008.

[2] B. J. Baliga, "The IGBT Compendium: Applications and Social Impact," 2011.

[3] H. R. Huff, "John Bardeen and transistor physics," in *AIP Conference Proceedings*, 2001, vol. 550, no. March 2001, pp. 3–32, doi: 10.1063/1.1354371.

[4] R. Hall, "Power Rectifiers and Transistors," *Proc. IRE*, vol. 40, no. 11, pp. 1512–1518, Nov. 1952, doi: 10.1109/JRPROC.1952.273990.

[5] J. Moll, M. Tanenbaum, J. Goldey, and N. Holonyak, "P-N-P-N Transistor Switches," *Proc. IRE*, vol. 44, no. 9, pp. 1174–1182, Sep. 1956, doi: 10.1109/JRPROC.1956.275172.

[6] J. M. Goldey, I. M. Mackintosh, and I. M. Ross, "Turn-off gain in p-n-p-n triodes," *Solid. State. Electron.*, vol. 3, no. 2, pp. 119–122, Sep. 1961, doi: 10.1016/0038-1101(61)90066-1.

[7] L. Coulbeck, W. J. Findlay, and A. D. Millington, "Electrical trade-offs for GTO thyristors," *Power Eng. J.*, vol. 8, no. 1, pp. 18–26, Feb. 1994, doi: 10.1049/pe:19940102.

[8] P. D. Taylor, W. J. Findlay, and R. T. Denyer, "High-voltage high-current GTO thyristors," *IEE Proc. I Solid State Electron Devices*, vol. 132, no. 6, p. 238, 1985, doi: 10.1049/ip-i-1.1985.0053.

[9] K. C. Saraswat, J. D. Meindl, and J. Berger, "A high voltage MOS switch," *IEEE J. Solid-State Circuits*, vol. 10, no. 3, pp. 136–142, Jun. 1975, doi: 10.1109/JSSC.1975.1050578.

[10] J. D. Plummer, J. Berger, and J. D. Meindl, "High voltage monolithic MOS driver arrays," in *1971 International Electron Devices Meeting*, 1971, pp. 102–102, doi: 10.1109/IEDM.1971.188418.

[11] H. J. Sigg, G. D. Vendelin, T. P. Cauge, and J. Kocsis, "D-MOS transistor for microwave applications," *IEEE Trans. Electron Devices*, vol. 19, no. 1, pp. 45–53, Jan. 1972, doi: 10.1109/T-ED.1972.17370.

[12] H. G. Dill, "A new insulated gate tetrode with high drain breakdown potential and low miller feedback capacitance," *IEEE Trans. Electron Devices*, vol. 15, no. 10, pp. 717–728, Oct. 1968, doi: 10.1109/T-ED.1968.16504.

[13] V. A. K. Temple, R. P. Love, and P. V. Gray, "A 600-volt MOSFET designed for low on-resistance," *IEEE Trans. Electron Devices*, vol. 27, no. 2, pp. 343–349, Feb. 1980, doi: 10.1109/T-ED.1980.19866.

[14] Yole Development, "Status of the Power Electronics Industry 2019: Market and Technology Report 2019," 2019.

[15] M. Darwish and K. Board, "Lateral resurfed COMFET," *Electron. Lett.*, vol. 20, no. 12, pp. 519–520, 1984, doi: 10.1049/el:19840360.

[16] T. Fujihira and Y. Miyasaka, "Simulated superior performances of semiconductor superjunction devices," *Proc. 10th Int. Symp. Power Semicond. Devices ICs. ISPSD'98 (IEEE Cat. No.98CH36212)*, no. V, pp. 423–426, 1998, doi: 10.1109/ISPSD.1998.702736.

[17] F. Udrea, A. Popescu, and W. I. Milne, “3D RESURF double-gate MOSFET: A revolutionary power device concept,” *Electron. Lett.*, vol. 34, no. 8, p. 808, 1998, doi: 10.1049/el:19980504.

[18] G. Deboy, N. Marz, J.-P. Stengl, H. Strack, J. Tihanyi, and H. Weber, “A new generation of high voltage MOSFETs breaks the limit line of silicon,” in *International Electron Devices Meeting 1998. Technical Digest (Cat. No.98CH36217)*, 1998, pp. 683–685, doi: 10.1109/IEDM.1998.746448.

[19] T. P. Chow and R. Tyagi, “Wide bandgap compound semiconductors for superior high-voltage unipolar power devices,” *IEEE Trans. Electron Devices*, vol. 41, no. 8, pp. 1481–1483, 1994, doi: 10.1109/16.297751.

[20] M. Bhatnagar and B. J. Baliga, “Comparison of 6H-SiC, 3C-SiC, and Si for power devices,” *IEEE Trans. Electron Devices*, vol. 40, no. 3, pp. 645–655, Mar. 1993, doi: 10.1109/16.199372.

[21] N. Kaminski and O. Hilt, “SiC and GaN devices – wide bandgap is not all the same,” *IET Circuits, Devices Syst.*, vol. 8, no. 3, pp. 227–236, 2014, doi: 10.1049/iet-cds.2013.0223.

[22] J. W. Palmour, J. A. Edmond, H.-S. Kong, and C. H. Carter, Jr., “6H-Silicon Carbide Power Dvices for Aerospace Applications,” in *Proceedings of the Intersociety Energy Conversion Engineering Conference*, 1993, pp. 249–254.

[23] A. Marzoughi, A. Romero, R. Burgos, and D. Boroyevich, “Comparing the State-of-the-Art SiC MOSFETs,” *IEEE Power Electron. Mag.*, pp. 36–45, 2017, doi: 10.1109/MPEL.2017.2692309.

[24] X. She, A. Q. Huang, and B. Ozpineci, “Review of Silicon Carbide Power Devices and Their Applications,” *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, 2017, doi: 0.1109/TIE.2017.2652401.

[25] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, “A Survey of Wide Bandgap Power Semiconductor Devices,” *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014, doi: 10.1109/TPEL.2013.2268900.

[26] N. Oi, M. Inaba, S. Okubo, I. Tsuyuzaki, T. Kageura, S. Onoda, A. Hiraiwa, and H. Kawarada, “Vertical-type two-dimensional hole gas diamond metal oxide semiconductor field-effect transistors,” *Sci. Rep.*, vol. 8, no. 1, p. 10, Dec. 2018, doi: 10.1038/s41598-018-28837-5.

[27] F. Udrea, “Power Microelectronics Lecture Notes,” 2015.

[28] B. J. Baliga, “Enhancement and depletion-mode vertical-channel M.O.S. gated thyristors,” *Electron. Lett.*, vol. 15, no. 20, pp. 645–647, 1979, doi: 10.1049/el:19790459.

[29] J. D. Plummer and B. W. Scharf, “Insulated-Gate Planar Thyristors: I—Structure and Basic Operation,” *IEEE Trans. Electron Devices*, vol. 27, no. 2, pp. 380–387, Feb. 1980, doi: 10.1109/T-ED.1980.19871.

[30] L. Leipold, W. Baumgartner, W. Ladenhauf, and J. P. Stengl, “A FET-controlled thyristor in SIPMOS technology,” in *1980 International Electron Devices Meeting*, 1980, pp. 79–82, doi: 10.1109/IEDM.1980.189758.

[31] J. Tihanyi, “Functional integration of power MOS and bipolar devices,” in *1980 International Electron Devices Meeting*, 1980, pp. 75–78, doi:

10.1109/IEDM.1980.189757.

[32] H. W. Becke and C. F. J. Wheatly, “Power MOSFET with an anode region,” United States of America Patent, 4,364,073, Dec-1982.

[33] J. P. Russell, A. M. Goodman, L. A. Goodman, and J. M. Neilson, “The COMFET—A new high conductance MOS-gated device,” *IEEE Electron Device Lett.*, vol. 4, no. 3, pp. 63–65, Mar. 1983, doi: 10.1109/EDL.1983.25649.

[34] B. J. Baliga, M. S. Adler, R. P. Love, P. V. Gray, and N. D. Zommer, “The insulated gate transistor: A new three-terminal MOS-controlled bipolar power device,” *IEEE Trans. Electron Devices*, vol. 31, no. 6, pp. 821–828, Jun. 1984, doi: 10.1109/T-ED.1984.21614.

[35] K. Yamagami and Y. Akakiri, “Transistor,” Japan Patent, SHO 47-21739.

[36] M. Rahimo, “Future trends in high-power bipolar metal-oxide semi-conductor controlled power semi-conductors,” *IET Circuits, Devices Syst.*, vol. 8, no. 3, pp. 155–167, 2014, doi: 10.1049/iet-cds.2013.0220.

[37] D. Ueda, K. Kitamura, H. Takagi, and G. Kano, “A New Injection Suppression Structure for Conductivity Modulated Power MOSFETs,” in *Extended Abstracts of the 1986 International Conference on Solid State Devices and Materials*, 1986, pp. 97–100, doi: 10.7567/SSDM.1986.B-3-3.

[38] H. R. Chang and B. J. Baliga, “500-V n-channel insulated-gate bipolar transistor with a trench gate structure,” *IEEE Trans. Electron Devices*, vol. 36, no. 9, pp. 1824–1829, 1989, doi: 10.1109/16.34248.

[39] F. Udrea, G. A. J. Amaratunga, and Q. Huang, “The effect of the hole current on the channel inversion in trench insulated gate bipolar transistors (TIGBT),” *Solid State Electron.*, vol. 37, no. 3, pp. 507–514, 1994, doi: 10.1016/0038-1101(94)90018-3.

[40] F. Udrea and G. A. J. Amaratunga, “Theoretical and Numerical Comparison Between DMOS and Trench Technologies for Insulated Gate Bipolar Transistors,” *IEEE Trans. Electron Devices*, vol. 42, no. 7, pp. 1356–1366, 1995, doi: 10.1109/16.391221.

[41] R. Hotz, F. Bauer, and W. Fichtner, “On-state and short circuit behaviour of high voltage trench gate IGBTs in comparison with planar IGBTs,” *Proc. Int. Symp. Power Semicond. Devices IC’s ISPSD ’95*, pp. 224–229, 1995, doi: 10.1109/ISPSD.1995.515039.

[42] M. Harada, T. Minato, H. Takahashi, H. Nishihara, K. Inoue, and I. Takata, “600 V trench IGBT in comparison with planar IGBT-an evaluation of the limit of IGBT performance,” in *Proceedings of the 6th International Symposium on Power Semiconductor Devices and Ics*, 1994, pp. 411–416, doi: 10.1109/ISPSD.1994.583811.

[43] M. Kitagawa, I. Omura, S. Hasegawa, T. Inoue, and A. Nakagawa, “A 4500 V injection enhanced insulated gate bipolar transistor (IEGT) operating in a mode similar to a thyristor,” in *Proceedings of IEEE International Electron Devices Meeting*, 1993, pp. 679–682, doi: 10.1109/IEDM.1993.347221.

[44] F. Udrea, S. S. M. Chan, J. Thomson, T. Trajkovic, P. R. Waind, G. A. J. Amaratunga, and D. E. Crees, “1.2 kV trench insulated gate bipolar transistors (IGBT’s) with ultralow on-resistance,” *IEEE Electron Device Lett.*, vol. 20, no. 8,

pp. 428–430, Aug. 1999, doi: 10.1109/55.778166.

[45] T. Laska, F. Pfirsch, F. Hirler, J. Niedermeyr, C. Schaffer, and T. Schmidt, “1200 V-trench-IGBT study with square short circuit SOA,” in *Proceedings of the 10th International Symposium on Power Semiconductor Devices and ICs. ISPSD’98 (IEEE Cat. No.98CH36212)*, 1998, pp. 433–436, doi: 10.1109/ISPSD.1998.702738.

[46] M. Otsuki, S. Momota, A. Nishiura, and K. Sakurai, “The 3rd generation IGBT toward a limitation of IGBT performance,” in *[1993] Proceedings of the 5th International Symposium on Power Semiconductor Devices and ICs*, 1993, vol. 81, no. 263, pp. 24–29, doi: 10.1109/ISPSD.1993.297101.

[47] T. Syau and B. J. Baliga, “Mobility study on RIE etched silicon surfaces using SF6/O2 gas etchants,” *IEEE Trans. Electron Devices*, vol. 40, no. 11, pp. 1997–2005, 1993, doi: 10.1109/16.239740.

[48] K. Shenai, “Optimized trench MOSFET technologies for power devices,” *IEEE Trans. Electron Devices*, vol. 39, no. 6, pp. 1435–1443, Jun. 1992, doi: 10.1109/16.137324.

[49] K. Shenai, “Nearly bird’s beak-free local oxidation technology for controlled dielectric formation in deep silicon trenches,” *Electron. Lett.*, vol. 27, no. 8, p. 637, 1991, doi: 10.1049/el:19910400.

[50] N. Thapar and B. Jayant Baliga, “Elimination of the ‘Birds Beak’ in trench MOS-gate power semiconductor devices,” in *8th International Symposium on Power Semiconductor Devices and ICs. ISPSD ’96. Proceedings*, pp. 83–86, doi: 10.1109/ISPSD.1996.509454.

[51] F. Udrea and G. A. J. Amaratunga, “A unified analytical model for the carrier dynamics in trench insulated gate bipolar transistors (TIGBT),” in *Proceedings of International Symposium on Power Semiconductor Devices and IC’s: ISPSD ’95*, 1995, pp. 190–195, doi: 10.1109/ISPSD.1995.515033.

[52] H. Yilmaz, “Cell Geometry Effect on IGT Latch-UP,” *IEEE Electron Device Lett.*, vol. 6, no. 8, pp. 419–421, Aug. 1985, doi: 10.1109/EDL.1985.26176.

[53] B. J. Baliga, H. R. Chang, T. P. Chow, and S. Al-Marayati, “New cell designs for improved IGBT safe-operating-area,” in *Technical Digest - International Electron Devices Meeting*, 1988, pp. 809–812, doi: 10.1109/IEDM.1988.32934.

[54] V. Parthasarathy, K. C. So, Z. Shen, and T. P. Chow, “Cell optimization for 500V N-channel IGBTS,” *IEEE Int. Symp. Power Semicond. Devices ICs*, no. 94, pp. 69–74, 1994, doi: 10.1109/ISPSD.1994.583652.

[55] H.-S. Kim, T.-S. Lee, C.-M. Yun, K.-H. Oh, P.-G. Im, and D.-J. Kim, “Hole bypassing N+ emitter structure of the trench IGBT for the safe switching operation,” *Proc. 9th Int. Symp. Power Semicond. Devices IC’s*, no. C, 1997, doi: 10.1109/ISPSD.1997.601490.

[56] A. Wintrich, U. Nicolai, W. Tursky, and T. Reimann, *Application Manual Power Semiconductors*, 2nd revise. Semikron International GmbH, 2015.

[57] S. Dewar, S. Linder, C. Von Arx, A. Mukhitinov, and G. Debled, “Soft Punch Through (SPT) – Setting new Standards in 1200V IGBT,” in *PCIM Europe*, 2000.

[58] T. Laska, M. Munzer, F. Pfirsch, C. Schaeffer, and T. Schmidt, “The Field Stop

IGBT (FS IGBT). A new power device concept with a great improvement potential," in *12th International Symposium on Power Semiconductor Devices & ICs. Proceedings (Cat. No.00CH37094)*, 2000, pp. 355–358, doi: 10.1109/ISPSD.2000.856842.

[59] H. Nakamura, K. Nakamura, S. Kusunoki, H. Takahashi, Y. Tomomatsu, and M. Harada, "Wide cell pitch 1200V NPT CSTBTs with short circuit ruggedness," in *13th International Symposium on Power Semiconductor Devices & ICs (ISPSD)*, 2001, pp. 299–302, doi: 10.1109/ISPSD.2001.934614.

[60] L. Lorenz, G. Deboy, A. Knapp, and M. Marz, "COOLMOS a new milestone in high voltage power MOS," *11th Int. Symp. Power Semicond. Devices ICs. ISPSD'99 Proc.*, pp. 3–10, 1999, doi: 10.1109/ISPSD.1999.764028.

[61] F. Bauer, "The MOS controlled super junction transistor (SJBT): a new, highly efficient, high power semiconductor device for medium to high voltage applications," in *Proceedings of the 14th International Symposium on Power Semiconductor Devices and Ics*, 2002, pp. 197–200, doi: 10.1109/ISPSD.2002.1016205.

[62] F. D. Bauer, "The super junction bipolar transistor: A new silicon power device concept for ultra low loss switching applications at medium to high voltages," *Solid. State. Electron.*, vol. 48, no. 5, pp. 705–714, 2004, doi: 10.1016/j.sse.2003.09.017.

[63] F. Udrea, "Semiconductor Device," United States of America Patent, 6,111,289, 2000.

[64] M. Antoniou, F. Udrea, and F. Bauer, "Optimisation of SuperJunction Bipolar Transistor for ultra-fast switching applications," in *Proceedings of the 19th International Symposium on Power Semiconductor Devices and IC's*, 2007, pp. 101–104, doi: 10.1109/ISPSD.2007.4294942.

[65] Kwang-Hoon Oh, Jaegil Lee, Kyu-Hyun Lee, Young Chul Kim, and Chongman Yun, "A simulation study on novel field stop IGBTs using superjunction," *IEEE Trans. Electron Devices*, vol. 53, no. 4, pp. 884–890, Apr. 2006, doi: 10.1109/TED.2006.870278.

[66] M. Antoniou, F. Udrea, F. Bauer, and I. Nistor, "The Soft Punchthrough+ Superjunction Insulated Gate Bipolar Transistor: A High Speed Structure With Enhanced Electron Injection," *IEEE Trans. Electron Devices*, vol. 58, no. 3, pp. 769–775, 2011, doi: 10.1109/TED.2010.2101076.

[67] F. Udrea, A. Popescu, R. Ng, and G. A. J. Amaratunga, "Minority carrier injection across the 3D RESURF junction," in *12th International Symposium on Power Semiconductor Devices & ICs. Proceedings (Cat. No.00CH37094)*, 2000, pp. 201–204, doi: 10.1109/ISPSD.2000.856806.

[68] H. Bartolf, A. Mihaila, I. Nistor, M. Jurisch, B. Leibold, and M. Zimmermann, "Development of a 60µm Deep Trench and Refill Process for Manufacturing Si-Based High-Voltage Super-Junction Structures," *IEEE Trans. Semicond. Manuf.*, vol. 26, no. 4, pp. 529–541, Nov. 2013, doi: 10.1109/TSM.2013.2272042.

[69] K. H. Oh, J. Kim, H. Seo, J. Jung, E. Kim, S. S. Kim, and C. Yun, "Experimental investigation of 650V superjunction IGBTs," in *28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2016, pp. 299–302, doi:

10.1109/ISPSD.2016.7520837.

[70] M. Antoniou, N. Lophitis, F. Udrea, F. Bauer, U. R. Vemulapati, and U. Badstuebner, “On the Investigation of the ‘Anode Side’ SuperJunction IGBT Design Concept,” *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1063–1066, 2017, doi: 10.1109/LED.2017.2718619.

[71] L. Zhu and X. Chen, “An investigation of a novel snapback-free reverse-conducting IGBT and with dual gates,” *IEEE Trans. Electron Devices*, vol. 59, no. 11, pp. 3048–3053, 2012, doi: 10.1109/TED.2012.2215039.

[72] Toshiba Electronic Devices and Storage Corporation (EMEA), “IEGT - Product Description,” 2019. [Online]. Available: https://toshiba.semicon-storage.com/eu/product/igbt-iegt/iegt.html. [Accessed: 20-Sep-2009].

[73] M. Kitagawa, A. Nakagawa, K. Matsushita, S. Hasegawa, T. Inoue, A. Yahata, and H. Takenaka, “4500 V IEGTs having switching characteristics superior to GTO,” in *Proceedings of International Symposium on Power Semiconductor Devices and IC’s: ISPSD ’95*, 1995, pp. 486–491, doi: 10.1109/ISPSD.1995.515086.

[74] H. Takahashi, H. Haruguchi, H. Hagino, and T. Yamada, “Carrier stored trench-gate bipolar transistor (CSTBT)-a novel power device for high voltage application,” in *8th International Symposium on Power Semiconductor Devices and ICs. ISPSD ’96. Proceedings*, 1996, pp. 349–352, doi: 10.1109/ISPSD.1996.509513.

[75] Mitisubishi Electric, “IGBT Modules,” 2019. [Online]. Available: http://www.mitsubishielectric.com/semiconductors/products/powermod/igbtmod/index.html. [Accessed: 20-Sep-2009].

[76] P. Gough, “MOS-gated thyristor,” United States of America Patent, 5,202,750, 1993.

[77] M. Mori, Y. Uchino, J. Sakano, and H. Kobayashi, “A novel high-conductivity IGBT (HiGT) with a short circuit capability,” in *10th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 1998, pp. 429–432, doi: 10.1109/ISPSD.1998.702737.

[78] K. Oyama, Y. Kohno, J. Sakano, J. Uruno, K. Ishizaka, D. Kawase, and M. Mori, “Novel 600-V trench high-conductivity IGBT (Trench HiGT) with short-circuit capability,” in *Proceedings of the 13th International Symposium on Power Semiconductor Devices & ICs. IPSD ’01 (IEEE Cat. No.01CH37216)*, 2001, pp. 417–420, doi: 10.1109/ISPSD.2001.934642.

[79] Hitachi, “IGBT - Product Description,” 2019. [Online]. Available: http://pdd.hitachi.eu/igbts.

[80] T. P. Chow, B. J. Baliga, H. R. Chang, P. V. Gray, W. Hennessy, and C. E. Logan, “P-channel, vertical insulated gate bipolar transistors with collector short,” in *1987 International Electron Devices Meeting (IEDM)*, 1987, pp. 670–673, doi: 10.1109/IEDM.1987.191517.

[81] S. Voss, F. J. Niedernostheide, and H. J. Schulze, “Anode design variation in 1200-V trench field-stop reverse-conducting IGBTs,” in *20th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2008, pp. 169–172, doi: 10.1109/ISPSD.2008.4538925.

[82] E. M. Findlay and F. Udrea, “Reverse-Conducting Insulated Gate Bipolar

Transistor: A Review of Current Technologies," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 219–231, Jan. 2019, doi: 10.1109/TED.2018.2882687.

[83] Infineon Technologies, "Reverse Conducting IGBT for Induction Cooking and Resonant Applications," 2014.

[84] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Convertors, Applications and Design*, Third Edit. USA: John Wiley & Sons, Inc., 2003.

[85] K. S. Oh, "Application Note 9016 IGBT Basics 1," 2001.

[86] D. O. Neacsu and T. Takahashi, "Computer-Aided Design of a Low-Cost Low-Power Snubberless Three-Phase Inverter," *Comput. Power Electron. 2000. COMPEL 2000. 7th Work.*, pp. 204–210, 2000, doi: 10.1109/CIPE.2000.904717.

[87] IEC 60747-9:2007, "Semiconductor devices – Discrete devices – Part 9: Insulated-gate bipolar transistors (IGBTs)," no. 2.0.

[88] B. J. Baliga, *The IGBT device : Physics, design and applications of the insulated gate bipolar transistor*. Elsevier, 2015.

[89] S. M. Sze and K. K. Ng, *Semiconductor Devices: Physics and Technology*. 2006.

[90] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. De Donker, *Semiconductor Power Devices*. Springer, 2011.

[91] H. Luo, Y. Chen, P. Sun, W. Li, and X. He, "Junction Temperature Extraction Approach With Turn-Off Delay Time for High-Voltage High-Power IGBT Modules," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 5122–5132, 2016, doi: 10.1109/TPEL.2015.2481465.

[92] Synopsys, *Sentaurus Device User Guide*, L-2016.03., no. March. 2016.

[93] W. Bludau, A. Onton, and W. Heinke, "Temperature dependence of the band gap of silicon," *J. Appl. Phys.*, vol. 45, no. 4, pp. 1846–1848, Apr. 1974, doi: 10.1063/1.1663501.

[94] D. B. M. Klaassen, J. W. Slotboom, and H. C. de Graaff, "Unified apparent bandgap narrowing in n- and p-type silicon," *Solid. State. Electron.*, vol. 35, no. 2, pp. 125–129, Feb. 1992, doi: 10.1016/0038-1101(92)90051-D.

[95] J. W. Slotboom, "The pn-product in silicon," *Solid. State. Electron.*, vol. 20, no. 4, pp. 279–283, Apr. 1977, doi: 10.1016/0038-1101(77)90108-3.

[96] J. W. Slotboom and H. C. de Graaff, "Bandgap narrowing in silicon bipolar transistors," *IEEE Trans. Electron Devices*, vol. 24, no. 8, pp. 1123–1125, Aug. 1977, doi: 10.1109/T-ED.1977.18889.

[97] J. W. Slotboom and H. C. de Graaff, "Measurements of bandgap narrowing in Si bipolar transistors," *Solid. State. Electron.*, vol. 19, no. 10, pp. 857–862, Oct. 1976, doi: 10.1016/0038-1101(76)90043-5.

[98] G. Camuso, E. Napoli, V. Pathirana, N. Udugampola, A. P. S. Hsieh, T. Trajkovic, and F. Udrea, "Effect of bandgap narrowing on performance of modern power devices," *IEEE Trans. Electron Devices*, vol. 60, no. 12, pp. 4185–4190, 2013, doi: 10.1109/TED.2013.2286528.

[99] R. Häcker and A. Hangleiter, "Intrinsic upper limits of the carrier lifetime in silicon," *J. Appl. Phys.*, vol. 75, no. 11, pp. 7570–7572, Jun. 1994, doi: 10.1063/1.356634.

[100] R. Van Overstraeten and H. De Man, “Measurement of the ionization rates in diffused silicon p-n junctions,” *Solid State Electron.*, vol. 13, no. 5, pp. 583–608, 1970, doi: 10.1016/0038-1101(70)90139-5.

[101] The Editors of the Encyclopedia of Britannica, “Trap,” *Encyclopædia Britannica, inc.*, 2016. [Online]. Available: https://www.britannica.com/science/trap-solid-state-physics. [Accessed: 03-Oct-2019].

[102] H. C. Card, “Aluminum-Silicon Schottky Barriers and Ohmic Contacts in Integrated Circuits,” *IEEE Trans. Electron Devices*, vol. 23, no. 6, pp. 538–544, 1976, doi: 10.1109/T-ED.1976.18449.

[103] CRRC, “TG450HF17M1-S300 Half Bridge IGBT Product Datasheet.”

[104] H.-D. Lee and Y.-J. Lee, “Arsenic and phosphorus double ion implanted source/drain junction for 0.25- and sub-0.25-μm MOSFET technology,” *IEEE Electron Device Lett.*, vol. 20, no. 1, pp. 42–44, 1999, doi: 10.1109/55.737568.

[105] J. Yamashita, A. Uenishi, Y. Tomomatsu, H. Haruguchi, H. Takahashi, I. Takata, and H. Hagino, “A study on the short circuit destruction of IGBTs,” *Power Semicond. Devices ICs, 1993. ISPSD ’93., Proc. 5th Int. Symp.*, pp. 35–40, 1993, doi: 10.1109/ISPSD.1993.297103.

[106] M. Watanabe et al., “Impact of three-dimensional current flow on accurate TCAD simulation for trench-gate IGBTs,” in *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2019, vol. 2019-May, pp. 311–314, doi: 10.1109/ISPSD.2019.8757640.

[107] E. M. Findlay and F. Udrea, “Modeling of Large Area Trench IGBTs: The Effect of Birds-Beak,” *IEEE Trans. Electron Devices*, vol. 66, no. 6, pp. 2686–2691, Jun. 2019, doi: 10.1109/TED.2019.2911020.

[108] M. Antoniou, F. Udrea, F. Bauer, and I. Nistor, “A new way to alleviate the RC IGBT snapback phenomenon: The Super Junction Solution,” in *22nd International Symposium on Power Semiconductor Devices & ICs (ISPSD)*, 2010, pp. 153–156.

[109] L. Storasta, A. Kopta, M. Rahimo, C. Papadopoulos, S. Geissmann, and R. Schnell, “The next generation 6500V BIGT HiPak modules,” in *PCIM Europe*, 2013, pp. 337–344.

[110] J. Won, J. G. Koo, T. Rhee, H.-S. Oh, and J. H. Lee, “Reverse-conducting IGBT using MEMS technology on the wafer back side,” *Electron. Telecommun. Res. Inst. J.*, vol. 35, no. 4, pp. 603–609, 2013, doi: 10.4218/etrij.13.1912.0030.

[111] M. Rahimo and L. Storasta, “Optimization and advantages of the Bi-mode insulated gate transistor,” *Facta Univ. - Ser. Electron. Energ.*, vol. 28, no. 3, pp. 383–391, 2015, doi: 10.2298/FUEE1503383R.

[112] A. P. S. Hsieh, G. Camuso, F. Udrea, Y. Tang, C. Ng, N. Ranjan, and A. Charles, “Field-stop layer optimization for 1200V FS IGBT operating at 200°C,” *Proc. Int. Symp. Power Semicond. Devices ICs*, pp. 115–118, 2014, doi: 10.1109/ISPSD.2014.6855989.

[113] W. C. Hsu, F. Udrea, H. Hsu, and W. Lin, “Reverse-conducting Insulated Gate Bipolar Transistor with an Anti-parallel Thyristor,” in *22nd International Symposium on Power Semiconductor Devices & ICs (ISPSD)*, 2010, pp. 149–152.

[114] U. Vemulapati, N. Kaminski, D. Silber, L. Storasta, and M. Rahimo, “Reverse

conducting-IGBTs initial snapback phenomenon and its analytical modelling," *IET Circuits, Devices Syst.*, vol. 8, no. 3, pp. 168–175, 2014, doi: 10.1049/iet-cds.2013.0222.

[115] M. Rahimo, A. Kopta, U. Schlapbach, J. Vobecky, R. Schnell, and S. Klaka, "The Bi-mode Insulated Gate Transistor (BIGT) a potential technology for higher power applications," in *21st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2009, pp. 283–286, doi: 10.1109/ISPSD.2009.5158057.

[116] M. Rahimo, U. Schlapbach, A. Kopta, J. Vobecky, D. Schneider, and A. Baschnagel, "A high current 3300V module employing reverse conducting IGBTs setting a new benchmark in output power capability," *20th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*. Orlando, FL, pp. 68–71, 2008, doi: 10.1109/ISPSD.2008.4538899.

[117] W. Chen, Z. Li, M. Ren, J. Zhang, B. Zhang, Y. Liu, Q. Hua, K. Mao, and Z. Li, "A high reliable reverse-conducting IGBT with a floating P-plug," in *25th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2013, pp. 265–268, doi: 10.1109/ISPSD.2013.6694437.

[118] H. Jiang, J. Wei, B. Zhang, W. Chen, M. Qiao, and Z. Li, "Band-to-band tunneling injection insulated-gate bipolar transistor with a soft reverse-recovery built-in diode," *IEEE Electron Device Lett.*, vol. 33, no. 12, pp. 1684–1686, 2012, doi: 10.1109/LED.2012.2219612.

[119] D. Werber, T. Hunger, M. Wissen, T. Schütze, M. Lassmann, B. Stemmer, V. Komarnitskyy, and F. Pfirsch, "A 1000A 6.5kV Power Module Enabled by Reverse Conducting Trench-IGBT-Technology," in *PCIM Asia*, 2016, pp. 269–276.

[120] D. Domes, "Control Method for a Reverse Conducting IGBT," in *PCIM Europe*, 2015, no. May, pp. 147–154.

[121] H. Jiang, B. Zhang, W. Chen, C. Liu, Z. Rao, and B. Dong, "A snapback suppressed reverse conducting IGBT with oxide with a floating p-region in trench collector," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 417–419, 2012, doi: 10.1109/APPEEC.2012.6307221.

[122] W. Zhang, Y. Zhu, S. Lu, X. Tian, and Y. Teng, "Increase of the reliability of the junction terminations of reverse-conducting insulated gate bipolar transistor by appropriate backside layout design," *IEEE Electron Device Lett.*, vol. 35, no. 12, pp. 1281–1283, 2014, doi: 10.1109/LED.2014.2364301.

[123] T. Yoshida, T. Takahashi, K. Suzuki, and M. Tarutani, "The second-generation 600V RC-IGBT with optimized FWD," in *28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2016, pp. 159–162, doi: 10.1109/ISPSD.2016.7520802.

[124] D. Kumar, M. Sweet, K. Vershinin, L. Ngwendson, and E. M. . Narayanan, "RC-TCIGBT: A Reverse Conducting Trench Clustered IGBT," in *19th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2007, pp. 161–164, doi: 10.1109/ISPSD.2007.4294957.

[125] A. Lale, A. Bourennane, and F. Richardeau, "RC-IGBT-thyristor structure having trenches filled with dielectric on the backside: Physical analysis and application to the integration of a multiphase generic power converter using the 'two-chip'

approach," in *17th European Conference on Power Electronics and Applications (EPE'15 ECCE Europe)*, 2015, doi: 10.1109/EPE.2015.7311704.

[126] L. Zhu and X. Chen, "A novel snapback-free reverse conducting IGBT with anti-parallel Shockley diode," in *25th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2013, pp. 261–264, doi: 10.1109/ISPSD.2013.6694436.

[127] Z. Lin, X. Chen, and B. Yi, "Snapback-free reverse-conducting IGBT with low turnoff loss," *Electron. Lett.*, vol. 50, no. 9, pp. 703–705, 2014, doi: 10.1049/el.2014.0169.

[128] M. Rahimo, U. Schlapbach, A. Kopta, R. Schnell, and S. Linder, "SPT+, the Next Generation of Low-Loss HV-IGBTs," in *PCIM Europe*, 2005, pp. 1–6.

[129] B. Jiang, F. X. C. Jiang, Z. Li, and X. Lin, "A reverse conducting IGBT with low on-state voltage and turnoff loss," in *11th International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, 2012, doi: 10.1109/ICSICT.2012.6467701.

[130] G. Deng, X. Luo, K. Zhou, Q. He, X. Ruan, Q. Liu, T. Sun, and B. Zhang, "A snapback-free RC-IGBT with Alternating N/P buffers," in *2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD)*, 2017, pp. 127–130, doi: 10.23919/ISPSD.2017.7988943.

[131] A. Nakagawa, "Numerical experiment for 2500 V double gate bipolar-mode MOSFETs (DGIGBT) and analysis for large safe operating area (SOA)," in *PESC '88 Record., 19th Annual IEEE Power Electronics Specialists Conference*, 1988, pp. 84–90, doi: 10.1109/PESC.1988.18119.

[132] J. W. Wu, S. Chowdhury, C. Hitchcock, J. J.-Q. Lu, T. P. Chow, W. Kim, and K. Ngo, "1200V, 25A bi-directional Si DMOS IGBT fabricated with fusion wafer bonding," in *2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, 2014, pp. 95–98, doi: 10.1109/ISPSD.2014.6855984.

[133] Daming Wang, Sai Tang, Shanglin Mo, Mengxuan Jiang, Xin Yin, Jun Wang, Zhikang Shuai, Z. J. Shen, and T. P. Chow, "Applicability of single-chip dual-gate bidirectional IGBTs in matrix converters," in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, 2016, pp. 292–296, doi: 10.1109/IPEMC.2016.7512301.

[134] A. Kopta, M. Rahimo, C. Corvasce, M. Andenna, F. Dugal, F. Fischer, S. Hartmann, and A. Baschnagel, "Next Generation IGBT and Package Technologies for High Voltage Applications," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 753–759, Mar. 2017, doi: 10.1109/TED.2017.2655485.

[135] L. Storasta, M. Rahimo, M. Bellini, A. Kopta, U. R. Vemulapati, and N. Kaminski, "The radial layout design concept for the Bi-mode insulated gate transistor," in *23rd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2011, pp. 56–59, doi: 10.1109/ISPSD.2011.5890789.

[136] M. Rahimo, C. Papadopoulos, C. Corvasce, and A. Kopta, "An advanced bimode insulated gate transistor BIGT with low diode conduction losses under a positive gate bias," in *2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD)*, 2017, pp. 483–486, doi: 10.23919/ISPSD.2017.7988884.

[137] M. Rahimo, M. Andenna, L. Storasta, C. Corvasce, and A. Kopta, “Demonstration of an Enhanced Trench Bimode Insulated Gate Transistor ET-BIGT,” in *28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2016, pp. 151–154, doi: 10.1109/ISPSD.2016.7520800.

[138] M. Antoniou, F. Udrea, and F. Bauer, “The superjunction insulated gate bipolar transistor optimization and modeling,” *IEEE Trans. Electron Devices*, vol. 57, no. 3, pp. 594–600, 2010, doi: 10.1109/TED.2009.2039260.

[139] J. Yu, F. Jiang, H. Wei, and X. Lin, “A superjunction snapback-free reverse-conducting Insultated Gate Bipolar Transistor with anti-parallel P-I-N diode,” *12th IEEE Int. Conf. Solid-State Integr. Circuit Technol.*, no. c, pp. 3–5, 2014, doi: 10.1109/ICSICT.2014.7021538.

[140] X. Xu and Z. Chen, “Simulation Study of a Novel Full Turn-On RC-IGBT With Ultralow Energy Loss,” *IEEE Electron Device Lett.*, vol. 40, no. 5, pp. 757–760, 2019, doi: 10.1109/LED.2019.2905145.

[141] R. Gejo, T. Ogura, S. Misu, Y. Maeda, Y. Matsuoka, N. Yasuhara, and K. Nakamura, “High switching speed trench diode for 1200V RC-IGBT based on the concept of Schottky Controlled injection (SC),” in *28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2016, pp. 155–158, doi: 10.1109/ISPSD.2016.7520801.

[142] A. Bourennane, H. Tahir, J. L. Sanchez, L. Pont, G. Sarrabayrouse, and E. Imbernon, “High temperature wafer bonding technique for the realization of a voltage and current bidirectional IGBT,” *Proc. Int. Symp. Power Semicond. Devices ICs*, pp. 140–143, 2011, doi: 10.1109/ISPSD.2011.5890810.

[143] S. L. Tu, G. Tam, P. Tam, H.-Y. Tsoi, and A. Taomoto, “Analysis of direct wafer bond IGBTs with heavily doped N+ buffer layer,” in *8th International Symposium on Power Semiconductor Devices and ICs. ISPSD ’96. Proceedings*, 1996, pp. 339–342, doi: 10.1109/ISPSD.1996.509511.

[144] A. Nakagawa, K. Watanabe, Y. Yamaguchi, H. Ohashi, and K. Furukawa, “1800V bipolar-mode MOSFETs: A first application of silicon wafer direct bonding (SDB) technique to a power device,” in *1986 International Electron Devices Meeting*, 1986, pp. 122–125, doi: 10.1109/IEDM.1986.191128.

[145] P. M. Shenoy, A. Bhalla, and G. M. Dolny, “Analysis of the effect of charge imbalance on the static and dynamic characteristics of the super junction MOSFET,” *Proc. 11th Int. Symp. Power Semicond. Devices ICs (ISPSD), Toronto, Ontario*, pp. 99–102, 1999, doi: 10.1109/ISPSD.1999.764069.

[146] CREE Inc., “Design Considerations for Designing with Cree SiC Modules Part 2. Techniques for Minimizing Parasitic Inductance,” 2013.

[147] K. Vogel and D. Domes, “IGBT inverter with increased power density by use of a high-temperature- capable and low-inductance design,” *PCIM Eur. Conf. Proc.*, pp. 238–243, 2012.

[148] S. Havanur and P. Zuk, “Power MOSFET Basics: Understanding Superjunction Technology,” pp. 1–5, 2015.

[149] X. Tang, Y. Pan, P. Zhang, J. Li, R. Jin, Z. Zhao, and X. Cui, “PETT oscillation characteristics in press pack IGBTs,” *2017 IEEE 6th Asia-Pacific Conf. Antennas Propagation, APCAP 2017 - Proceeding*, vol. 1, pp. 1–3, 2018, doi:

10.1109/APCAP.2017.8420702.

[150] J. J. Graczkowski, K. L. Neff, and X. Kou, “A Low-Cost Gate Driver Design Using Bootstrap Capacitors for Multilevel MOSFET Inverters,” in *2006 CES/IEEE 5th International Power Electronics and Motion Control Conference*, 2006, pp. 1–5, doi: 10.1109/IPEMC.2006.4778160.

[151] Jih-Sheng Lai and Fang Zheng Peng, “Multilevel converters - a new breed of power converters,” *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, 1996, doi: 10.1109/28.502161.

[152] A. Sanchez-Ruiz, M. Mazuela, S. Alvarez, G. Abad, and I. Baraia, “Medium voltage-high power converter topologies comparison procedure, for a 6.6 kV drive application using 4.5 kV IGBT modules,” *IEEE Trans. Ind. Electron.*, vol. 59, no. 3, pp. 1462–1476, 2012, doi: 10.1109/TIE.2011.2162213.

[153] G. Gateau, T. A. Meynard, and H. Foch, “Stacked multicell converter (SMC): properties and design,” pp. 1583–1588, 2002, doi: 10.1109/pesc.2001.954345.

[154] L. G. Franquelo, J. Pou, K. Gopakumar, Bin Wu, J. Rodriguez, J. I. Leon, M. Malinowski, M. A. Pérez, and S. Kouro, “Recent Advances and Industrial Applications of Multilevel Converters,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, 2010, doi: 10.1109/tie.2010.2049719.

[155] A. Beddard and M. Barnes, “Modelling of MMC-HVDC Systems – An Overview,” *Energy Procedia*, vol. 80, pp. 201–212, 2015, doi: 10.1016/j.egypro.2015.11.423.

[156] P. Palmer, X. Zhang, J. Zhang, E. Findlay, T. Zhang, and E. Shelton, “Coordinated Switching with SiC MOSFET for Increasing Turn-off dV/dt of Si IGBT,” in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 3517–3521, doi: 10.1109/ECCE.2018.8557666.

[157] N. Oswald, P. Anthony, N. McNeill, and B. H. Stark, “An experimental investigation of the tradeoff between switching losses and EMI generation with hard-switched All-Si, Si-SiC, and All-SiC device combinations,” *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2393–2407, 2014, doi: 10.1109/TPEL.2013.2278919.

[158] J. W. Palmour, L. Cheng, V. Pala, E. V. Brunt, D. J. Lichtenwalner, G. Y. Wang, J. Richmond, M. O’Loughlin, S. Ryu, S. T. Allen, A. A. Burk, and C. Scozzie, “Silicon carbide power MOSFETs: Breakthrough performance from 900 v up to 15 kV,” *Proc. Int. Symp. Power Semicond. Devices ICs*, pp. 79–82, 2014, doi: 10.1109/ISPSD.2014.6855980.

[159] J. W. Palmour, “Silicon carbide power device development for industrial markets,” *Tech. Dig. - Int. Electron Devices Meet. IEDM*, vol. 2015-Febru, no. February, pp. 1.1.1-1.1.8, 2015, doi: 10.1109/IEDM.2014.7046960.

[160] P. Losee et al., “1.2kV class SiC MOSFETs with improved performance over wide operating temperature,” *Proc. Int. Symp. Power Semicond. Devices ICs*, pp. 297–300, 2014, doi: 10.1109/ISPSD.2014.6856035.

[161] C. M. DiMarino, R. Burgos, and B. Dushan, “High-temperature silicon carbide: Characterization of state-of-the-art silicon carbide power transistors,” *IEEE Ind. Electron. Mag.*, vol. 9, no. 3, pp. 19–30, 2015, doi: 10.1109/MIE.2014.2360350.

[162] Y. Jiang, G. Hua, E. Yang, and F. C. Lee, “Soft-switching of IGBTs with the help

of MOSFETs in bridge-type converters," in *Proceedings of IEEE Power Electronics Specialist Conference - PESC '93*, 1993, pp. 151–157, doi: 10.1109/PESC.1993.471918.

[163] J. W. Kimball and P. L. Chapman, "Evaluating conduction loss of a parallel IGBT-MOSFET combination," in *Conference Record of the 2004 IEEE Industry Applications Conference, 2004. 39th IAS Annual Meeting.*, 2004, vol. 2, pp. 1233–1237, doi: 10.1109/IAS.2004.1348570.

[164] K. F. Hoffmann and J. P. Karst, "High frequency power switch - improved performance by MOSFETs and IGBTs connected in parallel," in *2005 European Conference on Power Electronics and Applications*, 2005, pp. 11 pp.-P.11, doi: 10.1109/EPE.2005.219594.

[165] M. Frisch and E. Temesi, "Power module design for an ultra efficient three-level utility grid solar inverter," in *PCIM Conference Proceedings*, 2013, pp. 462–469.

[166] U. R. Vemulapati, A. Mihaila, R. A. Minamisawa, F. Canales, M. Rahimo, and C. Papadopoulos, "Simulation and experimental results of 3.3kV cross switch Si-IGBT and SiC-MOSFET hybrid," *Proc. Int. Symp. Power Semicond. Devices ICs*, vol. 2016-July, pp. 163–166, 2016, doi: 10.1109/ISPSD.2016.7520803.

[167] M. Rahimo, F. Canales, R. A. Minamisawa, C. Papadopoulos, U. Vemulapati, A. Mihaila, S. Kicin, and U. Drofenik, "Characterization of a Silicon IGBT and Silicon Carbide MOSFET Cross-switch hybrid," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4638–4642, 2015, doi: 10.1109/TPEL.2015.2402595.

[168] A. T. Bryant, P. R. Palmer, E. Santi, and J. L. Hudgins, "Simulation and optimization of diode and insulated gate bipolar transistor interaction in a chopper cell using MATLAB and Simulink," *IEEE Trans. Ind. Appl.*, vol. 43, no. 4, pp. 874–883, 2007, doi: 10.1109/TIA.2007.900443.

[169] G. J. Roberts, A. T. Bryant, P. A. Mawby, T. Ueta, T. Nisijima, and K. Hamada, "Evaluation of silicon carbide devices for hybrid vehicle drives," *2007 Eur. Conf. Power Electron. Appl. EPE*, 2007, doi: 10.1109/EPE.2007.4417371.

[170] A. R. Hefner and D. L. Blackburn, "A Performance Trade-Off for the Insulated Gate Bipolar Transistor: Buffer Layer Versus Base Lifetime Reduction," *IEEE Trans. Power Electron.*, vol. PE-2, no. 3, pp. 194–207, Jul. 1987, doi: 10.1109/TPEL.1987.4766360.