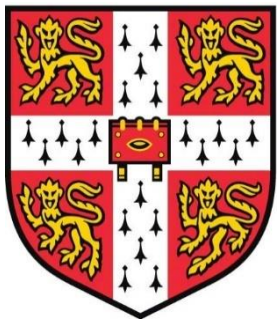
Electrical contacts on two-dimensional transition metal dichalcogenide semiconductors



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This thesis is submitted for the degree of *Doctor of Philosophy*.

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Declaration

I hereby declare that this thesis, submitted for the degree of Doctor of Philosophy at the University of Cambridge, is a result of my own work as PhD candidate in the Department of Materials Science & Metallurgy, University of Cambridge, under the supervision of Professor Manish Chhowalla. This thesis includes nothing which is the outcome of work done in collaboration except as declared in the Preface and specified in the text.

It is not substantially the same as any that I have submitted, or, is being concurrently submitted for a degree or diploma or other qualification at the University of Cambridge or any other University or similar institution except as declared in the Preface and specified in the text. I further state that no substantial part of my dissertation has already been submitted, or, is being concurrently submitted for any such degree, diploma or other qualification at the University of Cambridge or any other University or similar institution except as declared in the Preface and specified in the text.

It does not exceed the prescribed word limit for the relevant Degree Committee (no more than 65,000 words).

Yan Wang

July 2021

Abstract

Two dimensional (2D) transitional metal dichalcogenides (TMDs) such as molybdenum disulfide (MoS_2) have been demonstrated to be excellent semi-conductors for ultra-thin FETs. However, unusually high contact resistance and Fermi level pinning have been observed due to damage at the metal-2D TMD interface. Studies have shown that van der Waals (vdW) contacts formed by dry transfer of graphene and metals can avoid damage to atomically thin TMDs caused by metal deposition.

My doctoral thesis focuses on study of metal-2D TMD interfaces through high resolution cross-section scanning transmission electron microscopy (STEM) observations of the atomic structure, X-ray photoelectron microscopy (XPS) to analyze the chemical environment, and electrical transport measurements to extract the Schottky barrier heights for electrons and holes. My results suggest that chemical reactions between metal contacts and 2D TMDs during deposition along with damage due to kinetic energy transfer are two main sources of defects at the metal-semiconductor interface that lead to the Fermi level pinning. To avoid this, I developed strategies based on soft metal, indium, as a buffer layer to realise ultraclean vdW contacts on atomically thin 2D MoS_2, WS_2, NbS_2 and WSe_2. Using electronic measurements, I have demonstrated that the contact resistance of indium electrodes is ~ 3000 Ω·μm for single layer and ~ 800 Ω·μm for few layered MoS_2 – amongst the lowest observed for 3D metal electrodes evaporated on MoS_2 and is translated into high performance field effect transistors (FETs) with mobility of ~ 170 cm^2-V^{-1}-s^{-1} at room temperature.

Furthermore, I have also achieved clean vdW contacts with high work function metals such as Pd and Pt by optimization of evaporation conditions. FETs with ambipolar characteristics with higher hole currents can be achieved on MoS_2 with Pd contacts and pure P-type characteristics can be achieved on WSe_2 FETs with Pt contacts. The results of my doctoral work suggest that it is possible to make ultra-clean metal contacts on 2D TMD semiconductors to obtain both N- and P-type FETs.

Dedication

To my parents, friends, and mentors

-for their love, support, and guidance

A person who never made a mistake never tried anything new.

- Albert Einstein

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Contents

Chapter 1 Context and Motivation

Metal oxide semiconductor field effect transistors (MOSFETs) have been the building blocks of integrated circuits. The increasing reliance on high-speed electronics for data processing has led to down scaling of the MOSFET dimensions. This is because the ON current increases with shrinking transistor channel length. As a result, the supply voltage and the delay time decrease while the operating speed of the chips becomes faster. Since the first transistor was invented in 1947 by John Bardeen, Walter Brattain and Walliam Shockley at Bell Labs[1], the dimensions of the transistors have gone through aggressive scaling over the past few decades. Although the semiconductor industry still follows Moore's Law[2], that is the number of transistors in an integrated circuit doubles every 18 months, the seemingly never-ending trend is facing great challenges.

The roadmap of device scaling in industry is shown in **Figure 1.1**. Several key milestones are labeled, such as development of high *k* dielectrics[3], FinFET and gate-all-around FET structures. The most advanced transistor was announced by IBM recently using gate-all-around (horizontal nanosheets) FETs with 2 nm node[4]. The 2 nm node does not mean the channel length is 2 nm. Historically, the node name referred to transistor feature size such as the gate length. With the introduction of FinFET, the transistor density has increased while the gate length has remained more or less a constant. The node naming has lost physical meaning and now it simply means new generation of chips with better performance and lower power consumption. The FETs in 2 nm node technology actually consist of three layers of 5 nm thick nanosheets with a gate length of 12 nm. In addition to structure optimization, new materials such as carbon nanotubes[5], III-V semiconductors[6] such as gallium arsenide and two-dimensional (2D) materials[5] to mitigate short channel effects are also being investigated for next generation of electronics. These materials are promising because of their intrinsic properties such as high mobility and low dielectric constant. Semiconductor channel materials that allow for high degree of coupling with gate voltage are also urgently needed.

The high performance of today's field effect transistors (FETs) is achieved by miniaturization of the channel down to nanoscale dimensions as shown in **Figure 1.1**. The decrease in source-drain dimensions has also necessitated the decrease in channel thickness to enable electrostatic control of the carriers (electrons and holes) in the channel. However, the channel lengths in state-of-the-art electronics have reached dimensions where bulk

semiconductor-based transistors have begun to experience high OFF state currents. This leakage current and the resulting heat dissipation related challenges are collectively referred to as short channel effects[7]. The presence of OFF state current in bulk semiconductor devices is responsible for dissipation of substantial power, which is a function of the drive voltage and the leakage current. Decreasing the drive voltage to decrease the energy cost of transistors leads to substantial increase in the OFF state current (a decrease in voltage by 60 mV leads a ten-fold increase in off state current). Novel device structures such as ultra-thin body silicon on insulator (UTB SOI), FinFETs, tunnel FETs (TFETs)[8] and planar atomically thin body transistors[9] are being actively pursued to address the challenges of high energy consumption and power dissipation encountered at short channel lengths.

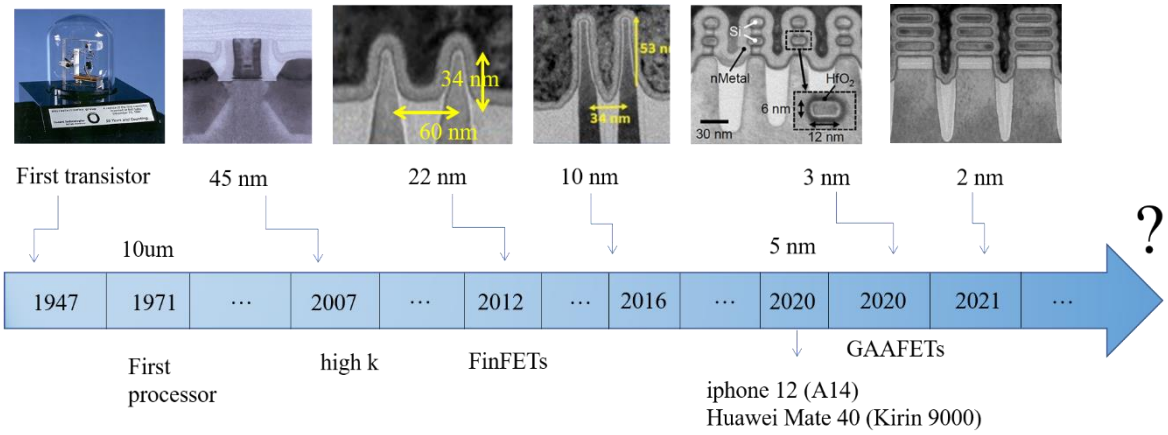


Figure 1.1 Roadmap of primarily silicon transistors scaling – from the first transistor made from bulk crystals in 1947 to this year's announcement by IBM of 2 nm node gate-all-around devices. In 2011, FETs shifted from planar devices to out of plane FinFETs. Starting in 2020, gate-all-around FETs (GAAFETs) of different structures were introduced.

Motivation for 2D TMD semiconductors in short channel FETs Therefore, semiconductor materials that allow scaling down to sub 10 nm channel lengths with minimal short channel effects are urgently needed. The characteristic channel "scaling length" (λ) for FETs is given by[10,11]:

$$\lambda = \sqrt{(\varepsilon_{channel} t_{channel} t_{ox})/\varepsilon_{ox}}$$

where $\varepsilon_{channel}$ is the dielectric constant of the channel, $t_{channel}$ is the thickness of the channel, t_{ox} is the insulating gate dielectric thickness and ε_{ox} is the dielectric constant of the gate insulator. Thus, smaller the characteristic length, the better the gate controls the channel and switches it off. Therefore, to achieve the smallest channel lengths, high dielectric constant gate insulators along with ultra-thin semiconductors are required. In principle, ultra-thin body (UTB) semiconductors from three-dimensional (3D) materials such as silicon can be achieved to

exploit the excellent electrostatics but they suffer from surface roughness that leads to scattering of the carriers, resulting in substantial degradation (mobility decreases in performance with thickness by sixth power, $\mu \sim t^6$ and band gap increases by square of thickness, $Eg \sim t^2$)[12]. The decrease in performance of UTB 3D semiconductors is partially related to creation of dangling bonds, interface states, and undesirable coupling with phonons.

2D TMD semiconductors such as MoS_2 that are naturally atomically thin can in principle mitigate several concerns related to short channel effects. Their atomically thin body allows excellent gate coupling because the carriers are confined within the sub 1nm thick semiconductor. The excellent gate electrostatics significantly decrease the leakage current. The fact that atomically thin individual layers of bulk-layered materials can be isolated necessitates the absence of dangling bonds, which means that surface roughness effects are absent. Recent progress suggests that such 2D TMD materials are promising for future electronics[13]. To illustrate the robustness of 2D semiconductors such as MoS_2 (single layer = 0.65 nm) against short channel effects, the characteristic scaling length for equivalent oxide thickness (EOT) of 1 nm is around 0.7 nm, an exceptionally low number showing that aggressive scaling down to few nanometers is possible with atomic thin semiconductors.

Importance of Contact Resistance in 2D TMD FETs: While the benefits of 2D TMD semiconductors in addressing short channel effects are obvious, they still possess lower performance compared to silicon and III-V semiconductor analogues due the high contact resistance[14]. To reap the benefits of short channel FETs, the contact resistances of atomic thin semiconductors must be reduced below the state-of-the-art down to the quantum limit[15]. The contact resistance (R_C) in FETs acts as a serious bottleneck for current flow through the channel because it reduces the effective gate voltage seen at the source injection point from V_G to V_G-I_DR_C. The drain current (I_D) therefore is greatly reduced because it depends strongly on the effective gate voltage at the contacts. For example, if we assume a $R_C \sim 1$ kΩ·μm, the voltage drops across just the contacts is $2I_DR_C \sim 2V$ to obtain a current of $I_D \sim 1$mA/μm. Thus, the contact resistances must be below ~ 0.1 kΩ·μm for energy-efficient logic switching.

Therefore, the primary motivation of my doctoral research was to understand the fundamental properties of metal-2D TMD semiconductor interfaces to realise low resistance N- and P-type contacts. To this end, my doctoral research has elucidated the atomic and electronic structures of metal-2D TMD semiconductor interfaces through high resolution microscopy and spectroscopy. My research has also provided insights into how to engineer the

interface to suppress Fermi level pinning and achieving low contact resistance N-type FETs. I have also realised high performance P-type FETs by utilizing high work function metals as contact electrodes. I describe my findings in Chapters that are organized in the following manner:

Chapter 2 provides detailed background on the structure (atomic and electronic), synthesis and characterisations of transition metal dichalcogenides (TMDs). Initially, the atomic and electronic structures of bulk and two-dimensional TMDs are described. Then synthesis methods that are relevant for this thesis are described. In the last part, I briefly describe the basics of main analytical techniques I used to characterise the TMDs.

Chapter 3 reviews and provides new insights in metal semiconductor junction physics for bulk and 2D semiconductors. The causes of Fermi level pinning and the approaches to unpin the Fermi level are discussed. I provide a framework for origins of Fermi level pinning based on metal/semiconductor interface physics. The mechanistic origins of Fermi level pinning in 2D TMD contacts are described and evidence from literature is provided as examples. Developments in engineering van der Waals (vdW) contacts on 2D TMDs are also summarized.

Chapter 4 describes the original experimental procedures for synthesis, characterisation and device fabrication for 2D TMDs. The improvements in sample preparation, residue minimization and characterisation made during my doctoral research are described. The challenges related to synthesis of 2D TMDs by CVD at device compatible temperatures, surface residue and other contamination along with development of method for preparation and imaging of cross-section TEM samples of 2D TMD/metal interfaces are described in this Chapter.

Chapter 5 describes original experimental results on realisation of vdW contacts based on indium alloys on 2D TMDs. The Chapter describes work to achieve low resistance indium contacts for N-type FETs. Work on Ti and Au contacts that leads to poor metal-2D TMD interface is also described for comparison. Detailed description of methods for making indium contacts, detailed characterisation of the indium 2D TMD interface using imaging and spectroscopy and device performance on different 2D TMDs is provided in this Chapter. In addition, description of work function engineering of contacts by alloying of indium with other metals is provided. Unpinning of Fermi level in vdW indium alloys contacts is described. Translation of indium knowledge to other soft metal contacts for clean contacts on 2D TMDs is also discussed in this Chapter.

Chapter 6 focuses on realising P-type FETs with high work function metal contacts. Clean contacts with high work function metals such as Pt and Pd on 2D TMDs are described. High performance P-type FETs are achieved for WSe_2 with clean Pt contacts. The efficient hole injection for MoS_2 is also demonstrated with clean Pd contacts. This Chapter also introduces substrate doping effect and its role in realising high performance P-type FETs. High performance photodiode utilising asymmetric contacts on TMDs are also demonstrated.

Chapter 7 summarises the main achievements from my doctoral work and provides suggestions for future work to exploit vdW contacts for devices.

Chapter 2 Two-dimensional Transition Metal Dichalcogenide Semiconductors

In this Chapter, I review the atomic and electronic structures of transition metal dichalcogenides, discuss how they are synthesized and how their chemical, electronic and atomic structures are characterised. Examples of methods, materials and characterisation results are given from the literature in this Chapter. The methods and analytical techniques discussed in this Chapter were used to carry out the research described in the thesis. Original results on materials synthesis and characterisation using the techniques described in this Chapter will be provided in Chapter 4.

2D materials are atomically thin. They are typically derived from layered materials that possess strong (covalent or ionic) bonding within the layer and weak van der Waals (vdW) bonding between the layers. The structure of 2D materials is intrinsically self-passivated so that most can be isolated into single layers without significant degradation of their properties. The absence of third dimension gives rise to unique optical, electrical and magnetic properties that are typically not present in their bulk counterparts[16,17]. Graphene, as the most successful case in 2D materials, has attracted great interest in exploring other 2D materials for novel device applications[18]. 2D transition metal dichalcogenides (TMDs) have also been widely studied because materials from this family can range from insulators, semiconductors and metals. 2D TMD semiconductors are the main focus of my doctoral research because unlike graphene, they possess a sizable band gap and fundamental properties such as low dielectric constant[18] and high effective mass[19] that are important for realising high performance short channel field effect transistors[20].

2.1 Transition metal dichalcogenides – structure, synthesis and characterisation

2.1.1 Crystal structure of TMDs

TMDs have the generic formula MX_2, where M represents a transition metal and X represents a chalcogen. Over 40 different TMD compounds can be realised via different combination of transition metals (from Group 4-10 in the periodic table shown below) and the chalcogens (S, Se, and Te shown as orange squares in the **Figure 2.1**[21]). Group 4–7 TMDCs are predominantly layered, while some of group 8–10 TMDCs form non-layered structures (as partially highlighted in the table). In layered structures, each layer consists of a hexagonally packed layer of metal atoms sandwiched between two layers of chalcogen atoms. Strong covalent

bonds extend through the atoms within the plane and weak van der Waals interaction exists between layers. The weak interlayer interaction makes it convenient to exfoliate bulk material into thinner nanosheets comprising a few or single layer.

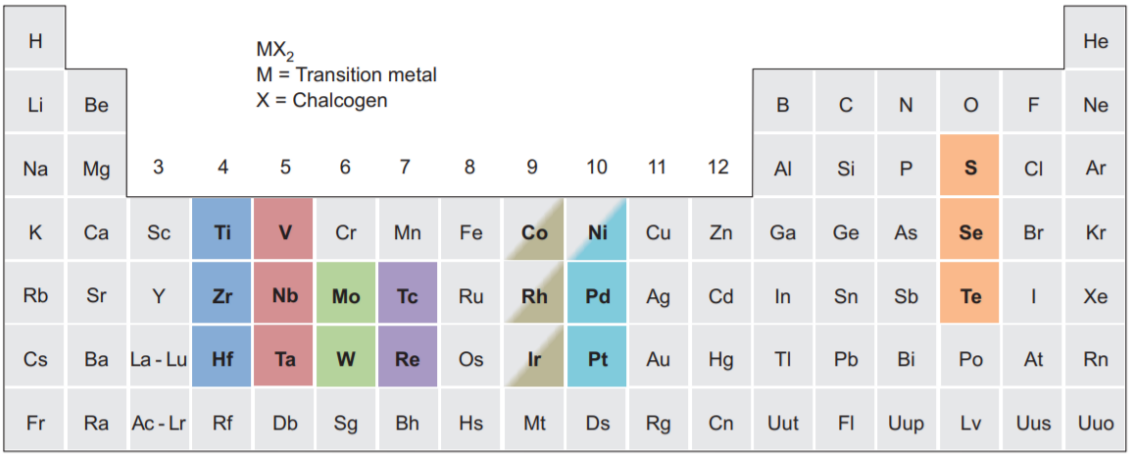


Figure 2.1 More than 40 different TMDs are possible. Transition metal and chalcogen (orange squares) atoms that form TMDs are highlighted. Partial highlights for Co, Rh, Ir, Ni, Pd, and Pt indicate that only some of the dichalcogenides form layered structures. The Figure is taken from Ref[21].

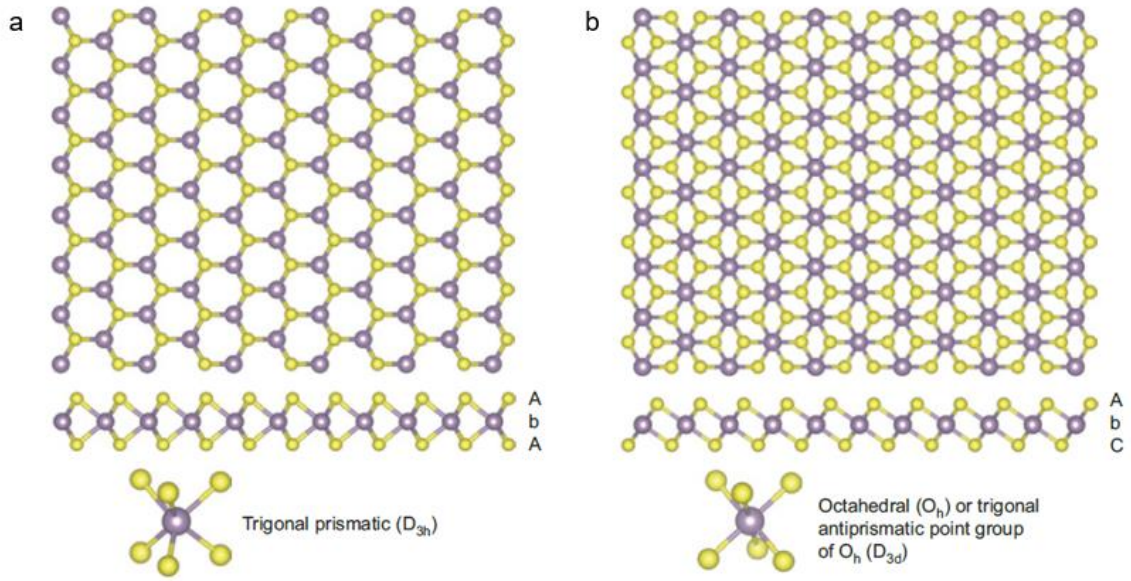


Figure 2.2 *c*-Axis and cross section view of single-layer TMD with (**a**) trigonal prismatic and (**b**) octahedral coordination. Atom color code: purple, metal; yellow, chalcogen. The labels AbA and AbC represent the stacking sequence where the upper- and lower-case letters represent chalcogen and metal elements, respectively. Reproduced from Ref[20].

Typical monolayer TMD consists of three atoms stacking together with metal atoms sandwiched between two planes of chalcogen atoms. Bulk TMDs are usually found in three crystal polymorphs: 1T, 2H and 3R. The number represents the number of layers needed to define the unit cell and the letters indicate crystal symmetry (T- trigonal, H- hexagonal, R- rhombohedral). The 2H phase has hexagonal configuration and each M atom is coordinated with six chalcogen atoms in a trigonal prismatic structure with a D_{3h} point group. In the 2H phase, one unit cell is defined by two layers with stacking sequence of AbA BaB as shown in **Figure 2.2a**. As shown in **Figure 2.2b**, 1T phase MoS_2 has a stacking sequence of AbC AbC and an octahedral coordination around the metal giving rise to a D_{3d} point group. The interlayer spacing in MoS_2 is ~ 6.5 Å. In addition to the crystal phases shown below, a distorted phase of 1T phase referred to as the 1T' phase also possible. The distortion in the structure helps increase its stability and calculations have suggested that the 1T' phase is more stable than the 1T phase[20].

The electronic properties of TMDs are predominantly determined by the number of *d* band electrons of the transition metal[21]. This is because the electronic states resulting from the chalcogens are located deep within the energy gap and therefore do not influence the optical or electrical properties. In contrast, the electronic states resulting from *d*-band of the transition metal are close to the Fermi level. The density of states (DOS) resulting from the *d*-band electrons are shown schematically in **Figure 2.3a** for TMDs with transition metals from different groups in the periodic table (**Figure 2.1**). Different *d* bond splitting occurs in TMD crystal structures with octahedral and trigonal prismatic coordinations. Octahedral coordination forms two non-bonding orbitals, $d_{yz,xz,xy}$ and d_{z^2,x^2-y^2}, while the trigonal coordination exhibits three *d* orbitals d_{z^2}, $d_{x^2-y^2, xy}$, and $d_{yz,xz}$. It can be seen from **Figure 2.3a** that if the highest *d* bands are fully occupied (indicated by dark blue states) such as in 1T-TiS_2, 2H-$MoSe_2$ and 1T-PtS_2, the TMDs exhibit semiconducting characteristics with a sizable energy gap between the valence and conduction bands with the Fermi level located within the gap. TMD with transition metals from groups 4, 6 and 10 s are typically semiconductors. In contrast, if the *d* bands are only partially occupied as in the case of 2H-NbS_2 and 1T-ReS_2, they exhibit metallic conductivity because the Fermi level is located within the band. Therefore, TMDs from groups 5 and 7 show metallic behavior. Thus, a crude approximation of whether a TMD is likely to be metallic or semiconduction can be from the number of electrons in the *d*-band of the transition metal – odd number of electrons may indicate metallic behavior while even number may suggest semiconducting behavior.

In addition to the number of electrons, the crystal phase of the TMDs is also important in determining the electronic properties. It is possible to engineer the phases of TMD materials by chemistry[22]. For example, the thermodynamically stable phase of MoS_2 is the 2H trigonal prismatic phase, which is semiconducting but it is possible to engineer it into the 1T phase, which is metallic[23].

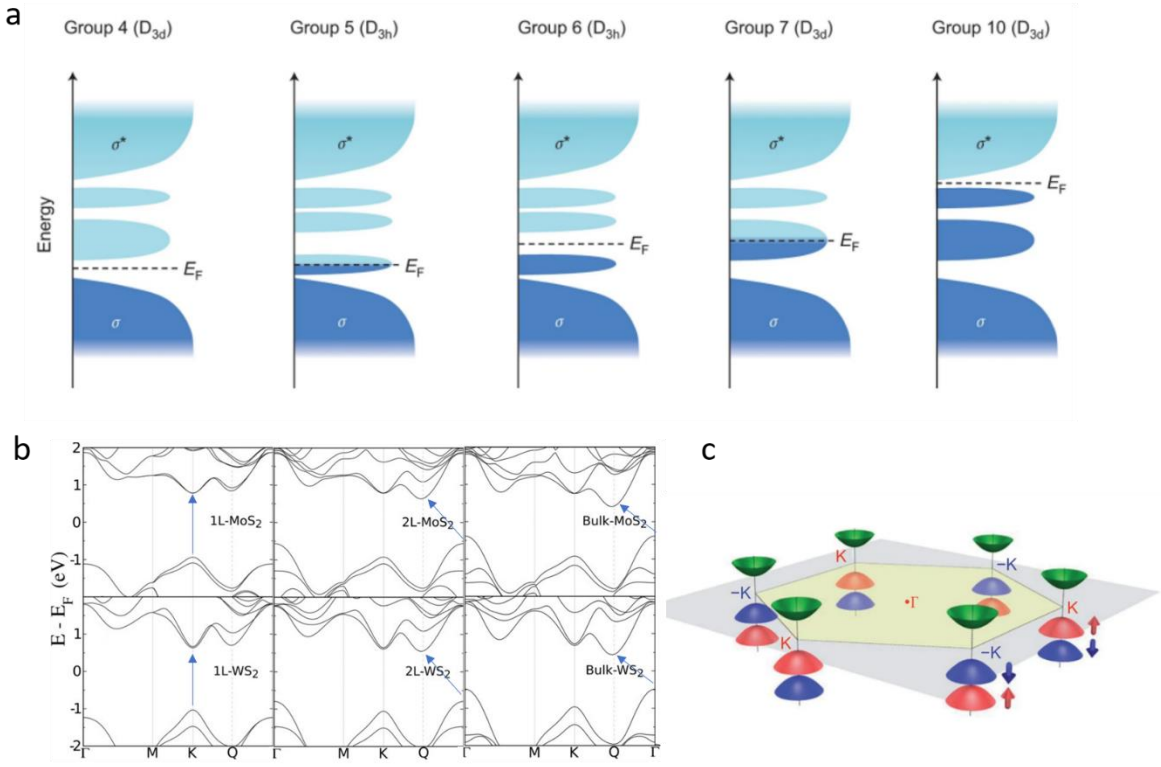


Figure 2.3 a, Schematic of density of states of TMDs with transition metals from different groups. The filling of d orbitals determine the bonding (dark blue labelled s) and anti-bonding states (light blue labelled s*). TMDs from groups 4, 6, and 10 are semiconducting and those from groups 5 and 7 are metallic. **b,** Calculated band structures of bulk, bilayer, and monolayer MoS_2 and WS_2[24]. Bulk MoS_2 is characterized by an indirect bandgap with a VBM at the Γ point and a CBM at the midpoint along Γ–K symmetry points in the first Brillouin zone. With reduced layer thickness, the indirect bandgap becomes larger. For monolayer MoS_2, it becomes a direct bandgap semiconductor with VBM and CBM coinciding at the K-point. **c,** Band structure of MoS_2 showing six valleys and opposite spin–orbit splitting of the valence band at the K and K' (−K) points[25]. The red and blue surfaces represent spin–orbit-split valence band maxima, each of which is associated with a particular electron spin. The green surfaces represent the conduction band minima or the valleys. Images are reproduced from Ref[24,25].

2.1.2 Band structure from 3D to 2D TMDs

The electronic properties of single layer TMDs are profoundly different from those of multi-layers. The main reason for this is the absence of weak interactions between the layers in monolayer TMD. The band structure of TMDs has been calculated from first principles density functional theory (DFT) to gain insights into their electronic structure.

The calculated band structure for bulk, bilayer and monolayer MoS_2 are shown in **Figure 2.3b**[24]. Unlike graphene, the TMDs contain two atoms (transition metal and chalcogen) in the unit cell for calculation of electronic structure. The band structure of TMDs (even for single layers) is completely different from the linear dispersion of graphene[26]. TMDs possess a sizable energy or band gap and the parabolic bands indicate that the carriers in TMDs are massive (in contrast to massless carriers in graphene) and the effective mass changes at different locations in the band structure. The band gap of bulk MoS_2 is ~1 eV with a valence band maximum (VBM) at the Γ point and a conduction band minimum (CBM) at the midpoint along Γ–K symmetry points in the first Brillouin zone. In contrast, the monolayer is a direct-gap semiconductor with VBM and CBM coinciding at the K-point. This indirect-to-direct bandgap transition from bulk to monolayer arises from quantum confinement effects (that is, absence of interactions between the *p* orbitals of sulfur atoms of adjacent layers). The direct band gap leads to enhanced photoluminescence in monolayers of MoS_2, $MoSe_2$, WS_2 and WSe_2, whereas only weak emission is observed in multilayers[27,28].

The first Brillouin zone of the reciprocal lattice of a typical group 6 TMD monolayer is shown in **Figure 2.3c**. The K points found at the six corners of the first Brillouin zone are inequivalent and therefore labelled as *K* and –K. A close examination of the band structure reveals that the energy level at the K and –K points in the valence band split at the momenta valleys (energy minima) due to the strong spin–orbit coupling in TMDs. Time reversal symmetry (a property in which motion is reversed when time is reversed) requires that the spin splitting at different valleys must be opposite, as shown in blue and red arrows in **Figure 2.3c**, where K and K′ show opposite orientations. This leads to a unique situation where spin and valley degrees of freedom are coupled. The valley states have been experimentally probed using circularly polarized light[25]. That is, when band edge electrons with a particular spin are excited with circularly polarized light, the electrons populate only one of the two valleys. When these electrons relax to the ground state, they emit circularly polarized light, which is an indication that valley polarization is present and preserved during the process. The ability to

achieve controlled valley polarization and its detection not only with light but also by other means (for example by electric field) could open up new ways for constructing switching 'valleytronic' devices.

The above shows that the single layer TMDs are exciting materials for opto-electronics. Therefore, it is crucial to optimize electrical contacts on monolayer TMD semiconductors. Much of the work on contacts has focused on multi-layered samples because they are easier to work with. They are also more forgiving in terms of tolerating poor contacts. While I also started with multi-layered TMD semiconductors, I used this knowledge to inform my work on monolayer TMDs. If the full potential of TMDs is to be realised then high quality contacts must be achieved on monolayers and despite the many challenges that is what I have tried to achieve during my PhD.

2.2 Synthesis methodology of TMDs

There are many methods for synthesizing TMDs[22]. For electronics, mechanical exfoliation and chemical vapor deposition are the most relevant. I have used both of these techniques to realise samples for field effect transistors. I also briefly describe chemical and liquid phase exfoliation for comparison.

2.2.1 Top-down exfoliation method

Mechanical exfoliation

Scotch tape was used to mechanically exfoliate few and single layers of 2D materials was first demonstrated by Novoselov *et al.*[29]. Since then, it has been widely used to produce high quality TMDs. In mechanical exfoliation, scotch tape is applied to the surface of a bulk layered crystal and then peeled off. This transfers flakes consisting of a small number of layers onto the tape. The scotch tape is then applied to the crystal again and peeled off again. This process is repeated several times before finally pressing the tape onto a substrate to transfer the flakes for study. This method has been successfully used to exfoliate TMDs, h-BN, and black phosphorous among others[22]. While the size and quality of monolayers are excellent with minimal defects due to the lack of chemical processing involved, the monolayer yield is low and there is no control over the size, shape and thickness. Despite the low yield, mechanical exfoliation remains widespread for laboratory studies because of the high quality of the samples.

Mechanical exfoliation is not suitable for large scale monolayer TMD production[30,31]. The mechanical exfoliated MoS_2 is shown in **Figure 2.4a**, with ~ 5 µm size monolayer[32]. Recently, several methods have been reported to enhance the yield and flake size of monolayer TMDs using mechanical exfoliation. Yuan *et al.* reported a modified mechanical exfoliation method for obtaining large sized TMDs[30]. They introduced two step process: substrate was first treated by oxygen plasma cleaning to remove any absorbates and an additional heat treatment to maximize the uniform contact area at the interface between the bulk crystal and the substrate. This led to flakes that were 50 times larger than the normal method.

Javey's group also reported a gold-mediated exfoliation method to obtain large monolayers[31]. Since the bond between gold and first TMD layer is stronger than van der Waals force between TMD layers, this enables selective peel off the first layer using a thermal tape which can be dissolved by acetone. The exfoliation result is shown in **Figure 2.4b**, exhibiting much larger monolayer MoS_2 (~500 µm) compared with simple mechanical exfoliation. The detailed of gold mediated transfer are shown in **Figure 2.4c**. The quality of monolayers

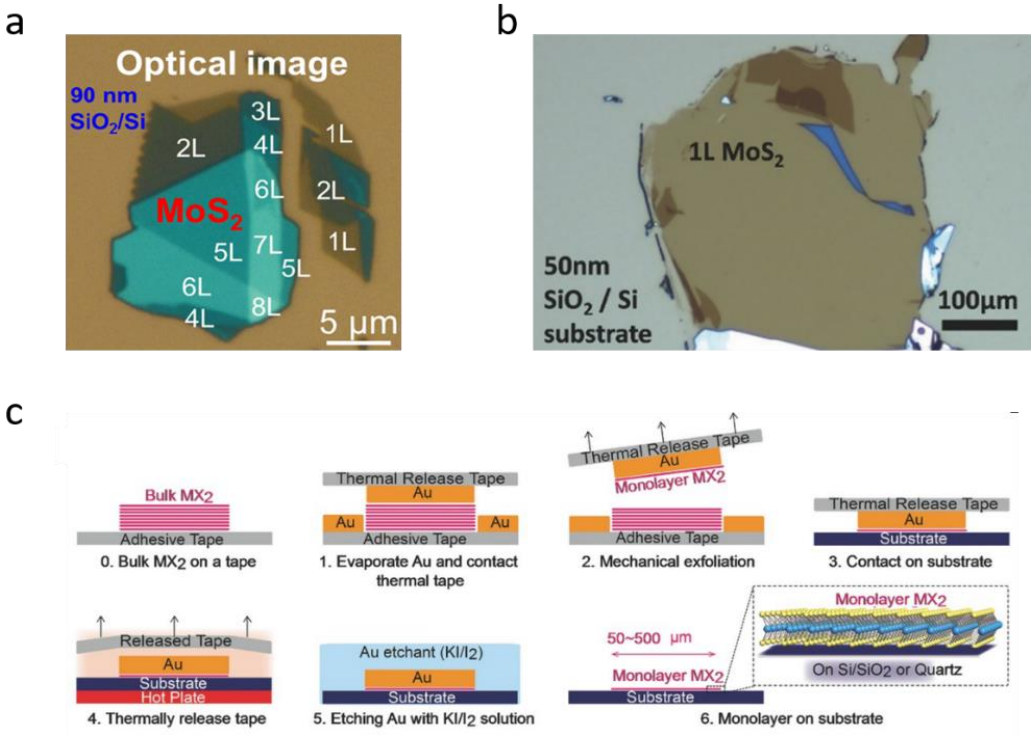


Figure 2.4 a, Optical microscope image of MoS_2 with different thicknesses exfoliated onto SiO_2(90nm)/Si substrate. **b,** Optical microscope image of the large-scale monolayer TMD exfoliated by Au assisted exfoliation method. **c,** Schematic illustration of the Au assisted exfoliation method. Images are reproduced from Ref[31,32].

obtained by this Au assisted exfoliation method is measured by photoluminescence (PL), the overall PL intensity is comparable to scotch tape exfoliated samples.

Liquid phase exfoliation (LPE) is another common method to exfoliate bulk crystals. Generally, solvents such as N-methylpyrrolidone (NMP) and dimethylformamide (DMF) are added to layered bulk crystals followed by sonication[33]. Sonication facilitates exfoliation by breaking the interlayer van der Waals forces but not the intralayer strong bonds. Good matching of the surface tension between the layered crystal and the solvent is important in enhancing exfoliation efficiency[33]. Chemical exfoliation is slightly different from LPE because some chemical interaction between the solvent and layered materials is used to facilitate exfoliation. The Chhowalla group has pioneered exfoliation of TMDs using n-butyllithium chemical exfoliation process[23]. In this method, lithium ions intercalate between the layers so that the lithiated material is easily exfoliated upon very mild sonication. The n-butyllithium method also leads to phase transition during exfoliation process. In semiconducting TMDs, phase transformation from the 2H to 1T occurs. While liquid phase and chemical exfoliations methods are low cost, the lateral dimension of the layers is submicron and the materials contains very high level of defects such as chalcogen vacancies and edge states – making them less useful for high performance electronics.

2.2.2 Bottom-up growth method

Chemical vapor deposition (CVD) is promising for wafer scale monolayer TMD growth. In general, the quality and size of CVD grown TMD samples are affected by parameters such as precursors (metal oxide typically for the transition metal and chalcogen powders), reaction temperature, gas flow rate, reaction pressure, type of substrate (SiO_2 is most commonly used but vdW epitaxy growth on h-BN has also been demonstrated[34,35]), and promoter. Recently, promoter such as perylene-3,4,9,10-tetracarboxylic acid tetrapotassium salt (PTAS) or 3,4,9,10-perylene-tetracarboxylicacid-dianhydride (PTCDA) in CVD has been shown to give large area high quality crystals[36]. It is believed that PTAS and other aromatic molecules help to lower the free energy for nucleation of TMDs. Furthermore, sodium and potassium salts such as NaCl, NaOH, KBr, and KOH have been reported to enhance the lateral size and lower the growth temperatures of TMDs[37–39]. CVD in the laboratory is typically performed using a tube furnace in a set up similar to that shown in **Figure 2.5** for growth of MoS_2. This is thermal CVD where temperature because temperature is used to initiate the reaction. I have built and used the tube furnace for the growth of high quality monolayer MoS_2. While I performed some

optimization of the process to obtain high quality monolayer MoS_2, my main interest was in using the material in electronic devices. Therefore, I describe thermal CVD method briefly here. Other researchers have used the technique to obtain different monolayer TMDs such as WS_2[40], WSe_2[41], $MoSe_2$[41] and their lateral heterostructures[42].

In CVD synthesis of TMDs, the reaction chamber (usually a tube furnace as shown in **Figure 2.5**) is typically heated to 650 °C in a nitrogen (N_2) environment. At this high temperature, the precursor powder (such as MoO_3 for MoS_2) is reduced by the sulfur vapor to form volatile suboxide: e.g. MoO_{3-x}. These suboxide compounds then diffuse to the substrate and further react with sulfur vapor to grow MoS_2 films in the form of triangles (shown in optical microscope image in **Figure 2.5**) that are single layers. The typical reaction pathway for MoS_2 by CVD is:

- $MoO_3(s) + {}^{x}/_{2}\, S(g) \xrightarrow{650^{o}C} MoO_{3-x}(g) + {}^{x}/_{2}\, SO_2\ (g)$
- Bulk transport of MoO_{3-x} (g) and S (g)
- Surface adsorption of MoO_{3-x} (g) and S (g)
- $MoO_{3-x} + \left(3 - {}^{x}/_{2}\right)S \xrightarrow{800^{o}C} MoOS_2 + \left(1 - {}^{x}/_{2}\right)SO_2$
- $MoOS_2 \xrightarrow{800^{o}C} MoS_2\,(s) + {}^{1}/_{2}\, O_2\ (g)$
- Bulk transport of O_2 away from the chamber

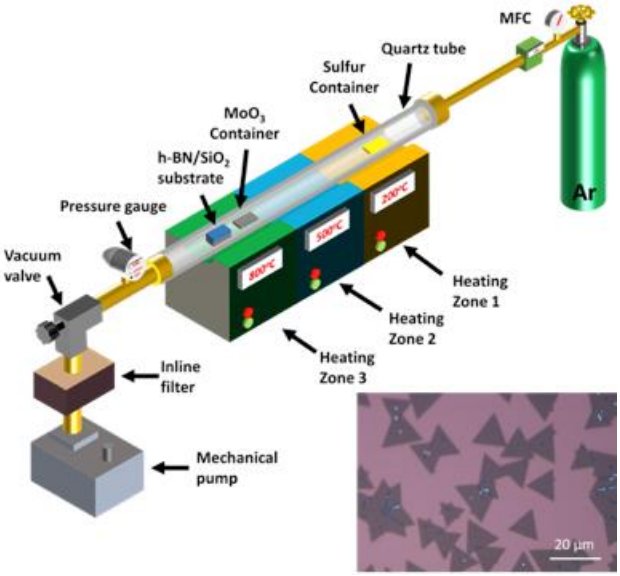


Figure 2.5 Schematic diagram of a CVD growth setup. The image is reproduced from Ref[43].

An example of MoS_2 growth results with and without PTAS are shown in **Figure 2.6**. Under the same growth conditions, uniform monolayer MoS_2 is obtained with PTAS promoter while only small MoS_2 particles are observed without PTAS.

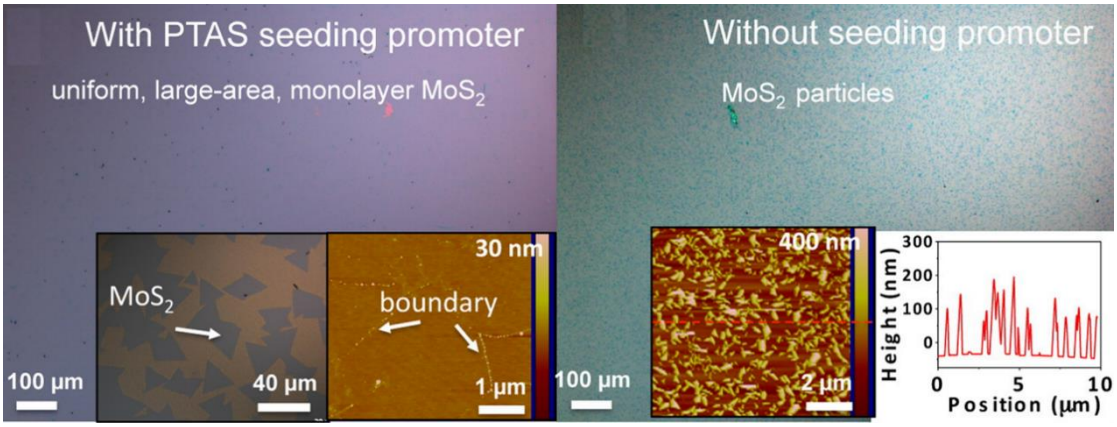


Figure 2.6 Optical microscope image of the CVD grown MoS_2 with and without PTAS seed promoter. The image is reproduced from Ref[36].

2.3 Characterisation of TMDs

2.3.1 Raman spectroscopy

Raman spectroscopy is a widely used technique to analyze 2D materials based on inelastic scattering of monochromatic light[44,45], usually a laser source. The scattering energy diagram is shown in **Figure 2.7a**. When a photon with frequency υ_0 been absorbed by a molecular, the excited molecular returns to the same base energy level and emits photon with the same energy $h\upsilon_0$. This type of scattering is called Rayleigh scattering. In other circumstances, when a photon interacts with a molecular at the base energy level and part of the energy $h\upsilon_m$ transferred to the active mode, the scattering photon energy is reduced to $h\upsilon_0 - h\upsilon_m$. This scattering is called Stokes Raman scattering. On the contrary, when a photon interacts with a molecular that already in excited state $h\upsilon_m$ and return to base energy level, the emitted photon energy goes up to $h\upsilon_0 + h\upsilon_m$. This scattering is called Anti-Stokes Raman scattering. In general, the Stroke scattering with higher intensity as shown in **Figure 2.7b** is used for analysis. The information of each detected wavelength is converted to the difference with the wavenumber of incident laser. **Figure 2.7b** at the bottom depicts the relation between Raman shift and the wavelength of the photon after interaction with molecular. The Raman shift can be calculated by the following equation:

$$\text{Raman shift } (\text{cm}^{-1}) = \frac{10^7}{\lambda_{ex}(\text{nm})} - \frac{10^7}{\lambda(\text{nm})}$$

Where λ_{ex} is the wavelength of the incident laser and λ is the wavelength of the Raman scattered photon.

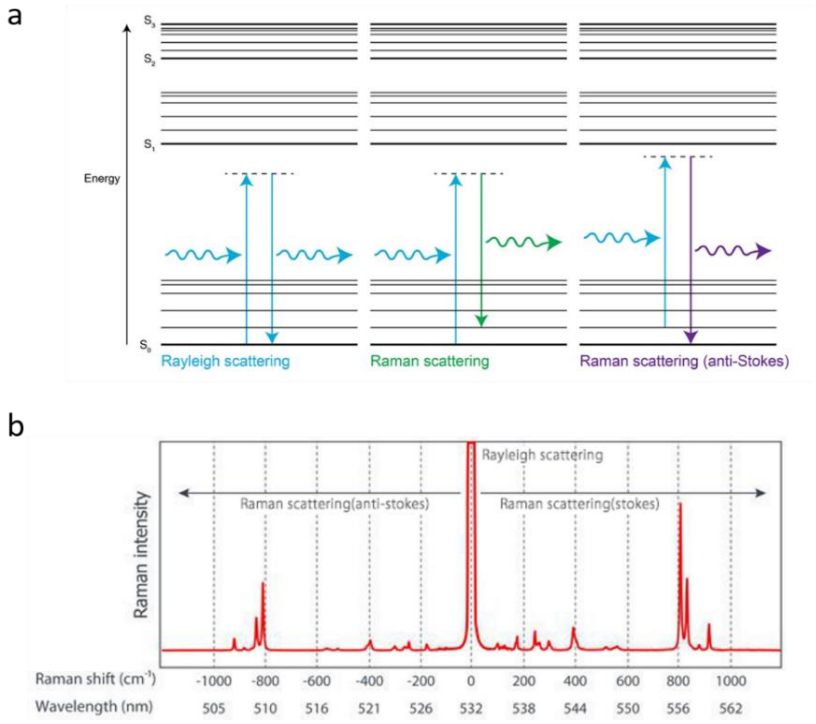


Figure 2.7 a, The scattering energy diagram. **b,** Relation between Raman shift and the wavelength of a photon after interaction molecular. Reproduced from Ref[46].

The molecular vibration information can be obtained from the Raman peaks. The width of the peak represents the degree of disorder of the material[47] and the shift of the peak position represents the in-plane stress[47]. Raman scattering was first applied to characterise different layers of MoS_2 down to monolayer by Lee *et al*[48]. The result is reproduced in **Figure 2.8** shows representative in-plane E^1_{2g} peak at 383.5 cm^{-1} and out-of-plane A_{1g} peak at 408.6 cm^{-1}. The main finding is that the E^1_{2g} vibration red shifted and the A_{1g} peak blue shifted with increasing layer number of the MoS_2. For layer number over four, the Raman peaks stay the same as bulk MoS_2. The reason for shift of E^1_{2g} and A_{1g} peaks is studied by calculation showing that due to change in atomic bonding length as well as the interlayer coupling[49,50]. The interlayer distance *c* increases with reduction of the layer numbers. The interlayer coupling also lead to electron redistribution among Mo and S atoms which changes the electronic properties for different layer MoS_2. Similar trends are observed in other TMDs such as $MoSe_2$, WS_2 and WSe_2[51–53].

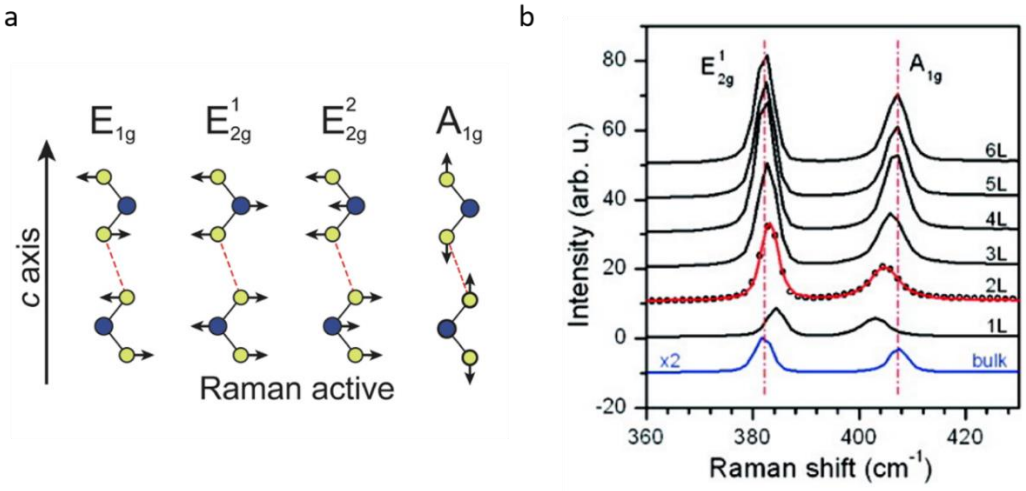


Figure 2.8 a, Schematic of the Raman active modes of MoS_2. **b,** Raman spectroscopy of MoS_2 showing E_{2g} and A_{1g} modes position for different thicknesses. Figures are reproduced from Ref[48].

2.3.2 Photoluminescence (PL)

Photoluminescence is a process in which the semiconductor absorbs a photon and excites one of its electrons to a higher electronic excited state, then radiates a photon when the electron returns to the ground energy state. The PL process schematic for direct bandgap semiconductor is shown in **Figure 2.9a**. When the direct bandgap semiconductor is illuminated with a photon that having greater energy than the bandgap, an electron from the valence excites to the conduction band, leaving a hole behind in the valance band. Then the excited electron relaxes back to the minima position of the conduction band, and the hole relaxes to the minima of the valence band. Eventually, the electron falls back to the conduction band, recombine with the hole and emits a photon with same energy of the semiconductor bandgap. However, the actual energy of the emitted photon is slightly lower than the band gap energy in TMDs due to strong binding between the electron-hole pair[54]. The exciton (electron-hole pair) binding energy in monolayer TMDs can be hundreds of meV[55] and this strong Coulombic attraction means that the excited electrons reside just below the conduction band and excited holes are located just above the valence band – giving photons of energies lower than the band gap energy.

In addition to band-to band recombination, there are also sub-band emissions that originate from defect states or impurity energy levels within the bandgap, as illustrated in **Figure 2.9b**. Type 1 and type 2 recombinations involve only one trapping energy level so that the PL energy directly reflects the defect trapping energy levels in the bandgap. Type 3 requires two or more trapping energy levels – making it difficult to determine the trapping energy levels. However,

if one of the trapping energy levels from shallow states (near conduction band or valence band), the PL exhibits strong thermal quenching characteristics due to carriers at the trap states relaxing back to the band edge.

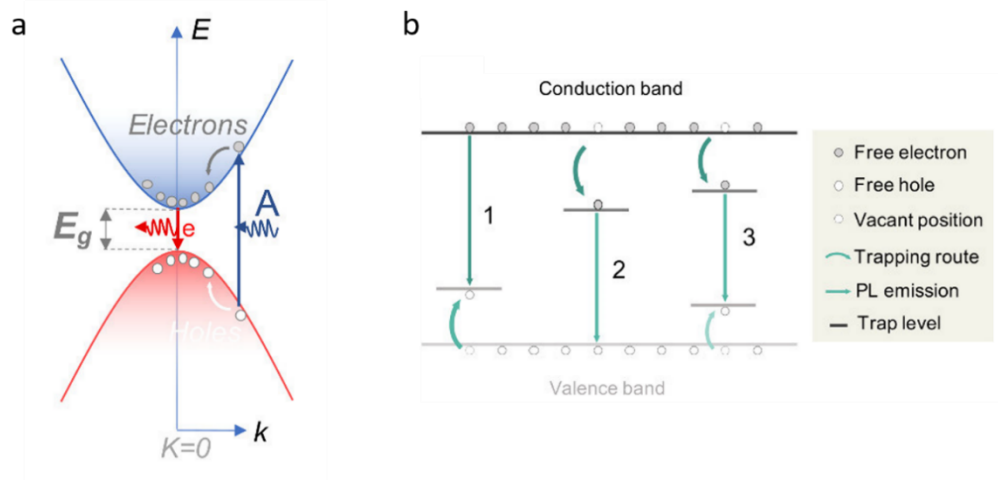


Figure 2.9 a, PL process for direct bandgap semiconductors. **b,** Schematic diagram for trap associated luminescence. The figures are reproduced from Ref[56].

Monolayer of group 6 TMDs such as MoS_2 is direct bandgap semiconductor where the lowest energy inter band transition occurs at the K point of the Brillouin zone. The prominent PL peaks A (~1.84 eV) and B (~2.00 eV) originate from the A and B excitons that arise from valence band splitting due to the large spin-orbit coupling[57]. A dramatic PL enhancement is observed as the thickness decreased down to monolayer, as illustrated in **Figure 2.10**. The peak

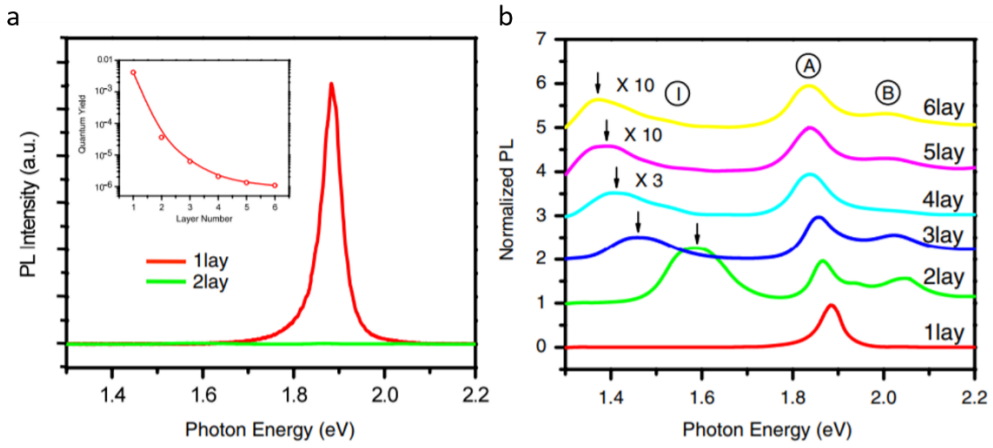


Figure 2.10 a, PL spectra for mono- and bilayer MoS_2 samples. **b,** Normalized PL spectra by the intensity of peak A of thin layers of MoS_2 from monolayer to six layers. The figures are reproduced from Ref[57].

position also moves to higher energies with decreasing number of layers. This is attributed to the indirect-to-direct bandgap transition shown in **Figure 2.3b**. For bilayer MoS_2, an indirect bandgap around 1.6 eV is more dominant than the direct bandgap PL signal, as shown in the green curve in **Figure 2.10b**. Qualitatively similar results are observed for other TMDs such as WS_2 and WSe_2 with the PL signal of monolayer 100- 1000 times higher than the bulk layers[58].

2.3.3 Atomic force microscopy (AFM)/Kelvin probe force microscopy (KPFM)

Atomic force microscopy (AFM) has a resolution below one nanometer in height and ~10 nm laterally, which is ideal for characterisation the thickness of different layer of TMDs. AFM measurement setup is shown **Figure 2.11a,** which consists of a cantilever with a sharp tip (probe) used to scan the specimen surface. When the cantilever is brought close to the sample surface, the tip is attracted towards the surface under the dominant influence of the van der Waals forces (blue line region in **Figure 2.11b**), which lead to deflection of the cantilever. When dF/dx exceeds the cantilever spring constant, the tip snaps into contact with the sample (red line region in **Figure 2.11b**). The repulsive Coulombic forces caused by the electrostatic interactions of the electrons in the tip with the electrons in the sample becomes dominant and follows Hooke's law: F = -kx. These deflections are measured using a laser beam, reflected from the cantilever and collected by a photodetector. Beyond topography measurement, AFM can also map adhesion, conductivity, surface potential, piezoelectric properties,

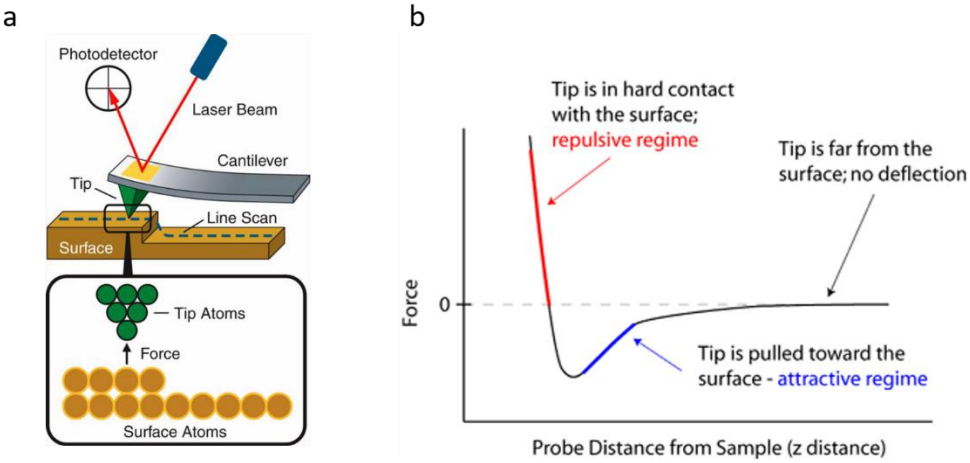


Figure 2.11 a, Scheme of a measurement with the AFM. A tip is approached towards the surface and a line scan is performed. The interaction between the tip and the surface is detected by the deflection of the laser beam resulting from movement of the cantilever due to differences in surface morphology. **b,** Force experienced on the cantilever tip depending on the distance from the sample surface. The images are reproduced from Ref[59].

electrochemistry, and work function. In this thesis, surface potentials of the TMDs are studied with AFM. Kelvin probe force microscopy (KPFM) is used to obtain changes in surface potentials on TMDs and therefore KPFM is introduced in the following section.

KPFM measures the local potential difference between the conducting cantilever and the TMD surface while scanning over the sample. When the cantilever approaches the sample, the difference between work function of the sample and the tip causes a built-in potential. An extra electrical potential is needed to nullify the built-in potential. The applied energy level is the work function difference between the tip and the sample. The tip usually has a fixed work function with Au coated surface or can be aligned by measuring highly oriented pyrolytic graphite (HOPG) which has a fixed work function of 4.6 eV. Then the work function of measured sample can be extracted by the following equation:

$$V_{CPD} = \frac{\Phi_{tip} - \Phi_{sample}}{-e}$$

Where Φtip and Φsample are the work function of the tip and sample, V_{CPD} is the contact potential difference.

Wang *et al.* were able to image the spatial work function variation in a CVD grown WS_2 flake by KPFM[60]. The topography AFM image and the corresponding KPFM work function mapping of the WS_2 flake are shown in **Figure 2.12**. The topography image clearly shows trigonal WS_2 and the HOPG substrate layers. The KPFM work function mapping indicates

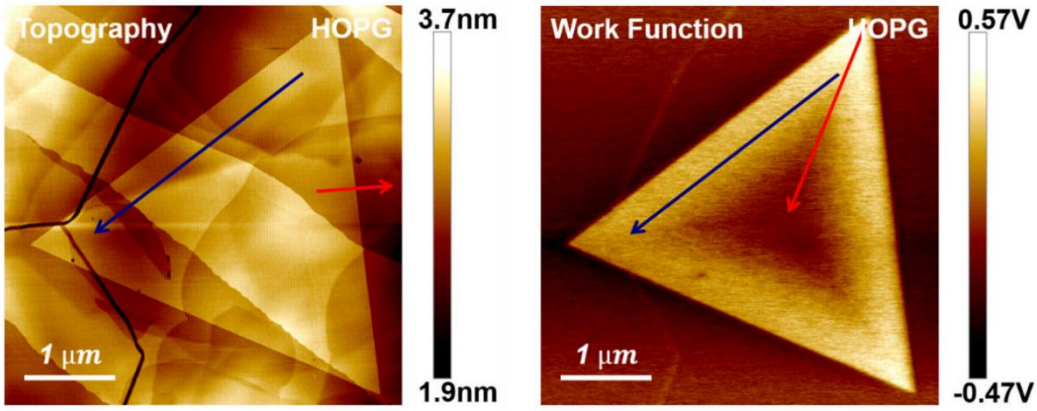


Figure 2.12 Left image is topography of monolayer WS_2 on HOPG. Right image is the corresponding KPFM mapping showing work function variation across the triangle. The blue arrow shows same work function at the edge of the triangle and the red arrow across the flake shows 0.6 eV difference from the edge to the center. Images are reproduced from Ref[60].

variation work function values up to 0.6 eV between center of the flake and edges of the triangle (along the red arrow in the work function map). Further analysis was done by scanning transmission electron microscopy and calculation, showing that the center has more antisite (S sitting in W vacancy) defects that causes Fermi level lift up. The results demonstrated that KPFM can be applied to unveil the spatial work function of 2D materials with high sensitivity.

2.3.4 X-ray photoelectron spectroscopy (XPS)/Auger electron spectroscopy (AES)/Ultraviolet photoelectron spectroscopy (UPS)

X-ray photoelectron spectroscopy (XPS) is a technique for analyzing the surface chemistry of a material[60]. The schematic of the photoelectron and Auger electron emission process are shown in **Figure 2.13**. XPS spectra are obtained by irradiating surface with a beam of X-rays (200-2000 eV) while simultaneously measuring the kinetic energy of electrons that are emitted from the surface of the material being analyzed. The core level electron in 1*s* orbital emits after absorbing the X-ray energy. The kinetic energy (KE) of the electron depends upon the photon energy ($h\upsilon$) and the binding energy (BE, relative to the Fermi level, specific energy for each element) of the electron.

$$\mathrm{KE} = h\upsilon - \mathrm{BE} - \emptyset_{\mathrm{spec}}$$

Where $\emptyset_{\mathrm{spec}}$ is the work function of the spectrometer. The X-ray source in XPS is monochromatic so that the discrete binding energies of the electrons can be determined. Since the electron binding energy is affected by the chemical surroundings, it is possible to determine which elements are on the surface and their chemical state by measuring the kinetic energy of the emitted electrons. XPS sensitivity is around 0.1% and depth resolution is around 10 nm[61]. Thus, XPS is ideal to analysis chemical composition and charge transfer through binding energy shift. For example, chemical exfoliated MoS_2 by butyllithium accepts electrons from Li forming 1T phase MoS_2[23]. This can be detected by XPS: the Mo 3*d* spectra exhibits peaks at ~ 229 and 232 eV that correspond to Mo $3d_{5/2}$ and $3d_{3/2}$ spectra,respectively[62]. Deconvolution of the peaks shows that the Mo binding energy of 1T MoS_2 shifted to lower binding energy by ~0.9 eV with respect to 2H MoS_2. Same trend is observed for the S 2*p* spectra. The lower binding energy can be explained by lower oxidation state of Mo in $LiMoS_2$[63]. For the XPS shift due to charge transferring, substitution bonding can be understood by electron/hole doping without oxidation state change[64–66]. The doping caused Fermi level shift will also lead to binding energy shift in XPS spectra as the binding energy is core level energy to Fermi level.

Thus, electron doping of the TMD will cause Fermi level up shift and binding energy level going higher. On the contrary, hole doping will lead to lower binding energy.

Auger Electron Spectroscopy (AES) is similar to XPS except the emitted secondary electron is analyzed rather than the primary electron[67]. An incident X-ray or electron creates a core hole in the core level such as 1*s* level in the schematic shown in **Figure 2.13**. An electron from the 2*p* level fills the 1*s* hole and emits an X-ray photon with the energy of core level difference. This emitted X-ray photon kicks off another electron in the 2*p* level to emit and this emitted Auger electron is analyzed by spectrometer. Thus, the kinetic energy of the emitted Auger electron is equal to the first emitted photoelectron binding energy (EB1) minus the binding energy level of the electron that fills the vacancy (EB2), minus the core level binding energy where the Auger electron is emitted (EB3).

Ultraviolet Photoelectron Spectroscopy (UPS) operates on the same principles as XPS, the only difference being that ionizing radiation source is tens of eV (photons emitted by helium gas have energies of 21.2 eV or 40.8 eV). As lower energy photons are used, most core level photoemissions are not accessible using UPS, the spectral is limited to the valence band region. Thus, only the valance band position and work function information can be obtained from XPS measurements. A typical XPS spectra is given in **Figure 2.14a** with the intensity versus binding energy using a He 21.2 eV source[68]. The work function of the material is extracted by the difference between the source and cutoff region at high binding energy (low kinetic energy

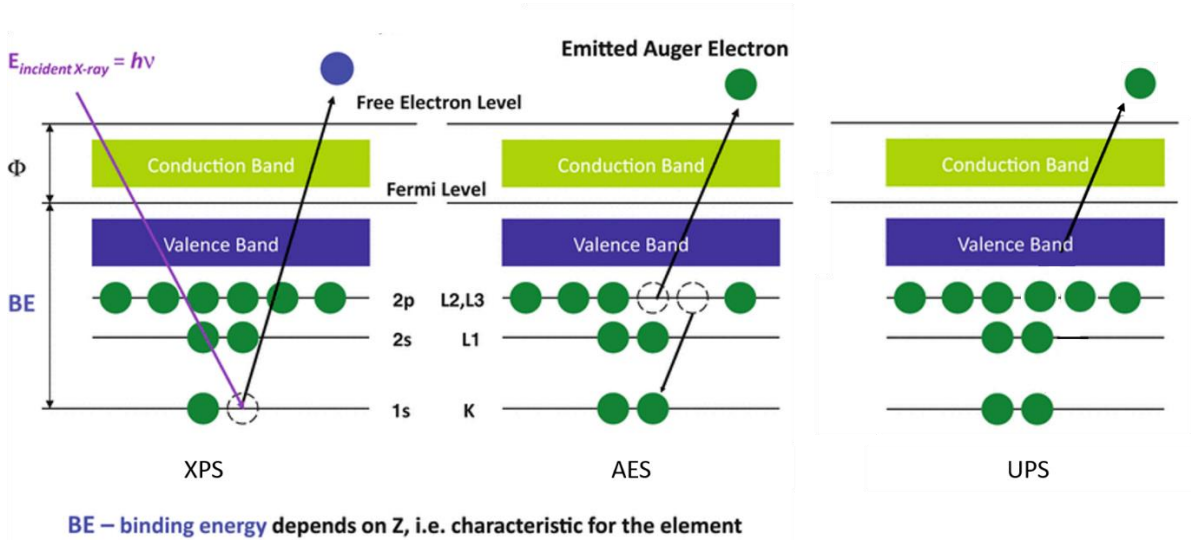


Figure 2.13 Schematics of XPS, AES and UPS measurement process. The images are reproduced from Ref[67].

labeled in the figure). Fermi level position to valence band level can also been obtained from the low binding energy region. This technique is helpful in determining metal-semiconductor interface band alignments as well as providing insight into how TMD energy levels vary with doping[69–71]. For example, Chen et al. studied the work function of WSe_2 before and after Au nanoparticle decoration[72]. As shown in **Figure 2.14b**, the pristine WSe_2 sample has around 1.8 eV from valence band edge to Fermi level position while the Au decorated sample exhibits around 1.37 eV, indicating P type doping of the Au nanoparticles. The high binding energy edge also shows 0.43 eV enhancement after Au doping. The energy band diagram of WSe_2 before and after Au decoration can be drawn as **Figure 2.14c**.

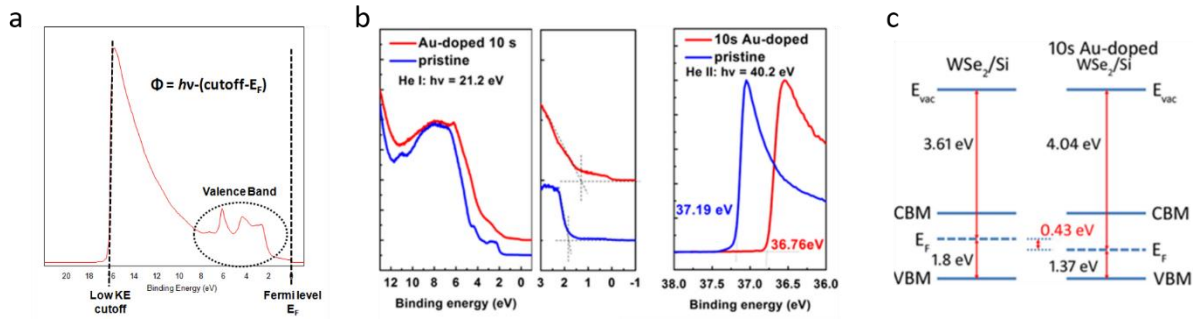


Figure 2.14 a, Typical XPS spectra showing the valence band edge and the binding energy cutoff for work function calculations. **b,** XPS of WSe_2 before and after Au decoration showing p type doping on WSe_2 with Au. **c,** Energy band diagram of WSe_2 before and after Au decoration extracted from the XPS measurements. Figures are reproduced from Ref[68,72]. [Small typo in the original figure from publication. The energy of He source should be 40.8 eV in Figure **b**. This does not affect the conclusions].

2.3.5 Transmission electron microscopy (TEM)

Transmission electron microscopy (TEM) is a powerful and versatile technique, it can provide not only high resolution imaging but also characterize the crystal structure through electron diffraction, chemical composition and electronic structure of the material through interaction with core level electrons. The main strength of TEM lies in its extremely high resolution (~ 0.08 nm) due to large electron lens and small wavelength of the electrons. The schematic of a transmission electron microscopy is shown in **Figure 2.15a**. An electron gun (thermionic or field-emission) works as the electron illumination source. The electrons accelerated from the electron source are focused into a small beam by the condenser lens and traverses the sample. Then the transmitted electron beams are focused by the objective lens to form the first image. This image is further magnified by the intermediate lens and projector lens onto a screen or

camera. The contrast on the screen is affect by atom mass, thickness and diffraction of the sample. Without considering the Bragg diffraction, a higher mass region scatters electrons at higher angles, thus fewer electrons contribute to the imaging. Oppositely, the low mass region forms a brighter image on the screen. Thickness of the sample has similar effect as the mass.

In scanning transmission electron microscopy (STEM), a sub-angstrom electron beam is scanning across the sample then several signals can be detected simultaneously to form images, the principle of the STEM is shown in **Figure 2.15b**[73]. The high-angle annular dark-field (HAADF) detector collects Rutherford scattering from the atomic nuclei, producing an image with strong sensitivity to atomic number Z. The HAADF image is collected at angle larger than 50 mrad. Annular bright-field (BF) detectors, located within the cone of illumination of the transmitted beam (less than 10 mrad) have been used to obtain images of light elements such as oxygen due to less scattering. If the bright-field detector is removed, electrons can be passed through a magnetic sector electron energy loss spectrometer to provide electronic structure information of the sample. A typical electron energy loss spectroscopy (EELS) records the energy distribution of electrons that pass through the sample, which can be classified into three

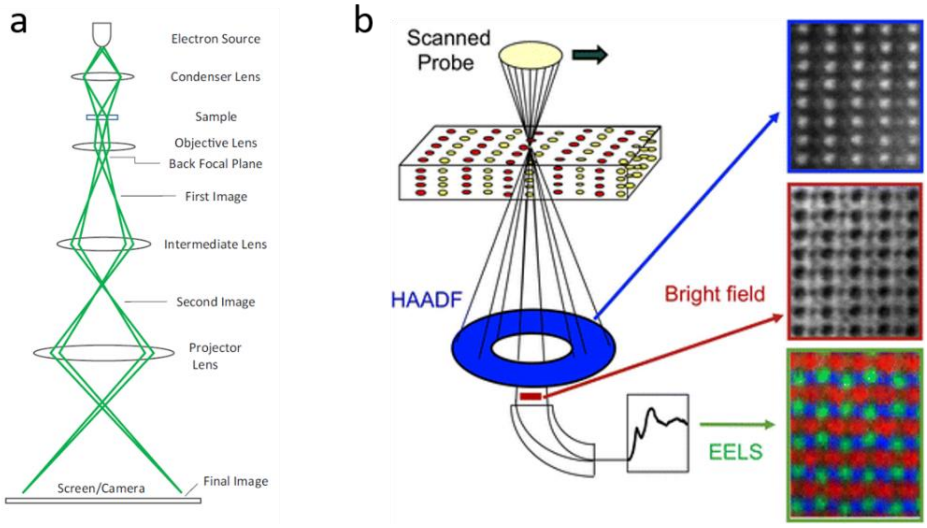


Figure 2.15 a, Schematic of a transmission electron microscope (TEM). **b,** Working principle of scanning transmission electron microscope (STEM) showing where high angle annular dark field (HAADF) and bright field (BF) images as well as where EELS spectra are collected. Top right is a HAADF image of $BiFeO_3$ where the brightest dots indicate Bi atoms and the less bright ones are Fe atoms. The center image is a bright-field image showing O columns. Below is a color composite EELS image of $LaMnO_3$ in which the Mn is shown in red, O in green, and La in blue. The images are reproduced from Ref[73,74].

regions. The zero-loss peak locates at 0 eV represents elastically scattered electrons. The region lower than 50 eV is the low-loss region, which represents electrons interact weakly with outer shell electrons. The high-loss region results from inner shell electrons excited to an unoccupied shell above the Fermi level when the electron beam interacts with the specimen. The spectrum in high-loss region is usually used to identify the element component of the sample.

TEM has been widely used to characterize TMD structure, atomic defect, and phase transition down to atomic level[75,76]. For example, vacancies are very common defects in 2D materials such as MoS_2, especially the CVD grown samples. The STEM is capable of distinguish a single S vacancy from a disulfur vacancy, as well as antisite defects from pristine lattice sites. The defects are classified into two categories: vacancies and antisite defects, as shown in **Figure 2.16**. The top left label represents the defect tape in the STEM image, V means vacancy and Mo_{S2} means antisite defect of Mo atom sitting in S position.

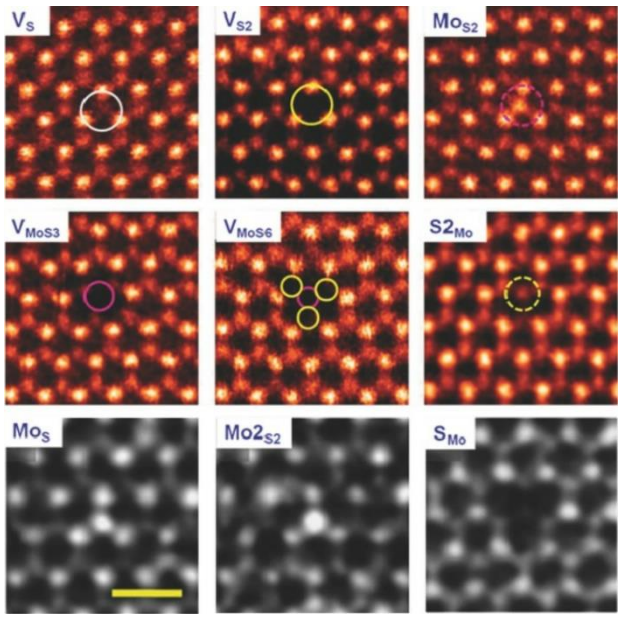


Figure 2.16 STEM image of various defect types in MoS_2. The defect type is labelled at the top left in each image. V means vacancy and Mo_{S2} means antisite defect of Mo atom sitting in S position. The images are reproduced from Ref[77,78].

Chapter 3 Contacts for 2D Semiconductors

Metal-semiconductor contacts are the foundation stone of modern electronic circuits. To fully utilize the fundamental advantages of 2D TMDs for short channel devices, high-quality contacts for both N-and P-type field effect transistors (FETs) must be achieved. In this Chapter, I will describe the basics of the metal-semiconductor interface for both three- and two-dimensional semiconductors. I will then describe Fermi level pinning that is widely observed when metals are contacted with 2D TMD semiconductors and explain its possible origins. In the final part of this Chapter, I will introduce different strategies that have been proposed to overcome the challenge of Fermi level pinning and achieve good contacts.

3.1 Metal- 3D semiconductor interface

In general, the conditions for ideal metal semiconductor contacts are: first, the metal and semiconductor are in intimate contact on atomic scale with no interlayer in between; second, there is no interdiffusion or intermixing of metal and semiconductor; third, no impurities or surface charges are present at the interface.

The energy band diagram of a separated metal with work function of $q\Phi_m$ and a semiconductor with electron affinity of $q\chi_s$ is shown in **Figure 3.1a**. The work function of the metal in **Figure 3.1a** is slightly below the conduction band energy of the semiconductor. When the metal comes into intimate contact with the semiconductor (energy band diagram shown in **Figure 3.1b**), electrons transfer from the metal to the semiconductor due to higher energy level of the work function compared to Fermi level of the semiconductor. Then, the electrons are accumulated at the interface and diffuse to bulk semiconductor region. The accumulated electrons create a built-in potential that facilitates electron drift from semiconductor to metal. Eventually, the current due to diffusion equals the current from drift and thermal equilibrium is established through semiconductor band bending at the metal-semiconductor interface, resulting in the energy band diagram shown in **Figure 3.1b**. The barrier height energy required for electron injection from the metal to semiconductor is $q\Phi_{b,n}$, as labeled in **Figure 3.1b**. The Schottky barrier height for electrons can be increased by increasing the work function of the contact metal. High work function metals can suppress electron injection into the semiconducting while facilitating hole injection. As shown in **Figure 3.1c**, when a high work function metal forms an intimate contact with a semiconductor, the electrons from bulk semiconductor diffuse into metal and the built-in potential that arises from this cause electrons

to drift from interface to bulk of the semiconductor. The thermal equilibrium is formed with energy bands of the semiconductor bending upwards. The hole Schottky barrier height in **Figure 3.1c** is the difference between the valance band (E_V) energy of the semiconductor and the metal work function energy.

The ideal Schottky barrier heights (the energy required for injection from metal into the semiconductor) for electrons ($q\Phi_{b,n}$) and holes ($q\Phi_{b,p}$) is given by:

$$q\Phi_{b,n} = q\Phi_{m,low} - q\chi_s$$

$$q\Phi_{b,p} = E_g - (q\Phi_{m,high} - q\chi_s)$$

Where q is the charge of electron or hole, χ_s is the electron affinity of the semiconductor, Φ_m is work function of the metal contact, and E_g is bandgap energy of the semiconductor. The barrier height depends on the difference between the metal work function and the semiconductor electron affinity, which makes it possible to inject either electrons or holes into the semiconductor by tuning the work function of the metal contact.

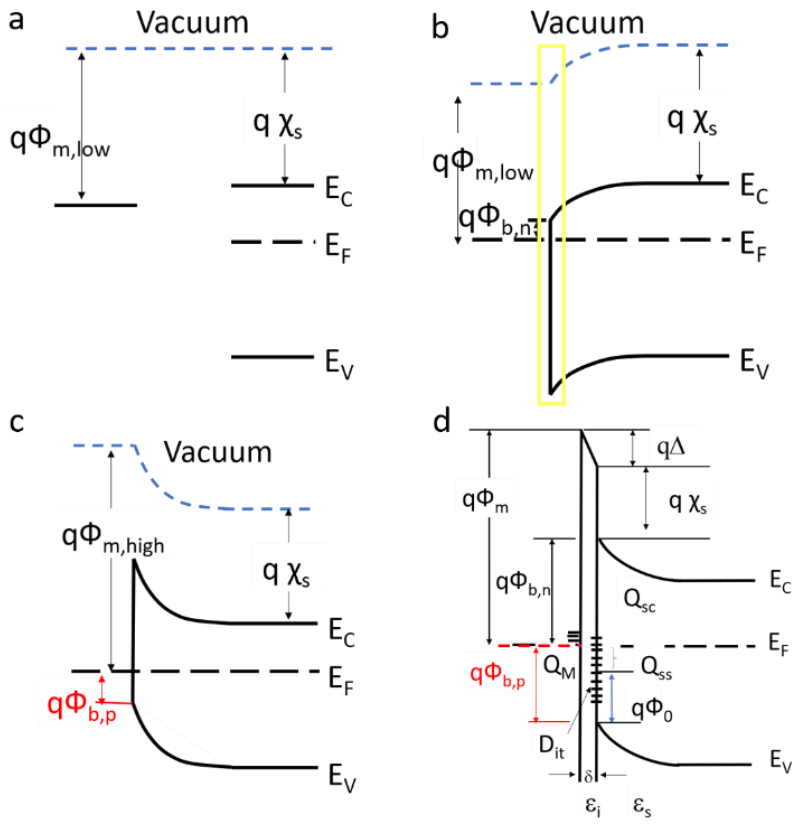


Figure 3.1 a, Energy band diagram of a metal with work function of $\Phi_{m,low}$ and semiconductor with electron affinity energy of $q\chi_S$ before contact. **b,** Energy band diagram for metal-semiconductor junction with low interface defects under thermal equilibrium. **c,** Similarly, when a metal with high work function $\Phi_{m,high}$ is brought into contact with the semiconductor, holes start to diffuse to the semiconductor side so that semiconductor bands bend upward to achieve thermal equilibrium. The Schottky barrier for holes in this case is $q\Phi_{b,p}$. **d,** The metal-semiconductor with high defect density of states at the interface is shown. Interface states energy level is labelled as $q\Phi_0$ above the valence band. This level is referred to as the neutral level above which the states are acceptor type (neutral when empty) and below which the states are of donor type (neutral when filled). In this case, when the metal forms an intimate contact with the semiconductor, a thin interfacial layer (d) is formed between the metal and semiconductor with a potential difference of Δ. The surface charge density Q_M in the metal side is equal to the interface charge traps Q_{SS} plus space charge density Q_{SC}. The energy level is pinned due to trap states and is not influenced by the metal work function, as indicated by black and red dashed lines at the interface. E_C = Energy level of conduction band of semiconductor, E_V = Energy level of valence band of semiconductor, E_F = Energy of Fermi level, Φ_m = metal work function, Φ_b = Schottky barrier height, $\Phi_{b,n}$ = electron Schottky barrier height, $\Phi_{b,p}$ = hole Schottky barrier height, Φ_0 = neutral level of interface states, χ_S = electron affinity of semiconductor, δ = thickness of interfacial layer, Q_{SC} = space charge density on semiconductor, Q_{SS} = interface trap charge density, Q_M = surface charge density on metal, D_{it} = interface trap density, ε_i = permittivity of interfacial layer, ε_s = permittivity of semiconductor, q = charge. E_C, E_V, E_F, $q\Phi_m$, $q\Phi_b$, $q\Phi_0$, $q\chi_S$ all have unit of eV. Q_{SC}, Q_{SS}, Q_M all have unit of C-cm^{-2}. D_{it} has unit of states-cm^{-2}-eV^{-1}.

Fermi level pinning

In practice, the Schottky barrier is independent of the metal work function for most semiconductors[79,80]. This is because there is a distribution of mid-gap states at the metal semiconductor interfaces due to the presence of defects (as illustrated in **Figure 3.1d**). These interface defects pin the Fermi level at their energy level and therefore the barrier height is determined by the mid-gape states rather than the work function of the metals. The energy level of interface states can be represented as $q\Phi_0$ above the valence band energy, E_V. Above this neutral energy level, states are acceptor type (neutral when empty) and below it the states are of donor type (neutral when filled). If the density of states near $q\Phi_0$ is large, then addition or depletion of carriers in the semiconductor cannot alter the Fermi level position at the surface

without large changes in surface charges. The degree of Fermi level pinning can be estimated by the pinning factor, S, that varies from 0 to 1.

The pinning factor can be derived from the interface-trap charge density that is given by $Q_{SS} = -qD_{it}(E_g - q\Phi_0 - q\Phi_b)$, where D_{it} is the interface trap density. The space charge that forms in the depletion region at the semiconductor/metal interface is given by $Q_{SC} = \sqrt{2q\varepsilon_s N_D(\Phi_b - \Phi_n - \frac{kT}{q})}$, where the ε_s is the dielectric of the semiconductor, N_D is the semiconductor doping concentration, $q\Phi_n$ is the energy from the Fermi level to the conduction band energy. The total equivalent surface charge density at the semiconductor surface is given by $Q_{SS} + Q_{SC}$, which develop the equal and opposite charge at the metal interface as shown in **Figure 3.1d**. The potential difference across the interfacial layer (thickness of δ) is obtained by applying Gauss' law: $\Delta = \frac{\delta Q_M}{\varepsilon_i}$ where ε_i is the dielectric of the interfacial layer. The potential drop across the interface layer can also be represented as (seen from the energy band diagram):

$$\Delta = \Phi_m - (\Phi_b + \chi_S)$$

Replacing the expressions for Q_m with those for Q_{SS} and Q_{SC}, the expression can be rewritten as:

$$\Phi_m - \left(\Phi_b + \chi_S\right) = \sqrt{\frac{2q\varepsilon_s N_D \delta^2}{\varepsilon_i^2}\left(\Phi_b - \Phi_n - \frac{kT}{q}\right)} - \frac{qD_{it}\delta}{\varepsilon_i}(E_g - q\Phi_0 - q\Phi_b)$$

The square-root term in the above equation is small [$\frac{2q\varepsilon_s N_D \delta^2}{\varepsilon_i^2}$ is around 0.036 V for $N_D = 10^{18}\text{cm}^{-3}$, $\varepsilon_s = \varepsilon_i = \varepsilon_0, \delta = 1$ nm] and therefore can be neglected to obtain:

$$\Phi_b = S(\Phi_m - \chi_S) + (1 - S)(\frac{E_g}{q} - \Phi_0), \text{ where } S = \frac{\varepsilon_i}{\varepsilon_i + q^2 D_{it}\delta}$$

From this, it can be seen that when the defect density of states at the interface is large ($D_{it} \to \infty$), then $S \to 0$, so that:

$$q\Phi_b = E_g - q\Phi_0$$

In this case, the Fermi level at the interface is pinned by the interface states and the barrier height is independent of the metal work function.

When the interface has low density of defect states ($D_{it} \to 0$), then $S \to 1$, and

$$q\Phi_b = q(\Phi_m - \chi_S)$$

The pinning factor S can be extracted by plotting the Schottky barrier energy versus the metal work function with S = 1 for an ideal metal/semiconductor interface. The S factor is generally far smaller than unity for semiconductors and the Schottky-Mott limit (S = 1) is rarely achieved. S is typically around 0.27 for silicon, 0.07 for GaAs and 0.02 for Ge[81,82]. The interface defect states can be calculated by $D_{it} = \frac{(1-S)\varepsilon_i}{Sq^2\delta}$. With this equation, the interface defects for different TMDs are calculated and summarized in Table 1. It can be seen that the experimentally obtained interface defects states for TMDs are higher than 3D semiconductors. In the following paragraph, I will discuss Fermi level pinning in 2D semiconductors.

Table 1 Summary of Fermi level pinning factors and interface states for different semiconductors

Semiconductor	Pinning factor S	Interface states (10^{13}/eVcm^2)	$q\Phi_0$ (eV)	ref
Si	0.27	2.7	0.3	[69]
GaAs	0.07	12.5	0.53	[69]
Ge	0.02	50.0	0.08	[68]
Multilayer MoS_2	0.15	21.2	1.1	[83]
Monolayer MoS_2	0.11	26.8	1.6	[83]
Multilayer $MoTe_2$	0.06	86.5	0.5	[84]
Monolayer $MoTe_2$	0.07	66.0	0.22	[83]
The interface states for TMDs were calculated by assuming δ = 1nm and the dielectric constant of the TMDs were taken from ref[83].				

3.2 Metal-2D semiconductor interface

For atomically thin semiconductors, it is challenging to dope the semiconductor without introducing large amount of defect states. Various strategies such as charge transfer doping[72–74], interfacial dipole formation doping[88,89], substitutional doping[90,91], and fixed charge layer doping[92,93] have been investigated. However, the doped samples generally exhibit low uniformity and stability, and devices are difficult to turn off[94]. More importantly, the interface

depletion width is weakly dependent on the carrier concentration in 2D semiconductors – making it difficult to achieve ohmic contacts through tunneling. Also, since the physical thickness of the semiconductor is much shorter than the depletion width, the metal-semiconductor interface equilibrium may not apply for 2D semiconductors. The energy band diagram of the metal-2D semiconductor is represented in **Figure 3.2**. The ideal (no interface density of states) low work function metal on 2D semiconductor contact is shown in **Figure 3.2a**. The band diagram in **Figure 3.2a** is simply an expansion of the very thin region (indicated by the yellow box in **Figure 3.1b**) of the bulk semiconductor junction. The Schottky barrier energy in this case is the difference between the metal work function energy and the conduction band energy of the 2D semiconductor. Similarly, the Schottky barrier energy for holes for a

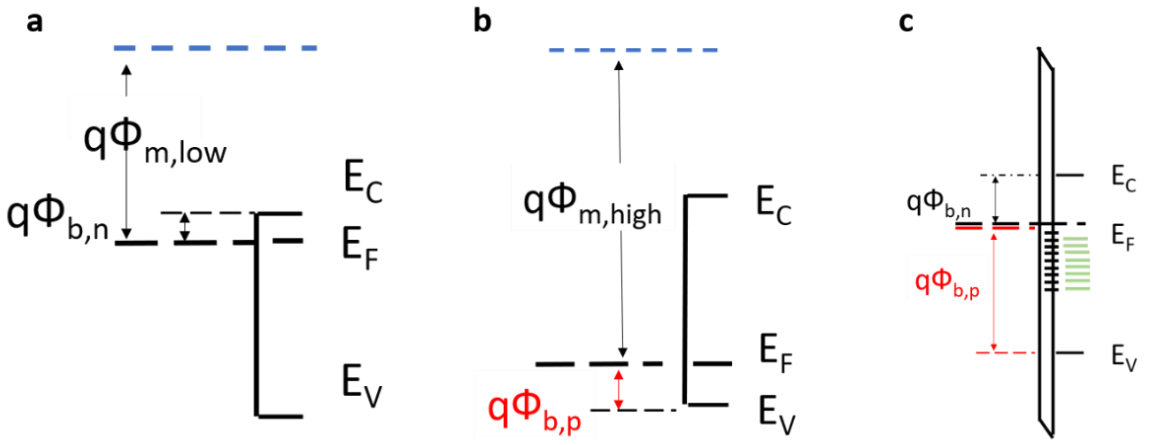


Figure 3.2 a, Energy band diagram for metal-2D semiconductor interface under thermal equilibrium. The atomically thin nature of the semiconductor means that the metal-2D semiconductor junction is essentially the yellow rectangle region from Figure 3.1b. Unlike 3D semiconductor, the 2D Fermi level is strongly influenced by the metal contact due to charge transfer. The electron Schottky barrier height in the metal-2D semiconductor junction is the energy difference between metal work function and conduction band energy of the semiconductor. **b,** Energy band diagram for high work function metal-2D semiconductor contact under thermal equilibrium. Similar to 3D semiconductor, low hole Schottky barrier can be achieved with high work function metal contact if the interface has low defect density. **c,** Energy band diagram for metal-2D semiconductor under thermal equilibrium with high interface defect density. Similar to the 3D case, the Fermi level is pinned at fixed energy due to trap states at the interface. Furthermore, the semiconductor/dielectric interface (green lines) is an additional source for trap states in the semiconductor bandgap that can influence the doping in the semiconductor.

high work function metal contacted to 2D semiconductor is shown in **Figure 3.2b**. For the non-ideal case, the Schottky barrier height is independent of the metal work function as in the 3D semiconductors case and the band diagram is essentially the interface region of **Figure 3.1d** as shown in **Figure 3.2c**.

Another important parameter that influences the metal-semiconductor junction is the substrate on which the 2D semiconductors are supported. The atomically thin nature of 2D semiconductors means that any surface charges on the supporting substrates can create interface states (green lines in **Figure 3.2c**) and affect the carrier injection. Surface states from substrates also dope the 2D semiconductor. Doping from most oxide substrates is N-type for

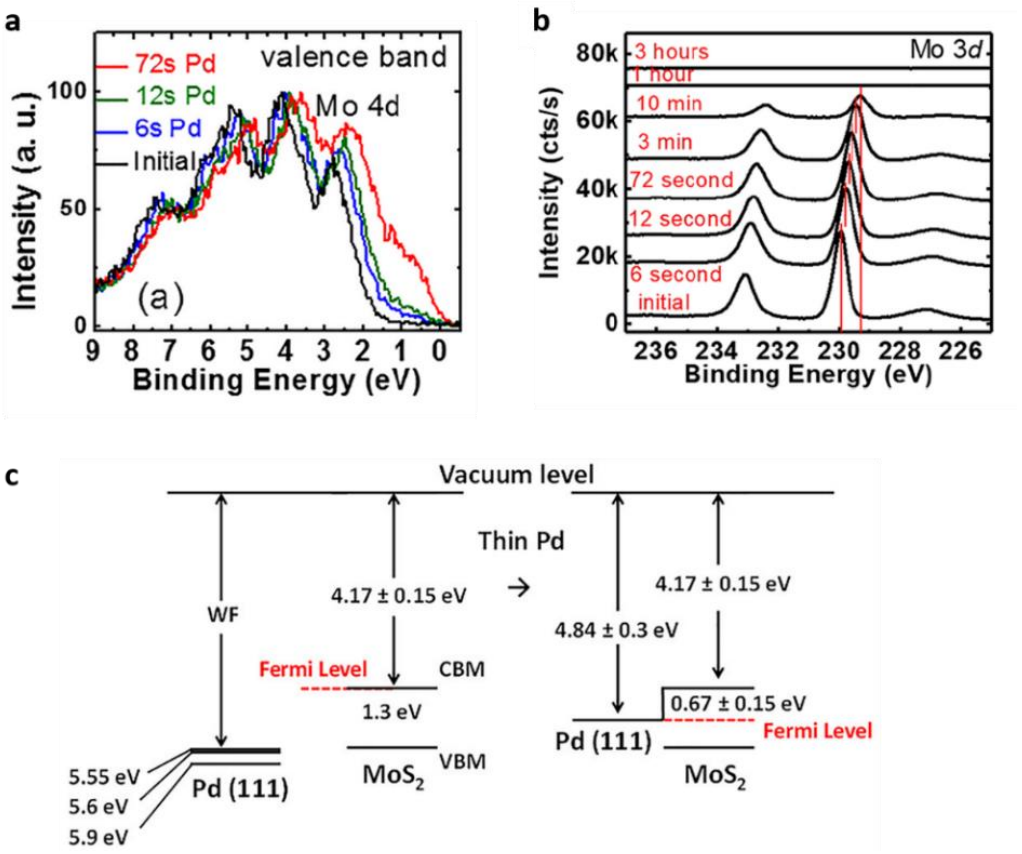


Figure 3.3 a, Valence band structure of pristine MoS_2 for the initial surface after 6, 12, and 72 seconds measured by XPS. The low binding energy region indicates how close the Fermi level is to the valance band edge. The spectra indicate that the Fermi level of MoS_2 moves towards the valance band edge after Pd deposition. **b,** Core level XPS spectra of Mo 3*d* for the prestine MoS_2 surface after 6 s, 12 s, 72 s, 3 min, 10 min, 1 h, and 3 h of Pd deposition. The right shift of the peak reveal hole doping of MoS_2 after Pd deposition. **c,** Energy band diagram of the Pd and MoS_2 not in contact and after Pd deposition. The images are reproduced from Ref[95].

2D TMD semiconductors and therefore P-type devices have been difficult achieve, even with ultra-clean vdW contacts. The influence of substrates on the FET performance will be discussed in Chapter 6.

It is difficult to experimentally probe the electronic structure of thin TMDs under metal contacts. Wallace's group probed the valence band edge of few layered MoS_2 before and after 5nm Pd deposition using X-ray photoelectron spectroscopy (XPS)[94]. The valence band and XPS spectra of MoS_2 before and after Pd deposition are shown in **Figure 3.3a** and **3.3b**. From **Figure 3.3a**, it can be seen that the valence band edge shifts to lower binding energies with longer Pd deposition time. From **Figure 3.3b**, it can be seen that the Mo 3*d* spectra blue shift with thicker Pd layers. Based on these results, the authors conclude that the Fermi level position shifts from being near the conduction band of MoS_2 to middle of the bandgap after Pd deposition, as shown in **Figure 3.3c**. The Pd work function is obtained by assuming thermal equilibrium at the metal-semiconductor interface. However, large change in Pd work function before and after deposition on MoS_2 (5.6 eV before and 4.8 eV after) is observed.

In conclusion, doping and position of Fermi level are strongly affected by deposition of metal contacts on few layered TMDs. Also, the work function of the metal deposited on TMDs is typically much lower than the bulk value – as measured by XPS and this could be one limitation for achieving P-type FETs with high work function contacts.

3.3 Origins of fermi level pinning for 2D semiconductors

Fermi level pinning of electrical contacts on 2D semiconductors mainly originates from defect related mechanisms illustrated in **Figure 3.4**. The defects at the metal-2D TMD semiconductor interface arise from: **a**, gap states due to chemical reactions; **b**, vacancies in the 2D semiconductor; **c**, interstitials introduced during contact fabrication; **d**, strain caused by metal-semiconductor lattice mismatch; **e**, interface dipoles formed by charge redistribution that shifts the potential levels from their original positions.

Chemical reactions at the metal-2D TMD interface: An example of the type of chemical reactions that can occur between a metal and 2D TMD semiconductors is best illustrated by the deposition of titanium contacts[96] shown in **Figure 3.4a**. Substantial distortion of the lattice and penetration of Ti into MoS_2 can be observed in cross-section scanning transmission electron microscopy (STEM) with electron energy loss spectroscopy (EELS). The Ti metal signal can be detected sown to fifth layer of MoS_2 due to its high affinity for sulfur. Reacted products such as Ti_xS_y and metallic Mo states can be also detected by X-ray photoelectron

spectroscopy (XPS)[97]. This chemical reaction/new bond formation also happens with other metals deposited on 2D TMDs. Wallace's group performed systematic XPS characterisation of the interface chemistry between different metals and TMDs (Sulfide, Selenide, Telluride). The results showed that metals such as Ti, Ir, Cr, and Sc all react with MoS_2 whereas Ir, Cr, and Sc react with $MoSe_2$ and Au, Ir, Cr and Sc react with $MoTe_2$[98,99]. More reactive metals such as Cr and Sc reduce the TMDs near the interface, causing the metal-semiconductor band alignments to deviate from the Schottky-Mott rule. Further study of Ni and Ag on bilayer MoS_2 show that Ni reduces MoS_2 to form NiS_2 while Ag forms clean van der Waals contact with MoS_2[100]. Mohney's group systematically studied the reactivity at metal/WS_2 interface by Raman spectroscopy[101,102]. The results showed that Ti and Al aggressively react with monolayer WS_2 while Cu, Pd and Au are less reactive with WS_2. Once the reaction occurs, annealing the device – a process typically used to improve the metal/semiconductor interface – further exacerbates the interfacial reactions in 2D TMDs and the device performance deteriorates[103,104]. Smyth *et al.* investigated Pd contact for WSe_2 who observed increased $PdSe_X$ intermetallic phase after annealing[105]. As a result, the FET performance changes from N-type to P-type. A variety of approaches have been proposed to suppress the interface chemical reaction to achieve Fermi level pinning free devices, I will introduce these strategies in Section 3.3.

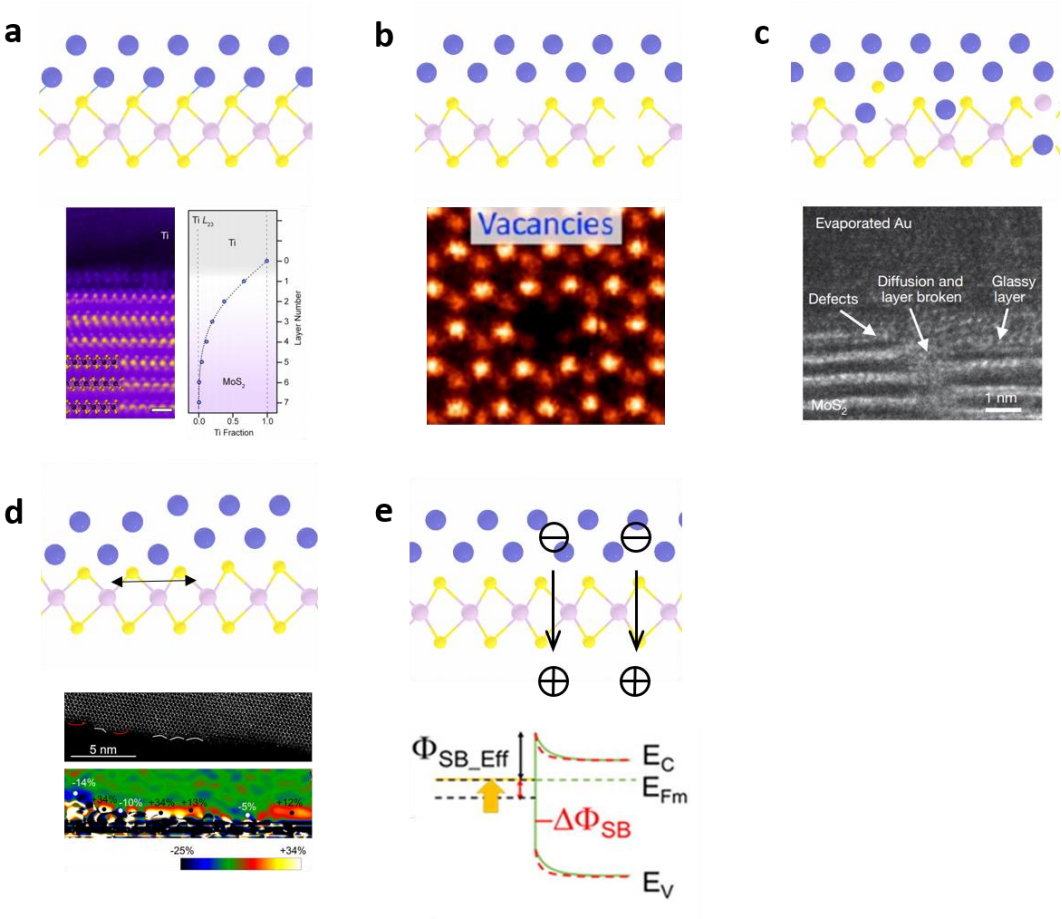


Figure 3.4 Schematic of mechanisms responsible for Fermi level pinning in metal-2D TMD semiconductor junctions. **a,** Schematic shows chemical reaction between metal atoms and chalcogens at the interface that leads to defect states[96]. A high resolution TEM image along with EELS chemical map of titanium fraction with a the number of layers is shown below. In the TEM image, strain and distortion of MoS_2 under Ti contact can be seen. The EELS map shows that Ti diffuses down to the fifth layer of MoS_2. **b,** Defects such as vacancies in 2D TMD semiconductors. In the schematic, both S and Mo vacancies are shown. In the image below, atomic resolution scanning TEM image of Mo vacancy is shown[78]. **c,** Schematic of damage or diffusion of metal into semiconductors caused by metal deposition on ultra-thin TMD semiconductors. High resolution TEM image of damage in multi-layered MoS_2[124]. **d,** The schematic indicates how local strain in TMDs can be induced by deposition of metal contacts. The interactions between the metal and chalcogen atoms in TMDs can lead to local distortions in bond lengths that give rise to local compressive/tensile strains indicated by the double-sided arrow. Below the schematic, STEM image of a MoS_2 edge (top) and the corresponding strain mapping image are shown. The concave edges of MoS_2 (white arcs in the image) exhibit compressive strain of ~ 34 % while the convex regions (red arcs) present tensile strain of ~14%[139]. The yellow regions in the strain map are of compressive strain and the blue regions are of tensile strain. **e,** Interface dipole between metal and semiconductor. The schematic shows fixed (positive) charges in SiO_2 cause dipoles across the metal-semiconductor interface that changes the Schottky barrier height as indicated in the energy band diagram below[144]. The symbols in the band diagram are: E_C = Energy level of conduction band of semiconductor, E_V = Energy level of valence band of semiconductor, E_{Fm} = Fermi level of semiconductor. The electron Schottky barrier height is labeled as Φ_{SB_Eff} in the band diagram. The decreases in the barrier height due to interface dipole is Φ_{SB}.

Defects (e.g. vacancies) on 2D TMDs: The deposition of metal on a semiconductor can also lead to Fermi level pinning due to defects on the surface of the semiconductor. Intrinsic defects such as vacancies, anti-site substitutions are commonly observed in TMDs by STEM (**Figure 3.4b**) or scanning tunneling microscopy (STM) due to the low defect formation energies (2.12 eV for sulfur vacancy and 1.1 eV if Mo vacancy is already present)[78]. Jeong *et al.* reported that atomic sulfur vacancies introduce defect states that are located 0.05 - 0.4 eV below the conduction band, which is consistent with Fermi level pinning energies in MoS_2 FET[83,106]. Efforts have been made to synthesize low defect TMDs to achieve better electronic and optical properties by self-flux growth[107]. Passivation of the TMDs has also been studied to remove the defects states in MoS_2 by deposition of monolayer organic titanyl phthalocyanine[108]. Density

functional theory and scanning tunneling microscopy results have shown that the organic/inorganic van der Waals interface induced suppression of defect states. Nan *et al.* observed strong PL enhancement of MoS_2 by passivate the defects with oxygen bonding[109]. Extrinsic factors such as absorbates, substrate surface roughness, strain, oxidization caused degradation also introduce defect states that locally tune the electronic structure of TMDs[110]. The most common way to reduce the interference caused by extrinsic factors is to sandwich the TMDs between insulating h-BN layers[111].

Defects induced by metal deposition: Another source of defects at the metal-semiconductor contact interface is during the metal deposition. Studies have shown that metal deposition can substantially modify semiconductors such as GaAs and organic molecules[112,113]. Substantial work has been done to minimize damage to organic molecules during fabrication of contacts. This work is relevant for making defect free contacts on atomically thin semiconductors, so we briefly review it here. It has been shown that reducing the kinetic energy of the metal atoms by introducing an inert gas in the vacuum chamber during evaporation as well as cooling the substrates can minimize damage to organic molecules[114,115]. Viscous liquid that is formed in eutectic mixture of gallium and indium (EGaIn) has been used successfully to make gentle contacts on molecules and achieve good rectification characteristics, confirming low penetration or reaction at the interface[116–118].

For device applications, metal deposition using evaporation methods (thermal or electron-beam) that are compatible with integrated circuits manufacturing are required. Bonifas *et al* reported a surface-diffusion-mediated method in which the metal is deposited remotely (tens of nm away) and then allowed to diffuse onto the organic semiconductor to realise soft contacts[119], which avoided heat irradiation and direct kinetic energy transfer from metal vapor atoms. This method requires precise control of the metal deposition region to the molecular that leads to not direct metal contact but reachable with atom diffusion. 2D semiconductors also suffer from damage from metal deposition[120–123]. The penetration of metal atoms and kinetic damage to atomically thin semiconductors (such as MoS_2 in **Figure 3.4c**[124]) can be reduced by decreasing the temperature due to radiation during deposition[83,125]. Although dry transferred metal contacts have been widely studied and applied to achieve clean interfaces for TMD based transistors[125–128] and photovoltaics[129], this method is not applicable for large scale fabrication, especially short channel FETs. For evaporated metal contacts, it has been shown that the diffusion of Au atoms is much higher than Cu and Ag on porphyrin monolayers. The lower penetration of Cu and Ag could partially be due to the lower heat of vaporization of these

metals compared to Au under the same vacuum conditions[130]. This along with the work on EGaIn has led to new strategies for achieving high quality contacts on atomically thin semiconductors. In particular, very thin layers of soft and low melting temperature metals such as indium can be gently deposited on the 2D semiconductor without causing any damage at the interface (see Chapter 5). These metals can then be capped with more refractory metals such as Au or Pd for protection. The work function of indium is very close to conduction band of MoS_2, making it an ideal contact for electron transfer. Chou *et al.* also achieved high performance FET based on monolayer MoS_2 with Sn contacts[131]. Recent work on bismuth as good contact metal is also consistent with this strategy[132].

Strain at the interface: It is reasonable to believe that the metal-semiconductor interface could have some strain due to lattice mismatch that could lead to electronic structure change of the TMDs. So, I will give a brief introduction of how strain could affect the electronic structure of 2D TMDs. Desai *et al.* experimentally demonstrated indirect to direct bandgap transition in multilayer WSe_2 under 2 % uniaxial tensile strain[133]. Lee's group revealed that $MoTe_2$ undergoes room temperature phase transition – from semiconductor 2H to metallic 1T phase – due to 0.2 % tensile strain applied by an atomic force microscopy tip[134]. The effect of strain on MoS_2-WSe_2 heterojunctions on electronic structure has also been investigated using scanning tunneling spectroscopy[135]. It was found that the valance band maximum (VBM) of MoS_2 is 0.45 eV below VBM of WSe_2 without strain. Due to the strain, the VBM is pushed upwards significantly, causing VBM of MoS_2 to be 0.65 eV higher than VBM of WSe_2. This interface strain changes the bandgap of MoS_2 as well as the band alignment between WSe_2 and MoS_2. Thus, it is reasonable that the presence of strain at the metal/2D semiconductor interface is also likely to influence the local electronic structure of the semiconductor and therefore the Schottky barrier height. However, experimental work on strain induced by metal deposition on 2D semiconductors has been limited. Gong *et al.* studied the effect on electronic properties of monolayer MoS_2 due to deposition of few nanometers of metal (Pd, Au, Ag) by Raman Spectroscopy[136]. The in-plane phonon E_{2g} mode of MoS_2 covered by 2 nm of Pd showed ~1.86 cm^{-1} red shift due to small lattice mismatch (0.5 %). In contrast, for Au and Ag (5.4 % and 5.7 % lattice mismatch), a clear splitting of the E_{2g} peak was observed (3.8 cm^{-1} for Au and 6.38cm^{-1} for Ag). From the Raman data, the authors conclude that strain in monolayer MoS_2 caused by Au and Ag deposition is ~0.84 % and ~1.0 %, respectively. Similar results have also been observed by Sun[137] and Golasa[138] *et al*. However, Raman spectroscopy only provides an indirect quantification of strain assuming the peak shift is solely caused by strain and not by

other effects such as increase in defect density or doping of the interface that can also cause Raman peak shifts[138]. TEM and geometrical-phase analysis (GPA) provide more direct quantification of the strain. However, to the best of my knowledge, there is no reported results on cross-section TEM with GPA mapping showing the strain at the metal-2D TMD interface. The schematic in **Figure 3.4d** shows possible local in-plane strain due to metal on top of a TMD. The interactions between the metal and chalcogen atoms can lead to tensile/compressive strain as indicated by the double-sided arrow in the schematic. STEM image of a MoS_2 edge and the corresponding strain mapping as an example of strain analysis are shown below the schematic[139]. The concave edge of MoS_2 in the STEM image (indicate by the white arcs) exhibit compressive strain up to 34 % while the convex regions (indicate by the red arcs) present a tensile strain up to 14 %. More direct strain mapping of the metal-semiconductor interface and its influence on electronic structure using electron energy loss spectroscopy from cross-sectional STEM is needed.

Interface dipoles: Last mechanism that could lead to Fermi level pinning is the formation of interface dipoles by electron density redistribution at the metal-semiconductor (M-S) junction that mainly originates from the energy level shift induced by charge transfer[140], the pushback effect[141], and/or the energy level broadening effect[142]. That is, when the metal is contacted with a 2D semiconductor, the wave functions from the two materials overlap and rearrangement of the electron density occurs. For example, in Pt/MoS_2 junctions, electron accumulation on Pt side of the interface occurs because the wave function of Pt is more extended and deformable than that of MoS_2 so that electrons are pushed back into Pt by repulsion from electron clouds of MoS_2. As a result, the metal work function of Pt is lowered when put in contact with MoS_2. The charge redistribution of Pd on MoS_2 surface has been detected by XPS – showing strong band bending effect and a decrease in metal work function from 5.55 eV to 4.84 eV upon deposition on MoS_2[95]. Interface dipoles have been engineered using self-assembled monolayers to reduce the Schottky barrier height[143]. Work by Joo *et al.* showed that the Au/MoS_2/BN heterostructure gives rise to dipole moments at the metal-semiconductor interface (as illustrated in **Figure 3.4e**) due to fixed charges in SiO_2 substrate that reduce the metal work function and Schottky barrier height[144].

3.4 State-of-the-art approaches for lower contact resistance

Various strategies have been investigated to lower the contact resistance for devices based on 2D semiconductors such as selecting different metal contact, Fermi level depinning by inserting

an insulating layer such as h-BN between metal and the semiconductor, doping, phase engineering, and using metallic 2D materials as contacts. In this section, I will review the state-of-the-art results for making good electrical contacts to 2D TMDs.

3.4.1 Contact metals selection

As discussed in section 3.1, the metal–semiconductor junctions are characterized by Schottky barrier Height (SBH), the value of which be in principle predicted by the Schottky– Mott rule on the basis of energy band alignment. Low Schottky barrier height leads to non-rectifying (ohmic) characteristic. In general, two approaches could be used to minimize the Schottky barrier: (1) using highly doped contact regions to reduce the Schottky barrier width; or (2) selecting metals with appropriate work functions matching with semiconductor band edges to lower the barrier for carrier injection. In CMOS devices, the first method is widely used, where the source and drain contacts are degenerately doped (n++ or p++) using ion implementation[7]. However, for 2D semiconductors, using ion implantation to heavily dope the materials is very challenging because they are atomically thin and easily damaged by high energies of the ions during implantation. Therefore, P-and N-type devices based on 2D TMD semiconductors rely on selecting high and low, respectively, work function metal contacts.

A variety of metals such as Sc, Ag, Sn, Al, Ti, Ni, Cu, Au, Co, W, Pd, and Pt have been used as contacts to 2D TMD materials[9,124,131,145–148]. The Fermi level pinning factor can be obtained by plotting the SBH versus the metal work function and extracting the slope, as discussed in Section 3.1. Typical pinning factor for metal contacts on MoS_2 is around 0.1, as shown in **Figure 3.5a**[124]. The low pinning factor (close to 0) indicates strong Fermi level pinning at the metal-semiconductor interface, meaning that the Schottky barrier height cannot be tuned by varying the work function of the metal. In contrast, studies have shown that creation of van der Waals contacts via metal transfer can provide clean interfaces without damaging the underlying 2D TMD semiconductor. In Duan's work[124], van der Waals metal–semiconductor junctions were achieved when metal thin films were transferred onto two-dimensional semiconductors to achieve an interface that is essentially free from chemical disorder and Fermi-level pinning. Using this technique, they were able to vary the SBH by using metals with different work functions to realise an ideal Schottky-Mott, as reflected by the S factor being close to 1 (0.96) in **Figure 3.5b**[124].

The chemical reactions between contact metal and the 2D TMDs were discussed in Section 3.2. The reactions usually create disorder under the contacts and lead to Fermi level pinning at

the metal- semiconductor interface, which is detrimental for FET performance. Thus, when choosing a metal contact for a 2D semiconductor, the first step is to avoid highly reactive metals. In general, if the enthalpy of metal sulfide formation is negative, then the sulfur will react with the deposited contact metal. Second, a low vaporization temperature metal is preferred as the kinetic energy of evaporated atoms is low and therefore damage to 2D TMD semiconductors during the metal deposition process is minimized. Third, the work function of the metal should match the conduction band of the 2D TMD semiconductor for electron transport and the valence band for hole transport. Recent work has demonstrated degenerate doping of the 2D TMDs with bismuth metal contacts through charge transfer to achieved low contact resistance[132].

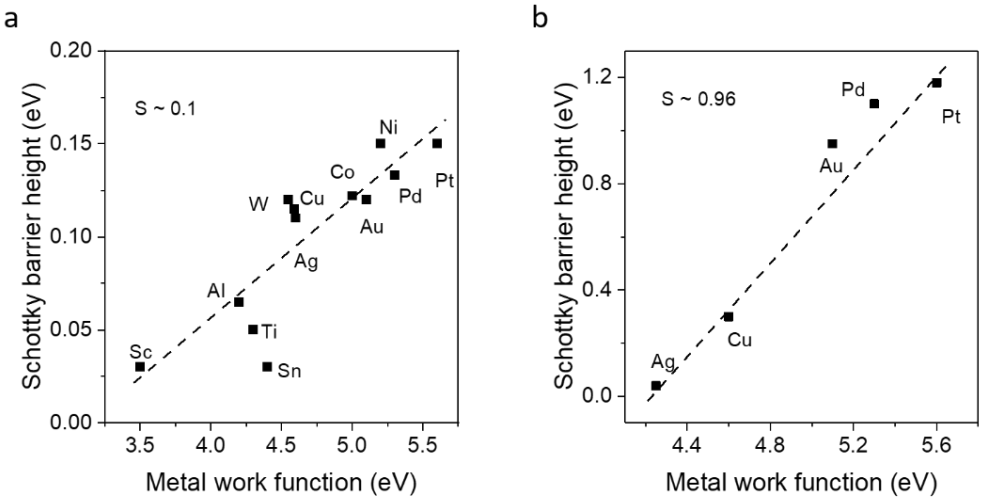


Figure 3.5 a, Schottky barrier height of MoS_2 FETs versus metal work function for different metal deposited by evaporation. **b,** Schottky barrier height of MoS_2 FETs versus metal work function for different metal contacts made by dry transfer process. These figures and the data are taken from Ref[9,124,131,145–148].

3.4.2 Unpinning the fermi level in 2D TMD FETs

Several different methods have been reported to unpin the Fermi level in 2D TMD devices. Kaushik *et al.* reported that insertion of TiO_2 between MoS_2 and contact metal can reduce the SBH by 0.3 eV[149], which decreases the contact resistance by 24 times. Similarly, the introduction of a Al_2O_3 thin layer also showed a decrease in contact resistance by approximately an one order of magnitude[150]. Wong's group also demonstrated good contacts using Ta_2O_5 as an effective tunnel barrier[151], as shown in **Figure 3.6a**. Contact resistance dropped two orders of magnitude when inserting 1.5 nm thick Ta_2O_5. However, as the Ta_2O_5

thickness is increased beyond 1.5 nm, but the resistance increases monotonically with thickness above 1.5 nm. Monolayer or bilayer h-BN have also been utilized as tunneling barrier for TMD contacts[152–154]. The device characteristic with h-BN exhibit better performance (higher mobility, current and absence of hysteresis) than metal-semiconductor contacts. Mleczko *et al.* reported high performance $MoTe_2$ FET by inserting monolayer h-BN between $MoTe_2$ and Sc metal contact[84] to prevent chemical reaction at the metal-semiconductor interface. The h-BN therefore acts has a buffer layer (see schematic in **Figure 3.6b**) that allows carrier injection while maintaining a clean metal-semiconductor interface as shown in the cross-sectional TEM image in **Figure 3.6b**.

TMD FETs with graphene as the contact layer have also been extensively studied because graphene is a semimetal nature with tunable Fermi level by electro-gating[155–157]. Compared to pristine metal–MoS_2 contact, insertion of a graphene layer between the metal and MoS_2 appears to eliminates the strain at the interface and overheating effects[136]. Leong *et al.* fabricated nickel-

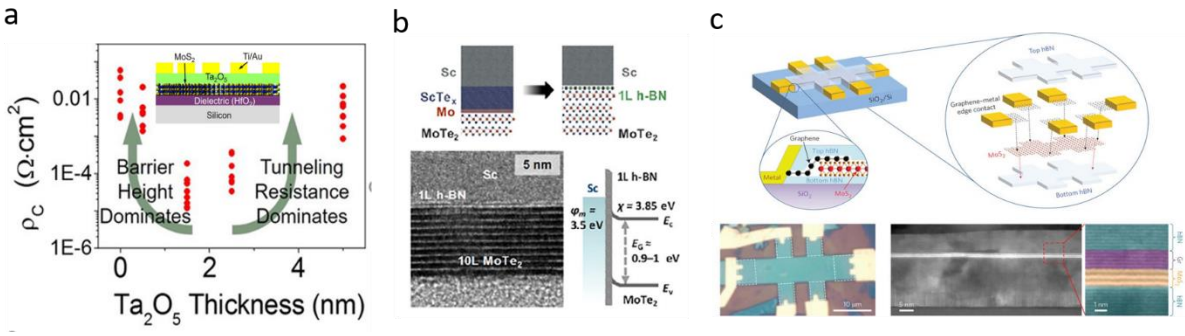


Figure 3.6 a, Specific contact resistivity as a function of Ta_2O_5 tunnel barrier thickness for MoS_2 FETs. The results show there is an optimal thickness of 1.5 nm below and above which the resistivity increases. Inset shows the schematic of the device. **b,** Schematic and cross-section TEM image of metal-semiconductor interface with 1L h-BN between. The schematic shows that in the absence of h-BN layer, there is chemical reaction between the Sc metal and Te atoms of $MoTe_2$. The presence of h-BN prevents such reactions. The TEM image confirms the absence of any reactions and shows good quality interface. The energy band diagram shows that the h-BN acts a tunnel barrier for injection of electrons. **c,** Schematic of MoS_2 FET with edge contacted graphene. The enlarged schematic shows the different device layers. The enlarged region at the contacts shows the configuration of the edge contacts. Optical microscope image of the device is shown along with cross-sectional low and high magnification images. Images are reproduced from Ref[79,106,146].

etched-graphene contacted devices through dry transfer process and yield two orders lower contact resistance compared to pure nickel contacts[136]. Liu *et al.* constructed a transparent contact to MoS_2 with zero contact barrier and linear output behavior at cryogenic temperatures (down to 1.9 K) for both monolayer and multilayer MoS_2[157]. Further optimization of the device configuration can be done by encapsulating the MoS_2 channel and the graphene electrodes between h-BN layers to reduce the interfacial charge scattering[111]. MoS_2 FET with edge graphene contacts encapsulated within h-BN is shown in **Figure 3.6c**, adopted from ref[111]. The device shows dramatic improvement with a record-high Hall mobility up to 34,000 $cm^2V^{-1}s^{-1}$ for six-layer MoS_2 below 5 K.

Farmanbar *et al.* have theoretically supported the experimental work on using 2D buffer layers for improving contacts by demonstrating a significant reduction in Schottky barrier height and an improvement in contact resistance through the insertion of various 2D layers[111]. They claimed that a 2D buffer layer such as graphene, h-BN, metallic NbS_2 or MoO_3 are potentially useful for achieving zero SBH for holes.

3.4.3 Doping

Ion-implantation is used to obtain N-or P-type doped semiconductors. However, this method is not appliable for 2D TMDs due to the damage caused by the process. Thus, various doping strategies such as surface charge transfer doping, interfacial dipole formation doping, and fixed charge layer doping have been studied for 2D TMDs.

Surface charge transfer doping mainly depends on the chemical potential of the 2D materials. Benzyl viologen (BV)[111], poly(vinyl-alcohol) (PVA)[158], polyethyleneimine (PEI)[85], potassium (K)[85], and Chloride (Cl)[159] have negative reduction potentials, which results in the donation of electrons to 2D materials to obtain n-doping. Yue *et al.* reported largely reduced contact resistance from 7 to 1.2 kΩ·μm by electron dope the contact region on MoS_2 with BV[111] as shown in **Figure 3.7a**. In contrast, tris(4-bromophenyl)ammoniumyl hexachloroantimonate ("Magic Blue")[86], gold chloride ($AuCl_3$)[87] and 2,3,5,6-tetrafluoro-7,7,8,8-tetracyanoquinodimethane (F4TCNQ)[160] dopants induce a p type doping in 2D materials due to their positive reduction potential. Fang et al also reported degenerate hole doping for WSe_2 with NO_2 chemisorption[161].

Fixed charge layer doping is commonly achieved by using non-stoichiometric high dielectric constant oxides such as TiO_X, HfO_X and Al_2O_X[92,162,163]. The doping can be achieved by encapsulating the 2D TMDs with the oxide thin film deposited by spin-coating or atomic

layer deposition process. For example, Rai *et al.* demonstrated record low contact resistance (180 Ω·μm) for few layered MoS_2 devices by encapsulating with non-stoichiometric amorphous TiO_X[92]. The doping arises from interfacial oxygen vacancies and provides an effective way to fabricate high performance TMD FETs. The doping level by non-stoichiometric HfO_X is further investigated by varying the O to Hf ratio[162]. The results indicate that higher oxygen vacancy concentration leads to higher electron doping of MoS_2 and lower contact resistance. More specifically, the doping level increased from 10^{11} cm^{-2} to 10^{13} cm^{-2} when O:Hf ratio was decreased from 2 to 1.5. The contact resistance of MoS_2 FET with different doping level from HfO_X is shown in **Figure 3.7b**. By tuning the O:Hf ratio, the contact resistance reduces by two orders from 1000 to 10 kΩ·μm.

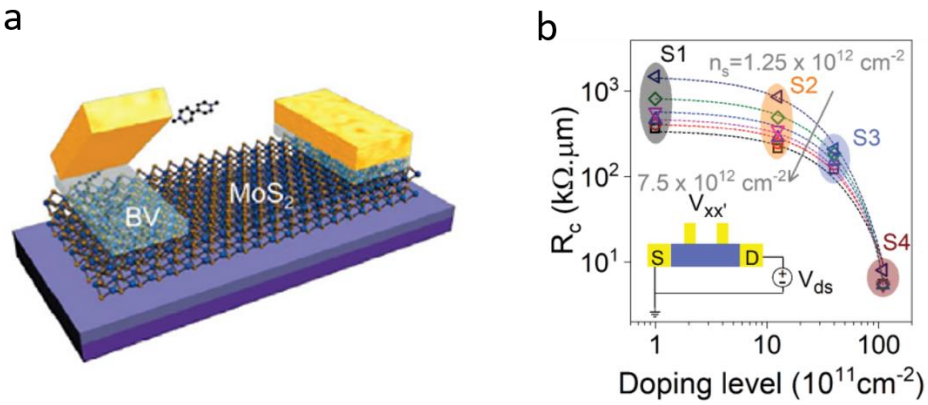


Figure 3.7 a, Schematic of MoS_2 FET device employing BV as interfacial doping later between the MoS_2 and metal contact[157]. **b,** Contact resistance of MoS_2 FET versus doping level of HfO_X on MoS_2. The doping level was varied by tuning the O:Hf ratio. S1, S2, S3, and S4 in the figure represent O:Hf ratios of 1.5, 1.75, 1.9 and 2, respectively. The images are reproduced from Ref[162,164].

3.4.4 Phase engineering

As discussed in previous section 2.1, the electronic structure of MoS_2 can be converted from 2H semiconductor phase to 1T metallic phase by chemical intercalation. The idea can be applied to do local phase transition to lower the contact resistance for TMD FETs. It has been demonstrated by Li intercalation[165,166], laser irradiation[167], electron irradiation[168] and argon plasma treatment[169] to locally treat the contact region TMDs.

The groundbreaking work on phase engineered lateral metallic 1T phase MoS_2 contacts to 2H phase MoS_2 semiconducting channel was reported by Kappera *et al.*[165,166]. The contact resistance of phase engineered contacts was found to be 0.22 kΩ·μm, as shown in **Figure 3.8a**.

This remains among the lowest value reported. In **Figure 3.8a**, the left inset shows an atomically sharp boundary between the 1T and 2H phases without defects and the inset on the right shows an electrostatic microscopy image of local phase transformation of a CVD grown MoS_2 monolayer. This approach was extended by Cho *et al.* using a laser to convert $MoTe_2$ from 2H semiconducting phase to the 1T' metallic phase[167], as shown in **Figure 3.8b**. They suggest that the phase transformation in $MoTe_2$ is triggered by Te vacancies induced by laser irradiation. The SBH of the $MoTe_2$ metal junction was reported to decrease from 200 meV to 10 meV after phase transformation, resulting in ohmic contacts The 2H to 1T phase transition in MoS_2 has also been induced by generation of S vacancies using electron beam[168] and Ar-plasma bombardment[169].

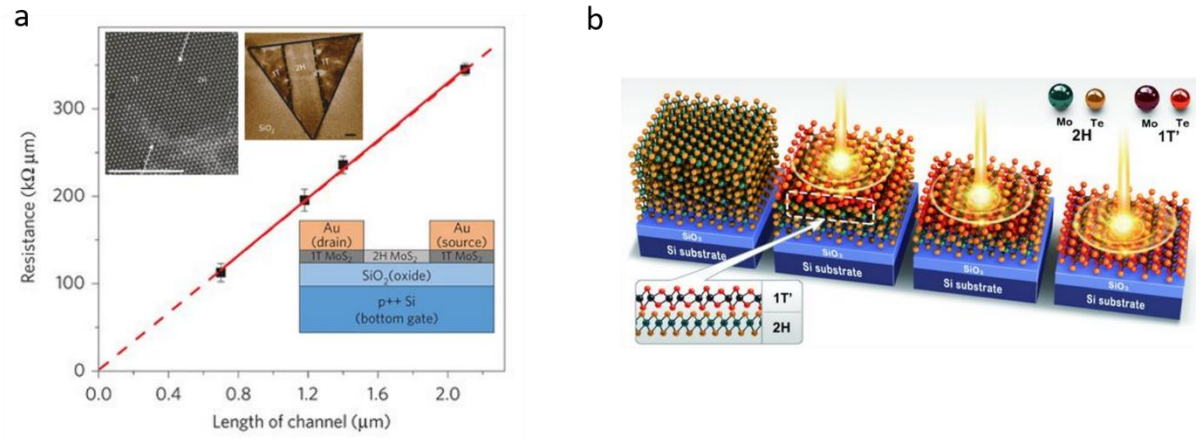


Figure 3.8 a, Transfer length method measurement for extracting contact resistance for phase engineered 1Tphase/2H phase/1T phase MoS_2 lateral junction. The extrapolation of the data using dashed line shows that the contact resistance is 220 Ω·μm. Lower inset shows the schematic of the FET device structure. Upper left is the atomic resolution TEM image of 1T and 2H phase boundary – showing that it is atomically sharp. **b,** Laser irradiation introduced thinning and phase transformation of $MoTe_2$. The images are reproduced from Ref[165–167].

3.4.5 Metallic TMD as contacts

Along with the phase engineered metallic contacts, there is interest in direct synthesis of metal-semiconductor lateral structures. Of the ~ 40 TMD compounds, the ones from Group 5 and 7 are metallic and these could be used to create lateral contacts to semiconducting TMDs during CVD growth. Epitaxial heterostructures between semiconducting 2H WSe_2 and metallic 1T' WTe_2, VSe_2 and $NbTe_2$ have all been experimentally demonstrated by two-step chemical vapor deposition method[170–172]. Compared to planar metal (Ti) contacts, the 1T' WTe_2 epitaxial vdW

contact possess Schottky barrier heights below 100 meV for both electron and hole injections[172]. Ambipolar WSe_2 FETs with better performance are achieved via 2H/1T' lateral heterojunction contacts, as shown in **Figure 3.9a**. Similarly, vdW $NbTe_2/WSe_2$ contacts also showed significant improvement in on-state currents and field-effect mobilities of FETs compared to FETs with Cr/Au contacts[170]. More recently, Li et al. reported precise control the nucleation location for growth of metallic TMD by laser patterning[173], producing a series of metal-semiconductor heterostructures. The optical image of a VSe_2/WSe_2 lateral heterostructure array and their FET characteristics are shown in **Figure 3.9b**. The results show that metallic VSe_2 contacts give two order of magnitude higher hole current than metal contacts for WSe_2 FETs.

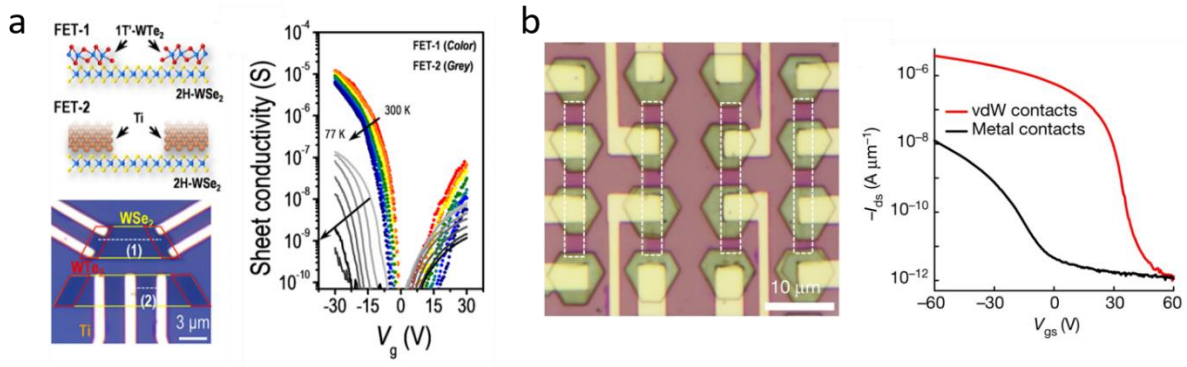


Figure 3.9 a, Illustration of the device scheme for vdW epitaxial metallic TMD (1T' WTe_2) grown on top of semiconducting 2H-WSe_2. FET-2 indicated the usual scheme in which the Ti metal is contacted directly to semiconducting 2D WSe_2. The FET characteristics are shown on the right. It can be seen that the devices with vdW 1T' metal TMDs perform better. **b,** Optical microscope image of back gated WSe_2 FET array with VSe_2 as contact metal electrodes. The transfer curve of FET shows two orders higher hole current with VSe_2 contacts compared with metal contacts. The images are reproduced from Ref[172,173].

Chapter 4 Experimental Methods: Materials Synthesis, Characterisation, and Device Fabrication

In this Chapter, key experimental details used to carry out my research are described. I have made important developments in sample preparation methods, sample characterisation, and device fabrication that were crucial for realising the results described in Chapters 5 and 6. I made key adjustments to chemical vapor deposition (CVD) methods to obtain high quality materials that are crucial for high performance devices. The main focus of my doctoral research is the metal-2D semiconductor interface. To characterise the interface, I sought to minimize, analyse and characterise contamination on the surface of 2D TMDs. I also analysed the metal-semiconductor interface using cross-section scanning transmission electron microscopy (STEM). The preparation of monolayer MoS_2-metal cross-section STEM foils is extremely challenging and was developed during my doctoral research to image the interface with atomic resolution.

4.1 Sample preparation

The 2D TMD samples used for research reported in this thesis were prepared by CVD and mechanical exfoliation. Heterostructures such as 2D TMDs on hexagonal boron nitride (h-BN) were prepared by dry transfer. In the following sections, modifications to usual sample preparation methods are described.

4.1.1 CVD

To obtain high quality 2D TMDs by CVD and realise high quality devices without the need to transfer onto electronic grade substrates, I focused on developing low temperature growth. CVD of 2D TMDs for electronic devices is typically done on SiO_2 on Si substrates. However, the typical CVD growth temperatures (> 800 °C) break the SiO_2 insulating layer so that back gated devices directly on the as grown 2D TMDs cannot be fabricated due to the high leakage current. Thus, 2D TMD growth conditions that do not destroy the oxide layer are preferred for device fabrication. I attempted to develop several methods for low temperature growth of MoS_2. Of these, most showed that growth of MoS_2 on SiO_2/Si substrates leads to destruction of the insulating properties of the SiO_2 – leading to substantial leakage between the source and gate electrodes of the FETs. I summarize the different methods in the following sections.

Method 1: PTAS assisted growth

Perylene-3,4,9,10 tetracarboxylic acid tetrapotassium salt (PTAS) seed layer on the substrate lowers the nucleation energy barrier for MoS_2 and thus allows low temperature growth[36]. Schematic illustration of the single zone furnace experimental set up for PTAS seed assisted growth of MoS_2 is shown in **Figure 4.1a**. The 2D MoS_2 was grown on 300 nm SiO_2/Si substrates that were washed with acetone, isopropanol and deionized water. The growth chamber is a 2.5 cm diameter quartz tube with flanges at the ends for gas input and output. The ~25 µL of 80 µM of PTAS (from 2D Semiconductors) was dropped onto the substrate using a

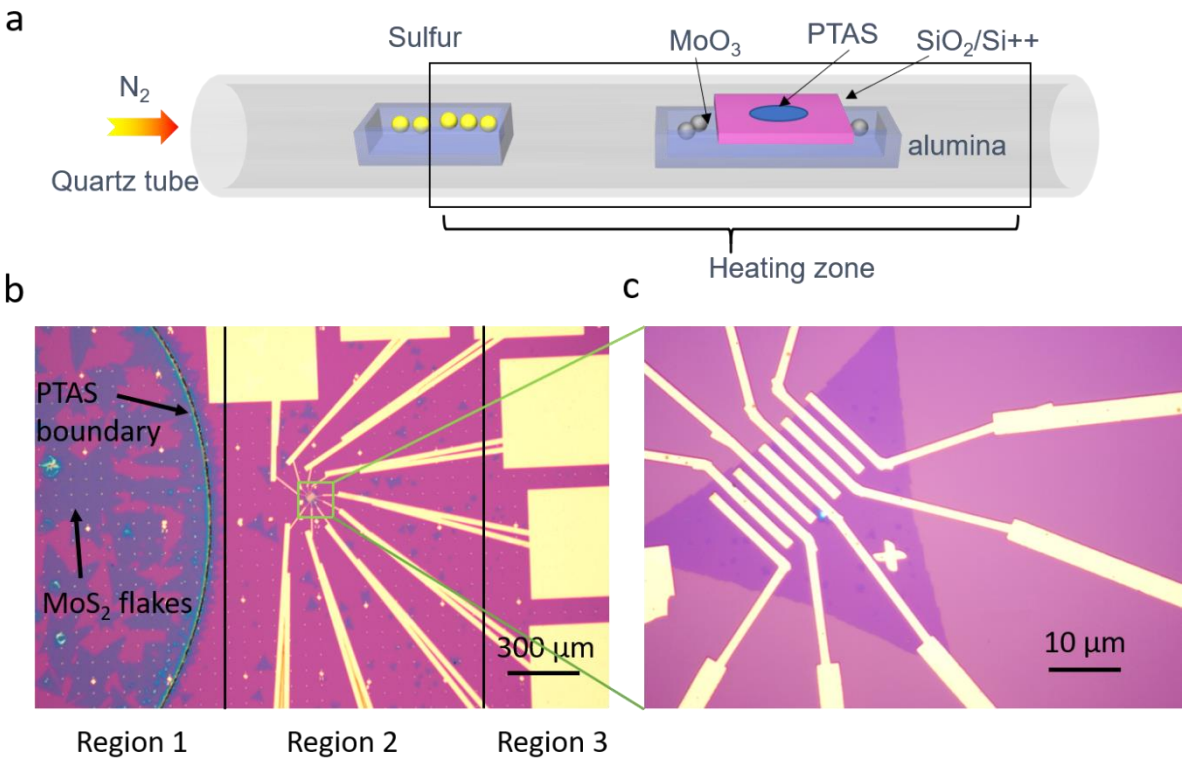


Figure 4.1 a, Schematic of single zone CVD furnace used for PTAS assisted MoS_2 growth. The quartz tube is placed within the furnace is shown in the schematic. The sulfur powder was placed upstream of gas flow and the MoO_3 powder was placed in the alumina boat placed at the center of the furnace. The black rectangle represents the furnace heating zone. A drop of PTAS seed was deposited on the SiO_2/Si substrate, which was placed face down on the alumina boat. **b,** Optical microscope image of CVD grown MoS_2. It can be divided into three regions. Region 1 is within the PTAS drop and high density of triangular blue flakes can be seen. Region 2 shows less dense region and Region 3 located far away from PTAS does not show any MoS_2 flakes. Lithographically patterned devices directly on CVD grown MoS_2 are shown in **b** and **c**. In **c,** several devices on a single triangular MoS_2 are shown.

pipette. After drying the PTAS on a hot plate in air at ~ 80 °C, the substrate was placed face-down on an alumina boat in the middle of the furnace. MoO_3 and sulfur powders were used as the precursors. The alumina boat at the center of the furnace contained 3 mg of MoO_3 and the alumina boat at the edge of the furnace contained 10 mg S. The rectangle in the figure is roughly the heating zone of the furnace. When the temperature at center of the furnace was set to 700 °C, the temperature at the edge of the furnace was ~ 200 °C – sufficient for sublimation of sulfur powder. To start the growth process, the tube was first heating up to the growth temperature at 700 °C within 15 minutes in nitrogen (N_2, ultrahigh purity, Air Gas, 500 standard cubic centimeters per minute (sccm)). The gas flow rate was changed to 60 sccm during growth. After 20 min at 700°C, the furnace was cooled to room temperature and the samples were removed from the tube. Typical results are shown in **Figure 4.1b**. Three regions are typically found on the substrate. Region 1 is within the PTAS droplet with high density of single layer MoS_2 triangles. Region 2 shows isolated MoS_2 flakes with lateral dimensions of 10 – 100 μm located near the PTAS ring. Region 3 shows small flakes of less than 10 μm in lateral size away from the PTAS droplet edge.

Typically, field effect transistors (FETs) were made on flakes in Region 2 because they are well distanced and laterally large, as shown in the **Figure 4.1b**. **Figure 4.1c** is the zoomed in part of the device (the green square in **Figure 4.1b**). While the growth of MoS_2 on PTAS at relatively low temperature of 700 °C yielded good results in the terms of the material quality, electrical device measurements showed significant leakage current between the gate and drain electrodes. I have found that deposition of PTAS on SiO_2 on Si substrates leads to leaky devices in almost all cases. While the exact reason for this is unclear, I decided to pursue other methods to grow MoS_2 at low temperature to increase the yield of devices.

Method 2: Salt assisted growth

Another way to grow MoS_2 at low temperature is by mixing salt (such as NaCl, KI) into the Mo powder precursor[174] to lower the melting temperature of MoO_3 (~ 795 °C). The salt reacts with MoO_3 to form a low-melting-point metal chloride that acts as the Mo source for MoS_2 growth. The general reaction can be written as:

$$2NaCl + 3MoO_3 \rightarrow MoO_2Cl_2 + Na_2Mo_2O_7$$

$$MoO_2Cl_2 + 4H_2 + 3X(S, Se, Te) \rightarrow MoX_2 + 2HCl\ (g) + 2H_2O(g) + H_2X(g)$$

Following this concept, I optimised the growth conditions for NaCl assisted growth. The best growth was achieved with 3 mg of MoO_3 mixed with 0.5 mg of NaCl. The mixture was poured into an alumina boat that was then placed in center of the furnace. Another alumina boat containing ~20 mg sulfur powder was placed upstream near the furnace edge, as indicated in **Figure 4.2a**. The tube was then filled with flowing Ar/H_2 (5% H_2) for 15 min at 500 sccm. Then the furnace was heated to 680 °C to vaporize the MoO_3 and the sulfur powders. The gas flow rate was changed to 80 sccm during growth. After 10 min, the furnace was cooled to room temperature and the samples were removed. The optical microscopy image of the growth result is shown in **Figure 4.2b**. The bright yellow region in the figure is a scratch to observe contrast between the substrate and the MoS_2 film. To reduce the flux Mo vapor onto the substrate,

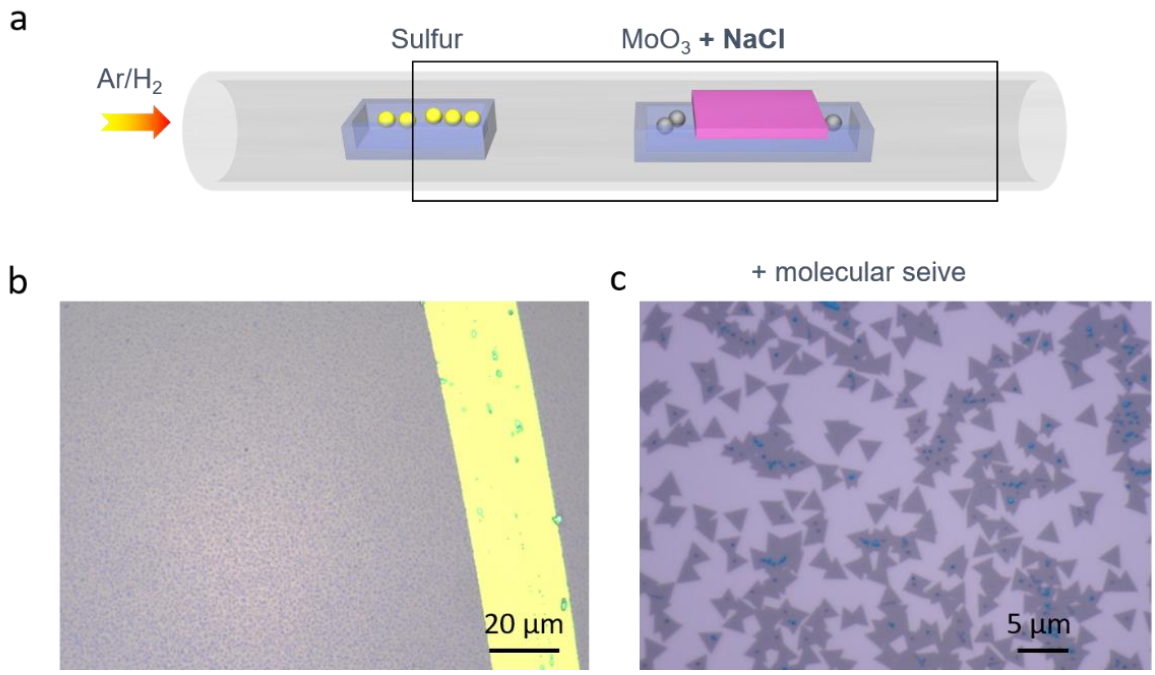


Figure 4.2 a, Schematic of the CVD growth quartz tube for NaCl assisted MoS_2 deposition. The quartz tube is placed within the furnace is shown in the schematic. The sulfur powder was placed upstream of gas flow and the MoO_3 with NaCl powder was placed in the alumina boat placed at the center of the furnace. The SiO_2/Si substrate was placed face down on the alumina boat. The black rectangle represents the furnace heating zone. For the molecular sieve involved growth, the molecular was mixed in the alumina boat with MoO_3. **b,** Optical microscope image of CVD grown MoS_2 flakes showing uniform MoS_2 triangles. A scratch was made by tweezer on the film to show better contrast of the film. **c,** Growth with molecular sieve to control the source release rate. Isolated small triangles are obtained with this method.

molecular sieves were added in the alumina boat lower the source release rate[174]. As a result, isolated small triangles (less than 5 µm) are obtained by this method (shown in **Figure 4.2c**).

FETs fabricated on highly dense MoS_2 growth regions revealed substantial leakage current. This is most likely due to the fact that these regions are electrically continuous and some of the flakes grow on the edges of the SiO_2/Si substrates, which can cause short circuit between the bottom gate and the drain. The FETs on less densely packed flakes obtained using molecular sieve, do not exhibit any leakage current but their laterally small dimensions make it difficult to fabricate many devices on the same flake – needed for assessing contact properties. Therefore, I sought to increase the lateral growth rate using the salt assisted growth method with eutectic intermediate reaction.

Method 3: Salt assisted growth with eutectic intermediate reaction

Another explanation for MoS_2 growth at low temperature using salt assisted method is the formation of eutectic intermediates from reaction between MoO_3 and alkali metal compounds[39]:

$$AB + MoO_3 \rightarrow Na_2MoO_4 + Na_2Mo_2O_7 + byproduct \uparrow$$

Where A refers to an alkali metal and B indicates the anions. The gaseous byproduct are typically MoO_2Cl_2 and H_2O. As a result, the eutectic intermediates containing alkali metal molybdates are formed and have high mobility due to their low melting point. They tend to join together and react with sulfur vapor described by the follow equations[39]:

$$Na_2Mo_2O_7 + 7S \rightarrow 2MoS_2 + Na_2SO_3 + 2SO_2$$

$$Na_2MoO_4 + 5S \rightarrow MoS_2 + Na_2S + 2SO_2$$

Both of the above reactions have negative Gibbs free energy that are thermodynamically favorable. Further, the eutectic intermediates are more likely to attach to the edges of small flakes, leading to large lateral growth. Several key parameters are important and must be controlled precisely. First, it is important that the sulfur does not sublimate before the eutectic intermediates are generated because the sulfur must react with the eutectic intermediates to form MoS_2 on the substrate. Second, the amount of NaCl used in this method is less than 1mg and therefore it is challenging to uniformly mix the NaCl with the MoO_3 powder. A better method is to spin coat the SiO_2 on Si substrate with NaCl or NaOH dissolved in water to achieve uniform distribution. Third, for clean and uniform growth of MoS_2, hydrophilic SiO_2 substrate is preferred as it also allows uniform distribution of Na during spin-coating.

To achieve hydrophilic SiO_2, we treated the surface with oxygen plasma[175] before spin coating with 0.1 M NaOH or NaCl. The growth setup shown in **Figure 4.3** is similar to those shown above with MoO_3 powder placed in the center of the furnace and sulfur powder placed outside the heating zone (as indicated by the black rectangle in **Figure 4.3a**). The furnace was heated to growth temperature (700 °C) in N_2 atmosphere and stabilized for one minute. The quartz tube was then pushed forward so that sulfur begins to sublimate (as indicated by the red rectangle in **Figure 4.3a**). The results from the growth in this way are shown in **Figure 4.3b**, which shows monolayer MoS_2 flakes with lateral dimensions of 20-40 µm. FET measurements indicate that samples grown using this method do not exhibit substantial leakage currents. The main reason for this is that the reaction with the eutectic intermediates occurs on the surface

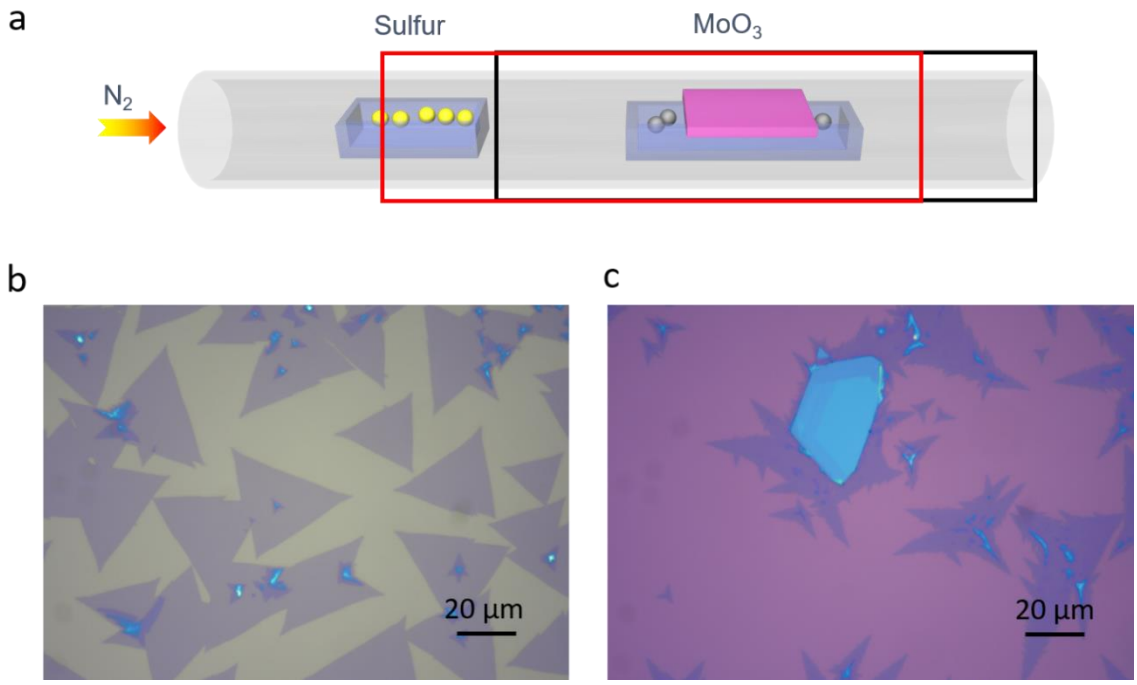


Figure 4.3 a, Schematic of the setup for eutectic intermediates growth. The sulfur powder was placed upstream of gas flow and the MoO_3 powder was placed in the alumina boat placed at the center of the furnace. The treated (coated with NaCl or NaOH solution) SiO_2/Si substrate was placed face down on the alumina boat. The furnace heating zone is indicated by the black rectangle. After the furnace reached growth temperature and stabilized for one minute, the tube was pushed right shift and the furnace heating position shifted to the position as indicated by the red rectangle. **b,** Optical microscope image of MoS_2 flakes with lateral dimensions of > 20 µm. **c,** Optical microscope image of CVD growth of MoS_2 on mechanical exfoliated h-BN. The MoS_2 only grows around the h-BN flake rather than on top of it.

only and therefore MoS_2 is only formed on the SiO_2 surface and not on the sides so that short circuiting is less likely to occur.

This method showed high quality MoS_2 flakes of very high quality. It is well known that MoS_2 on h-BN yields very good device characteristics. Therefore, direct growth of MoS_2 on h-BN is highly appealing. A substantial effort therefore was spent on trying to grow MoS_2 on h-BN using the eutectic intermediate reaction method. To do this, h-BN flakes were mechanically exfoliated on SiO_2/Si substrates and growth was performed using the method outlined above. It was found that growth of MoS_2 on h-BN did not occur using this method. The optical microscope image of one attempt of growth on h-BN is shown in **Figure 4.3c** where the trapezoid flake is h-BN and other light blue contrast flakes are CVD grown MoS_2. We observed only lateral growth around BN.

4.1.2 Mechanical exfoliation

CVD growth provides large monolayer MoS_2 flakes for FETs. However, it is easier to work with multi-layer TMD samples initially for optimization of contacts and other parameters. It is not possible to make multi-layered TMDs by CVD and therefore mechanically exfoliated multilayered samples were used in this study.

The multilayer TMD samples were obtained by the Scotch tape method[176] described in Chapter 2. The optical microscope image of mechanically exfoliated samples is shown in **Figure 4.4a**. The black arrow indicates monolayer MoS_2 while the red arrow represents multilayer (thickness of less than 10 nm) flake.

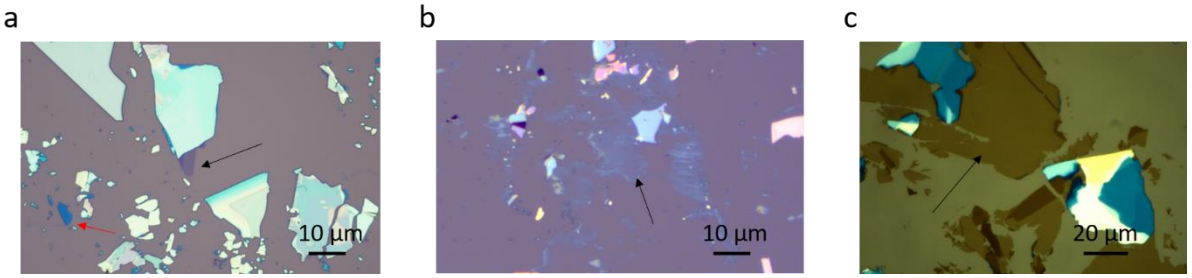


Figure 4.4 Optical microscope images of MoS_2 made by different mechanical exfoliation methods. **a,** typical tape method without further treatment[176]. The black and red arrows are monolayer and thin flakes, respectively, that are suitable for FET fabrication. **b,** Mechanical exfoliation with heat treatment[30]. The arrow indicates residue region left on the substrate. **c,** Au assisted exfoliation[31] giving large scale monolayers.

I have also attempted several techniques[30,31] that claim to yield exfoliated flakes with large lateral size, as described in Chapter 2. One such method is heating the tape before peeling off from substrate[30]. However, this method leaves a substantial amount of residue on the substrate as shown in **Figure 4.4b**. Another method is Au assisted exfoliation[31], results of which are shown in **Figure 4.4c**. It yields large monolayer MoS_2 flakes with lateral size of over 50 µm. Although this seems to be a good approach to obtain large and clean looking monolayer samples, the sample quality turns out to be poor as described below.

To assess the quality of monolayer MoS_2 samples, atomic force microscopy (AFM) and photoluminescence (PL) spectroscopy were performed. AFM was done with tapping mode in Bruker and PL was measured with 514 nm laser in Renishaw system. The AFM of the Scotch tape exfoliation sample is shown in **Figure 4.5a**. The average surface roughness was found to be ~ 0.247 nm as labeled in the figure. In contrast, the AFM image (**Figure 4.5b**) of the Au assisted exfoliated sample an average surface roughness of ~ 1.386 nm due to the residue left behind on the MoS_2 surface from the Au etching process[31]. The PL spectra of the exfoliated

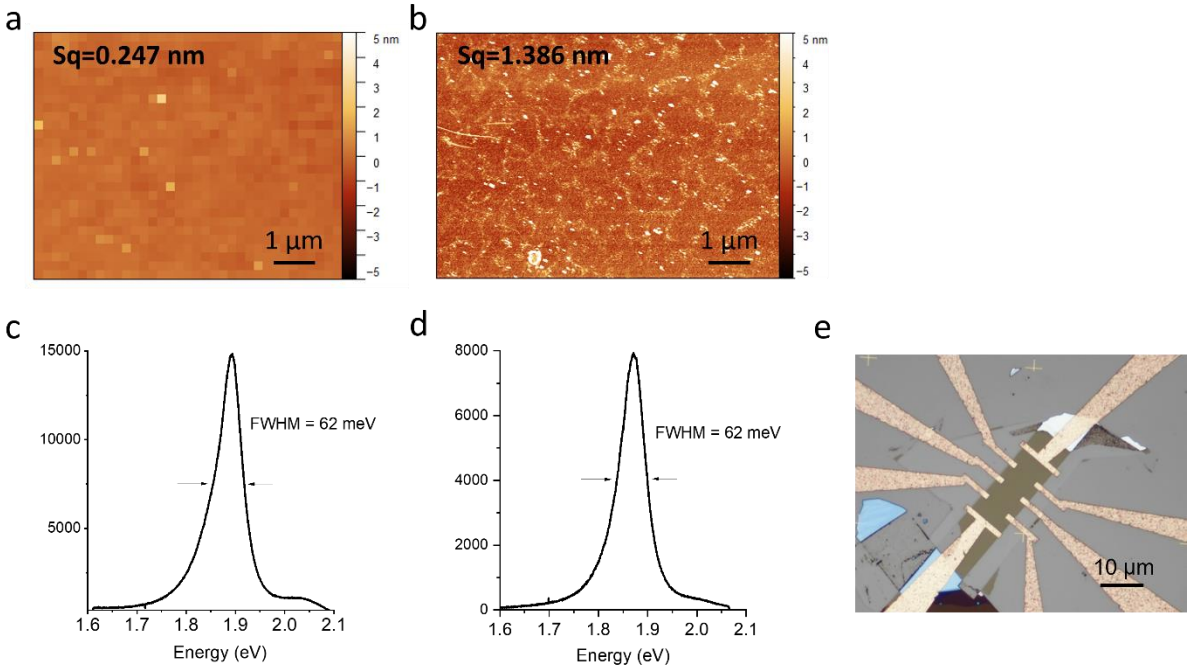


Figure 4.5 Comparison of monolayer MoS_2 made by Scotch tape and Au assisted mechanical exfoliation methods. **a,** AFM image of MoS_2 surface fabricated by Scotch tape method without further treatment. b, AFM image of MoS_2 surface made by Au assisted exfoliation. **c,** PL of monolayer Scotch tape MoS_2. **d,** PL of monolayer MoS_2 made by Au assisted exfoliation. **e,** Optical microscope image of FET contacts on monolayer MoS_2 made by Au assisted exfoliation.

samples are shown in **Figure 4.5c** and **d**. The full width half maximum (FWHM) of the two types of samples is similar (~ 62 meV) while the intensity of the PL from the Scotch tape sample is slightly better than the Au assisted exfoliated sample under the same measurement conditions. FET devices fabricated on the mechanically exfoliated samples made using the Au assisted method revealed that it was challenging to achieve clean contacts. The optical microscope image of a typical device made from Au assisted samples is shown in **Figure 4.5e**. The metal electrodes appear rough and discontinuous due to the presence of residue on the samples. FETs fabricated with Au assisted samples generally performed poorly. Based on my experiments, I have concluded that while Au assisted exfoliation approach is suitable for producing large area monolayer TMDs for optical measurements, they are not ideal for device applications unless the contamination issue is solved. Thus, I used the mechanically exfoliation by Scotch tape method for the multilayered samples used throughout my thesis.

4.1.3 Dry transfer

Dry transfer technique provides an ideal platform for stacking TMDs on arbitrary substrates[177]. In Chapter 6, different substrates are used to investigate the effect of dielectric environment on

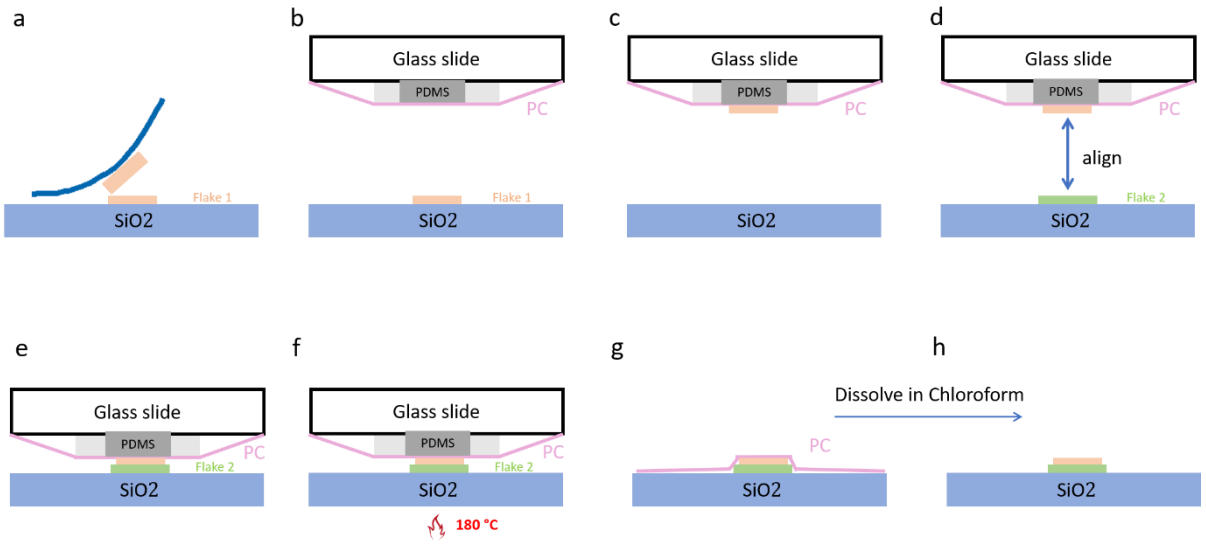


Figure 4.6 Schematic of PC assisted dry transfer method. **a,** Flake 1 on SiO_2 substrate is obtained by the Scotch tape method. **b,** A stamp with glass slide/PDMS covered by thin film PC is brought into contact with flake 1. **c,** Flake 1 is picked up by the stamp. **d,** Alignment of the stamp with flake 1 and flake 2 on target substrate. **e,** The stamp is brought in contact to stack on flake 2. **f,** The stage is heated up to 180 ° C for 5 minutes to melt the PC. **g,** The stamp is removed, leaving PC and flake 1 on the substrate. **h,** The PC is dissolved by chloroform.

device performance including h-BN made by mechanical exfoliation. Dry transfer technique can be used to stack 2D semiconductors on h-BN. The most common dry transfer approach is the polycarbonate (PC) assisted method illustrated in **Figure 4.6**. In the PC method, a thick flake is mechanically exfoliated by the Scotch tape method onto a SiO_2 substrate first. Then a stamp (glass slide with PDMS covered by thin PC film) is brought in contact with the exfoliated flake on the SiO_2 so that it adheres to the stamp. The stamp picks up flake 1 in the figure and places it on to another flake 2. The stacking is assisted by a microscope for precise alignment. During this process, the substrate is fixed by vacuum stage. When flake 1 makes contact with flake 2, the sample stage is heated to 180 ° C to release PC and flake 1 onto flake 2, as shown in **Figure 4.6e-g**. Finally, the PC is dissolved by immersing the sample in chloroform. **Figure 4.7** depicts a sample transferred by this procedure. The optical image of h-BN flake is shown in **Figure 4.7a** and MoS_2 stacked on h-BN is shown in **Figure 4.7b**. The sample was also imaged by AFM (shown in **Figure 4.7c**). The image shows that there is substantial contamination on the sample surface. The average roughness of the h-BN region (indicate by the black square) was found to be ~1.31nm and the average roughness of the heterostructure (indicate by the red square) was ~ 2.06 nm due to air bubbles trapped between h-BN and MoS_2 or contamination on bottom side of flake 1 due to absorbates on SiO_2 substrate.

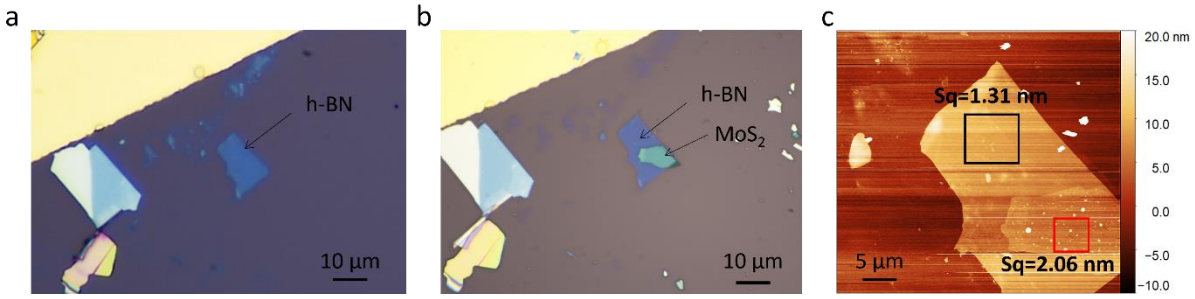


Figure 4.7 a, Mechanically exfoliated h-BN on SiO_2. **b,** MoS_2/h-BN heterostructure made by PC assisted dry transfer method. **c,** AFM image of the stacked sample. The average roughness of the h-BN region (black square) is around 1.31 nm, which is higher than typical mechanically exfoliated MoS_2. The average roughness of the MoS_2/h-BN region (red square) is even higher due to air bubbles trapped between MoS_2 and h-BN.

Since significant contamination was found in samples fabricated by the PC assisted transfer approach, the PDMS assisted dry transfer approach[178] was investigated (**Figure 4.8**). In this method, instead of exfoliating on SiO_2 first, flake 1 was exfoliated directly on PDMS as indicated in **Figure 4.8a**. Then the PDMS substrate was placed upside down under a

microscope to align with flake 2. The stamp was brought into contact with flake 2. Flake 1 can then be detached from PDMS by heating at 60 ° C for 2 minutes. This method is easier than the PC assisted transfer but the thickness of flakes on PDMS is more difficult to identify due to low contrast. The flakes exfoliated on PDMS also tend to have wrinkles due to the stretchability of the PDMS substrate. **Figure 4.9** depicts one sample transferred by this procedure. **Figure 4.9a** shows an optical microscope image of h-BN flake before transfer and **Figure 4.9b** shows image of stacked MoS_2/h-BN heterostructure. The AFM image of the MoS_2 on top of h-BN is shown in **Figure 4.9c**. The average surface roughness of black square region was found to be ~ 1.21 nm. The results show that this method also leads to some surface

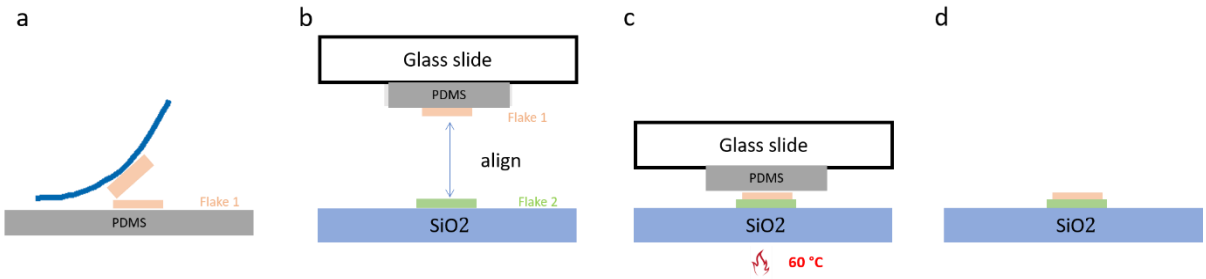


Figure 4.8 Schematic of PDMS assisted dry transfer method. **a,** Mechanically exfoliated flake 1 on PDMS substrate. **b,** Alignment of flake 1 with flake 2. **c,** The stamp is brought in contact with flake 2 and the stage is heated to 60 ° C for 2 minutes to detach flake 1 from PDMS. **d,** The stamp is removed, leaving the heterostructure on the target substrate.

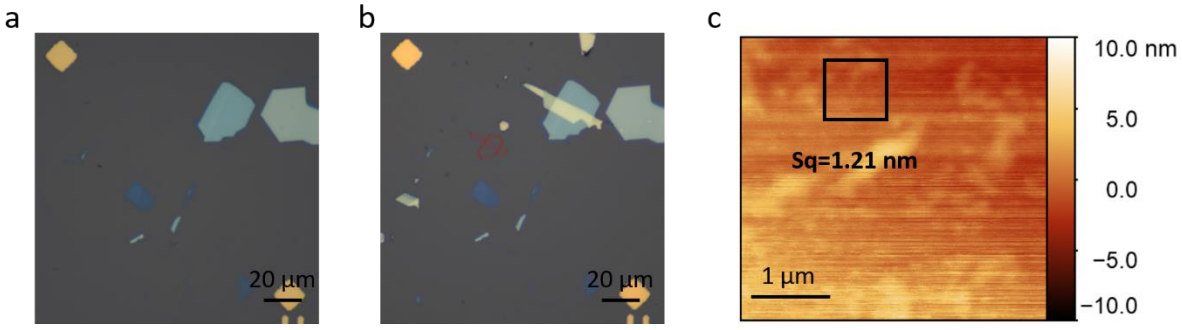


Figure 4.9 a, Mechanically exfoliated h-BN on SiO_2. **b,** MoS_2/h-BN heterostructure made by PDMS assisted dry transfer method. **c,** AFM image of the stacked sample. The average roughness (black square) of MoS_2 surface is ~ 1.21 nm, which is less than that of PC assisted transfer method.

contamination on MoS_2 surface but results from many samples such that the method is slightly cleaner compared to the PC assisted transfer technique. Therefore, I have used the PDMS assisted transfer technique to fabricate heterostructures.

4.1.4 Wet transfer

Wet transfer is frequently used to transfer 2D TMDs from one substrate to another. For example, CVD samples grown on sapphire or SiO_2 at high temperatures are not suitable for making devices. These samples therefore need to be transferred to other dielectric substrates for device fabrication. 2D TMD samples that require TEM imaging also need to be transferred onto TEM grids (usually Cu foil with carbon film). Poly (methyl methacrylate) (PMMA) wet transfer method is commonly used[178] and is described in **Figure 4.10**. In this method, PMMA is applied to coat the 2D TMDs on SiO_2 substrate. The sample is then etched using a 0.5 M KOH solution or diluted HF solution (HF is cleaner in my experience), leaving 2D TMDs with PMMA floating in the solution. To remove KOH or HF, the PMMA/TMDs film is washed thoroughly with DI water. The sample is then scooped out of the solution using target substrate or TEM grid and allowed to dry. Finally, acetone is used to dissolve the PMMA, leaving the 2D TMDs on the new substrate.

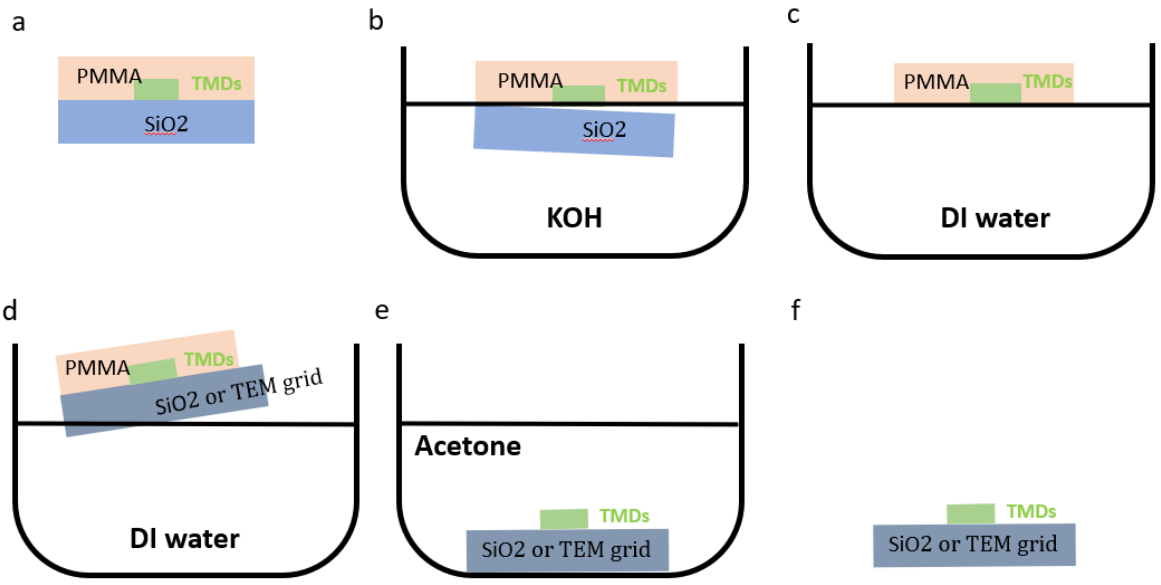


Figure 4.10 Schematic of PMMA wet transfer process. **a,** PMMA is coated onto substrate with 2D TMDs. **b,** KOH (or HF) is used to etch SiO_2 substrate and detach the PMMA/TMDs film. **c,** The PMMA/TMDs film is rinsed with DI water. **d,** Target substrate is used to scoop the sample out. **e,** PMMA is removed with acetone. **f,** Target substrate with 2D TMDs.

4.1.5 PMMA residue

The biggest challenge with using PMMA for transfer is the residue that it leaves on the 2D TMDs. PMMA residue is also a severe problem in device fabrication where it is used as the resist for lithographic patterning. I carried out a detailed study of PMMA residue and devised

methods to minimize it on 2D TMDs. Different approaches such as plasma treatment and thermal annealing have been reported to minimize PMMA residue on 2D TMDs[179]. One issue with plasma and thermal treatments is that it can damage the fragile 2D TMDs. Another approach involves using methyl methacrylate (MMA) monomer instead of PMMA. Studies have shown that the removal of PMMA is achieved by breaking the polymer backbone bond[180]. Further work has shown that low molecular weight/low chain length PMMA reduces residue on graphene sample[181]. Inspired by this, I compared the amount of residue left behind from MMA with PMMA on 2D TMDs. Meanwhile, due to their differing viscosities, several concentrations of PMMA were investigated for comparison.

First, mechanically exfoliated MoS_2 on SiO_2 samples were spin coated with PMMA (~ 400 nm) or MMA/PMMA (~ 100 nm/ 400 nm, first coat MMA then cover PMMA). Then the polymer was removed by dipping the sample in acetone for over one hour. After which the samples were observed in AFM to obtain roughness, as shown in **Figure 4.11**. In figure, the letters A and EL represent anisole and ethyl lactate solvents, respectively. PMMA concentrations of 2%, 4%, 6%, and 8% represented by the letters A2, A4, A6, and A8 were investigated. The results show that the average surface roughness after PMMA removal is much higher than for MMA samples.

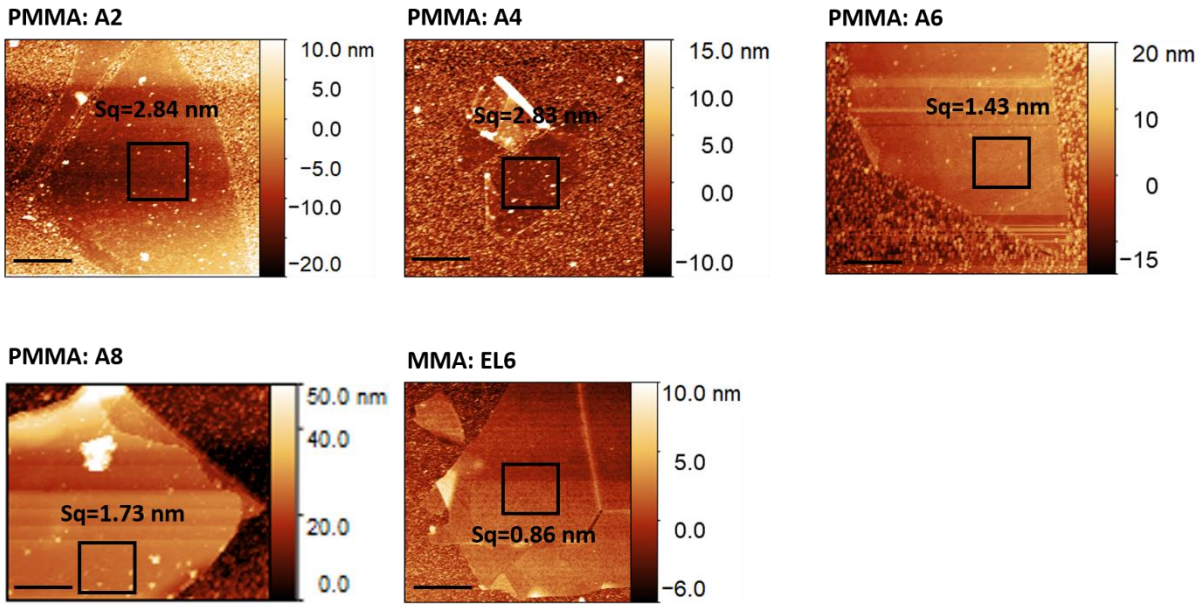


Figure 4.11 AFM images of MoS_2 flakes after removal of PMMA or MMA/PMMA. The label A represents the solvent anisole and EL stands for solvent ethyl lactate. Numbers after the label represent PMMA concentration. Molecular weight PMMA = 950000 g/mol. Scale bar = 5µm.

The PMMA was further examined by X-ray photoelectron spectroscopy (XPS, Thermo Fisher Scientific). **Figure 4.12a** shows C 1*s* spectra for pristine mechanically exfoliated MoS_2 sample. It shows typical adventitious carbon signal (most samples exposed to atmosphere have this detectable carbon contamination)[181]. **Figure 4.12b** shows MoS_2 C 1*s* spectra after MMA removal, whereas MoS_2 C 1*s* spectra after PMMA removal are shown in **Figure 4.12c**. The XPS spectrum for MMA coated MoS_2 sample is comparable to that of pristine sample. In contrast, the XPS of PMMA coated sample shows higher concentration of C=O peak at binding energy of 288.3 eV and C-C peak at binding energy of 286 eV. Those peaks are recognized as different species in PMMA[179,181,182].

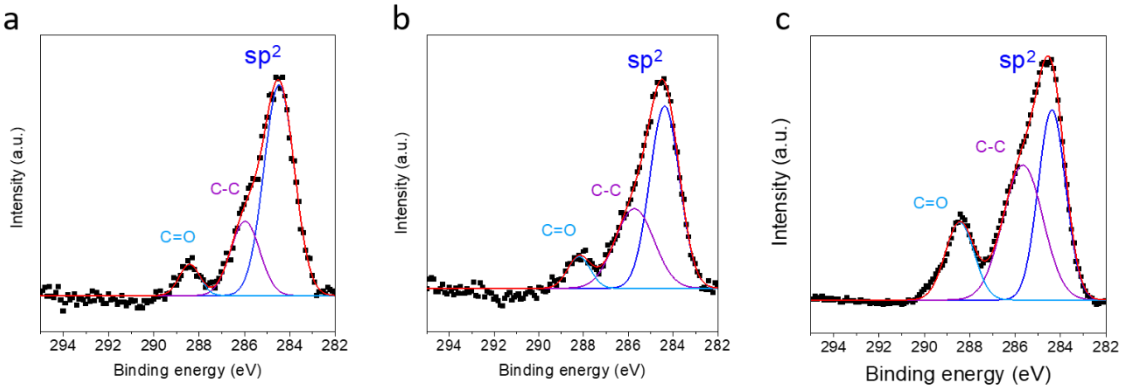


Figure 4.12 a, C 1*s* XPS peak of pristine MoS_2 sample arising from adsorbates. **b,** C 1*s* spectrum of MoS_2 sample after removing MMA. **c,** C 1*s* spectra of MoS_2 sample after removing PMMA.

Lastly, scanning transmission electron microscopy (STEM, FEI Titan G2 60-300, 80 kV) was used to directly observe the cleanliness of monolayer MoS_2 after removing MMA or PMMA. CVD grown MoS_2 samples were transferred onto TEM grid by the wet transfer method described above. Four samples were investigated for comparison. The first sample was MMA assisted wet transfer and removal with acetone. The second sample was MMA assisted wet transfer and MMA removal after electron beam (e-beam) exposure and development (the dose of e-beam is 500 $\mu C/cm^2$). Third sample was PMMA assisted wet transfer removed by acetone. The fourth sample was PMMA assisted wet transfer in which the PMMA was removed by electron beam exposure and development. Low and high magnification high angle annular dark field (HAADF) STEM images of the four types of MoS_2 are shown in **Figure 4.13**. It can be seen from the low magnification images that all four samples contain some white contrast, suggesting that all possess surface residue. Some large clusters (> 100 nm) can be seen in the PMMA-assisted wet transferred samples. The high magnification STEM images show clean areas (indicated by red regions) and contaminated regions. According to the STEM study,

MMA assisted transferred samples have a larger proportion of clean areas compared to PMMA assisted samples.

I also conducted a control experiment in which only DI water was used to transfer MoS_2 onto a TEM grid for imaging (without any polymer). The amount of residue in polymer free transfer sample was comparable to when MMA was used. Although we were unable to conclude that the MMA assisted transfer method is completely clean, AFM, XPS, and STEM studies reveal that it is very close to pristine samples and much cleaner than PMMA assisted transfer.

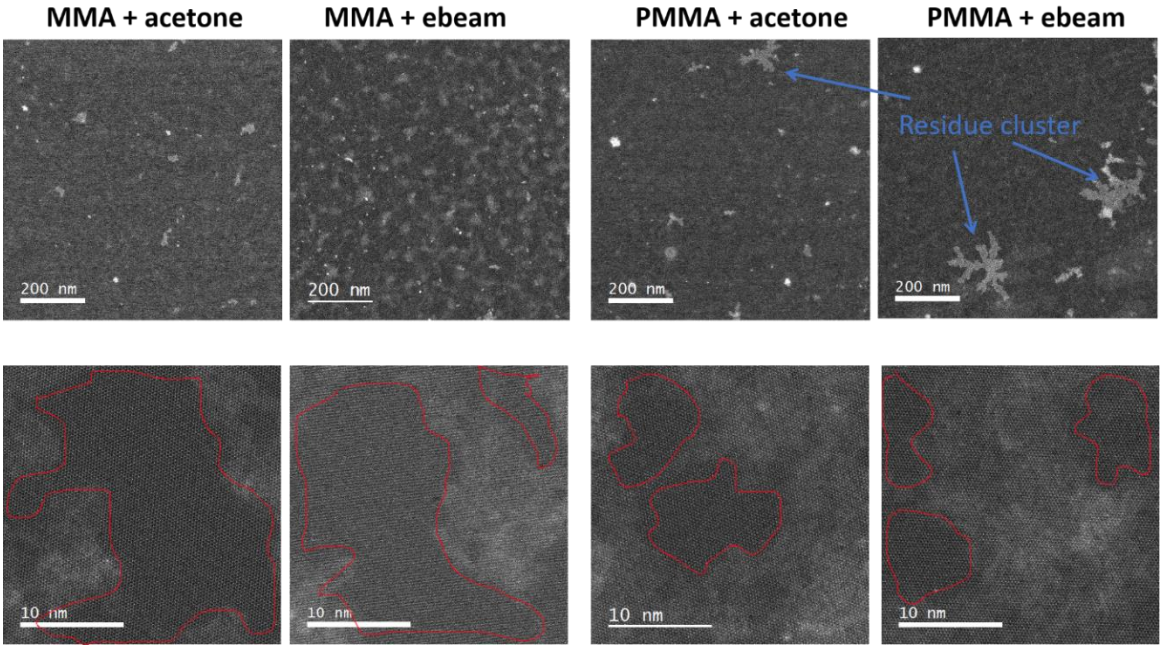


Figure 4.13 Low (upper four images) and high (lower four images) magnification HAADF STEM images of monolayer MoS_2 transferred by: MMA assisted wet transfer and dissolved by acetone; MMA assisted wet transfer and removed by e-beam exposure followed by development; PMMA assisted wet transfer and dissolved by acetone; PMMA assisted wet transfer and removed by e-beam exposure followed by development. The blue arrows indicate large residue clusters. The red circles demonstrate clean regions.

4.2 Characterisation of 2D TMDs

CVD, mechanically exfoliated and transferred samples were characterized in detail using the techniques described in Chapter 2.

4.2.1 Raman/PL

The PL spectra (measured with Renishaw, 514 nm laser, 100 µW laser power) from CVD grown MoS_2 flakes are shown in **Figure 4.14a**. Measurements were made on ten different flakes. It can be seen that the PL spectra vary from flake to flake even on the same chip. The PL intensity as well as the peak position can vary. The PL peaks contain contributions from excitons (electron-hole pairs) and trions (charged exciton containing two electrons and one hole). Typically, in CVD MoS_2, the different trion and exciton ratios lead to PL peak being located between 1.82 eV and 1.85 eV for ten spectra shown in **Figure 4.14a**. The overall PL peak energy is slightly lower for CVD MoS_2 compared to that of mechanically exfoliated MoS_2 (see **Figure 4.5**, PL peak located at ~ 1.88 eV). This might be due to greater electron doping of CVD MoS_2 from SiO_2 substrate. The lowest FWHM among the ten spectra was found to be 52 meV (flake 6, red curve in **Figure 4.14a**).

Amani *et al.* reported PL enhancement of monolayer MoS_2 by treating it with bis(trifluoromethane) sulfonimide (TFSI)[183]. They attribute the PL enhancement to hole doping from TFSI. In **Figure 4.14b**, the PL spectra of MoS_2 before and after TFSI treatment are presented for comparison. Due to hole doping, which minimizes negative trion contributions, the peak blue shifts to 1.85 eV. These findings suggest that the CVD grown MoS_2 are electron doped – possibly from SiO_2 substrates. The Raman spectra (measured with Renishaw, 514 nm laser, 100 µW laser power) of CVD MoS_2 sample before and after TFSI treatment are shown in **Figure 4.14c**. Typical E_{2g} and A_{1g} peaks are observed[48]. The E_{2g} peak right shifts after TFSI treatment, indicating hole doping of the sample, which is consistent with the PL results.

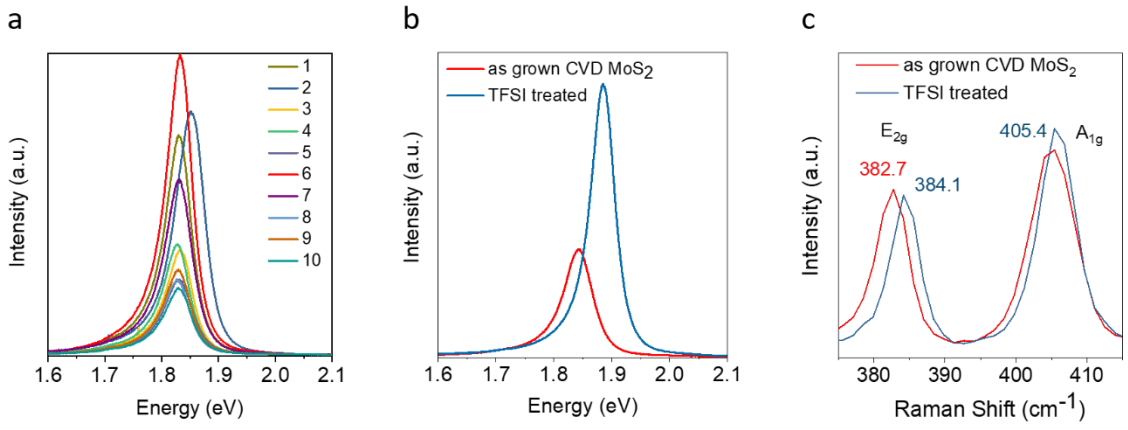


Figure 4.14 a, PL spectra of CVD grown MoS_2. Ten flakes were randomly selected for comparison. **b,** PL spectra of CVD grown MoS_2 before and after TFSI treatment. **c,** Raman spectra of CVD grown MoS_2 before and after TFSI treatment.

4.2.2 XPS

XPS is commonly used to determine the chemical state of 2D materials. The spot size of X-ray beam in typical XPS is ~ 400 μm and therefore large crystals are required. XPS results from freshly cleaved MoS_2 crystals are shown in **Figure 4.15a** and **b**. The binding energies for Mo 3*d* and S 2*p* doublets are located at 229.3 eV (Mo $3d_{5/2}$) and 162.1 eV (S $2p_{3/2}$) – typical of pristine MoS_2. XPS is sensitive to damage and defects and therefore can be used to assess the quality of 2D TMDs. For example, **Figure 4.15c** shows Mo 3*d* spectrum of cleaved MoS_2 crystal after a 10-second exposure to low-energy (1kV) Argon ion bombardment. An extra Mo $3d_{5/2}$ peak arises at lower binding energy of 228.2 eV due to defective MoS_2. This is similar to the spectra formed when Titanium is deposited on top of MoS_2 and reacts with it to generate intermediate states[184].

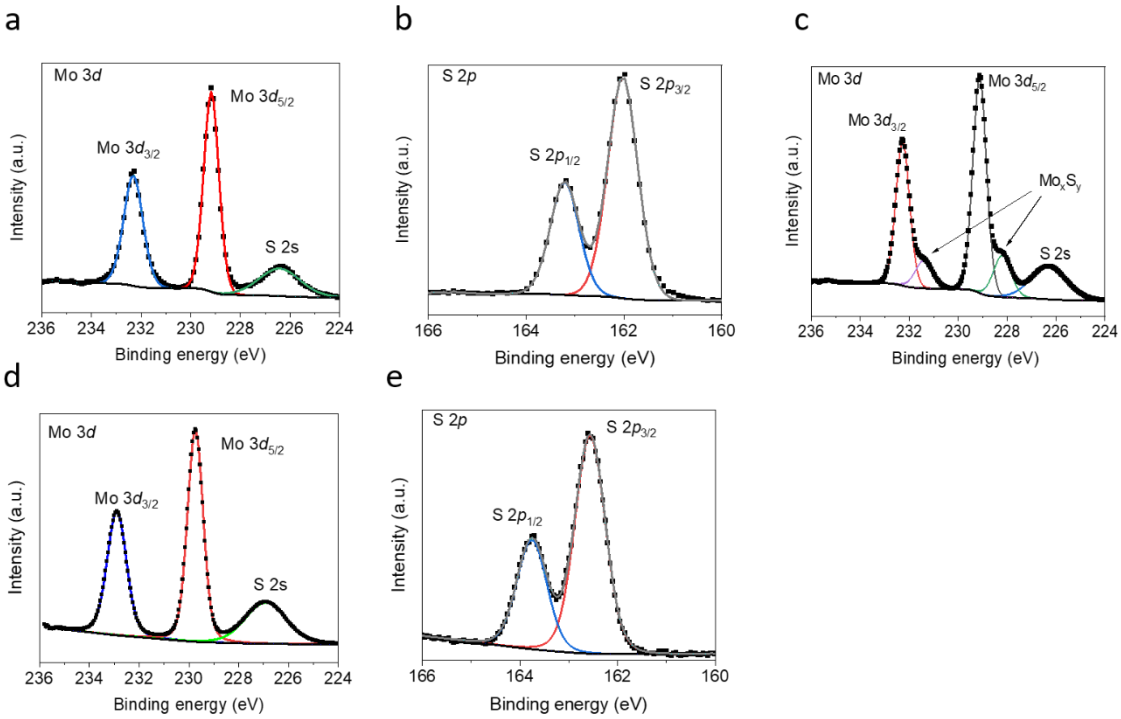


Figure 4.15 XPS of MoS_2. **a,** Mo 3*d* spectrum of mechanically exfoliated crystal. **b,** S 2*p* spectrum of mechanically exfoliated crystal. **c,** Mo 3*d* spectrum of mechanically exfoliated crystal after a 10-seconds of mild ion gun treatment. Additional defective peak is observed due to damage. **d,** Mo 3*d* spectrum of CVD grown MoS_2. **e,** S 2*p* spectrum of CVD grown MoS_2. The CVD sample shows a higher binding energy compared to the mechanically exfoliated sample due to electron doping.

The XPS results of CVD grown MoS_2 are shown in **Figure 4.15d** and **e**. The binding energy values for Mo 3*d* and S 2*p* doublets are located at 229.8 eV (Mo $3d_{5/2}$) and 162.6 eV (S $2p_{3/2}$), respectively. The binding energy of CVD sample is 0.5 eV higher than for the exfoliated crystal, indicating significant electron doping in the CVD sample. This is consistent with PL/Raman results discussed in the previous section.

4.2.3 Cross-section STEM

To observe the atomic structure of the metal- semiconductor interface, cross-section STEM imaging was used to examine the interface. This section describes the sample preparation methodology that was developed to obtain atomic resolution images.

The cross-section specimens were prepared by focused ion beam (FIB, FEI Helios NanoLab 450). Specimen preparation process is shown schematically in **Figure 4.16**. The side view of metal contact on MoS_2 on SiO_2/Si substrate is shown in **Figure 4.16a**. To begin, a thin layer of protective platinum (Pt) is deposited on top of area to be imaged. Then the sample is placed in the FIB and etched using 30 kV Ga ions, as shown in **Figure 4.16c**. The sample is tilted during the ion milling so that preferential etching is achieved and T shape is obtained. The tilting process shown **Figure 4.16d** and **e** are repeated until the bottom section of the sample can be separated from the substrate. This process allows specimen to be thinned down to less than 100 nm. Subsequently, lower energy (5 keV, 2 keV, and 1 keV) Ga ions are used to remove damaged surface layers. The image plane is labeled in **Figure 4.16f**. **Figure 4.16g** shows the top view SEM image of a FET device in which the MoS_2 triangle is clearly seen along with the metal electrodes on top. The device with protective Pt layer is shown in **Figure 4.16h**. **Figure 4.16i** shows the completed specimen, with the white contrast zone indicating the image region.

The cross-section specimen must be as thin as possible to obtain crisp atomic structure images. However, getting a very thin sample is challenging since the milling procedure can easily destroy it. Another critical factor for obtaining clear atomic images is selecting the right imaging zone axis. **Figure 4.17** illustrates how the image axis affect the imaging results using a simple simulation based on two layers of MoS_2 with 20 by 20 unit cells. The top view of the bilayer MoS_2 is shown in **Figure 4.17a** (view from *c* axis, blue arrow in the figure). The side view is acquired by observing from *a* axis (red arrow in the figure), as illustrated in **Figure 4.17b**. When viewing along the *a* axis, all 20 Mo atoms aligned perfectly in one dot. As a result,

the contrast in STEM of one MoS_2 unit (red rectangle) comes from the signal of 20 unit cells added together. If the image angle misaligned by 1 degree, the side view of each atom becomes

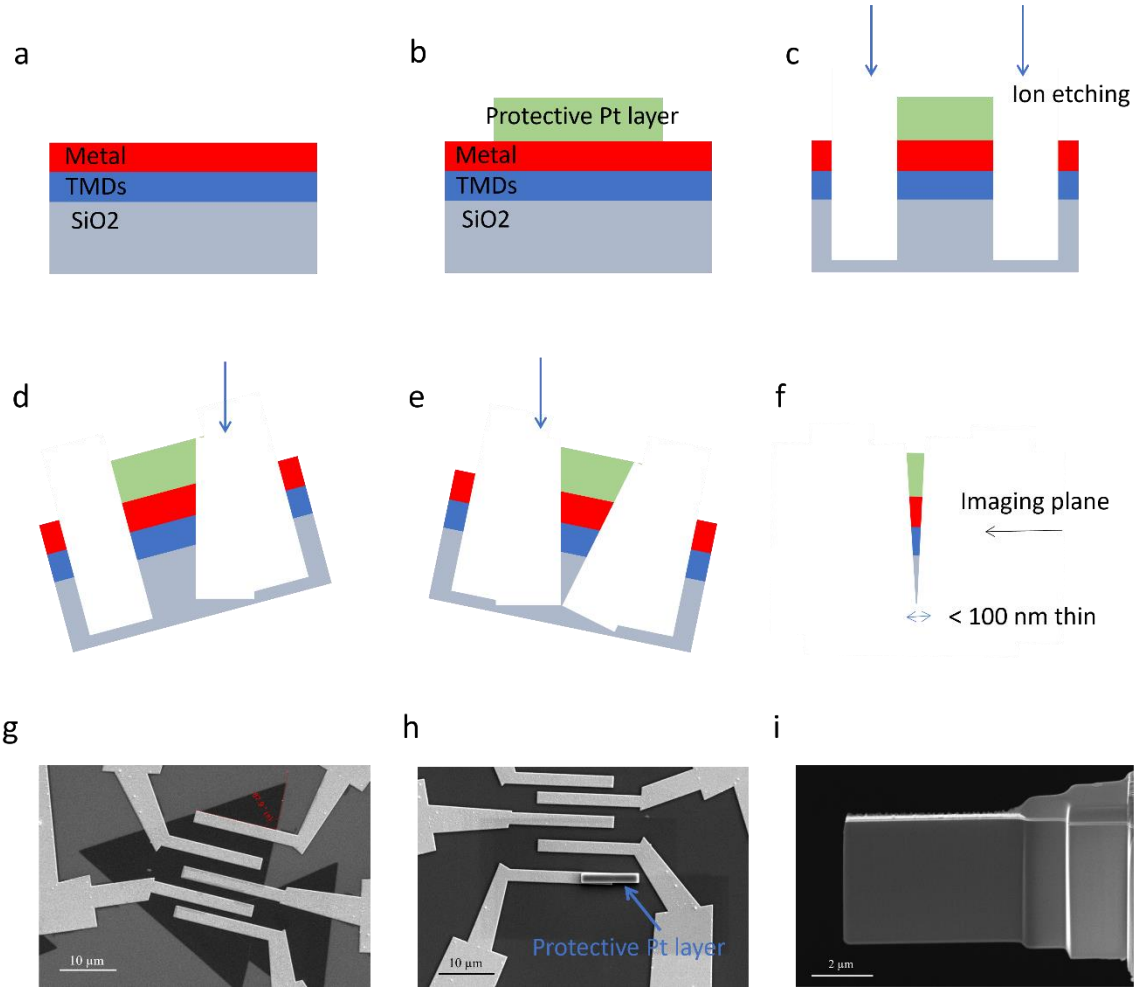


Figure 4.16 Schematic of FIB process for preparing cross-section STEM sample. **a,** Side view of the metal-TMD on SiO_2 substrate. **b,** Pt deposition on top of region to be imaged. **c,** Ion milling step to remove bulk region around the chosen area. **d, e,** Ion milling during tilting to make T shape structure. **f,** Repeating steps **d** and **e**, the specimen can be thinned down to less than 100 nm for imaging. The imaging plane is indicated by the arrow in the figure. **g,** SEM image of a device for FIB. **h,** Pt layer (indicated by the arrow) deposited on the chosen region. **i,** SEM image of a completed FIB sample.

blurry, as illustrated in **Figure 4.17c**. If the image angle is off by 2 degrees, the atoms in the side view become jumbled together, making it impossible to distinguish each one (**Figure 4.17c**). These simulations use just 20 unit cells along the *a* axis (less than 10 nm), but the real FIB samples are about 100 nm. For atomic structure images, imaging from the right zone axis

without any mismatch is critical. As a result, the FIB sampling must carefully select the appropriate flake and angle. The *a* and *b* axes of a CVD grown sample with a triangular form are easily determined. Mechanically exfoliated flakes frequently possess random shapes. If the flake shows one straight line at the boundary, this line is usually assumed to be the *a* axis orientation.

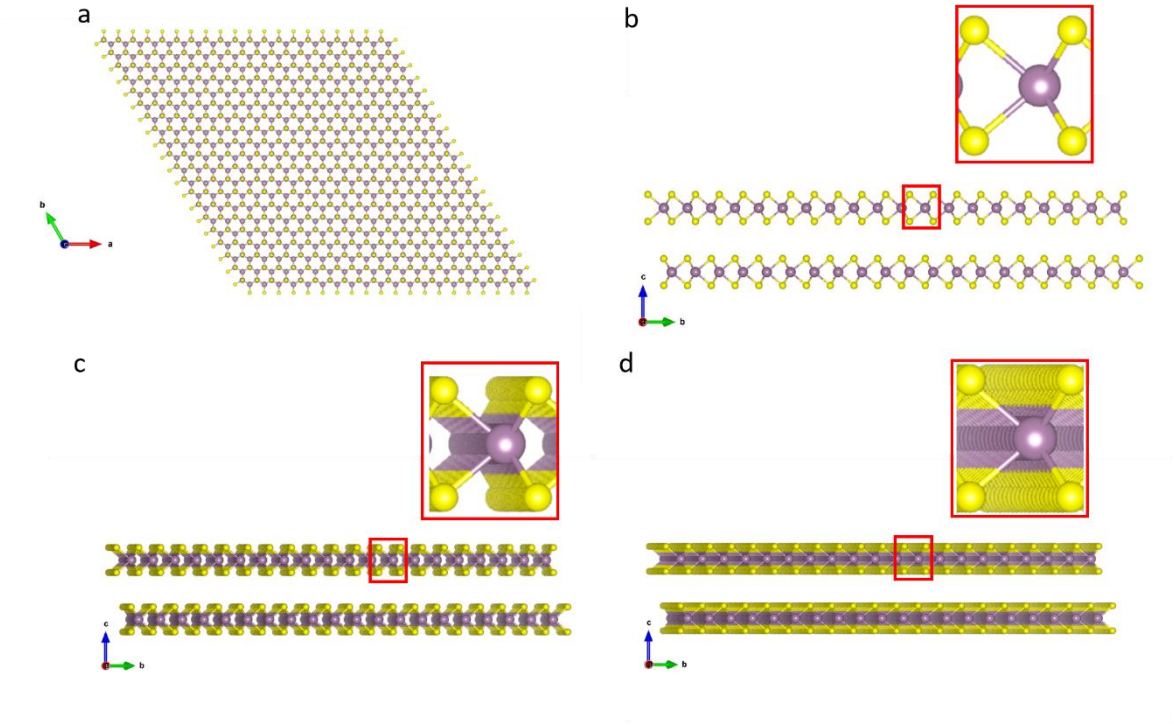


Figure 4.17 a, Top view from *c* axis of bilayer MoS_2 with 20 by 20 unit cells in each layer. **b,** Side view from *a* axis. The red rectangle is from zoomed in region in one layer, showing 20 Mo atoms aligned perfectly. **c,** Imaging from *a* axis with 1 degree misalignment. The atoms become blurred. **d,** Imaging from *a* axis with 2 degree misalignment. The atoms become indistinguishable.

4.3 Field effect transistors (FETs)

As part of the methods development part of my doctoral research, I have optimized lithographic processing to minimize contamination and damage to 2D TMDs. I summarize my findings in the following section.

Electron beam lithography (EBL) was used to make 2D TMD devices. The standard procedures of EBL are: spin-coating of the electron resist that acts as the mask for writing lithographic patterns on the substrate. We used e-beam resist MMA 495 EL6 and PMMA 495

A6 at 4000 rpm for 40s (MicroChem Inc., 495/950 represent molecular weights of 495,000 & 950,000 g/mol; A6 represents 6% of polymer in anisole, EL6 represents a concentration of 6% in solvent ethyl lactate). This was selected because I found that it offered ease of lift-off after metal deposition and because it left behind less residue on the TMDs as discussed in section 4.1.5. **Figure 4.18** illustrates the EBL process from coating by e-beam resist to exposure to development to metallization and lift-off.

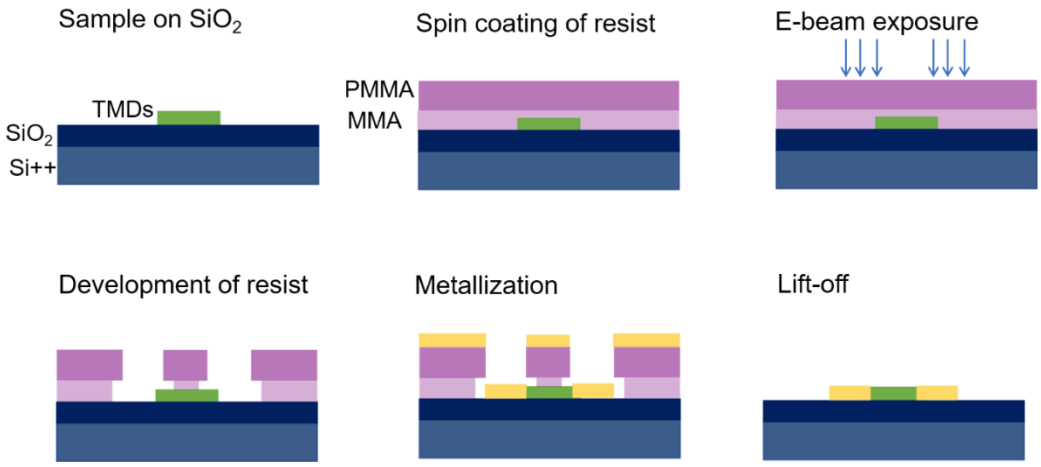


Figure 4.18 Standard E-beam lithography process used in this study.

As discussed in section 4.1.5, MMA leaves minimal residue on 2D TMDs after removal with acetone. I also evaluated MMA/PMMA resist exposed under different electron beam dose energies to study differences in surface contamination. To do this, six strips were written on one mechanically exfoliated flake with dose energies ranging from 300 to 800 µC/cm^2 (50 keV, 1 nA, 500 µC/cm^2 was used for writing). The optical image of the sample after development of

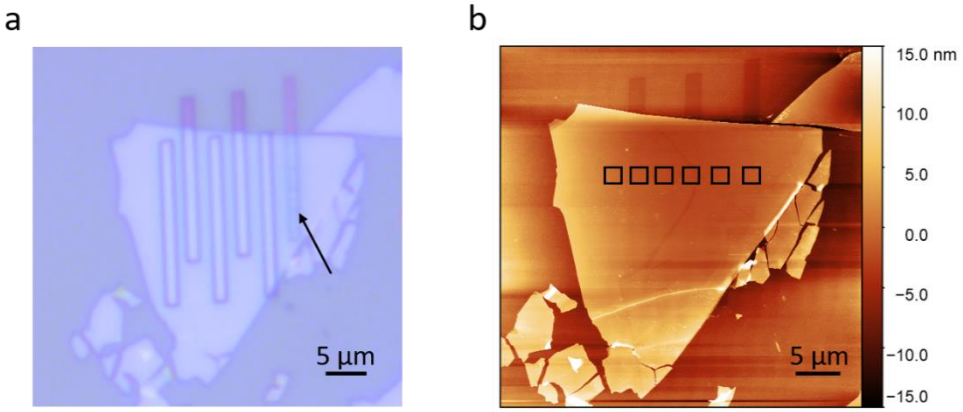


Figure 4.19a, Optical microscope image of strips written by e-beam lithography after development. **b**, Average roughness ranged from 0.295 to 0.336 nm. This is further confirmation that negligible residue is left on MoS_2 when MMA is used.

resist is shown in **Figure 4.19a**. For 300 μC/cm^2 exposed strip on the right (indicate by the black arrow), the strip clearly shows unremoved resist due to underexpose. The AFM image of the sample after MMA/PMMA removal in acetone is given in **Figure 4.20b**. The strips on the SiO_2 can be seen but no clear contrast is observed on the MoS_2 flake. In the squares labelled in **Figure 4.19b**, the average roughness ranged from 0.295 to 0.336 nm. This is further confirmation that negligible residue is left on MoS_2 when MMA is used.

Chapter 5 Clean van der Waals Contacts for N-type 2D TMD FETs

This Chapter describes how different metals affect the performance of 2D TMD FETs. I have achieved ultraclean van der Waals (vdW) contacts[1] on CVD grown monolayer MoS_2 using indium that show good device performance (low contact resistance, high mobility, and high drain current). Furthermore, FETs based on other TMDs such as WS_2, NbS_2 and WSe_2 are also demonstrated with indium contacts to achieve low contact resistance. Other soft metals such as Ga and Ag are also investigated as contacts for 2D TMDs. Finally, the effect of annealing on the formation of alloys between indium and capping layers is investigated for potential tuning of Schottky barrier height by work function engineering.

5.1 Device structure and measurements

FETs: Most devices discussed in this work are bottom gate and top contact FETs. The device structure is shown in **Figure 5.1a**. Heavily doped silicon was used as the gate electrode and SiO_2 as the insulator. To characterize the FET properties, we measured the transfer curve by applying a fixed drain voltage and sweeping the gate voltage. A typical transfer curve is shown in Figure 5.1b, plotted in both linear (black) and logarithmic (blue) forms. The threshold voltage is extracted at gate voltage axis intercept of the linear extrapolation of the transfer curve at its maximum first derivative point (dashed line in **Figure 5.1b**). Output characteristics were measured by applying fixed gate voltage and sweeping the drain voltage at each gate voltage step (**Figure 5.1c**). Ideal output characteristics should possess linear and saturation regimes as shown in the Figure. Non-ideal output characteristics exhibit non-linearity due to poor contacts and absence of saturation due to poor electrostatics. The drain current in FETs is given by[7]:

$$I_D = \mu C_{ox} \frac{W}{L} (V_G - V_T) V_D, \qquad \text{when } V_D \ll V_G - V_T, \textit{linear region}$$

$$= \mu C_{ox} \frac{W}{2L} (V_G - V_T)^2, \text{ when } V_D > V_G - V_T, \textit{saturation region} \qquad (5\text{-}1)$$

where μ is the mobility of carriers, C_{OX} is the capacitance of the gate insulator ($C_{OX} = \varepsilon_0\varepsilon_r/d$, ε_0 is permittivity of vacuum, ε_r is dielectric constant of the insulating layer and d is the thickness of the insulating layer), W is the width of FET channel, L is the FET channel length, V_G is the

[1] Ultraclean van der Waals contacts: No physical damages caused by metal depositions and no chemical reactions occur at the contacts.

gate voltage, V_T is the threshold voltage, and V_D is the drain voltage. Mobility of the FET channel material can be extracted from the transfer curves using the following equation:

$$\mu = \frac{g_m L}{V_D C_{ox} W} \tag{5-2}$$

The maximum transconductance, g_m, is extracted from the largest slope value of the transfer curve:

$$g_m = \frac{\partial I_D}{\partial V_G} \tag{5-3}$$

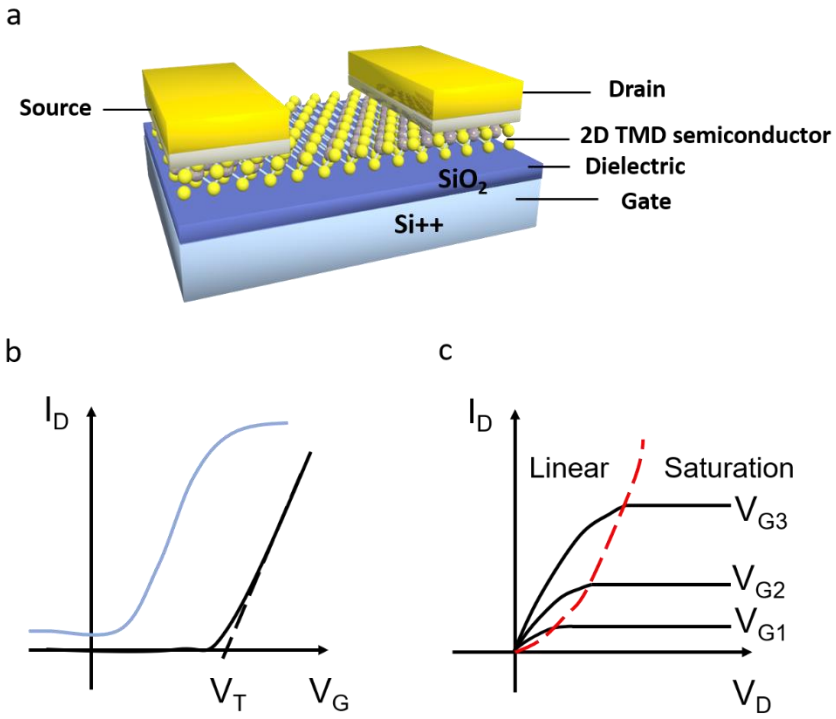


Figure 5.1 a, Schematic of a bottom gate field effect transistor structure. **b,** Typical transfer curves of FETs plotted in both linear and logarithmic (blue) forms. V_T is determined by extrapolation of linear region of transfer curve to the gate voltage axis as indicated by the dashed line. **c,** Typical output curves of FETs. The left side of the red dashed curve is the linear region of the output characteristics and the right side is the saturation region.

Contact resistance: The resistance at the contact (R_C) leads to a potential drop at the metal-semiconductor junction, which in turn increases the drain bias required to drive the charge carriers through the semiconductor. The value of R_C can be extracted using the Y-function[185], four-probe[186] or the transfer length methods (TLM)[187]. The TLM is used in this thesis to extract contact resistance as it is less dependent on the device structure. The V_G dependent contact resistance can be extracted by TLM using devices with different channel lengths (**Figure 5.2a**).

In TLM, the total resistance between source/drain electrodes and semiconductor is obtained by measuring the resistance at different channel lengths (L). The total resistance of the device (R_{total}) is given by:

$$R_{total} = \frac{R_{SH}L}{W} + 2R_C = \frac{R_{SH}}{W}(L + 2L_T) \quad (5\text{-}4)$$

Plotting R_{total} versus the channel length allows the extrapolation of the data to the y-axis intercept, which is equal to $2R_C$. The intercept at x-axis is $2L_T$ (transfer length) and the slope is the channel sheet resistance, R_{SH}. In this geometry, the contact length is kept constant and larger than the transfer length. The charge injection from the metal contact into the semiconductor does not occur uniformly over the entire contact length. Instead, current flow at the metal semiconductor interface occurs over a small active contact length, which leads to current crowding under the contact that gives rise to specific contact resistivity[188] (**Figure 5.2b**).

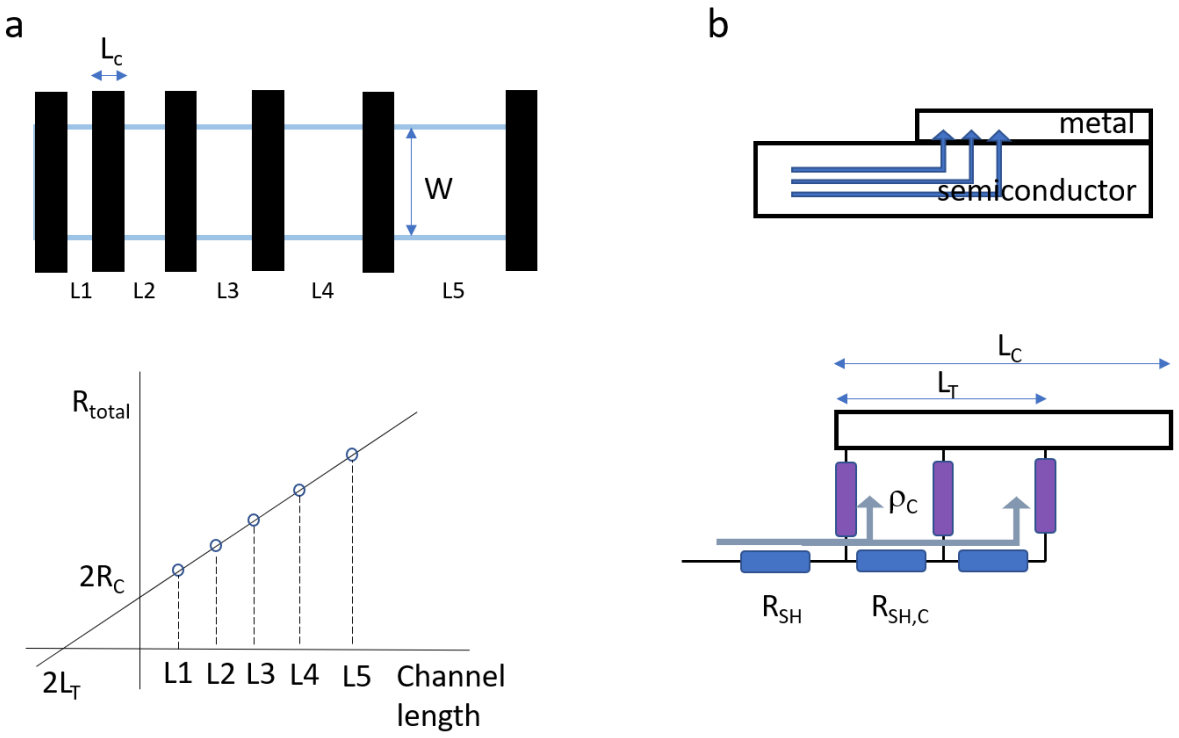


Figure 5.2 a, TLM structure for contact resistance measurements. The total resistance between source and drain is measured for various contact channel lengths and plotted versus the channel length in the plot below. The intercept at x-axis is $2L_T$ and the intercept at y-axis is $2R_C$. **b,** Current transfer from semiconductor to metal contact and the equivalent circuit with current encountering interfacial contact resistivity and sheet resistance under the contact.

The voltage distribution and contact resistance can be extracted from a distributed resistive network model[189,190] using the following equations:

$$V(x) = \frac{I\sqrt{R_{SH-C}\rho_c}}{W} \frac{\cosh[(L-x)/L_T]}{\sinh(L/L_T)} \quad (5\text{-}5)$$

$$R_C = \frac{\sqrt{R_{SH-C}\,\rho_c}}{W} \coth\left(\frac{L}{L_T}\right) = \frac{\rho_c}{L_T} \coth\left(\frac{L}{L_T}\right) \quad (5\text{-}6)$$

where $R_{SH\text{-}C}$ is contact resistance under the metal contact and ρ_C is the interface specific resistivity. $L_T = \sqrt{\frac{\rho_C}{R_{SH-C}}}$ can also be considered as the distance over which most of the current is transferred from the semiconductor to the metal. By assuming the sheet resistance under the contact is the same as the channel, the interface specific resistivity can be extracted.

5.2 Metal contacts on 2D TMDs

Two dimensional TMDs such as molybdenum disulfide (MoS_2) have been demonstrated to be excellent semiconductors for ultra-thin FETs[9]. Titanium (Ti) and Gold (Au) are widely used as metal contacts for TMDs[191,192] and unusually high contact resistance has been observed. At the beginning of my doctoral research, I fabricated FETs with Ti and Au contacts to study the origins of the high contact resistance. Typical transfer curves, output characteristics and contact resistances of MoS_2 FETs with Ti and Au electrodes are shown **Figure 5.3**. The transfer and output characteristics of Ti contacted MoS_2 FETs are shown in **Figure 5.3a** and **b**. The I_D-V_D curves are non-linear, which indicates non-ohmic characteristic for Ti contacts. This phenomenon is widely observed in literatures and it indicative of severe Fermi-level pinning at the contacts[193,194]. Ti/MoS_2 interface has been studied with XPS by McDonnell *et al.*[184] Their results showed that titanium reacts with MoS_2 to form TixSy and metallic Mo at the interface. We further studied the Ti/MoS_2 interface using atomic-resolution STEM and EELS. An atomic-resolution STEM image of the Ti/MoS_2 interface shown in **Figure 5.4a** indicates that the topmost MoS_2 is barely identifiable due to the reaction at the interface. The EELS spectra on the right compared the S $L_{2,3}$ edge between topmost MoS_2 indirect contact with Ti and fifth layer MoS_2 where the S is considered pristine. The peak at around 175 eV is absent for the topmost layer MoS_2, indicating the electronic structure of the top layer MoS_2 is changed by depositing Ti on top of it. I also made devices on CVD grown monolayer MoS_2 with Ti contacts, but most of them failed owing to contact damage. The cross-sectional STEM image and the corresponding elemental mapping of Au, Ti, and Mo are shown in **Figure 5.4b** and **c**. It can be

seen from Mo mapping that the Mo distribution is not uniform due to diffusion from Ti into the semiconductor.

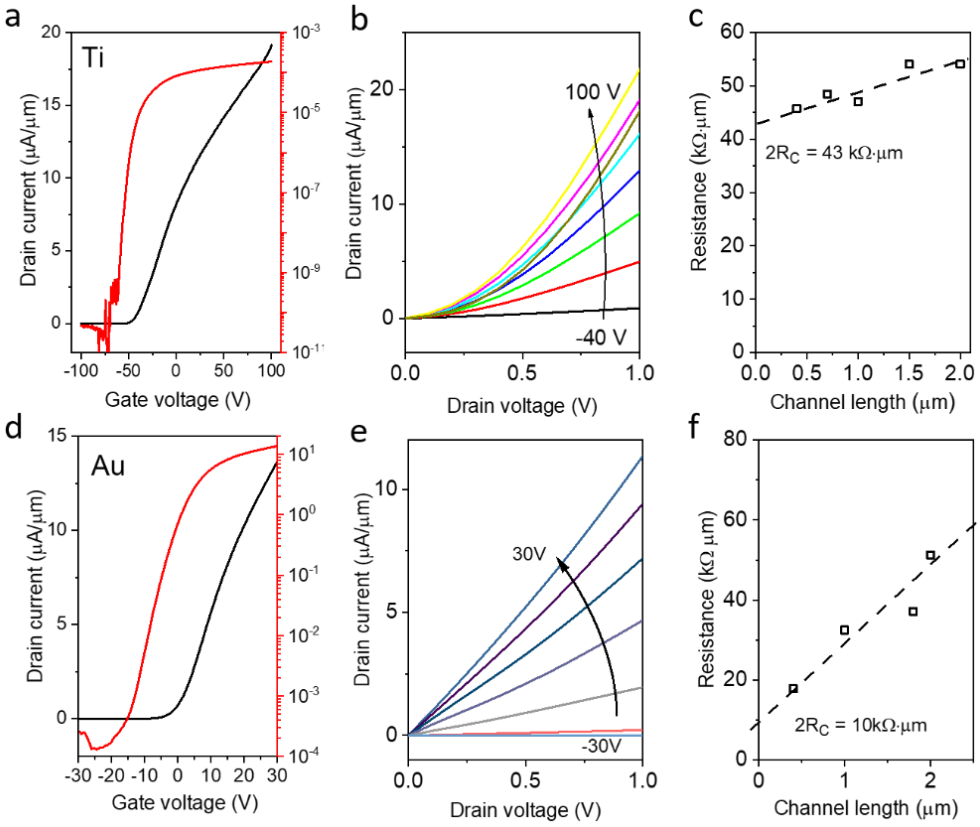


Figure 5.3 a-c, Typical transfer curve, output performance and contact resistance results of Ti contacted multilayer MoS_2 FET. W/L = 10μm/2μm. **d-f,** Typical transfer curve, output performance and contact resistance results of Au contacted multilayer MoS_2 FET. W/L = 8μm/3μm. Drain voltage = 1V for the transfer curve measurements.

The mobilities of FETs extracted from transfer curves (**Figure 5.3a** and **d**) by applying **equation 5-2**, Ti and Au contacted devices were 10 and 28 $cm^2V^{-1}s^{-1}$, respectively. The contact resistances extracted by the TLM method for Ti and Au contacted MoS_2 FET were 21.5 kΩ·μm and 5 kΩ·μm, respectively. Although Au contacted MoS_2 devices showed much lower contact resistance compared to Ti contacted devices, studies by Duan's group[124] proved that Au deposition also introduced defects at the Au/MoS_2 interface due to the kinetic energy transfer during the deposition. Kim *et al.* have recently reported the fabrication of atomically clean metal/TMD contacts by evaporating metals at a relatively low thermal energy and cooling the substrate holder down to 100 K by liquid nitrogen during deposition[195]. However, they found that Au deposition still caused damage to the top two layers of MoS_2 even at 100 K deposition.

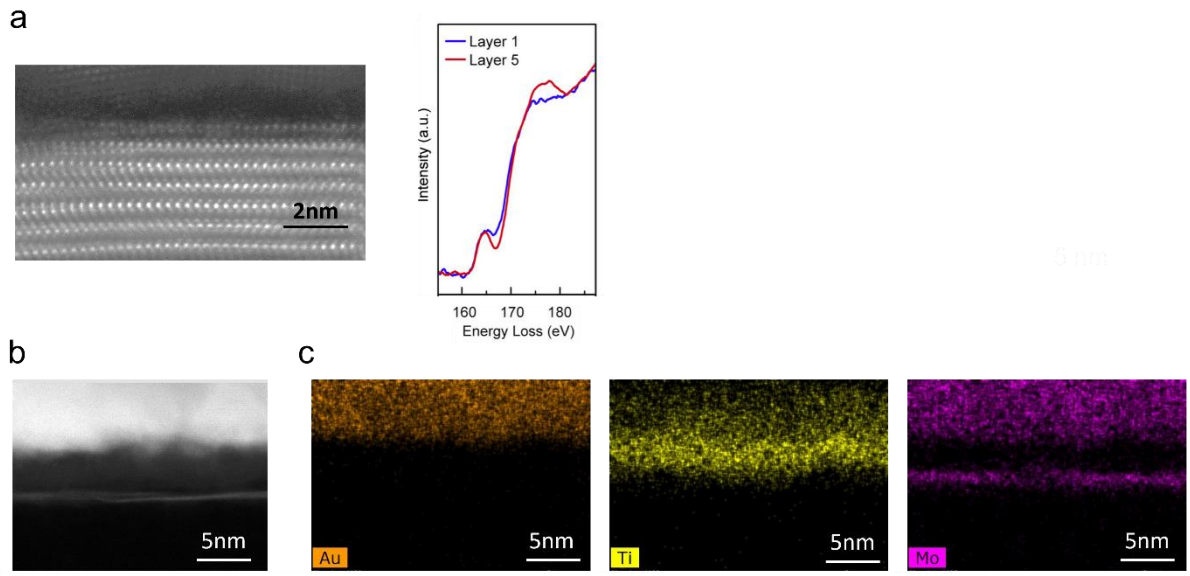


Figure 5.4 a, Atomic-resolution ADF-STEM image of the Ti-MoS_2 interface is shown on the left. EELS spectra on the right show S $L_{2,3}$ edge measured at the topmost layer and the fifth layers of MoS_2. The S L_2 and L_3 peaks were found at 165 and 178 eV. The S edge spectra of MoS2 from first layer showed substantial difference from the fifth layer indicating the electronic structure of MoS2 changed after Ti depositing on top of it. **b,** Cross-section STEM image of Ti metal on monolayer MoS_2 showing that the monolayer is damaged by the metal contact. **c,** Elemental mapping of Au, Ti and Mo showing nonuniform distribution of Mo atoms due to Ti diffusion into the MoS_2 layer.

Criteria for making good contacts on 2D TMDs

As described in Chapter 3, Fermi level pinning can arise from several factors in 2D TMD-metal contacts. The first step in making good metal contacts for 2D TMDs is to avoid highly reactive metals. In general, if the enthalpy of metal sulfide formation is negative, then the sulfur will react with the deposited contact metal. While formation of metal-semiconductor alloys at the interface is beneficial in some cases for bulk semiconductors (e.g. silicides[195]), it is detrimental for 2D materials. Second, the quality of as synthesized TMDs must be improved to minimize the intrinsic defect density. Additional doping from the environment (adsorbed layers and charges from substrate) should be minimized. Third, metal evaporation conditions must be closely controlled. For example, choosing low vaporization temperature metals, using indirect evaporation to minimize kinetic damage to 2D semiconductor, ensuring low deposition temperature and employing ultra-high vacuum conditions to minimize trapping of adsorbed molecules in the junction. Fourth, the influence of lattice mismatch on the electronic property of 2D TMDs should be considered. Fifth, sources of metal-semiconductor interface dipoles that

can dramatically change the metal work function must be controlled. These considerations must then allow for contacts with the work functions that match the conduction band of the 2D semiconductor for electron transport and the valence band for hole transport.

The important parameters that affect the interface between metals and the 2D TMDs are work function of the metal, kinetic energy of metal deposition, and the reactivity of the metal with TMDs. The work function versus the vapor temperature of different metals at two vacuum conditions are given in **Figure 5.5**. It can be seen that indium has the lowest vapor temperature and its work function is very close to the conduction band of MoS_2[196]. Indium has been reported as an electrode to passivate and dope cadmium selenide nanocrystal channel transistors. We therefore chose to investigate very gentle deposition of indium on 2D TMDs to potentially realise pristine interface. To do this, we first deposited 10 nm of indium on the 2D TMDs. We capped this indium layer with 100 nm of Au layer to protect the soft indium from oxidation and damage. We, therefore, refer to these contacts as In/Au.

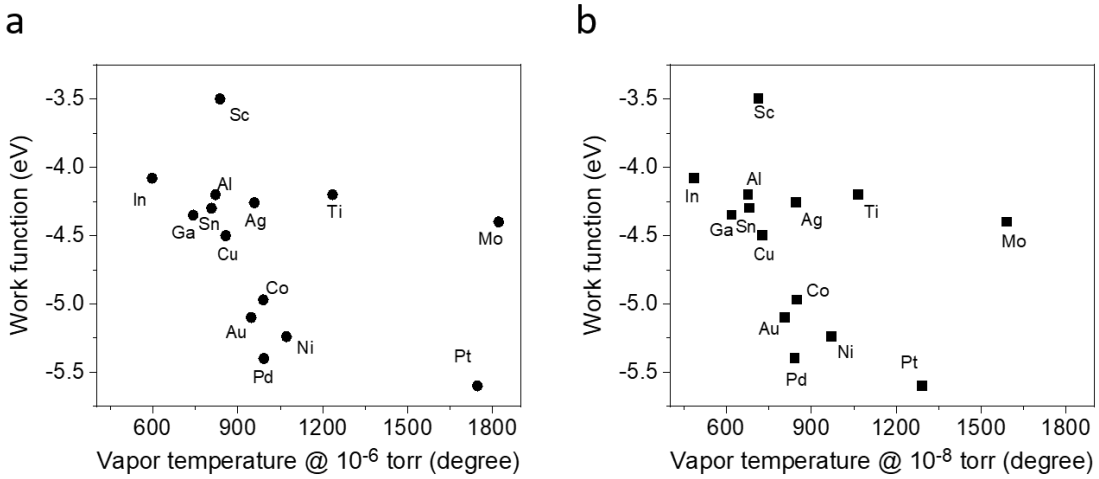


Figure 5.5 a, Work function and vapor temperature of different metals at 10^{-6} torr vacuum condition. **b,** Work function and vapor temperature of different metals at 10^{-8} torr vacuum condition. (Data from Kurt J. Lesker[197]).

5.3 Clean van der Waals contacts for MoS_2

5.3.1 Indium contact characterisation

Here, I describe my work on realising clean vdW contacts on TMDs based on indium (In). We began by depositing indium on 2D MoS_2 using electron beam evaporation. We used a very low deposition rate of 0.3 Å/s and base vacuum of less than 10^{-6} Torr. The aim was to deposit In in the gentlest way to impart minimum kinetic or thermal energy to the evaporated atoms. To

characterise the interface chemistry of the In/MoS_2, we conducted XPS study on the contacts. The XPS measurement was done with 3 nm In deposited on MoS_2 crystal and the sample was transferred to XPS chamber without exposing in air. The binding energy values for the Mo 3*d* and S 2*p* doublets were found to be 229.3 eV (Mo $3d_{5/2}$) and 162.1 eV (S $2p_{3/2}$) – typical of pristine MoS_2[197]. Nonstoichiometric Mo_xS_y peaks were not observed, as indicated as blue region in **Figure 5.6a** and **b**. Chemical state of the interface is provided in the form of In 3*d* spectra and In MNN Auger measurements in **Figure 5.6 c** and **d**. XPS of In 3*d* spectra shows In metal $3d_{5/2}$ (443.8 eV) and $3d_{3/2}$ (451.4 eV) peaks along with In metal loss features. X-ray induced Auger spectrum showing pristine In metal peak at 402.9 eV. In_2O_3 has a clear peak at 400.2 eV, which is absent in our samples. There is no sign of In_2S_3 (407.3 eV)[197] and In MNN

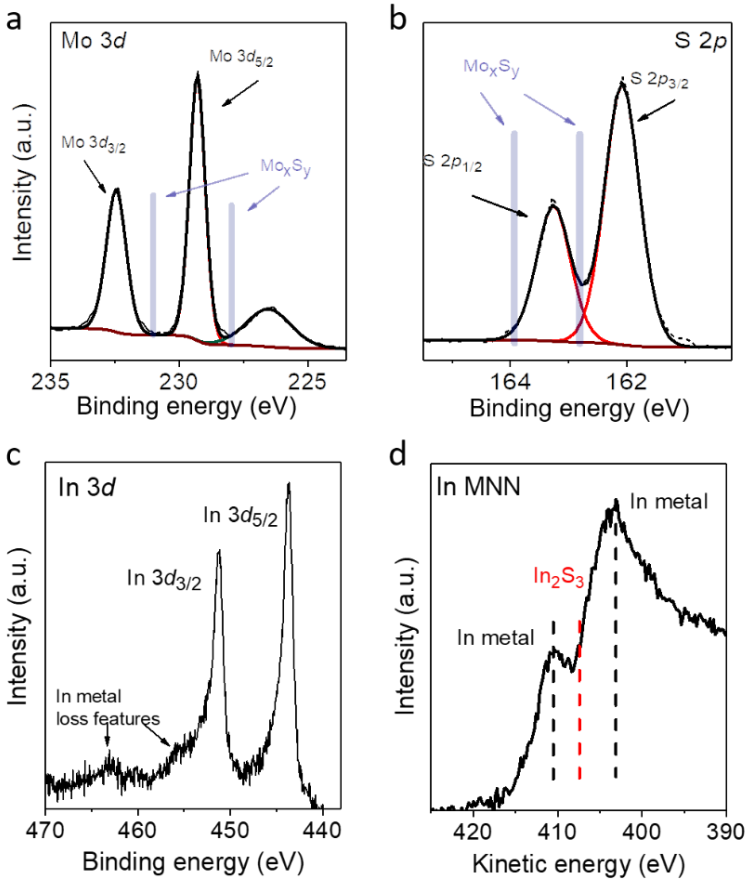


Figure 5.6 a, XPS of In-MoS_2 interface showing Mo 3*d* doublets. **b,** XPS of In-MoS_2 interface showing pristine S 2*p* doublets. The absent of Mo_xS_y peaks at the blue line positions indicate the interface is free of intermediate states due to chemical reaction. **c,** XPS of In-MoS_2 interface shows In metal $3d_{5/2}$ (443.8 eV) and $3d_{3/2}$ (451.4 eV) peaks along with In metal loss features. **d,** X-ray induced Auger spectrum showing pristine In metal peaks.

Auger spectra indicates no chemical reaction at the interface. The XPS results prove that the deposition of In does not modify the MoS_2 or create any new chemistry at the interface. Because In metal oxidizes when exposed to air, unless otherwise indicated, the contact metals utilized for devices in this thesis are thin In (~ 10 nm) capped with Au (~ 80 nm). All the devices are annealed at 200 °C in Ar/H_2 atmosphere before measurements. The effect of the annealing will be discussed in section 5.5.

To image the In/MoS_2 interface at atomic resolution, we conducted cross-sectional annular dark field scanning transmission electron microscopy (ADF STEM) study on the device contact. In contrast to the Ti/MoS_2 interface analysis in **Figure 5.4**, the In/MoS_2 interfaces shown in **Figure 5.7a** for few layered MoS_2 are atomically sharp with no detectable evidence of reaction between the In metal and molybdenum disulfide layers. ADF STEM and intensity profile in **Figure 5.7b** of In/Au contact to multilayer MoS_2 shows that the MoS_2 interlayer distance is 6.2 Å, sulfur to sulfur distance between two layers is 2.7 Å and the interface metal to first layer sulfur distance is also ~ 2.7 Å, indicating van der Waals contact at the interface. The EELS was measured using a focused electron beam probe with spatial resolution of ~ 0.8 Å so that the spectra from highly localized regions at the interface could be obtained. The S L_2 and L_3 peaks were found at 165 and 178 eV[198]. Since the S $L_{2,3}$ edge arises from the transition of $2p$ ($2p_{1/2}$ and $2p_{3/2}$) core electrons to unoccupied $3d$ states, the spectroscopic profile would be sensitive to the local bonding environment. The electronic band structure of the first layer MoS_2 will change if MoS_2 reacts with In/Au. It can be seen that the sulfur $L_{2,3}$-edge exhibits

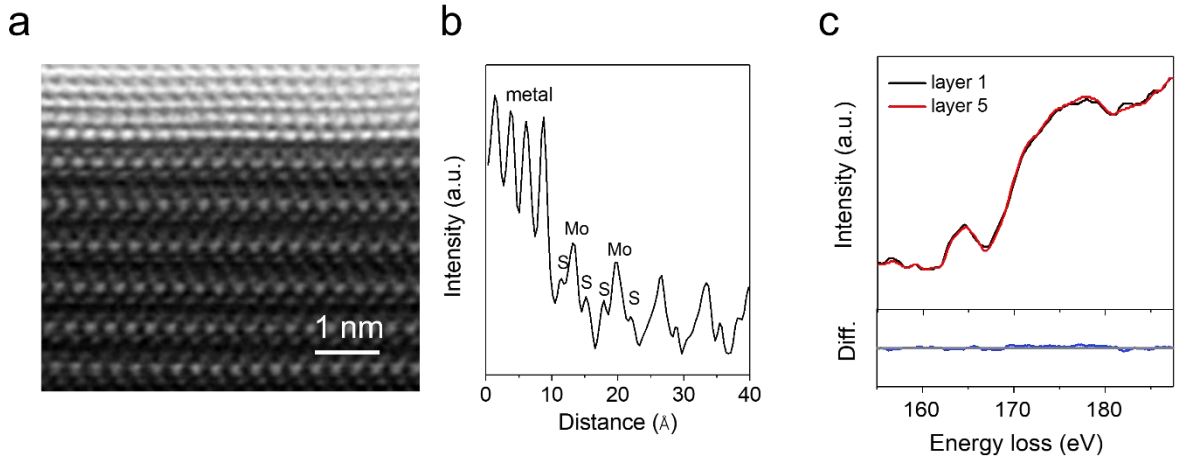


Figure 5.7 a, Atomic resolution ADF- STEM images of In/Au on multilayer MoS_2. **b,** Intensity profile of In/Au contact to multilayer MoS_2. **c,** EELS spectra of S $L_{2,3}$-edge showing that the sulfur atoms of the top layer are completely unaffected by the deposition of In on top.

experimentally negligible difference between the topmost MoS_2 layer in contact with the indium metal and the fifth layer of MoS_2 – suggesting the deposition of indium does not introduce any chemical reactions, distortions, or strain at the metal/semiconductor interface or within the 2D MoS_2.

5.3.2 Device performance with clean contacts for multilayer MoS_2

The transfer and output characteristics of multilayer MoS_2 FET with In/Au contacts are shown in **Figure 5.8a** and **b**. The transfer curve shows good ON/OFF ratio and high current density. The output curve at room temperature shows that the highest current density is 196 μA/μm at drain voltage of 3 V and gate voltage of 40 V. More importantly, the output characteristics at low temperature (**Figure 5.8c**) also shows linear output characteristics indicating the absence of a contact barrier with In/Au contact. The device was further measured at different temperatures to extract the Schottky barrier height (SBH). The transfer curve in **Figure 5.8d** clearly shows thermionic emission regime where the current increases with higher temperature and the tunnelling regime where the drain current tends to saturate. The SBH is extracted by making use of the distinctly different temperature dependences of the thermal transport (charges going 'over' the barrier) and tunneling (charges going 'through' the barrier) dominated regimes of the FET transfer characteristics. The thermionic current-voltage relationship of a Schottky barrier diode is given by[7]:

$$I = AA^*T^{\alpha}e^{-\frac{q\emptyset_B}{kT}}\left(e^{\frac{qV}{nkT}} - 1\right) \tag{5-7}$$

where A is the contact area, $A^* = 4\pi qk^2m^*/h^3$ is the Richardson constant, α is related to the contact structure (α = 1 for planar charge injection and α = 3/2 for sideways charge injection[199]), $\emptyset_B$ is the Schottky barrier height, n is the ideality factor, k is Boltzmann constant and T is temperature. An Arrhenius relationship is obtained from this equation:

$$ln(I_D/T^{\alpha}) = \ln(AA^*) - q(\emptyset_B - V/n)/kT \tag{5-8}$$

when $V \gg kT/q$ at different gate voltages. The barrier height is extracted from the slope of the Arrhenius plot in which the logarithm of the drain current is plotted as a function of inverse of temperature at different gate biases. The extracted barrier height versus gate voltage is plotted in **Figure 5.8e**. The real Schottky barrier height can then be determined at the flat band (V_{FB}) condition by adjusting the gate bias ($V_G = V_{FB}$). For gate values below V_{FB}, $\emptyset_B$ changes linearly with the gate voltage since the drain current is due to thermal transport. For $V_G > V_{FB}$, thermal assisted tunneling is reached and the dependence is no longer linear. This transition point is the

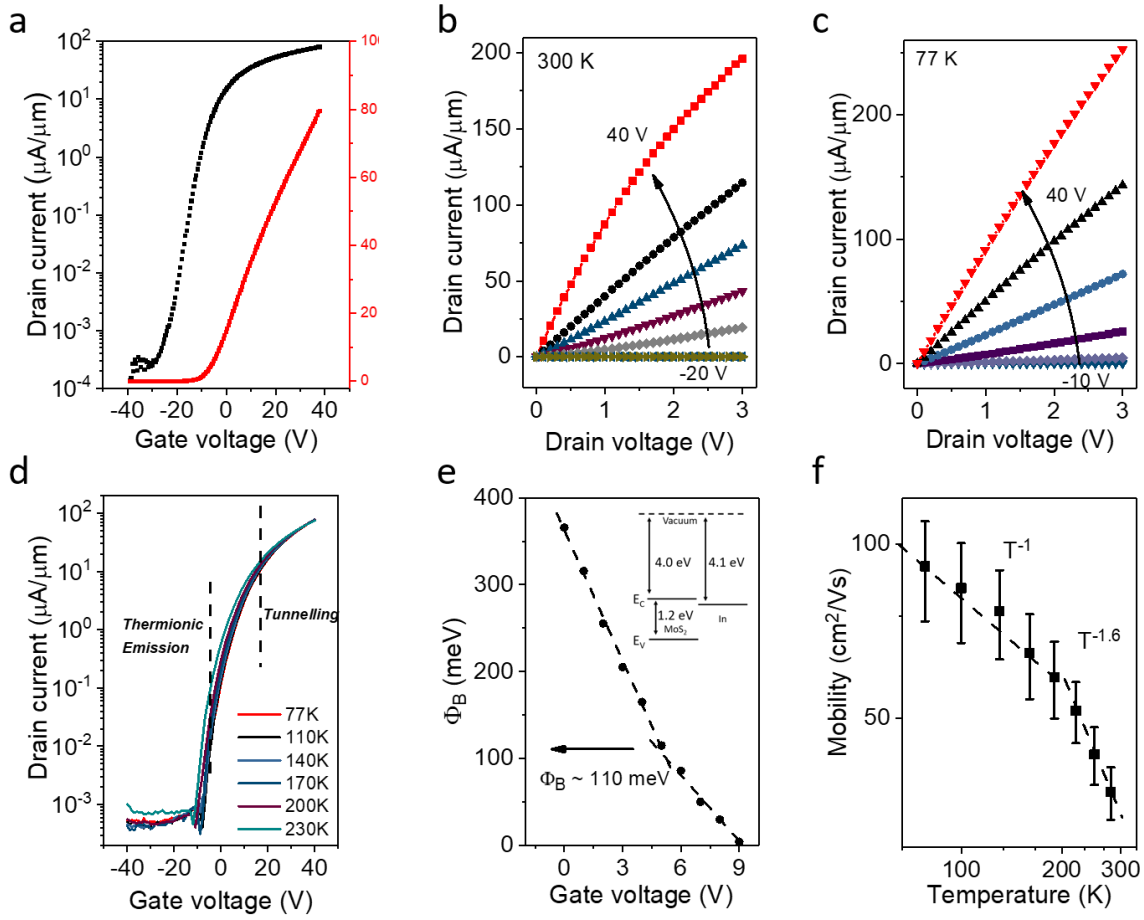


Figure 5.8 a, Typical transfer curves for MoS_2 FET with In/Au contact at room temperature. **b,** Output curves at room temperature show that the highest current density that was obtained is 196 μA/μm. **c,** Output characteristics at low temperature (77 K). Linear output characteristics indicate low contact barrier. **d,** Transfer characteristics of MoS_2 FET at different temperature showing metal-insulator transition at gate voltage of 35V. **e,** Schottky barrier extraction versus gate voltage. Inset shows energy bands of indium metal and MoS_2. **f,** Mobility versus temperature revealing phonon-limited property at low temperatures and acoustic phonon scattering at high temperatures.

true value of the Schottky barrier. The SBH extracted is around 110 meV for multilayer MoS_2 with InAu contact as shown in **Figure 5.8e**. This barrier height energy value is close to the difference between the Indium work function and the conduction band energy of MoS_2, which indicates the contact is free of Fermi level pinning. Measurements of mobility with temperature (**Figure 5.8f**) reveals that the phonon-limited mobility scales as $\mu \propto T^{-1}$ at low temperatures and as $\mu \propto T^{-1.6}$ at high temperatures because of acoustic phonon scattering[198].

The contact resistance of the In/Au contacted few-layered MoS_2 was extracted by the TLM method described in section 5.1. The results are plotted in **Figure 5.9a**. The contact resistance extracted is for In/Au contacts was found to be 800 **Ω**·μm for few layered MoS_2. As shown in **Figure 5.9b**, the contact resistance decreases with increasing carrier concentration for In/Au electrodes. The results of contact resistance of Sc, Ti and Au electrodes deposited in ultra-high vacuum (10^{-9} Torr) from the literature are included for comparison[9,187]. Comparison of contact resistance from literature for different types of electrode materials given in **Figure 5.9c** shows In/Au contacts possess the lowest contact resistance. Contact resistance of few-layered MoS_2

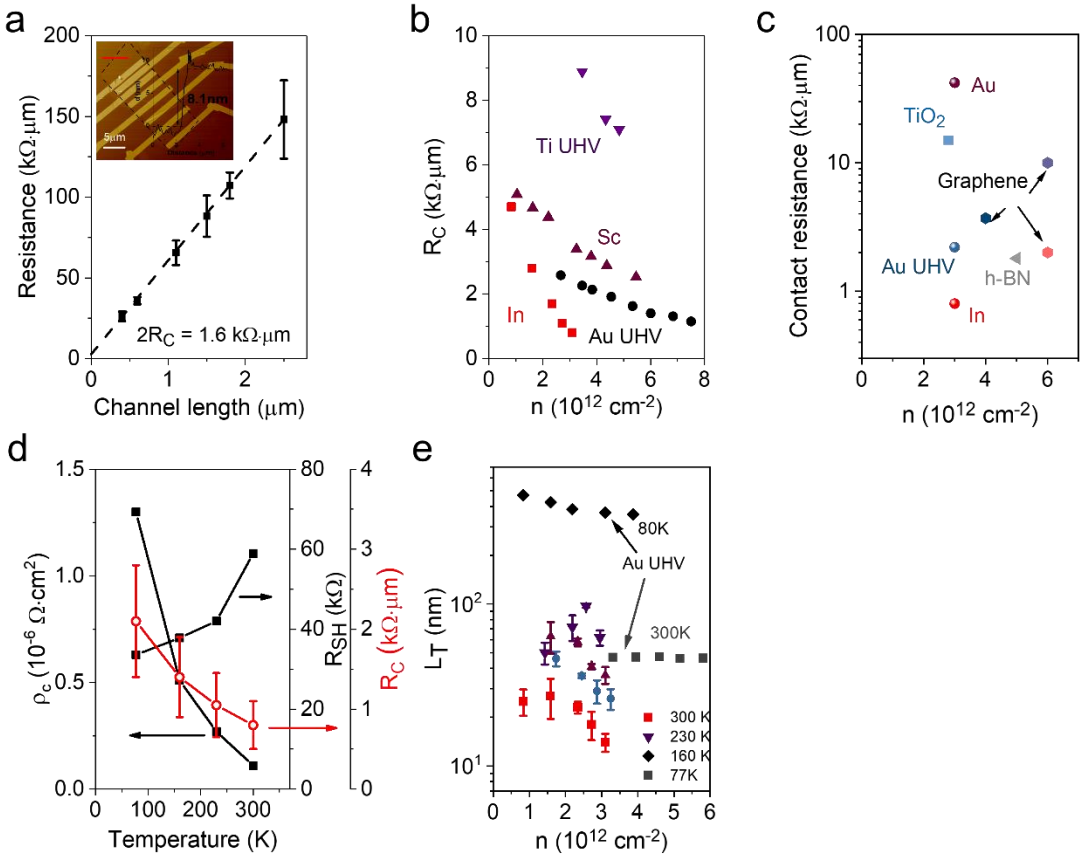


Figure 5.9 a, TLM results of In/Au contacted to few-layered MoS_2. Insert is the AFM image of the device. Scale bar is 5 μm. The error bars result from the averaging of least five measurements. **b,** Contact resistance versus carrier concentration for In/Au electrodes. Sc[9], Ti and Au electrodes deposited in ultra-high vacuum[187] (10^{-9} Torr) are provided for comparison. **c,** Comparison of contact resistance from literature and our results for different types of contacts[9,111,149,156,192,202]. **d,** Interfacial contact resistivity, sheet resistance and contact resistance versus temperature. **e,** Transfer length versus carrier concentration at different temperatures. Reported Au contacted MoS_2 results are included for comparison.

was extracted by TLM at different temperatures. **Figure 5.9d** shows that the contact resistance decreases with increasing testing temperature. The sheet resistance (R_{SH}) obtained from the slope of the TLM plot shows that R_{SH} increases with increasing temperature. This can be explained by the R_{SH} dependence of mobility: $R_{SH} = \frac{1}{nq\mu}$, where n is the carrier concentration, q is charge and μ is mobility. From **Figure 5.8f**, it can be seen that the mobility decreases with increasing temperature due to acoustic phonon scattering. Therefore, R_{SH} increases with increasing measurement temperature. The interfacial contact resistivity and transfer length can be further extracted from equation 5-6:

$$\rho_C = \frac{(R_C W)^2}{R_{SH}} \tag{5-9}$$

$$L_T = \sqrt{\rho_C / R_{SH}} \tag{5-10}$$

At 300 K the lowest effective contact resistivity is $\rho_C \approx 1 \times 10^{-7}$ Ω·cm^2 for In/Au contacts. This contact resistivity value is still one order of magnitude higher than Si[200,201]. ρ_C decreases with increasing T (**Figure 5.9d**) due to increased thermionic emission. The extracted L_T (**Figure 5.9e**) is 10 - 20 nm at 300 K, a relatively small value consistent with a large R_{SH} and small ρ_C. The contact length should be larger than this value to avoid current crowding at the contact. The transfer length rapidly decreases with rising temperature, as R_{SH} increases due to phonon scattering and ρ_C decreases from enhanced thermionic emission.

5.3.3 Performance of monolayer MoS_2 FETs with vdW contacts

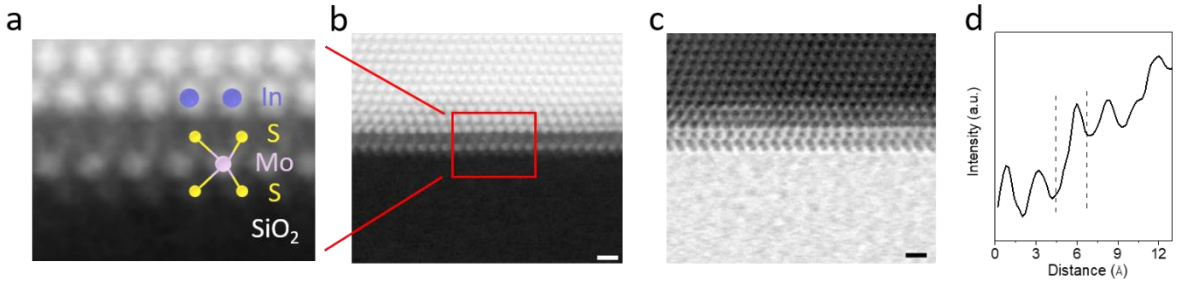


Figure 5.10 a, Atomic resolution images of In/Au on single layer MoS_2. **b,** Low-pass filtered annular dark field (ADF) STEM image showing Mo, S and In atoms as indicated by the enlarged image in figure a. Corresponding bright field (BF) STEM image of the monolayer. Scale bars = 5 Å. **c,** Bright field STEM of In/Au contact to monolayer MoS_2. **d,** The intensity profile shows that the interface metal to first layer sulfur distance is ~ 2.4 Å.

High performance FETs based on multilayer MoS_2 have been demonstrated with clean In contacts. This section will introduce clean contacts on CVD grown monolayer MoS_2. Atomic structure of the In/Au interface with monolayer MoS_2 was also studied by cross-sectional ADF STEM imaging. Unlike the Ti contacts on monolayer MoS_2 (**Figure 5.4b**), our analysis reveals that the In-MoS_2 interfaces for single layer MoS_2 is also atomically sharp with no detectable evidence of reaction between the indium metal and molybdenum disulfide layers. ADF and BF (bright field) STEM images in Figure **5.10b** and **c** clearly show the single layer MoS_2 and In/Au alloy contact on top with atomic resolution. The zoomed in interface is shown in **Figure 5.10a**. ADF intensity profile across the interface for In/Au on monolayer MoS_2 revealed that the spacing between the sulfur atoms and In/Au atoms is around 2.4 Å (**Figure 5.10d**) – indicating that the indium metal gently deposits on the 2D semiconductor.

Typical transfer and output curves for In/Au contacted single layer MoS_2 as the channel in FETs are shown in **Figure 5.11a** and **b**. The devices were fabricated on off-the-shelf thermal SiO_2 (300 nm) on Si and were not encapsulated. Despite this, the transfer characteristics exhibited sharp turn on and high current with mobility values reaching 167 $cm^2V^{-1}s^{-1}$. The TLM results shown in **Figure 5.11c** for indium electrodes on CVD grown single layer MoS_2 reveal contact resistance of ~ 3.3 kΩ·µm (at n = 5.0×10^{12} cm^{-2}). The higher contact resistance in single

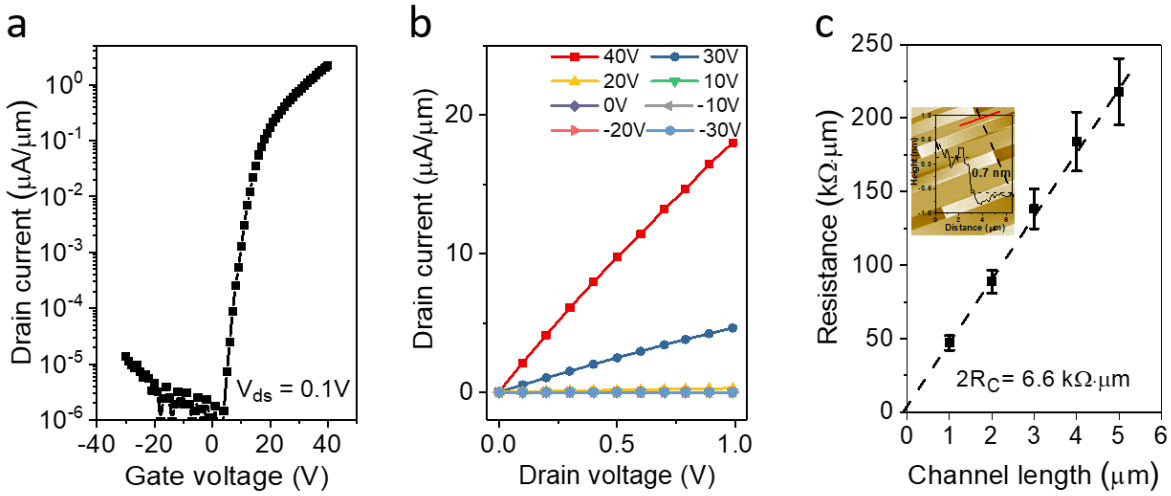


Figure 5.11 a, Typical transfer characteristics of a FET with monolayer MoS_2 as the channel and In/Au as the source and drain electrodes, length and width of the device are 2 and 6 µm. **b,** Linear output characteristics of In/Au contact indicating the absence of a contact barrier. **c,** Contact resistance of CVD grown monolayer extracted using the TLM. The error bars result from the averaging of least five measurements.

layer MoS_2 compared to the few-layered material can be attributed to substrate-carrier scattering that is more prominent in monolayers than multi-layers.

It is helpful to compare the experimental values with fundamental limits of contact resistance. The quantum contact resistance as a function of carrier concentration in the 2D semiconductor can be obtained by the Landauer approach[203] described briefly here. The current in a FET where carrier transport through the channel is ballistic[204] is given by:

$$I = \frac{2q}{h}\int T(E)M(E)\big(f_1(E) - f_2(E)\big)dE = \frac{2q}{h}\int T(E)M(E)\left(\frac{df_0}{dE}\right)qVdE \qquad (5\text{-}11)$$

where *h* is the Planck's constant, T(E) is the transmission probability, M(E) is the transmission modes for charge injection from metal contact into the channel, f(E) is the Fermi-Dirac distribution, *q* is unit charge and V is potential difference. The ideal maximum conductance (G) is given by:

$$G = \frac{2q^2}{h}T(E)M(E) \qquad (5\text{-}12)$$

For ultra-clean contacts on 2D TMDs, a vdW gap is present between the metal contact and the semiconductor. In such as a case, the maximum transmission probability (T_{max}) is obtained by assuming zero thermal barrier for tunneling through the vdW gap (size of gap = d in the equation below) between the metal and the semiconductor[204]:

$$T_{max} = e^{-2k_0 d} \qquad (5\text{-}13)$$

Where k_0 is the decay constant that equals to $\sqrt{\frac{2m\varphi}{\hbar^2}}$ and φ is the tunneling energy barrier. The number of modes in a 2D channel can be estimated by assuming periodic boundary conditions. At energy of $E_f = \frac{\hbar^2 {k_f}^2}{2m}$, the modes can propagate when $-k_f < k_y < k_f$ (k_f is Fermi wavevector), where the allowed values of k_y are spaced by $2\pi/W$ (W is channel width). The propagating mode number is given by:

$$M = \mathrm{Int}\left[\frac{2k_f}{k_y}\right] = \mathrm{Int}\left[\frac{k_f W}{\pi}\right] \approx W\sqrt{\frac{2n_s}{\pi}} \qquad (5\text{-}14)$$

the carrier concentration n_s in a two-dimensional channel is given by $n_s = {k_f}^2/2\pi$ and Int [x] is the maximum integer function. Using these expressions, the contact resistance quantum limit can be written as:

$$R_{C,min}W = \frac{W}{G_{max}} = \frac{h}{2q^2} e^{2k_0 d} \sqrt{\frac{\pi}{2n_s}} \quad (5\text{-}15)$$

It can be seen that the quantum limit of the contact resistance strongly depends on the carrier concentration in the 2D channel. The tunneling efficiency is also important for the contact resistance. The impact of the vdW tunnel gap on the contact resistance quantum limit as a function of the carrier concentration is shown in **Figure 5.12**. The results are plotted for vdW tunnel distances of d = 0 Å, 1 Å, 2 Å and 3 Å. Original data from Jena *et al.* for contact resistances of silicon, gallium nitride, indium gallium arsenide as well as graphene[205] are included for comparison. The solid black line (d = 0 Å) in **Figure 5.12** represents the quantum limit for contact resistance and it can be seen that mature semiconductors technologies approach this limit. The dashed lines in **Figure 5.12** represent different thicknesses of vdW gap values. It can be seen that the quantum limit for quantum resistance increases with increasing vdW gaps. Experimental results from several studies on contact resistance on monolayer MoS_2 without intentional doping are also included for comparison. It is clear from this analysis that while ultraclean contacts with vdW gaps on 2D TMD semiconductors improve the performance of devices, decreasing the contact resistance require clean contacts with thinner vdW gaps or high degree of doping of the 2D semiconductor – something that remains very challenging. Most carrier concentrations calculated in the studies are gate

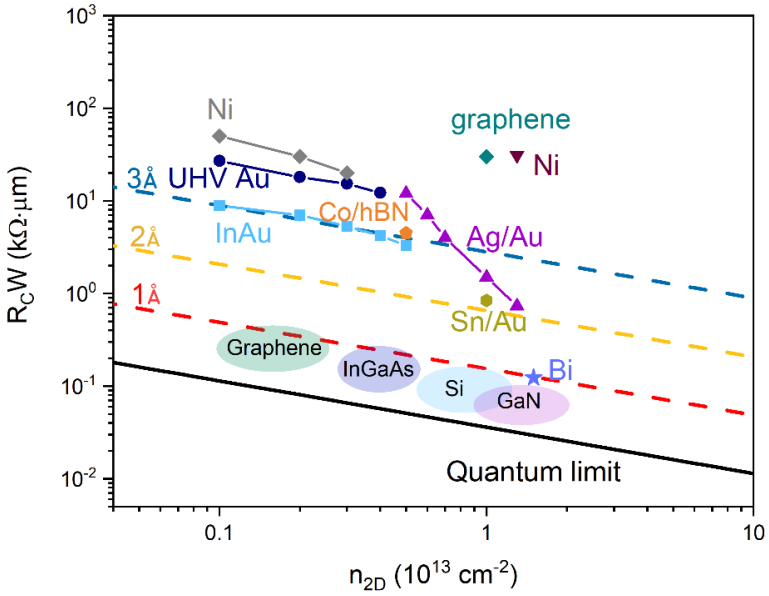


Figure 5.12 Contact resistance versus carrier concentration for monolayer MoS_2 with different contacts and varying size of vdW gap. The contact resistance values are reproduced from Ref[131,132,154,204,206–209].

electrical field doped carrier concentrations. This value could be adjusted by the metal contact or dielectric through charge transfer. One recent work report by Shen *et al.* revealed that the contact resistances approaching the quantum limit can be achieved when the metal-induced gap states are formed and the MoS_2 is degenerately doped by bismuth metal[132], for example.

5.4 Clean contacts on other 2D TMDs

5.4.1 Contact resistance of metallic 2D NbS_2

In addition to MoS_2, I have also deposited In/Au on metallic NbS_2. It can be seen from **Figure 5.13** that we obtain a contact resistance of 220 Ω·μm for NbS_2 grown by CVD, which is among the lowest values reported for any metal contact on a 2D TMDs. Ti/Au contact results are also included in **Figure 5.13b** for comparison. The contact resistance extracted is around 1 kΩ·μm. Semi-metal graphene usually has a few to tens of kΩ·μm contact resistance which limits the device performance[210,211].

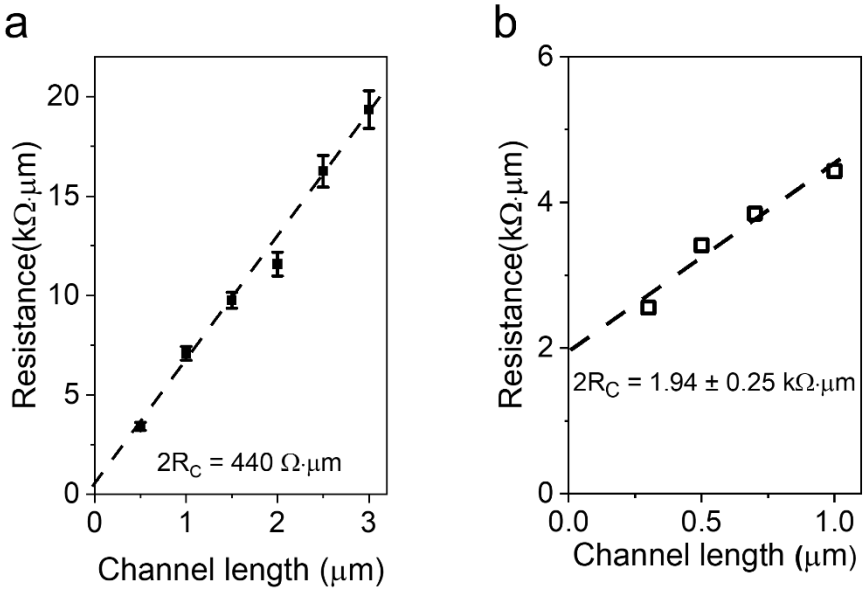


Figure 5.13 a, Contact resistance of NbS_2 with In/Au contacts. The error bars result from the averaging of least five measurements. **b,** Contact resistance of NbS_2 with Ti/Au contacts. The standard error is from linear fit of one TLM device.

5.4.2 Contact resistance of In/Au on 2D WS_2

Transfer characteristics of WS_2 FETs with indium and titanium contacts are shown in **Figure 5.14a** for comparison. The In contacted FET shows substantial higher mobility (83 $cm^2V^{-1}s^{-1}$) than Ti contacted FET (1.2 $cm^2V^{-1}s^{-1}$). Output curves of WS_2 devices are given in **Figure 5.14b** and **c** with In contacts showing linear ohmic behavior while Ti contacts show non-ohmic

contact. The TLM plot in **Figure 5.14d** shows that the contact resistance for WS_2 is 2.4 kΩ·µm, which is also amongst the lowest reported in the literature as indicated by the summary of different results shown in **Figure 5.15e**.

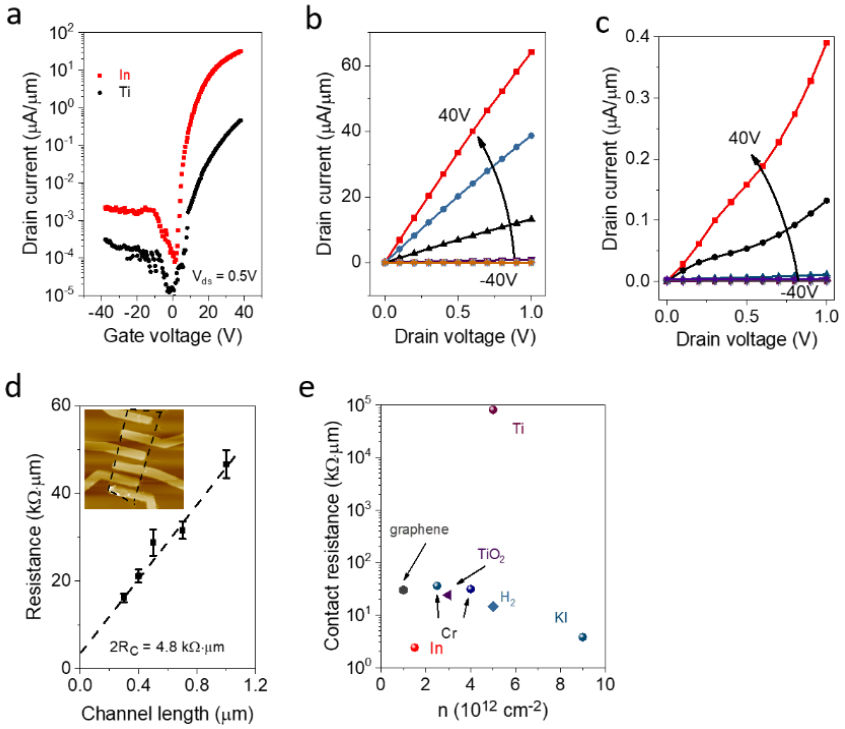


Figure 5.14 a, Transfer characteristics of FET with WS_2 as the channel material and In contacts, length and width of the device are 1 and 1.2 µm. Transfer curve of Ti contacted WS_2 device is included for comparison, length and width of the devices are 0.5 µm and 2 µm, respectively. **b,** Output characteristics of WS_2 with In contacts. **c,** Output characteristics of WS_2 with Ti contacts. **d,** TLM contact resistance of In electrodes on mechanical exfoliated WS_2. The error bars result from the averaging of least five measurements. **e,** Contact resistance versus carrier concentration from different studies reported in the literature[212–217].

5.5 Indium alloy formation for work function engineering

The FETs fabricated using electron-beam lithography are usually annealed in forming gas (Ar/H_2) environment. Here, the results of a systematic study of annealing on In contacted device performance are described. The same FET devices were tested before and after annealing at 100 °C, 200 °C, 300 °C and 400 °C, successively. Mobilities of the FETs at different annealing temperature are plotted in **Figure 5.15a**. For comparison, pure Au contacted MoS_2 device is presented in **Figure 5.15b**. In contacted MoS_2 devices showed better performance after annealing at 100 and 200 °C while Au contacted devices showed drop in

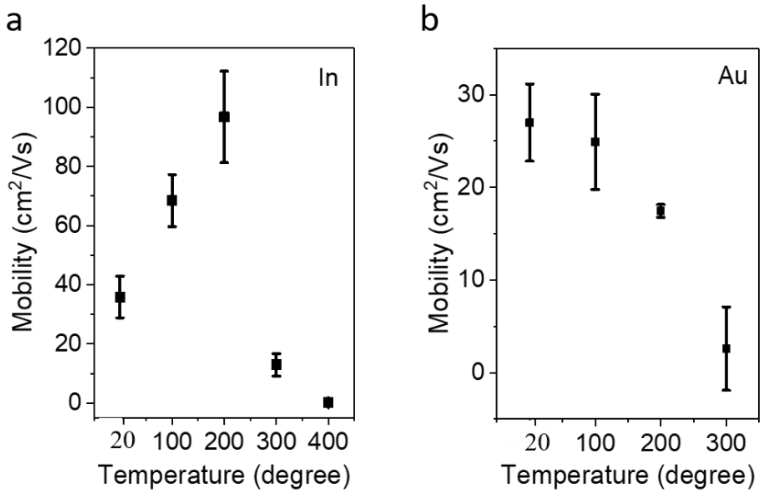


Figure 5.15 a, Mobility extracted before and after annealing with In and (**b**) Au contact.

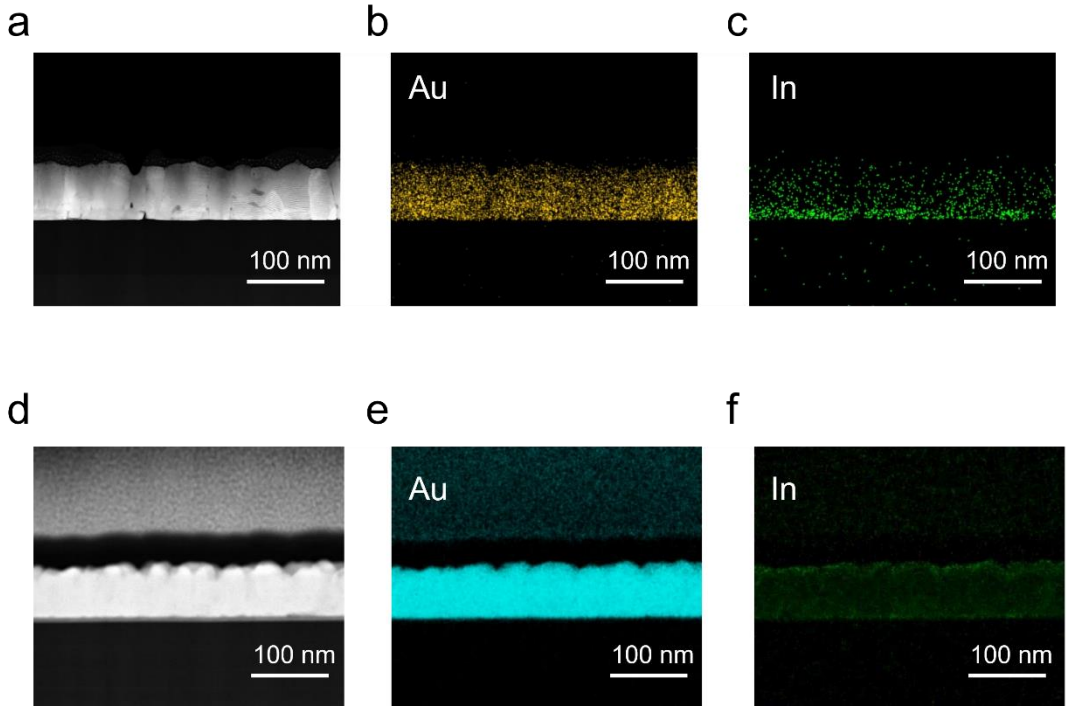


Figure 5.16 a, HAADF STEM image of In/Au contact on MoS_2 before annealing. **b, c,** EDS mapping of Au and In before annealing. In is mainly located near the interface. **d,** HAADF STEM image of In/Au contact after annealing. **e, f,** EDS mapping of Au and In after annealing.

mobility with annealing. The improvement in device performance after annealing is attributed to more uniform distribution of indium across the interface and the metal electrode. The vdW interface is not disturbed by annealing. In fact, the images shown in **Figure 5.10** are from an annealed device. Energy dispersive spectroscopy (EDS) elemental mapping of In and Au

distribution before and after annealing at 200 °C are shown in **Figure 5.16**. The upper images are In/Au contacts on MoS_2 before annealing**. Figure 5.16a** shows some metal grain boundaries in the HAADF STEM image. The indium is mainly located within 20 nm of the interface. In contrast, the metal electrode is free of grain boundaries post annealing (**Figure 5.16d**). In and Au also become more uniformly distributed after annealing.

5.6 Work function engineered contacts on WSe_2

The soft nature of indium allows it to readily form stable alloys with high work function metals such as Pd and Pt. This property can be used to adjust the work function of electrodes to facilitate electron or hole injection while maintaining the ultra-clean interface. To demonstrate this, I have studied the WSe_2 FET properties with different composition of alloys. WSe_2 was chosen because it has low conduction and valance band energy levels compared to MoS_2[218] so that holes can be injected easily by a metal with high work function.

First, the formation of ultra-clean interface was confirmed by cross-sectional ADF STEM image of indium electrodes on two layers of WSe_2. The STEM image in **Figure 5.17a** reveals clean van der Waals interface between In/Au and WSe_2. The intensity profile in **Figure 5.17b** shows that the interface metal to first layer selenide distance is ~ 2.9 Å and the gap between WSe_2 interlayer distance is 3.1 Å.

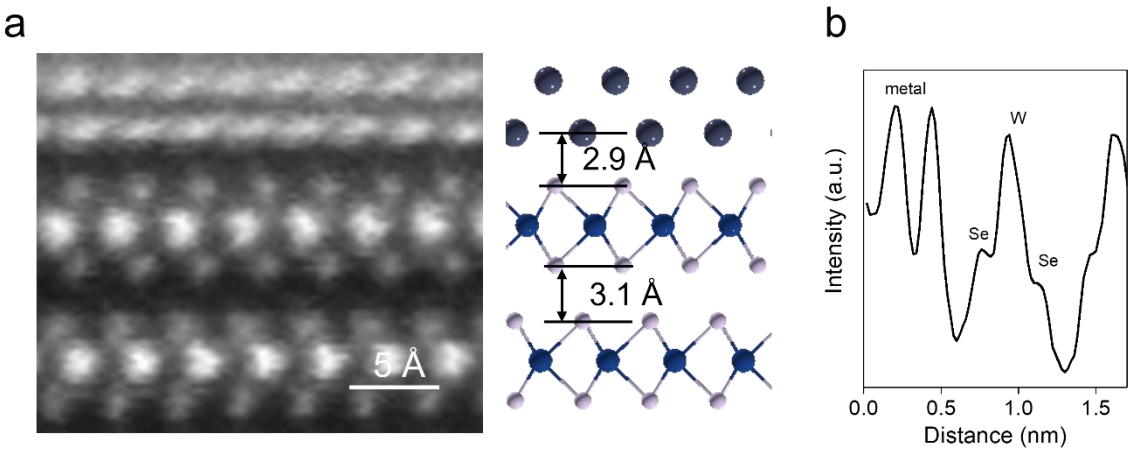


Figure 5.17 a, Atomic resolution images of In/Au on WSe_2 and the corresponding ball and stick model. **b,** The intensity profile shows that the interface metal to first layer selenide distance is ~ 2.9 Å.

FETs with In/Au alloy electrodes on WSe_2 shows pure N-type characteristics before annealing, as shown in **Figure 5.18a**. Liu *et al.* also observed small ohmic contact resistance

with indium contacts on WSe_2[219]. Upon annealing, the transfer curve of In/Au alloy electrodes on WSe_2 shows ambipolar FET characteristics with the electron current being higher than the hole current due to higher composition of Au at the interface. To further demonstrate the clean interface is free of Fermi level pinning, I made WSe_2 FETs with In/Pd contacts. The typical transfer curve of WSe_2 FET with In/Pd electrodes shown in **Figure 5.18b** exhibits higher hole current and lower electron current due to the increased work function. This can be explained by the energy band diagram in **Figure 5.18c**. With increasing composition of Au or Pd at the interface, the work function of the contact metal moves towards the valence band energy level of WSe_2, leading to more hole injection. The work functions of the alloys were measured by KPFM (Bruker, aligned with graphite), and the results are shown in **Figure 5.18c** (right side). To further increase the work function of the metal contact, In/Pt was used as contact for WSe_2.

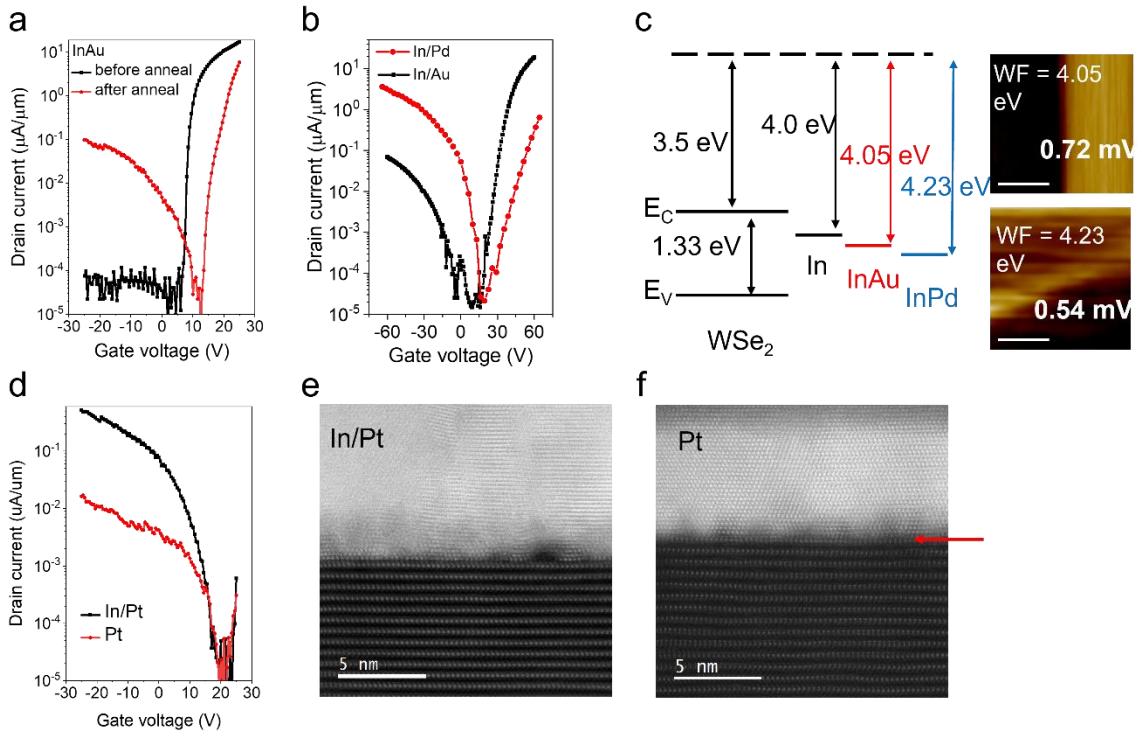


Figure 5.18 a, Transfer curve of WSe_2 EFT with In/Au contact before and after annealing. The device shows pure N-type transfer curve before annealing and ambipolar behavior after annealing. **b,** Ambipolar transfer characteristics showing N-type dominant behavior with In/Au contacts and hole dominant behavior with In/Pd contacts. **c,** The energy band levels of WSe_2 and metal alloys. The work functions of the alloys measured by KPFM are shown on the right. Scale bar is 5 μm. **d,** Transfer curves of WSe_2 FETs with In/Pt contact and pure Pt contact. **e,** HAADF STEM image of In/Pt contact on WSe_2 showing pristine clean interface. **f,** HAADF STEM image of Pt contact on WSe_2 showing the first layer WSe_2 damaged by the metal contact as indicated by the red arrow.

The transfer curve of In/Pt and pure Pt contacted WSe_2 FETs are shown in **Figure 5.18d**. The In/Pt contacted WSe_2 FET exhibits higher hole current density than In/Pd contacts. However, the current density is lower than dry transferred Pt contacts[125] and bottom contacts FETs[220]. This is probably due to low work function of alloy due to indium at the interface. **Figure 5.18d** and **f** show poor device performance due to damaged interface when pure Pt is employed as contacts for WSe_2 FETs. With In/Pt contact, clear gap between metal and the first layer of WSe_2 can be seen in the STEM image. In contrast, the first layer WSe_2 is hard to distinguish due to intermixing with pure Pt contact (as indicated by the red arrow).

The contact resistance of WSe_2 FET extracted from TLM for electron injection is 16 kΩ·µm and for holes it is 225 kΩ·µm with InAu contact (**Figure 5.19a**). These large values are consistent with the large energy offsets between the Fermi level of In/Au (4.05 eV), the conduction (3.50 eV) and valence (4.83 eV) bands of WSe_2. Comparison of resistance values

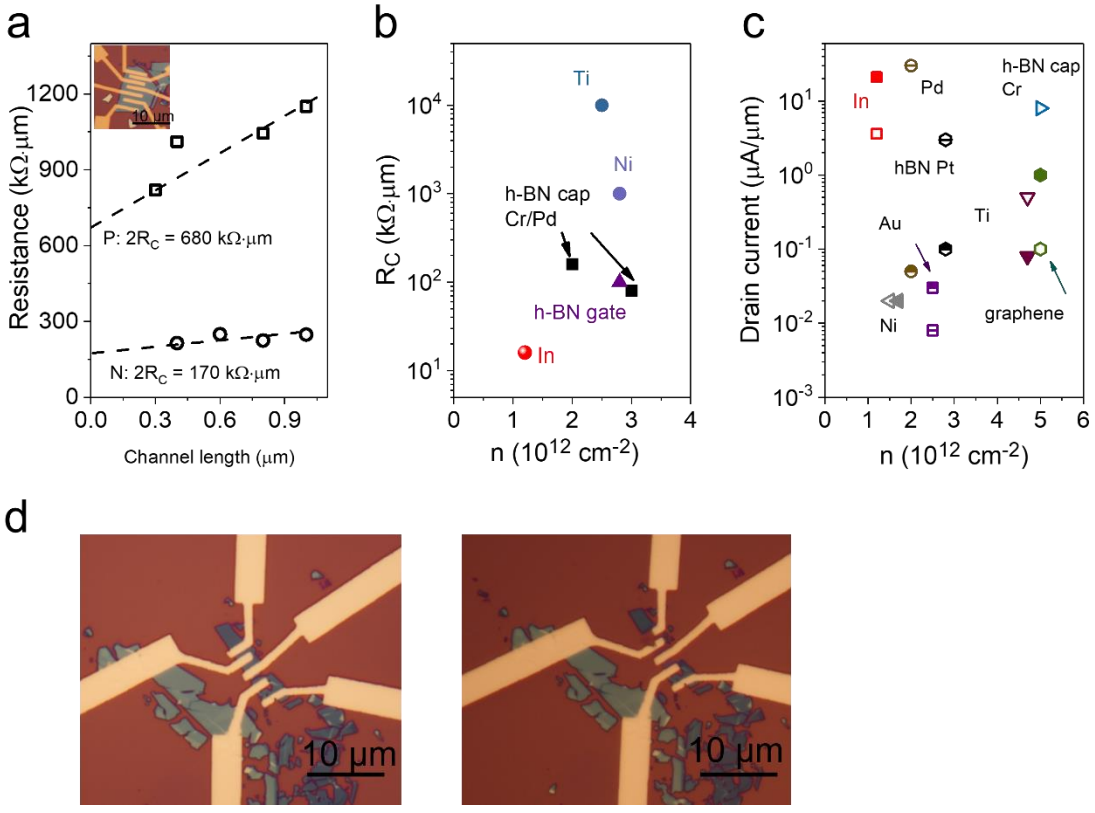


Figure 5.19 a, TLM results of In/Au contacted WSe_2 device. **b,** Comparison of contact resistances versus carrier concentrations with those reported in the literature[221–224]. **c,** Comparison of drain current with different contacts reported in the literature[221–228]. **d,** Optical images of WSe_2 FET with high contact resistance before and after electrical measurements. The device was burned due to high heat dissipation at the contact.

with literature shown in **Figure 5.19b** and **c** reveal that the indium contacts yield the lowest resistance values and both the electron and hole currents are higher. During the measurements, I found that these high contact resistance devices are easily burned. The optical images of one such device before and after measurements are shown in **Figure 5.19d**.

In conclusion, to realise pure P-type FETs and low contact resistance for holes, alloying with indium is unlikely to work. Therefore, ultra-clean vdW interfaces with pure high work function metals are needed. I will introduce how to realise clean interface without indium in Chapter 6.

5.7 Other soft metals as contacts on 2D TMDs

I have also investigated other low melting point metals such as Silver (Ag) and Gallium (Ga) as potential contact materials. The typical transfer curves of Ag and Ga contacted MoS_2 are given in **Figure 5.20a** and **5.20d**. Current density with Ag contacts was 30 µA/µm and for Ga

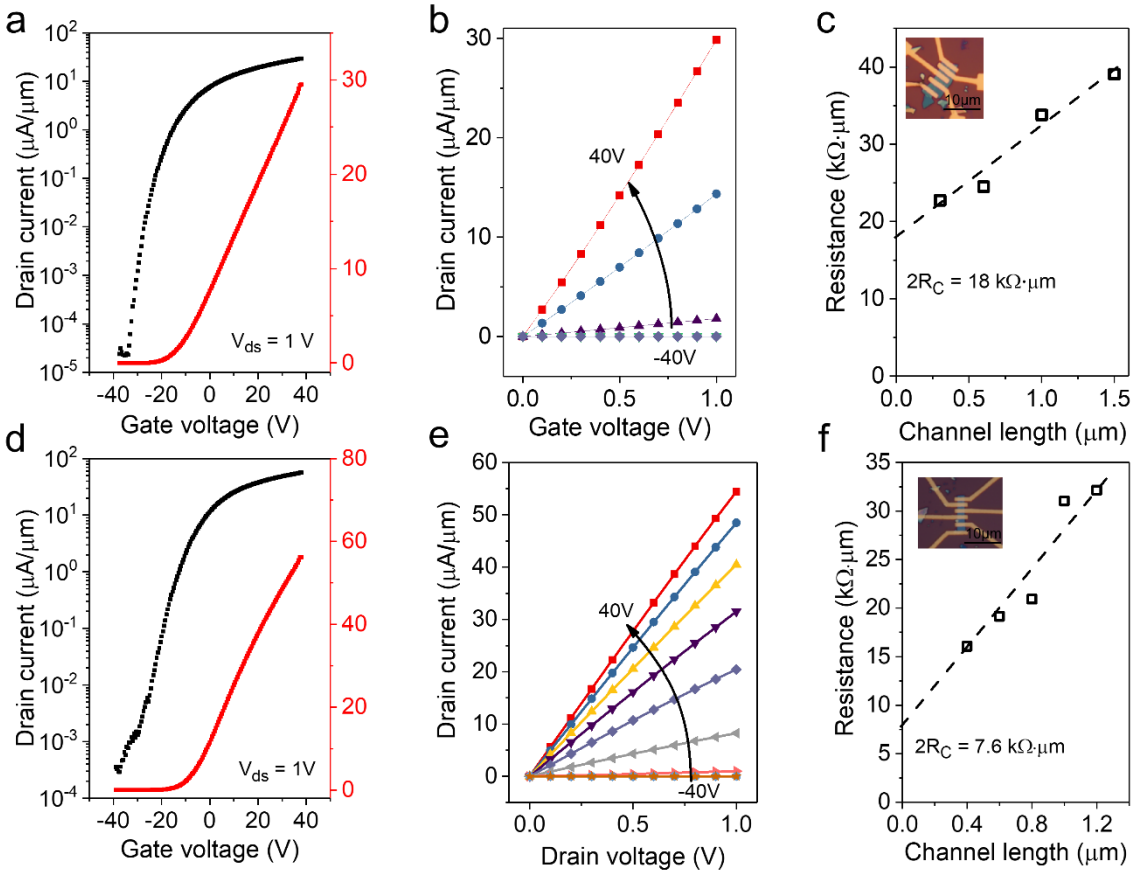


Figure 5.20 a-c, Typical transfer curve, output performance and contact resistance results of Ag and Ga (d-f) contacted multilayer MoS_2 FETs. Inset photos are optical microscope images of Ag and Ga contacted devices for TLM measurements.

contacts on MoS_2 it was 58 µA/µm. The output characteristics in Figure **5.20b** and **5.20e** also show linear output characteristics indicating low contact barrier. The contact resistance from TLM measurements of Ag on MoS_2 was ~9 kΩ·µm and ~3.8 kΩ·µm for Ga contacts.

The interface chemistry between Ag/MoS_2 and Ga/MoS_2 was studied using XPS. The results shown in **Figure 5.21a** and **b** indicate that both Ag and Ga do not react with MoS_2. In addition, **Figure 5.21d** shows a clean Ga/MoS_2 interface without any intermixing. Although the MoS_2 atoms are not distinguishable, the gap between metal Ga and the MoS_2 layer is clear (see section 4.2.3, the atomic resolution image needs to be observed at the correct zone axis without any mismatch). Since both Ga/MoS_2 and Ag/MoS_2 interfaces are clean, the higher contact resistance of Ga and Ag contacted MoS_2 FET compared to In contacted FET maybe due to higher barrier heights. Ultraviolet Photoelectron Spectroscopy (UPS, He 21.2 eV as source) measurements confirm higher work function of Ga and Ag compared to In. The UPS spectra of In, Ga, and Ag are shown in **Figure 5.21c**. The work function value is the difference between the source energy and the cutoff binding energy level as indicated in the figure. The work function of Ga (4.28 eV) and Ag (4.2 eV) are higher than In (4.05 eV).

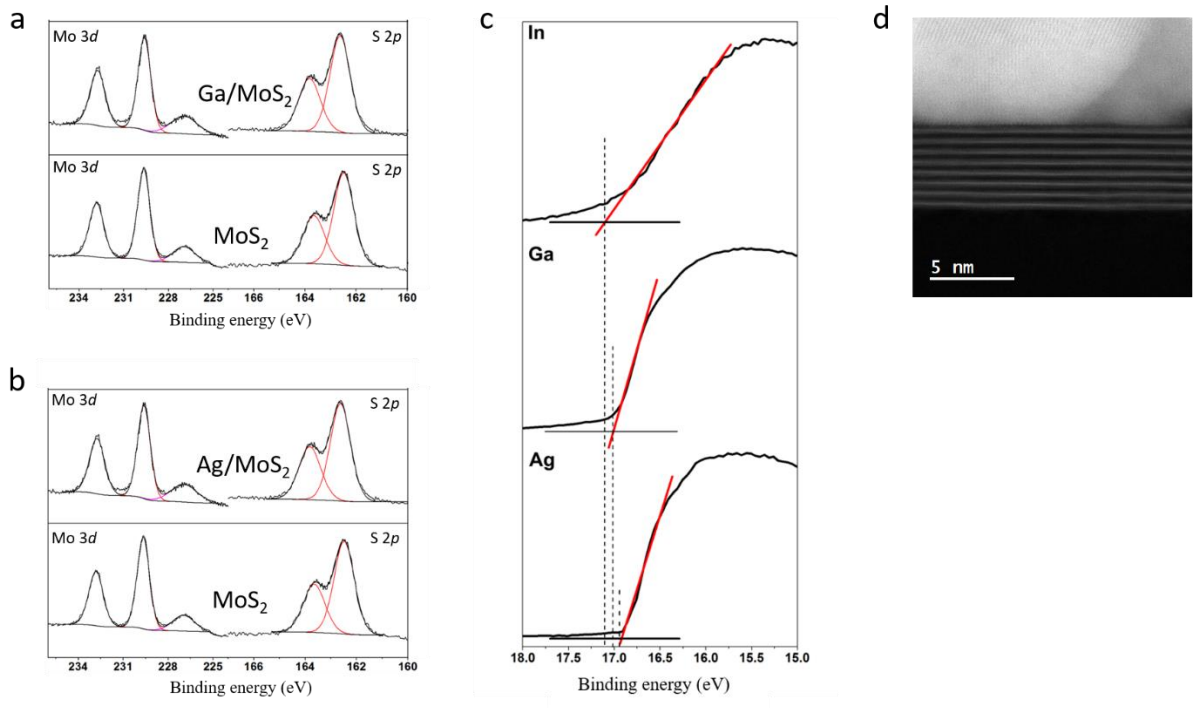


Figure 5.21 a, XPS of Ga/MoS_2 interface showing pristine Mo 3*d* doublets and S 2*p* doublets. **b,** XPS of Ag/MoS_2 interface showing pristine Mo 3*d* doublets and S 2*p* doublets. **c,** Work function measurements of In, Ga, and Ag metals using Ultraviolet Photoelectron Spectroscopy (UPS, He 21.2 eV as source). **d,** HAADF STEM image of Ga contact on MoS_2 showing pristine interface.

In conclusion, when metals form clean vdW interfaces with 2D TMDs, the contact resistance is dominated by the energy band alignment between metal and the semiconductor.

6 High work function metals as contacts for P-type FETs

In Chapter 5, clean contacts free of Fermi level pinning for N-type 2D TMD FETs were described. To fully utilize the fundamental advantages of 2D TMDs for short channel devices, high performance P-type FETs based on 2D TMDs must also be achieved. In this Chapter, I will describe the utilisation of high work function metal contacts such as Pd and Pt as contacts to achieve efficient hole injection in 2D TMDs. The interface between high work function metal contacts and TMDs were studied by cross-section STEM, XPS and electrical measurements. In this Chapter, I also demonstrate high performance photodiodes using asymmetric N- and P-type vdWs contacts. In addition, I explain how the substrate influences TMDs and its effect on performance P-type FETs.

6.1 Optimization of high work function meta deposition on 2D TMDs

The TEM images in **Figure 5.16** reveal substantial grain boundaries in the as deposited indium/gold metal contacts on 2D MoS_2. This is attributed to dendritic growth of indium on MoS_2. The morphology of e-beam deposited indium (10 nm) on MoS_2 was characterized by AFM and the measured image is shown in **Figure 6.1a**. The dendritic morphology of indium on MoS_2 is similar to Au grown on MoS_2 as characterised by Sun *et al.* using TEM[229]. The AFM image shows pin holes in the indium metal layer that could allow Au atoms from the capping layer to penetrate through the holes and form intimate contact with MoS_2. The cross-section STEM image in **Figure 6.1b** shows a pure Au grain making direct contact with monolayer MoS_2. It can be seen from the image that the pure Au grain fills ~30 nm gap between

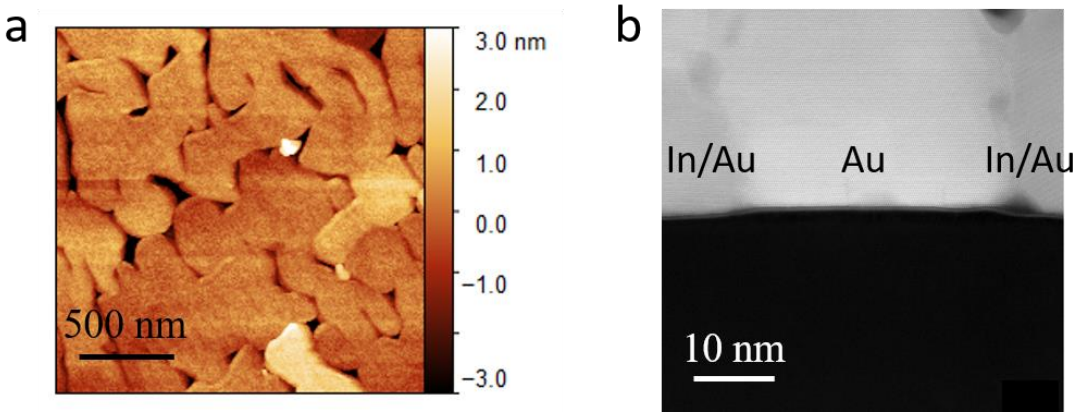


Figure 6.1 a, AFM image of 10 nm indium deposited on MoS_2 exhibiting dendritic morphology and pin holes between metal grains. **b,** Cross-section STEM image of In/Au alloy and monolayer MoS_2 interface without annealing. A region is shown where pure Au grain forms clean contact with MoS_2.

In/Au alloy grains. Surprisingly, in contrast with direct deposition of Au on MoS_2[230] that results in damage at the interface, the Au/MoS_2 interface appears pristine. This piqued my interest in making clean interfaces between high work function metals and 2D TMDs.

Taking a step back to consider how damage is induced during metal deposition on 2D TMDs reveals that there are two main causes of defects at the interface: kinetic energy transfer from metal atoms to 2D TMDs and heating of the device due to irradiation from the evaporation crucible. In electron beam evaporation, the metal evaporation rate can be controlled by adjusting the electron beam current to the crucible holding the metal. Higher electron beam current means higher crucible temperature and higher deposition rate of metal but also higher irradiation heating of the device. Controlling the evaporation parameters allows some mitigation of the two causes of damage at the interface. For example, high deposition rate

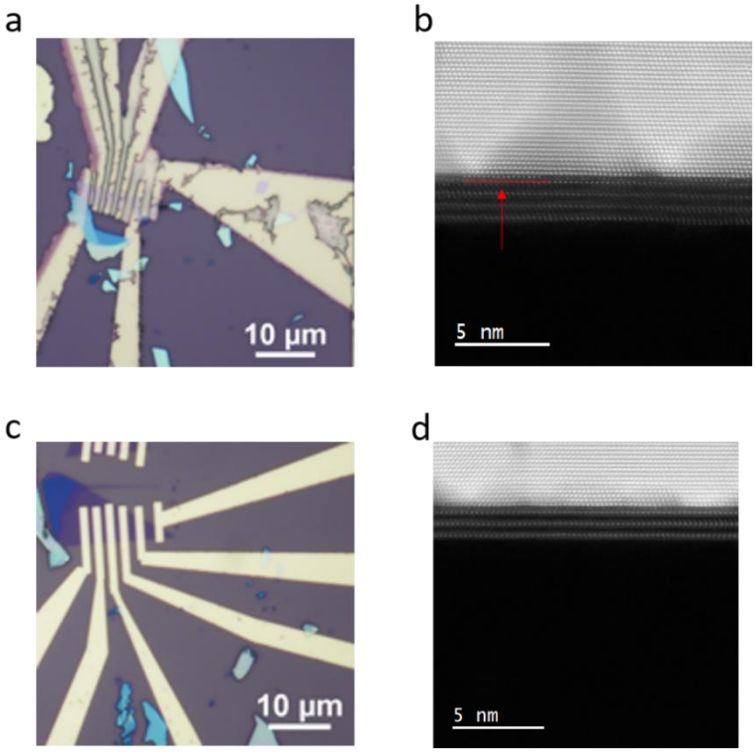
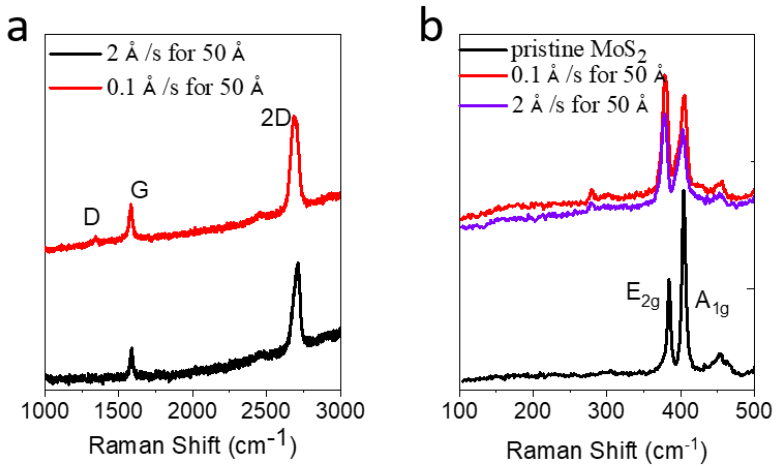


Figure 6.2 a, Optical microscope image of a MoS_2 device with 30 nm Au contacts deposited at a rate of 0.1 Å/s. The Au electrodes could not be lifted off due to damage to PMMA due to irradiation. **b,** Cross-section STEM image of the device from **a** shows distorted interface with Au atoms sitting on S positions (indicated by the red arrow). **c,** Optical microscope image of a MoS_2 FET with 30 nm Au contacts deposited at 2 Å/s. **d,** Cross-section STEM image of the device from **c** shows much cleaner interface indicating that shorter heat irradiation time leads to less damage on MoS_2.

means high kinetic energy transfer but less heating due to irradiation while lower deposition rate may lead to lower kinetic energy transfer but longer exposure to irradiation. To determine the dominant cause of damage, I compared damage caused by deposition of 30 nm Au film on MoS_2 at low (0.1 Å/s) and high (2 Å/s) deposition rates. The optical image of a device made with low deposition rate Au contacts is shown in **Figure 6.2a**. The image shows that the developed PMMA (the e-beam resist) could not be lifted off properly due to damage caused by heating due to longer irradiation time. The poor liftoff is indicated by the fact that channels between the electrodes are not well defined because the PMMA is not removed from those regions. The inability to lift off the developed PMMA suggests that it experienced temperatures in excess of 300 °C to undergo crosslinking, which decreases its solubility in acetone that is used to remove it after development. The corresponding cross-section STEM image (**Figure 6.2b**) shows that Au atoms sit on S positions on MoS_2, which indicates damage in the form of



c

	E_{2g}	A_{1g}	A_{1g} FWHM
MoS_2	384.2	404.0	2.5
0.1 Å/s	378.7	404.2	4.5 ± 0.5
2 Å/s	378.7	404.2	4.1 ± 0.4

average from 8 spectra

Figure 6.3 a, Graphene Raman spectra after deposition of 5 nm Au at different rates. The low deposition rate sample (longer irradiation time) exhibits an additional defective peak of graphene at 1360 cm^{-1}. **b,** MoS_2 Raman spectra after deposition of 5 nm Au at different rates. The out of plane A_{1g} peak becomes broader after Au deposition. **c,** Summary of Raman peak positions of MoS_2 after capping with 5 nm Au. The average of E_{2g} FWHM becomes broader with longer irradiation.

chemical reaction - also suggesting that the device has experienced high temperature. In contrast, at high deposition rate, the fabricated FETs show clean contact patterns and much cleaner interface (**Figure 6.2c** and **d**). This suggests that the PMMA can be easily lifted off because it is not crosslinked and therefore highly soluble in acetone. The very clean interface also suggests absence of kinetic and chemical damage at the interface. Thus, these experiments indicate that shorter irradiation time is an important parameter for achieving clean contacts on MoS_2 by minimizing heating of the device.

I also deposited 5 nm Au film at different deposition rates (0.1 Å/s and 2 Å/s) on graphene and CVD grown monolayer MoS_2 and investigated damage by Raman spectroscopy. The Raman spectra of graphene with Au is shown in **Figure 6.3a**. There are two representative peaks of graphene in the spectra, the in-plane vibrational (E_{2g}) G band and the two phonon 2D band[231]. The low deposition rate sample (longer irradiation time) shows an additional D peak located at 1360 cm^{-1} that is recognized as the signal from defective graphene[232]. For monolayer MoS_2, although the defective peaks are absent, the broader A_{1g} peak from low deposition rate sample indicates presence of some disorder.

6.2 Optimization of e-beam evaporation parameters

The current and voltage supply for different metal depositions with 0.1 Å/s and 2 Å/s are summarized in **Figure 6.4a**. The energy required for 10 nm of metal deposition at 2 Å/s deposition rate is much lower than 0.1 Å/s. To minimize radiation heating from exposure to hot crucible during deposition, I sought to optimize the evaporation procedure. The metal evaporation was conducted at a base pressure of < 10^{-8} torr to minimize surface adsorbates on the 2D TMDs and decrease the vapor temperature of metals (see Figure 5.5, vapor temperature of Au is ~950 °C at 10^{-6} torr and ~800 °C at 10^{-8} torr). A relatively long working distance between the crucible and substrate (i.e. the device) of 70 cm was used to minimize the kinetic energy of the impinging evaporated atoms on the device. Furthermore, during heating of the crucible to metal sublimation temperature, the crucible and substrate shutters were kept closed to avoid radiative heating of the device. Once the crucible was sufficiently hot for metal sublimation to occur, the deposition was carried out in steps to ensure the device/ sample holder remained at or close to room temperature. For example, a typical process involved multiple steps of 10 nm Pd or Pt depositions at a rate of 2 Å/s. After this initial 50s step, the deposition was paused for one hour to allow the vacuum chamber and substrate holder to cool to room temperature before starting the next deposition step. **Figure 6.4b** shows the temperature versus

time sketches for deposition of 300 Å Pt in a single step and with multiple steps. The temperature versus time plot on the left (without steps) shows that during deposition the temperature of the holder gradually increases with time. Usually, the substrate temperature increased from 18 °C to 36 °C during 300 Å Pt deposition and the chamber pressure increased from 5×10^{-8} torr to 8×10^{-7} torr. In contrast, the sketch on the right shows the temperature variation during deposition with three steps (100 Å Pt for each step). After each 100 Å of Pt deposition, the chamber and substrate holder were allowed to cool to room temperature and the chamber pressure returned to the base pressure before running another deposition (red curve region in the plot). As a result, the temperature of the sample holder remained quite low (~24°C) compared to the deposition without steps. These temperatures were recorded from the

a

0.1 Å/s for 100 Å	Current (mA)	Voltage (kV)	Time (s)	Energy (kJ)
Au	80	10	1000	**800**
Pd	85	10	1000	**850**
Pt	130	10	1000	**1300**

2 Å/s for 100 Å	Current (mA)	Voltage (kV)	Time (s)	Energy (kJ)
Au	92	10	50	**46**
Pd	95	10	50	**47.5**
Pt	150	10	50	**75**

b

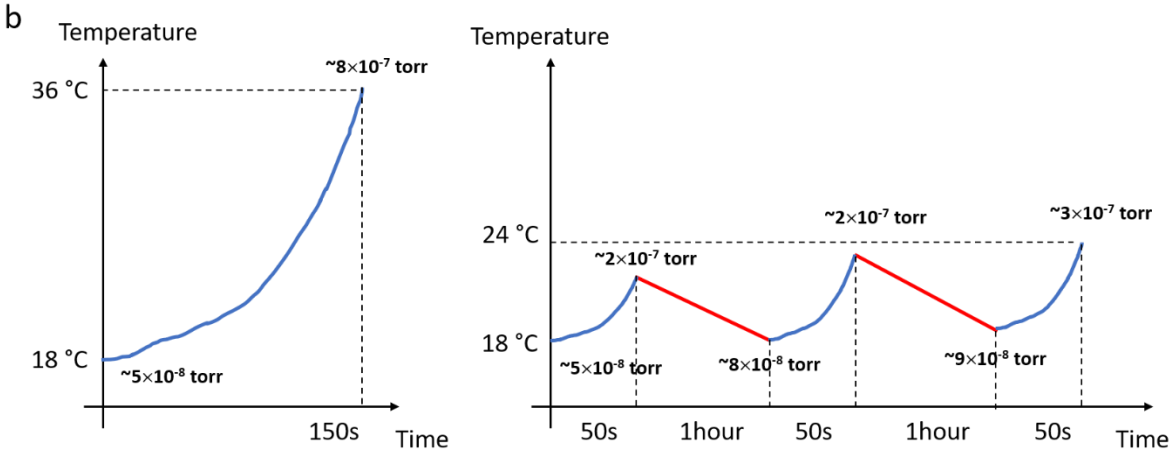


Figure 6.4 a, Summary of e-beam evaporation current and voltage applied to deposit Au, Pd and Pt at 0.1 Å/s and 2 Å/s. The irradiation energy supplied to the device for high rate deposition is much lower than for low rate deposition. **b,** Comparison of substrate temperature versus time for 300 Å Pt depositions done in single and multiple steps. The left figure (single step deposition) shows that during deposition, the temperature of the holder gradually increases with time. For deposition with steps, the chamber and substrate holder were allowed to cool to room temperature before running the next deposition. Thus, the temperature of the sample remained lower than deposition without steps.

thermocouple connected at the bottom of the sample holder (a massive copper block). The real device temperature is likely to be much higher than the temperature of the Cu block. The temperature of the Cu block surface exposed to irradiation where the device is placed is likely to be higher than the back thermocouple reading. This supported by the fact that the PMMA crosslinks (**Figure 6.2a**) at low deposition rates. I use the values from the thermocouple to compare relative heating of the device during contact evaporation. Typically, 20 nm of Pd capped with 20 nm of Au was used for Pd contacts (all deposited at 2 Å/s in 100 Å steps). For Pt contacts, 10 nm of Pt capped with 30 nm of Au was used. The results from this approach for realising P-type FETs based on 2D TMDs are described in the following sections.

6.3 Metal work function on 2D TMDs

The lower valence band energy level (4.9 - 5.4 eV by different calculation methods) of WSe_2 compared to MoS_2 (5.8 - 6.4 eV by calculation)[232] makes it easier to inject holes using high work function metals such as Pd (5.1 eV) and Pt (5.6 eV)[7]. However, the work function of metals is strongly dependent on the crystal structure. That is, Hulse *et al.* reported Pd (110) work function to be 5.2 eV, while Pd (100) work function was measured to be 5.65 eV and Pd (111) work function of 5.9 eV[233]. Wang *et al.* reported work function of 4.86 eV for Pd (110)[234]. A range of work function values from 5.2 to 5.7 eV have been reported for different crystal orientations of Pt[234]. Thus, it is important to determine the work function of metals deposited on 2D TMDs. To this end, UPS measurements were conducted to obtain work functions of Pd and Pt films deposited on WSe_2. The depth of penetration of UPS measurement is ~ 3 nm. To

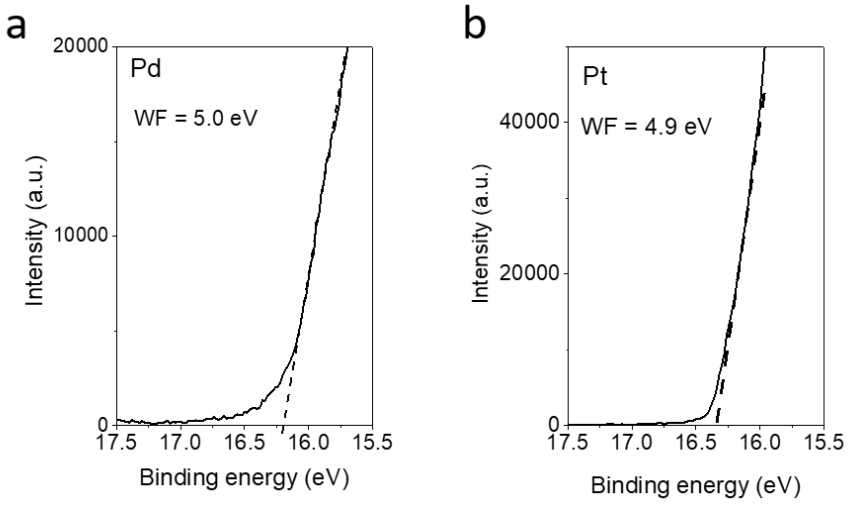


Figure 6.5 Work function measurements of Pd and Pt metals using Ultraviolet Photoelectron Spectroscopy (UPS, He 21.2 eV as source).

avoid oxidation of metal films, samples were prepared by depositing 10 nm Pd or Pt on WSe_2 and capping with 20 nm of Au. Then, the samples were loaded into the XPS chamber and the Au capping layer was etched by an Ar ion gun. XPS was used to confirm Au was fully removed and only Pd or Pt was exposed before UPS measurements. The work function results shown in **Figure 6.5** indicate that Pd has a work function of 5.0 eV and Pt has a work function of 4.9 eV. The work functions of Pd and Pt are lower than bulk crystals but they are sufficiently high for injection of holes into WSe_2 or MoS_2 as the metal energy levels are closer to the valence band energy of WSe_2 and MoS_2 than the conduction band energy.

6.3.1 Interface between Pd and multilayer WSe_2

To fabricate P-type FETs using high work function metals, Pd and Pt metals were deposited on 2D WSe_2 and MoS_2. In this section, the work on Pd/WSe_2 is described. Specifically, the Pd/WSe_2 interface was studied with XPS and ADF STEM imaging. Devices with clean interfaces were fabricated and tested. We prepared cross-section samples for ADF STEM study of Pd/WSe_2 interface. The Pd electrodes were evaporated on WSe_2 by using the approach described in section 6.1. It is well known that few-layered TMDs are easily damaged during metal deposition[124]. By minimizing the heating of the sample due to irradiation from the crucible during evaporation, clean interface was achieved between high work function Pd metal and multilayer WSe_2. As shown in **Figure 6.6**, the interface between Pd and WSe_2 is clean and no evidence for intermixing is observed. The image shows that Pd atoms are well aligned on top of the WSe_2 without any diffusion into the WSe_2 layer.

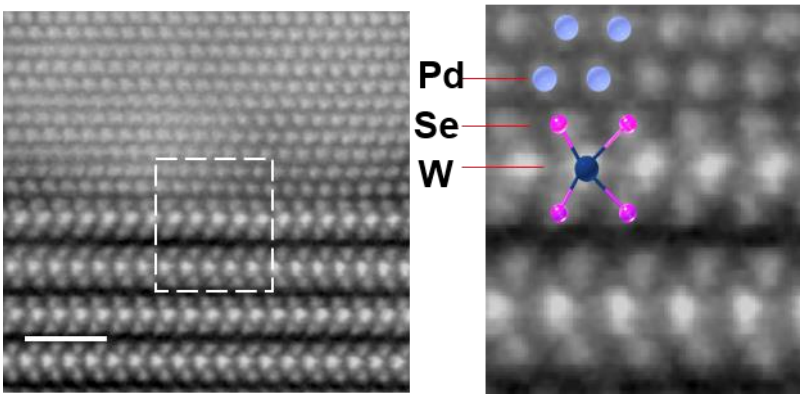


Figure 6.6 Atomic resolution annular dark field (ADF) STEM image showing clean interface between Pd and WSe_2. Scale bar = 1 nm. Right image is enlarged dashed rectangle region from left showing ADF STEM image where Mo, S and Pd atoms are visible.

XPS was employed to investigate the chemistry of the Pd/WSe_2 interface. Since Pd metal film is easily oxidized in air and the oxide peak overlaps with PdSex peaks, the sample for XPS measurements was prepared by depositing 30 nm of Pd on top of WSe_2 and capping with 20 nm of Au (schematic of the sample is shown in **Figure 6.7a**). XPS measurements on the Pd film were by obtained Ar ion etching (1kV, low energy) the Au capping layer and the Pd layer until the signal from WSe_2 could also be measured. The Pd signal was captured every 10 seconds during Ar ion etching. Several representative scans of Pd spectra are plotted in **Figure 6.7b** at different etching times. Only the Au 4*d* peak at 334.5 eV was observed before etching,

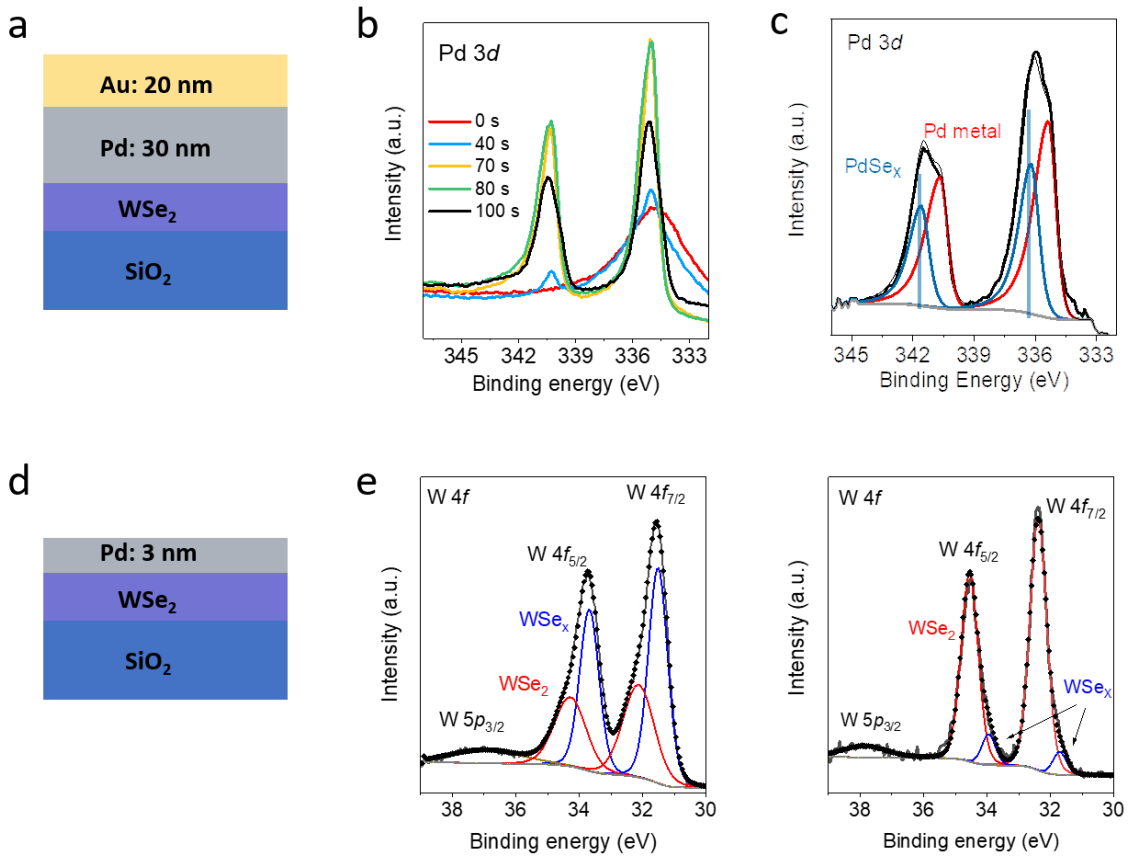


Figure 6.7 a, Schematic of Pd/WSe_2 sample for XPS measurements capped with Au to avoid oxidation of Pd. **b,** Pd 3*d* spectra captured at different Ar ion etching times. **c,** Pd 3*d* spectra when the Pd/WSe_2 interface is detected showing $PdSe_x$ peaks which indicate reaction of Pd with WSe_2. **d,** Schematic of the Pd/WSe_2 sample (only thin Pd deposited on WSe_2) for W signal capture. **e,** W 4*f* spectra detected at two different spots on the sample show intermediate WSe_x signal. The red peaks are W $4f_{7/2}$ at ~ 32.2 eV and W $4f_{5/2}$ at ~ 34.4 eV belonging to WSe_2. Additional defective peaks (blue curves) for WSe_x are observed at ~ 31.7 eV and 33.9 eV. The two different ratios of intermediate states could be due to inhomogeneous thickness of Pd layer.

as shown by the red curve. The 3*d* doublet of Pd metal peak appears at 335.0 eV and 338.3 eV as the Au layer is etched away. After 70 seconds, the Au film is fully removed, only the Pd metal signal is observed. After 100 seconds, the intensity of Pd metal signal begins to decrease (black curve) and WSe_2 signal appears. **Figure 6.7c** provides the Pd/WSe_2 interface chemical information obtained after 120s of Ar ion etching, when the XPS spectrum of Pd shows doublet peaks associated with PdSex at 336.2 eV and 341.6 eV. In the tungsten XPS spectrum, we observed formation of intermediate WSe_x states. However, as described in section 4.2.2 of the thesis, an extra Mo $3d_{5/2}$ peak is observed for defective MoS_2 when MoS_2 crystal is treated with 10-second low-energy Argon ion bombardment. Therefore, the presence of intermediate W states in Ar ion milled XPS samples cannot be taken as intermediate states due to interface reaction. Therefore, to confirm that intermediate tungsten states form at the interface of Pd/WSe_2 exist due to Pd deposition, we performed XPS on 3nm of Pd on top of WSe_2 (schematic of the sample is shown in **Figure 6.7d**). We were careful in avoiding oxidation of the Pd by minimizing the time between the deposition and XPS measurements. The XPS scans of W 4*f* spectra at two different locations on the sample are shown in **Figure 6.7e**. Both scans show WSe_x intermediate states (blue curves) due to chemical reaction between Pd and WSe_2. This is similar to the results of Smyth *et al.* who observed chemical reactions at Ir/WSe_2 and Cr/WSe_2 interfaces[235]. The difference in the XPS spectra at the two different locations is attributed to heterogeneity in the Pd thin film. At 3nm, the Pd thin film on WSe_2 may not be continuous and therefore the reaction at the interface is inhomogeneous. Our XPS analysis shows that while the STEM imaging shows a clean interface, there are chemical interactions between the Pd and Se at the Pd/WSe_2 interface. Therefore, these interfaces cannot be classified as vdW contacts.

6.3.2 FETs based on Pd contacts on 2D WSe_2

To achieve P-type FETs, the electron doping from SiO_2 must be suppressed along with realising vdW contacts with high work function metals. To this end, it is important to passivate the SiO_2 substrate with self-assembled monolayers (SAMs), or by placing the 2D TMDs on h-BN or polymethyl methacrylate (PMMA) substrates. Duan *et al.* observed N-type MoS_2 transistor with dry transferred Pt contacts[236]. P-type FETs were only achieved by placing Pt/MoS_2 on PMMA substrates where electron doping from the substrate is suppressed. I will discuss the doping effect of different substrates on TMDs in section 6.6. FETs on different substrates (SiO_2, h-BN, PMMA) were fabricated with high work function contacts to realise P-type devices. The substrates were prepared using the following recipe: SAM treated SiO_2 were obtained by

immersing in FOTS (trichloro-(1H,1H,2H,2H-perfluorooctyl) silane, silane/n-hexadecane (1:1000 v:v), purchased from Sigma-Aldrich) for 1 hour to passivate the surface -OH groups. After passivation, the substrate was rinsed with acetone and isopropanol multiple times. The h-BN used in this work was few-layered h-BN grown by CVD. The PMMA substrate was obtained by spin coating (MicroChem, A6) at 3000 rpm for 1 minute and heating at 180 °C for 5 minutes. Since the PMMA substrate is not compatible with the e-beam lithography process, TEM grid was used as shadow mask to achieve FETs with channel length of ~ 10 µm.

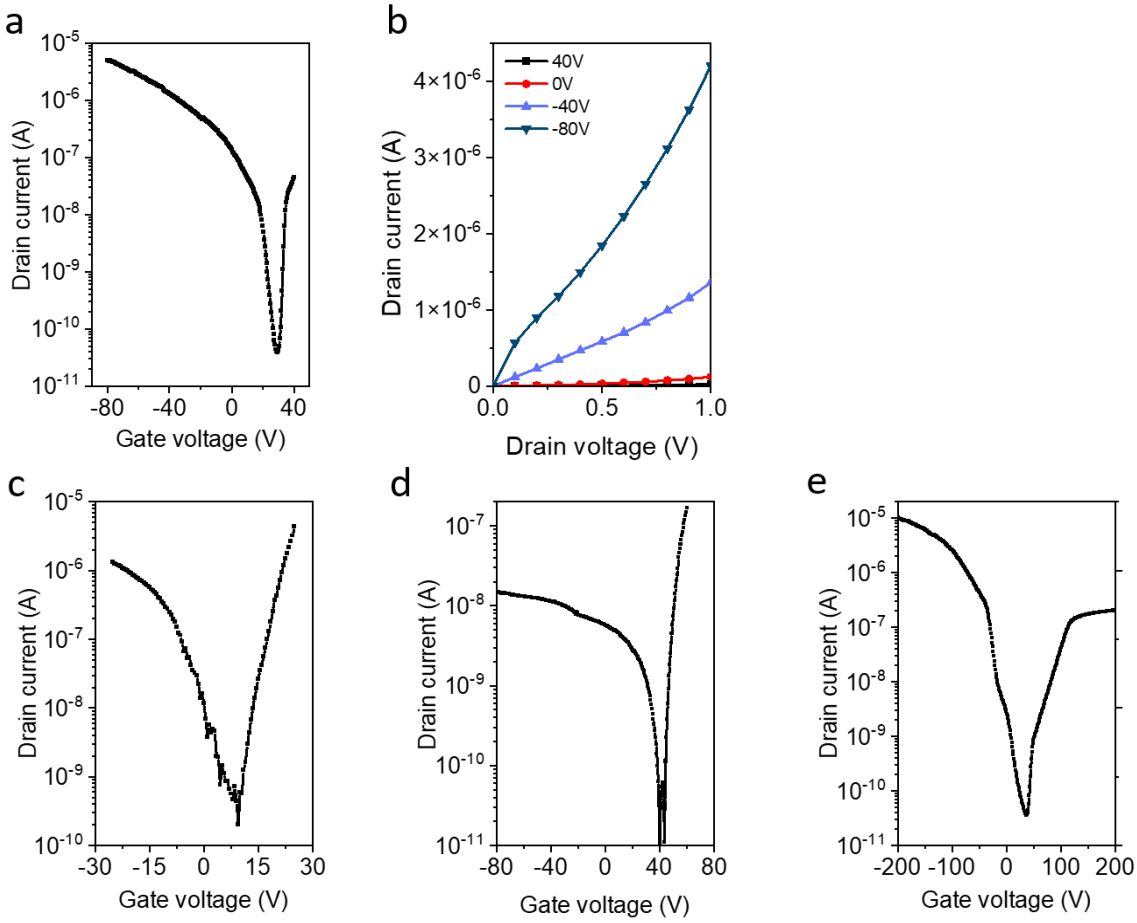


Figure 6.8 a, Transfer curves of WSe_2 device with Pd contacts on SAM treated SiO_2 showing ambipolar characteristics with higher hole branch. Device dimensions: W/L = 5µm /1.5µm. **b,** Output curves of WSe_2 device with Pd contacts. **c,** Transfer curves of WSe_2 FET with Pd contacts on SiO_2. W/L = 7µm /2µm. **d,** Transfer curves of WSe_2 FET with Pd contacts on h-BN. W/L = 4µm /2.5µm. **e,** Transfer curve of WSe_2 FET with Pd contacts on PMMA. The substrate has little influence on the hole injection level for WSe_2. W/L = 15µm /10µm. The source drain bias voltage = 1V for transfer curves.

Electrical measurements on FETs fabricated using Pd contacts, multilayer WSe_2 as the semiconductor channel and SAM treated SiO_2 as the substrate are shown in **Figure 6.8a** and **b**. The transfer curves in Figure **6.8a** show ambipolar (showing both electron and hole currents) characteristics with two orders of magnitude higher hole current than electron current. The output curves show non-linear characteristics in **Figure 6.8b**, which indicate substantial contact resistance (see section 5.1 of the thesis). These results suggest that while Pd contacts allow hole injection, electron injection also occurs due to defective nature of the interface. The transfer curves of WSe_2 devices on SiO_2, CVD grown h-BN on SiO_2, and PMMA on SiO_2 are plotted in **Figure 6.8c-e**. All results show ambipolar behavior for WSe_2 FET with Pd contacts. It can be seen that none of the devices show pure P-type characteristics, indicating that substrate doping has only small influence on the hole injection into WSe_2 because the contact is damaged due to chemical reaction, creating states at the interface.

6.3.3 Pt contacts on multilayer WSe_2

From the above, it is clear that Pd reacts with WSe_2 and forms intermediate states at the interface, which limits the hole injection efficiency for realising high performance P-type FETs. Thus, Pt contacts on WSe_2 were investigated. We have found that clean vdW contacts of Pt on WSe_2 can be achieved by ensuring that temperature of the devices remains close to room temperature during the deposition process. We therefore deposited 10 nm of Pt on WSe_2 using the multi-step deposition process (50s of Pt deposition then pause for 1hour) and deposited 30

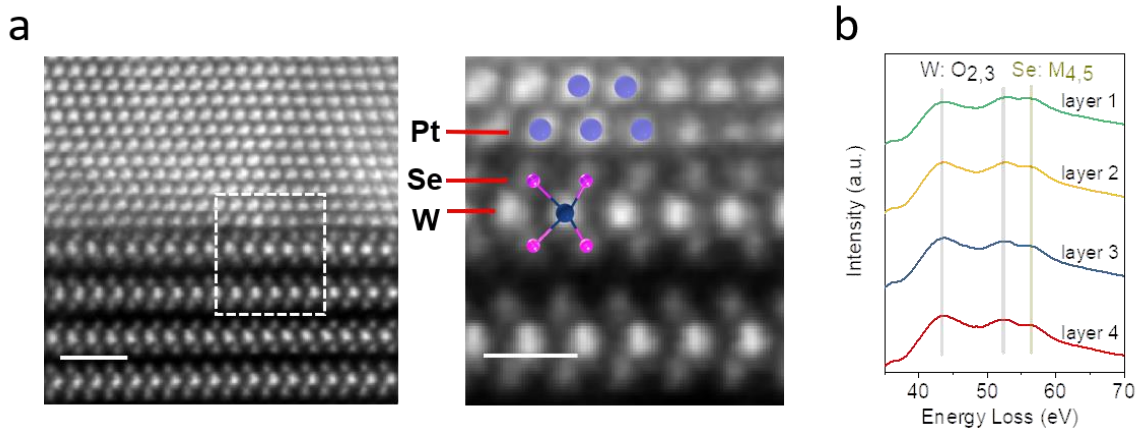


Figure 6.9 a, Atomic resolution annular dark field (ADF) STEM image showing clean interface between Pt and WSe_2. Scale bar = 1 nm. Right image is enlarged dashed rectangle region from left showing ADF STEM image where W, Se and Pt atoms are visible. Scale bar = 0.5 nm. **b**, EELS showing that the electronic structure of the Se atoms in all layers is similar.

nm of Au (10 nm at each step). The cross-section ADF STEM images from deposition of Pt on multi-layered WSe_2 are shown in **Figure 6.9a**. The spacing between the Pt and Se atoms is ~ 2.3 ± 0.1 Å. The chemical states of WSe_2 at the interface is characterized by electron energy loss spectroscopy (EELS) analysis using a 0.9 Å electron beam probe focused on the WSe_2 layer adjacent to the deposited metal. The EELS data shown in **Figure 6.9b** are taken from several different WSe_2 layers showing the $O_{2,3}$ edge of W and $M_{4,5}$ edge of Se. Absence of differences between EELS spectra of different WSe_2 layers reveals that the electronic structure of the Se atoms at the interface is largely unperturbed.

Absence of chemical interactions between Pt and Se atoms at the Pt/WSe_2 interface was also confirmed by XPS analysis. The interface Pt signal is obtained using the approach for Pd contacts described above. That is, the sample for XPS measurement was prepared by depositing

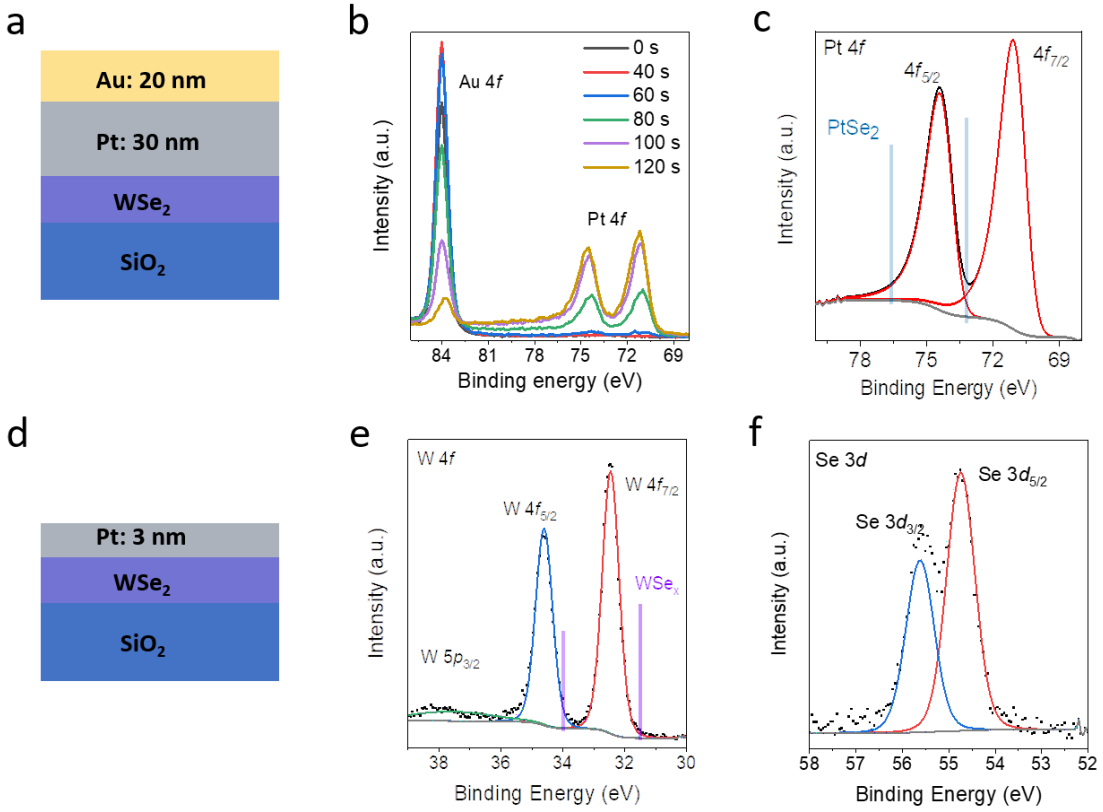


Figure 6.10 a, Schematic of the Pt/WSe_2 sample capped with Au for XPS measurements. **b,** Pt 4*f* spectra captured at different Ar ion etching times. **c,** Pt 4*f* spectra taken when the Pt/WSe_2 interface is detected showing pristine Pt metal signal. **d,** Schematic of Pt/WSe_2 sample for W signal capture. **e, f,** XPS of the Pt/WSe_2 interface showing pristine W and Se peaks. The XPS also shows that the deposition of Pt causes the peaks to be right shifted by 0.3 eV, indicating slight hole doping of WSe_2 from Pt deposition.

30 nm of Pt and 20 nm of Au on freshly cleaved WSe_2 crystal (schematic of sample is shown in **Figure 6.10a**). The Ar ion etching time dependence of Pt 4*f* signals are plotted in **Figure 6.10b**, showing decreasing Au $4f_{7/2}$ intensity at 84.0 eV and increasing Pt 4*f* intensity at 71.0 eV and 74.3 eV with longer etching times. The Pt 4*f* peaks in **Figure 6.10c** were obtained when the WSe_2 signal appeared to probe the Pt/WSe_2 interface. The Pt 4*f* spectra at the Pt/WSe_2 interface show only pristine Pt $4f_{5/2}$ at ~ 74.3 eV and Pt $4f_{7/2}$ at ~ 71.0 eV and no signal for $PtSe_2$ or $PtSe_X$ formation was observed[237]. Similar to Pd/WSe_2, we also analyzed the WSe_2 signal by probing thin Pt film (~3 nm) deposited on WSe_2 crystal. Unlike Pd/WSe_2 interface, no WSex signal was observed at the Pt/WSe_2 interface. Both W 4*f* and Se 3*d* spectra show pristine WSe_2 spectra with 0.3 eV right shift to lower binding energies, which indicates slight P-type doping of WSe_2 after Pt deposition.

6.3.4 FETs based on Pt contacts on 2D WSe_2

The electrical characteristics of FETs fabricated on multilayer WSe_2 using Pt as contacts are shown in **Figure 6.11**. Purely P-type FETs with high saturation hole currents of 1.04×10^{-4} A (at channel width/length of 4µm/2µm) and no measurable electron currents can be achieved with Pt contacts on few layered WSe_2 (SAM treated SiO_2 as substrates), as observed in the transfer and output characteristics of devices in **Figure 6.11a** and **b**. In addition, the influence of substrates (SiO_2, CVD grown BN on SiO_2, and PMMA on SiO_2) on hole injection into WSe_2 with high work function Pt contacts is indicated in **Figure 6.11 d-f**. It can be seen that WSe_2 FETs show P-type characteristics independent of the substrate. Mobility values of ~ 190 cm^2-$V^{-1}s^{-1}$ were obtained using the methodology described in section 5.1 with on/off ratios of 10^7 – comparable to those obtained for mechanically transferred Pt contacts[125]. The transconductance of WSe_2 FET versus gate voltage is shown in **Figure 6.11c**. The maximum transconductance (g_m) is found at gate voltage of ~ 8V. In fact, the g_m values are similar between gate voltage of 2V and 9V. The threshold voltage (V_T) is around 12 V. To obtain the mobility of the device from the linear regime ($V_D \ll V_G - V_T$), the drain current (4.36×10^{-5}) at gate voltage of 2V was used to extract the mobility. The extracted mobility was found to be 189.48 cm^2-$V^{-1}s^{-1}$.

The transfer characteristics of WSe_2 FET with Pt contact measured at different temperatures are shown in **Figure 6.12a** and **b**. The barrier height was extracted using the method described in section 5.3.2 and equation 5.8 from the slope of the Arrhenius plot in which the logarithm of the drain current was plotted as a function of inverse of temperature at different gate biases from -10V to -40 V shown in **Figure 6.12d**. The extracted barrier height

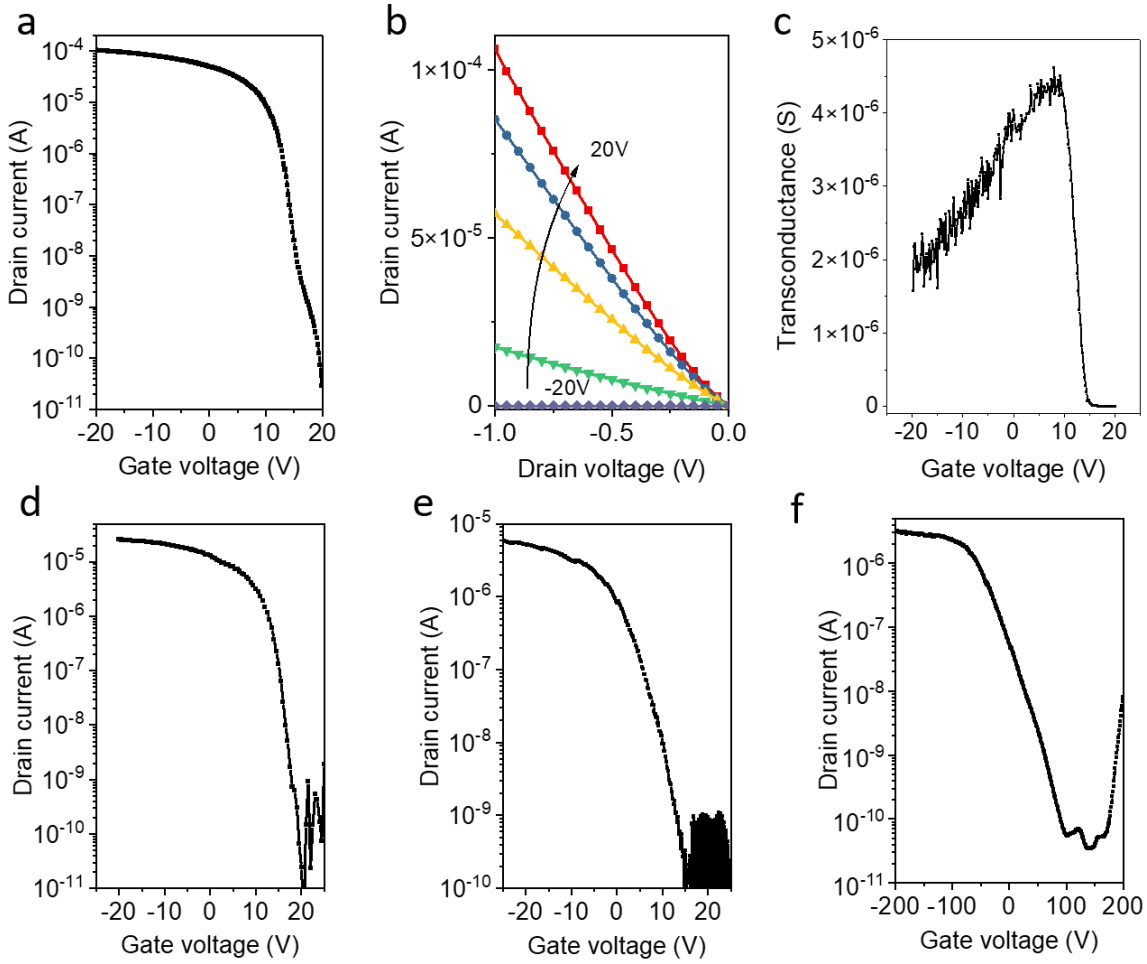


Figure 6.11 a, Transfer curves of WSe_2 FET with Pt contacts on SAM treated SiO_2 showing P-type behavior with high hole currents. W/L = 4µm/2µm. **b,** Output curves of WSe_2 device with Pt contacts shows reasonable linear IV curve. **c,** Transconductance of WSe_2 FET versus gate voltage. **d,** Transfer curves of WSe_2 FET with Pt contacts on SiO_2. W/L = 5µm/0.5µm. **e** Transfer curves of WSe_2 FET with Pt contacts on h-BN. W/L = 3.2µm/0.8µm. **f,** Transfer curves of WSe_2 FET with Pt contacts on PMMA. W/L = 14µm/10µm. It can be seen that the the FETs show P-type characteristics with Pt contact independent of the substrates. Source drain voltage = 1V for all transfer curves.

versus gate voltage is plotted in **Figure 6.12e**. The real Schottky barrier height can then be determined at the flat band (V_{FB}) condition by adjusting the gate bias ($V_G = V_{FB}$). Analysis of the hole Schottky barrier height reveals that it is 200 meV, which leads to efficient injection of holes and acts as significant barrier for injection of electrons. The low Schottky barrier results in linear output curves – a necessary criteria for ohmic contacts – even at low temperature where thermal injection is limited (**Figure 6.12c**).

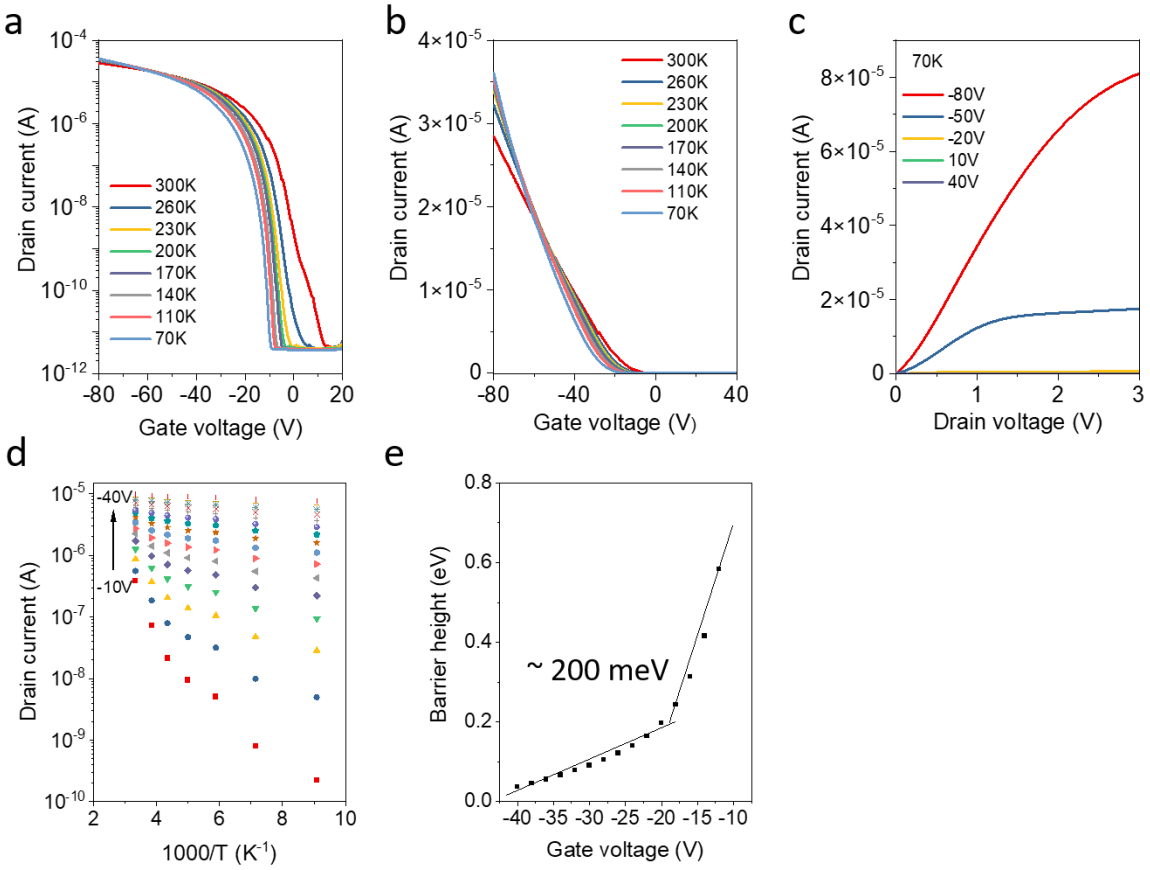


Figure 6.12 a, Transfer curves of WSe_2 FET with Pt contacts at different temperatures. **b**, Transfer curves from **a** plotted in linear form. W/L = 3.8µm/0.5µm. **c**, Output curves of the WSe_2 FET at 70 K showing linear characteristics at low temperature. **d**, Logarithm of the drain current plotted as a function of inverse of temperature at different gate biases from -10V to -40 V. **e**, Schottky barrier extraction indicating ~ 200 meV barrier for Pt contacted WSe_2.

6.4 Contact resistance of WSe_2 FETs

TLM results of WSe_2 FETs with Pt contacts are shown in **Figure 6.13a**. The contact resistance for P-type WSe_2 is around 6 kΩ·µm at carrier concentration of 3.75 ×10 ^{12} cm^{-2}. This value is lower than results from literature without any treatment of WSe_2 as summarized in **Figure 6.13b**. Chemical treatment of 2D TMDs is challenging in terms of stability and reproducibility. The clean van der Waals contact shows comparable contact resistance value compared to doped WSe_2 results and dry transferred contacts[120,238–241].

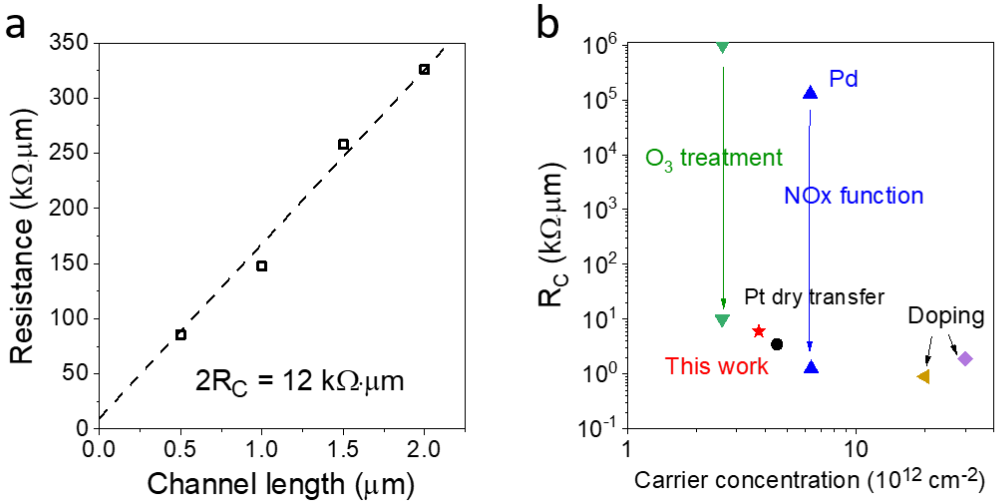


Figure 6.13 a, TLM results of WSe_2 FET with Pt contacts. **b,** Summarised contact resistance values of WSe_2 FETs from literature showing the contact resistance achieved by clean vdW contact is comparable to other strategies. Data taken from references[120,238–241].

6.5 Annealing effect for FETs with high work function metal contacts

In Chapter 5.5, I showed that the performance of MoS_2 FET with In/Au contacts improved after annealing at 200°C. Several studies reported improved 2D TMD device performance after annealing due to removal of surface absorbates[187,242,243]. The influence of thermal annealing on high work function metal contacted FET were investigated and the results are shown in **Figure 6.14**. The transfer curve of WSe_2 FETs shows pure P-type characteristics with high hole current

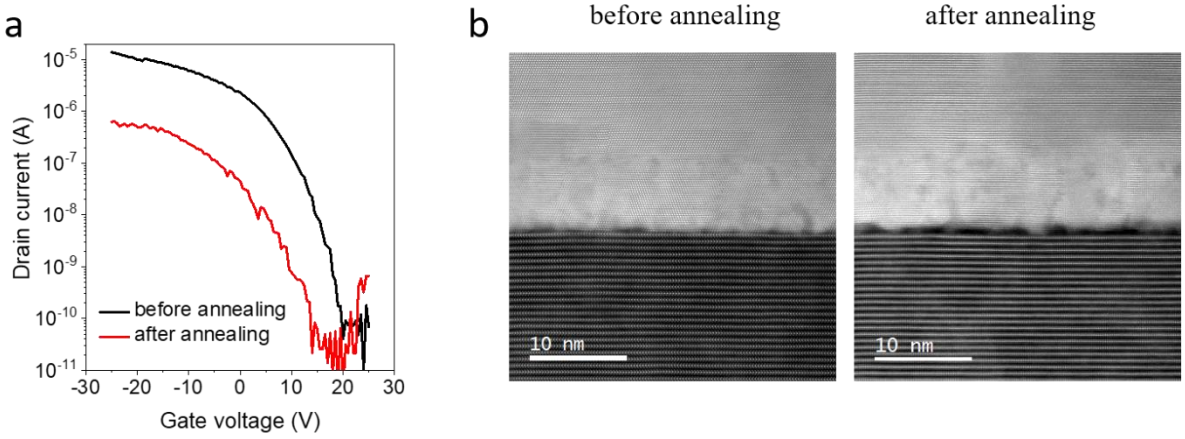


Figure 6.14 a, Transfer curves of WSe_2 FET with Pt contacts before and after thermal annealing. The results show that the hole current decreases post annealing. **b,** Cross-section STEM images of the Pt/WSe_2 contact before and after annealing. The Pt contact de-wets from the WSe_2 surface after thermal annealing.

before annealing. However, the current degrades by over one order of magnitude after annealing at 200°C in Ar/H_2. The cross-section STEM images of the Pt/WSe_2 contact before and after annealing are shown in **Figure 6.14b**. It shows that the Pt metal contact de-wets from the WSe_2 layer post annealing. This de-wetting decreases the area of physical contact between the WSe_2 and Pt metal, which leads to a decrease in current.

6.5.1 Monolayer WSe_2 FETs with Pt contacts

In addition to few-layered WSe_2, I have sought to realise high work function vdW contacts on monolayer WSe_2 grown by chemical vapor deposition (CVD). CVD WSe_2 was grown using the method reported by Liu *et al.*[244] on SiO_2 at high temperature. The samples were transferred to new substrates for device fabrication by the method described in section 4.1.4. The characterisation of CVD grown WSe_2 is shown in **Figure 6.15**. The Raman spectra show typical A_{1g} peak at 250 cm^{-1} and the PL spectra show a peak at ~1.65 eV.

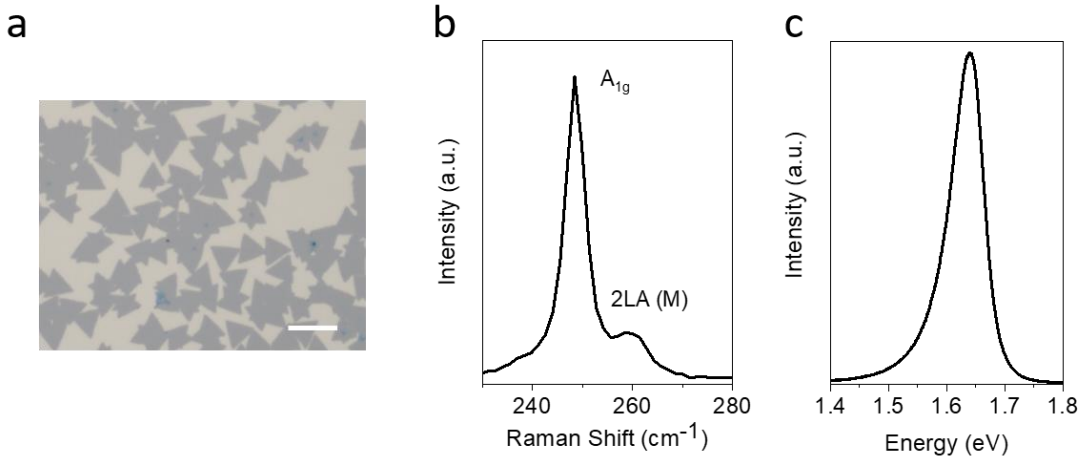


Figure 6.15 a, Optical microscope image of CVD grown WSe_2 on SiO_2. Scale bar = 10 µm. **b**, Raman of WSe_2 showing good quality WSe_2. **c**, PL of monolayer WSe_2 showing a peak at ~ 1.65 eV.

Atomic-resolution cross-section ADF STEM image of Pt on monolayer WSe_2 is shown in **Figure 6.16a**. The transfer characteristics of CVD grown monolayer WSe_2 FETs are shown in **Figure 6.16b**. It can be seen that the device shows purely P-type behavior with high saturation hole currents of ~ 10^{-6} A. The mobilities of monolayer devices were found to range from 1 – 20 of cm^2-$V^{-1}s^{-1}$. These results suggest that it is possible to fabricate clean vdW contacts using high work function metal contact Pt on CVD grown monolayer WSe_2 to achieve P-type FETs.

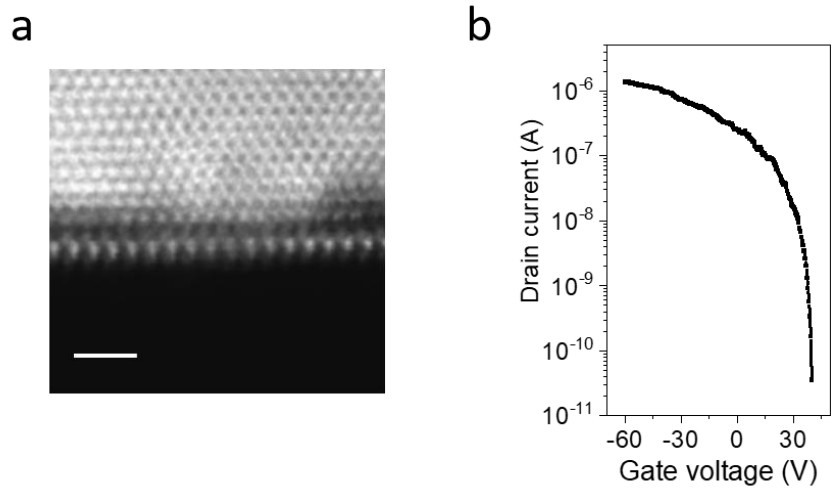


Figure 6.16 a, ADF STEM image showing clean interface between Pt and monolayer WSe_2. Scale bar = 1 nm. **b**, Transfer curve of monolayer WSe_2 with Pt contact showing pure P-type characteristics. W/L= 3.6 µm / 0.6 µm. Bias voltage = 1V.

6.6 P-type FETs based on 2D MoS_2

The conduction and valence band energies of MoS_2 are higher than those for WSe_2, which makes it more difficult to inject holes – even using the high work function metal contacts. In addition, Fermi level pinning by interface defects pins the metal work function near the conduction band. As a result, reported MoS_2 FETs with high work function metal contacts such as Pd and Pt typically show N-type characteristics[192,245–249]. Only dry transferred Pt contact was demonstrated to inject holes into MoS_2[124]. In this section, hole injection into MoS_2 can be achieved by clean van der Waals contacts deposited by standard e-beam evaporation. More importantly, as a proof of concept, the hole current in monolayer MoS_2 is demonstrated with high work function Pd metal contact for the first time.

6.6.1 Pd contacts on multilayer MoS_2

The Pd/MoS_2 interface was first characterised by cross-section ADF STEM. The Pd electrodes were evaporated on MoS_2 by the approach described in section 6.1. Clean vdW contacts of Pd on MoS_2 are achieved as shown in **Figure 6.17a**. The spacing between the Pd and S atoms is ~ 2.3 ± 0.1 Å. The absence of chemical bonding at the interface is confirmed by EELS analysis (**Figure 6.17b**) using a 0.9 Å electron beam probe focused on the sulfur atom adjacent to the deposited metal. The results show that the $L_{2,3}$ edge of the S atom (~ 164 eV and 175 eV indicated by the vertical blue lines in the figure) at the interface is the same as that of S atoms

in the layers away from the interface – suggesting that the electronic structures of the S atoms are the same and no chemical interaction occurs between S and Pd at the interface.

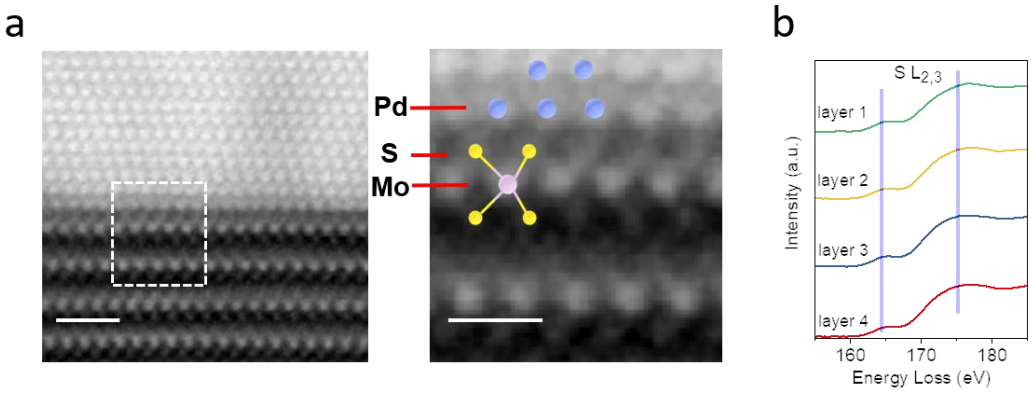


Figure 6.17 a, Atomic resolution annular dark field (ADF) STEM image showing clean interface between Pd and MoS_2. Scale bar = 1 nm. Right image is enlarged dashed rectangle region from left showing ADF STEM image where Mo, S and Pd atoms are visible. Scale bar = 0.5 nm. **b**, EELS showing that the electronic structure of S atoms in all layers is similar. Electron energy loss spectroscopy of the S $L_{2,3}$-edge, showing that the sulfur atoms of the top layer are completely unaffected by the deposition of metal on top.

The interface chemical interactions between Pd and MoS_2 were further investigated by XPS. The Pd 3*d* doublet spectra in **Figure 6.18a** showed only pristine Pd $3d_{3/2}$ at ~ 340.3 eV and Pd $3d_{5/2}$ at ~ 335.0 eV and no evidence for PdS_2[250] was observed. The MoS_2 signal was obtained by probing thin Pd film (~3 nm) deposited on freshly cleaved MoS_2 crystal. The binding energy values for the Mo 3*d* and S 2*p* doublets were found to be 229.3 eV (Mo $3d_{5/2}$)

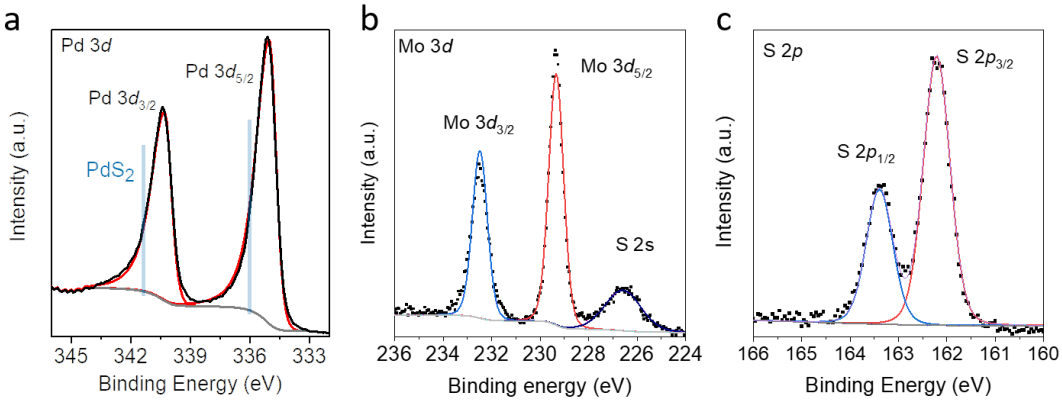


Figure 6.18 a, Pd 3*d* doublets from the Pd/MoS_2 interface showing pristine Pd metal signal. **b, c,** XPS of the Pd/MoS_2 interface showing pristine Mo and S doublets without any shift or intermediate states.

and 162.1 eV (S $2p_{3/2}$) - typical of pristine MoS_2. Nonstoichiometric MoS_X peaks were not observed. The results show that there is no doping or chemical reaction between Pd and MoS_2.

The characteristics of multilayer MoS_2 FETs with Pd contacts are shown in **Figure 6.19**. Remarkably, it can be seen from **Figure 6.19a** and **b** that the deposition of Pd on few-layered MoS_2 (SAM treated SiO_2 substrate) leads to primarily P-type FET transfer and output characteristics with the saturation hole current reaching ~ 10^{-5} A while the saturation electron current remains below 10^{-6} A. The hole mobility for MoS_2 was found to be 45 cm^2-$V^{-1}s^{-1}$ (g_m = 8.8×10^{-7}S). In addition, the influence of substrates (SiO_2, CVD grown h-BN on SiO_2, and PMMA on SiO_2) on hole injection into MoS_2 with high work function Pd contacts is shown in

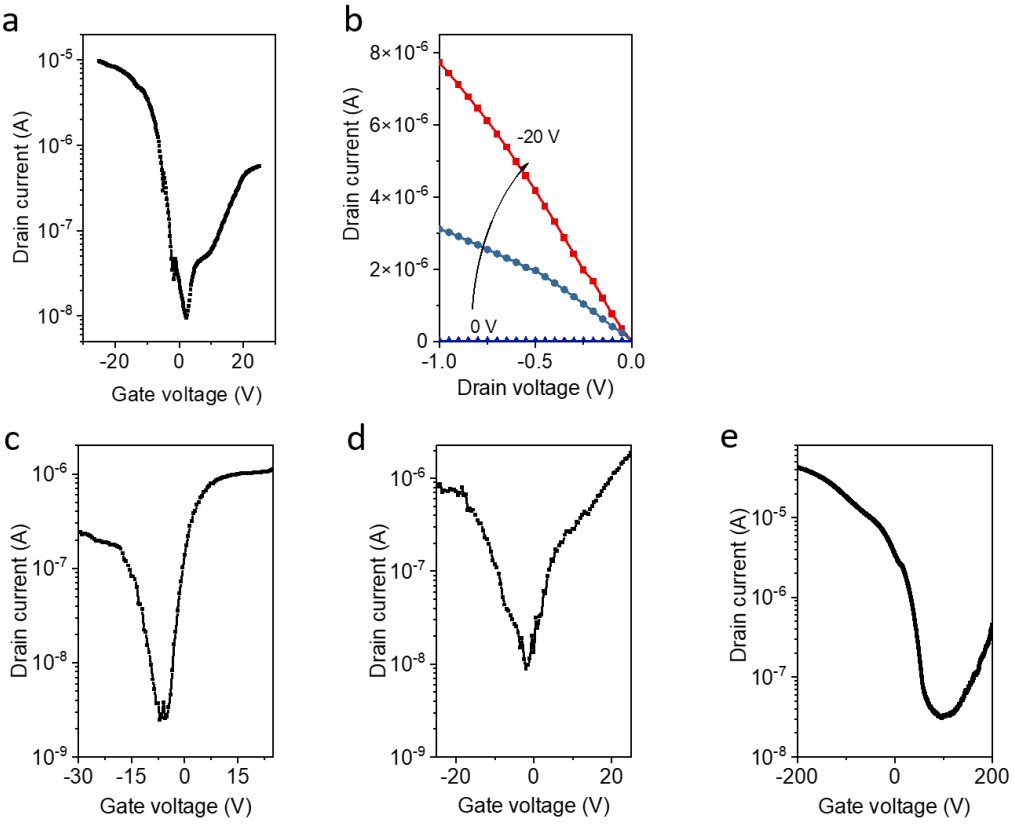


Figure 6.19 a, Transfer curves of MoS_2 FETs with Pd contacts on SAM treated SiO_2 showing ambipolar characteristic with higher hole current. W/L = 2.5µm/1.5µm. **b,** Output curves of MoS_2 FETs with Pd contacts showing linear IV curves. **c,** Transfer curves of MoS_2 FET with Pd contacts on SiO_2. W/L = 6µm/1.5µm. **d,** Transfer curves of MoS_2 FET with Pd contacts on h-BN/SiO_2. W/L = 2.8µm/1µm. **e,** Transfer curve of MoS_2 FET with Pd contacts on PMMA/SiO_2. W/L = 16µm/10µm. It can be seen that FETs show efficient high hole currents with Pd contacts on MoS_2. SAM treated SiO_2 and PMMA substrates can suppress the electron doping that lead to higher hole currents. Source drain bias voltage = 1V for all transfer curves.

Figure 6.19 c-e. It can be seen that MoS_2 FETs show high hole currents with clean vdW Pd contacts. Due to electron doping from SiO_2, the FETs fabricated on SiO_2 substrates exhibit slightly lower hole current compared to the electron current. The PMMA substrates suppress the electron doping and therefore two orders of magnitude higher hole current compared to electron current is achieved for MoS_2 FETs.

The transfer characteristics of MoS_2 FETs with Pd contact measured at different temperatures are shown in **Figure 6.20a** and **b**. The device showed ambipolar characteristics with high hole currents down to 40K. The hole Schottky barrier height is lower than electron Schottky barrier height. Thus, the hole current branch exhibits a strong temperature dependent behavior due to thermal injection transport. In contrast, the electron branch does not change significantly with measurement temperatures due to tunneling dominant transport. The barrier height extracted from the slope of the Arrhenius plot in which the logarithm of the drain current is plotted as a function of inverse of temperature at different gate biases. The extracted barrier height versus gate voltage is plotted in **Figure 6.20c**. Analysis of the hole Schottky barrier height reveals that it is ~ 500 meV. The fact P-type operation can be achieved with such a large Schottky barrier via modulation of Fermi level with gate voltage indicates that the Pd/2D MoS_2 interface is clean and the Fermi level is unpinned.

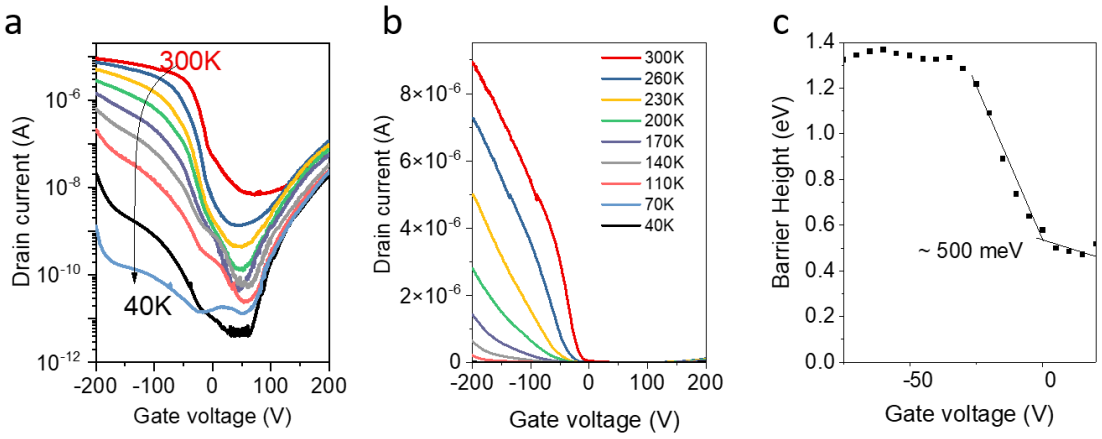


Figure 6.20 a, Transfer curves of MoS_2 device with Pd contacts on PMMA on SiO_2 substrates at different temperatures. The hole transport part showed a more obvious temperature dependence compared to the electron branch, indicating thermally activated transport for holes and tunnel dominant transport for electrons due to higher Schottky barrier for electrons. **b**, Transfer curves from **a** plotted linearly. **c**, Barrier height versus gate voltage data indicate ~ 500 meV for hole Schottky barrier height.

6.6.2 Pt contacts for multilayer MoS_2

The Pt/MoS_2 interface was characterized by cross-section ADF STEM and XPS shown in **Figure 6.21**. Clean vdW contacts of Pt on MoS_2 were achieved as shown in **Figure 6.21a**. Absence of chemical interactions between Pt and S atoms at the interface was confirmed by several XPS analysis. The Pt 4*f* spectra show only pristine Pt $4f_{5/2}$ at ~ 74.3 eV and Pt $4f_{7/2}$ at ~ 71.0 eV and no evidence for PtS formation[251]. The Mo 3*d* signal analysis was obtained by probing thin Pd film (~3 nm) deposited on MoS_2 crystal. Unlike Pt/WSe_2 interface, no binding energy shift was observed for Pt/MoS_2. The results show that Pt does not react with MoS_2 and no electron/ hole doping occurs.

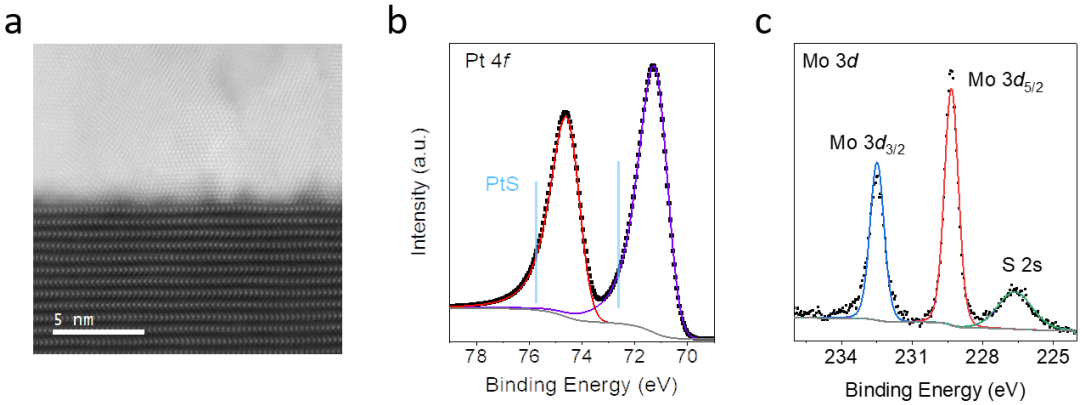


Figure 6.21 a, Atomic-resolution ADF STEM image of Pt/MoS_2 showing clean interface between Pt and MoS_2. **b**, Pt 4*f* doublets showing pristine Pt metal without any PtS signal. **c**, XPS of the Pt/MoS_2 interface showing pristine Mo 3*d* doublets without any shift or intermediate states.

The characteristics of multilayer MoS_2 FETs with Pt contacts are shown in **Figure 6.22**. Ambipolar characteristics with higher electron current were observed for MoS_2 FETs on SAM treated SiO_2 substrates. For comparison, the influence of substrates (SiO_2, CVD grown h-BN on SiO_2, and PMMA on SiO_2) on hole injection into MoS_2 with high work function Pt contacts is shown in **Figure 6.22 c-e**. Due to electron doping from SiO_2, devices fabricated on SiO_2 substrate show only tens of nA of hole current. The h-BN, PMMA substrates show higher hole currents for MoS_2 FETs. Even though both Pd and Pt metal contacts form clean vdW contacts with MoS_2, the results reveal that Pt is less effective for hole injection compared to Pd. This is probably due to the slightly lower work function measured by UPS as shown in Figure 6.4.

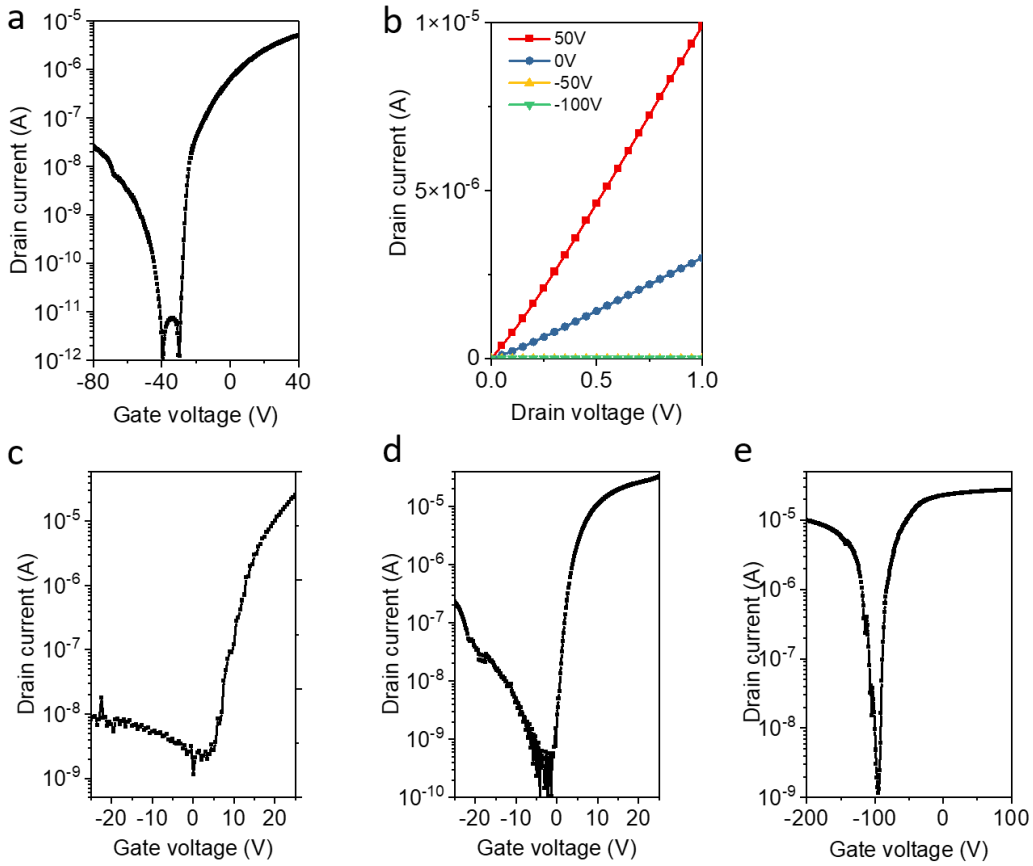


Figure 6.22 a, Transfer curves of MoS_2 FETs with Pt contacts on SAM treated SiO_2 showing ambipolar characteristics with higher electron current. W/L = 2µm/0.5µm. **b,** Output curves of MoS_2 device with Pt contacts showing linear IV curves. **c,** Transfer curves of MoS_2 FET with Pt contacts on SiO_2. W/L = 2µm/0.8µm. **d,** Transfer curves of MoS_2 FETs with Pt contacts on h-BN/SiO_2. W/L = 6µm/2µm. **e,** Transfer curve of MoS_2 FETs with Pt contacts on PMMA/SiO_2. W/L = 18µm/10µm. It can be seen that FETs show some hole current with Pt contacts on MoS_2. Source drain bias voltage = 1V for all transfer curves.

6.6.3 Monolayer MoS_2 FETs with Pd contacts

In addition to few-layered MoS_2, I have investigated high work function vdW contacts on single layer MoS_2 grown by chemical vapor deposition (CVD). CVD MoS_2 samples were grown using the method described in section 4.1. Cross-section ADF STEM image of Pd on monolayer MoS_2 is shown in **Figure 6.23a**. The transfer characteristics of CVD grown monolayer MoS_2 FETs are shown in **Figure 6.23b**. The device shows ambipolar behavior with higher hole currents relative to electron currents. Hole injection into monolayer MoS_2 is exceptionally difficult even with clean contacts of high work function metals because the valence band is located > 6 eV below the vacuum level, which means that there is a significant

barrier for hole injection. The fact that we are able to obtain hole currents in monolayer MoS_2 FETs is consistent with realisation of clean vdW contacts and absence of Fermi level pinning.

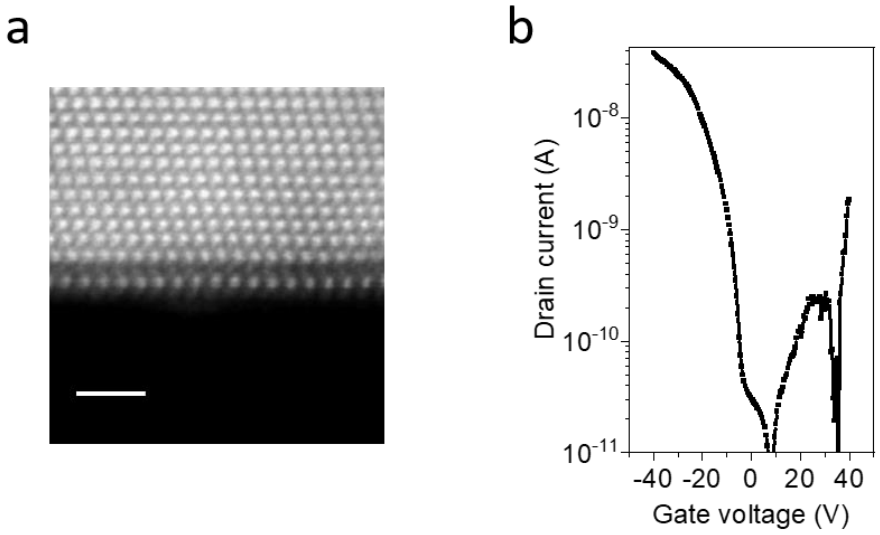


Figure 6.23 a, ADF STEM image showing clean interface between Pt and monolayer MoS_2. Scale bar = 1 nm. **b**, Transfer curve of monolayer MoS_2 with Pt contact ambipolar behavior with higher hole current than electron current. Source drain bias voltage = 1V for the transfer curve.

6.7 Effect of substrates on 2D TMD FETs

6.7.1 Fermi level of MoS_2 on different substrates

To realise high performance P-type 2D FETs with high work function metals as contacts, electron doping from the substrate must be suppressed. In section 6.3, FET results from 2D TMDs on different substrates (SiO_2, h-BN, PMMA) were described. The results show that the substrates influence the hole current levels of P-type FETs. Thus, it is important to understand how the substrates affect electronic properties of 2D TMDs. In this section, I show Kelvin Probe Force Microscopy (KPFM, see section 2.2.3) results on 2D TMDs on different substrates.

The Fermi level energy level of the 2D TMDs can be extracted from the KPFM results. Given the assumption that the conduction and valence band energy levels do not vary with different substrates, the KPFM results represent the carrier concentrations in 2D TMDs. **Figure 6.24a** shows AFM and KPFM images of MoS_2 on different substrates such as SiO_2, SAM treated SiO_2, CVD grown h-BN, PMMA, Al_2O_3, and mechanically exfoliated h-BN. The Fermi energy level (relative to vacuum) of the MoS_2 flakes are indicated in the KPFM images and summarized in **Figure 6.24b.** In the figure, the conduction band of pristine few layered MoS_2 is located at 3.9 eV and the valence is located at 5.2 eV. The Fermi level indicated by the dashed

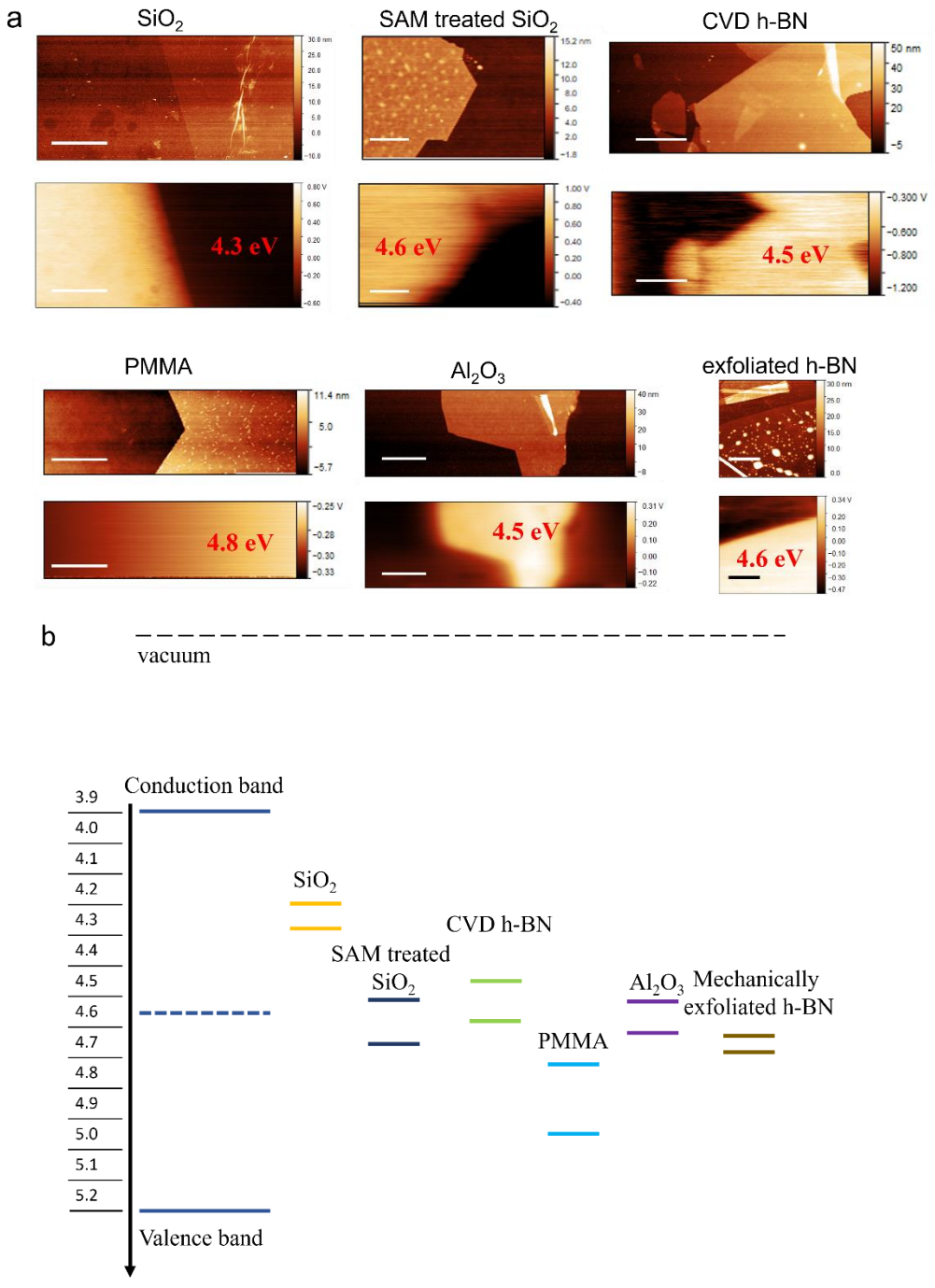


Figure 6.24 a, AFM and KPFM results of MoS_2 flakes on different substrates such as SiO_2, SAM treated SiO_2, CVD grown h-BN, PMMA, Al_2O_3, and mechanically exfoliated h-BN. **b**, Summary of Fermi level positions of MoS_2 on different substrates. The two lines for each substrates represent the Fermi level range measured from several samples. The energy in eV increases in the direction indicated by the arrow. Scale bars are 5 μm.

line is assumed to be in the middle of the gap. The Fermi level of MoS_2 shifts dramatically for different substrates. The electron doping from bare SiO_2 substrate is clearly indicated by the

Fermi level shifting closer to the conduction band. In contrast, hole doping from PMMA substrate is indicated by the Fermi level shift towards the valence band. Two lines for each type of substrate represent the range of the Fermi level energies measured on several samples.

Al_2O_3 and mechanically exfoliated h-BN substrates are also included for comparison. The results show they tend to give intrinsic MoS_2 without significant doping. Although several groups observed electron doping of TMDs by encapsulating them with HfOx or AlOx thin films[162,252–255], it is not very clear how these oxides affect the TMDs. The doping level of MoS_2 is inferred by Raman spectroscopy but more accurate doping type and doping levels should be assessed by Hall measurements. Hole doping of 2D TMDs with dielectrics could be useful for realising high performance P-type FETs together with vdW high work function metal contacts.

6.7.2 FETs on h-BN substrates

Mechanically exfoliated h-BN is frequently used to encapsulate TMDs to avoid interactions with the environment for FETs and optical measurements. The MoS_2/h-BN heterostructure was stacked by the dry transfer method described in 4.1.3. The optical microscope image of the device is shown in **Figure 6.25a**. The MoS_2 and h-BN flakes are labelled in the Figure. Two pairs of Pd contacts were made on MoS_2 and MoS_2/h-BN. The transfer curves of the FETs show that the MoS_2 FET with h-BN substrate has higher hole current and lower electron current than MoS_2 FET on SiO_2.

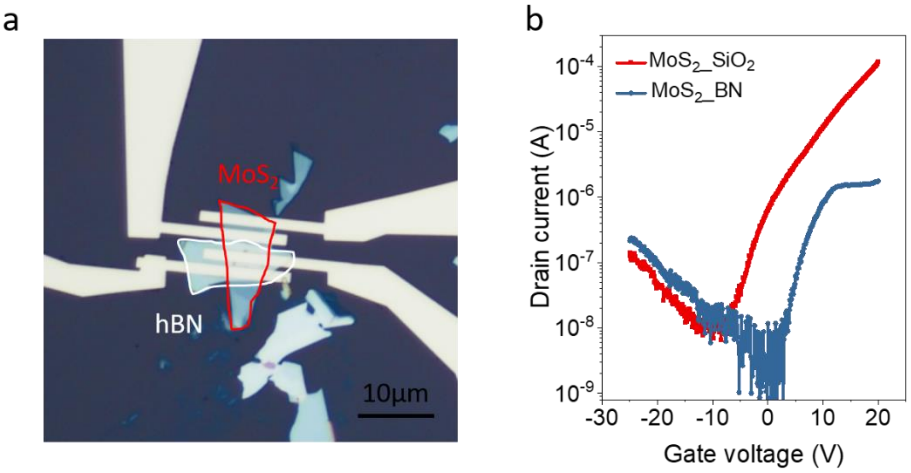


Figure 6.25 a, Optical microscope image of MoS_2 FET with Pd contacts. MoS_2 flake partially sits on mechanically exfoliated h-BN. W/L = 8μm/2μm. **b**, Transfer curves of MoS_2 FETs show that the MoS_2 FET with h-BN substrate has higher hole current and lower electron current than MoS_2 FET on SiO_2. Source drain voltage = 1V for transfer curves.

6.7.3 MoS_2 FETs on WSe_2 and WS_2 as substrates

After investigation of h-BN as substrate, I further studied MoS_2 FET performance with other TMDs such as WSe_2 and WS_2 as substrates to screen electron doping from SiO_2. The devices were designed in such a way that Pd electrodes only contact MoS_2 flake for MoS_2/WSe_2 and MoS_2/WS_2 heterostructures. The optical microscope images of the devices are shown in **Figure 6.26a** and **c**, where the MoS_2, WSe_2 and WS_2 flakes are labelled. **Figure 6.26b** shows that the hole current of the MoS_2 FET on WSe_2 is two orders of magnitude higher than the hole current of the MoS_2 FET on SiO_2. **Figure 6.26d** further shows that the hole current of the MoS_2 FET on WS_2 is one order greater than the hole current of the MoS_2 FET on SiO_2.

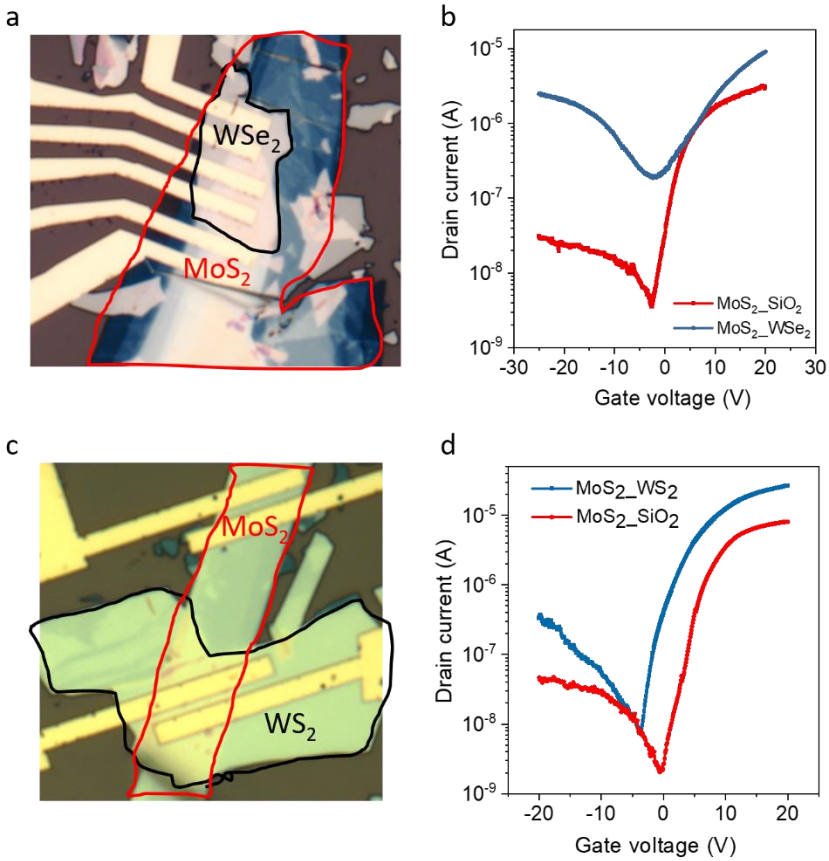


Figure 6.26 a, Optical microscope image of MoS_2 FET with Pd contacts. The large MoS_2 flake covers the mechanically exfoliated WSe_2 flake. MoS_2: W/L = 10μm/2μm. MoS_2/WSe_2: W/L = 8μm/2μm. **b**, Transfer curves of MoS_2 FETs show that the MoS_2 FET with WSe_2 substrate has higher hole current than MoS_2 FET on SiO_2. **c**, Optical microscope image of MoS_2 FET with Pd contacts. The MoS_2 flake covers the mechanically exfoliated WS_2 underneath. MoS_2: W/L = 5μm/1μm. MoS_2/WS_2: W/L = 8μm/1μm. **d**, Transfer curves of MoS_2 FETs show that the MoS_2 FET with WS_2 substrate has higher hole current than MoS_2 FET on SiO_2. Source drain voltage = 1V for transfer curves.

These device characteristics could be interpreted as the formation of a new heterostructure semiconductor that has the conduction band of MoS_2 and valence band of WSe_2. This is supported by the fact that a PL peak at a lower energy level is commonly observed in MoS_2/WSe_2 or $MoSe_2/WSe_2$ heterostructures[256,257]. This is attributed to interband energy level between conduction band of MoS_2 and valence band of WSe_2. Thus, the hole Schottky barrier for MoS_2/WSe_2 is lower than MoS_2 with Pd contacts and therefore the devices show higher hole currents.

6.7.4 Al_2O_3 substrates

As discussed in section 6.4.1, the Fermi level of MoS_2 on Al_2O_3 substrate is close to the middle of the bandgap, indicating no electron or hole doping from the substrate. The MoS_2 FETs with Pd contacts and WSe_2 FETs with Pt contacts were fabricated and tested on Al_2O_3. 30 nm of Al_2O_3 was deposited on highly doped silicon by atomic layer deposition (ALD) as the dielectric layer. The FET characteristics of MoS_2 and WSe_2 on Al_2O_3 are shown in **Figure 6.27**. The transfer curve of MoS_2 FET in **Figure 6.27a** shows ambipolar characteristics with higher electron current and the WSe_2 FET in **Figure 6.27b** shows purely P-type transfer curve. We have found that MoS_2 or WSe_2 FETs employing Al_2O_3 substrates as dielectric show higher hole currents than SiO_2, but lower hole currents than SAM treated SiO_2. Further exploration

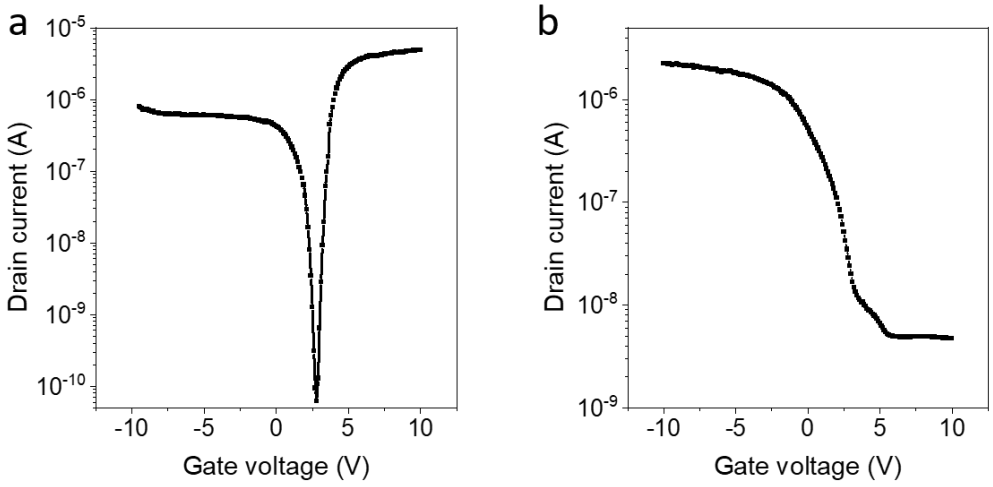


Figure 6.27 a, Transfer curve of MoS_2 FET with Pd contacts on Al_2O_3 dielectric showing ambipolar characteristic with higher electron current. W/L = 6µm/10µm. **b,** Transfer curve of WSe_2 device with Pt contacts on Al_2O_3 dielectric showing pure P-type characteristics. W/L = 8µm/10µm. Source drain bias voltage = 1V for transfer curves.

on how high *k* dielectric oxides affect the TMDs will be beneficial for realising high performance P-type FETs.

6.7.5 PMMA, PVC encapsulation of 2D TMD FETs

The KPFM results shown in **Figure 6.28** indicate slight hole doping of MoS_2 by PMMA. Here, I show PMMA effects on FET performance before and after PMMA encapsulation. The transfer curves of MoS_2 FET with Pd contacts (on SiO_2 substrate) are shown in **Figure 6.28**. The device before PMMA encapsulation shows ambipolar behavior with higher electron current. After PMMA coating, the electron current branch dramatically decreased while the hole current remains similar.

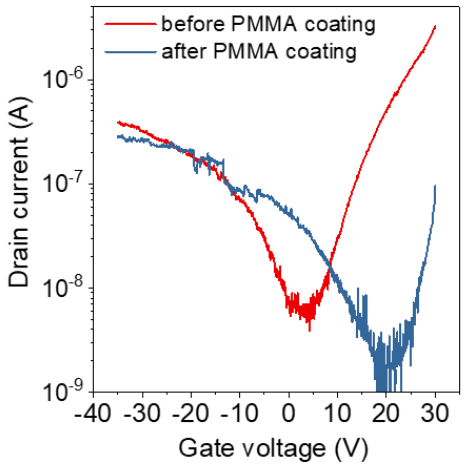


Figure 6.28 Transfer curves of MoS_2 FET with Pd contacts before and after PMMA encapsulation. The electrical measurements show that the electron current branch decreases after PMMA encapsulation. Source drain bias voltage = 1V for transfer curves.

Polyvinyl cinnamate (PVC) has been widely used in organic FETs as a dielectric layer[258–261]. I therefore investigated PVC as top gate dielectric for SiO_2 bottom gated MoS_2 and WSe_2 FETs. PVC was spin coated onto the devices. Unfortunately, the top gate FETs did not work. However, the bottom gated device showed significant hole current enhancement after capping with PVC. The transfer curves of MoS_2 and WSe_2 FETs before and after PVC encapsulation (measured with bottom gate) are shown in **Figure 6.29**. Transfer curves of MoS_2 FETs show that the electron current decreased while hole current increases after PVC coating. Transfer curves of WSe_2 FETs show that the hole current increases over two orders of magnitude after PVC coating.

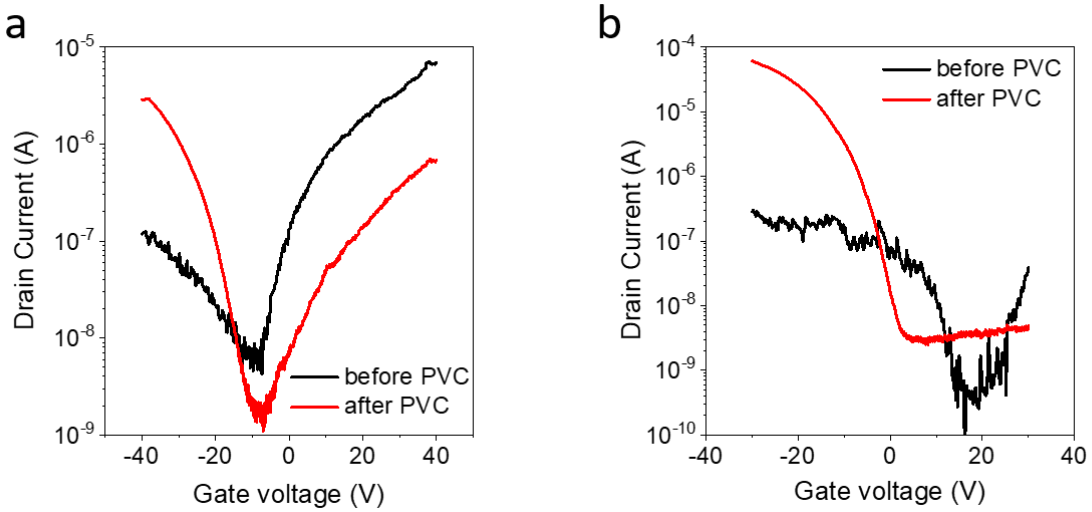


Figure 6.29 a, Transfer curves of MoS_2 FET with Pd contacts before and after PVC coating. The results show that the electron current decreases while the hole current increases after PVC coating. W/L = 1.5µm/1µm. **b,** Transfer curves of WSe_2 FET with Pd contacts before and after PVC coating. Before PVC coating, the WSe_2 FET showed poor device performance with only hundreds of nA current. The hole current increases over two orders of magnitude after PVC coating. W/L = 5µm/2µm. Source drain bias voltage is 1V for transfer curves.

6.8 Asymmetric contacts for photodiode

The integration of N- and P-type vdW contacts onto 2D TMDs in ultra-thin photovoltaics and photodiodes is demonstrated in this section. The schematic of the device is shown in **Figure 6.30a** where indium alloy vdW contacts described in Chapter 5 are used or electron injection and high work function vdW contacts based on Pt and Pd in this Chapter are utilised for hole injection. This way, metal-semiconductor-metal (MSM) diodes on the same 2D TMD are realised. The FET output curves for In/Au-MoS_2-Pd devices shown in **Figure 6.30b** exhibit diode characteristics at all gate voltages, with a rectification ratio of up to 10^6. The diode properties in dark and under illumination are shown in **Figure 6.30c**. A significant photocurrent is generated under illumination and open circuit voltage of ~ 0.5 V is obtained. The corresponding power conversion efficiency is calculated to be ~ 0.40 % and power output of 267 nW is obtained at Vm= 0.3 V (maximum power output point). A similar device consisting of In/Au-WSe_2-Pt also exhibited diode-like behavior at different gate voltages (**Figure 6.30d**) with a rectification ratio of up to 10^7. The current-voltage characteristics under dark and illumination for the In/Au-WSe_2-Pt devices are shown in **Figure 6.30e**. The open circuit

voltage measured in these devices is larger (0.6 V), which results in higher conversion efficiency of 0.82 % with a maximum power output of 572 nW at Vm= 0.35 V.

To evaluate the photocurrent generation efficiency of the MSM diodes, the photoresponsivity $R = \frac{I_{sc}}{P_{laser}}$ was extracted, where I_{sc} is the short-circuit current and P_{laser} is the laser power. With R determined, we can further extract the external quantum efficiency $EQE = \frac{Rhc}{e\lambda}$,where h, c, e and λ are Planck's constant, the speed of light, the electron charge and the laser wavelength, respectively. The responsivity of the photodiodes was found to be

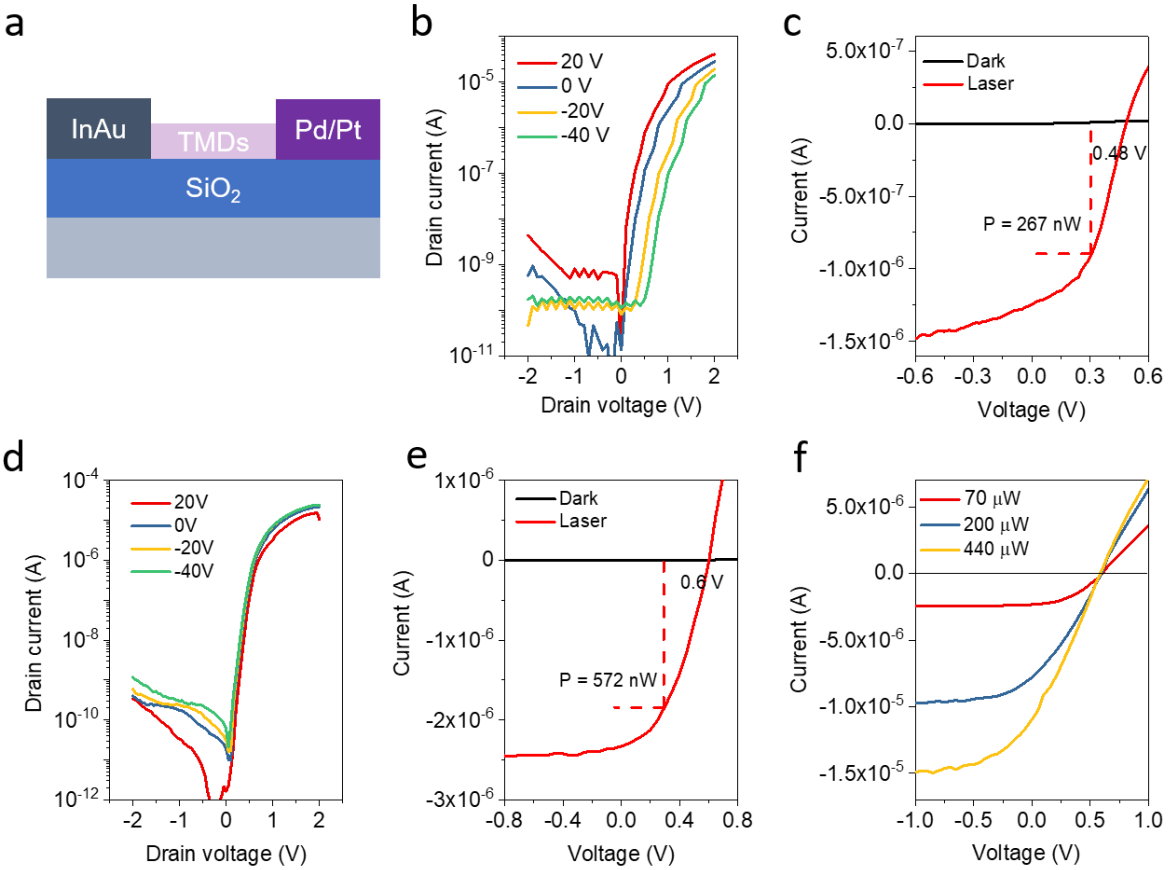


Figure 6.30 a, Schematic illustration of assymetric contacts diode. b, Output curves of MoS_2 device with In/Au and Pd contacts showing good rectification behavior. **c**, I-V curves of the diode under dark and illumination (532 nm, 70 μW), demonstrating open circuit voltage of 0.48 V and output power of 267 nW. The red dashed lines show the corresponding power area for maximum power conversion. **d,** Output curves of WSe_2 device with In/Au and Pt contacts showing good rectification behavior. **e,** I-V curves of the diode under dark and illumination (532 nm, 70 μW), demonstrating an open circuit voltage of 0.6 V and output power of 572 nW. **d,** I-V curves under different illumination power showing increasing current and stable open voltage.

17.6 mA W^{-1} and 33.1 mA W^{-1} with external quantum efficiencies of 4.1% and 7.7% for the In-MoS_2-Pd and In-WSe_2-Pt devices, respectively. The photodiode properties (power output, power conversion efficiency, responsivity and external quantum efficiencies) for MoS_2 and WSe_2 devices are among the highest reported[216,262,263]. We have also measured diode properties at three different laser powers as shown in **Figure 6.30d**. It can be seen that the photocurrent increases with power but the open circuit voltage (defined by the contacts) remains constant.

6.9 Summary

I have demonstrated clean vdW contacts based on high work function metals such as Pd and Pt on few- and single-layered MoS_2 and WSe_2 TMDs. These contacts lead to some P-type characteristics on single layer MoS_2 and purely P-type on WSe_2. The results also suggest that the Fermi level is unpinned and can be modulated with gate voltage. Although the hole current is limited by substrate electron doping, hole injection is still effective with clean contacts. To demonstrate the reproducibility of high-performance P-type FETs, the electron to hole current ratios of MoS_2 (421 devices in total) and WSe_2 (263 devices in total) are plotted in **Figure 6.31**. **Figure 6.31a** shows the summarised results for MoS_2 FETs with different contacts (In, Au, Pd, and Pt) and different substrates (SiO_2, CVD h-BN, PMMA, and SAM treated SiO_2). The left side of the purple dashed line represents the region where the hole current is dominant and the right side represents the electron current dominant region. Most devices on MoS_2 are N-type. This is because it is exceptionally challenging to inject holes into MoS_2 and it is also very challenging to make vdW contacts. The latter is responsible of N-type devices even when Pd or Pt metals are used as contacts due to Fermi level pinning near the conduction band. In general, however, Pd contacts are better for P-type characteristics compared to other metal contacts for MoS_2 FETs. **Figure 6.31b** shows the summarised results for WSe_2 with different contacts and different substrates. Majority of WSe_2 FETs show hole current dominant characteristics. Due to chemical reactions between Pd and WSe_2, the Pt contacts give better P-type characteristics than the Pd contacts.

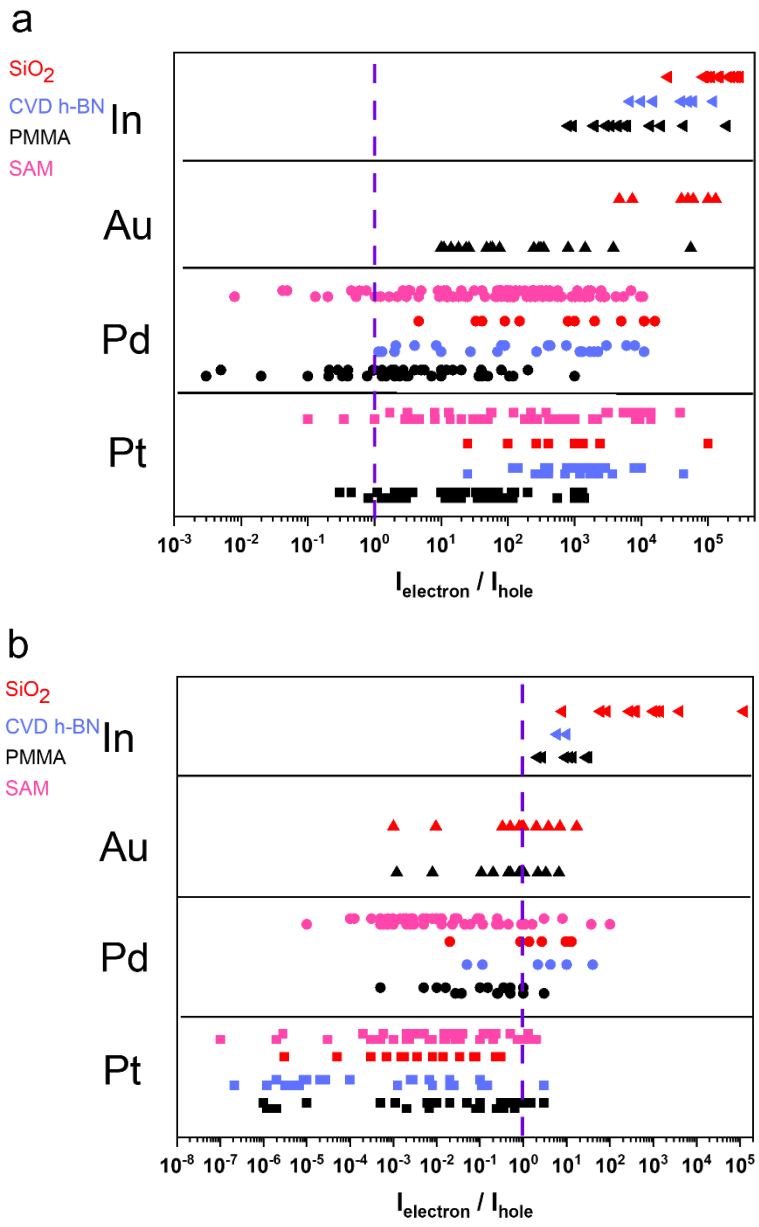


Figure 6.31 a, Summarised results of electron to hole current ratios for MoS_2 FETs with different metal contacts (In, Au, Pd, and Pt) and different substrates (SiO_2, CVD h-BN, PMMA, and SAM treated SiO_2). High work function Pd metal contacts show high reproducibility of hole injection in MoS_2 on SAM treated SiO2 substrates and PMMA. **b,** Summarised results of electron to hole current ratios for WSe_2 FETs with different metal contacts and different substrates. Majority of WSe_2 FETs show dominant hole current characteristics.

7 Summary and Future work

In this Chapter, key achievements of this thesis are summarised. Future work based on my findings is proposed to further explore the metal-TMD interface.

To reap the benefits of TMD semiconductors for short channel FETs, the issue of high contact resistance and severe Fermi level pinning observed with different TMDs must be solved. During my doctoral research, I have carefully characterized interfaces between different 3D metals and single layer 2D TMDs. Based on the knowledge gained from this work, I developed a strategy based on soft metals to realize ultra-clean vdW contacts on single layer 2D semiconductors such as MoS_2. Using scanning transmission electron microscopy (STEM) imaging, I have shown that the indium alloy-MoS_2 interface is atomically sharp with no detectable chemical interaction between the metal and semiconductor, suggesting van-der-Waals-type bonding between the metal and monolayer MoS_2. Using electronic transport measurements, I have shown that the contact resistance of indium electrodes is ~ 3000 $\Omega \cdot \mu m$ for single layer and ~ 800 $\Omega \cdot \mu m$ for few layered MoS_2 – amongst the lowest observed for 3D metal electrodes evaporated on MoS_2 and is translated into high performance FETs with mobility of ~ 167 $cm^2\text{-}V^{-1}\text{-}s^{-1}$. I have also demonstrated low contact resistance of 220 $\Omega \cdot \mu m$ on ultrathin NbS_2 and near ideal band offsets, indicative of defect free interfaces, in WS_2 and WSe_2 contacted with indium. In addition, the soft nature of indium allows it to form stable alloys with different metals, which can be used to adjust the work function of the electrodes while maintaining the ultra-clean interface with TMDs. The tunable device performance with In, In/Au, In/Pd, and In/Pt on WSe_2 FETs suggest the interface between indium alloys and WSe_2 is free of Fermi level pinning. I have further demonstrated that other soft metals such as Ag and Ga can also work as efficient electron injection contacts for TMDs due to their low work function values. This work provides a simple method for making ultra-clean vdW contacts using standard laboratory technology on single layer 2D TMDs.

The second important challenge is to achieve P-type FETs on TMDs with hole injection, which would allow fabrication of basic logic circuit components (integrated with indium contacts for N-type FETs) without heterostructure growth or transfer. However, achieving P-type devices from evaporation of high work function metals onto 2D TMDs has proven to be exceptionally challenging. While mechanical transfer of Pt on multi-layered WSe_2 and MoS_2 has been reported, P-type devices on single layered WSe_2 and MoS_2 have yet to be realised. Furthermore, the stacking dry transfer is not feasible for large area device applications.

Therefore, I have developed the approach to realise high-performance purely P-type devices on single and few-layered MoS_2 and WSe_2 using industry compatible electron beam evaporation of high work function metals such as Pd and Pt. Using atomic resolution imaging and spectroscopy, I have demonstrated near ideal vdW interfaces without chemical interactions between the high work function metals and 2D TMDs. For WSe_2, electronic transport measurements reveal that P-type FETs based on vdW Pt contacts exhibit high mobility values of ~ 190 cm^2-$V^{-1}s^{-1}$ at room temperature with saturation currents of > 10^{-4} Amperes (A) and on/off ratio of 10^7. Although the valence band of MoS_2 is higher than WSe_2, I have also successfully fabricated ambipolar FETs with high hole currents on MoS_2 with clean vdW Pd contacts. More importantly, P-type FETs on monolayer WSe_2 and the P-type characteristics on monolayer MoS_2 have also been demonstrated with clean vdW contacts.

Finally, I have showed an ultra-thin photovoltaic cell based on N- and P-type vdW contacts with an open circuit voltage of 0.6 V and power conversion efficiency of 0.82% – among the highest reported. The demonstration of high-performance N- and P-type contacts on 2D TMDs solves a fundamental problem in the field and opens up pathways for realising the full potential of atomically thin body semiconductors for novel electronic devices.

Looking forward, the contact engineering for TMDs remains challenge to achieve the quantum Looking forward, contact engineering for TMDs remains the key challenge for novel devices. Future contacts must achieve quantum resistance. I suggest the following approaches for achieving quantum limit of contacts on 2D TMDs.

1. **Degenerate doping of 2D TMDs with metal contacts for P-type FETs**
   Shen *et al.* reported degenerate doping of MoS_2 with bismuth contact to achieve low contact resistance for N-type FETs[132]. In the study of high work function metals as contacts, no evidence of significant hole doping of TMDs from Pd or Pt was observed. In **Figure 5.12** of this thesis, I show that vdW contacts introduce tunnel barriers between the metal and 2D TMD that act to increase the contact resistance. Therefore, other contact metals similar to bismuth that minimise or eliminate the tunnel barrier thickness and dope the 2D TMDs should be found and investigated.
2. **Tuning the work function of metals on 2D TMDs**
   TEM studies show strong epitaxial alignment between MoS_2 and (220) oriented Au[229,264]. The work function is strongly dependent on the crystal orientation of the metal[234]. It would be interesting to further investigate if preferred crystal orientations of metals on TMDs

could be controlled as a way to alter the metal work function and Schottky barrier height between metal and TMDs.

3. **Doping from dielectric insulators**

   To realise high performance P-type FETs on TMDs, the electron doping effect from SiO_2 must be suppressed. However, the dielectric substrate doping effects on atomically thin semiconductors are not very clear. Zheng *et al.* reported different carrier concentrations of MoS_2 grown on different complex oxide substrates[265]. The carrier concentration was extracted by comparing the trion to exciton ratios[266]. Hall measurements should preferred be performed to determine the carrier concentrations in TMDs on different substrates.

4. **Electronic structure of TMDs on different substrates**

   The influence of electronic interactions at the MoS_2−SiO_2 interface was studied by Lee et al. using X-ray spectroscopy (XAS and XPS) and calculations[267]. The results show that the O ions in SiO_2 adjacent to S in MoS_2 participate in orbital hybridization so that O 2*p* contributes to both the valence and conduction bands of the system. The conduction/valence band edges can be measured by scanning tunneling microscopy[268]. Alternatively, ionic gate spectroscopy allows the determination of semiconducting bandgap in a simple way- directly from the transfer characteristics of FETs[269,270]. This could be applied to study the electronic structure of TMDs on different substrates.

5. **2D/2D heterostructures**

   The electronic structure of 2D TMDs is also affected by 2D dielectrics, graphene and other 2D semiconductors. The modification of 2D semiconductors by putting them on other 2D materials can be applied to tune the band alignment with high work function metal contacts to achieve pure P-type FETs. Raja *et al.* demonstrated that the dielectric environment can be modified by capping monolayer WS_2 or WSe_2 with layers of graphene and h-BN[271]. It was found that increased dielectric screening reduced the electronic band gap and exciton binding energy in the range of hundreds meV. Electronic bandgap of monolayer $MoSe_2$ on graphene measured by scanning tunneling microscopy showed 11% difference compared to $MoSe_2$/HOPG due to different dielectric screening properties of the substrates[272]. The MoS_2/WS_2 heterostructure FETs showed an improvement in FET device performance compared to MoS_2 FETs on SiO_2 due to the suppression of Coulomb scattering[273]. These approaches can be pursued for optimisation of electronic structure of 2D semiconductors for hole transport.

6. Novel device structures enabled by vdW N- and P-type contacts

Next generation of electronic devices will rely on new device operating mechanisms. For example, tunnel (T) FETs that offer ultra-low power device operation. 2D TMDs are ideally suited for TFETs but absence of P- and N-type doping has hampered their progress. The methodology described in this thesis can be used to achieve P- and N-type doping via contacts to realise TFETs with subthreshold slope values of < 60mV/decade and operation at low voltage.

8 Appendix

8.1 Plasma treatment of TMDs

O_2 plasma treatment prior to contact metal deposition has been reported by several groups to achieve P-type FETs using MoS_2 and WSe_2[274–276]. I investigated O_2 plasma treatment on MoS_2 to study its influence on contact properties. The optical images of a MoS_2 sample (contact region developed after E-beam lithography) before and after O_2 plasma treatment (10W, 10s) are shown in **Figure 8.1a** and **b**. No obvious damage on MoS_2 could be observed from optical images. However, FET from MoS_2 treated by O_2 plasma showed very low currents as seen in **Figure 8.1c**. To understand why the device showed such poor performance, cross-section STEM was conducted to image the contact interface. The STEM image shows that the first layer of MoS_2 is heavily damaged, as indicated by the red arrow in **Figure 8.2a**. The electron energy loss spectroscopy was measured using a focused electron beam probe so that the spectra from each MoS_2 layer at the interface could be obtained. It can be seen from **Figure 8.2b** that the sulfur $L_{2,3}$ edges (indicated by the blue vertical lines) of the first and second layers of MoS_2 (first layer being the one in contact with the metal) exhibit very low signal compared to other layers. Energy dispersive spectroscopy (EDS) elemental mapping of Pd, Mo, S, and O are shown in **Figure 8.2c**. The O distribution clearly shows that the MoS_2 top surface is oxidized. In conclusion, even weak O_2 plasma causes the oxidation of MoS_2 that leads to deteriorated device performance.

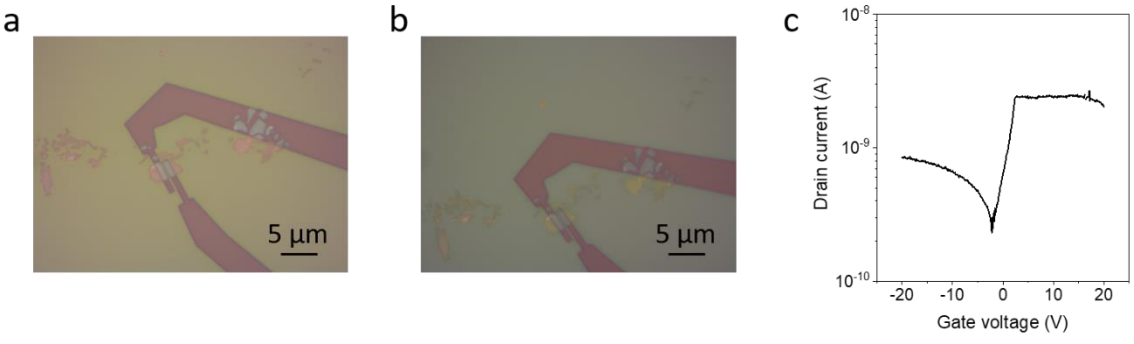


Figure 8.1 a, Optical microscope image of MoS_2 device before and after (**b**) oxygen plasma treatment. **c,** Transfer curve of MoS_2 FET with oxygen plasma treatment prior to metal deposition. W/L = 4µm/0.8µm. Source drain voltage is 1V for transfer curve.

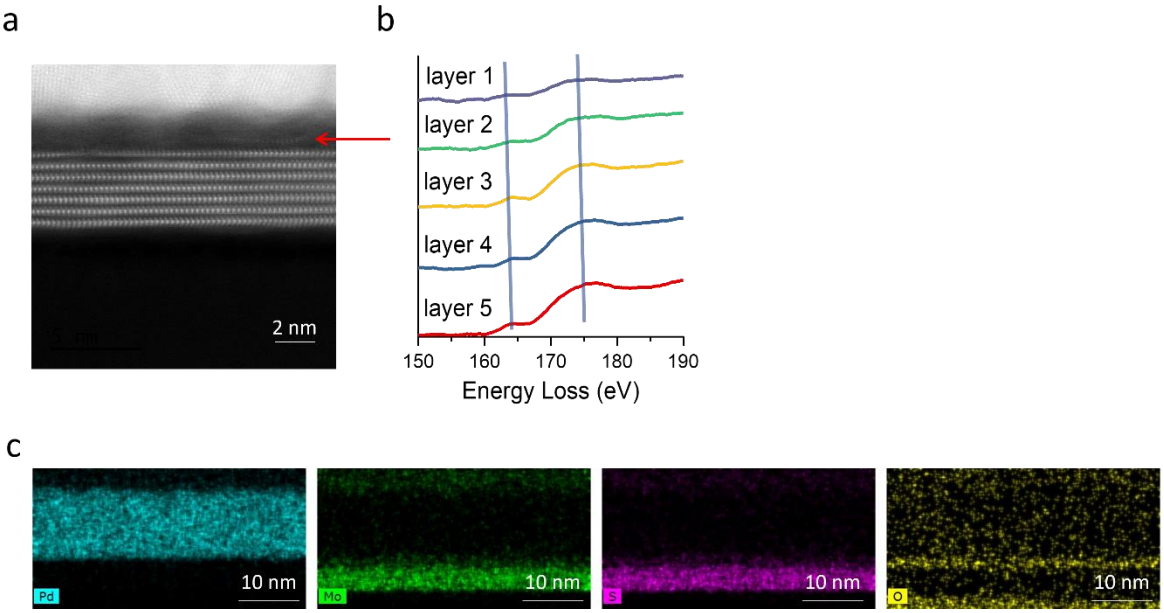


Figure 8.2 a, Cross-section STEM image of the Pd/MoS_2 interface with oxygen plasma treatment prior to metal deposition. It clearly shows the topmost MoS_2 layer is totally damaged, as indicated by the red arrow. **b,** EELS spectra of different layers of MoS_2 at the interface. The sulfur $L_{2,3}$ edges of the first layer and second layer MoS_2 exhibit very low signal compared to other layers. **c,** EDS elemental mapping of Pd, Mo, S, and O showing the topmost MoS_2 is oxidized.

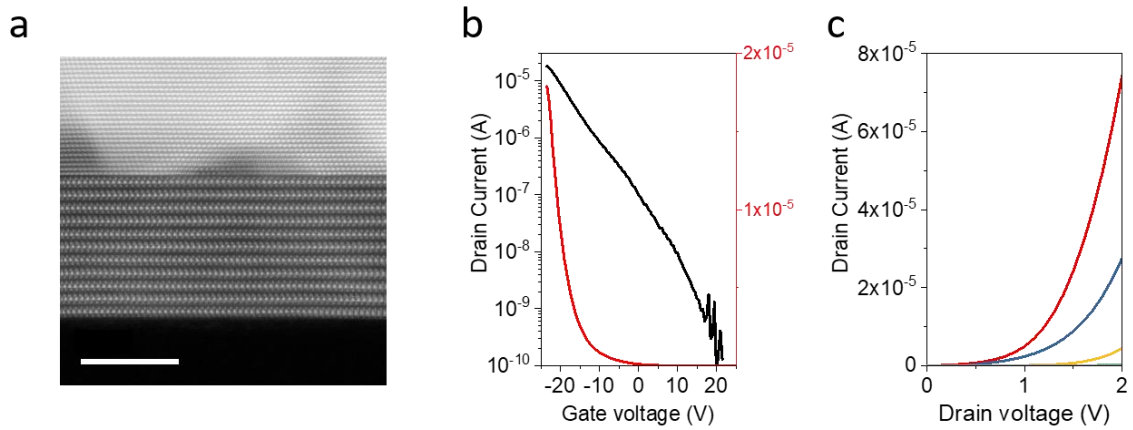


Figure 8.3 a, Cross-section STEM image of the Au/WSe_2 interface shows pristine interface. **b,** Transfer curves of WSe_2 FETs with Au contacts. **c,** Output characteristics of WSe_2 FET with Au contacts showing non-linear IV curve. W/L =8µm/2µm. Source drain voltage is 1V for transfer curve.

8.2 Au contacts for P-type FETs

I have also demonstrated WSe_2 FETs with Au contacts and found that although Au forms clean contacts with WSe_2, P-type behavior is limited (large Schottky barrier leading to non-linear output characteristics) by its relative low work function compared to Pt. The cross-section STEM of the Au/WSe_2 interface given in **Figure 8.3a** shows pristine interface without any intermixing. The transfer curve and output characteristics shown in **Figure 8.3b** and **c** indicate that WSe_2 FETs with Au contacts exhibit P-type behaviour with non-ohmic contacts.

8.3 PL of 2D TMDs on different substrates

The carrier concentrations in MoS_2 can be compared by the trion to exciton ratios in PL spectra. Here I show the PL of monolayer MoS_2 on substrates such as diamond like carbon (DLC), PMMA, SiO_2 and h-BN. The optical images of mechanically exfoliated MoS_2 on different substrates are shown in **Figure 8.4a** and the PL spectra are shown in **Figure 8.4b**. The PL were measured with Renishaw system (514 nm laser, 100 µW laser power) and normalized at the highest intensity to compare the full width half maximum (FWHM). The 2D MoS_2 on DLC showed the lowest FWHM without any sign of a trion peak. PL of monolayer MoS_2 on other substrates showed some trion shoulder at ~ 1.82 eV, indicating doping from the substrates.

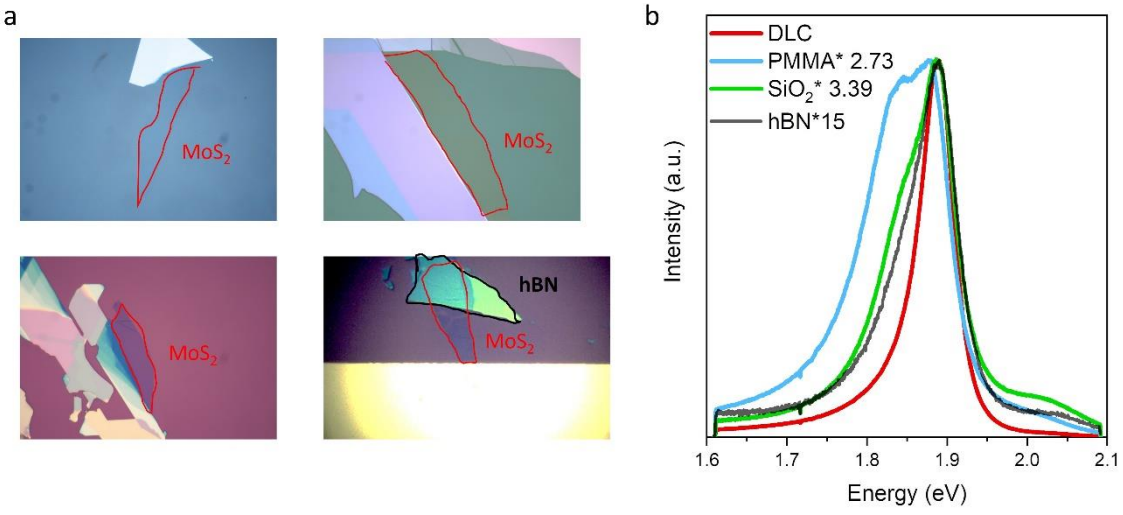


Figure 8.4 a, Optical microscope images of monolayer MoS_2 on different substrate such as diamond like carbon, PMMA, SiO_2 and h-BN. **b,** PL spectra of monolayer MoS_2 on different substrates. Monolayer MoS_2 on DLC shows sharp PL peak at 1.88 eV without any trion signal. Monolayer MoS_2 on other substrates show clear shoulder at ~1.82 eV corresponding to the trion peak position.

8.4 CVD MoS_2 on STO

Here I show some interesting results on CVD grown MoS_2 on strontium titanate ($SrTiO_3$, STO) substrates. The same growth conditions described in section 4.1.1 were applied to grow MoS_2 on STO. Unlike the typical growth of MoS_2 triangles on SiO_2, the growth on STO showed multilayer MoS_2 ribbons with monolayers around them (**Figure 8.5a** and **b**). Aljarb *et al.* reported a ledge-directed epitaxy (LDE) growth of monolayer MoS_2 nanoribbons on β-gallium oxide (β-Ga_2O_3) (100) substrates[277]. Ma *et al.* also observed rectangle shape of MoS_2 with highly aligned orientation on *a*-plane sapphire[278]. The ribbon growth of MoS_2 on STO maybe due to heteroepitaxial growth on the ledges of STO. I further characterised the MoS_2 on STO with Raman and PL measurements. The Raman spectra in **Figure 8.5c** show typical A_{1g} and E_{2g} peaks for MoS_2. PL peak of monolayer MoS_2 on STO is located ~1.86 eV as shown **Figure 8.5d**.

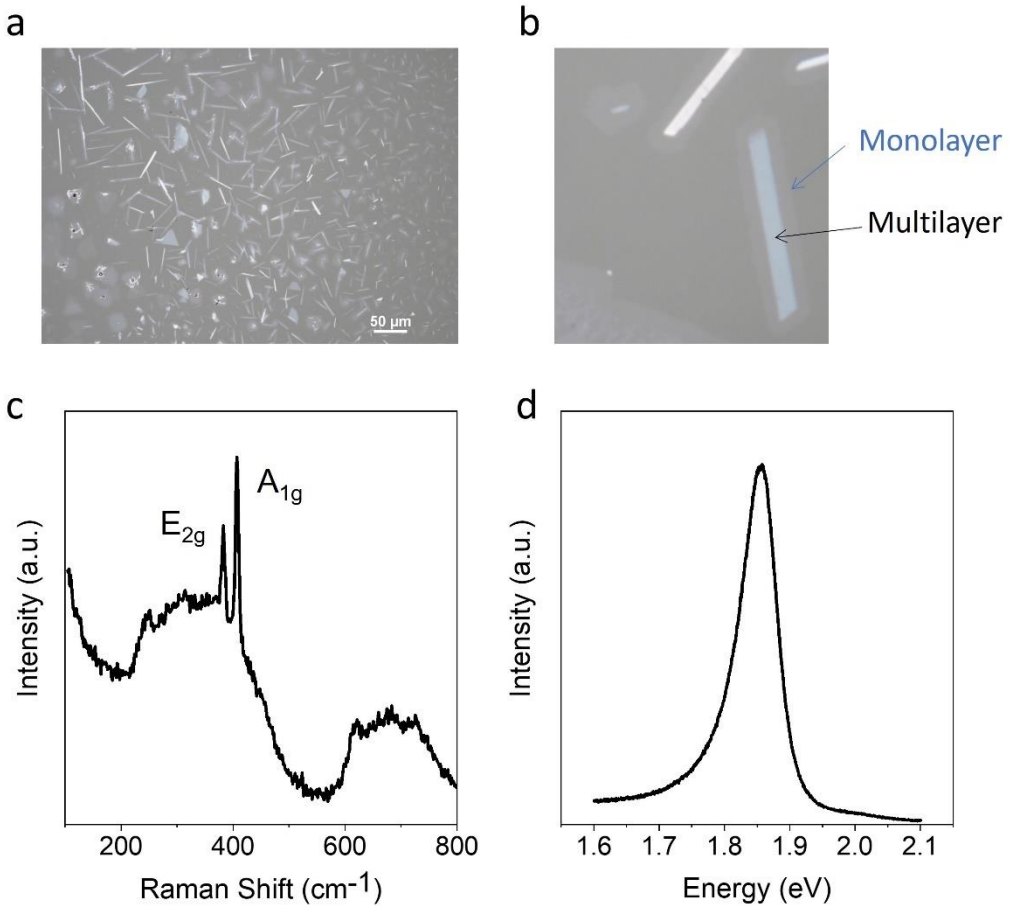


Figure 8.5 a, b, Optical microscope images of CVD grown MoS_2 on STO. **c,** Raman spectrum of MoS_2 on STO showing typical A_{1g} and E_{2g} peaks. **d,** PL of monolayer MoS_2 grown on STO with a peak at ~1.86 eV.

The XPS measurement results of CVD grown MoS_2 on STO are shown in **Figure 8.6**. The Mo 3*d* spectra showed Mo metal, MoS_2 and MoO_3 doublets as shown in Figure 8.6a. The MoO_3 is from the CVD source deposited on substrate. To this date, it is still not clear why the sample shows some signal of Mo metal. The S 2*p* doublet shows pristine MoS_2 peaks.

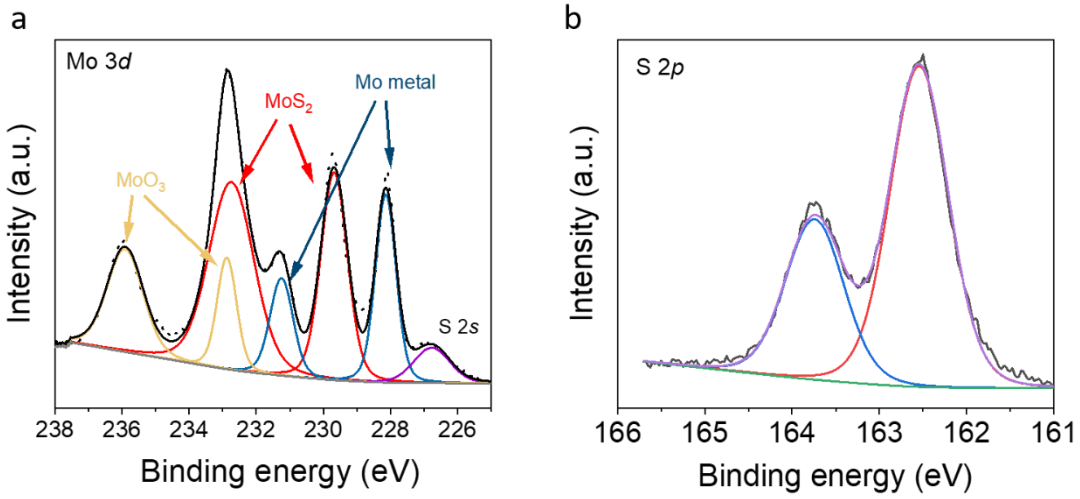


Figure 8.6 XPS of CVD MoS_2 grown on STO **a,** Mo 3*d* spectrum of CVD MoS_2 grown on STO showing Mo metal, MoS_2 and MoO_3 peaks. **b,** S 2*p* spectrum of CVD MoS_2 grown on STO.

Cross-section STEM was conducted to analyze the MoS_2/STO interface. The low and high magnification STEM images of the interface are shown in **Figure 8.7a** and **b**. Although the interface is difficult to image with atomic resolution, the top few layers of MoS_2 are clearly observed while the bottom five layers cannot be resolved. This indicates that the top few layers of MoS_2 are twisted at different angles relative to the bottom five layers. EDS elemental mapping of Mo, S, O, Sr and Ti in **Figure 8.7c** shows that MoS_2 is not oxidized. In addition to the side view, I transferred MoS_2 onto TEM grid by the wet transfer method to observe the plane view. The top view of a MoS_2 ribbon is shown in **Figure 8.8a** with multilayer and monolayer regions indicated by arrows. The high magnification STEM images of multilayer edges are shown in **Figure 8.8b** and **c**. Moire patterns were observed in the STEM image with periodical distance of ~ 5Å. EDS elemental mapping of the MoS_2 ribbon shown in **Figure 8.8d** indicates the ribbon is pristine MoS_2.

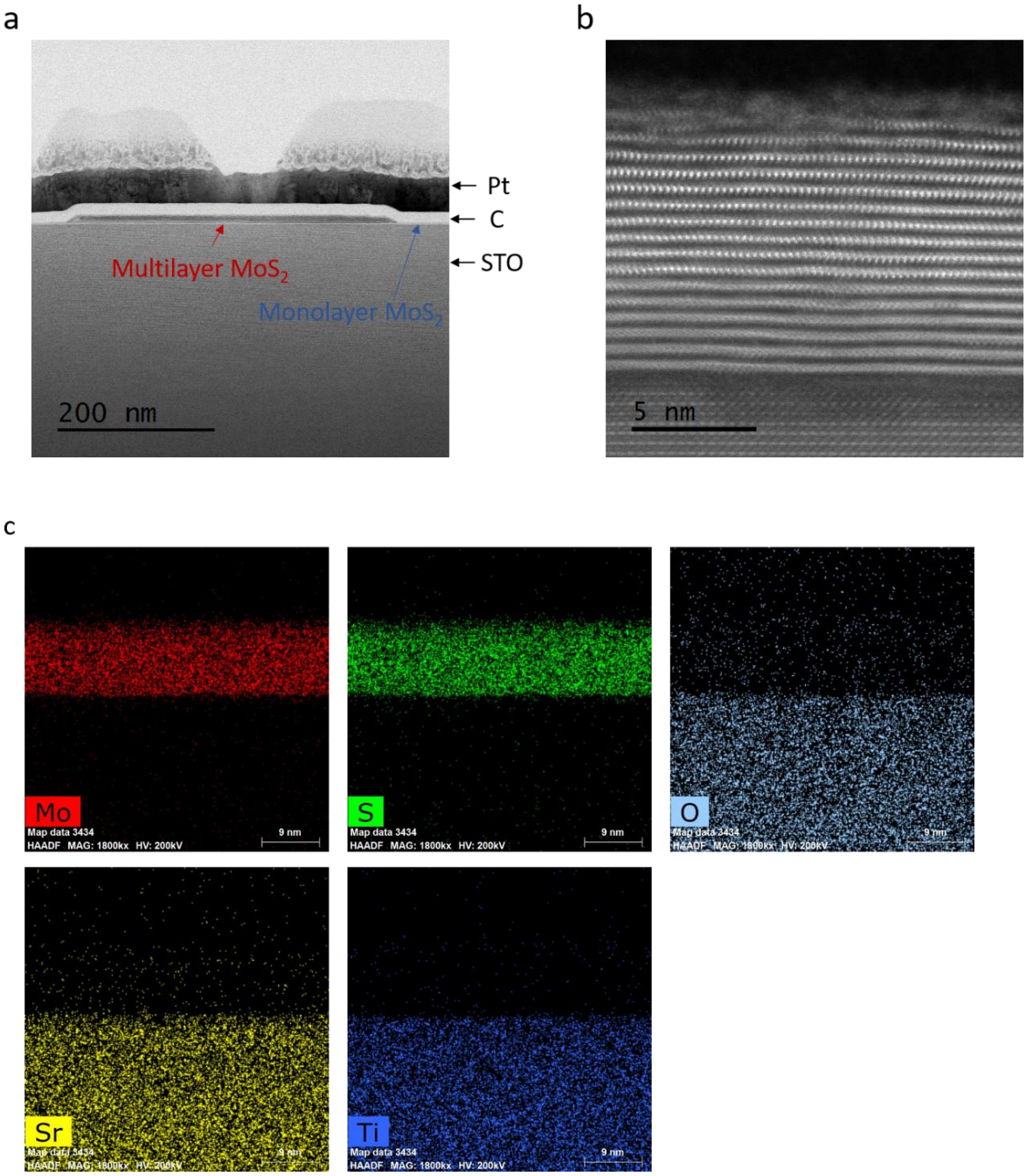


Figure 8.7 a, b, Cross-section STEM image of the MoS_2/STO interface. It shows the image zone of top few MoS_2 layers are different from the bottom five layers, which indicates top few MoS_2 layers are twisted at different angles from bottom five layers. **c,** EDS elemental mapping of Mo, S, O, Sr and Ti.

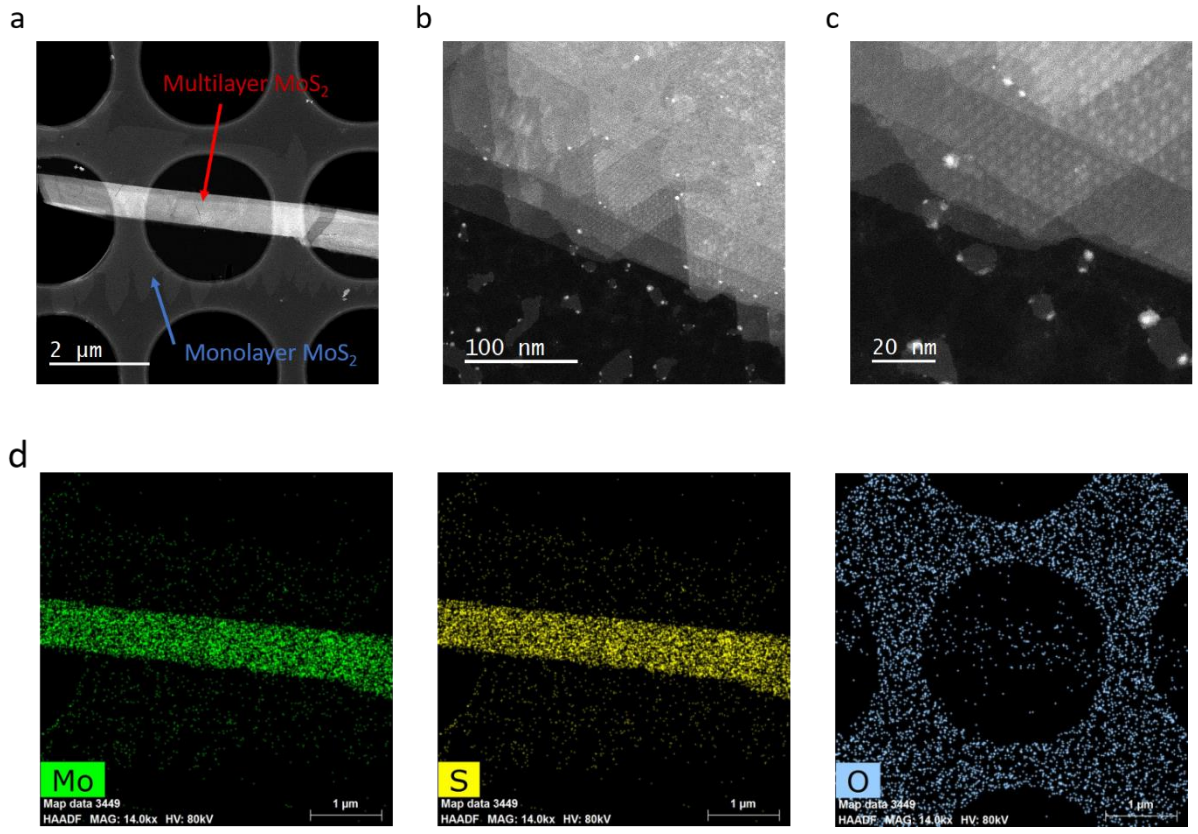


Figure 8.8 a-c, Top view STEM images of MoS_2 ribbon showing Moire patterns with periodical distance of ~ 5Å. **d,** EDS elemental mapping of Mo, S, and O indicate that MoS_2 ribbon is not oxidized.

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