Ultra-thin GaAs Photovoltaics for Space Applications

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To Mom, Dad, Ariel and Kent for their love and support

Declaration

I hereby declare that except where specific reference is made to the work of others, the contents of this dissertation are original and have not been submitted in whole or in part for consideration for any other degree or qualification in this, or any other university. This dissertation is my own work and contains nothing which is the outcome of work done in collaboration with others, except as specified in the text and Acknowledgements. This dissertation contains fewer than 60,000 words excluding appendices, bibliography, footnotes, tables and equations and has fewer than 150 figures.

Larkin Sayre
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Publications

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Journal articles

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Conference proceedings

- L. Sayre, F. Lang, J. Bundesmann, A. Denker, P. Pearce, A. Johnson, and L. Hirst. Ultra-thin Single-junction GaAs Solar Cells For Extreme Space Environments. In 2020 47th IEEE Photovoltaic Specialists Conference (PVSC), pages 1621–1625, June 2020.
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- P. Pearce, L. Sayre, A. Johnson, L. C. Hirst, and N. Ekins-Daukes. Design of photonic light-trapping structures for ultra-thin solar cells. In Physics, Simulation, and Photonic Engineering of Photovoltaic Devices IX, volume 11275, page 112750T. International Society for Optics and Photonics, March 2020.

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Abstract

Ultra-thin photovoltaics (<100 nm) have shown an intrinsic tolerance to radiation-induced damage which makes them a potentially advantageous power source for spacecraft which need to withstand harsh environments outside Earth's atmosphere. In the ultra-thin regime, high transmission losses can be mitigated by integrating light management structures with nanoscale features. A new type of ultra-thin single-junction GaAs solar cell was designed using drift-diffusion simulations with an 80 nm absorber layer thickness and optimised passivation layers. In particular, the use of InGaP as the front surface passivation layer, instead of the more widely used AlGaAs, produced optimal front surface passivation and performance despite being a direct band-gap semiconductor. The annealed n-type contact was optimised using a transmission line measurement study to minimise series resistance at the metal-semiconductor interface while avoiding excess diffusion of Au into the active layers of the device which degrades shunt resistance.

Periodic metal-dielectric nanostructures were simulated and optimised for light management in 80 nm devices using rigorous coupled-wave analysis. Displacement Talbot lithography (DTL) was used for the first time in a photovoltaic application to produce these nanostructures. DTL is a non-contact, wafer-scale interference lithography technique that produces periodic features with excellent uniformity over significant topography in a single exposure. A hexagonal array of Ag pillars in a SiN layer was patterned on the back surface of the ultra-thin devices to increase the optical path length of photons through the active layers. A wafer lift-off process using an epoxy bond and substrate etch back technique was developed to remove the devices from their growth wafers. This lifted-off design produced an AM0 short circuit current of 15.35 mA/cm^2 and an AM0 efficiency of 9.08%, a 68% increase over the planar on-wafer equivalent. Optical simulations confirmed the contributions of Fabry-Perot and waveguide modes to this current increase. Simulated fabrication and design improvements showed a feasible pathway to 16% AM0 efficiency.

Planar on and off-wafer 80 nm ultra-thin devices were then exposed to 68 MeV and 3 MeV proton radiation to test their resilience in the space environment. Irradiation results for on-wafer devices have shown boosted absorption of light compared to previous 80 nm on-wafer ultra-thin designs in the literature. Maximum power values for off-wafer devices with

integrated back surface planar mirror also exceeded cells that are two orders of magnitude thicker from 3×10^{11} p^{+}/cm^{2}, the lowest 3 MeV proton fluence that was tested. Devices with 3500 nm thickness produced just 53% of pre-exposure short circuit current at an equivalent fluence of 7.21×10^{12} p^{+}/cm^{2}. However, there was no degradation in short-circuit current for 80 nm devices up to 2×10^{14} p^{+}/cm^{2}. Time-resolved cathodoluminescence analysis was carried out on radiation damaged devices and was used to correlate the onset of short circuit current degradation with the point when extrapolated carrier lifetime drops below the calculated time for carriers to traverse the junction. This is the first evidence in the literature that suggests the intrinsic radiation tolerance of ultra-thin cells is due to carrier lifetimes remaining long in relation to junction traverse time even after radiation-induced defects are introduced.

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Nomenclature

Symbols

α	Absorption coefficient
λ	Wavelength
Ω	Ohm
k	Boltzmann's constant
q	Elemental charge

Solar cell parameters

η	Efficiency
FF	Fill Factor
J_{01}	Reverse saturation current (first diode)
J_{02}	Reverse saturation current (second diode)
J_{SC}	Short circuit current density
n_1	First diode ideality factor
n_2	Second diode ideality factor
R_{par}	Shunt resistance
R_{ser}	Series resistance
V_{OC}	Open circuit voltage

Acronyms / Abbreviations

AFM	Atomic Force Microscopy
AM0	Air Mass 0
AM1.5	Air Mass 1.5
ARC	Anti-Reflection Coating
BARC	Bottom Anti-Reflection Coating
BOL	Beginning Of Life
CL	Cathodoluminescence
DDD	Displacement Damage Dose
DIV	Dark IV
DLTS	Deep-Level Transient Spectroscopy
DTL	Displacement Talbot Lithogrpahy
ELO	Epitaxial Lift-Off
EOL	End Of Life
EQE	External Quantum Efficiency
FE	Field Emission
GEO	Geosynchronous Equatorial Orbit
HALE	High Altitude Long Endurance
HCSC	Hot Carrier Solar Cell
HEO	Highly Elliptical Orbit
ICP	Inductively Coupled Plasma
LEO	Low Earth Orbit
LIV	Light IV
MBE	Molecular Beam Epitaxy

MEO	Middle Earth Orbit
NIEL	Non-Ionising Energy Loss
PV	Photovoltaics
RCWA	Rigorous Coupled-Wave Analysis
RF	Remaining Factor
ROSA	Roll-Out Solar Array
RTG	Radioisotope Thermoelectric Generator
SEM	Scanning Electron Microscopy
SLARC	Single-Layer Anti-Reflection Coating
SPENVIS	SPace ENVironment Information System
SRH	Shockley-Read-Hall
TE	Thermionic Emission
TFE	Thermionic Field Emission
TLM	Transmission Line Measurement
TMM	Transfer Matrix Method

Chapter 1

Introduction to ultra-thin solar cells for space power applications

The Sun continuously releases a huge amount of energy from the fusion reaction of hydrogen nuclei into helium. Approximately 3.4 million EJ of energy from the sun makes it to the Earth's surface every year [12]. The sun's energy can be captured by photovoltaic (PV) cells and converted into usable electricity. PV technologies are important for a range of applications including residential rooftop power generation, providing grid scale electricity and, as will be the focus of this thesis, powering the electronics of satellites and spacecraft. Satellite-enabled technologies span a huge range of industries from communication to climate monitoring and are predicted to continue growing in importance in the coming years [13].

1.1 The solar spectrum

The sun's radiation is primarily in the visible and near infra-red portions of the electromagnetic spectrum. Its spectrum is estimated well by modelling the sun as a blackbody emitter at a temperature of 5800 K. The standard spectrum used to test terrestrial PV is the standardised Air Mass 1.5 (AM1.5) spectrum. Figure 1.1 shows the AM1.5G and 5800K blackbody emission spectra for comparison along with the AM0 spectrum which is used for testing space PV. AM notation is used to signify the spectra that results after attenuation by the Earth's atmosphere (AM1.5G) or without any attenuation (AM0). G stands for global which means the diffuse component is included. The integrated power density of AM1.5G solar spectrum is 1000 W/m^2 while for AM0 it is 1353 W/m^2. While the solar constant of AM0 is higher than that of the AM1.5 spectrum, the efficiency of solar cells tested under AM0 is lower than that under AM1.5 because the Earth's atmosphere attenuates large portions of the lower wavelength, near ultra-violet region and the below bandgap near IR region where typical solar cells do not perform well.

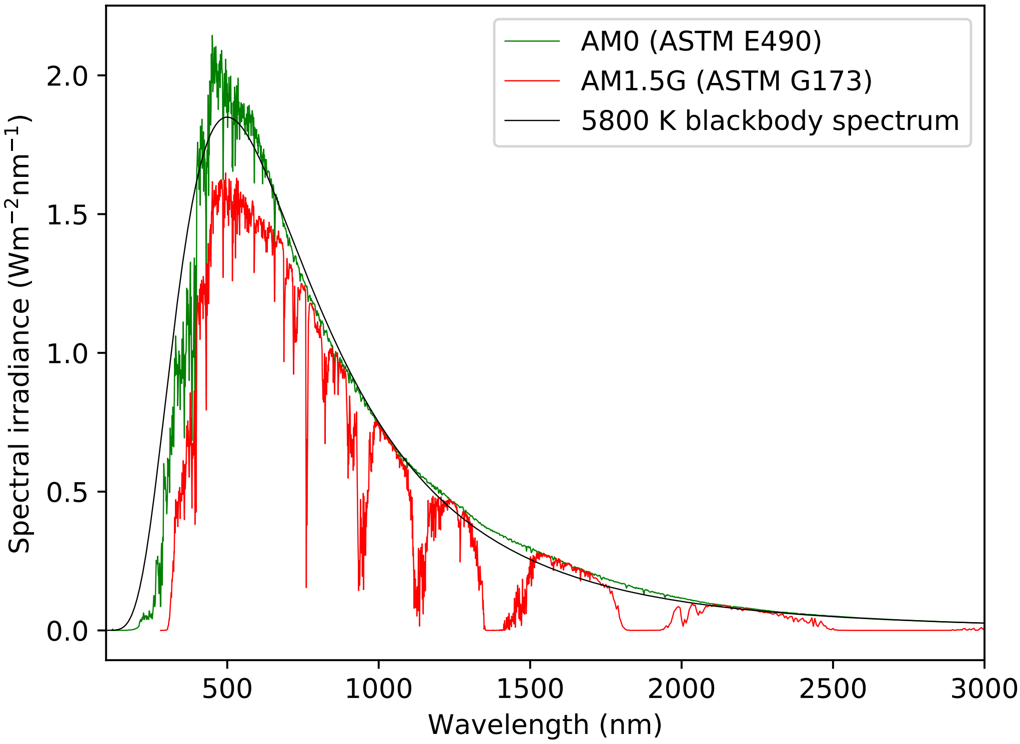


Fig. 1.1 AM0, AM1.5G and 5800 K blackbody radiation spectra, data from ASTM standards [1].

1.2 Photovoltaics

Typically, PV cells are semiconductor devices that make use of the photovoltaic effect to convert the energy of light incident on their surface to usable electricity. Upon absorption of a photon with an energy greater than or equal to the semiconductor material's bandgap, an electron-hole pair is generated which can be extracted as useful current. The efficiency with which a solar cell converts incident energy from photons into usable electricity is limited by various loss processes. The theoretical limit of efficiency for a solar cell material is dictated by its material bandgap and is known as the Shockley-Queisser limit [14]. The theory behind solar cell operation, in relation to this work, is described in detail in Chapter 2.

1.2.1 Solar cell materials

Solar cells made from crystalline silicon are the current industry standard for terrestrial PV. This is due to the low cost and mature manufacturing infrastructure of silicon wafers which was spurred by the rise of the electronics industry. Silicon is not the ideal solar cell material but it is more economical to produce for large-scale solar deployment than other semiconductor materials that are more efficient per unit area. One such material that is more efficient than silicon is gallium arsenide, referred to as GaAs from here onwards. GaAs performs better than silicon as a PV absorber layer due to its direct and near-ideal bandgap of 1.42 eV. GaAs is a III-V semiconductor meaning it is made up of elements from group III and group V of the periodic table. Since GaAs is much more expensive to produce than Si, it has found targeted applications in concentrator PV and spacecraft solar power where costs per cell are small in comparison to overall project costs. Furthermore III-V materials offer a radiatively limited material system in which extrinsic losses can be eliminated, making it an appropriate platform for the study and development of next generation solar cells and emerging concepts such as hot carrier solar cells (HCSC) [15, 16] that could overcome the Shockley-Queisser limit.

1.3 Space power systems

The invention and initial development of PV, well before grid-scale solar energy generation was considered, was spurred on by their applications in the space industry [17]. PV technologies have many advantages when it comes to space power generation. Other power systems that have been considered for spacecraft include batteries and radioisotope thermoelectric generators (RTG). However, batteries can be heavy and have finite lifetimes and there is an insufficient amount of radioisotope fuel to supply the fleets of satellites in use today. Moreover, proliferation of nuclear materials remains a concern. This leaves solar arrays as the best technology for most spacecraft except for deep-space missions where solar irradiance is significantly reduced due to the large distances from the sun. For these deep-space missions, RTGs have been used [18].

The first solar-powered satellite to be launched into space was the Vanguard I in 1958 and it was powered by silicon solar cells [19] with an efficiency of approximately 10% at beginning of life (BOL). It still orbits the Earth to this day although it stopped transmitting in 1964. Space PV technologies have come a long way since this first launch of a solar cell into space. The current industry standard for space power systems are highly-efficient, multi-junction, III-V PV technologies [20, 21]. They are significantly more costly per unit area to produce than silicon but are more efficient. They have been developed for space applications since launch costs per kilogram of mass are high which means the cost of the array is a less significant portion of overall costs. Multi-junction cells hold the current world records for power conversion efficiency [22]. The drawbacks of these multi-junction designs are that they are rigid and require protective coverglass when exposed to the damaging radiation present in space. Progress towards making satellite solar arrays flexible and reducing the need for heavy coverglass would be hugely beneficial for the satellite industry.

1.3.1 Space radiation environment

Outside of the Earth's atmosphere there are regions with high levels of damaging radiation that satellites must pass through when in certain orbits [23]. These areas are called the Van Allen belts and they are visually represented in Fig. 1.2. These belts are made up of energetic charged particles, mainly protons and electrons, that have become trapped due to the Earth's magnetosphere. Models of the radiation profiles of the Van Allen belts have improved over the years from data collected from spacecraft travelling through them including the Van Allen Probes launched in 2012 [24]. The low altitude belt is mainly made up of protons while the high altitude belt is primarily electrons.

When a high energy proton or electron is incident on a crystalline solar cell in space, defects can form in the lattice structure of the absorber layer that degrade the performance of the solar cell. During many years on orbit these stable defects build up in the solar arrays of satellites and they put a limit on satellites' mission lifetimes. Protective coverglass is often used to shield solar arrays from this radiation but the added weight that coverglass adds is a major cost to the overall mission.

1.3.2 Trends and challenges

Satellite technologies have grown in importance and now touch many aspects of modern life from communication and weather forecasting to security and defense [25]. Large-scale satellite constellations such as those launched by SpaceX and OneWeb show the importance of optimised space power systems that can last for many years as more and more satellites are launched into Earth orbit [13] and issues of space debris become significant.

A review of the future of space PV by the US Air Force Research Laboratory [26] identified four major challenges that need to be addressed: power system cost reduction, volumetric specific power, solar array reliability and solar array development schedule. Further attributes identified by the space PV industry as crucial for future development include: tolerance to damaging radiation and flexible form factors.

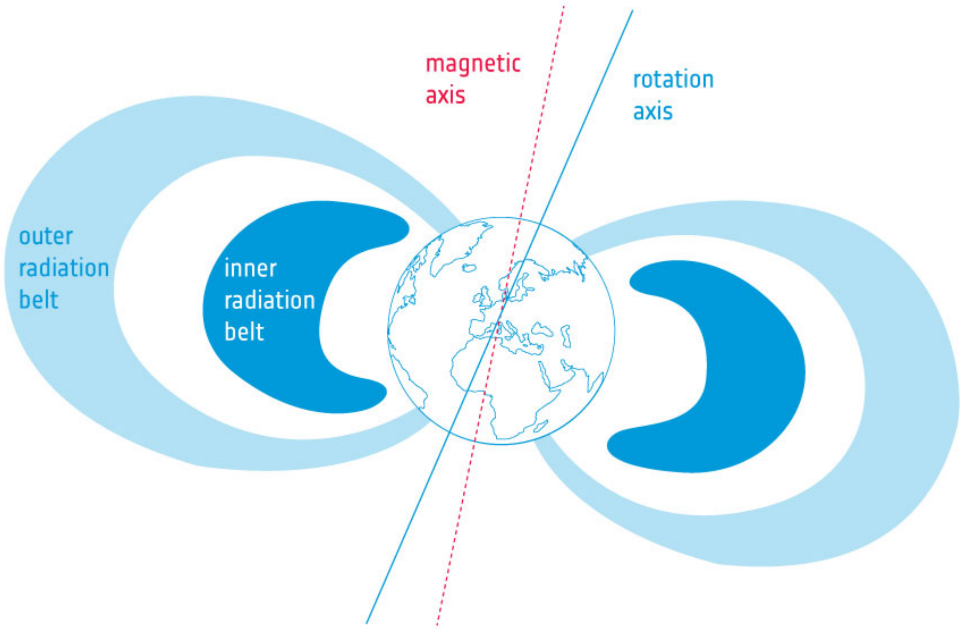


Fig. 1.2 Diagram of the Earth's Van Allen belts alongside the magnetic and rotational axes of the planet, image from the European Space Agency [2].

Flexible form factors have been partially achieved with rigid cells by using individual hinged sections such as the Roll-Out Solar Array (ROSA) designed by Redwire [27]. However this is still a work-around that involves a complicated mechanism with many components and many potential failure modes during deployment. A PV technology that could be flexible at the cell scale has been identified as a key goal of the space PV industry as it could significantly reduce the stowed volume of the solar array during launch.

1.3.3 Opportunities

Since every kilogram of mass launched into space is expensive, there is an opportunity for a new space PV technology, with a higher specific power, to disrupt the industry. Solar arrays on a spacecraft need to maximise the watts produced per kilogram. The PV power systems of satellites are also a large part of the overall mass which makes their specific power even more important [28]. Specific power can be looked at in terms of mass (W/kg) or stowed volume (W/m^3). Both are important metrics to consider for space applications. This differs from the requirements of terrestrial PV for residential roofs or grid-scale power generation where module cost and power conversion efficiency per unit area are often more important than W/kg of the PV system.

A further opportunity within the space PV industry is designing solar arrays that can facilitate the use of hostile orbits. Currently, there are gaps in the capabilities of satellites when it comes to imaging the Earth's surface. For instance, the polar regions of the Earth do not get regular satellite coverage despite being of huge interest for imaging as our planet warms [29, 30]. Molniya orbits are an example of missions that are strategically advantageous for coverage of high latitudes but satellites are exposed to more damaging radiation because they have to pass repeatedly through the Earth's Van Allen radiation belts [31].

Other missions of interest that are currently beyond the capabilities of today's space PV include Jupiter's moon Europa. It is seen as one of the best candidates for finding evidence of extra-terrestrial life in our solar system. Thus far, Europa has only been imaged with brief flybys from Jovian orbiting spacecraft in order to minimise radiation damage to on-board solar arrays [32]. Missions to the surface of Europa to investigate have been stymied by its harsh radiation environments.

Extending the end of life (EOL) performance of space solar cells could also extend the mission lifetimes of Earth orbiting spacecraft in crowded orbits and reduce the need for launching replacement satellites that contribute to space debris. There is significant opportunity for new types of radiation tolerant, high specific power and flexible solar cells in the space PV industry.

1.4 Ultra-thin GaAs solar cells for space applications

Ultra-thin GaAs solar cells are proposed for use as space PV due to their potential for high specific power, intrinsic radiation tolerance [6, 33] and flexible form factors. In order to exploit these characteristics, the high transmission losses inherent in the ultra-thin regime need to be mitigated, particularly in the longer wavelength region of the incident spectrum. In order for ultra-thin cells to compete with the thicker multi-junction cells used in space applications, "light management" layers can be used to increase the path length of light through the absorber layer. This increases the likelihood that an incident photon will be absorbed and produce an electron hole pair. The term "light management" is used in this thesis to refer to any structure or reflector that is integrated into the design of a solar cell to increase optical path length through the device active layers or reduce reflection at the front surface.

1.4.1 Intrinsic radiation tolerance

An explanation for why ultra-thin solar cells exhibit intrinsic radiation tolerance has been proposed in previous work [6] and is investigated further in this thesis. This proposed explanation is that when the absorber layer of a single-junction solar cell is thinned down to the ultra-thin regime (100 nm or less), the distance from the junction to the contacts is also significantly reduced which means carriers are still likely to be collected at the contacts even when radiation-induced defects are introduced. For standard space PV cells which have length scales of tens to hundreds of microns, there is a substantial distance for the carriers to travel before being collected at the contacts which means that at high defect densities, carriers are likely to encounter a defect along the way and recombine. For the ultra-thin regime on the other hand, the distance to the contacts is much shorter. As a result, carriers are less likely to encounter defects, and are more likely to be available as current. In summary, in the ultra-thin regime the short-circuit current does not degrade until extremely high defect densities are reached.

1.4.2 Progress and state-of-the-art

Maximising the performance of thinned GaAs solar cells centres on increasing absorption of photons from 600 nm up to the bandgap of GaAs which is 870 nm. This is because shorter wavelengths are fully absorbed in thinned GaAs absorber layers, due to the high absorption coefficient in the short wavelength range. Thick single-junction GaAs devices that have long optical path lengths have achieved excellent efficiencies. Alta Devices presented 27.6% efficient cells [34] in 2011. They currently hold the efficiency world record for single junction GaAs cells.

Ultra-thin GaAs cells have seen exciting advancements in recent years [35]. Certified 19.9% efficiency has been achieved [36] with a GaAs absorber layer of 205 nm (330 nm including passivation layers). Table 1.1 compares recent progress in the performance of GaAs solar cells near the ultra-thin regime. This thesis will present ultra-thin GaAs cells with 80 nm absorber layers and explore their potential use in a space radiation environment. The final row of Table 1.1 denotes the light management structure used to improve the performance of the ultra-thin devices.

Planar mirrors on the back surface of a solar cell can increase optical path length up to a factor of 2. Randomised texturing such as surface roughening on the front or rear of a solar cell can increase optical path length at most by a factor of $4n^2$ where n is the refractive index of the film. This is often referred to as the Lambertian or Yablonovitch limit [37, 38]. Periodic nanostructures such as photonic crystals can couple incident light to discrete guided modes, which can be tuned to maximise total internal reflection in the film. Optimised quasi-random structures can scatter light into a tuned range between the evanescent limit and the escape cone with a broad engineering tolerance [39]. Photonic crystal and quasi-random structures can surpass the Lambertian limit.

Table 1.1 Comparison of ultra-thin single-junction GaAs solar cell performance in the literature under AM1.5 illumination. Light management row refers to the type of structure used to extend the optical path length through the device: PM - Planar Mirror, PC - Photonic Crystal, QR - Quasi-Random, R - Roughening. * - measured under monochromatic 1-sun like illumination

Author	Vandamme*	Lee	Chen	Chen	Vandamme*	Buencuerpo	Yang	van Eerden
Year	2015	2015	2016	2019	2015	2022	2014	2020
	[40]	[41]	[42]	[36]	[40]	[43]	[44]	[45]
Absorber thickness (nm)	120	200	200	205	220	260	300	300
Absorber thickness incl. passivation (nm)	320	340	260	330	320	420	360	425
J_{SC} **(mA/cm^2)**	14.81	22.0	16.8	22.0	19.42	26.4	24.5	24.8
V_{OC} **(V)**	0.818	0.942	0.94	1.00	0.865	1.119	1.00	1.027
FF **(%)**	72	78	81	79.2	77	75.7	77.8	83.9
η **(%)**	8.7	16.2	12.8	19.9	12.9	22.35	19.1	21.4
Light management	PM	PC	PC	PC	PM	QR	R	R

1.5 Structure of the thesis

Chapter 2 will detail the theory underpinning this investigation. The methods used to simulate device performance and design light management structures will be presented. The theory of radiation tolerance testing for PV will also be explained, as well as the modelling of the space radiation environment, so ground testing of space solar cells can be extrapolated to actual spacecraft mission conditions.

Chapter 3 will present the design and optimisation of a novel ultra-thin solar cell layer structure. This layer structure is then used in the solar cell devices presented in Chapters 4, 5 and 6. Simulations of band structure, layer thicknesses and electrical performance will be detailed. The optimisation of contact metalisation, contact layers and anneals will be presented.

Chapter 4 will present an ultra-thin solar cell with integrated nanophotonic light-trapping structures patterned with Displacement Talbot Lithography. Optimisation of fabrication methods, the results of detailed characterisation and correlation with simulations will be detailed.

Chapter 5 will present the radiation tolerance testing carried out on planar on and off-wafer ultra-thin devices and will give detailed analysis of performance parameter degradation. The chapter will also consider the application of these devices for scientifically interesting but hostile orbits such as Highly Elliptical Earth Orbits (HEO) and orbits around Jupiter.

In Chapter 6, further optimisation of the ultra-thin device design is discussed, including a detailed loss analysis and path to improvement. Avenues for potentially improving beginning and end of life performance for ultra-thin solar cells used in space applications will be presented.

Chapter 7 will discuss the outcomes and future perspectives that can be taken from this work.

Chapter 2

Theory of ultra-thin solar cell design and characterisation

2.1 Introduction

Fundamental theory and techniques used for simulation, design and the analysis of data are explained in this chapter. First, the physics of solar cells is presented with specific attention to the special case of the ultra-thin regime. This is followed by an explanation of the device fabrication and metal contact quality testing techniques used in subsequent chapters. Methods for boosting light absorption in the ultra-thin regime are then explored. Finally, the theory behind radiation tolerance testing of solar cells and how those results are extrapolated to on-orbit conditions is detailed. The underpinning goal throughout is to optimise, fabricate and test novel ultra-thin solar cells in order to enable new spacecraft missions in hostile orbits.

2.2 Solar cell physics

Solar cells need to have two specific characteristics in order to produce electricity when photons are incident on their surface. These are the ability to absorb electromagnetic radiation that produces electron-hole pairs and an asymmetry in electrical resistance that ensures charge carriers flow in one direction through the device. By converting photogenerated chemical potential into voltage across the device terminals, this current can then perform electrical work on a load connected in series with the solar cell.

2.2.1 Semiconductors

The band gap of a semiconductor material is the difference in energy level between the valence band (where electrons are bound to their atom and are not free to flow through a circuit) and the conduction band (where electrons have been excited and can conduct electricity). The presence of a bandgap is one of the criteria for classifying a material as a semiconductor. Insulators also have bandgaps but they are much greater than those of semiconductors. When a photon that has an energy equal to or above the bandgap of the semiconductor material is absorbed, an electron-hole pair is created. These photogenerated charge carriers can either flow through the circuit or recombine radiatively or non-radiatively. The energy that the photon provides that is in excess of the material's bandgap is lost as heat through interaction with lattice phonons in a process called thermalisation.

2.2.2 Absorption of photons

The probability that a photon incident on the surface of a solar cell will be absorbed depends on the optical properties of the absorber material. For a first approximation of absorption, the Beer-Lambert law can be used once the extinction coefficient, k, values for the material have been measured. The absorption coefficient at a specific wavelength is calculated by using Equation 2.1

$$\alpha = \frac{4\pi k}{\lambda} \tag{2.1}$$

where α is the absorption coefficient and λ is the wavelength of the incident light. Single pass absorption, assuming no reflection at the front surface, can then be calculated by using Equation 2.2

$$\text{Absorption} = 1 - \exp(-\alpha d) \tag{2.2}$$

where d is the thickness of the absorbing slab. Ellipsometry measurements are used in this thesis to accurately measure the thickness and optical properties of the layers of ultra-thin solar cells. This data is then used in simulations explained in Section 2.4.3 and in producing Figure 2.1 which shows the absorption in GaAs slabs of varying thicknesses over a range of incident wavelengths from 300-1000 nm. This figure shows the high transmission losses inherent in the ultra-thin regime particularly in the longer wavelength regions.

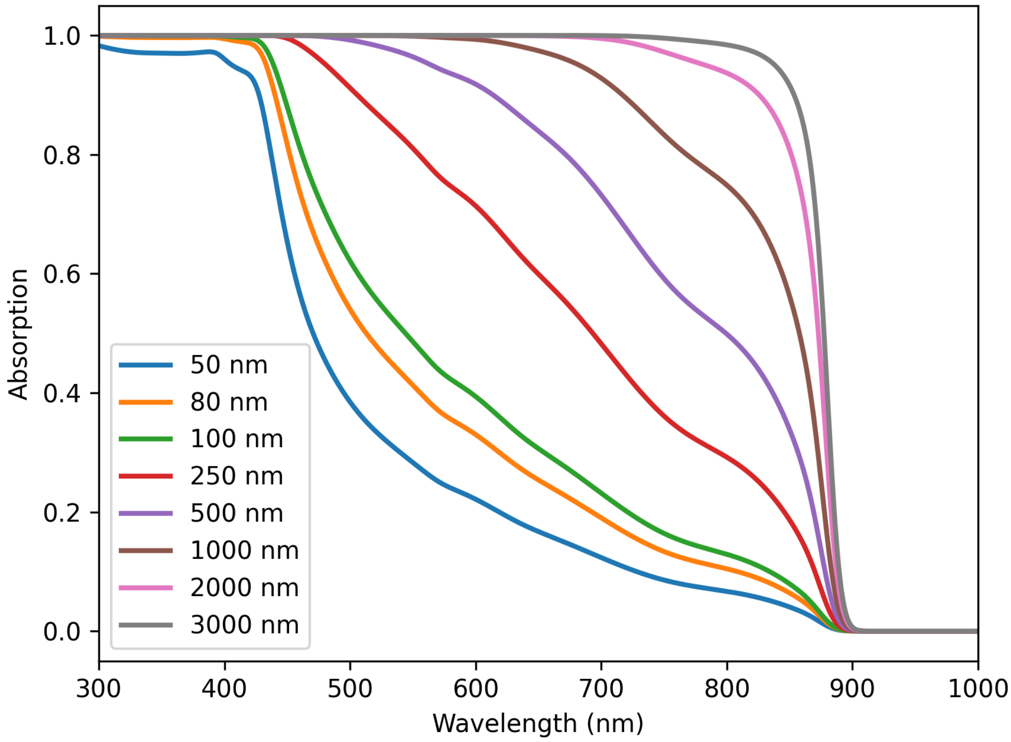


Fig. 2.1 Absorption as a function of wavelength for different thicknesses of GaAs slab.

2.2.3 Thickness and theoretical efficiency limits

As Equation 2.2 shows, devices with thinner absorber layers will absorb fewer photons. This is because the thinner layer leads to a decreased optical path length which is one of the innate disadvantages of thinned solar cell designs. The device is also more susceptible to shunt pathways forming during processing thus potentially degrading the shunt resistance.

However operating in the thinned regime can lead to significant advantages. These include improved carrier collection and higher open circuit voltages [46]. Carrier collection efficiency is likely improved in the ultra-thin regime due to reduced transit distances to terminals and open circuit voltages may be increased since light management targets high photon density in a small volume which increases the density of charge carriers. Higher densities leads to higher chemical potential and therefore an increase in open circuit voltage. As mentioned previously, there is also significant evidence that solar cells with absorber layers on the order of 100 nm in thickness exhibit an increased intrinsic tolerance to damaging radiation when compared to thicker designs.

The Shockley-Queisser limit for single-junction solar cells [14] states that 33% efficiency is the maximum achievable limit for a material with an ideal bandgap of 1.4 eV and a thick absorber layer. In practice, PV systems achieve lower than the Shockley-Queisser limit due to non-ideal bandgaps, defects in the material structure and other processes that reduce power conversion efficiency. There are certain losses that are intrinsic and unavoidable (e.g. thermalisation losses) while other losses are extrinsic and can, in theory, be avoided by optimised device design (e.g. contact shading, non-radiative recombination) [47].

2.2.4 Recombination

There are broadly two different mechanisms by which an electron and hole recombine: radiative and non-radiative. Radiative recombination dominates in direct semiconductor materials such as GaAs while non-radiative recombination is more prevalent in indirect semiconductors such as Si. When radiative recombination occurs, a photon is emitted when an electron-hole pair recombines. Non-radiative recombination, which releases heat instead of a photon, can also be split into two categories, Shockley-Read-Hall (SRH) and Auger recombination. SRH recombination occurs when states in the forbidden energy band gap are introduced due to defects in the material. These states trap electrons and provide a pathway to recombination. Auger recombination is the process by which an electron and hole recombine but rather than emitting the energy as a photon or heat, the energy is transferred to a third electron in the conduction band which then thermalises back down to the conduction band edge.

Photon recycling is a process that can occur when a radiative recombination event takes place and the photon that is emitted is re-absorbed by the semiconductor material before escaping through the front or rear surface. This process enhances the efficiency of the solar cell and the rate of photon recycling can be increased in thin, radiatively limited cells by increasing the optical path length within the solar cell active layers.

2.3 Solar cell modelling and characterisation

2.3.1 Diode behavior

In the dark, an ideal solar cell can be modelled as a rectifying diode connected in parallel to a current source. By using a source meter, a voltage sweep can be carried out to investigate the diode behavior of the cell under test. The resulting current is exponentially related to the applied voltage and is governed by the following diode equation:

$$I = I_0 \left\{ \exp \left[\frac{qV}{kT} \right] - 1 \right\} \tag{2.3}$$

where I is the resulting current, I_0 is the reverse saturation current, q is the fundamental charge, V is the applied voltage, k is the Boltzmann's constant and T is the temperature. The I_0 term is a measure of recombination in the device and is inversely related to the material bandgap. When exposed to illumination, the light generated current term is introduced:

$$I = I_0 \left\{ \exp \left[\frac{qV}{kT} \right] - 1 \right\} - I_L \tag{2.4}$$

where I_L is the light-generated current. When taking a current voltage sweep of a solar cell in the dark, the applied voltage creates the electron-hole pairs. By analysing the diode behavior of a solar cell in the dark and under illumination, insight into the electrical performance can be gained and improved devices can be designed.

Fig. 2.2 illustrates the current-voltage characteristics of a typical solar cell in the dark and under illumination. J_{SC} is the short circuit current density, V_{OC} is the open circuit voltage, FF is the fill factor, V_{mpp} is the voltage at the maximum power point and J_{mpp} is the current density at the maximum power point. For the rest of this thesis J (current density) will be used instead of I (current) because J values allow for direct comparison of solar cells of different areas. J-V sweeps are common testing methods for solar cells and allow us to calculate the efficiency with which the solar cell is converting incident energy into electricity.

By calculating the power produced at the max power point and dividing this value by the power of the incident spectrum (AM1.5, AM0 etc.), the efficiency can be determined. In theory, the curve in the dark should match the curve under illumination with an offset in current density equal to the J_{SC}. This concept is called the superposition principle.

2.3.2 The 2-diode model

Moving beyond the idealised single diode model of a solar cell leads us to the more accurate 2-diode model. Figure 2.3 shows the equivalent circuit used to model the behavior of a standard solar cell. Experimental data can be fitted to this model in order to extract parasitic resistance (R_{ser} and R_{par}), diode ideality factors (n_1 and n_2) and saturation current values (J_{01} and J_{02}). These values are used to pinpoint potential device processing improvements. The second diode current value, J_{02}, is of particular interest to the ultra-thin regime since the depletion region accounts for a large fraction of the total device thickness and the second

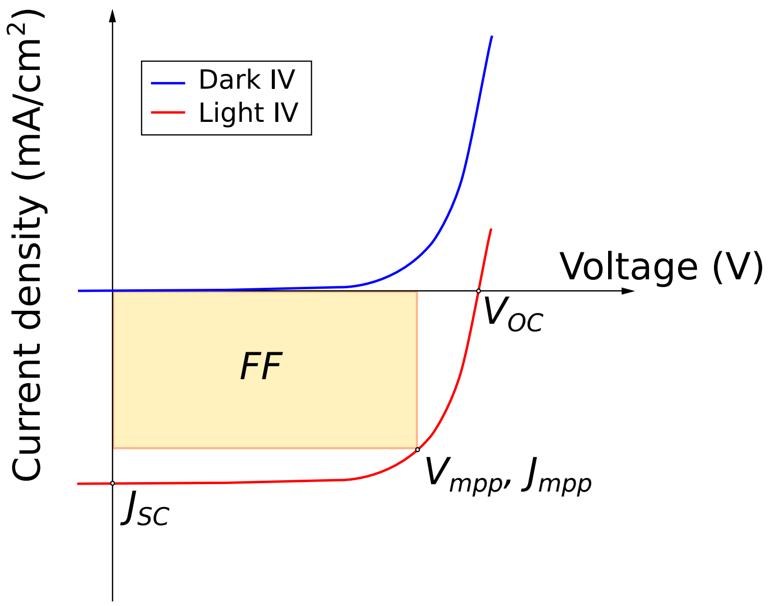


Fig. 2.2 Diagram of dark and light current-voltage characteristics for a typical solar cell with labelled performance parameters: J_{SC}, V_{OC}, FF, V_{mpp} and J_{mpp}.

diode represents losses due to carrier recombination through defect centres in the depletion region. The ideality factors n_1 and n_2 are measures of how well the data follows the diode equation. Equation 2.5 is the 2-diode equation under illumination.

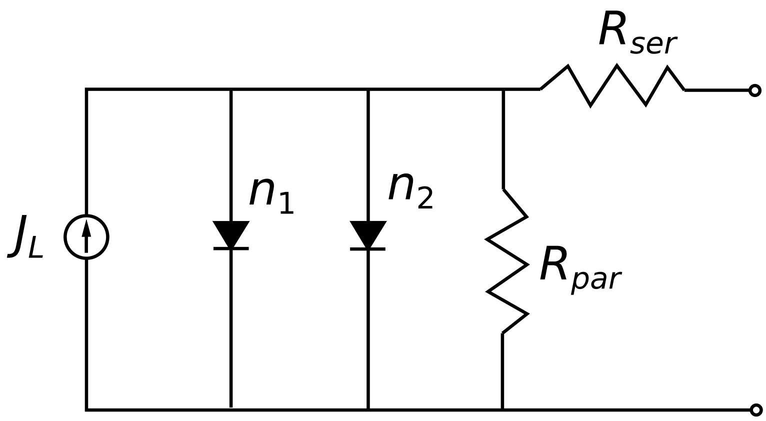


Fig. 2.3 Diagram of the 2-diode model equivalent circuit that is used to model solar cell electrical characteristics with labelled parameters: J_L, n_1, n_2, R_{ser} and R_{par}.

$$J = J_L - J_{01}\left\{\exp\left[\frac{q(V+JR_{ser})}{n_1 kT}\right]-1\right\} - J_{02}\left\{\exp\left[\frac{q(V+JR_{ser})}{n_2 kT}\right]-1\right\} - \frac{V+JR_{ser}}{R_{par}} \tag{2.5}$$

where J is the current density in mA/cm^2, J_L is the photocurrent, J_{01} is the dark saturation current of the first diode, q is the elemental charge, V is the voltage, R_{ser} is the series resistance, k is Boltzmann's constant, T is temperature and R_{par} is the parallel or "shunt" resistance.

2.3.3 Characterisation under illumination

A high J_{SC} indicates high levels of absorption between about 300 nm and the bandgap of the absorber material as this is the region where there is the highest irradiance from the solar spectrum. J_{SC} is a good metric for assessing the effectiveness of any light-trapping structures integrated into the solar cell design.

The maximum voltage a solar cell can produce occurs at open circuit. This V_{OC} value is affected by the recombination rate in the solar cell. Eq. 2.4 can be rearranged for V_{OC}:

$$V_{OC} = \frac{kT}{q}\ln\left(\frac{I_L}{I_0} + 1\right) \tag{2.6}$$

The fill factor (FF) of a solar cell is calculated in Equation 2.7 and is affected by parasitic resistance values.

$$FF = \frac{J_{mpp}V_{mpp}}{J_{SC}V_{OC}} \tag{2.7}$$

The overall power conversion efficiency of a solar cell is then calculated in Equation 2.8.

$$\eta = \frac{P_{mpp}}{P_{in}} = \frac{J_{SC}V_{OC}FF}{P_{in}} \tag{2.8}$$

2.3.4 Spectral response

The spectral response of a solar cell can also be analysed to provide more information about performance. By illuminating a solar cell with monochromatic light and measuring the current produced, the quantum efficiency can be analysed. External quantum efficiency (EQE) measures the ratio of electrons collected as current to incident photons. EQE data in this work is taken in discrete steps from 300 nm up to the bandgap of the absorber material at zero bias.

2.4 Light management in solar cells

During operation of a solar cell under illumination, there are optical losses that need to be minimised to produce the best possible device performance. Shading losses due to front surface contacts should be minimised while also providing short pathways for carriers to flow from the junction to the contact to avoid excess series resistance and therefore a degradation in fill factor. Some light will also be reflected off the front surface of the solar cell or pass through the device without being absorbed. Anti-reflection coatings are used to minimise front surface reflection. Light-scattering structures can be used at the front or rear surface to increase the optical path length through a solar cell and reduce transmission loss.

For monocrystalline Si solar cells with absorber layer thicknesses on the order of microns, front or rear surfaces can be textured through an anisotropic wet chemical etch step [48]. This creates pyramidal structures that reduce reflection and increase optical path length by scattering light. For solar cells with absorber layers on the order of 100 nm, such as the ultra-thin GaAs solar cells in this thesis, light management structures on the front and rear surfaces must have much smaller length scales in order to enhance absorption.

2.4.1 Anti-reflection coatings

Anti-reflection coatings (ARC) are commonly used in solar cells to reduce the front-surface reflection of light. The material and coating thickness are carefully chosen so that reflected light from the air to ARC interface interferes destructively with the light reflected from the ARC to solar cell interface. The wavelength at which this interference is destructive should be adjusted to align with the maximum point of the solar spectrum. This maximises the efficiency boost that a front surface ARC provides. Equation 2.9 can be used to calculate the ideal ARC film thickness for a specific wavelength of light.

$$d = \frac{\lambda}{4n_{ARC}} \tag{2.9}$$

where d is the film thickness, λ is the wavelength of the incident light, and n_{ARC} is the refractive index of the ARC. The ARC also performs most effectively when its refractive index is the mean of the refractive indices of the air, n_{air} and the solar cell material, n_{semi}. This ideal value is calculated in Equation 2.10.

$$n_{ARC} = \sqrt{n_{air}n_{semi}} \tag{2.10}$$

Multiple layer ARC coatings can further reduce front-surface reflection. In practice, the number of ARC layers rarely exceeds two as there is a diminishing reduction of reflection past two layers and significant added manufacturing complexity. Very thin single layer anti-reflection coatings (SLARC) are optimal for the ultra-thin regime where any parasitic absorption at the front surface can have a significant effect.

2.4.2 Light-trapping structures

Light-trapping structures are used to make ultra-thin cells behave as optically thicker devices. The goal of light-scattering is to increase the optical path length of incident photons to increase the likelihood of photon absorption and photogeneration. These structures increase the short-circuit current by increasing the likelihood that a photon is absorbed and therefore contributes to photocurrent [49]. This is particularly important for long wavelength photons because they have higher absorption depths. As a simple first step towards boosting the absorption in a solar cell, a planar back surface mirror can be added. Highly reflective materials such as Ag are good candidates. This mirror enhances light absorption by doubling the path length of light through the absorber layer.

To move beyond double-pass absorption from a planar mirror, a non-planar light-trapping structure can be used. This structure can either be a disordered, "randomised" surface [50] or a periodic structure [36, 51, 52]. Light management can give further performance benefits beyond increasing the optical path length. Bulk recombination and resistivity losses can be reduced since a thinner layer of material is needed to absorb the same number of photons.

Structures can be placed on the front surface of solar cells which can be easier to fabricate compared with a rear surface structure. The limitation of using the front surface, however, is that gains in short circuit current from increased optical path length can be cancelled out by parasitic absorption of short wavelength photons at this front surface. The back-surface scattering layer comes with its own challenges in terms of fabrication. The structure must be either grown as part of the solar cell layer stack or the layers must be grown in an inverted orientation so the light-trapping layer may be added before flipping and bonding the design to a different host substrate.

Boosting light absorption in the ultra-thin regime requires a different approach to those used in cells that are orders of magnitude thicker such as conventional Si cells. Since incident light can be approximated as coherent over the length scale of the ultra-thin absorber layer, standard light-trapping methods would not enhance performance. Moreover, the ultra-thin scale rules out random texturation like the anisotropic etches used for Si as the feature sizes would be orders of magnitude larger than the ultra-thin layers. A structure with nanoscale features is therefore needed.

There are a variety of methods for fabricating these nanoscale light management structures, each with their own benefits and drawbacks. These will be discussed in detail in Section 4.2.2.

2.4.3 Optical simulation of light-trapping in ultra-thin solar cells

A variety of models and techniques can be applied to a solar cell design to predict performance. Different optical modelling methods are appropriate for different length scales and take into account different optical effects. A first approximation of solar cell performance can be calculated through the Beer-Lambert Law discussed in Section 2.2.2. This method does not take into account any surface effects such as front surface reflection or any scattering of light.

Ray-tracing is an optical method which calculates reflection and refraction at material interfaces. This method is only applicable for describing systems that have feature sizes much larger than the wavelength of light as this means interference and diffraction effects can be ignored [53]. This method is therefore not applicable to the ultra-thin regime where the length-scale of the device is in the same order of magnitude as the wavelengths of the incident photons.

The transfer matrix method (TMM) [54] can be used to more accurately predict the reflection, transmission and absorption of light at multiple interfaces and any interference effects that are produced. This wave-optical method has the drawback that it can only describe planar layers and an effective medium approximation must be used to model structures incorporating more than one material in a single layer. TMM is accurate in the ultra-thin regime and is used in this thesis to model planar device structures.

Rigorous coupled wave analysis (RCWA) [55] uses Maxwell's equations to model periodic structures and is used in this thesis to simulate ultra-thin solar cells with integrated nanoscale light management structures.

2.5 Optimising electrical contacts

In order to extract current from a solar cell p-n junction, contacts must be formed to both the p and n sides of the device. For optimal solar cell performance the contact should be "ohmic" which means that, during an I-V sweep, the relationship between current and voltage is linear. This is shown in Figure 2.4 on the left and contrasted to a non-ohmic (or "rectifying" contact) where the current and voltage are non-linear. The symmetric curve in b) is for a pair of back-to-back rectifying contacts. A single rectifying contact would show a non-symmetric curve.

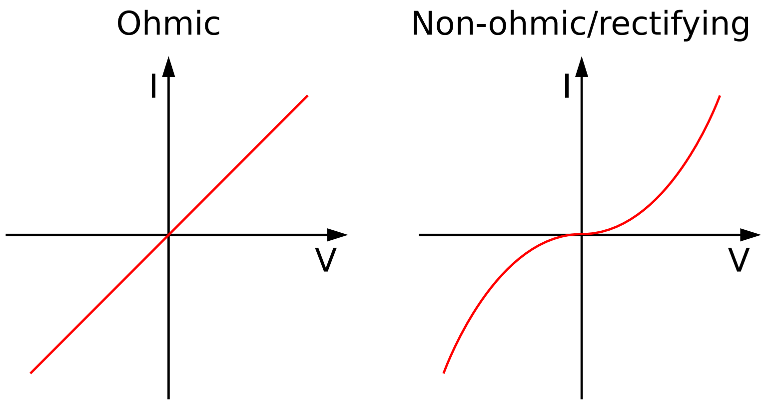


Fig. 2.4 Example current-voltage plots for ohmic (left) and non-ohmic/rectifying contacts (right).

Transport across a metal-semiconductor interface depends on the work functions of the two different materials. When they are brought into intimate contact, a depletion region forms and the characteristics of this region affect the transport of carriers.

There are three different mechanisms whereby electrons move across the interface between a metal and a semiconductor. These are: thermionic emission, thermionic-field emission and field emission [56]. Thermionic emission (TE) occurs when carriers travel over the top of the potential barrier between the metal and semiconductor. TE is the dominant mechanism in non-ohmic/rectifying diodes. Field emission (FE) is the preferred mechanism for carriers to move across the barrier and lead to an ohmic contact. During FE, the carrier tunnels through the barrier to the other side. The third mechanism is thermionic field emission (TFE) which is a combination of thermionic and field emission whereby the electron tunnels through the upper part of the potential barrier.

When forming contacts, parallel resistance should be maximised thus ensuring alternate pathways through the junction are not available to carriers. Series resistance should be minimised to ensure carriers are able to flow easily to the contacts and through to the external circuit. Series resistance is the sum of the two contact resistances at either side of the junction and lateral resistances in the absorber layer.

There are a variety of materials and techniques for forming high quality electrical contacts to standard semiconductor solar cells. Aluminium is commonly used for contacting to both p and n-type silicon. For GaAs, alloys of Ni, Ge and Au are common for the n-type contact and Ti, Pt, Zn and Au for the p-type [57, 58].

Thermal evaporation of metals onto the surface of III-V solar cells with a photolithography lift-off step is a commonly used method to form the desired contacting pattern [59]. Metal contacts can also be added via other techniques such as sputtering [60] however these methods present difficulties in the ultra-thin regime due to their potential for causing excess diffusion of the metals into the active layers of the device. Therefore thermal evaporation was chosen to produce metal contacts to the ultra-thin solar cells in this thesis.

2.5.1 Contact resistance

Once an ohmic contact has been formed, with FE as the dominant mechanism of carrier transfer, the contact resistance of the interface can be quantified. The total resistance measured across two metal contacts interfacing with a section of semiconductor material is R_{total}. This is the total resistance value inhibiting the free flow of electrons and can be calculated using Equation 2.11.

$$R_{total} = 2R_m + 2R_c + R_{semi} \tag{2.11}$$

where R_m is the resistance in the metalisation, R_c is the contact resistance and R_{semi} is the resistance in the semiconductor material. We can assume that R_c » R_m and neglect the R_m term to get Equation 2.12

$$R_{total} = 2R_c + R_{semi} \tag{2.12}$$

Therefore an I-V sweep taken by probing to two contact pads on a semiconductor slab will give the sum of the resistance in the semiconductor, which is affected by the distance that separates the two contact pads, and the contact resistances at each of the two metal-semiconductor interfaces. In order to isolate a generalised parameter for resistance, a systematic approach is needed. The goal is to measure the contact resistivity, ρ_c, in units of Ωcm^2. This value can then be used to directly compare the quality of a contact as it is independent of the geometry of the contacts. ρ_c is the product of the contact resistance, R_c, and the area of the contact, A_c, as shown in Equation 2.13.

$$\rho_c = R_c A_c \tag{2.13}$$

2.5.2 Transmission line measurement method

Transmission line measurement (TLM) is a method commonly used to determine the resistivity, ρ_c, of the interface between a semiconductor and a metal [61]. First, a bulk wafer of the semiconductor that is under test needs to be produced. This wafer needs to be just the bulk semiconductor of interest as opposed to a multi-layered structure. This is because carriers can penetrate below the surface of a multilayer structure of a device which produces compound effects from different sheet resistances and the presence of different depletion layers. A TLM of a bulk layer allows the independent extraction of contact resistances.

A mesa etch is carried out to create channels on this surface and confine the path of the carriers when I-V sweeps are carried out. Metal contacts are then evaporated onto these channels and an anneal is carried out if needed. Figure 2.5 shows an example TLM pattern with yellow sections showing the metal contacts and the blue area showing the mesa. An I-V sweep is then carried out by probing to pairs of contact pads with increasing distance between them. This spacing is dictated by the photolithography mask used (denoted by L_1, L_2, L_3 etc.). If ohmic contacts have been achieved, the resistances at each spacing can be calculated from the I-V sweep. These resistances are then plotted against spacing and a line of best fit can be calculated as shown in Figure 2.6. The y-intercept of this line of best fit is equal to twice the contact resistivity of the metalisation. In this way, different doping levels, metal layer combinations, and anneal conditions can be compared in terms of the contact resistivities they produce.

Measuring the area of the contact A_c in Equation 2.13, is more complicated than simply measuring the area of metalisation pad over the semiconductor. This is because current does not move uniformly beneath a metal-semiconductor interface. There is a phenomenon called "current crowding" [62] that means the current flowing into the metal area is highest at the edge and tails off as distance from the edge is increased.

The magnitude of the x-intercept of the line of best fit in Figure 2.6 is equal to $2L_T$. L_T is the transfer length which is a measure of the distance that a carrier travels in the semiconductor underneath the contact before being collected. Using L_T rather than the width of the contact pad is a more accurate measure of contact area A_c. This is shown in Equation 2.14

$$A_c = WL_T \tag{2.14}$$

where W is the width of the mesa etched channel as shown in Figure 2.5.

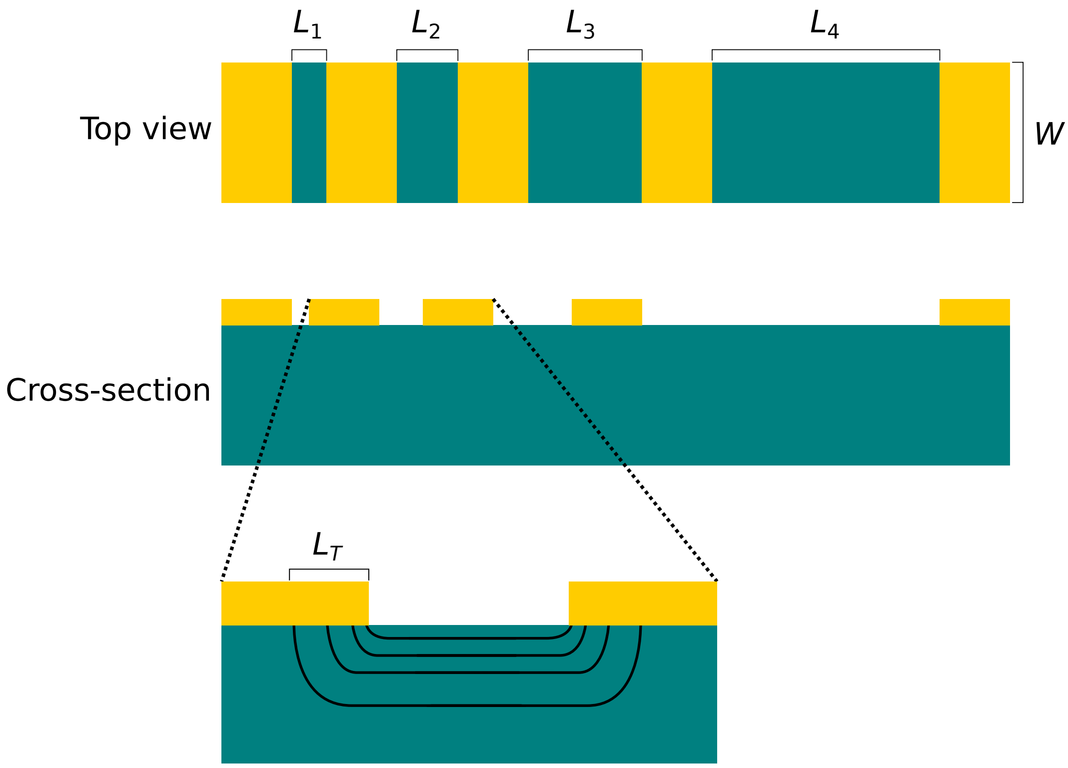


Fig. 2.5 Diagram of a TLM sample showing top view, cross-sectional view and a visualisation of transfer length, L_T, yellow areas represent metalisation, blue areas are semiconductor contact layer material. L_1, L_2, L_3 and L_4 show the different spacings between each pad of metalisation that is essential for TLM analysis.

2.6 Radiation damage in solar cell materials

As discussed in Chapter 1, satellites orbiting Earth and other planets are exposed to damaging radiation (mainly in the form of protons and electrons) that can cause degradation in the materials that make up on-board electronics and solar arrays. Energetic particles primarily cause displacement damage in the lattice structure of crystalline absorber layers [63]. In GaAs solar cells this means dislocations and interstitials are formed when atoms in the lattice are displaced from their original position. Higher energy particles can lead to compound effects with primary knock-on atoms causing clusters of defects.

2.6.1 Defect annealing

Defects in a solar cell can be unstable with the interstitial atom eventually returning to its original position [64, 65]. This can complicate the analysis of solar cell and semiconductor material degradation if defects are not stable. The time between the introduction of defects and defect density characterisation can be significant if annealing effects are present. Deep-

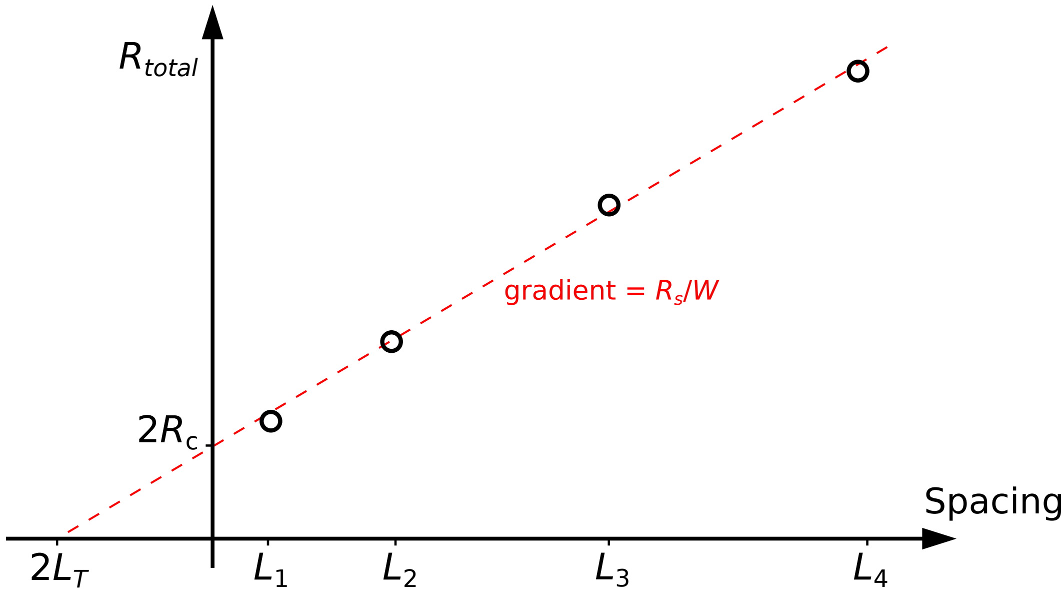


Fig. 2.6 Example of a TLM resistance versus spacing plot that can be used to calculate the contact resistance, R_c, and transfer length, L_T of a metal-semiconductor interface. The gradient of the line of best fit is equal to R_s divided by the width of the metalisation pad.

level transient spectroscopy (DLTS) can be used to analyse the density and nature of defects before and after annealing [66].

2.6.2 Defect tolerance of ultra-thin devices

Defects introduced by irradiation reduce the lifetime of carriers in solar cells. Higher densities of defects due to higher fluences of irradiation means the carriers are more likely to recombine at a defect site before being collected at the contacts. Ultra-thin GaAs solar cells have shown an intrinsic tolerance to the introduction of these radiation-induced defects [6, 67]. In Hirst et al. (2016) 80 nm single junction GaAs cells showed no degradation in short circuit current during 3 MeV proton irradiations whereas cells with absorber layer thicknesses of 800 nm and 3500 nm showed significant degradation.

The reason proposed for this intrinsic tolerance is that when the absorber layer is thinned down to the ultra-thin regime, the carriers have a shorter distance to travel before reaching the contacts of the device. This means that even with higher defect densities the carrier lifetimes are still long enough to allow them to be collected. The open circuit voltage of ultra-thin devices degrades with a similar profile to the thicker 800 nm and 3500 nm cells as expected.

2.6.3 Radiation tolerance testing methods

The overall goal of radiation testing of solar cells is to determine the rate of degradation of a given solar cell type as it is exposed to different fluences and types of damaging radiation. With a standardised procedure for this, different solar cell types can be directly compared in terms of their resilience to space radiation. The most common testing in the literature is exposing cells to protons and electrons at specific energies and analysing the degradation in solar cell performance due to the introduction of defects.

Pre and post exposure solar cell characterisation can be split into two broad categories: macroscopic analysis at the device level such as LIV and EQE, and microscopic analysis such as defect density and cathodoluminescence. Microscopic trends can be correlated to macroscopic results and provide insight into the mechanisms that decrease the performance of solar cells as they are exposed to radiation. Absolute values of performance metrics such as short circuit current and open circuit voltage give information about rates of degradation. Remaining factors of these performance metrics are also important to compare across device types with different beginning of life performances.

Radiation tolerance testing of solar cells can be extended beyond ground testing by progressing to flight testing [68] where solar cells are placed on spacecraft and their performance is tested while on orbit to analyse degradation in actual orbital conditions. Flight tests provide valuable data but are much more costly and complicated to execute so ground testing using particle beams is used in this thesis to investigate ultra-thin cells and their radiation-induced degradation.

2.6.4 Displacement damage dose method

Two methods for modelling solar cell degradation due to damaging radiation are considered. These are the equivalent fluence method developed by the Jet Propulsion Lab [69–71] and the displacement damage dose (DDD) method developed by the Naval Research Lab [72, 73]. This investigation uses the DDD method because it requires far fewer irradiation results in order to draw conclusions about the damage profile of devices.

The DDD method uses non-ionising energy loss (NIEL) [74] which is the amount of energy lost by an incident particle as it travels through the target material causing displacement defects. The energy deposited in the material is the DDD and is related to NIEL in Equation 2.15:

$$\mathrm{D} = (\mathrm{NIEL})\Phi \tag{2.15}$$

where D is the displacement damage dose and Φ is the fluence of damaging radiation in particles per unit area.

The DDD method applies to both proton and electron irradiation as well as to the degradation induced by gamma rays. However, for electrons and gamma rays more than one irradiation at different energies or further calculations are needed in order to find the performance degradation versus displacement damage curves for a specific solar cell type. Proton damage correlates directly to DDD and is therefore a good place to start when analysing the radiation tolerance of a specific solar cell type such as ultra-thin GaAs single-junction cells.

2.6.5 Modelling the space radiation environment

In order to extrapolate the results of radiation ground testing to on-orbit conditions, the space radiation environment needs to be quantified. Since the launch of the first solar-powered satellite in 1958, our understanding of the radiation profiles around Earth and other planets in our solar system has become more and more advanced. There is still uncertainty in the models used to predict radiation environments and therefore "worst-case" estimates for damaging radiation are most often used. This ensures that solar arrays are designed with large enough factors of safety to guarantee they can carry out their missions.

The radiation environment models used in this thesis are as follows: NASA AP9/AE9 for Earth orbits [75] and the Jovian Specification Environment model (JOSE) for orbits around Jupiter [76]. These models are implemented in the SPace ENVironment Information System (SPENVIS) developed by the European Space Agency [77]. In order to properly use SPENVIS, an orbit trajectory for the proposed mission needs to be specified. Data such as the spectra of radiation, integral proton/electron flux and ground track co-ordinates can then be extracted. From there, conclusions can be made about damage to solar arrays and mission lifetimes can be calculated.

Chapter 3

Device simulation and design

3.1 Introduction

Previous studies have shown the intrinsic radiation tolerance of GaAs solar cells with an ultra-thin (<100 nm) absorber layer [6, 33, 78]. 80 nm absorber layer devices have shown no degradation in J_{SC} when exposed to 3 MeV proton fluences up to 1×10^{14} p^{+}/cm^{2} without any protective coverglass in place. In contrast, cells with absorber layers an order of magnitude thicker had degraded to less than 30% of their original J_{SC} value [6]. The theory behind this tolerance to damaging radiation is explained in section 2.6.2. In order to take advantage of this feature, while maintaining good beginning of life device performance, ultra-thin cells must have carefully designed contact and passivation layers as well as integrated light management features to mitigate high transmission losses near the bandgap of GaAs. Previous studies have reached 19.9% efficiency (under AM1.5 illumination) for a 205 nm GaAs absorber layer with a periodic nanostructured light management layer [36]. Performance improvements for ultra-thin devices are ongoing [35].

This chapter details the design process of single-junction GaAs solar cells with an absorber layer thickness of 80 nm. These are some of the thinnest solar cell device layer structures currently in the literature for any material system [79]. The device layer structure is designed to produce optimal electrical characteristics. Diode performance was analysed using the 2-diode model to look at parasitic resistance values. A transmission line measurement study was carried out to minimise contact resistivities of the n and p-type metalisations while avoiding excess diffusion of Au into the active layers of the ultra-thin device. These diffusion effects are particularly important to consider in the ultra-thin regime where a small amount of diffusion can penetrate through a large proportion of the overall device thickness.

Patrick See carried out the first set of metalisations and produced Figure 3.8. Figure 3.2 is adapted from a diagram produced by Louise Hirst. Ellipsometry measurements and data fittings to determine layer thicknesses were carried out by Phoebe Pearce. Chapters 4, 5 and 6 detail the devices that were produced using the layer structure designed and optimised in this chapter.

3.2 Ultra-thin device design

An 80 nm homojunction of GaAs was chosen as the absorber layer for the devices as this length scale has shown intrinsic radiation tolerance in previous studies [6]. GaAs was chosen since it is a well-established platform for development as the ultra-thin regime is explored. It has a near ideal bandgap for single junction devices and mature device fabrication methodology within thicker device regimes, making it a suitable platform for developing devices at this novel ultra-thin scale. While GaAs is well understood from a radiation damage perspective, as it forms the middle junction of current commercial space multi-junction cells, other III-V alloys such as InP [80, 81] are more resilient to radiation damage. InP and its related alloys also exhibit self passivation at surfaces. Ideally, the findings of the ultra-thin GaAs device development in this thesis could be translated to these other material systems such as InP in the future.

The design of ultra-thin devices requires more optimisation than simply reducing the thickness of the absorber layer. Passivation and contact layers must also be thinned to avoid high levels of parasitic absorption, maintain radiation tolerance and ensure flexible form factors are possible. Surface and interface defect states must be passivated as they degrade device performance by acting as carrier recombination sites. Interfaces are particularly important in the ultra-thin regime where surface effects dominate.

3.2.1 Lattice matching

In order to avoid the introduction of strain into the ultra-thin device layers, lattice matched materials should ideally be used for the epitaxial growth. Contact and passivation layer material choices are therefore based on the GaAs lattice constant of 5.65 Å since that is the chosen absorber material. Figure 3.1 gives a visual comparison of the lattice constants of some of the common III-V alloys that were considered for contact and passivation layers. As shown in Figure 3.1, a limited number of ternary alloys can be grown lattice matched to GaAs. These alloys such as InAlP and InGaP served as a starting point for narrowing the design space.

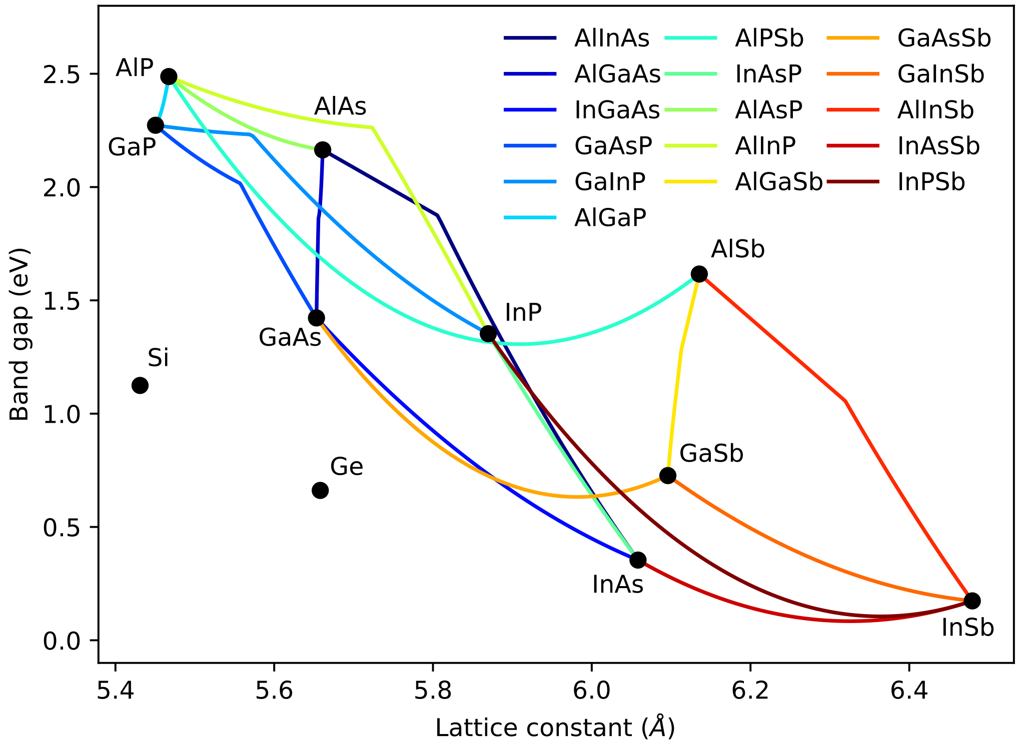


Fig. 3.1 Lattice constants of common III-V alloys plotted against material band gap. Lines connecting circles indicate the varying properties of ternary alloys. Plot from [3].

3.2.2 Passivation layers

Passivation layers are needed to ensure that carriers of the correct type are able to move freely towards the contacts and the opposite carriers are blocked. These layers can be natively grown from the same materials as the absorber layer or can be formed of non-native materials such as the use of alumina passivation layers for Si solar cells [82]. The best performance thin single-junction GaAs solar cells in the literature make use of high bandgap alloys as passivation layers [36] so this is the material system used for the ultra-thin devices.

High bandgap and/or indirect bandgap materials are desirable for barrier layers, particularly for the window layer as they will cause less parasitic absorption of shorter wavelength light. Passivation layer design can be adjusted in three ways: alloy composition, doping density and layer thickness. In theory the layer thickness should be kept to a minimum to avoid parasitic absorption and keep series resistance low. Heterojunctions between the absorber and passivation layers create depletion regions at the interfaces and introduce discontinuities in the band structure of the device. These discontinuities can be advantageous if they are blocking minority carriers but they can be detrimental if they introduce potential barriers to majority carriers.

Previous ultra-thin devices in the literature have made use of AlGaAs as passivation layers however this alloy is not lattice matched to GaAs. This could be a more significant issue for the 80 nm length scale chosen in this study as any strain introduced will likely have a more prominent impact. AlGaAs can also be a direct bandgap semiconductor depending on Al fraction which can introduce parasitic absorption.

Figure 3.2 shows the alloys considered for passivation for ultra-thin devices. Of the group of ternary alloys lattice matched to GaAs, AlP based alloys have lower valence band energies and are well suited for n-type barrier and GaP alloys have higher valence band energies and are therefore better suited to be a p-type barrier. InAlP and InGaP were found to have good band alignment with GaAs. InAlP is an indirect semiconductor which is desirable for passivation layers but InGaP is direct. InGaP and InAlP are fairly well lattice matched to GaAs with Ga and Al fractions of 0.51 and 0.53 respectively. Their band alignment was further adjusted with the addition of dopants as can be seen in Figure 3.2 b). Adjustment of alloy composition was pursued first because dopants introduce the potential for band-bending at the interface between barrier and absorber layers. Band alignments could be further optimised by the use of quaternary alloys but that is beyond the scope of the investigation.

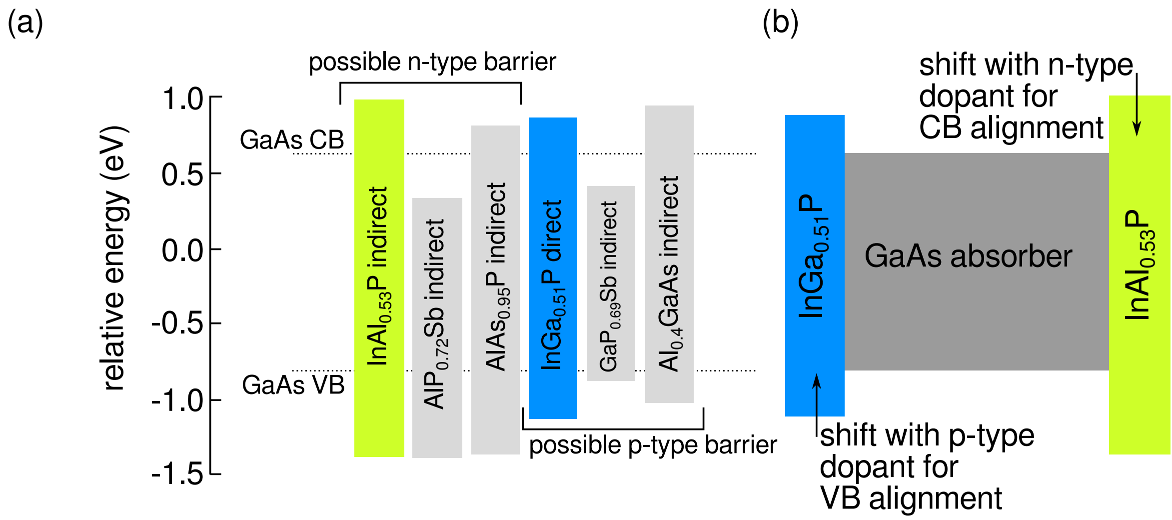


Fig. 3.2 Band alignment diagrams showing the optimisation of barrier layer material choice. a) Lattice matched ternary alloys investigated as possible barrier layers, b) Band alignment of InGaP and InAlP passivation layers with ultra-thin GaAs absorber layer.

Drift-diffusion simulations were carried out using Solcore [3] to simulate the band structure and dark current densities of the proposed structure with InGaP and InAlP barrier layers for different doping levels.

Figure 3.3 shows how simulation was used to understand trends in performance by varying different quantities such as passivation layer thickness. This figure shows how as the passivation layer thickness is increased, the dark current improves but quickly converges as the thickness reaches approximately 20 nm. Field effects are not taken into account in the drift-diffusion simulations so thinner barrier layers (2 nm, 5 nm etc) could have worse performance than predicted in Figure 3.3 due to tunneling effects. The passivation layer thicknesses were therefore set at 20 nm since going above this thickness does not improve the predicted electrical performance but would increase the parasitic absorption. With 20 nm passivation layers, the total active layer thickness of the structure is 120 nm.

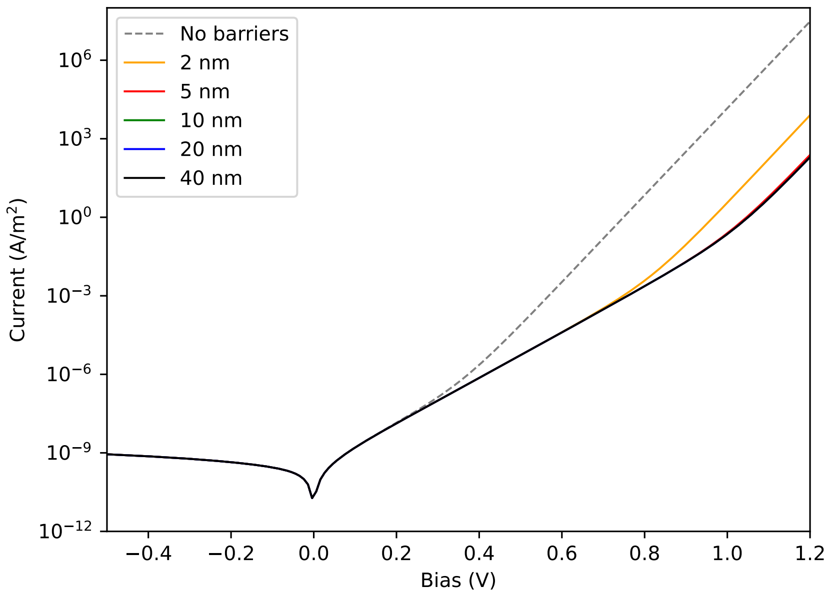


Fig. 3.3 Drift-diffusion simulation [3] analysing how a range of different passivation layer thicknesses affects the dark currents. Predicted dark IV curves show trends in performance as passivation layer thickness is increased.

3.2.3 Absorber doping density

Figure 3.4 a) and 3.4 b) show the range of absorber doping densities that were simulated. DIV simulations indicate that the higher doping of 1×10^{18} cm^{-3} could lead to lower dark current levels.

Two sets of wafers were available for growth so this gave the opportunity for designing two different layer structures to enable direct comparison later when fabricated into diodes and solar cell devices. Two different absorber layer doping densities were proposed to provide this comparison; 1×10^{18} and 1×10^{17} cm^{-3}. The 1×10^{18} cm^{-3} doping density is similar to what would be used in a more standard thick device. Chapter 4 presents only the results of devices produced with the wafers doped to 1×10^{18} cm^{-3}. Chapter 5 presents devices made with the other set of lower doped wafers.

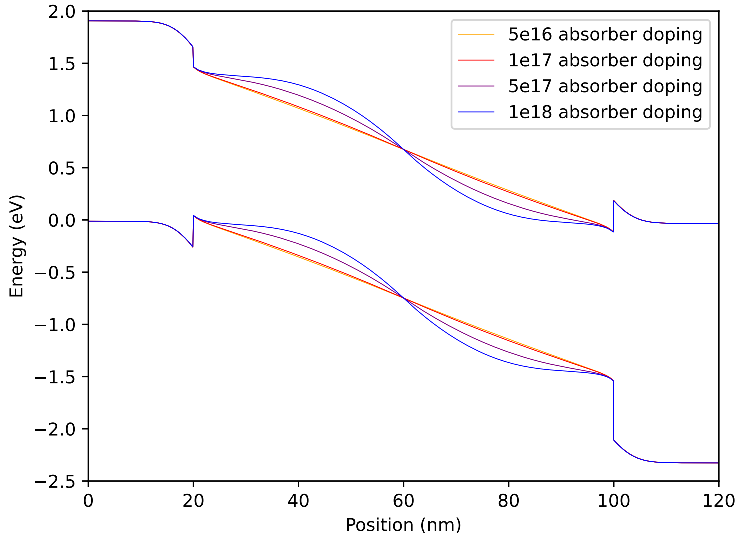
3.3 Contacting schemes

Forming high quality contacts between semiconductors and metals has been extensively explored. Parasitic resistances in solar cells can significantly degrade the efficient transport of carriers and therefore the overall device performance. The main goal of optimising contacts is to produce a contact that exhibits "ohmic" behavior where voltage and current are linearly related and to minimise the contact resistance (see Section 2.5). For an optimal metal-semiconductor interface field emission should dominate and this is best achieved with high doping densities in the semiconductor material. Adding highly-doped contact layers between the passivation layer and the metal contact on each side of the device allows for the formation of low resistance ohmic contacts. High doping lowers the potential barrier for carriers.

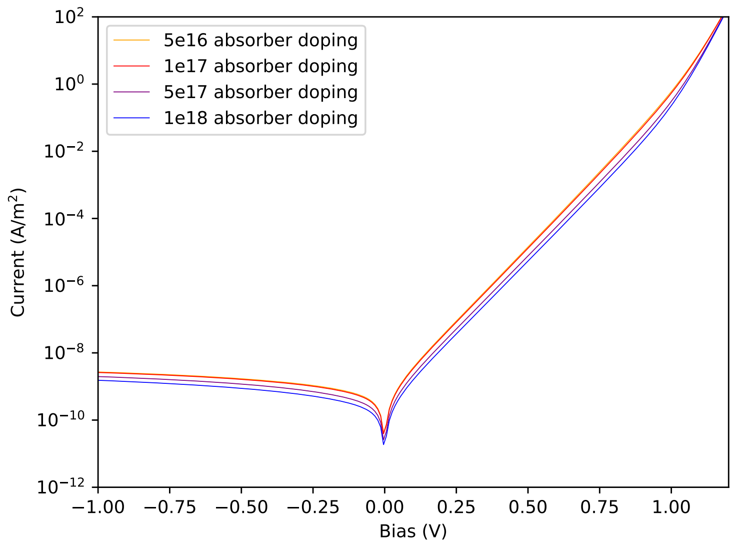
3.3.1 Metal contacts to GaAs

The electrical properties of the interface between doped GaAs and contact metalisation significantly affect the performance of the solar cell. The metalisation is often deposited using a photolithography step, thermal evaporation of layers of different metals/alloys then a lift-off step to leave metal only in the desired areas. After the lift-off step, an anneal can be carried out if needed to diffuse metal into the semiconductor contact layer and reduce resistivity.

Contacts made up of layers of Au, Ge and Ni are common for n-type contacts to GaAs [83]. Ni is commonly used as a thin first layer on top of the GaAs to aid with wetting. Au and Ge are then added in eutectic proportions. Another Ni layer and/or Au can be added on top to prevent balling of the AuGe layer [84] and encapsulate the layers underneath. Ti and Au are commonly used for p-type GaAs. Annealing is often necessary for metal-semiconductor contacts, particularly to n-type GaAs, to ensure they exhibit ohmic behavior. For AuGeNi n-type metalisation during the heating step Ge diffuses into the GaAs and forms the ohmic contact.



(a) Band structure



(b) Simulated dark IV

Fig. 3.4 Drift-diffusion simulations [3] showing a) band structures and b) dark IV of ultra-thin device design with varying absorber layer doping densities: 5×10^{16}, 1×10^{17}, 5×10^{17} and 1×10^{18} cm^{-3}. Passivation layer doping was set at 5×10^{18} cm^{-3} and 20 nm thicknesses.

3.3.2 TLM study design

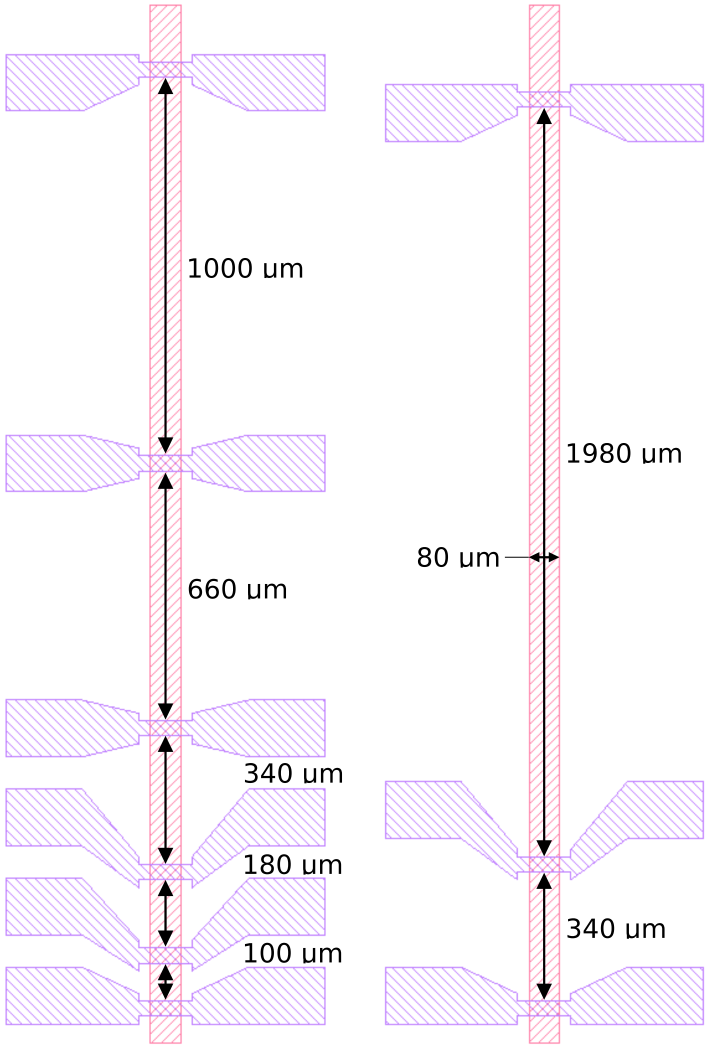


Fig. 3.5 Schematic of a transmission line measurement mesa and metalisation for determining the resistivity values of metal-semiconductor contacts. Pink areas show the mesa, purple is metalisation.

Section 2.5.2 explains the theory behind TLM measurements. A TLM study was carried out for the ultra-thin GaAs devices designed in this chapter in order to ensure high quality contacts were formed while avoiding any detrimental effects during metalisation and any annealing steps. The goals of the study were to find the optimised contact layer doping level, optimal anneal conditions for the contact metalisation and measure the contact resistivities achieved for both the p and n-type contacts. The TLM wafers used to measure different doping densities were all 1 micron of GaAs grown onto a native substrate. A range of doping levels and anneals were studied and compared in terms of the quality of the metal-semiconductor contact produced. Current voltage sweeps were carried out after the TLM contact schematic was evaporated onto the surface to determine the resistivity of the metal-semiconductor interface. Figure 3.5 is a schematic of the TLM mesa and metalisation that was used in the study. A contact resistivity value, R_c of less than 5×10^{-5} Ωcm^2 was identified as the overall goal of the TLM study for both p and n-type metalisation.

3.4 p-type contact

3.4.1 Contact layer doping density

The p-type contact metalisation resistivity was optimised by adjusting the Be doping concentration of the p-type GaAs contact layer. Initial tests used a non-annnealed contact. The metalisation used was Ti/Au with thicknesses of 20/200 nm. The Ti layer was used to aid adhesion to the GaAs contact layer surface. This is a standard metalisation that has shown high quality p-type contacts in the best-performing thin GaAs solar cells in the literature [36].

3.4.2 TLM results

Four different doping density samples were used for the p-type TLM study. When contact layer doping was increased above 5×10^{18} cm^{-3} the contact became ohmic as shown in Figure 3.6. For a doping level of 1×10^{19} cm^{-3} an ohmic contact was also achieved with a lower contact resistivity of 2.44×10^{-4} Ω cm^2. Table 3.1 lists the resistivities and doping densities for all p-type TLM samples. Figures 3.7 a) and 3.7 b) show the data analysis carried out to determine these contact resistivities from plots of TLM spacing versus measured resistance.

Since 1×10^{19} cm^{-3} is the highest possible doping level available for this material, the p-type contact has reached its optimal performance and this doping density was chosen as the final value for the layer structure design. 25 nm was chosen as the thickness for the p-type contact layer since no anneal is needed to achieve ohmic behavior so the diffusion of Au into the active region of the device is not a major concern and the layer can be very thin.

Since a non-annealed contact was found to be optimal for the p-type, this allows for an annealed n-type contact to be added first followed by the p-type contact. If the p-type contact were then to be annealed as well, the heating would further anneal the n-type metalisation and potentially degrade the shunt resistance by diffusing excess Au into the active layers of the device.

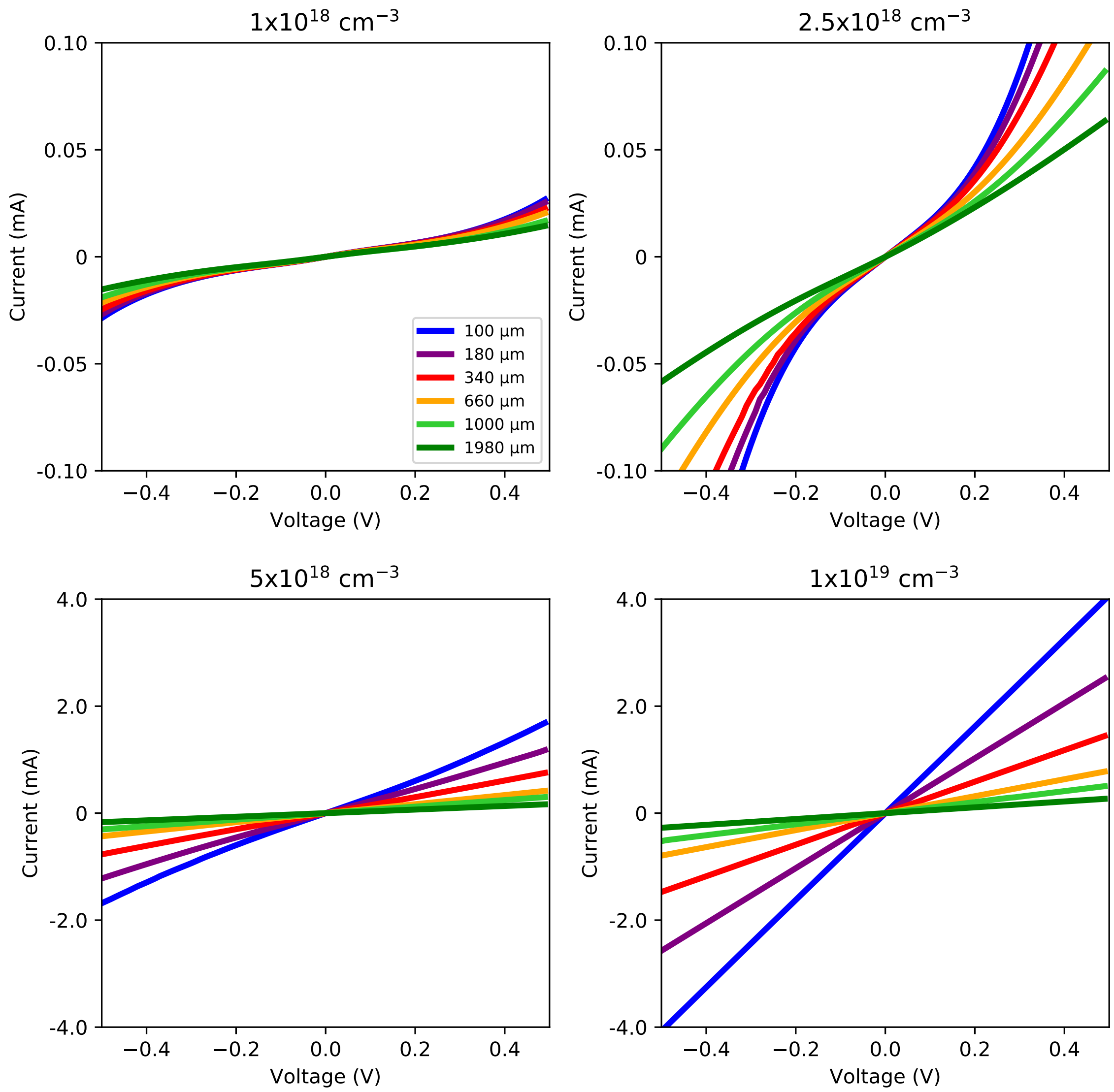
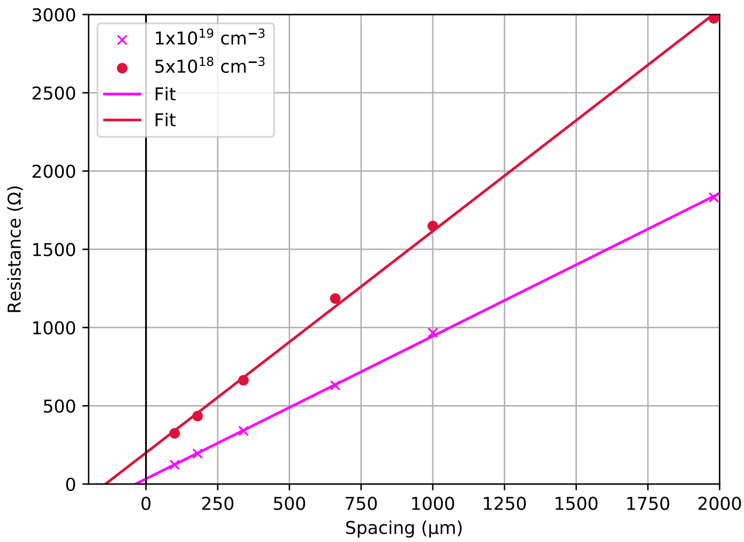


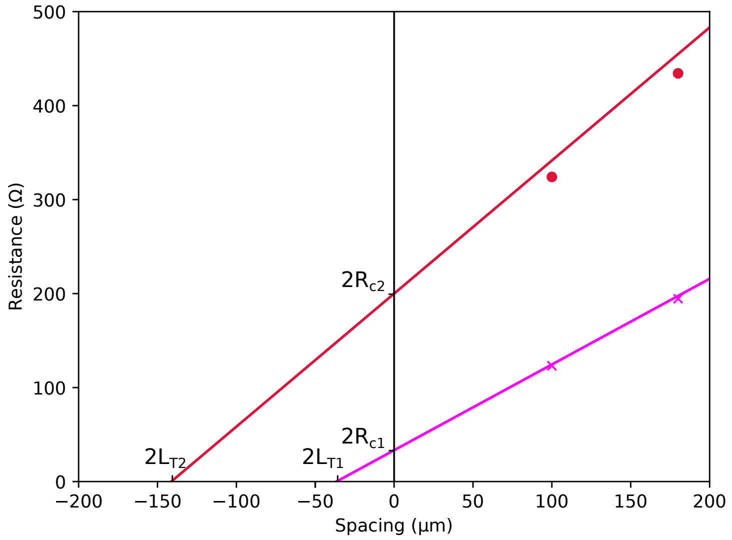
Fig. 3.6 p-type contact TLM results for four different doping density GaAs wafers metalised with 20/200 nm of Ti/Au. The top two plots show non-ohmic behavior while the bottom two plots show ohmic behavior. The highest doped sample showed the lowest contact resistivity.

3.5 n-type contact

A layered metal contact was chosen using 10/130/20/200 nm of Ni/AuGe/Ni/Au. The AuGe was used at a eutectic ratio of 88:12%. 176:24 mg placed into the evaporation boat resulted in approximately 130 nm of AuGe deposited). This layered metalisation approach was chosen instead of a NiGeAu mixture evaporated from one boat. The layered approach allows for



(a)



(b)

Fig. 3.7 a) p-type contact TLM results, resistance versus spacing. b) Line of best fit p-type contact TLM results, extrapolated to calculate contact resistance R_c and transfer length L_T for each doping condition.

a high quality contact with good surface topography. This metalisation was kept constant throughout TLM and device testing to allow direct comparison of anneal conditions.

3.5.1 Preliminary anneal optimisation

The n-type contact metalisation was investigated with the goal of finding the optimal contact layer doping density and anneal condition that would produce the lowest contact resistance while avoiding diffusion of Au into the active layers of the ultra-thin device. Therefore, preliminary n-type contact metalisation tests were carried out on TLM wafers followed by further anneal optimisation on actual ultra-thin solar cell devices after the full layer structure was grown by molecular beam epitaxy (MBE).

Using Si as the dopant for n-type GaAs means the maximum doping density value is limited [85]. This is because Si, a group IV element, can act as a donor or acceptor in GaAs depending on whether it sits on a Ga or As site. This effect is called autocompensation. A non-annealed n-type contact was attempted but was not successful in creating an ohmic contact at an initial doping level of 3×10^{18} cm^{-3}. Therefore an annealed n-type contact was likely needed so an n-on-p layer design was chosen for growth. This allowed the n-type contact to be annealed before the flip and bond process of removing the growth substrate and inverting the structure. This also meant that a thicker n-type contact layer (300 nm) was chosen to allow for an anneal and avoid degradation of shunt resistance if Au diffuses from the contact layer towards the active layers of the device during heating.

Chips with Si doped GaAs at a density of 3.0×10^{18} cm^{-3} were patterned with TLM patterns and annealed at the different conditions listed in Table 3.2. Figure 3.8 shows the preliminary TLM patterned samples after these anneals were carried out. For the longer and hotter anneals (as shown by the 80 seconds at 430°C micrographs) the surface of the contact begins to degrade and excess diffusion of Au into the active layers is likely. The TLM results for these samples show very low resistivities (see Table 3.2 for these results). Based on these encouraging results, the device layer structure was finalised and n-type contact anneal testing was carried out with on-wafer devices as well as with TLM analysis.

Table 3.1 p-type contact resistivity results for varying doping density, all samples metalised with 20/200 nm of Ti/Au.

Dopant	**Doping density** (cm^{-3})	**Anneal condition**	**Contact resistivity** (Ωcm^2)
Be	1.0×10^{18}	None	Non-ohmic
Be	2.5×10^{18}	None	Non-ohmic
Be	5.0×10^{18}	None	5.65×10^{-3}
Be	1.0×10^{19}	None	2.44×10^{-4}

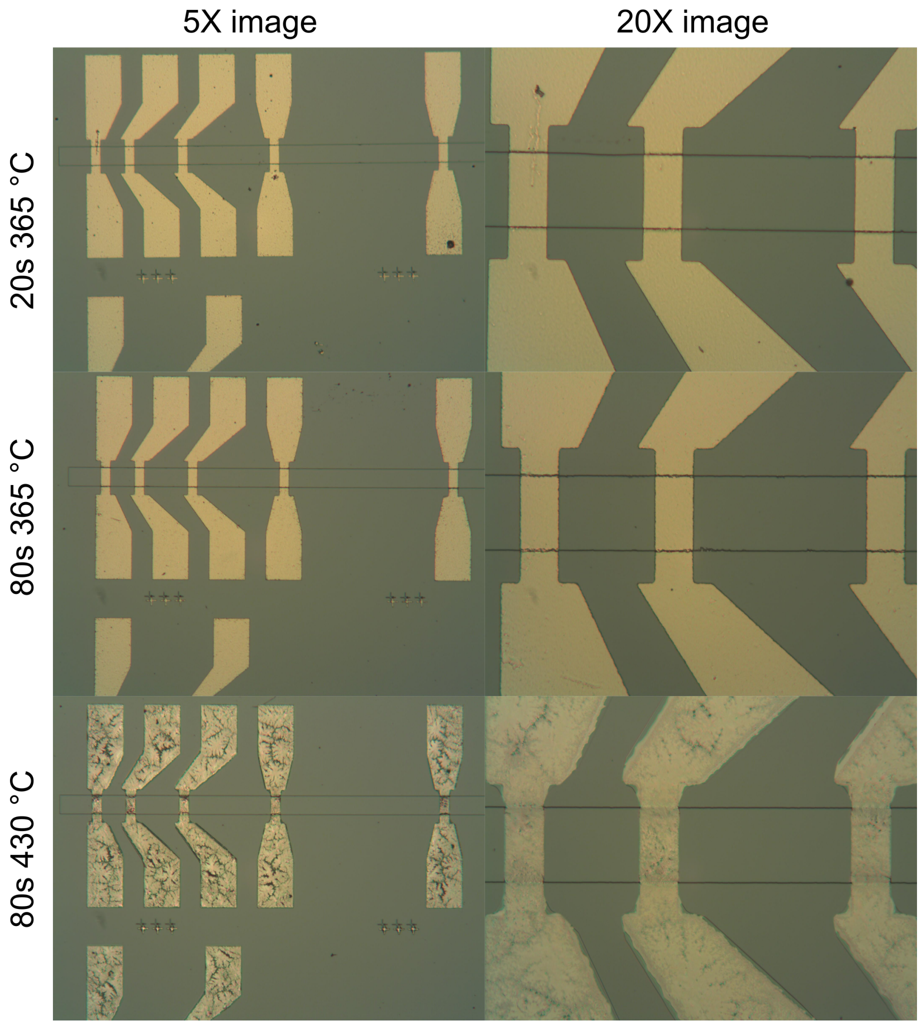


Fig. 3.8 TLM micrographs taken by Patrick See.

Table 3.2 n-type contact resistivity results for 3.0×10^{18} cm^{-3} doped GaAs for varying anneal conditions. All samples were metalised with 10/130/20/200 nm of Ni/AuGe/Ni/Au.

Dopant	**Doping density** (cm^{-3})	**Anneal condition**	**Contact resistivity** (Ωcm^2)
Si	3.0×10^{18}	20 seconds, 365°C	1.61×10^{-7}
Si	3.0×10^{18}	80 seconds, 365°C	1.42×10^{-8}
Si	3.0×10^{18}	80 seconds, 430°C	1.05×10^{-6}

3.5.2 Contact layer design

The device layer structure was finalised and grown by MBE on 4 inch GaAs wafers. This design is detailed in Section 3.6. 5.0×10^{18} cm^{-3} was chosen as the doping density of the n-type contact layer with the goal of being able to reduce the anneal time and temperature when compared to 3.0×10^{18} cm^{-3} but still achieve an ohmic contact. A TLM wafer with 1 micron of 5.0×10^{18} cm^{-3} GaAs was used in conjunction with the full device wafers to further optimise the anneal balancing contact resistivity with actual device performance.

3.5.3 TLM and device anneal study

The first round of on-wafer devices were processed (see Section 4.3.2 for fabrication details) with an anneal of 50 seconds at 365°C. These devices showed degraded parallel resistance when dark IV sweeps were taken and the 2-diode model was fitted to the data. This indicates that excess Au diffusion or other damage mechanisms had taken place for anneals in the 50 seconds at 365°C range.

Next, TLM wafers with the higher doping density of 5.0×10^{18} cm^{-3} were tested with the same metalisation but no anneal to see if this would produce an ohmic contact. A non-annealed contact would be ideal since diffusion of Au during heating would be avoided and therefore the contact layer thickness could be reduced as a thick buffer would no longer be needed. However, the non-annealed contact and shorter anneals at lower temperatures did not produce ohmic contacts as shown in Table 3.3.

Table 3.3 n-type contact resistivity results for varying anneal conditions, all samples were metalised with 10/130/20/200 nm of Ni/AuGe/Ni/Au.

Dopant	**Doping density** (cm^{-3})	**Anneal condition**	**Contact resistivity** (Ωcm^2)
Si	5.0×10^{18}	None	Non-ohmic
Si	5.0×10^{18}	20 seconds, 335°C	Non-ohmic
Si	5.0×10^{18}	50 seconds, 335°C	1.47×10^{-3}
Si	5.0×10^{18}	80 seconds, 335°C	1.48×10^{-3}
Si	5.0×10^{18}	20 seconds, 350°C	3.66×10^{-3}
Si	5.0×10^{18}	80 seconds, 350°C	4.10×10^{-4}
Si	5.0×10^{18}	20 seconds, 365°C	9.10×10^{-4}
Si	5.0×10^{18}	80 seconds, 365°C	1.14×10^{-3}

An anneal condition of 20 seconds at 350°C was ultimately chosen as the ideal condition for the n-type contact as it produced an ohmic contact in TLM analysis and the best parallel resistance values in fabricated devices (fabrication discussed in Section 4.3.2) after 2-diode model analysis.

3.6 Optimised layer structure

Table 3.4 shows the optimised layer structure as grown by molecular beam epitaxy (MBE). The epitaxial layers were grown on 4 inch GaAs growth wafers with a thickness of 625 μm. The "measured thickness" in the last column was taken by spectroscopic ellipsometry (SE) measurements from six different samples from the wafers with 1×10^{18} cm^{-3} absorber layer doping density. This provided more accurate data about the thickness of each layer as grown. The six samples were produced by selectively etching away each layer of the stack in Table 3.4 using alternating NH_4OH and HCl based etchants (2:1:10 ratio of NH_4OH:H_2O_2:H_2O and 1:5 ratio of HCl:H_2O).

The SE measurements also gave the n and k values (real and imaginary parts of the refractive index) of each specific material which were then used in simulations. SE measurements were done using a Woollam V-VASE ellipsometer with a wavelength range of 250-1000 nm at angles of incidence of 65°, 70° and 75° [86].

Data from the chip with just the InAlP etch stop layer and the GaAs substrate was fitted first. A multi-layer model was used with a semi-infinite GaAs slab, InAlP layer and an InAlP native oxide. Each subsequent sample with one more layer on top each time (and native oxide) was then added to the model to build up a complete analysis of the layer structure. The native oxide in each case was found to have a thickness of 1-2 nm. It was not possible to differentiate between the n and p-doped absorber layers so they were analysed as a single layer and were found to have a combined thickness of 87 nm.

Table 3.4 Optimised ultra-thin device layer structure as grown by MBE, two different wafers were grown to compare two absorber layer doping densities so x = 17 or 18. Measured thickness values were taken from a wafer with 1×10^{18} cm^{-3} absorber layer doping density.

Material	Role	Dopant	Doping density (cm^{-3})	Target thickness (nm)	Measured thickness (nm)
GaAs	n-type contact	Si	5×10^{18}	300	318
$In_{0.47}Al_{0.53}P$	Hole barrier	Si	5×10^{18}	20	17
GaAs	n-type absorber	Si	1×10^{x}	40	87
GaAs	p-type absorber	Be	1×10^{x}	40	
$In_{0.49}Ga_{0.51}P$	Electron barrier	Be	5×10^{18}	20	19
GaAs	p-type contact	Be	1×10^{19}	25	25
$In_{0.47}Al_{0.53}P$	Etch stop			150	145
GaAs	Substrate			-	-

Chapter 4

Ultra-thin GaAs solar cells with nanophotonic light-trapping layer

4.1 Introduction

A novel 80 nm device with an integrated light-trapping layer was designed, fabricated and characterised with particular focus on applications as a space power system. Device fabrication methods were developed to produce on and off-wafer devices for comparing planar and nanostructured embodiments.

Device performance results for three different types of devices are detailed. The three devices are on-wafer planar, off-wafer planar with an integrated Ag back surface mirror and off-wafer with an integrated nanophotonic metal-dielectric grating. Devices were analysed and compared using standard techniques including external quantum efficiency (EQE), current-voltage sweeps in the dark (DIV) and light current voltage sweeps under 1-sun AM0 spectrum (LIV) as these devices are designed to be used in the space environment. Detailed simulation and optical analysis was carried out by Eduardo Camarillo Abad and Phoebe Pearce to confirm that Fabry-Perot and waveguide modes contribute to the increase in absorption seen in the off-wafer devices. Eduardo produced Figure 4.11 and Phoebe produced Figures 4.12 and 4.13. Pierre Chausse carried out the DTL patterning steps which are detailed in Section 4.3.4 and produced the images used in Figures 4.7 and 4.8.

The main results of this chapter have been published in a conference proceeding [87] and a journal article titled *"Ultra-thin GaAs solar cells with nanophotonic metal-dielectric diffraction gratings fabricated with displacement Talbot lithography"* [4].

4.1.1 Absorption in the ultra-thin regime

Along with band structure, lattice matching etc., the absorption characteristics of a specific layer structure must be considered. Absorption in GaAs slabs with a variety of thicknesses is plotted for incident light in the wavelength range from 300-1000 nm in Figure 4.1. The extinction coefficient values for this figure were measured through ellipsometry from GaAs grown under the same conditions as the absorber layer GaAs that was used to make devices.

For the 50 nm slab the absorption is near 1 for the shorter wavelength region but it drops sharply past about 450 nm. When the absorber thickness is reduced below about 80 nm the absorption in the 300-400 nm region also begins to degrade. A slab with 3000 nm however, is highly absorbing until very close to the GaAs band edge. Therefore when working in the ultra-thin regime, boosting absorption in the longer wavelength regions of the spectrum is important. In order to do this, the optical path length of incident photons through the active layers of the device needs to be increased.

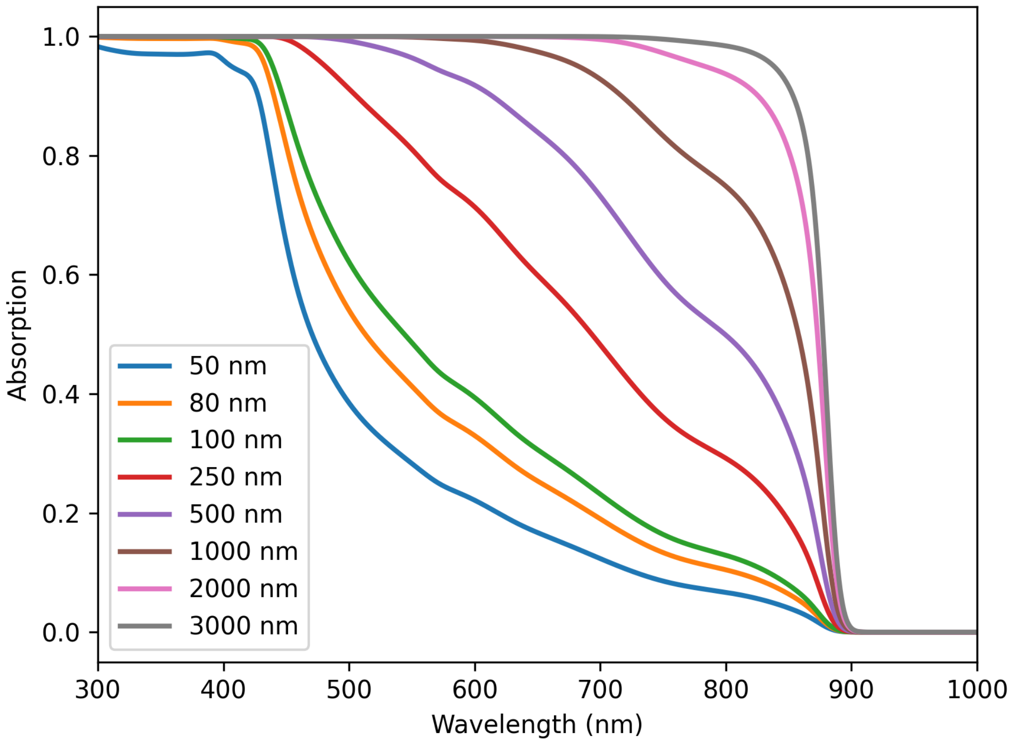


Fig. 4.1 Absorption as a function of wavelength for different thicknesses of GaAs slab.

4.2 Light management structure for the ultra-thin regime

In order to increase the optical path length of incident photons through the absorber layer of the ultra-thin cells, a light management layer must be introduced. To go beyond the double pass limit, the light must be scattered into totally internally reflected modes. For the ultra-thin regime we are working with, the features of this structure must be on the order of the wavelength of the incident light. This means standard contact photolithography techniques for producing III-V solar cells will not be able to produce sufficiently high resolution light management layers. The effect of the proposed nanophotonic layer on device performance was first optimised through simulation and different fabrication techniques.

4.2.1 Design and simulation

When simulating the optical properties of a solar cell, different methodologies can be employed. The Beer-Lambert law (Equation 2.2) gives an approximation of the absorption in a single layer of material. Ray-tracing can be used for structures with features much larger than the wavelength of light (such as pyramidally textured Si cells with absorber layers on the order of hundreds of microns). The transfer matrix method (TMM) can give absorption characteristics of multi-layered structures at the nanometer scale with different material interfaces. The effective medium approximation is used by TMM to incorporate 3D structures such as diffraction gratings. This approximation averages the optical properties of the component materials weighted by volume. However, this technique will only consider specular reflection and associated interference. It will not consider diffraction effects.

Rigorous coupled-wave analysis (RCWA) is a Fourier technique that goes a step further than TMM by solving Maxwell's equations and can handle complex nanostructured layers. RCWA simulations were carried out by Eduardo Camarillo Abad and Phoebe Pearce to optimise the design of the nanostructured light management layer for the 80 nm devices. These simulations indicated that a photonic crystal design with a periodic structure was the optimal design and was chosen over randomly textured or quasi-random structures [88]. A metal-dielectric photonic crystal structure was chosen for this first iteration of devices. For structures that incorporate metals, an ordered array design is favorable. When using more absorbing materials along with highly reflective metals, the structure must be carefully optimised to fully exploit the benefit of the structure.

4.2.2 Methods for fabricating nanostructures

Various methods for fabricating structures with nanoscale features have been explored. Desirable qualities of the process for making the structure include: uniformity of the grating, large-area coverage, ability to alter the dimensions and structure of the grating, scalability, repeatability, non-destructive to equipment, good coverage over significant topography and more.

Using electron beam lithography to nano-pattern a resist followed by an etch step could provide sufficient resolution and great flexibility in the design of the pattern but the technique is expensive and time-intensive.

Self-assembly of nanospheres has been explored as a method for patterning [89, 90]. A suspension of nanospheres is coated onto the surface then used as a mask for an etching or deposition step. However, issues of uniformity of the resulting pattern are persistent which mean this method has not been developed to a point where it would be useful for integration into ultra-thin solar cell processing.

Nanoimprint lithography has been used to pattern a 205 nm GaAs cell and achieve 19.9% AM1.5 efficiency [36]. This method produces high quality structures at the nanoscale [91, 92] but requires contact between the sample and a patterned mold. This means there is wear on the mold with each use and it must be regularly replaced. This process is also hindered by particulate contamination and is not compatible with substrate topography.

Polymer blend lithography has been used for a 260 nm device achieving 22.35% AM1.5 efficiency [43]. This is an interesting technique for producing randomised nanostructures but it does not provide control over the exact pattern created. Anisotropic wet etching of a GaP layer has shown good light-trapping properties [93] but it also does not provide precise control over the design of the features.

4.2.3 Displacement Talbot Lithography

Displacement Talbot Lithography (DTL) was found to achieve nearly all of the desired qualities of a nanoscale patterning process. DTL is a recently developed photolithographic technique that can produce high aspect ratio structures with feature sizes down to about 100 nm. DTL has many advantages over other methods including that it produces a high-quality grating structure, the process is wafer-scale, the mask can be reused infinite times (as there is no contact with the sample) and the grating showed good uniformity over the significant topography of the n-type contacts used for the devices in this study.

The DTL method creates a 3D interference pattern [94] that repeats every Talbot period by shining monochromatic, collimated light through a grating. For this project a resist is patterned using the DTL process then an etch is carried out to pattern the film below the resist. The DTL method can also be used in a lift-off process. Since the effective image is independent of the distance between mask and sample [95], the method can be used on a substrate with significant topography. DTL has so far shown great results in the nano-patterning of III-nitride materials and in producing metal-dielectric gratings [96]. This is the first time that DTL has been used for a PV application and is therefore an exciting advancement for the field of nano-structured solar cells.

The DTL mask is produced by electron beam lithography or interference lithography. This means it is an expensive item to make but, since there is no contact between sample and mask, it can be used infinitely. Therefore this technique is cost effective at scale. The mask dictates the pitch of the features and the grating geometry as well as the shape of the features in the unit cell (e.g. circle, square). For these devices a hexagonal pattern of circles was used which produced a dielectric layer with cylindrical holes in a hexagonal array. The exposure dose during DTL determines the diameter of the holes. After etching, another material can be layered over the top of the patterned film to fill in the holes.

4.2.4 Optimised structure

SiN and Ag were chosen as the two materials for the light-trapping layer. RCWA simulations were used to design the array geometry in terms of pitch, Ag coverage and grating thickness. The final design is a hexagonal array of circular pillars with a 300 nm diameter and a pitch of 500 nm. Figure 4.2 shows the optimised unit cell of the metal-dielectric structure.

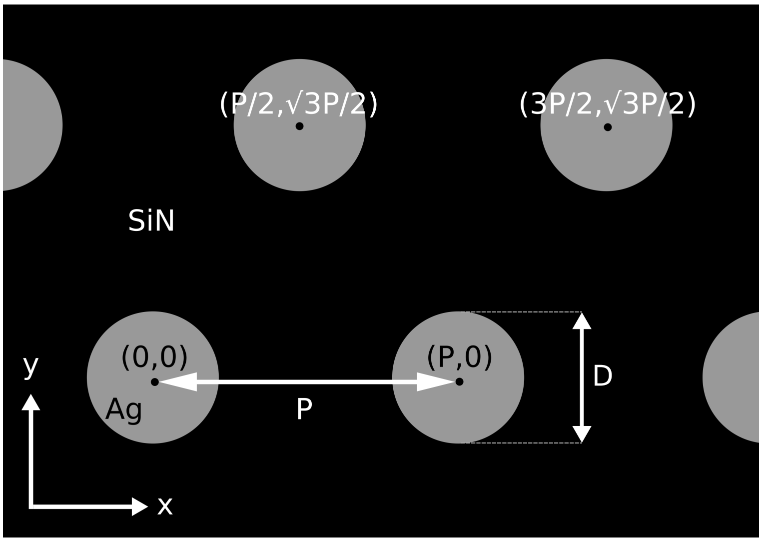


Fig. 4.2 Unit cell diagram of the DTL patterned hexagonal array, black areas are SiN, gray are Ag. Nominal array period, P, is 500 nm and nominal Ag pillar diameter, D, is 300 nm.

4.3 Device fabrication methods

4.3.1 Contact metalisation

N-type contacts were annealed Ni/AuGe/Ni/Au layered metalisation with thicknesses of 10/130/30/200 nm and anneal conditions of 20 seconds at 350°C. A eutectic mixture of AuGe was used (88:12 wt%) as this gives low contact resistance when the Ge diffuses into the GaAs layer upon melting. Ni layers above and below the AuGe as well as a thick Au layer over the top surface aim to reduce the changes in morphology that result from the AuGe melting as it is heated. Profilometry of the resulting contact showed a thickness of roughly 700 nm (including the 300 nm of n-type contact layer). P-type contacts were Ti/Au layered metalisation with thicknesses of 20/200 nm and no anneal due to the higher doping level of the p-type contact layer producing a non-annealed ohmic contact. See Section 3.5 for full discussion of metalisation and anneal conditions.

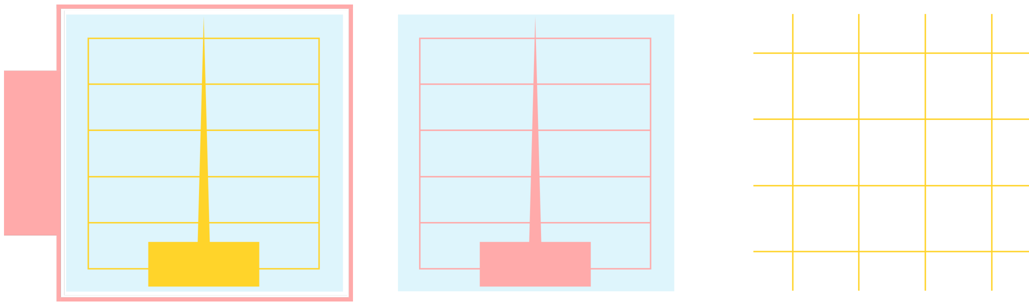
On-wafer devices were produced with a fully front-contacting scheme. All devices were 2.5 mm $\times$ 2.5 mm square in area (total area 0.0625 cm^2) with approximately 10% shading from the front contact grid. The majority of this area is the contact pad to make probing to the devices easier. The front grid fingers were used to reduce the series resistance losses due to lateral carrier movement before being collected at contacts. Figure 4.3 a) shows the on-wafer device contacting scheme.

Off-wafer devices were produced with a square grid n-type contact metalisation on the back of the cells with 3% coverage. The metals used for this ohmic contact have poor reflectivity and therefore were not evaporated onto 100% of the device back surface. Coverage was kept to a minimum to maximise the path length enhancements provided by the back surface mirror (in the planar case) and the metal-dielectric grating (in the DTL patterned case). This was balanced with the need to reduce series resistance in the devices that comes from lower levels of contact coverage [97]. Figure 4.3 b) shows the off-wafer front contact scheme and 4.3 c) shows the off-wafer back contact scheme.

The wafers from Table 3.4 were processed into three types of devices: on-wafer planar, off-wafer planar with Ag back reflector and off-wafer with integrated light-trapping layer. Their fabrication is detailed in the following three sections.

4.3.2 On-wafer planar devices

Figure 4.4 a) shows the processing steps for the on-wafer device type. Each step is explained below. In Figure 4.6 a) a chip with four on-wafer devices is shown to illustrate this fully-front contacting design. Etch mixtures and concentrations were adapted from [98].



(a) (b) (c)

Fig. 4.3 Contacting design for all three device types: a) fully front-contacting design for on-wafer devices b) front contacting design for off-wafer devices, c) back contact grid design for off-wafer devices. The blue regions indicate the 2.5 mm $\times$ 2.5 mm device area, pink regions indicate the p-type contacts and yellow regions indicate n-type contacts. Plot from [4].

1. 1 cm $\times$ 1 cm chips were cleaved from MBE grown 4" wafers. The layer structure design and optimisation is detailed in Chapter 3. Each chip was sonication cleaned in acetone for 30 seconds then rinsed in isopropyl alcohol.

2. A mesa photolithography and etch step was used to isolate the 2.5 mm $\times$ 2.5 mm device area. A positive S1813 resist was used to protect the mesa area during alternating dips in selective NH_4OH and HCl based etchants. First, a 2:1:10 ratio mixture of NH_4OH:H_2O_2:H_2O removed the 300 nm n-type GaAs contact layer at an etch rate of $\sim$17 nm/second. A 1:5 ratio mixture of HCl:H_2O removed the 20 nm InAlP layer at an etch rate of $\sim$1 nm/second. The 2:1:10 NH_4OH:H_2O_2:H_2O etchant then removed the 80 nm GaAs absorber layer. Finally a concentrated HCl dip rapidly removed the 20 nm InGaP layer. The p-type GaAs contact layer was left intact. The resist was then removed in acetone and the sample cleaned in isopropyl alcohol.

3. The front surface n-type annealed contact was deposited using a photolithography and lift-off method. AZ5214E image reversal resist was used for the lift-off and the metalisation is detailed in Section 4.3.1. A 30 second dip in 1:10 HCl:H_2O etchant was used to remove the native oxide layer before thermal evaporation of the contacts. After metalisation and lift-off, the chips were then annealed for 20 seconds at 350°C

4. The p-type non-annealed contact was then deposited in a square pattern around the edges of the mesa area using the same image reversal resist and native oxide removal process. The p-type contact also has a large contact pad area to the side for ease of probing as can be seen in Figure 4.4 a).

5. An inverted mesa photolithography and etch process was then used to protect the p-type GaAs contact layer around the edges of the device area while etching away the 300 nm n-type GaAs contact layer on the front surface using the 2:1:10 NH_4OH:H_2O_2:H_2O etchant. The image reversal AZ5214E resist was used for this process.

4.3.3 Off-wafer planar devices with Ag back reflector

Off-wafer planar devices with Ag back reflector were fabricated with the steps described below and visually represented in Figure 4.4 b). A photo of fabricated off-wafer planar devices is shown in Figure 4.6 b).

1. The 4" wafers were cleaned using acetone and an isopropyl alcohol rinse. A 30 second dip in 1:10 HCl:H_2O etchant was used to remove the native oxide layer before thermal evaporation of the contacts. A photolithography lift-off step using AZ5214E image reversal resist was used for the evaporated Ni/AuGe/Ni/Au n-type annealed contact. The n-type contact design is a square grid of 10 micron thick channels with 3% coverage. A 2:1:10 ratio mixture of NH_4OH:H_2O_2:H_2O was used to remove the 300 nm n-type GaAs contact layer areas not covered by metalisation at an etch rate of $\sim$17 nm/second.

2. A grid of 12 mm $\times$ 12 mm Ag squares were then evaporated onto the wafer using a shadow mask with square holes. 450 nm of Ag was deposited. Each Ag square was then cleaved from the wafer into an individual chip. The pattern of discrete 12 mm $\times$ 12 mm Ag squares was used instead of a continuous planar layer of Ag over the whole wafer because when etching back the GaAs growth substrate, if there is Ag at the edges of the chip, it will be attacked by the NH_4OH based etchant and destroy the chip. This was found to be a much more effective method for fabrication than attempting to protect the edges of the chip with another temporary material that is resistant to the etchant.

3. A high glassing temperature (T_g > 140°C) epoxy was used to bond the Ag coated chips to a Si carrier chip. The epoxy is OPT5054-4G two-part Opti-tec epoxy. The epoxy was chosen because of its low viscosity, 12 hour pot life, low shrinkage and because the glassing temperature is above that reached during photolithography steps that need to occur after the adhesive is used. The adhesive has a ratio of 100:85, resin to hardener and a mixed viscosity of 500 - 1000 cps. A cure was performed for 30 minutes at 120°C. After epoxy bonding, the growth substrate was etched back using a NH_4OH:H_2O_2 etchant at a ratio of 1:10. The chip was agitated continuously using

a pipette and rotated 90° at 5 minute intervals to aid the evenness of the etch. After 70-90 minutes in the etchant, some areas of the chip had etched down to the InAlP etch stop layer and bright red spots could be seen. Once a section of the InAlP was visible, the chip was transferred to a slower etchant with a 1:4:15 ratio of NH_4OH:H_2O_2:H_2O. The chip was further agitated in this etchant until all the GaAs islands were removed. The 150 nm InAlP layer was then removed with a dip in concentrated HCl. Ridges of epoxy that formed around the sides of the device chip were removed carefully with a razor at this stage to ensure that during subsequent photolithography steps contact between the surface of the chip and the mask could be achieved.

4. Front p-type Ti/Au contact metalisation was then evaporated onto the surface using the same AZ5214E image reversal photolithography lift-off method as the n-type metalisation. Before the mesa etch, the p-type contact layer was etched away using the same 2:1:10 NH_4OH based etchant as before at an etch rate of $\sim$17 nm/second.

5. Device areas were then isolated using a positive S1813 photoresist and mesa etch to produce 2.5 mm $\times$ 2.5 mm square devices. First, a concentrated HCl dip was used to remove the 20 nm InGaP layer. A 2:1:10 ratio mixture of NH_4OH:H_2O_2:H_2O removed the 80 nm GaAs absorber layer at an etch rate of $\sim$17 nm/second. Finally a concentrated HCl dip rapidly removed the 20 nm InAlP layer to expose the Ag layer which was electrically connected to the n-type contact metalisation. The resist was then removed in acetone and the sample cleaned in isopropyl alcohol. A grid of nine 2.5 mm $\times$ 2.5 mm devices were produced per chip.

4.3.4 Off-wafer devices with integrated light-trapping layer

The off-wafer DTL patterned devices were fabricated in the same way as the off-wafer with Ag back surface mirror devices in the section above except the DTL step was inserted between the n-type contact etch back and the Ag evaporation. The off-wafer DTL patterned device process is shown in Figure 4.5 and a photo of the resulting devices is shown in Figure 4.6 c). The DTL patterning (steps 2 to 6 in this section) was carried out over the entire 4" wafer by Pierre Chausse at the University of Bath.

1. The wafer was first metalised with the n-type contact in a grid structure over the whole wafer in the same way as for the off-wafer planar devices with Ag mirror. The 300 nm n-type GaAs contact layer was also etched away with a 2:1:10 ratio mixture of NH_4OH:H_2O_2:H_2O at a rate of $\sim$17 nm/second before the DTL patterning.

2. The metal-dielectric layer was fabricated by depositing an 100 nm nominal thickness layer of SiN with plasma-enhanced chemical vapour deposition. A bottom anti-reflection coating (BARC) was spin-coated over the wafer using a two-cycle process (5 seconds at 500 rpm then 30 seconds at 3000 rpm).

3. The wafer then had two baking steps (80°C for 60 seconds then 200°C for 90 seconds) to give a BARC thickness of approximately 250 nm. A PFI-88 positive resist was spin-coated on the BARC (same two-cycle process as above) then a bake at 90°C for 90 seconds. This resulted in a thickness of approximately 750 nm.

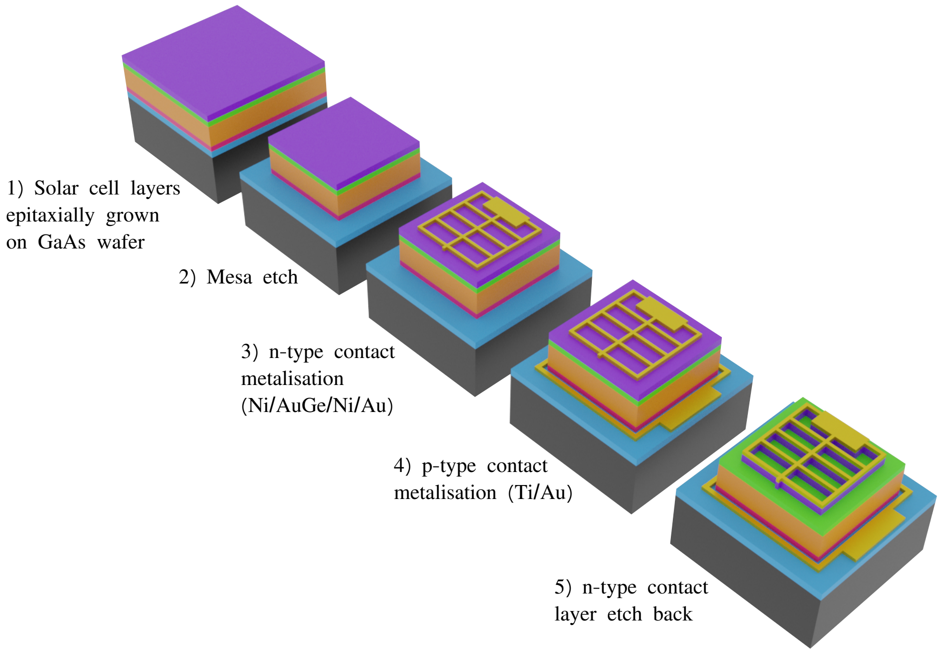
4. The resist was then exposed using a 375 nm laser and a DTL mask with a hexagonal array of openings with a pitch of 500 nm. A displacement of 20 Talbot periods was used during exposure (Talbot period of the mask was 750 nm) from an initial gap between mask and sample of approximately 100 microns. 55 mJ/cm^2 exposure dose was used.

5. Next was a post-bake for 90 seconds at 120°C and resist development with MF-CD-26 for 90 seconds. Etching was then done with an inductively coupled plasma (ICP) dry etch system for 550 seconds at 25 sccm CHF_3 with 300 W ICP power and with 50 W RIE power at 65 mTorr and 20°C.

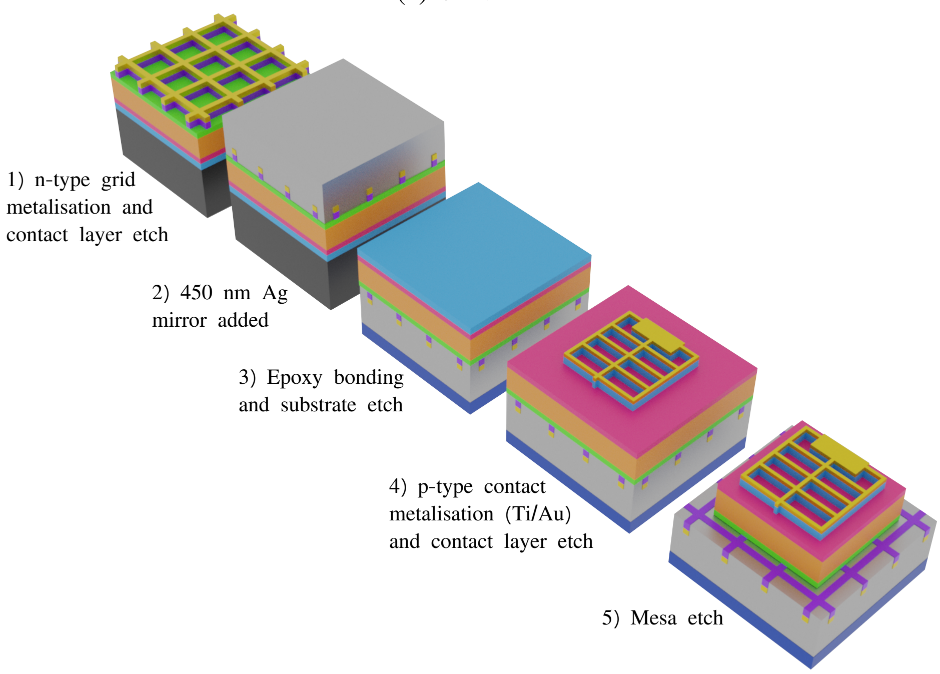
6. Remaining resist was removed by exposure to 375 nm laser at 2 mW/cm^2 power setting for 2 minutes. The exposed resist was developed and the wafer cleaned with acetone and isopropyl alchohol. A gentle O_2 plasma was used to remove the BARC.

Once the DTL patterned wafer was returned from our collaborators at the University of Bath, the Ag squares were evaporated and the processing proceeded in the same way as section 4.3.3 from point 2 onwards.

There was concern that the SiN being coated over the n-type contact grid metalisation would electrically isolate the grid from the Ag layer and therefore make it impossible to probe to the devices during testing. However, this was not an issue and electrical connection was achieved which indicates that sufficient amounts of Ag were able to electrically contact the n-type metalisation underneath through the holes etched in the SiN. This further shows the versatility of the DTL method in being able to pattern high quality features over an uneven surface with significant topography.



(a) On-wafer



(b) Off-wafer planar Ag

Fig. 4.4 Device fabrication methods for a) on-wafer device and b) off-wafer device with planar Ag mirror. Lengths not to scale.

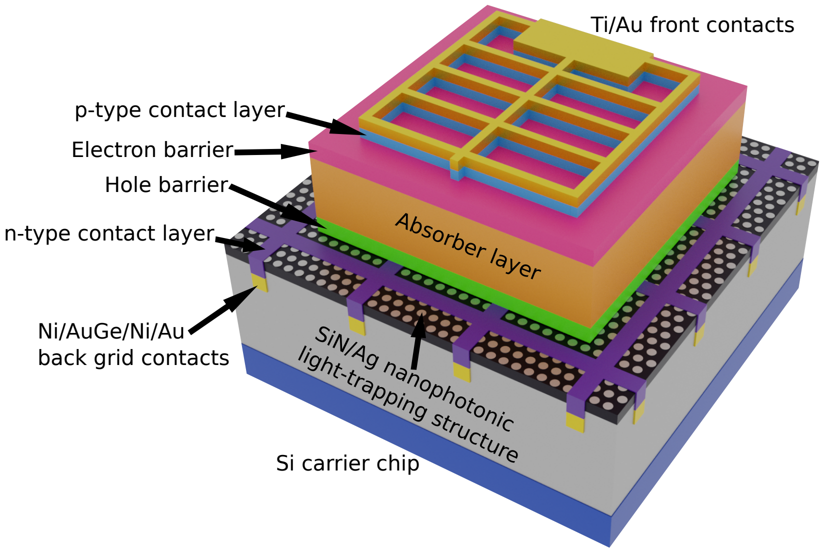
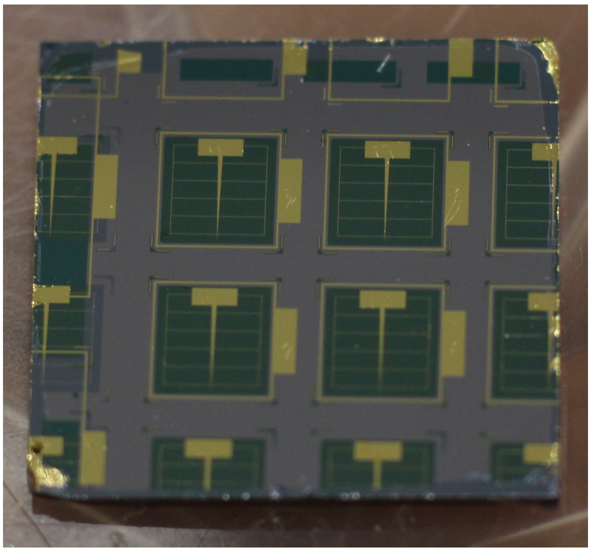
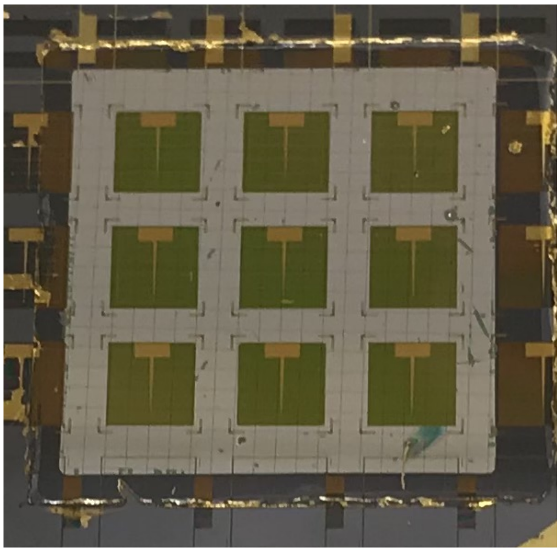
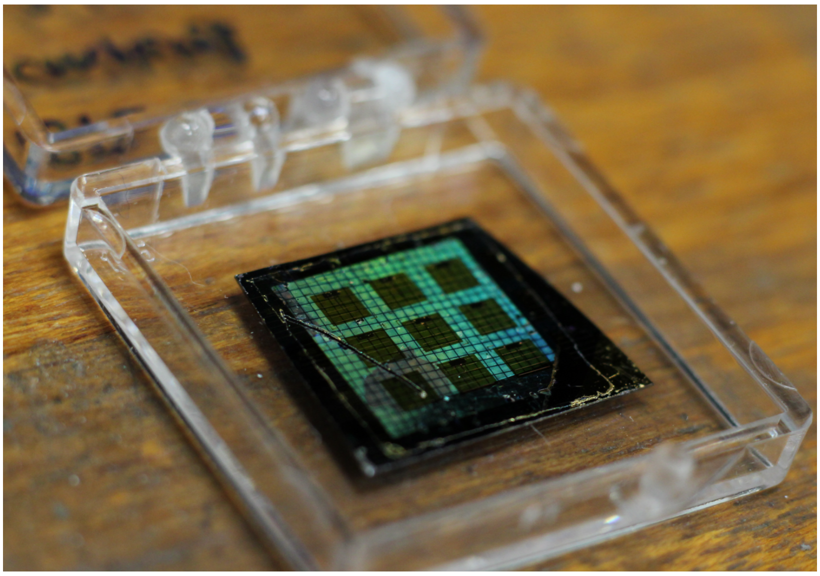


Fig. 4.5 Visualisation of off-wafer device with DTL patterned metal-dielectric grating structure. Lengths not to scale. Image from [4].

(a) (b)



(c)

Fig. 4.6 Photos of a) fabricated on-wafer devices, b) fabricated off-wafer planar Ag devices and c) fabricated off-wafer DTL patterned devices.

4.3.5 Analysis of the DTL grating

Scanning electron microscope (SEM) and atomic force microscopy (AFM) images were taken to assess the quality and uniformity of the SiN_x layer after DTL patterning. Figure 4.7 is a cross-sectional SEM image that shows the DTL patterned features and the good anisotropy in the etched holes. Further SEM images were used to look at the uniformity of the holes. A separate chip with a layer of SiN_x deposited by the same technique as the DTL layer was used to measure the optical constants of the SiN_x. Figure 4.8 shows the remarkable uniformity achieved during the DTL process over a full wafer.

Despite this uniformity, there are some fabrication issues that were identified. These deviations from the perfect simulated structure described in this section may reduce the diffraction efficiency properties of the nanophotonic structure. Figure 4.7 shows there are small domes of unetched SiN_x at the bottom of the holes. This SiN_x is potentially an issue as it could stop the Ag layer from coming into electrical contact with the n-type contact metalisation. It will also increase parasitic absorption and reduce the light-trapping potential of the structure. However, further etching to remove the domes was not attempted since there was a risk of etching into the 20 nm InAlP passivation layer underneath.

The walls of the etched holes also show some tapering and Figure 4.8 shows that some holes are not perfectly circular or are missing altogether. It is important to note that the cross-sectional SEM figure was taken after the SiN_x etch step but before the BARC was removed with a plasma etch. There was some residual BARC/etch residue left over after plasma etching visible on the surface and detected with AFM.

AFM measurements were taken on chips cleaved from the patterned wafer. These measurements confirmed the presence of the domes at the bottom of the etched holes. Etch depth was measured from the top of the domes to the SiN_x top surface. 125 holes were analysed giving an average hole depth of 80.5 $\pm$ 10.9 nm and an average hole diameter of 229 $\pm$ 24 nm.

4.4 Results

All three device types were characterised using LIV, DIV and EQE. The results and analysis of this characterisation are presented in this section.

4.4.1 Light IV

LIV was taken using a dual-source TS Space Systems Compact Solar Simulator using an AM0 spectrum. A water-cooled system maintained test temperature at 25°C. Figure 4.9 a) shows the LIV sweeps of the hero cells of each type. Table 4.1 shows the extracted LIV parameters for these devices.

The off-wafer device types show a significant increase in J_{SC} due to boosted longer wavelength light absorption because of increased optical path length. Off-wafer devices

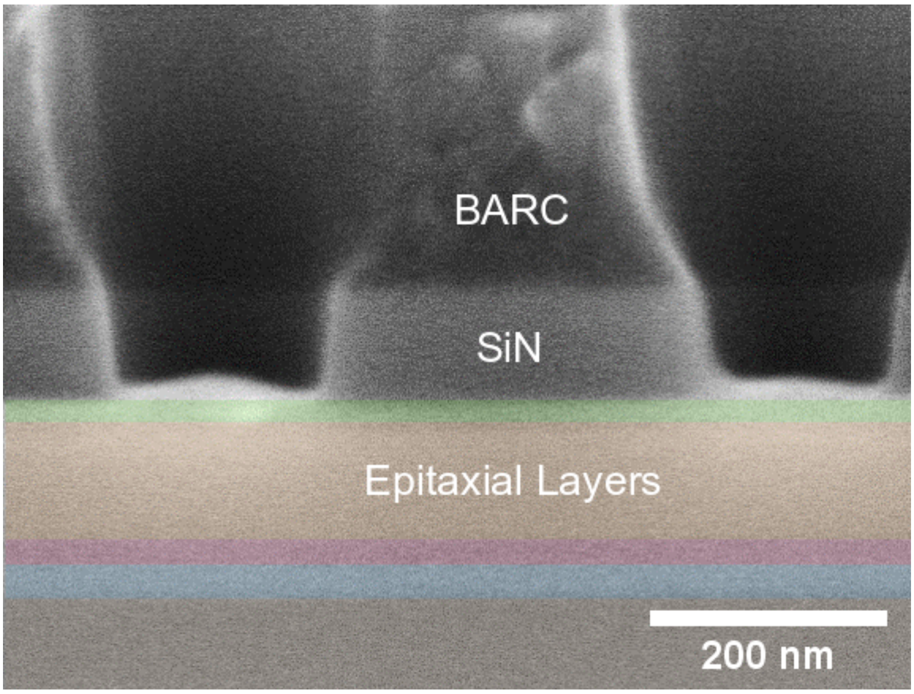


Fig. 4.7 Cross-sectional SEM image of DTL patterned SiN and the epitaxial layers of the solar cell. Image from [4].

Table 4.1 AM0 LIV results for best-performing cells of: on-wafer planar, off-wafer planar Ag and off-wafer DTL patterned.

	J_{SC} (mA/cm^2)	V_{OC} (V)	FF (%)	AM0 Efficiency (%)
On-wafer planar	10.05	0.928	78.41	5.40
Off-wafer planar Ag	15.33	1.010	79.22	9.06
Off-wafer DTL patterned	15.35	1.012	79.08	9.08

also show good V_{OC} values. This is in part due to the low bulk recombination loss property of solar-cells in the ultra-thin regime. Off-wafer devices also exhibit increased V_{OC} in comparison to the on-wafer embodiment. This increase is larger than that expected due to the improved J_{SC} and the superposition principle. For the DTL device, superposition accounts for 28 mV of V_{OC} increase so the remaining 56 mV above the value for the on-wafer device suggests a fundamental voltage enhancement due to light management.

4.4.2 EQE

External quantum efficiency (EQE) was taken on a Bentham PVE300 Quantum Efficiency testing apparatus. The setup includes a monochromatic source from dual xenon/quartz halogen lamps. The wavelength range that can be tested is 300-1800 nm. The ultra-thin

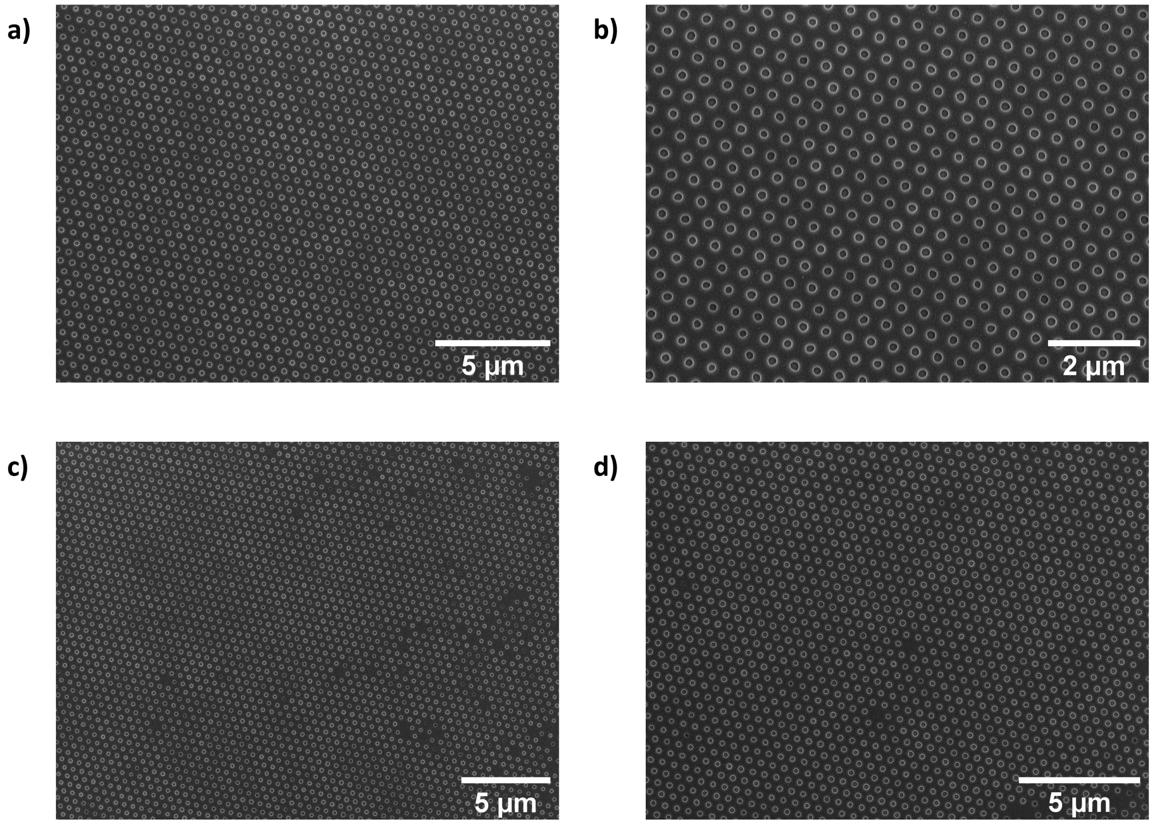
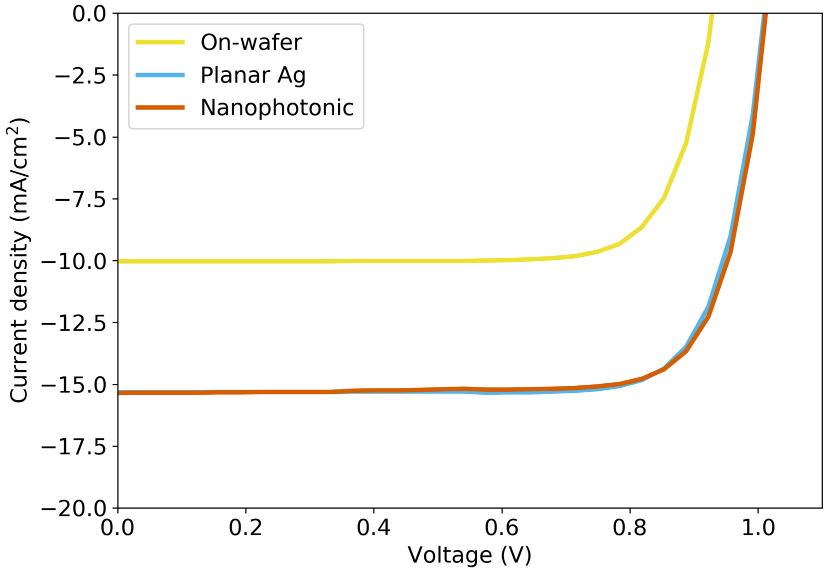


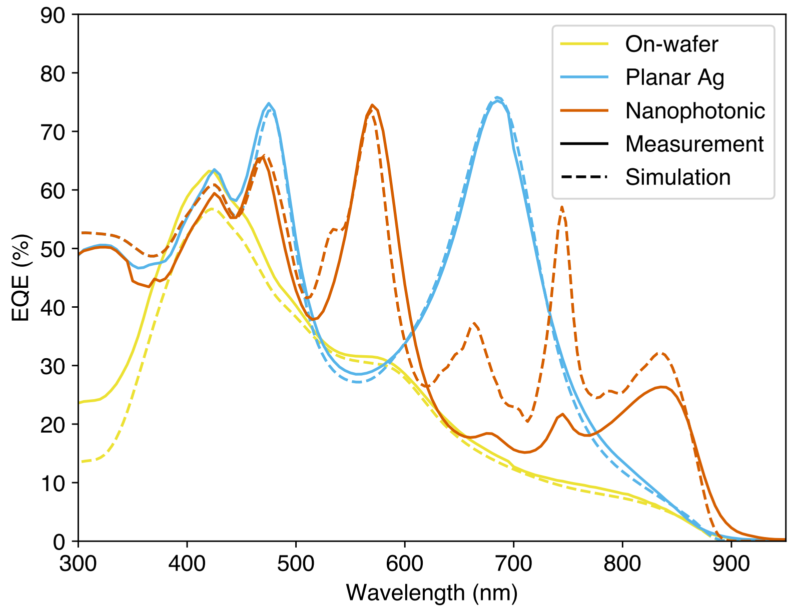
Fig. 4.8 SEM images of the DTL patterned SiN grating before the Ag layer was evaporated. Some defects can be seen in the hexagonal array of holes. Images from [4].

devices were tested from 300-1100 nm with a 5 nm step size in transformer mode. A 1.5 mm $\times$ 1.5 mm square aperture at the monochromator exit port was used which results in a 1.8 mm $\times$ 1.8 mm image of the square aperture on the plane of the device. The cross-over point between the two lamps was set at 700 nm due to the instability of the xenon lamp at longer wavelengths. A stationary scan at 555 nm was used to align the square spot in the centre of the device area before taking measurements.

Simulations of EQE were carried out by Phoebe Pearce using TMM and RCWA. Figure 4.9 b) shows the measured versus simulated EQE for each device type. EQE simulations are purely optical and calculate the fraction of photons absorbed at a given wavelength in the GaAs and InGaP layers of the device, assuming 100% carrier collection efficiency. TMM simulations were used for the on-wafer and off-wafer planar devices. Excellent agreement was found for the off-wafer planar with Ag mirror device as shown by the blue lines. This agreement is particularly good for the shorter wavelength regions. RCWA was used for the off-wafer DTL patterned device simulations.



(a)



(b)

Fig. 4.9 a) AM0 LIV results for hero cells of each of the three device types with 10% contact shading and no ARC. b) EQE measurements of the three device types compared to simulations. Plots from [4].

Long-wavelength regions of both the off-wafer device types show boosted absorption but different spectral features. The DTL device correlates qualitatively with simulation in terms of peak location but the magnitude of the peaks is much lower for the experimental result. This could be due to the differences between the idealised, simulated structure and the actual nanophotonic structure that was fabricated and analysed in Section 4.3.5.

4.4.3 Dark IV

DIV was taken with a Keithley 2401 SourceMeter in complete darkness. The 2-diode model [5] was fitted to the data to extract dark saturation currents, ideality factor and parasitic resistance values. The forward-bias region was used for the fittings. The first diode ideality factor, n_1, was held at 1 while the second diode ideality factor, n_2 was allowed to vary.

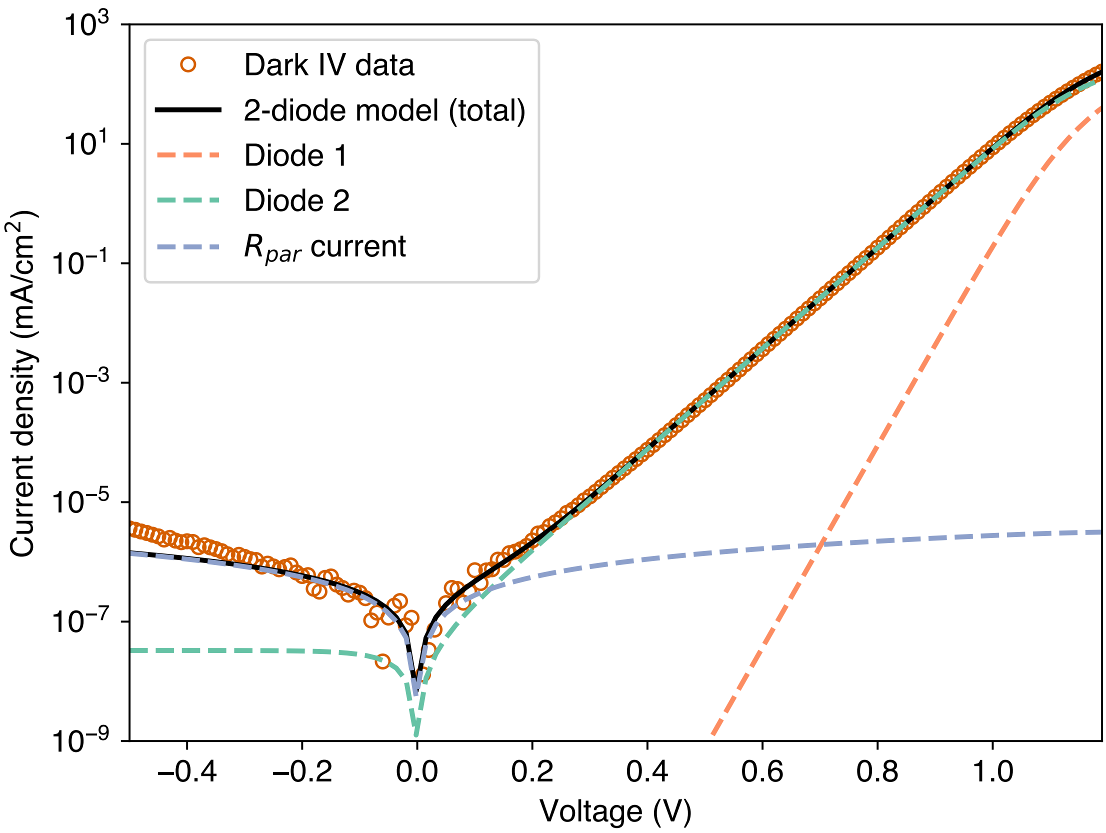


Fig. 4.10 Dark IV sweep of best-performing DTL device shown with 2-diode model fitting including the contributions of the diode terms and the shunt resistance [5]. Plot from [4].

Table 4.2 compares the extracted 2-diode model fitting parameters for the best performing DTL patterned cell to other single junction GaAs devices of different thicknesses in the literature. J_{02} values are of particular interest for ultra-thin devices as the depletion region accounts for a large portion of the total device thickness. J_{02} is a measure of the recombination in the depletion region and a low value indicates a high quality ultra-thin device. The J_{02} values of the cells in this work are comparable to cells with thicknesses that are orders of magnitude larger. In terms of parasitic resistances the DTL hero device also displays good performance and similar values to the literature. This work is therefore an improvement on previous 80 nm devices in terms of diode quality.

Table 4.2 2-diode model parameters extracted from hero DTL device and comparison to other ultra-thin cells in the literature, *n_2 was constant for these devices.

	Thickness						
	Total (nm)	Absorber (nm)	J_{01} (mA/cm^2)	J_{02} (mA/cm^2)	n_2	R_{ser} (Ωcm^2)	R_{par} (Ωcm^2)
Kayes [34]	1000	-	6×10^{-18}	1×10^{-9}	2*	-	-
Chen [36]	330	205	2.8×10^{-17}	4.3×10^{-8}	2*	0.8	2.4×10^{3}
Hirst [6]	840	800	2.48×10^{-19}	7.71×10^{-9}	1.96	0.99	8.94×10^{7}
	120	80	1.74×10^{-18}	1.41×10^{-6}	2.70	13.23	3.77×10^{6}
This work [4]	120	80	2.67×10^{-18}	3.29×10^{-8}	2.01	2.01	3.60×10^{8}

4.4.4 Optical analysis

The contribution of two main effects are considered. These are Fabry-Perot resonances (thin film effects) and waveguide modes. Fabry-Perot resonances are due to specularly reflected light. Waveguide modes are due to constructive interference of waves in the active layers that are confined within the device rather than escaping through the front or rear surfaces. For the off-wafer planar devices, Fabry-Perot is the optical effect that can be seen in the EQE data. For the off-wafer DTL patterned devices, both waveguide modes and Fabry-Perot resonances are present (Figure 4.11).

4.5 Discussion and future improvements

The on-wafer device EQE shows a peak in absorption at about 450 nm and a decrease in EQE at longer wavelength due to transmission losses. Long wavelength EQE is improved for both of the off-wafer designs. The best performing cell was one of the DTL patterned devices. However, the best planar Ag cell showed an almost identical performance with just 0.02% difference between them in terms of efficiency. The short circuit current values for these two devices are very similar but their EQE results show very different peaks over the spectrum. This demonstrates that integration of nanophotonic structures will not

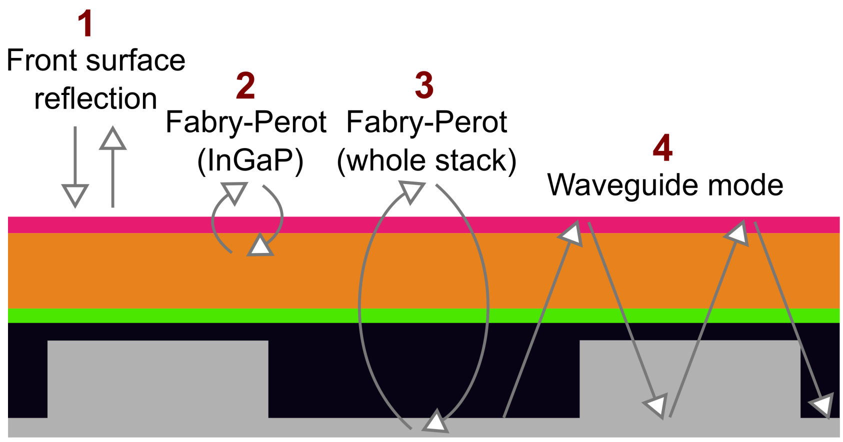
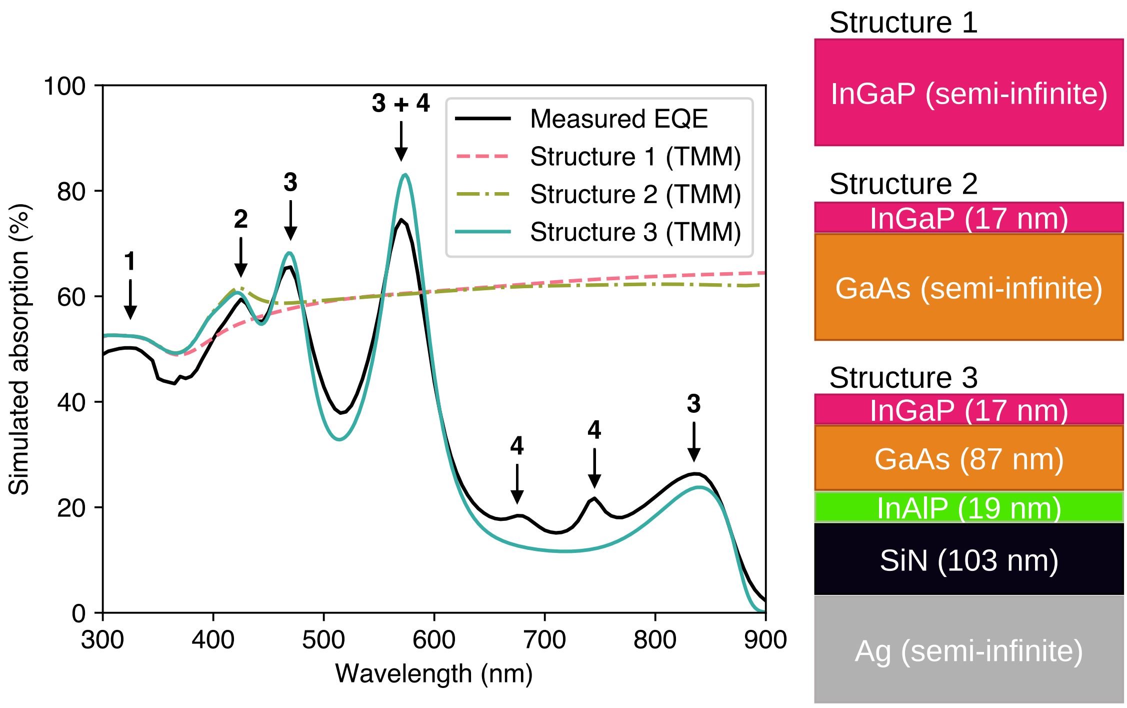


Fig. 4.11 Diagram of the different interactions of light with DTL patterned off-wafer devices. (1) Reflection at the air to front surface interface, (2) Fabry-Perot modes from the front surface InGaP passivation layer, (3) Fabry-Perot modes of the complete layer stack and (4) Waveguide modes that increase total internal reflection. Plot from [4] and courtesy of Eduardo Camarillo Abad.



(a) (b)

Fig. 4.12 a) Measured EQE plotted alongside TMM EQE simulations of three different planar structures. b) Diagram of the three structures used in TMM simulations. Plots from [4] and courtesy of Phoebe Pearce.

always provide efficiency enhancement over planar devices. The metal/dielectric gratings can introduce parasitic absorption and therefore the benefits of diffraction must overcome this effect to yield an efficiency benefit.

4.5.1 Passivation layer analysis

As explained in Chapter 3, a 20 nm InGaP layer was chosen as the front surface passivation layer for the off-wafer devices. It serves as the back surface passivation layer for the on-wafer embodiment since the layer structure is inverted. The on-wafer devices, with InAlP as the front surface passivation layer, exhibited a relative suppression of the EQE at short wavelengths when compared to off-wafer designs. This indicates that photons with energy above the direct bandgap threshold were absorbed in the InAlP layer but not collected.

InGaP was chosen for its favorable band alignment. It is often overlooked as a potential electron blocking layer due to it being a direct-bandgap semiconductor, and therefore positioning it on the front surface could result in parasitic absorption. Other authors including Chen et al. [36] have opted for an AlGaAs front surface passivation layer as an alternative. However, it was found in this study that the InGaP makes an optimal blocking layer with near ideal passivation of the surface. Furthermore, all charge carriers produced in the InGaP are collected as current. Figure 4.13 shows the simulated absorption in each of the three active layers of a planar off-wafer device. This absorption is plotted with the experimentally measured EQE and shows the significant contribution of the InGaP front surface passivation layer to the good device performance in the off-wafer embodiment.

4.5.2 Epoxy bonding

The epoxy used for the off-wafer devices is rated to have a glassing temperature above 140°C which is sufficient for the heating required in photolithography steps taken after the bonding is complete (e.g. front contact metalisation lift-off lithography). The epoxy was carefully mixed and coated onto a Si carrier chip that was larger than the area of the device chip. The device chip was then placed on top with the Ag surface facing down and the epoxy wicked to the Ag surface with light downward pressure from a pair of tweezers.

The two-part epoxy was prone to developing bubbles during mixing that would leave voids underneath the devices after bonding. However if the epoxy was left to outgas in air, the resulting devices showed degraded V_{OC} values potentially due to strain introduced by the hardened epoxy.

Different amounts of epoxy were used to investigate how allowing the epoxy to wick to the vertical sides of the device chip may help protect the device area from lateral etching and

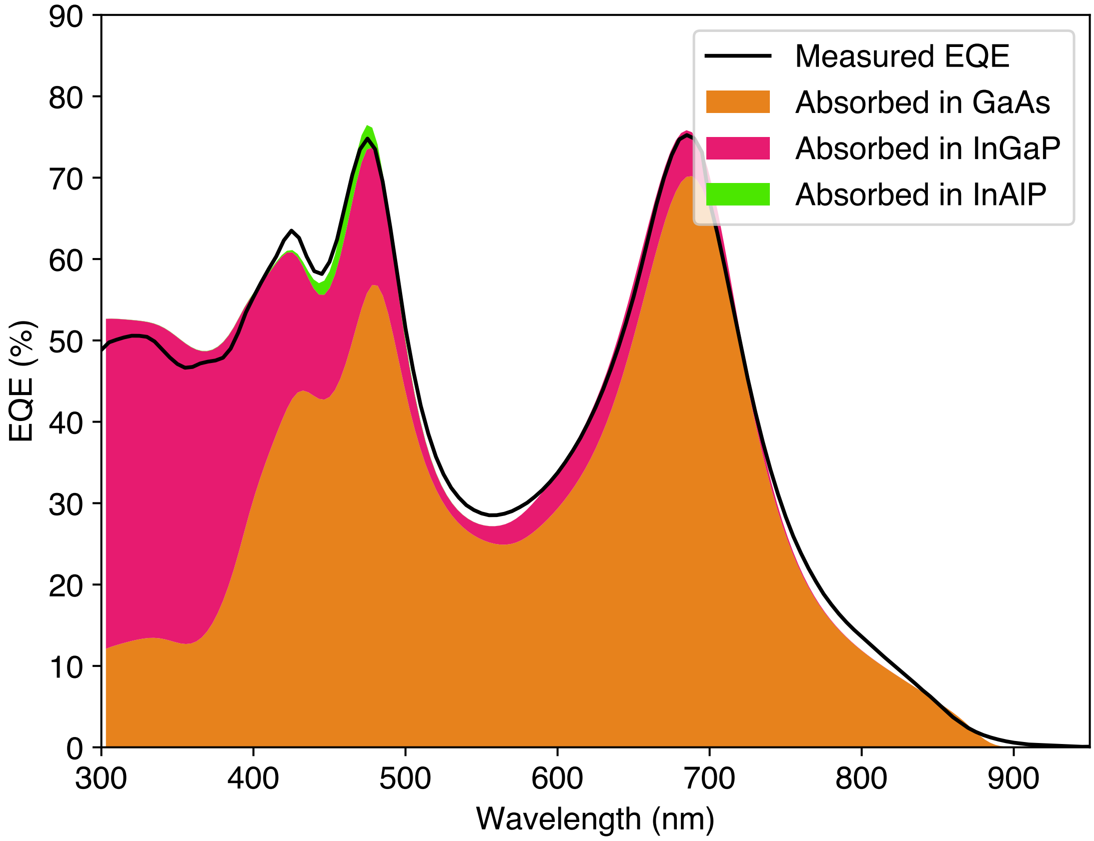


Fig. 4.13 Simulated absorption in each of the three active layers of a planar Ag device compared to measured EQE. Plot from [4] and courtesy of Phoebe Pearce.

also allow an easier removal of any epoxy ridges. These ridges need to be removed to allow for subsequent photolithography steps that require full contact between sample and mask. Figure 4.14 shows a failed substrate etch back likely due to strain introduced in the device chip due to the epoxy. As the substrate was etched away it became more fragile and reached a point where the thin layer began cracking. The smaller square area within the Si carrier chip is approximately 12 mm $\times$ 12 mm.

Epoxy bonding was also chosen for the lifted-off devices as there is significant topography from the n-type contact layer and n-type contact metalisation. Profilometry showed ridges of about 700-800 nm in height on the Ag surface. The epoxy is able to fill in and planarise this ridged surface for bonding to the Si carrier chip. The topography from the n-type contact structure would likely produce voids in other non-adhesive bonding methods such as anodic bonding. Other adhesive bonded ultra-thin GaAs devices have shown promising performance such as [36, 93, 43]. These studies used SU-8 and OrmoStamp which have shown good results as bonding mediums. Vandamme et al. [40] produced planar cells with an Ag back mirror using a UV reticulated polymer adhesive but also struggled with achieving good V_{OC} values which may be related to the effect of the bonding and/or different passivation layer choices.

Using a thicker Ag layer or moving towards an electroplating method to achieve µm scale layers of Ag could potentially improve the issue of the epoxy causing strain in the active layers of the device. Ideally a method should be designed that does not include the use of an adhesive bonding medium since there is a difference in thermal properties between the adhesive and the solar cell layers that can lead to degradation during the solar cell's lifetime. Future improvements to these devices will be focused on a bonding method that is repeatable, robust and can withstand the conditions of space that these devices are intended for (radiation tolerance, heat cycling etc.).

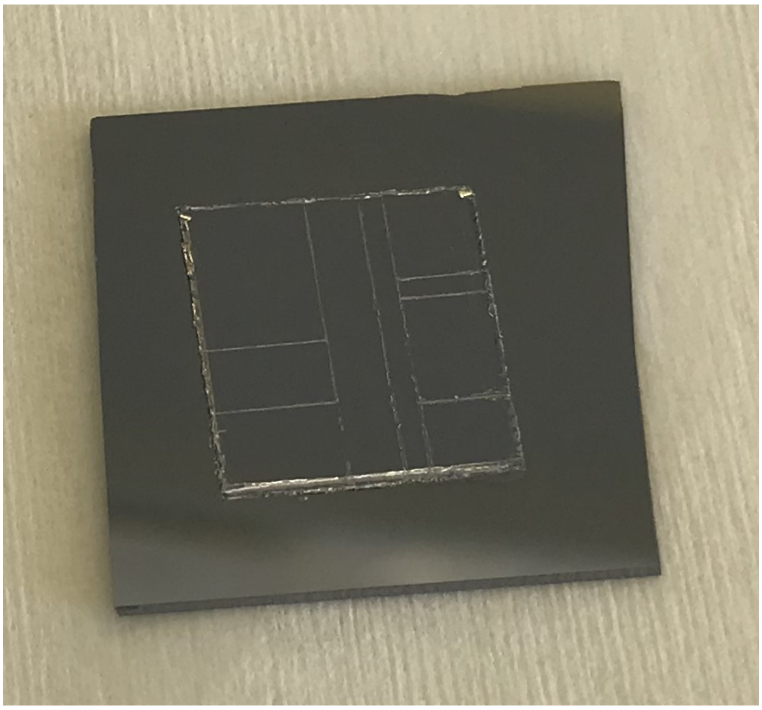


Fig. 4.14 Photo of Si carrier chip with device chip epoxy bonded on top after a failed substrate etch back due to strain-induced cracking.

4.5.3 Growth substrate etch back

Spacing between each device was kept to a minimum in order to decrease the size of the chip. This increased yield of devices from each wafer and improved the uniformity of the substrate etch back. The larger the chip the more difficult it is to isotropically etch through the 625 µm growth substrate. Thinner growth wafers or mechanically grinding away part of the thickness would significantly improve this issue. Epitaxial lift-off (ELO) techniques [99] to allow the re-use of wafers were not applied in this case but are essential for the future of ultra-thin devices in order to take advantage of the materials savings when thinning the absorber layer thickness [100].

The growth substrate was also 625 µm thick which meant that the substrate etch back required an extended period of time in the etchant and the resulting etch was not uniform across the approximately 12 mm $\times$ 12 mm area of the chip. Certain areas would etch down to the InAlP etch stop layer while other areas still had GaAs islands on them which ran the risk of puncturing through the InAlP layer to the active layers and ruining the chip.

Chapter 5

Radiation tolerance of ultra-thin GaAs solar cells

5.1 Introduction

In this chapter, the results of radiation damage testing of 80 nm ultra-thin GaAs solar cells are presented. The devices analysed have the same layer structure as designed and optimised in Chapter 3. The ultra-thin devices were exposed to proton beams at two different energy levels: 68 and 3 MeV at a range of fluences. Higher energy (68 MeV) protons are of interest as they are less well studied and are more abundant in orbits of interest including highly elliptical Earth orbits and orbits around Jupiter. Lower energy (3 MeV) protons are more widely studied and therefore useful for literature comparison. They are also more damaging.

Felix Lang carried out the 68 MeV proton irradiations at the Helmholtz-Zentrum Berlin as well as pre and post irradiation 1-sun AM0 LIV characterisation and in-situ current measurements. We acknowledge the support of The University of Manchester's Dalton Cumbrian Facility (DCF), a partner in the National Nuclear User Facility, the EPSRC UK National Ion Beam Centre and the Henry Royce Institute. Armin Barthel and Carl Andrews carried out the first two sessions (there were three in total) of 3 MeV proton irradiations at DCF. Armin also produced Figure 5.17. Carl Andrews of DCF operated the irradiating system for all three sets of 3 MeV exposures. The main results of this chapter have been published in two conference proceedings [101, 102] and a journal article titled *"Radiation effects in ultra-thin GaAs solar cells"* [10].

5.1.1 Satellite missions

Many aspects of today's society depend on services facilitated by satellite technologies. The satellite industry is predicted to expand further and continue to be important in many industries such as communications, defense and climate monitoring [13, 103]. As more satellites are launched, strategically advantageous and low radiation orbits such as low Earth orbit (LEO) will become increasingly cluttered [104]. Therefore, different orbits such as middle Earth orbits (MEO) and highly elliptical orbits (HEO) will be looked at due to their availability and also the specific benefits they can provide. As the altitude is increased the number of satellites needed for complete coverage of a region is reduced which makes MEOs an attractive option. HEOs are necessary for coverage of high latitude locations e.g. Northern Canada, Russia and the polar regions [9]. However, these orbits pass through the Earth's Van Allen belts and are therefore exposed to high levels of damaging radiation. Radiation tolerant power systems will therefore be needed to exploit these orbits [105].

The radiation that satellites encounter outside of the Earth's atmosphere is mostly in the form of high energy protons and electrons. SPace ENVironment Information System (SPENVIS) is an online tool, developed by the European Space Agency, that is used in this thesis for modelling and visualising orbits and the levels of damaging radiation present [77]. SPENVIS can be used to model Earth orbits as well as Martian and Jovian environments.

Improving the radiation tolerance of space PV could enable missions beyond Earth's orbits. Europa, one of Jupiter's moons, is considered a good candidate for the discovery of extra-terrestrial life [106]. It potentially has organisms living beneath the surface of its icy oceans [107]. One major issue with testing this theory is the extreme radiation environment of Europa. Any spacecraft deployed to the surface of Europa will need to withstand bombardment from high energy protons and electrons for long enough to collect and analyse samples and transmit data back to Earth.

Space-based solar power (SBSP) is another potential application of radiation tolerant solar cells. These solar arrays would be deployed to produce power that is then beamed down to the surface of Earth for terrestrial use [108]. Extending their lifetime would help make SBSP projects more cost effective and reduce the need for replacing modules and covering them with thick protective glass sheets.

5.1.2 Protecting satellite solar arrays from damaging radiation

Satellite electronics can often be shielded from radiation by thick layers of metal such as the Juno Radiation Vault [109]. The materials of the solar panels, however, cannot be covered with opaque materials as they need to absorb sunlight and produce electricity. The use of transparent coverglass is therefore necessary to protect solar arrays that are susceptible to radiation-induced damage. Currently all spacecraft that use solar energy have needed some rigid protective shielding in order to carry out their missions. Typically, borosilicate based glass with good transparency in the 350–1250 nm range is used [110].

The integration of space-worthy coverglass is effective in extending the lifetime of a satellite's power system. This coverglass attenuates lower energy protons and electrons which cause the most damage. However, the added weight of the coverglass increases launch costs and eliminates the possibility of flexible form factors for the panels. Some progress has been made towards flexible solar arrays by designing hinges between the individual rigid cells so the array can be "rolled up" and stored more compactly during launch [27]. This is only a partial solution however as the solar cells themselves are still rigid and the hinging adds complexity, mass and more potential mission failure points. Achieving truly flexible solar arrays would be a huge advancement for the space power industry as it could greatly reduce stowed volume of the solar arrays during launch of the spacecraft.

5.2 Radiation tolerance testing of solar cells

In order to test the resilience of solar cells in space conditions before launching them into orbit, fabricated devices are exposed to increasing fluences of damaging radiation [111]. These irradiations are carried out with unidirectional beams at a single energy level. The devices are characterised before and after each exposure to determine their degradation profile. In this way the BOL and EOL performances of different solar cell types can be compared. While on orbit, actual space solar arrays would be exposed to protons and electrons at a range of energies and angles of incidence. The damage induced in crystalline semiconductors by irradiation is dependent on particle flux, kinetic energy, species and angle of incidence. The displacement threshold energy for a compound material like GaAs is dependent on the lattice direction so there may be some difference in radiation effects between proton beams at normal incidence and the proton irradiation on-orbit at a range of incident angles. This angle dependence is assumed to be negligible in this study. The DDD method, as explained in section 2.6.4, is used to directly compare the degradation results of solar cells that have been exposed to ions at different energy levels. The method can also be used to extrapolate damage data to actual orbital conditions and therefore predict how long a specific solar cell type will survive on orbit.

5.2.1 Semiconductor materials for space applications

High energy protons and electrons incident on a solar cell can cause atomic dislocations such as interstitials and vacancies in the lattice structure of the active layers. These dislocations can act as recombination centres for carriers and therefore reduce the maximum output power of the solar array. Defect formation in GaAs has been studied extensively in the literature [63, 65]. Early solar-powered satellites used Si arrays to provide electricity but this has since been replaced with high-efficiency III-V multi-junction cells for many applications that provide better performance. III-V compounds such as GaAs have shown increased radiation tolerance when compared to Si [112, 113].

5.2.2 Cell degradation parameters

As the fluence of damaging radiation incident on a solar cell is increased, more and more defects in the lattice structure are formed. The effects of these defects on device performance can be investigated by characterising solar cell performance before and after exposures. The performance parameter of particular interest for the ultra-thin solar cell design is the short circuit current J_{SC}, as explained in Section 2.6.2. The degradation profile of other performance parameters such as V_{OC}, FF, P_{max} and J_{02} are also used to compare ultra-thin cells to thicker, more traditional devices.

5.2.3 Effects of radiation damage in ultra-thin solar cells

Ultra-thin solar cells have shown high tolerance to damaging radiation with no degradation in short circuit current up to extremely high fluences [6]. A potential explanation for this phenomenon is that the length scale of the device is very small and hence carrier lifetimes remain long enough for carriers to be collected at the contacts before recombining, even after defects have been introduced. In contrast to the short circuit current, the open circuit voltage and fill factors degrade similarly to thicker cells as defects are introduced. The combination of these effects means that the P_{max} remaining factor for the ultra-thin regime exceeds thicker cells and at extremely high fluences even shows better absolute performance [6].

5.3 68 MeV proton irradiations of ultra-thin GaAs solar cells

Depending on the specific orbit that a satellite is using, the radiation environment can be very different. Some orbits such as HEOs and Europa have higher components of high energy proton radiation (see Figure 5.16). While lower energy particles are more damaging to solar cells than higher energies, the higher energies are less well studied. Lower energy particles are also more readily blocked by thin layers of coverglass. For these reasons, 68 MeV protons were chosen to investigate the radiation tolerance of ultra-thin solar cells.

The devices used for these irradiations are on-wafer planar cells with the layer structure detailed in Table 3.4 and absorber layer doping of 1×10^{18} cm^{-3}. All devices are 2.5 $\times$ 2.5 mm square areas fabricated with the same procedure as described in Section 4.3.2. Devices have 10% front contact shading and no ARC.

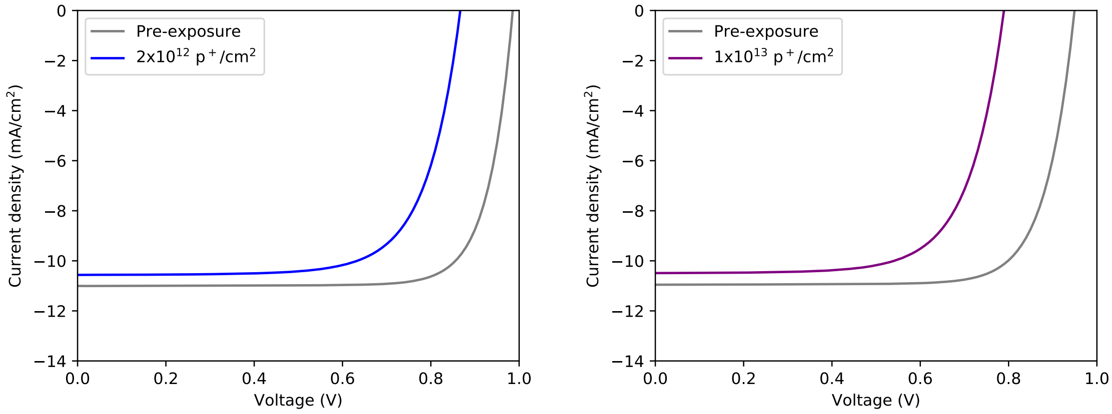
5.3.1 Irradiation procedure

Two on-wafer devices with 1×10^{18} cm^{-3} absorber layer doping and the layer structure shown in Table 3.4 were irradiated with 68 MeV protons at two different fluences. Irradiations were carried out on the two devices during the same one-day session. Samples were wire bonded to allow for in situ measurements. They were characterised before and after irradiation using a Keithley source meter for dark IV and an AM0 solar simulator for light IV. Target fluences were 2×10^{12} p$^+$/cm^2 and 1×10^{13} p$^+$/cm^2. Actual measured fluences were 1.994×10^{12} p$^+$/cm^2 and 9.951×10^{12} p$^+$/cm^2.

The irradiations were carried out at the tandetron-cyclotron combination of the Helmholtz-Zentrum Berlin which provided a highly stable irradiation at a proton energy of 68 ± 1 MeV. A thin scattering foil and aperture masks were used to ensure a uniform irradiation over an area of 2.56 cm^2. Beam intensity was monitored online using a transmission ionization chamber.

5.3.2 Results

Devices were characterised using LIV, DIV and EQE. Figure 5.1 shows the undamaged and post-irradiation AM0 LIV results. The LIV results are also summarised in Table 5.1 with remaining factors for each quantity and fluence. The open circuit voltage and maximum power degrade significantly after each of the irradiations. As in a previous study on ultra-thin solar cell radiation tolerance, the short circuit current does not degrade in the same way as other parameters. 96% of pre-exposure current is maintained at each of the fluences tested which shows that ultra-thin cells maintain their excellent radiation tolerance for these high energy protons at these fluences.



(a) (b)

Fig. 5.1 1-sun AM0 light IV experimental results for on-wafer devices pre-exposure, after exposure to 2×10^{12} and 1×10^{13} p^+/cm^2 fluences of 68 MeV protons.

Table 5.1 1-sun AM0 light IV performance parameters before and after on-wafer device irradiations with 68 MeV protons at two different fluences. RF is the remaining factor for each quantity.

Fluence (p^+/cm^2)	J_{SC} (mA/cm^2)	J_{SC} RF	V_{OC} (V)	V_{OC} RF	P_{max} (mW/cm^2)	P_{max} RF	FF (%)	FF RF
Pre-exposure	11.00	-	0.985	-	8.61	-	79.51	-
2×10^{12}	10.56	0.96	0.867	0.88	6.54	0.76	71.72	0.90
Pre-exposure	10.96	-	0.949	-	8.00	-	76.85	-
1×10^{13}	10.49	0.96	0.789	0.83	5.74	0.72	70.26	0.91

Figure 5.2 shows the normalised in-situ current taken during an irradiation of one of the ultra-thin on-wafer devices and a commercially available III-V triple-junction cell (3G28C, Azur Space) [114]. Both devices show degradation as the fluence is increased with the ultra-thin cell showing slightly better remaining factor at the target fluence of 1×10^{13} p^+/cm^2. Radiation induced current analysis does not give a complete picture of the performance of the cell as the mechanism of current generation is not due to photons but it does show similar degradation profiles for the two device types.

While this in-situ data implies that the ultra-thin cell is not performing significantly better than the triple-junction cell, there could be multiple explanations for this. These include

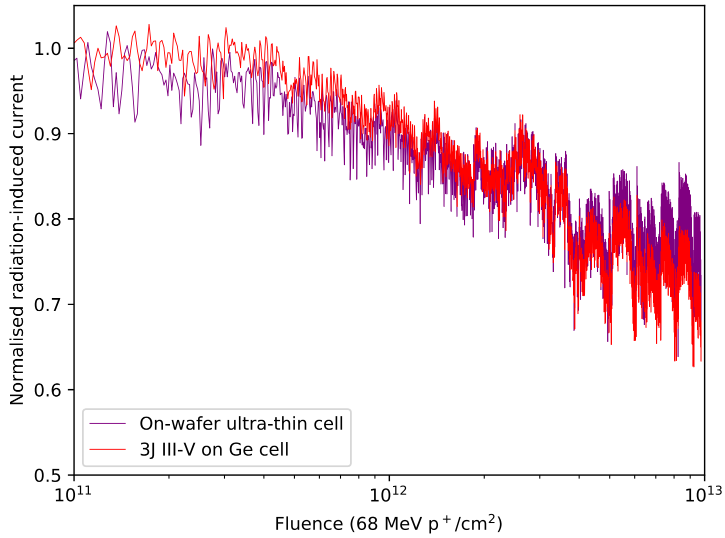


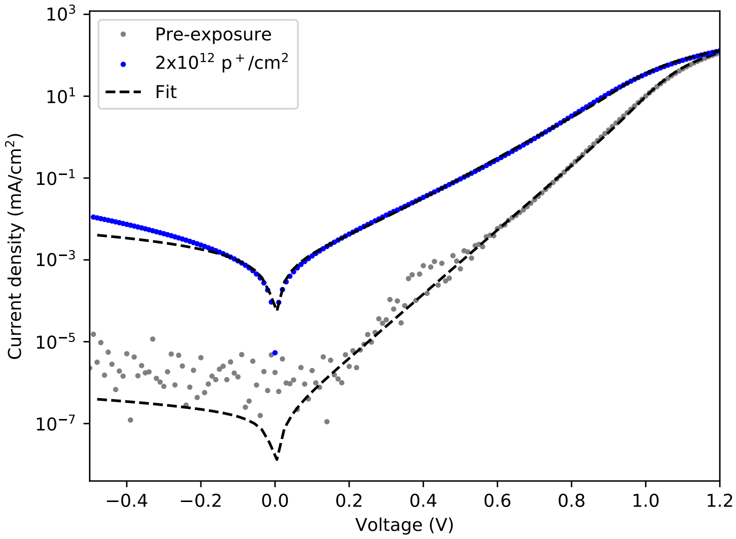
Fig. 5.2 Normalised in-situ radiation-induced current for 3J III-V on Ge (3G28C, Azur Space) and on-wafer ultra-thin cells. In-situ data collection was carried out by Felix Lang.

that the Azur cell has radiation resistant InGaP as its top cell. Another explanation could be that the displacement damage is still low for these high energy protons so the Azur cell remains current matched which means the sensitive GaAs middle cell never acts as the current limiting component.

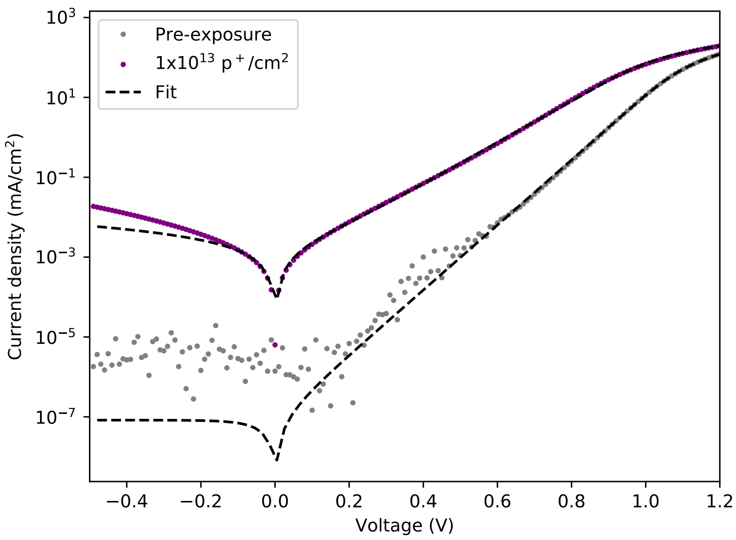
Figure 5.3 shows the DIV results for undamaged and post-irradiation ultra-thin devices. Pre-exposure data appears noisy in the low current regions due to the current values being smaller than the sensitivity of the measurement equipment. 2-diode model fitting can still be carried out on the data and was used to extract DIV parameters and analyse degradation. These values are presented in Table 5.2.

Table 5.2 2-diode model fitting results [5] for on-wafer ultra-thin devices before and after 68 MeV proton irradiations at two different fluences. n_1 was held constant at 1 and the forward bias region of dark IV data was used for fitting.

Fluence (p^+/cm^2)	J_{01} (mA/cm^2)	J_{02} (mA/cm^2)	n_2	R_{ser} (Ωcm^2)	R_{par} (Ωcm^2)
Pre-exposure	7.17×10^{-20}	1.05×10^{-10}	2.15	1.11	1.67×10^{9}
2×10^{12}	2.77×10^{-15}	2.77×10^{-4}	3.33	1.69	1.28×10^{5}
Pre-exposure	3.65×10^{-17}	8.26×10^{-8}	2.08	0.98	3.30×10^{13}
1×10^{13}	1.76×10^{-14}	4.86×10^{-4}	3.18	1.31	8.99×10^{4}



(a)

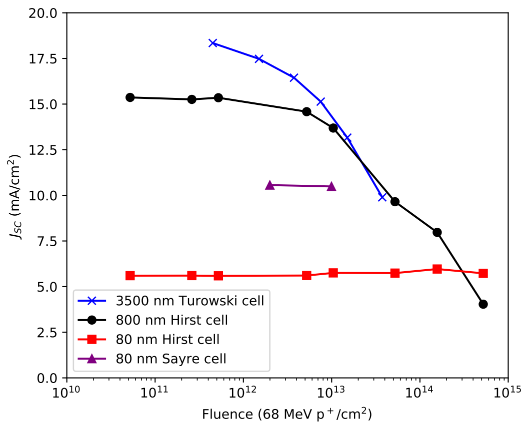


(b)

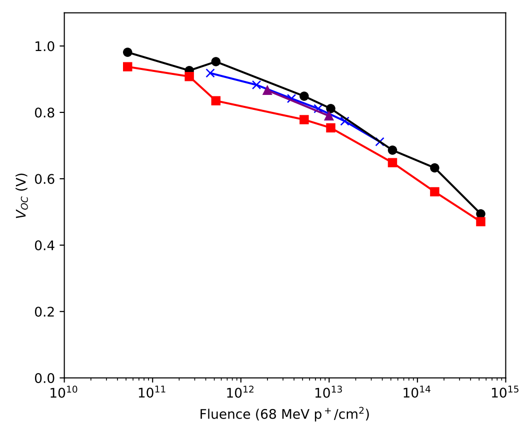
Fig. 5.3 Experimental DIV results for on-wafer devices pre-exposure, after exposure to 2×10^{12} and 1×10^{13} p^+/cm^2 fluences of 68 MeV protons. Dashed lines show the results of 2-diode model fitting [5].

In ultra-thin devices, the depletion region makes up a large portion of the overall thickness. This means the J_{02} term, which is a measure of recombination in the depletion region, dominates over J_{01}. As fluence is increased, the J_{02} term also increases since defects are being introduced into the depletion region that increase this reverse saturation current.

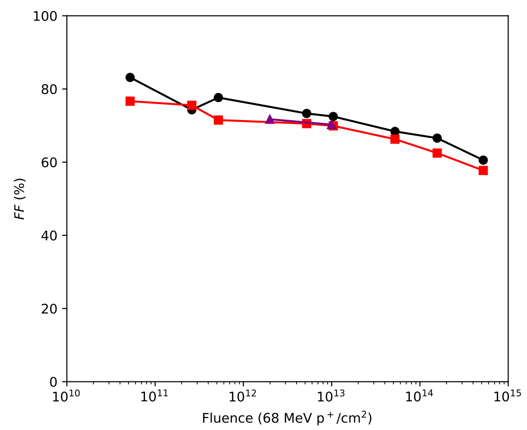
Figure 5.4 shows the performance parameters of irradiated devices plotted against 68 MeV equivalent fluence. All devices are single junction GaAs solar cells irradiated with high energy protons. These plots provide comparison of radiation tolerance and overall device performance with data from literature, for three different length scales: 80 nm, 800 nm and 3500 nm. See Appendix A for details of the equivalent fluence calculation that was used to scale the other device degradation data using DDD and NIEL. Other device degradation data was taken with 2 MeV [7] and 3 MeV [6] protons.



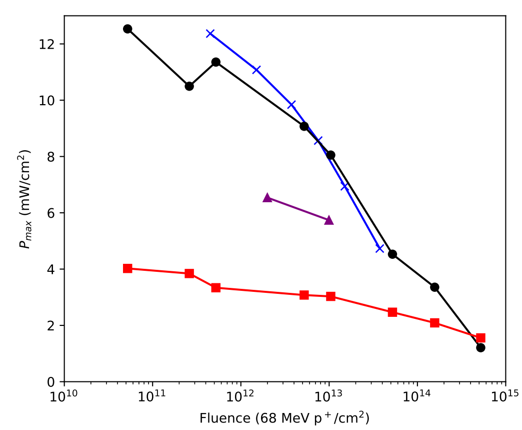
(a) J_{SC}



(b) V_{OC}



(c) FF



(d) P_{max}

Fig. 5.4 Device performance versus fluence for four different device types [6, 7]. a) short circuit current, b) open circuit voltage, c) fill factor and d) maximum power.

In terms of short circuit current, open circuit voltage and maximum power, the devices showed an improvement in performance over previous 80 nm devices in the literature [6]. The two irradiation data points from this investigation are a starting point that provide further evidence of the intrinsic radiation tolerance of ultra-thin solar cells. The boost in short circuit current indicates that the 80 nm devices in this work may outperform the thicker devices in terms of current produced at a lower fluence level than previous 80 nm devices (see Section 4.5.1 for discussion of improved diode behavior of on-wafer cells that contributed to this short circuit current boost). Assuming the short circuit current is maintained at higher fluences for these devices as it was for the 80 nm devices shown in red, a 68 MeV proton equivalent fluence of approximately 5×10^{13} p^{+}/cm^{2} is the crossing point whereby the ultra-thin regime may begin to outperform devices that are one and two orders of magnitude thicker. To test this prediction and as a continuation of the study of ultra-thin solar cell radiation tolerance, 3 MeV proton irradiation was carried out as higher DDD is more readily achieved at this energy than 68 MeV. 3 MeV exposures were also carried out with both on and off-wafer devices and this work is detailed in the next section.

5.4 3 MeV proton irradiations of ultra-thin GaAs solar cells

The devices used for 3 MeV proton exposures were produced with the layer structure detailed in Table 3.4. On and off-wafer planar devices were produced both with 1×10^{17} cm^{-3} absorber layer doping densities. The fabrication process used for these devices is identical to the devices in Sections 4.3.2 and 4.3.3. The on-wafer devices have an n on p orientation while the off-wafer cells are p on n as they have been bonded to a Si carrier chip and their growth wafer and etch stop layer have been etched away. All devices are 2.5 $\times$ 2.5 mm square areas without anti-reflection coatings. On-wafer devices have 10% front contact shading and the off-wafer devices have an improved front contacting scheme with 4.2% shading.

5.4.1 Irradiation procedure

Ultra-thin devices were irradiated with 3 MeV protons at the Dalton Cumbrian Facility. A 5 MV tandem pelletron ion accelerator (NEC model 15SDH-4 with a TORVIS source) was used to create the proton beam. Three sets of devices were irradiated to different proton fluences over three separate irradiation sessions. This yielded eight data points (each at a different fluence) for comparison 3×10^{11} p^{+}/cm^{2} to 3×10^{15} p^{+}/cm^{2}. The highest fluence of 1×10^{16} p^{+}/cm^{2} caused complete loss of device function for both on and off-wafer devices, hence eight data points were collected instead of the maximum of nine. The samples on each of the three sets are identical devices (processed in the same batch of fabrication) meaning the data can be directly compared with fluence as the variable. There are some small variations between the three sets of devices due to processing imperfections between chips and measurement noise during testing. Because of time limitations, it was necessary to adjust the beam flux depending on the magnitude of the target fluence. The beam flux therefore ranged from 2×10^{10} p^+/cm^2s to 3×10^{11} p^+/cm^2s. However, beam flux was held constant during each individual irradiation.

Improvements in device processing meant that the devices had very good uniformity as evidenced by less than 0.05 mA/cm^2 variation between short circuit current values for on-wafer devices. This allowed meaningful comparison with post-exposure data of different devices. Each set of devices contained on-wafer devices and off-wafer devices with planar Ag back surface mirrors. Best performing device results from these two different types were used to plot performance degradation as proton fluence was increased. Devices were characterised pre-exposure and as soon as possible after each of the three irradiation sessions (within two weeks of the irradiations). The three irradiations were carried out with approximately one month in between each session. Eight data points were collected for the on-wafer devices but for the off-wafer devices, only the first six fluence levels produced usable device data. This is due to the delamination of the epoxy used in the off-wafer devices and is explained in Section 5.4.6.

5.4.2 Performance degradation

Figure 5.5 shows how J_{SC} changes as a function of 3 MeV proton fluence for five different solar cell types. The three devices with 80 nm absorber layers show no significant degradation in J_{SC} up to a fluence of 2×10^{14} p^+/cm^2. The 800 nm devices do not significantly degrade until a fluence of 1×10^{12} p^+/cm^2 is reached but then show significant drop-off in current. Current degradation is most pronounced in the 3500 nm cells which degrade to below the current output of the off-wafer ultra-thin cells at the relatively low fluence of 1×10^{12} p^+/cm^2.

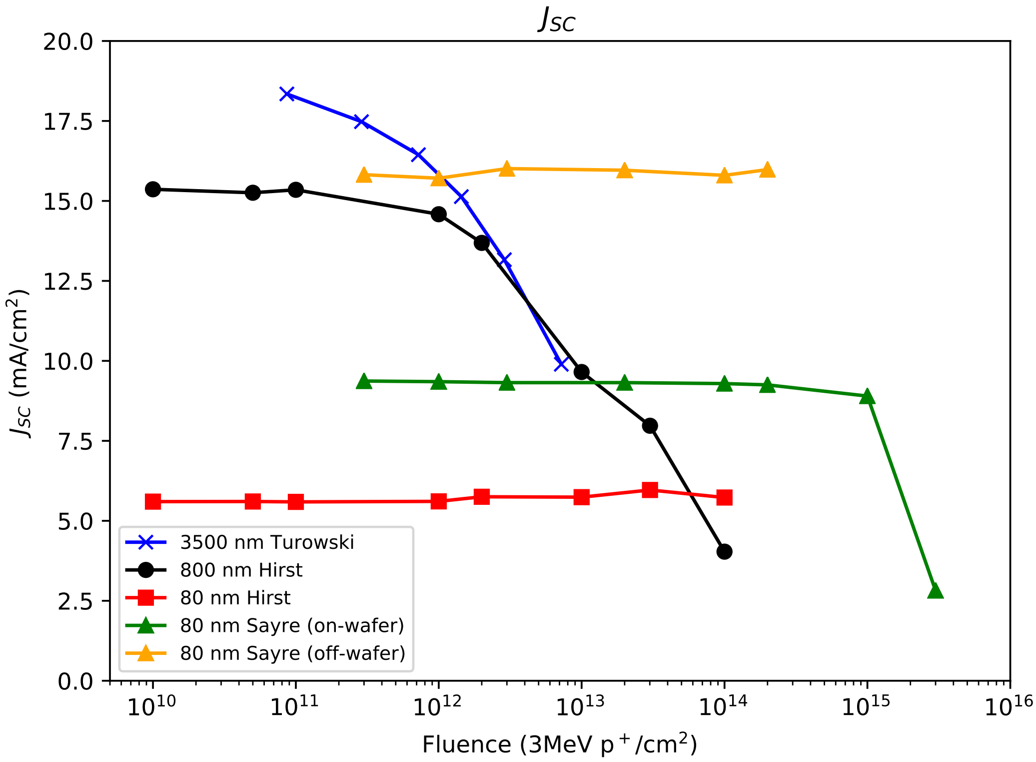
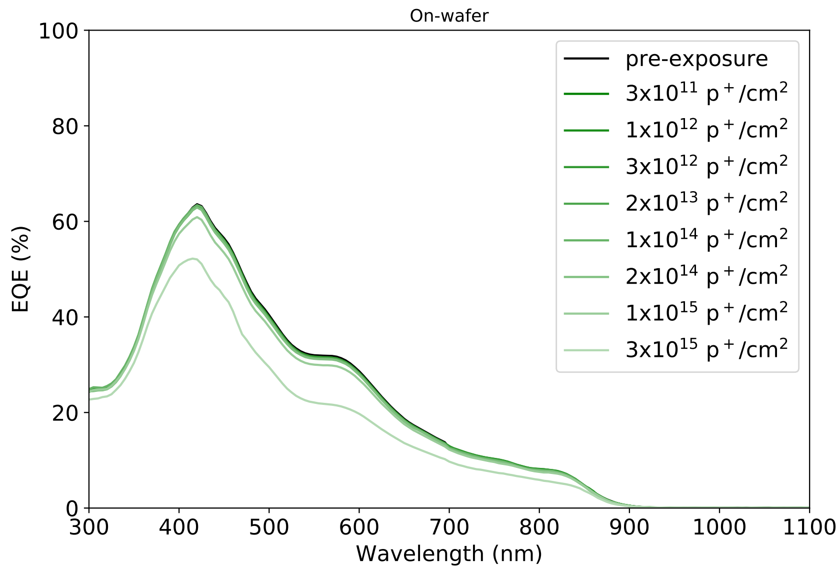


Fig. 5.5 Degradation in short circuit current of 5 different solar cell types against 3 MeV proton equivalent fluence [6, 7].

Figure 5.6 a) shows the EQE for the on-wafer cells and how a degradation is only observed once fluences of 1×10^{15} p$^+$/cm^2 and above are reached. Figure 5.6 b) shows the same data but for the off-wafer cells. No degradation is found at these lower fluences for these devices similarly to the J_{SC} data.



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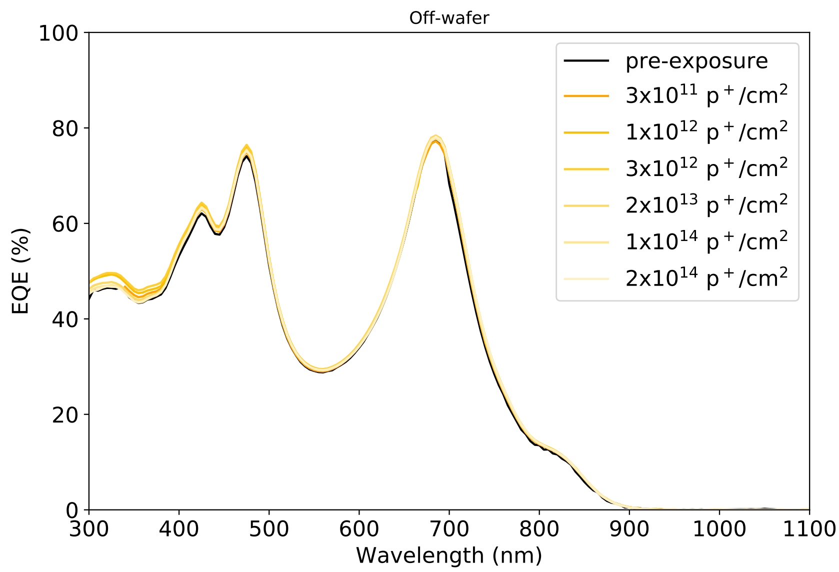


(b)

Fig. 5.6 EQE results for a) on-wafer and b) off-wafer devices before and after exposure to increasing fluences of 3 MeV protons.

Figure 5.7 shows the degradation in P_{max} for the devices as fluence is increased. This plot nicely illustrates the progress that has been made in making the ultra-thin cell competitive with more traditional length scale devices. Even at the lowest fluence of 3×10^{11} p$^+$/cm^2, the 80 nm off-wafer cells are out-performing devices that are two orders of magnitude thicker.

The on-wafer cells also begin to outperform the thicker cells at approximately 1×10^{13} p^{+}/cm^{2}

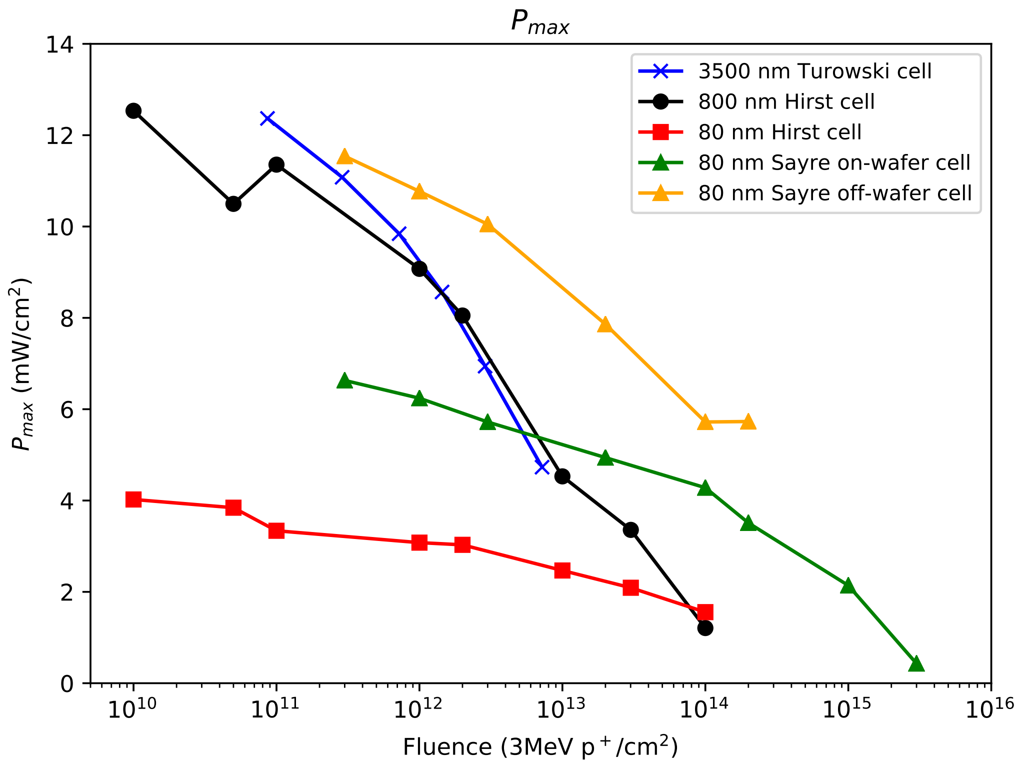


Fig. 5.7 Degradation in maximum power of 5 different solar cell types against 3 MeV proton equivalent fluence [6, 7].

Figure 5.8 shows the degradation in V_{OC} as fluence is increased. The starting V_{OC} values for the on and off-wafer devices both showed improvement over the other devices. This is a result of well-designed device layer structure which is confirmed with the low pre-exposure J_{02} values extracted for both device types. For the off-wafer devices, the V_{OC} is further improved from that of the on-wafer embodiment. This indicates a boost in voltage due to the introduction of the back surface mirror. This boost is larger than that which would be expected through the principle of superposition (see Section 4.4.1 for further analysis) since the off-wafer photocurrent is approximately 6 mA/cm^2 higher than that of the on-wafer devices. Figure 5.9 shows the degradation in fill factor as fluence is increased. The on-wafer devices show the best absolute performance in terms of this metric.

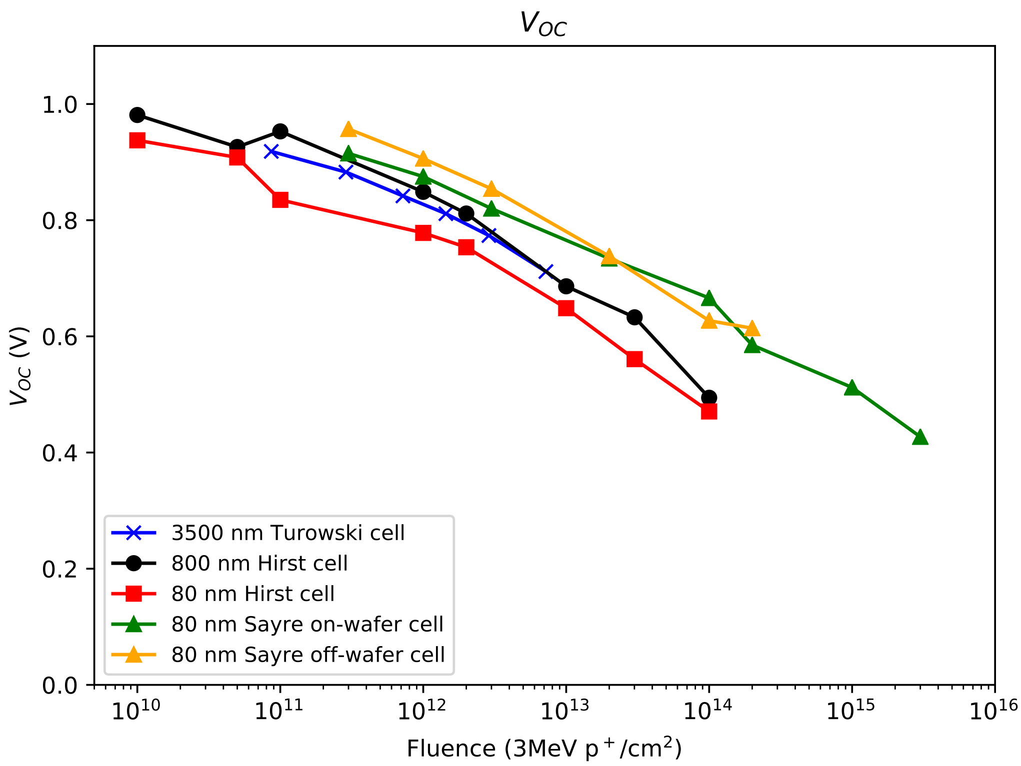


Fig. 5.8 Degradation in open circuit voltage of 5 different solar cell types against 3 MeV proton equivalent fluence [6, 7].

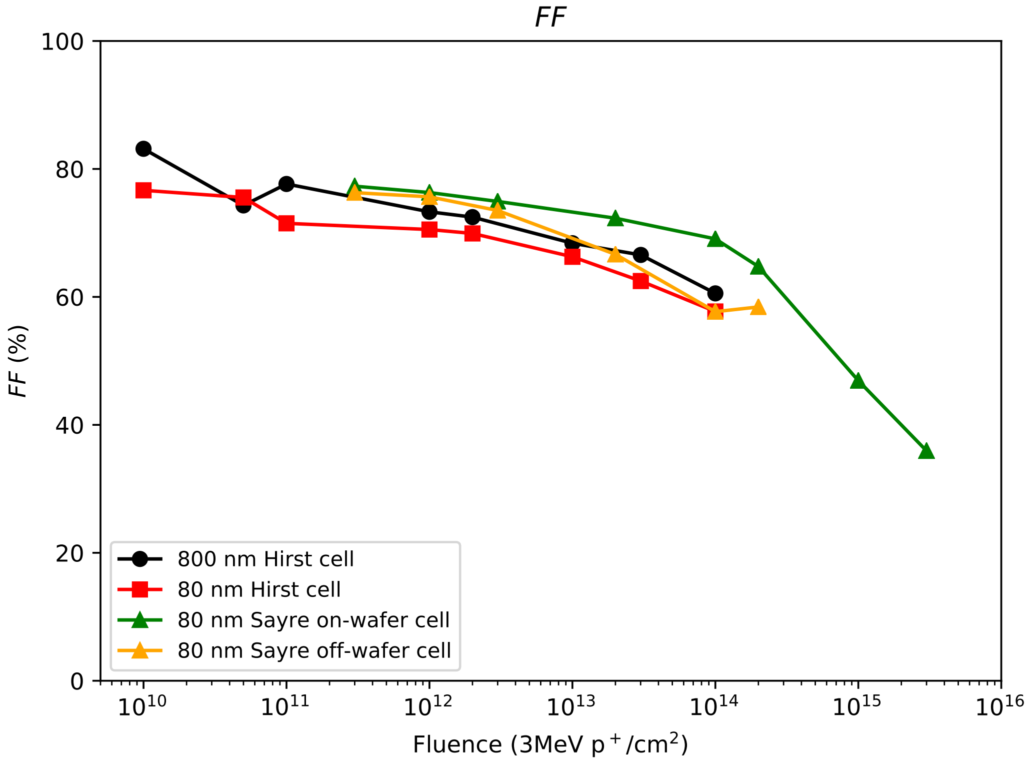


Fig. 5.9 Degradation in fill factor of 5 different solar cell types against 3 MeV proton equivalent fluence [6, 7].

5.4.3 Recombination currents and parasitic resistances

As 3 MeV fluence is increased the recombination currents and parasitic resistances of the devices are changing due to the effects of defects in the active layers. The 2-diode model was used to fit dark IV data at each fluence level and extract values for recombination currents, diode ideality factor and parasitic resistances. Figure 5.10 shows the J_{02} values for four of the device types at increasing fluences. The value increases with fluence for all types with a gradient of less than 1 except for the off-wafer cells that may have a higher rate of J_{02} increase due to epoxy heating effects. The on-wafer cells in this study show a very similar gradient to the previous 80 nm devices in the literature and show lower values than the other cell types for essentially the whole fluence range.

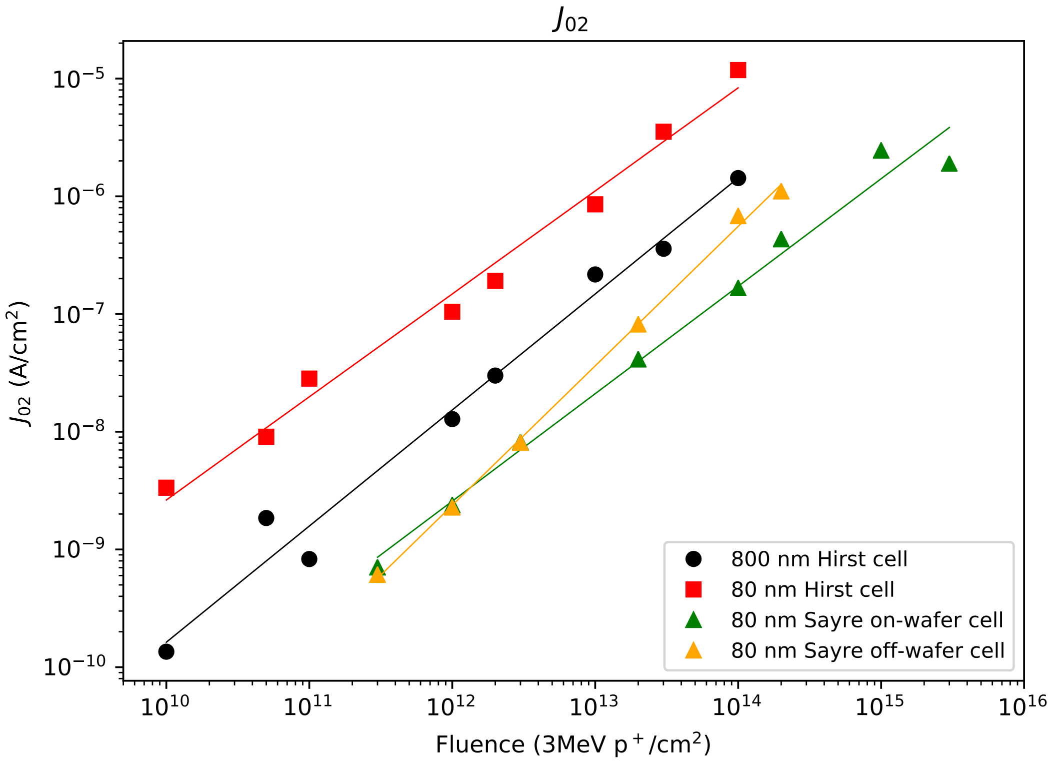
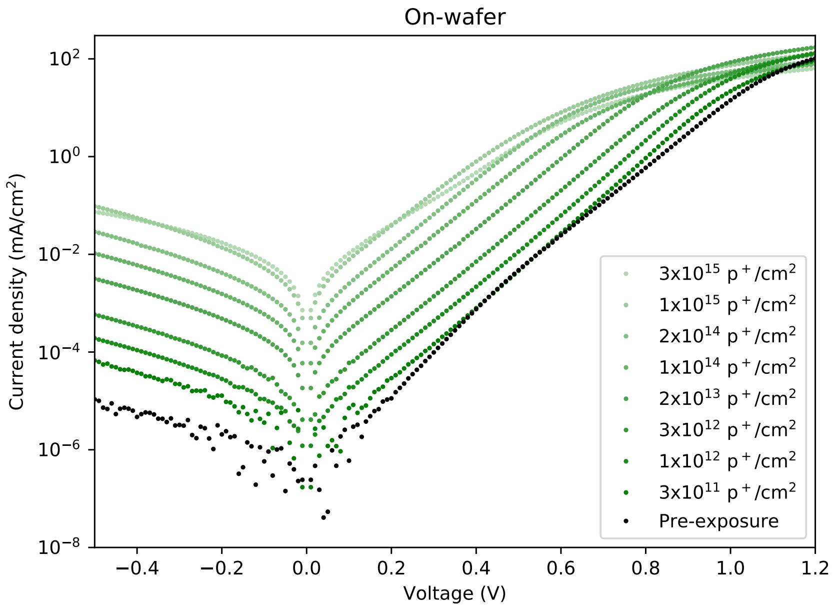


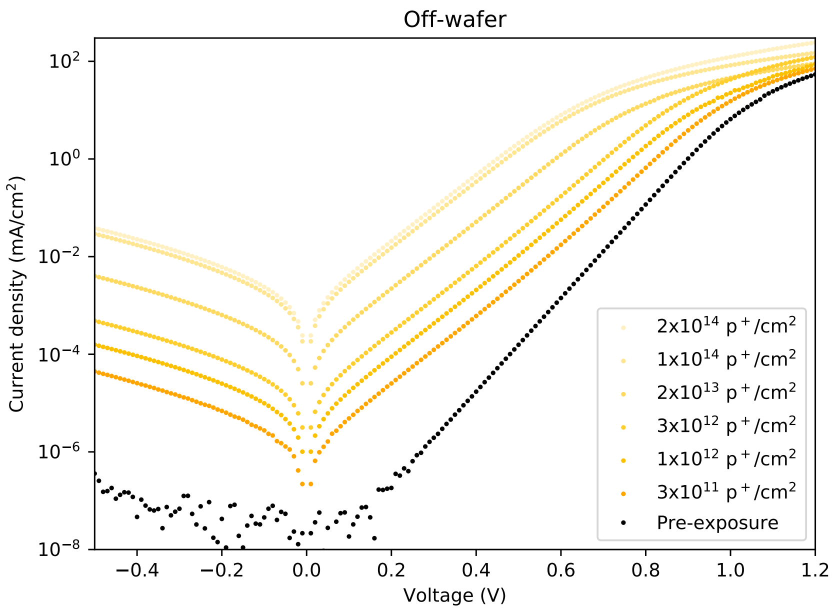
Fig. 5.10 Degradation in J_{02} of 5 different solar cell types against 3 MeV proton equivalent fluence [6, 7].

Figure 5.11 shows the experimental dark IV data from on and off-wafer devices. For the on-wafer data points at higher fluences, the series resistance plays an increasing role in the degradation of diode performance. This is confirmed by R_{ser} values extracted from the experimental data. 2-diode parameters extracted through fitting are displayed in Tables 5.3 and 5.4 and give further evidence of series resistance increasing with increasing fluence for the on-wafer cells. The series R_{ser} values for the off-wafer devices do not show a clear trend which may be due to the effect of the epoxy or the different contacting design applied to the back surface.

The on-wafer data provides the best platform for comparing these 2-diode fitting values since we can be sure the epoxy layer has not affected the degradation of electrical performance and that the effects we see are the result of only radiation damage. n_2 values increase steadily for all the devices which could be an artifact of the higher series resistances that begin to dominate at lower and lower voltages as fluence is increased.



(a)



(b)

Fig. 5.11 Dark IV experimental data for undamaged and damaged devices at a range of 3 MeV proton irradiation fluences a) on-wafer device data, b) off-wafer device data. A smaller range of fluences was available for the off-wafer devices than the on-wafer devices due to catastrophic device damage at the higher fluences likely caused by epoxy degradation in the off-wafer devices.

Table 5.3 2-diode model fitting results [5] for on-wafer devices for a range of 3 MeV proton fluences.

Fluence (p^+/cm^2)	J_{02} (mA/cm^2)	n_2	R_{ser} (Ωcm^2)
Pre-exposure	1.16×10^{-7}	2.05	1.29
3×10^{11}	7.03×10^{-7}	2.21	2.26
1×10^{12}	2.38×10^{-6}	2.28	1.84
3×10^{12}	8.14×10^{-6}	2.30	2.29
2×10^{13}	4.11×10^{-5}	2.33	2.04
1×10^{14}	1.66×10^{-4}	2.35	5.75
2×10^{14}	4.31×10^{-4}	2.33	5.53
1×10^{15}	2.44×10^{-3}	2.71	4.10
3×10^{15}	1.89×10^{-3}	2.80	7.16

Table 5.4 2-diode model fitting results [5] for off-wafer devices for a range of 3 MeV proton fluences.

Fluence (p^+/cm^2)	J_{02} (mA/cm^2)	n_2	R_{ser} (Ωcm^2)
Pre-exposure	2.58×10^{-9}	1.77	2.38
3×10^{11}	6.09×10^{-7}	2.26	3.27
1×10^{12}	2.27×10^{-6}	2.29	2.05
3×10^{12}	8.05×10^{-6}	2.33	2.27
2×10^{13}	8.15×10^{-5}	2.41	3.98
1×10^{14}	6.78×10^{-4}	2.50	3.06
2×10^{14}	1.10×10^{-3}	2.57	1.94

5.4.4 Remaining factor analysis

Figure 5.12 shows the remaining factors (RF) for four different solar cells. RF analysis was carried out for the on-wafer devices in this study and not the off-wafer since there is a wider range of fluence data points available and the potential device degradation induced by epoxy heating and delamination effects in the off-wafer embodiment could not be decoupled from the radiation induced performance loss.

Despite the higher fluences at which the on-wafer cells were tested, the remaining factors are very high in all four quantities plotted. At first glance, the on-wafer devices show similar trends in degradation to the previous 80 nm devices in red but it is important to note that this degradation is after exposure to fluences that are orders of magnitude higher.

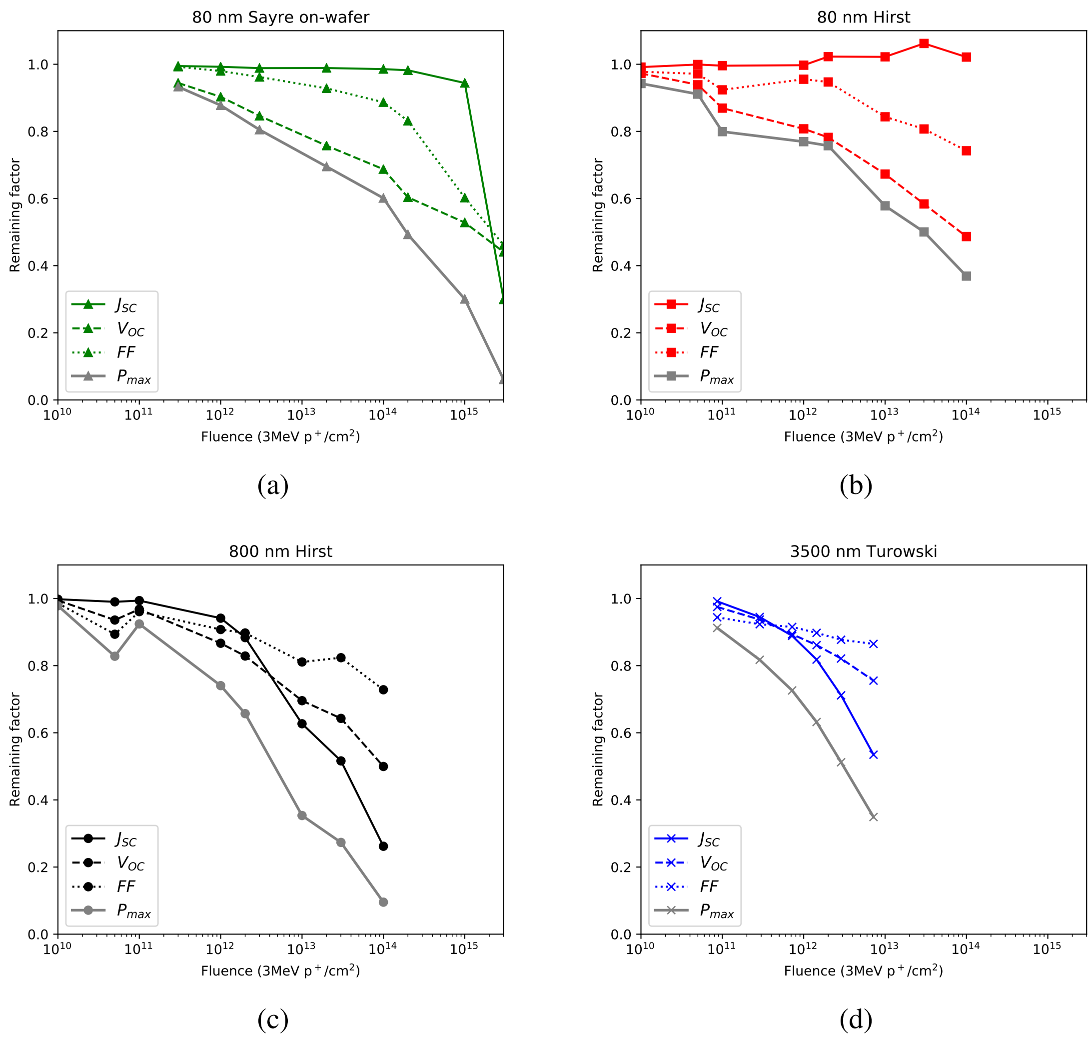


Fig. 5.12 Remaining factors for short circuit current, open circuit voltage, maximum power and fill factor for four different device types [6, 7].

Figure 5.13 shows the RF of maximum power for four devices compared on one plot for direct comparison. The on-wafer devices from this study perform significantly better than thicker devices in terms of maximum power RF which provides further evidence that the ultra-thin regime, when carefully optimised in terms of diode performance, light management and bonding method can be an enabling technology for hostile spacecraft missions.

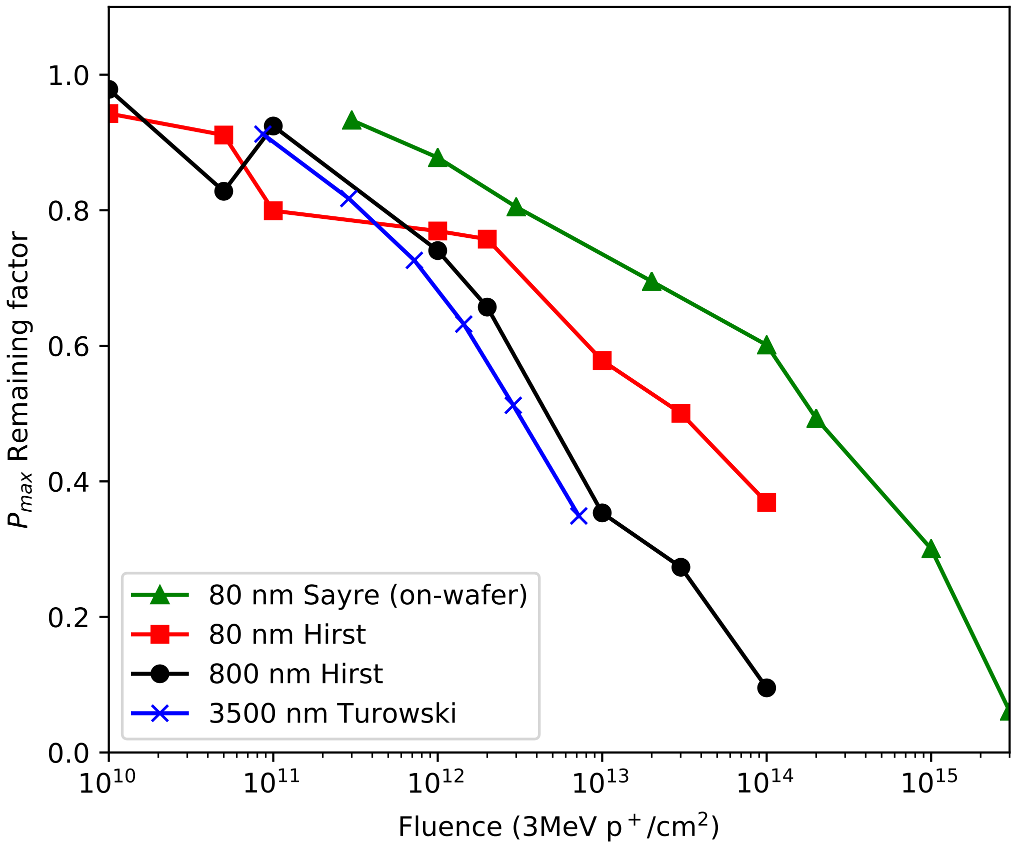


Fig. 5.13 Maximum power remaining factor comparison for four different solar cell types [6, 7].

5.4.5 Summary

For the ultra-thin devices in this study, the short circuit current is not degraded until extremely high fluences are reached. This is consistent with previous works on ultra-thin devices. Furthermore, this is the first study to reach a high enough fluence that a degradation in short circuit current is demonstrated for an ultra-thin cell. This is potentially because the carrier lifetime is still long enough to reach the contacts even when high levels of defects are introduced but a point is eventually reached where the lifetime drops below the time needed to traverse the junction.

5.4.6 Epoxy heating effects

During irradiations with fluences below 1×10^{15} p^{+}/cm^{2}, the temperature of the samples did not increase significantly above room temperature. However, for fluences of 1×10^{15} and above, the stage current needed to be higher which produced some heating. The maximum temperature reached by the thermocouple spot welded to the aluminium carrier plate was approximately 90°C which is well below the threshold for annealing. It is also well below the glassing temperature of the epoxy (only applicable to the off-wafer devices). The glassing temperature of the OPT5054-4G two-part Optitec epoxy is listed as greater than 140°C. However, for fluences 1×10^{15} p^{+}/cm^{2} and above the off-wafer cells began to sustain damage visible to the naked eye and large sections of the device area appear to have delaminated (see Figure 5.14). This may be due to the mismatch in thermal expansion coefficient between the epoxy and the semiconductor and metal layers. It may also be that there was excess heating in the epoxy layer beyond that detected by the thermocouple which was not in direct contact with the samples.

In the space environment, it is not likely that such extreme temperature gradients would be encountered but the higher rate of degradation of the epoxy bonded cells during irradiation does indicate a need for a more robust bonding medium or process to take full advantage of the radiation tolerance of the devices in the space environment.

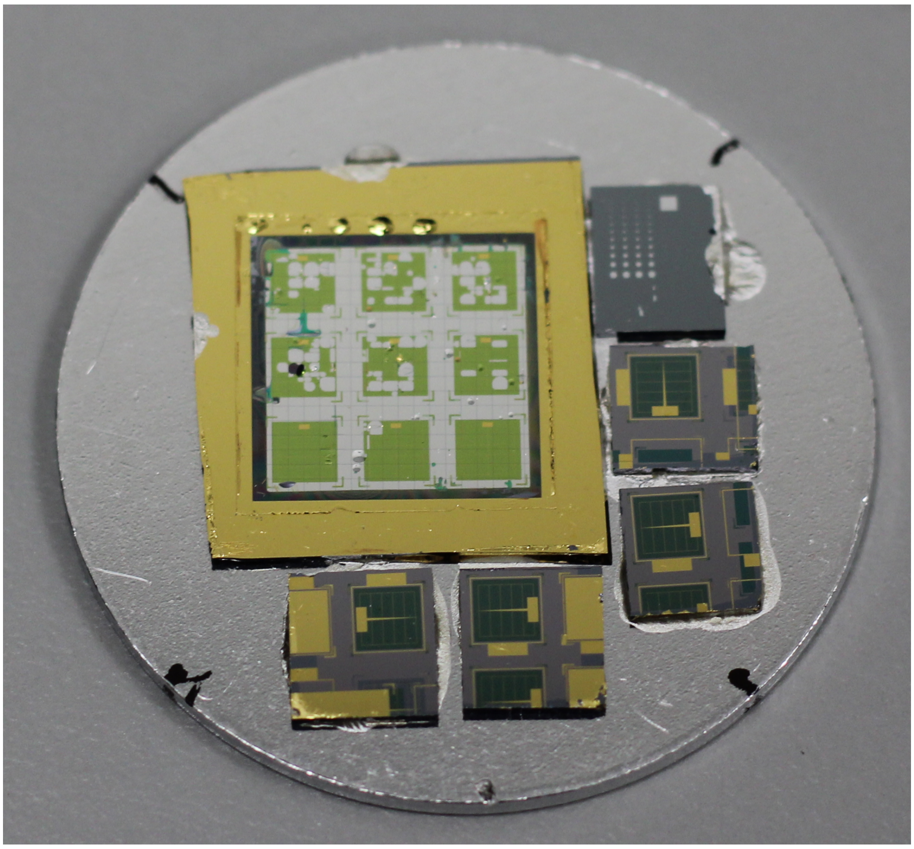


Fig. 5.14 Photo of 3 MeV proton exposed samples showing the visible flaking and damage in the off-wafer device chip, the large chip in the upper left area is the off-wafer devices, the smaller chips on the lower and right hand edges are the on-wafer devices.

5.5 Extrapolation to on-orbit conditions

Orbits of interest are analysed and compared to the radiation tolerance testing carried out on the 80 nm devices in this chapter. This provides context for the high levels of radiation tolerance exhibited by these devices and shows that they are a step towards enabling exciting future space missions. The specific orbital geometry and mission profiles referred to in this section are detailed in Appendix B.

5.5.1 Jovian/Europa mission

Jupiter, the largest planet in our solar system, has 79 known satellites (moons, asteroids etc.). One of it's moons, Europa is seen by the scientific community as a potential location for the discovery of extra-terrestrial life. Disruptions in the magnetosphere of Jupiter around Europa were detected by the Juno mission [115, 116]. This disruption indicates the presence of an electrically conductive medium beneath the surface of the icy moon which could be salty water. Studying the surface and sub-surface of Europa would therefore unlock exciting avenues for astrobiology and oceanography [117]. This would require a lander to be deployed to the surface of the icy moon [118]. However, there are high levels of damaging radiation present around Jupiter and its moons. This means the radiation tolerance of the PV power systems needs to be extremely high [119].

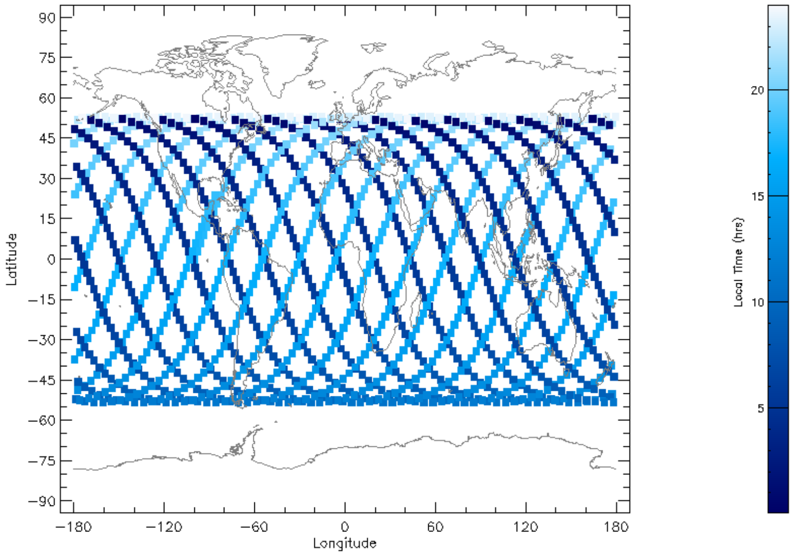
Exploration of Jupiter and its orbital environment with man-made satellites began in the 1970s with Pioneer 10 [120]. Since Jupiter is a long distance from Earth, the amount of solar radiation reaching spacecraft in its environment is a small fraction of that reaching Earth. Therefore the area of the solar array needed to produce sufficient power increases significantly. This increases the need for a PV technology with a high power to weight ratio and little to no heavy coverglass. Additionally, Europa has very little atmosphere so any lander deployed to its surface would need to be slowed down with some sort of rocket system. This adds another weight constraint on the mission. The lighter the system, the easier it will be to slow it down during the final approach to the surface of Europa. The Europa Clipper is planned for launch by NASA in 2024 and will use flybys of Europa to map its surface rather than orbiting it to minimise radiation dose to power systems and electronics [121].

68 MeV irradiations are useful for investigating the degradation of solar cells in Jovian environments since there are increased levels of these higher energy ions. The displacement damage dose equivalent to 1×10^{13} p^{+}/cm^{2} fluence of 68 MeV protons corresponds to approximately 5 years in a Europa orbit [122]. Ultra-thin on-wafer devices showed 96% of BOL short circuit current and 72% of BOL maximum power after damage at this level.

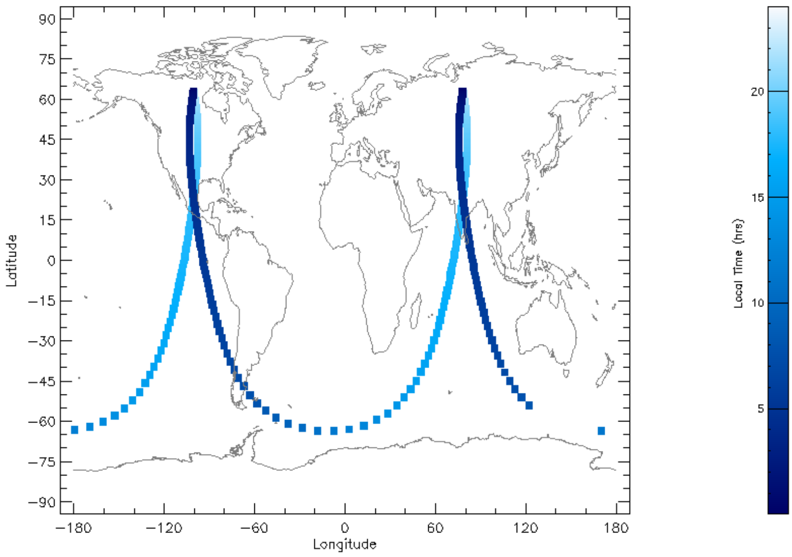
5.5.2 HEO/Molniya orbit

HEO orbits can provide continuous coverage to the Earth's polar regions with far fewer satellites than polar LEO orbits. Due to their eccentricity, satellites in HEO orbits have a long dwell time over specific points on Earth that are dictated by the exact geometry of their orbits. In order to provide continuous satellite coverage to a specific polar region just three HEO satellites with a period of approximately 8 hours would be needed. This is in contrast to the large constellations of LEO satellites that would be needed to provide equivalent coverage [9].

Ground track diagrams show the point on Earth that a satellite is directly above during its orbit. Figure 5.15 a) shows the ground track for the LEO orbit used by Starlink [8]. It shows how the LEO orbit does not remain over a single region for any significant amount of time. Figure 5.15 b), on the other hand, shows a Molniya orbit which is a specific HEO type that has a very long dwell time over specific polar regions.



(a) Starlink LEO



(b) Molniya

Fig. 5.15 Ground tracks showing time of day during satellite orbit for a) a Starlink LEO orbit at 550 km [8] and b) a Molniya orbit [9].

5.5.3 Solar cell performance on orbit

Different orbits can have very different levels of damaging radiation. Figure 5.16 shows the differential proton flux versus energy for four different orbits: Molniya, Starlink LEO, GEO and Europa (one of the moons of Jupiter). This illustrates the significantly higher radiation levels present over the lifetime of any spacecraft in a HEO orbit or Jovian environment than more standard LEOs and GEOs.

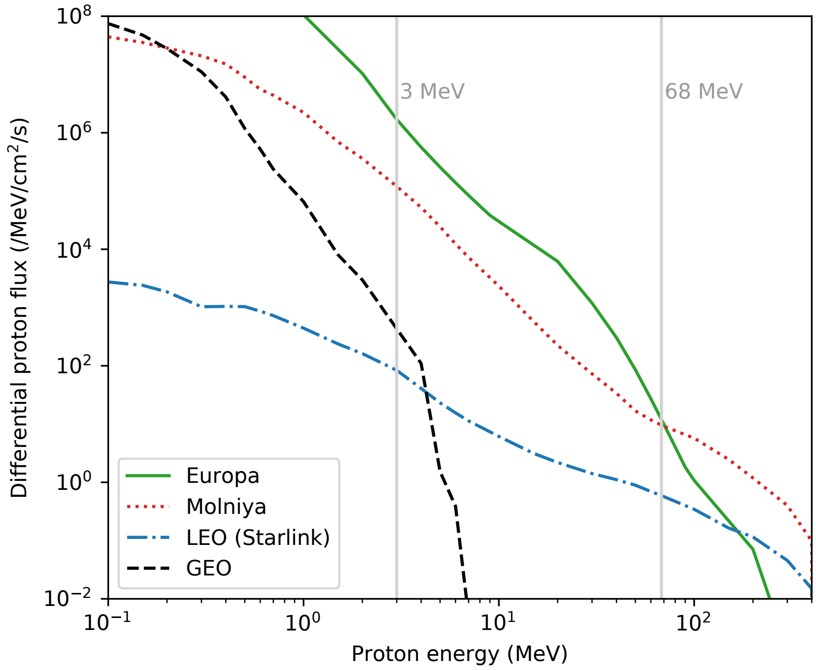


Fig. 5.16 Differential proton flux versus energy for Europa, Molniya (HEO), LEO used by Starlink and GEO orbits.

Coverglass placed over the top of space solar panels attenuates the incoming damaging radiation and reduces the damage that the active layers of the device sustain during mission lifetimes. This attenuation is dependent on the coverglass thickness and can be incorporated into radiation damage modelling during spacecraft missions. Figure 5.17 shows the effect of varying thicknesses of coverglass on the maximum power output of four different solar cells after 20 years in a Molniya orbit. In order to retain 7 mW/cm^2 power output after 20 years on orbit in this hostile environment, just 81 μm of standard CMG coverglass would be needed to protect the 80 nm off-wafer devices in this study. By comparison the 800 nm devices [6] would require 258 μm of coverglass to retain the same power output. This presents a massive cost saving for the overall satellite mission through a reduction in coverglass weight.

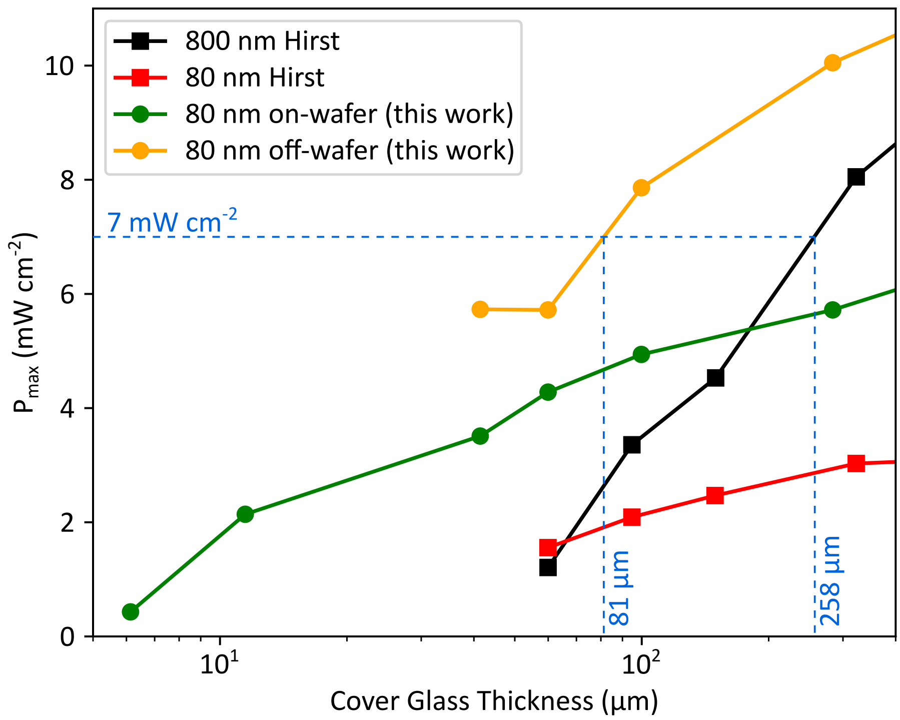


Fig. 5.17 Maximum power output of four different solar cell types with varying CMG coverglass thicknesses after 20 years in a Molniya orbit. Plot from [10] and courtesy of Armin Barthel.

5.6 Discussion

5.6.1 Further testing for space-worthiness

Beyond the mono-energetic irradiations carried out in this investigation, there are many other rigorous tests that need to be performed before a solar cell technology can be considered useful for space missions [123]. These space-worthiness tests include vibration, thermal cycling, shock, pressure and many more. Space weather should also be taken into account with fluctuations above the predicted radiation environment due to storms potentially causing anomalous amounts of damage to satellites [124]. The Sun's activity undergoes an approximately 11 year cycle with solar minimum and maximum periods. Solar energetic events are more likely during the solar maximum phase. Magnetic storms can also increase the particle levels in the Earth's radiation belts.

5.6.2 Other potential space photovoltaics materials

Other materials have been proposed for use as space PV systems such as perovskites [125, 126]. Perovskites have not yet shown the high stability and performance of epitaxially grown III-Vs but they are an exciting option in terms of low cost processing and the issues of damage due to moisture are avoided when on orbit [127]. Lifetime requirements may also be less stringent for certain space applications than for terrestrial PV which works to the advantage of perovskites. They also show promise in achieving flexible form factors and self-healing properties [128]. Perovskites have shown potential for higher specific power than traditional III-V on Ge cells but they still require some form of encapsulation which significantly increases their overall weight. Ultra-thin GaAs cells by contrast, are stable in vacuum and non-vacuum conditions and therefore do not need the added weight of encapsulation.

Chapter 6

Ultra-thin device loss analysis and pathway to improvement

6.1 Introduction

Previous chapters have presented 80 nm ultra-thin devices with the goal of achieving radiation tolerant, high specific power cells that can be used in the hostile environments outside of the Earth's atmosphere. Significant progress has been made in the design and fabrication of planar and nanostructured 80 nm devices. This 80 nm length scale has shown excellent tolerance to high energy proton radiation at extremely high fluences. These results show exciting performance improvements over previous ultra-thin devices in the literature but the best efficiency of 9.08% in the case of the off-wafer DTL patterned devices is not a high enough value to compete with the technologies currently used for space PV. However, when other metrics other than raw efficiency are considered, such as specific power and radiation tolerance, these ultra-thin devices may enable currently inaccessible satellite mission profiles.

In this chapter, using both simulations and extrapolations from experimental device data, a detailed loss analysis is carried out with the goal of further improving the beginning and end of life (BOL/EOL) performance of the ultra-thin devices to boost their value as potential space power systems. Simulation is used to show a feasible pathway from 9.08% AM0 BOL efficiency to 16% for DTL patterned ultra-thin devices. Each step along this pathway to 16% is analysed for feasibility and potential impact on performance and fabrication. An anti-reflection coating with specific features for the ultra-thin regime is designed and tested. The DTL patterning is analysed for potential improvements that could contribute to increased photocurrent.

Finally, EOL performance and CL analysis is used to inform future device design improvements. Carrier lifetime is correlated with the fluence of damaging radiation that devices were exposed to. This provides evidence that the degradation in short circuit current seen in the 3 MeV damaged on-wafer devices at high fluences is due to carrier lifetimes degrading to a value below the time it would take them to traverse the junction and reach the contacts. Using this new analysis, layer structures optimised for different spacecraft mission profiles are discussed.

Phoebe Pearce carried out the simulations used to optimise the ARC layer thickness, produced Figure 6.3 and the improved efficiency simulations summarised in Figure 6.4. Eduardo Camarillo Abad carried out the TMM simulations incorporated into Figure 6.2. Armin Barthel carried out the CL measurements on damaged ultra-thin devices and processed the CL data.

In this chapter three devices are referred to: on-wafer, planar Ag and DTL. These are the same devices that were presented in Chapter 4. On-wafer refers to planar devices still on their growth substrate with no light management as fabricated in Section 4.3.2. Planar Ag refers to off-wafer planar devices with an integrated back surface mirror as fabricated in Section 4.3.3. DTL refers to devices patterned with the metal-dielectric periodic back-surface light management structure detailed in Section 4.3.4.

6.2 Anti-reflection coatings for ultra-thin cells

6.2.1 Silicon dioxide coatings

ARC coatings are standardly employed to reduce optical losses in solar cells due to front-surface reflection. 110 nm SiO_2 coatings were deposited using a thermal evaporator as the first test for ARC coatings on the ultra-thin devices. The SiO_2 was thermally evaporated onto the front surface of on and off-wafer planar devices. The thickness was determined by the match between peak position in the TMM simulation and the measured EQE. In order to ensure the devices could still be electrically contacted, the front and rear contact pads needed to be protected from the SiO_2 coating. A metal shadow mask with small tabs covering the contact pads was used rather than another photolithography lift-off step. Device chips were temporarily attached to the shadow mask using Kapton tape to ensure the tabs aligned with the contact pads and stayed in the correct place during evaporation.

Characterisation of devices was carried out before and after SiO_2 evaporation to isolate the effect of the film. EQE, AM0 LIV and DIV was taken to analyse the electrical and optical effects of the coating. Figure 6.1 presents the LIV and DIV data. The coating produced an increase in short circuit current for both the on and off-wafer devices as shown in Table 6.1. However, there was a significant decrease in open circuit voltage and fill factor. This voltage degradation caused overall efficiency and maximum power decreases in the devices even though there was a boost in short circuit current.

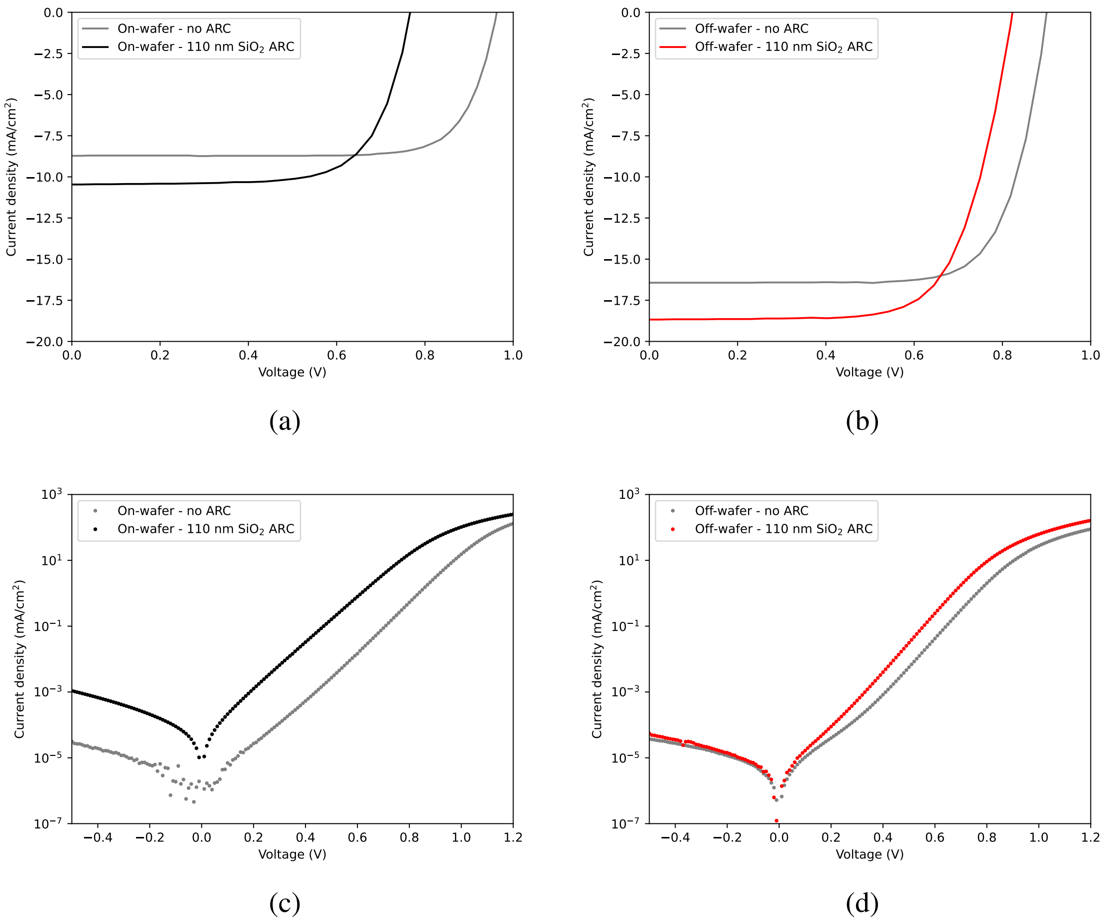


Fig. 6.1 LIV and DIV experimental data of on-wafer and planar Ag devices before and after addition of a 110 nm SiO_2 ARC. a) and b) show LIV, c) and d) show DIV.

J_{02} values also increased significantly after the addition of the ARC coatings in both device types. This indicates increased recombination in the depletion region. Very similar degradation characteristics are seen in both types of devices which indicates that the presence of the epoxy in the off-wafer devices is not the main cause of the issue.

EQE analysis, both simulated and experimental, was also used to investigate the effect of the SiO_2 coating. Figure 6.2 compares three sets of data for the two device types. These are pre-ARC, with 110 nm SiO_2 ARC coating and TMM simulated device with 110 nm SiO_2 ARC. This figure shows significantly lower EQE in the shorter wavelength region for the

Table 6.1 Comparison of pre-ARC and ARC coated on-wafer and planar Ag device AM0 LIV performance.

Device type	J_{SC} (mA/cm^2)	V_{OC} (V)	FF (%)	AM0 efficiency (%)	P_{max} (mW/cm^2)
On-wafer	8.74	0.962	77.79	4.84	6.54
On-wafer with ARC	10.45	0.766	71.01	4.20	5.68
Planar Ag	16.43	0.900	74.55	8.15	11.03
Planar Ag with ARC	18.67	0.823	69.72	7.92	10.71

Table 6.2 Comparison of pre-ARC and ARC coated on-wafer and planar Ag device DIV performance.

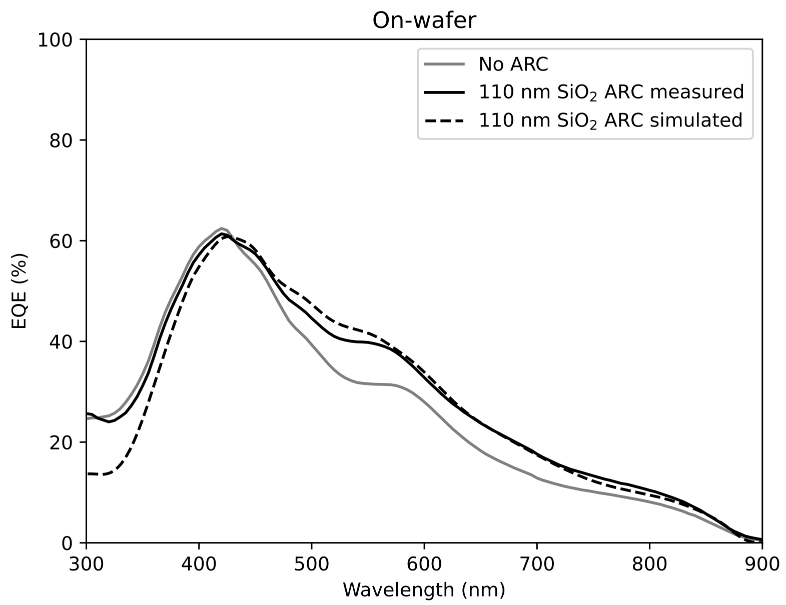
Device type	J_{02} (mA/cm^2)	n_2	R_{ser} (Ωcm^2)	R_{par} (Ωcm^2)
On-wafer	5.20×10^{-7}	2.26	1.06	2.40×10^{7}
On-wafer with ARC	5.21×10^{-5}	2.42	1.09	9.72×10^{6}
Planar Ag	3.19×10^{-7}	1.98	2.47	9.81×10^{6}
Planar Ag with ARC	1.34×10^{-6}	1.93	1.89	1.79×10^{7}

off-wafer device than is predicted by simulation. This effect is not explained by parasitic absorption in the ARC layer as the 110 nm SiO_2 layer is transparent in this wavelength region.

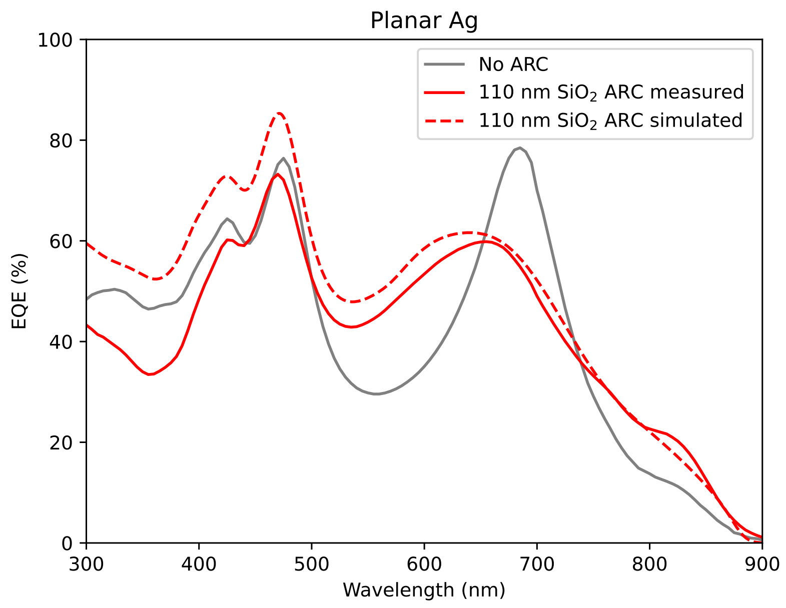
6.2.2 Band-bending

One potential explanation for the degradation in open circuit voltage and fill factor after the addition of an SiO_2 coating for both on and off-wafer devices is the introduction of band-bending effects at the front surface of the devices. For the on-wafer devices the SiO_2 is in contact with the front surface InAlP layer and for the off-wafer devices it is in contact with the InGaP due to the inverted geometry. Since the devices are so thin, changes to the electrical properties of the semiconductor material due to the ARC addition do not need to penetrate very far to have a significant effect on device performance.

The shorter wavelength EQE data in Figure 6.2 b) is lower than predicted in simulation which suggests that the SiO_2 coating is creating an effect at the front surface that leads to a loss of V_{OC} and FF. Due to the presence of device layers vulnerable to HCl on the front surface, a dip to remove the native oxide was not carried out before the ARC coating was



(a)



(b)

Fig. 6.2 EQE of a) on-wafer and b) planar Ag devices without ARC, with ARC and simulated with ARC. The ARC layer is a 110 nm film of SiO_2.

added. The presence of this oxide may have further degraded the interface of the ARC and the front surface passivation layer.

The choice of a high *k* dielectric such as SiO_2 may be part of the problem. These materials have shown Fermi-level pinning in transistors and this effect may be present here [129]. The penetration depth of the depletion region formed at the dielectric-semiconductor interface does not need to be large in order to affect performance since the passivation layers are only 20 nm. Other groups have used much thicker passivation layers when designing ultra-thin cells which may be how they were able to produce devices of a similar absorber layer length scale with ARC coatings and achieve open circuit voltages above 1 V [36, 43, 45].

A proposed solution would be to increase the thickness of the front-surface passivation layer to reduce the band bending effect at the front surface which is particularly clear in the off-wafer device. The excellent passivation properties of InGaP on the front surface of the solar cell as discussed in Section 4.5.1 suggest that the thickness of the layer could be increased without significant degradation in current due to parasitic absorption. Interface control of the native oxide on the front surface is also needed to avoid mid-gap pinning.

6.2.3 ARC design for the ultra-thin regime

Simulations were carried out to determine the optimum thickness and material for the ARC used with the ultra-thin devices in this study. Single and dual layer ARCs were compared as multiple ARC layers of different materials are often used for multi-junction space solar cells. Figure 6.3 a) shows the optimisation of a single-layered coating of Al_2O_3 using the TMM method to extract predicted photocurrent. Approximately 70 nm was the thickness of Al_2O_3 simulated to be ideal for all three device types. A dual layered ARC using MgF_2 and Ta_2O_5 was also simulated using a TMM method, as shown in Figure 6.3 b), which predicted lower photocurrent values. This combined with the added fabrication complexity of a dual layer means that a single layer approach is predicted to give the best performance.

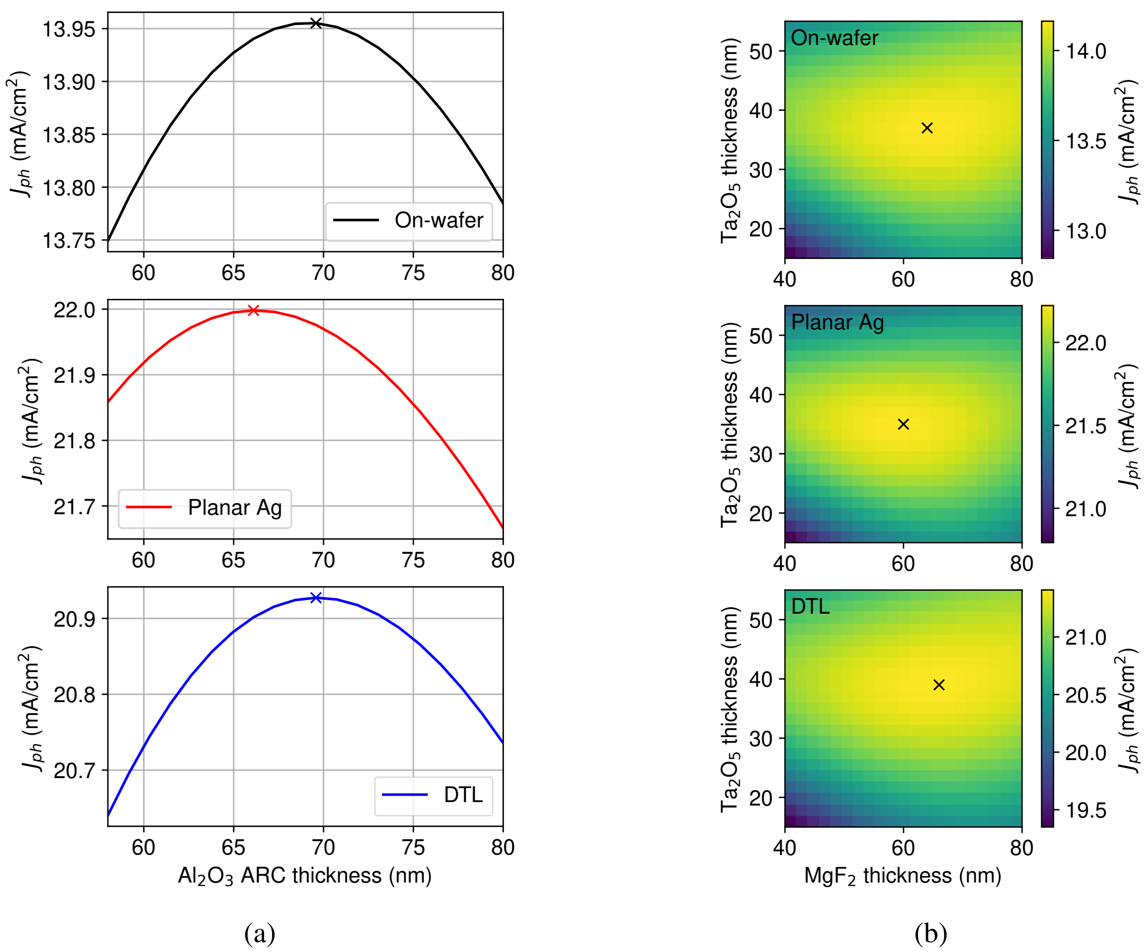


Fig. 6.3 a) Photogenerated current as a function of the thickness of a single-layer Al_2O_3 anti-reflection coating and b) photogenerated current for the three devices as a function of the thickness of both MgF_2 and Ta_2O_5 used in a double-layer anti-reflection coating. In both cases, the on-wafer and planar devices were simulated using TMM while the nanophotonic device incorporating a grating was simulated using RCWA. The cross in each plot indicates the location of the maximum. Plot from [4] and courtesy of Phoebe Pearce.

6.3 Beginning of life performance optimisation

6.3.1 Optimisation of light management structure

Table 6.3 details the predicted performance increases due to simulated fabrication improvements for all three devices. This highlights the importance of optimising the nanophotonic metal-dielectric grating since the introduction of the SiN layer increases parasitic absorption when compared to a planar Ag reflective layer. When the structure is fully optimised, as in

Table 6.3 Measured and simulated short circuit current and AM0 efficiency for on-wafer, off-wafer with planar Ag mirror and DTL patterned hero devices.

	J_{SC} (mA/cm^2)		Efficiency (%)	
Device type	measured	improved	measured	improved
On-wafer	10.04	15.1	5.40	9.5
Planar Ag	15.33	21.8	9.06	14.0
DTL	15.35	26.0	9.08	16.0

simulations, the maximum performance is higher than a planar mirror but with fabrication imperfections, the DTL performance is very similar to that of the planar Ag device.

An efficiency of 16% would not allow these ultra-thin GaAs cells to compete with the industry standard multi-junction cells currently used for space power applications in terms of absolute efficiency. However, these devices have much higher power production per unit of mass and previous studies have shown a superior radiation tolerance in the ultra-thin regime. These two features combined with the potential for flexible form factors and lowered need for heavy coverglass could enable exciting new space missions and the use of hostile but strategically advantageous Earth orbits.

6.3.2 DTL device loss analysis

With the integration of an ARC, optimisation of light management structures and reduction in front-contact shading losses, it was simulated that the efficiency of the devices could reach 9.5%, 14.0% and 16.0% for the on-wafer, off-wafer planar Ag and the off-wafer DTL patterned devices respectively. This shows how the optimised DTL patterned device has more potential for increased performance than the planar Ag type despite their similar experimental performance in this project.

Figure 6.4 provides a visualisation of these improvements to the DTL patterned device that could feasibly be implemented and the resulting boost in J_{SC}. The biggest predicted improvement is from the addition of a single-layered ARC. Further optimisation of the grating design is also predicted to boost the current. The simulated improvements are listed below:

1. Addition of an ARC
2. Fully etched grating
3. Adjusting the disk radius to 1/3 of pitch

4. Adjusting pitch to be 600 nm
5. Reducing front contact shading from 10% to 3%

Point (2) can likely be achieved by optimising the etching process. By varying the etch time and intensity and analysing the resultant nanostructures with cross-sectional SEM, the residual domes of SiN at the bottom of the etched holes could be reduced or eliminated. The improvement in point (3) to change the disk radius to 1/3 of the period is easily implemented by changing the exposure time during the patterning. Point (4) to change the period of the pattern to 600 nm would require a new mask to be ordered with the updated period.

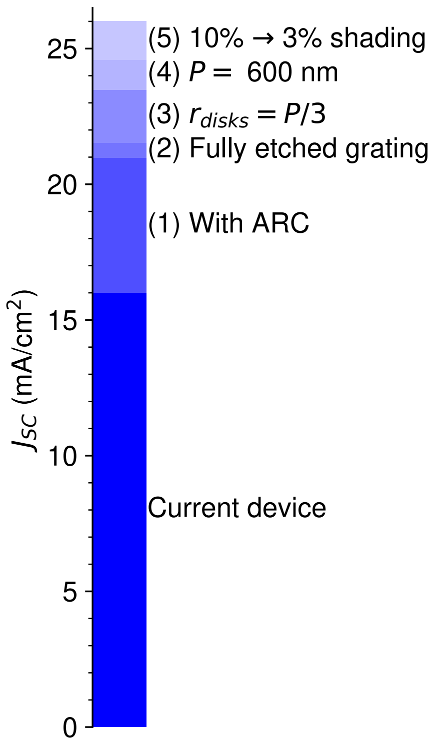


Fig. 6.4 Simulated short circuit current improvements to DTL patterned off-wafer devices with fabrication optimisation and the addition of an anti-reflection coating. Current experimental device performance is plotted as a baseline with each simulated improvement making a contribution to improved current output. r_{disks} is the radius of the holes etched into the SiN layer during DTL patterning that were then filled with Ag, P is the period of the DTL patterned grating. This figure is courtesy of Phoebe Pearce.

6.4 End of life performance optimisation

Once beginning of life performance is fully optimised, our attention can turn to end of life performance after exposure to damaging radiation. When designing solar cells for specific space applications, the orbit needs to be taken into consideration. The lifetime of the power system is often the limiting factor in satellite mission lifetimes. Extensive radiation testing in Chapter 5 provided more evidence that ultra-thin solar cells have an intrinsic tolerance to damaging radiation. A detailed CL study was carried out to correlate carrier lifetime degradation with device performance. This is the first time that the mechanism by which ultra-thin solar cells show intrinsic radiation tolerance has been investigated.

6.4.1 Cathodoluminescence study

CL was used to analyse the radiation induced degradation in ultra-thin solar cells at the nanometre scale. CL is a scanning electron microscopy technique [130] that can be used to investigate radiation-induced non-radiative defects in solar cell materials. If carriers that are excited into the conduction band by the incident electrons radiatively recombine then the emitted photons are detected and quantified. The emitted luminescence can be resolved spectrally, spatially and temporally. Since the technique uses electrons, the spatial resolution is very high. 90% of the energy of the electrons is deposited within a depth of approximately 130 nm and a width of approximately 140 nm.

6.4.2 Radiation-induced performance degradation analysis

Minority carrier lifetimes were extracted from time-resolved CL time traces plotted against 3 MeV proton fluence. This lifetime data was taken with the on-wafer devices that were presented in Chapter 5. Data for fluences above 2×10^{14} p^+/cm^2 was not taken as the lifetimes are so short they have fallen below the instrument response time. Therefore an extrapolation was used to approximate the carrier lifetime in the highest fluence regions of 1×10^{15} to 1×10^{16} p^+/cm^2.

The time that a carrier takes to travel across the junction after photogeneration is referred to as the transit time. This value is assumed to be constant for the ultra-thin devices in this study and can be compared to the carrier lifetime that is degrading with increasing fluence. The point where the carrier lifetime drops below the transit time should in theory correlate with when the short circuit of the devices begins to degrade. Equation 6.1 is used to calculate the transit time for the devices in this study.

$$t_{tr} = \frac{W^2}{\mu V} \tag{6.1}$$

Where t_{tr} is the transit time, W is the junction width, μ is the carrier mobility and V is the built-in voltage across the junction. Hole mobility in GaAs is less than electron mobility so is the limiting factor and was used to calculate transit time. A mobility of 490 $cm^2V^{-1}s^{-1}$ [131] was used to find a transit time of approximately 0.1 ps. This transit time is the same order of magnitude as the lifetime that is extrapolated for the fluence range of 1×10^{15} to 1×10^{16} p^+/cm^2. This means the onset of degradation of short circuit current agrees well with the point at which the carrier lifetime drops below the junction transit time. This evidence supports the theory that ultra-thin solar cells exhibit high radiation tolerance due to carrier lifetimes remaining long in relation to the junction transit time up until extremely high fluences.

6.5 Improved device layer structure

The results of radiation damage testing indicate that an absorber layer thicker than 80 nm (but still on the order of 100 nm in thickness) will still exhibit higher radiation tolerance than standard thicker solar cells but the onset of short circuit current collapse will occur at a lower fluence. A study analysing a range of absorber layer thicknesses (100 nm, 110 nm, 120 nm etc.) could therefore be useful to carry out. If these cells were then irradiated under the same conditions, their degradation characteristics could be compared. The radiation damage levels that correspond to a break-down in short circuit current could be determined as well as a correlation between onset of short circuit current degradation and thickness of device. This would provide further evidence that the theory of why ultra-thin solar cells have an intrinsic radiation tolerance proposed in this thesis is correct. Furthermore, satellite power systems could be tailored to specific mission profiles. The absorption of photons would be maximised and radiation tolerance maintained.

Chapter 7

Conclusions and future perspectives

7.1 Conclusions

A new design for ultra-thin single-junction GaAs solar cells has been demonstrated. A fresh look was taken at the design space available for III-V alloys that can be grown lattice matched to GaAs. Alloys with favourable band gap alignments were chosen as passivation layers and alignments were further optimised by adjusting doping densities. Drift-diffusion simulations were used to optimise both the absorber and passivation layer thicknesses and doping densities.

TLM studies were used to determine ideal contact layer doping densities and optimise the n-type contact metalisation anneal conditions. Since surface effects dominate in the ultra-thin regime, anneals were carried out at a reduced temperature and time to a standard thicker device to prevent diffusion of Au into the active layers. This diffusion can cause a degradation in the parallel resistance of the device. 2-diode model analysis of devices was used in conjunction with TLM analysis to balance the goal of low contact resistivities while avoiding Au diffusion.

On-wafer devices were electrically characterised and showed excellent J_{02} values indicating low amounts of recombination in the depletion region. An epoxy adhesive bonding method was then developed to remove devices from their growth substrate. For the first time, DTL patterning was used in a PV application to produce a periodic nanostructure on the back surface of the cell. This non-contact interference lithography technique showed great promise for patterning feature sizes on the nanoscale with high levels of uniformity and over significant topography. DTL is a wafer-scale technique and is therefore inherently scalable. AM0 efficiencies of 9.08% were achieved with 10% contact shading and no ARC. A feasible pathway to 16% AM0 efficiency was identified for these DTL patterned ultra-thin devices.

7.1.1 Improved diode behavior

The electrical characterisation of the ultra-thin devices in this study have shown improvements over previous cells in the literature. Table 7.1 shows the 2-diode model fitting parameters of the best performing DTL patterned off-wafer device. J_{02} values for this study are lower than previous ultra-thin devices in the literature and are in line with devices that are one and two orders of magnitude thicker. Series resistance values are decreased from previous 80 nm devices but are still larger than thicker devices which is an area of future improvement that could increase fill factors further.

Table 7.1 2-diode model parameters extracted from hero DTL device and comparison to other ultra-thin cells in the literature, *n_2 was constant for these devices.

	Thickness						
	Total (nm)	Absorber (nm)	J_{01} (mA/cm^2)	J_{02} (mA/cm^2)	n_2	R_{ser} (Ωcm^2)	R_{par} (Ωcm^2)
Kayes [34]	1000	-	6×10^{-18}	1×10^{-9}	2*	-	-
Chen [36]	330	205	2.8×10^{-17}	4.3×10^{-8}	2*	0.8	2.4×10^{3}
Hirst [6]	840	800	2.48×10^{-19}	7.71×10^{-9}	1.96	0.99	8.94×10^{7}
	120	80	1.74×10^{-18}	1.41×10^{-6}	2.70	13.23	3.77×10^{6}
This work [4]	120	80	2.67×10^{-18}	3.29×10^{-8}	2.01	2.01	3.60×10^{8}

7.1.2 Optimised front surface passivation

The use of InGaP as the window layer showed near ideal passivation properties. The use of this alloy for thin and ultra-thin cells is often overlooked because it is a direct bandgap material. However, in this study it was found that for the off-wafer devices with InGaP acting as the window layer, virtually all carriers produced in the layer were collected. This excellent passivation is evidenced in Figure 7.1 which shows the measured EQE and the calculated EQE from absorption in the InGaP and GaAs layers assuming 100% carrier collection efficiency for a planar Ag off-wafer device. There is a significant boost in the short wavelength light absorbed in the 20 nm InGaP layer in the off-wafer cell when compared to the on-wafer.

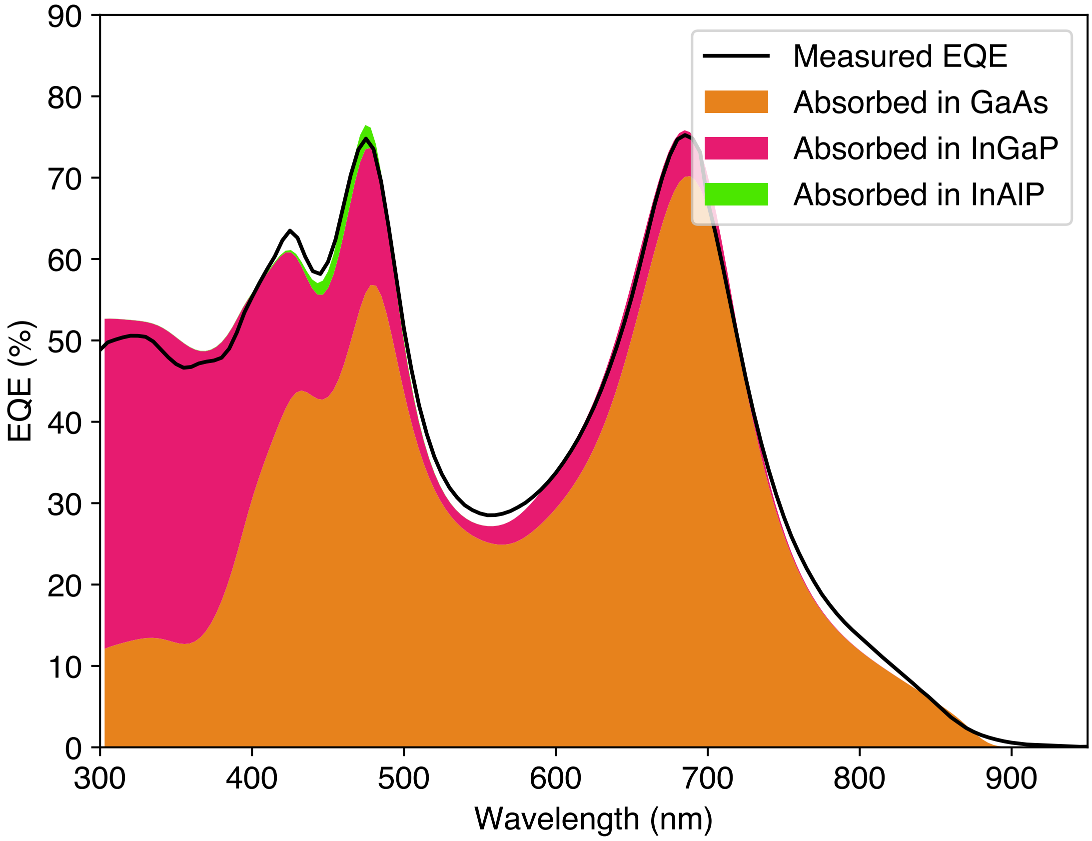


Fig. 7.1 EQE of on and off-wafer planar devices showing the boost in short wavelength absorption as a result of high quality passivation properties of InGaP as a window layer. Plot from [4].

7.1.3 Pushing the limits of high specific power

The benefits of reduced absorber layer thickness is only incremental for ultra-thin solar cells [35]. The true value of ultra-thin PV lies in their high performance in terms of specific power, radiation tolerance, high voltages achieved through light-trapping and potential for flexible form factors. Material savings could become significant if non-destructive epitaxial lift-off techniques are developed at scale that enable growth wafer re-use [100].

As shown in Figure 7.2, the major advance in this study is that 80 nm absorber layer devices are producing more power per unit area than traditional device length scales that are two orders of magnitude larger for the wide range of proton fluences tested. This is due to optimised ultra-thin layer design and successful integration of light management. The material savings of the thinner active layers is a marginal benefit but the radiation tolerance in the ultra-thin regime means significantly thinner coverglass can be used to shield the panels on orbit. This is a significant advantage for use in the space industry as the mass of coverglass over large solar arrays adds a significant amount to the cost of launching a spacecraft.

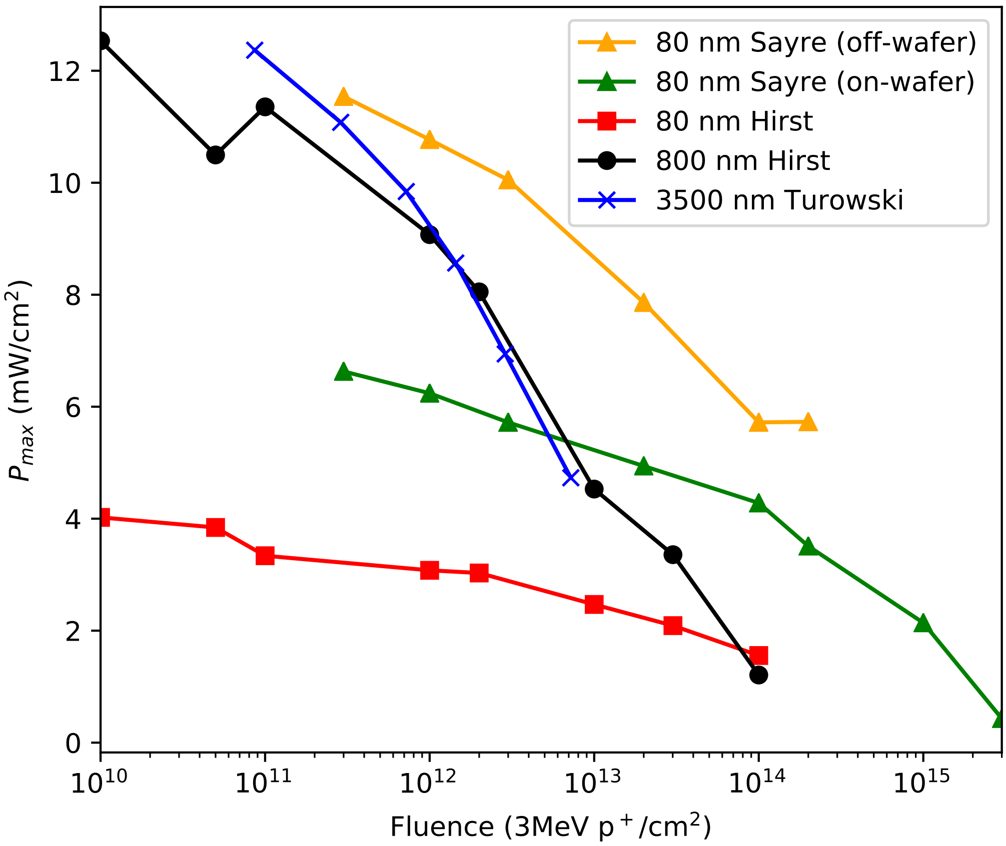


Fig. 7.2 Maximum power comparison for five different solar cell types [6, 7].

7.1.4 Superior radiation tolerance

Figure 7.3 shows the maximum power remaining factors for four solar cell types analysed in this study. Not only do the on-wafer devices (shown in green) show higher remaining factor than their thicker counterparts, but they also show significant improvement over previous 80 nm devices in the literature. At the relatively high fluence of 1×10^{14} p^+ cm^{-2}, 800 nm devices have degraded to 9.5% of BOL value and previous 80 nm devices have degraded to 36.9%. By contrast, the 80 nm on-wafer devices in this study are producing 60.1% of their BOL power.

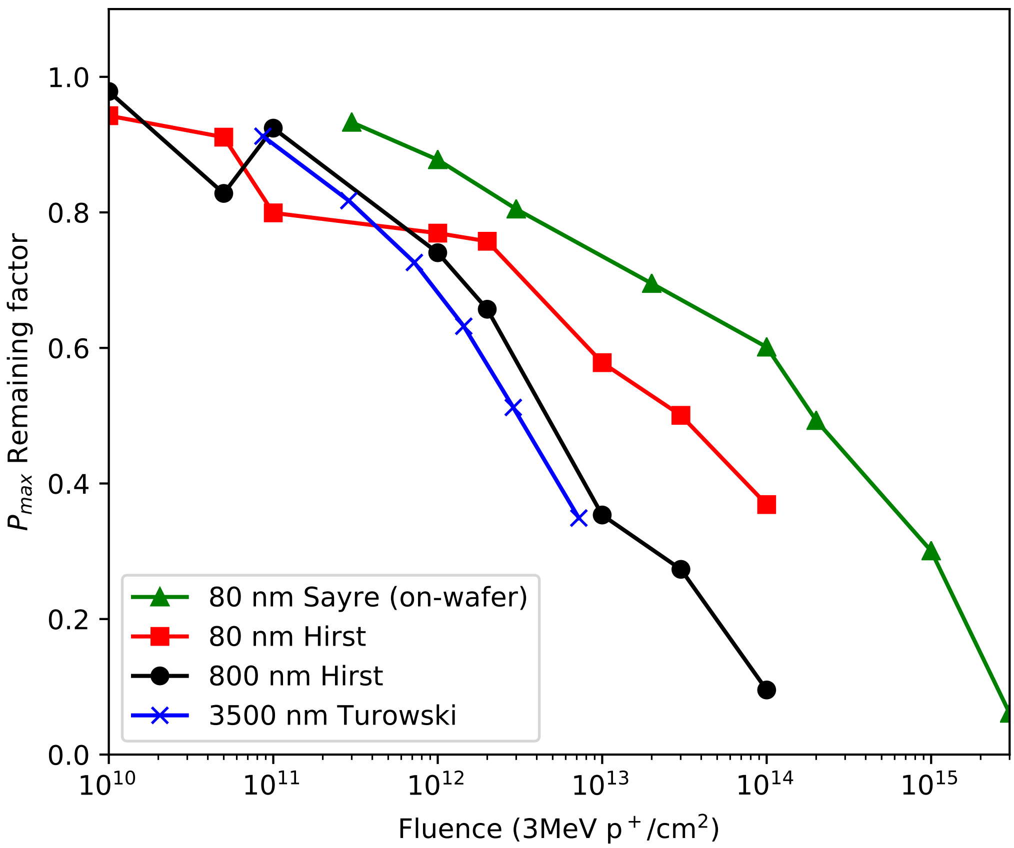


Fig. 7.3 Maximum power remaining factor comparison for four different solar cell types [6, 7].

7.1.5 Analysis of the effects of radiation-induced defects

Detailed CL analysis was carried out to correlate radiation-induced defects in the ultra-thin regime with carrier lifetime. This study presents the first evidence supporting the theory that ultra-thin solar cells show enhanced radiation tolerance because of a reduced distance for carriers to travel before being collected at contacts. By calculating the expected transit time for carriers across the junction after photogeneration, the damage threshold at which carrier lifetime drops below this transit time was compared to the point at which short circuit current began to degrade. There was good agreement between these points for the 3 MeV proton irradiated on-wafer cells with J_{SC} degradation beginning between 1×10^{15} to 1×10^{16} p^+/cm^2 fluence levels. This is the first experimental evidence that provides insight into the mechanism behind the intrinsic radiation tolerance of ultra-thin solar cells.

7.2 Future perspectives

7.2.1 Other applications

Beyond their use as power systems for spacecraft, ultra-thin cells have potential applications in a range of niche cases including Space-Based Solar Power (SBSP) projects [132–134], high altitude long endurance (HALE) airplanes [135, 136] and hot carrier solar cells (HCSC) [137–139]. They could also be a stepping stone to terrestrial electricity production from GaAs cells if reliable growth wafer re-use can be further developed to reduce the high costs of GaAs production and take advantage of the massive reduction in materials usage when moving from microns to hundreds of nanometers in absorber layer thickness.

SBSP has been proposed as a way to provide continuous baseload power through PV technology. This would mean placing panels in Earth orbit and beaming the energy they collect down to receiving stations on Earth. The arrays would need to be resistant to radiation over long periods of time to provide power to Earth receiving stations. Replacing panels in space would drive up project costs. The high specific power and intrinsic radiation tolerance of ultra-thin cells make them an interesting candidate for this emerging application.

High Altitude Long Endurance (HALE) airplanes are another potential application of ultra-thin GaAs solar cells. HALE aircraft are extremely lightweight solar and battery-powered unmanned aerial vehicles that operate at the upper regions of the Earth's atmosphere. They are of particular interest for defense and monitoring applications and have the advantage of being able to return to the Earth's surface regularly unlike Earth orbiting satellites. Flexible form factors, which ultra-thin solar cells can likely achieve, are particularly important for HALE aircraft since mounting over curved surfaces is essential to keep drag to a minimum.

Solar cells in the ultra-thin regime are also of interest to hot carrier solar cells (HCSC). Thermalisation and transmission losses make up the majority of the energy incident on any solar cell. Inventing a cell architecture that could harness this wasted energy and overcome the Shockley-Queisser limit would be of huge benefit to the cost-effectiveness of solar energy as we strive to achieve rapid uptake of solar energy world-wide . Ultra-thin solar cell research is a stepping stone towards achieving hot-carrier solar cells due to higher carrier densities achievable in such small volumes.

7.2.2 Nanophotonic structures for the ultra-thin regime

This thesis has focused on periodic metal-dielectric layers as the non-planar light-trapping structure to attempt to move beyond the double-pass absorption limit. It was shown that, during fabrication, if there is any deviation from the ideal structure, the performance of the patterned device can be significantly degraded. Quasi-random patterning has been proposed as a potential alternative to the tight fabrication tolerances that need to be achieved for successful integration of periodic light-trapping layers [39].

Quasi-random structures are optimised to couple light to guided modes that lead to total internal reflection. Low-cost and scalable patterning techniques such as polymer blend lithography have already shown significant promise when integrated as light management layers in thin cells [43]. These are an interesting future avenue for integration with electrically optimised ultra-thin device designs such as those designed in this thesis.

7.2.3 Tailoring the ultra-thin solar cell design to future space missions

By designing a range of ultra-thin devices with varying absorber layer thicknesses (100 nm, 110 nm, 120 nm etc.) and exposing them to the same fluences of damaging radiation, the thresholds at which short circuit current degradation begins could be determined for each device thickness. This would facilitate the design of devices that have the maximum thickness, and therefore increased light absorption, that still maintains high radiation tolerance and no degradation in output current up to a specific fluence that is tailored to the individual space mission.

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Appendix A

Displacement damage dose calculations

Displacement damage dose calculations

Table A.1 Non-ionising energy loss values for Ga, As and GaAs for protons at 3, 50 and 70 MeV. Values are from literature [11].

Energy (MeV)	NIEL value (MeV cm^2/g)		
	Ga	As	GaAs
3	2.04×10^{-2}	1.97×10^{-2}	2.00×10^{-2}
50	4.19×10^{-3}	4.04×10^{-3}	4.12×10^{-3}
70	3.90×10^{-3}	3.73×10^{-3}	3.82×10^{-3}

From the 50 and 70 MeV NIEl values, a linear interpolation was used to calculate the 68 MeV value, 3.85×10^{-3} MeV cm^2/g. This value and Equation A.1 below were then used to calculate the equivalent fluence values in Figure 5.4.

$$\Phi_e = \frac{\mathrm{D}}{\mathrm{NIEL}} \tag{A.1}$$

Where Φ_e is the equivalent fluence in cm^{-2}, D is the displacement damage dose in MeV/g and NIEL is the non-ionising energy loss value in MeV cm^2/g.

Appendix B

Modelling the radiation environment during spacecraft missions

This appendix details the specific parameters used to simulate on-orbit radiation conditions for ultra-thin cells. Four orbits were considered: LEO orbit used by Starlink, GEO, HEO/Molniya, and a Europa lander concept.

Orbit generation

Spacecraft trajectories were defined using the built-in SPENVIS tool [77]. For circular Earth orbits (LEO and GEO), an altitude value and inclination define the orbit. For elliptical Earth orbits (Molniya and other HEOs), inclination along with perigee and apogee or semi-major axis and eccentricity need to be defined. The four main orbits investigated and presented in Chapter 5 are detailed here.

- LEO: The Starlink "first shell" orbit was used for this mission. The orbit has an altitude of 550 km and an inclination of 53.0° [8].

- GEO: The geostationary orbit modelled in this thesis has an altitude of 35,786 km and a longitude of 0 [140].

- Molniya: A standard Molniya orbit was used with perigee of 717.74 km, apogee of 39.750 km, semi-major axis of 26,553 km, eccentricity of 0.737, argument of perigee of 270° and an inclination of 63.4° [9].

- Europa: The orbit of Europa around Jupiter was modelled to illustrate the radiation environment that a lander to the surface of the Jovian moon would experience. The parameters used are a semi-major axis of 671,100 km, an eccentricity of 0.0094 and an inclination of 0.47° [141].

Simulating satellite missions

Missions were all assumed to begin on January 1st 2025 at 12 am to ensure fair comparison of proton and electron fluxes. Consistent choice of time period ensures the fluctuations in radiation fluxes due to solar maximums and minimums does not affect the comparison of orbits.

Different radiation models have been developed over the years as more and more data is collected about the radiation environments in space. The most up to date AP9/AE9 [75] models were used to analyse the radiation fluxes for Earth orbits. JOREM [76] was used to model the Europa orbit.