MODELLING AND DESIGN OF DIAMOND POWER SEMICONDUCTOR DEVICES

Nazareno Donato

St Edmund's College

University of Cambridge

Department of Engineering

This dissertation is submitted for the degree of Doctor of Philosophy

July 2019

DECLARATION

This dissertation is the result of my own work and includes nothing which is the outcome of work done in collaboration except as declared in the Preface and specified in the text. It is not substantially the same as any that I have submitted, or, is being concurrently submitted for a degree or diploma or other qualification at the University of Cambridge or any other University or similar institution except as declared in the Preface and specified in the text. I further state that no substantial part of my dissertation has already been submitted, or, is being concurrently submitted for any such degree, diploma or other qualification at the University of Cambridge or any other University or similar institution except as declared in the Preface and specified in the text. It does not exceed the prescribed word limit for the relevant Degree Committee.

In accordance with the Department of Engineering guidelines, this thesis contains approximately 45,000 words and 106 figures.

The work presented in this dissertation was carried out in the Department of Engineering, University of Cambridge, during the period January 2016 to July 2019 under the supervision of Professor Florin Udrea.

Nazareno Donato

St Edmund's College, Cambridge

July 2019

MODELLING AND DESIGN OF DIAMOND POWER SEMICONDUCTOR DEVICES (ABSTRACT)

Nazareno Donato

With its remarkable electro-thermal properties such as the highest known thermal conductivity (~22 W/cm· K at room temperature) of any material, high hole mobility (>2000 $cm^2/V{\cdot}s$), high critical electric field (>10 MV/cm), and large bandgap (5.47 eV), Diamond has overwhelming advantages over Silicon and wide bandgap semiconductors (WBG) for ultra-high voltage and high temperature applications (>3 kV and >450 K, respectively). However, despite its tremendous potential, fabricated devices based on this material have not yet delivered the expected high-performance. This is due to three main reasons: (i) the lack of consistent physical models and design approaches specific to diamond-based devices that could significantly accelerate their development; (ii) the absence of shallow acceptor and donor dopant species which has resulted in poor room temperature performance; (iii) the technological issues of the manufacturing process. With the principal aim of modelling the next generation of diamond devices, this Ph.D dissertation endeavours to numerically model the main electro-thermal properties of diamond devices for power electronic applications. Optimized unipolar mode diamond field effect transistors have been designed by means of finite element simulations and their performance has been assessed against the state-of-the-art diamond FETs. Particular attention is given to the static and dynamic properties of deep dopant levels and their effects in WBG semiconductor-based devices. Moreover, by means of a more global comparison technique and through accurate theoretical analysis, diamond FETs and diodes' performance have been projected and compared with that of GaN and SiC devices. This work concludes with possible implementations of diamond devices in power converters and provides a roadmap of diamond devices for power electronics. These promising results give a new impetus to the rather small, but growing diamond community and enable future research in the field with the goal of bringing diamond to the commercial world.

To my family: Elvira, Mariano and Stellamarina

Per aspera sic itur ad astra

ACKNOWLEDGEMENTS

First of all, I would like to thank the EPSRC scholarship for supporting me financially while undertaking this Ph.D. work.

I would like to give special thanks to my supervisor Prof. Florin Udrea for his enthusiasm, unfailing and valuable support and professional guidance during this Ph.D.

I am also grateful to my advisor Prof. Gehan Amaratunga for his help and advices.

My sincere thanks also go out to all the member of the High Voltage Microelectronics and Sensors lab and the Camutronics team for their constant support and for creating a friendly and enjoyable environment.

I would like to thank all my friends and in particular Luca, Dario, Valerio, Gianluca, Gennaro, Giovanni for their valuable friendship.

A special acknowledgment goes to my girlfriend Bethan for her support, encouragement and patience during the preparation of this dissertation.

Finally, I would like to thank my loving and unique family and in particular my mum for her reassurance and constant support during all these years.

CONTENTS

LIST OF FIGURES

LIST OF TABLES

1 INTRODUCTION

1.1 Power devices and circuits: a brief introduction

Power semiconductor devices are electronic switching devices used in electrical power conversion, conditioning and control circuits. Since the introduction of solid-state devices in the 1950s and their wide spread in industrial and consumer applications, the power semiconductor business has been growing steadily with an increasing impact on the economy.

In 2016, the global market of power semiconductors (including discrete components, power ICs and modules) increased by 3.5% from 2015, reaching a revenue of $35.1 billion[1]. The map of power device applications as a function of frequency of operation and power capacity is illustrated in figure 1.1. The power devices field is currently dominated by silicon-based devices. This is because silicon (Si)-technologies are very mature and currently offer the best trade-off between performance and cost. The optimization of the design of Silicon based transistors alongside the technological progress in the fabrication and quality control have allowed Insulated Gate Bipolar Transistors (IGBTs), Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs), Superjunctions and thyristors to dominate applications where there is the need for either high power but low frequencies or low to medium power and relatively higher frequencies.

Nevertheless, there exists a huge variety of applications in the medium- to high- power (e.g. automotive sector, satellite communications, high speed trains, mobile terminals) where Si-based devices are not able to deliver efficient solutions due to ON state and switching losses and poor thermal dissipation management [2]. Besides, Si-devices are fast approaching their theoretical limits [3].

The increasing demand for a low carbon and energy efficient society has raised the need for new technologies for power electronics applications. In this context, new classes of materials namely wide bandgap (WBG) and ultra-wide bandgap (UWBG) semiconductors have been researched to quantify their advantages in terms of efficiency, device area, heatsink and passive filter volume reduction, radiation hardness and switching frequency compared to Si devices [4-6].

While GaN and 4H-SiC devices have been successfully commercialized and also demonstrated to outperform their Si-based counterparts [7, 8], diamond still faces a number of challenges which are hindering the full exploitation of its potential[9].

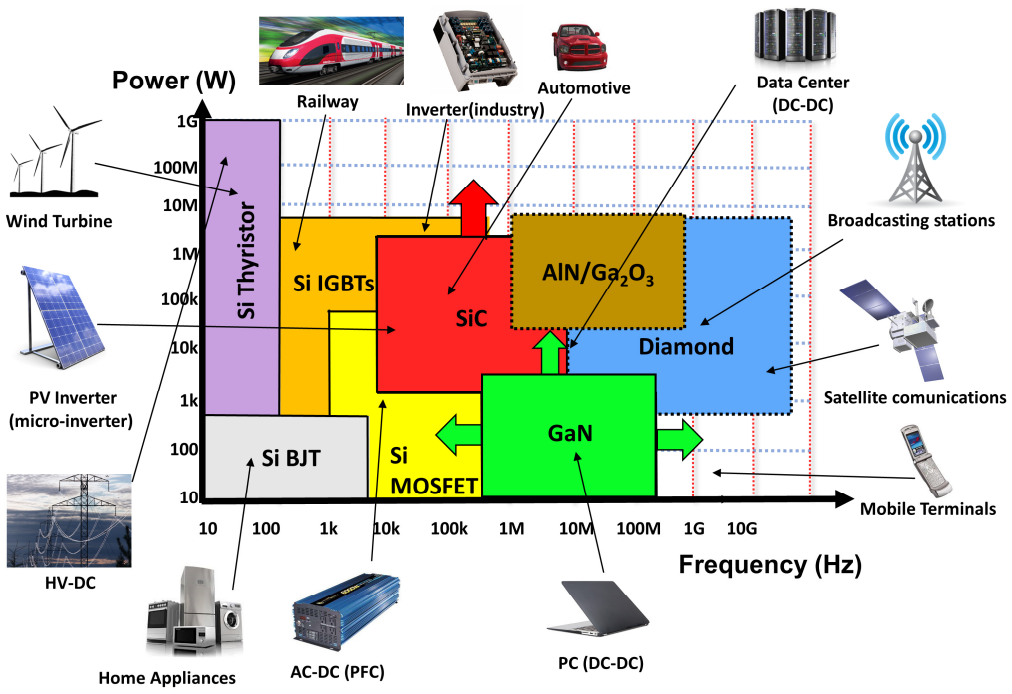


Figure 1.1: Applications for power devices in the power versus frequency domain. Arrows show the possible evolution of each material. Dashed regions represent non-commercial materials (to date).

1.2 Wide and Ultra-wide Bandgap semiconductors: properties, and benefits

In the last three decades wide bandgap and ultra-wide bandgap semiconductors materials have been investigated for power applications due to their better physical properties among which, higher critical electric field and carrier mobility. A full picture of the physical properties of WBG and UWBG is given in table 1.1 where one can clearly note the advantages of these materials when compared to silicon.

Table 1.1. Material properties of silicon, WBG and UWBG semiconductors for power applications.

Material			WBG			UWBG		
		Silicon	4H-SiC	GaN		Ga_2O_3	Diamond	AlN
Bandgap (eV)		1.1	3.3	3.4		4.9	5.5	6.1
Critical Electric Field (MV/cm)*		0.3	2.8	3.5		8	7.7-20	10
RT Mobility (cm^2/Vs) *	**electron**	1500	1000	2000 (2DEG)	>1000 (bulk)	300	1060	300
	hole	480	120	<100 (2DHG)	<200 (bulk)	14	2100 (bulk)	<300 (2DHG)	14
Thermal Conductivity (W/mK)		150	370	100(on Si) 165(on Shappire) 253 (on GaN)		11-27	2200 - 2400	253-319
Relative permittivity (a.u.)		11.8	9.8	9		9.9	5.5	8.5
Substrate diameter(inch)**		8-17.7	8	8		4	<1	2
Substrate Dislocations (per cm^{-2})		<10	10^2	10^4		10^4	10^4-10^6	10^4
Saturation velocity (x10^7 cm/s)	**electron**	1	1.9	2.5		2	2.5	1.4
	hole	0.8	1.2	----		-----	1.4	
Built-in Voltage (V)***		0.6	2.8	2.9		----	4.9	--
n-type dopants		available	available	available		available	moderate	moderate
p-type dopants		available	available	available		not available	Available	poor
Commercial devices		MOSFETs IGBTs Diodes Thyristors BJTs	Diodes BJTs MOSFETs	HEMTs		--	---	--

* Critical electric field and mobility are assumed to be doping independent. Smaller ionization coefficients are specific to the wide-bandgap materials and this results in higher critical electric field.

** Typical size.

*** Calculation assumed constant doping for both sides of the junction ($1x10^{15}$ cm^{-3}), room temperature conditions and bandgap values which can be found in the table 1.1.

One of the main criteria that can be used to assess materials for power applications is the trade-off between breakdown voltage (BV) and specific ON state resistance (R_{on_spec}).

This has been plotted in figure 1.2, based on the material properties reported in table 1.1. One can clearly see that at room temperature 4H-SiC and GaN have the best BV/R_{on_spec} trade-off when compared to silicon technologies including Si-superjunction and IGBTs. The smaller R_{on_spec} for the same BV enables the reduction in wafer area which in turn, translates into lower input capacitance and higher switching frequency. In particular, GaN devices can benefit from the extremely high channel electron mobility (2000 $cm^2/(Vs)$) and input capacitances as low as tens of pF that allow them to efficiently switch at high frequencies (>500 kHz) and consequently reduce the size of the passive components in the power system [10].

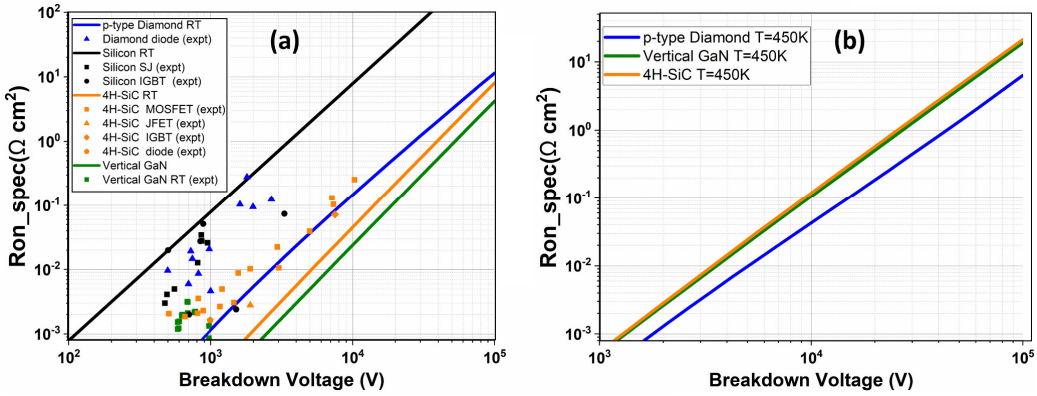


Figure 1.2: Vertical R_{on_spec} vs BV unipolar limit for semiconductors and comparison with experimental results at room temperature (T=300 K) (a) and for high operating temperature (T=450 K) (b). The calculated limit is the result of an optimization procedure which assumes PT profile for the electric field, mobility function of temperature and doping, temperature dependent breakdown field for 4H-SiC (calculated by means of the ionization integral) and the incomplete ionization in the case of p-type diamond. Silicon RT is used as reference considering a constant critical electric field (table 1). As it can be noted, boron doped diamond (p-type diamond) shows a better trade-off only for high temperature (b). Data taken from[11-21] and references therein.

Moreover, diamond shows superior performance (compared to GaN and SiC) only at higher junction temperature due to the enhanced boron activation.

1.2.1. Silicon Carbide (SiC)

Due to the easy doping control and processing, 4H-SiC Schottky diodes devices have been already commercialized in 2001 by Infineon [22] which have recently released the 5th generation of CoolSiC diodes with a maximum reverse voltage of 1.2 kV and an ON state current up to 40 A [23]. 4H-SiC Schottky diodes have been mainly adopted in power converters due to their remarkable 'zero reverse recovery' losses. In addition, the availability of a native oxide for SiC enabled the first mass production of 4H-SiC power MOSFETs in the 600 V range by ROHM in 2010 [24], immediately followed by the first commercial 1.2 kV 4H-SiC MOSFET from Cree [25] and by several similar devices from other semiconductor companies. State-of-the-art commercial 4H-SiC power MOSFETs range from 650 V/1.7 kV – 50 A domain to 3.3 kV (expected for the next generation [26]). 5 kV and 10 kV 4H-SiC Power MOSFETs are now in research with spectacular results. This is however an area where large area IGBTs and even larger area thyristors are very well established and difficult to displace. R&D is also pushing towards the fabrication of bipolar 4H-SiC devices (such as BJTs, IGBTs and Thyristors) which will offer more benefits compared to 4H-SiC unipolar devices for high voltage ratings (>10 kV) [27, 28]. Furthermore, recent reliability studies on the stability of the threshold voltage in 4H-SiC MOSFET under negative and positive bias temperature instability (NBTI and PBTI) tests [29, 30], have illustrated how metal oxide semiconductor-based 4H-SiC commercial devices may still not represent the best solution for harsh environments and fast switching operations.

1.2.2. Gallium Nitride (GaN)

A few years after the research in vertical 4H-SiC devices started, lateral power devices based on AlGaN/GaN heterostructures have been announced and subsequently undergone extensive development. Their main advantage is related to their piezo-polarization nature that allows the formation of a high carrier density layer, the so-called two-dimensional electron gas (2DEG), at the AlGaN/GaN interface without any intentional doping in the structure [31]. The main transistors based in GaN are HEMTs (high electron mobility transistors) with variations in the gate structure to obtain enhancement mode operation that leads to technologies such as the p-GaN gate [32]

and GaN-based MISFETs (Metal-insulator-semiconductor FETs) [33]. GaN transistors are characterized by high carrier density (~1×10^{13} cm^{-2}), high mobility (>2000 $cm^2/(Vs)$), high critical electric field (3.5 MV/cm) and can reach extremely high frequency of operation (>500 kHz), thus enabling compact and lighter power systems. GaN power devices have been first made commercially available in 2010, about 17 years after their first experimental demonstration [34, 35]. Today, GaN enhancement-mode HEMTs are available on the market for 100 V [36], 600 V [37], 650 V [38] and a 900 V depletion-mode is also available [39]. Although GaN devices are very promising candidates for the next generation of power devices in the 650 V applications, their lateral configuration limits the maximum handling power capability to a few kW. Scaling to higher breakdown voltages without compromising the wafer area is not immediate due to their lateral configuration.

An approach towards the optimization of the lateral voltage blocking capability is the multi-level field relief structures proposed in [40-43]. GaN is compatible with several substrates: 4H-SiC, sapphire, Si, and most recently GaN-on-diamond is also being investigated. However, the most attractive solution from a cost point of view is that based on a silicon substrate that allows not only the use of low-cost silicon wafers and established semiconductor foundries, but also paves the way to monolithic integration of circuit components including gate drivers (as achieved by [44]). Nevertheless, reliability issues associated to trap-states at the surface [45], in the bulk GaN active layers and in the AlGaN-based stress-relief-layer grown on Si [46-48], have slowed down the adoption of these transistors.

A few technologies claim no trap-related reliability [49, 50] but significant research effort is still on-going to solve the bulk-related issues. In principle, vertical GaN devices on GaN substrates would allow for a better current extraction and increase in the total power handling capability with the additional benefit of a more linear scaling of the ON state resistance (R_{on}) with the BV. Both transistors and diodes have been demonstrated in vertical GaN configuration with a BV up to 5 kV for diodes [51, 52] and up to 1.6 kV for MOSFETs [53-55]. However, several issues, such as the material cost, quality of the thick GaN layers, and the availability of larger wafers need to be addressed prior the commercialization of vertical GaN technology.

1.2.3. Gallium Oxide (β-Ga_2O_3)

On the horizon, new materials named UWBG semiconductors would offer enhanced properties in terms of critical electric field, switching speed and low leakage current compared to 4H-SiC and GaN. Such UWBG power devices would result in ON state losses similar or lower than those of bipolar Silicon or unipolar WBG devices, while and at the same time, drastically reducing the switching losses thanks to the lack of stored bipolar charge [56] or smaller capacitances. β-Ga_2O_3 benefits from some interesting properties which could be exploited in unipolar mode devices [57, 58]. Its intriguing electrical properties and the affordable cost of the substrates (similar to GaN) make this material one of the future candidates for power electronic applications. Nevertheless, on one hand, its intrinsic low thermal conductivity has usually resulted in heteroepitaxial grown devices in which thermal issues are less severe compared to the homoepitaxial solutions. On the other hand, the lack of a controllable and efficient p-type doping, has restricted the number of topologies to only n-type doped (In_2O_3, SnO_2 and ZnO) unipolar mode devices [59]. Lately, intrinsic majority hole conduction has been discovered to exist in nominally undoped β-Ga_2O_3 [60, 61], when compensation by background native donors is reduced. Depletion mode FETs (MESFETs and MOSFETs) have been fabricated showing a record breakdown voltage of 2.3 kV and 1 A in the forward state [62], while Schottky diodes have shown to exhibit more than 1 kV of breakdown voltage thanks to an accurate field plate design [63].

1.2.4. Aluminum Nitride (AlN)

AlN is another attractive UWBG material for high power and temperature applications. Typically used as a nucleation layer in lateral GaN HEMTs, this material exhibits high critical electric field, high thermal conductivity of 319 $Wm^{-1}K^{-1}$ at room temperature and a wide band gap of about 6.1 eV (see table 1.1). AlN allows to overcome some of the issues related to the graded buffer layers needed for the fabrication of III-V materials on Si substrate (like GaN HEMTs). Moreover, the good thermal conductivity of AlN improves the heat dissipation capability of current GaN devices. AlGaN HEMTs with high Al composition [64], 1 kV vertical Schottky Si-doped AlN diodes

[65] and >2.5 kV n-type AlN MESFET have been successfully manufactured in the past few years [66]. To date, some of the main technological concerns are related to the difficult conductivity control of AlN layers and the expensive price for bulk AlN substrates.

1.2.5. Diamond

Diamond has distinctive advantages when compared with other UWBG semiconductors, due to its high hole-electron mobility, critical electric field, the highest known thermal conductivity and the widest bandgap [67, 68]. It has also peculiar features such as electron emission and surface transfer doping for hydrogen terminated surfaces. Recent breakthroughs have demonstrated efficient chemical vapor deposition (CVD) doping techniques for both p-type and n-type dopant species and relatively large area high pressure high temperature (HPHT) and CVD substrates [69]. Nevertheless, substrates are still limited in terms of cost and availability, and the resistivity of diamond layers is affected by the partial ionization of the dopants. In spite of this, several devices with high ON state current (up to 10 A [70]), fast switching performance [71] and high breakdown voltage (>2 kV) without any field relief structure [21] have been manufactured. Although the future commercialization of such devices seems to be limited only to niche applications (mainly high power, frequency and temperature), some new key improvements in the substrate growth and device' fabrication route may enable the use of diamond devices in a wider range of applications.

1.3 Outline of the thesis

In **Chapter 2**, the physics and the material properties of semiconducting diamond are presented in detail. Particular attention is paid to the properties of diamond in the context of power electronics applications. Defects, substrate growth and classification, carrier mobility and several other crucial physical mechanisms are also addressed. A thorough description of the TCAD modelling of diamond devices is presented. **Chapter 3** presents a systematic review of the applications and current state-of-the-art

of diamond while highlighting the issues that still need to be addressed prior to commercialization. This chapter concludes with a review of the state-of-the-art field relief design terminations in diamond and a careful analysis of the packaging, reliability' issues and thermal management challenges for diamond electronics.

The design and modelling of unipolar mode diamond JFETs and deep depletion MOSFET is studied in **Chapter 4**. The effect of several peculiar properties of diamond, such as the incomplete ionization effect, is addressed and deeply investigated by means of finite element simulations. The static and dynamic effects of the incomplete ionization of the dopants in diamond and other WBG semiconductor-based devices are examined in **Chapter 5**. The equations governing this complex physical mechanism are reviewed and described in detail. The static effects of the partial ionization have been analysed with reference to a classic 1D p-n junction and by monitoring the profile of majority carriers in the device. Dynamic effects which lead to charge imbalance in superjunction devices and kink in the CV curves of metal-oxide-capacitor (MOS) device are also investigated.

Chapter 6 aims to assess the limits of the figure of merits for power electronic devices with respect to diamond devices and suggests an alternative approach to compare diamond and other WBG semiconductor devices. Additionally, a theoretical comparison between diamond Schottky diodes and bipolar PIN diodes is carried out for different voltage ratings, temperature and switching frequencies. Finally, a suggested roadmap to a market-ready diamond power technology concludes this chapter.

Chapter 7 concludes this thesis and addresses the future research plan.

2 PHYSICS AND TCAD MODELLING OF SEMICONDUCTING DIAMOND

2.1 Introduction

The remarkable electrical and physical properties of diamond have often led to extensive research efforts in developing electronic devices based on it. A scientific community has formed which considered diamond as the semiconductor material for the future generation of power electronic devices.

This chapter takes a closer look at the analysis of the material properties of semiconducting diamond and their physical modelling for finite element simulations' tools.

The first part of this chapter focuses on the specific techniques to improve the doping efficiency and control, the unique properties arising from surface termination, the heterojunction structures and the carrier mobility for diamond.

The second part concentrates on computer based-simulation tools and discusses in detail the most significant physical models and parameters for diamond devices.

2.2 Material requirements

Diamond can be defined as "a perfectly ordered disposition of carbon atoms"[72]. More specifically, at the microscopic scale, diamond is made of two face centred cubic (FCC) cells which are displaced along the body diagonal by a quarter of their diagonal length. Additionally, each carbon atom in the structure is covalently bonded with other 4 neighbours' atoms. The strong covalent bonds make diamond an almost perfect thermal material with a high value of thermal conductivity. Moreover, the elevated energy required to separate carbon atoms in a diamond lattice makes diamond the hardest material available on Earth.

Despite the fact that diamond gemstones can be found in nature, synthetic diamond for electronic applications is usually fabricated in laboratories. The synthesis of diamond requires the accurate control of pressure and temperature to avoid graphitization. As can be seen in figure 2.1, different pressure and temperature conditions are needed for CVD and HPHT diamond growth. Additionally, the availability of a wafer (usually an HPHT one) is required for the CVD growth.

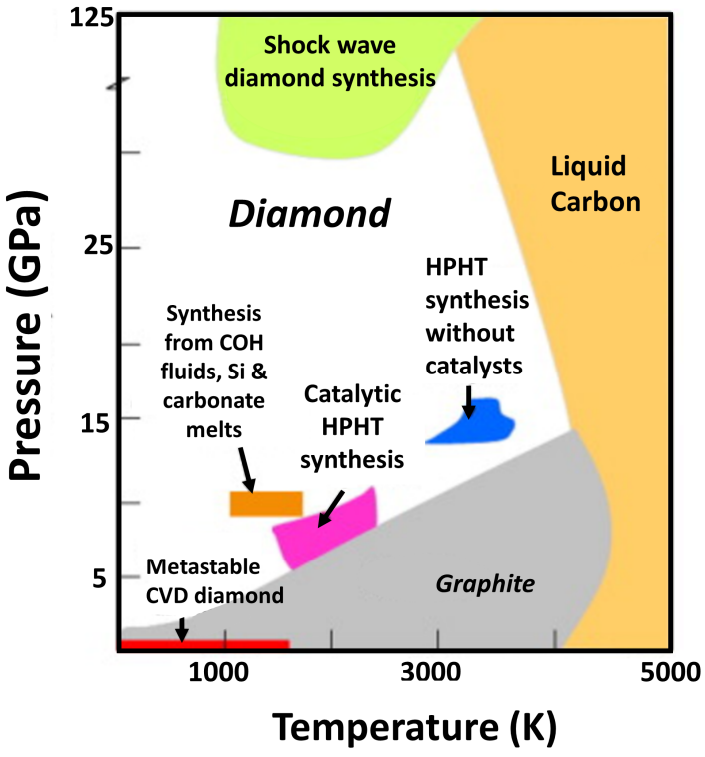


Figure 2.1: Carbon phase diagram. CVD diamond is metastable, and graphitization can occur at ~1700 K and for high pressure conditions. Picture reproduced from [73].

The performance of diamond electronic devices depends heavily upon the crystalline quality of the HPHT or CVD substrates on top of which the devices are fabricated. The dislocations density and the total area of the substrate determine the performance such as the maximum available current in the ON state, the BV as well as the level and the origin of the leakage current. Therefore, assessing the quality of the substrate upon which several other diamond layers are grown is a critical step.

2.2.1. Substrates and growth

Diamond crystals are usually classified on the basis of the type of impurities concentration (nitrogen and boron) and their arrangement in the crystalline structure. An accurate classification of diamond crystals can be found in table 2.1 and it applies to both natural and synthetic diamonds (HPHT or CVD). The HPHT technique for the realization of synthetic diamond substrates allows to achieve high purity with a low defect density but the total size is normally restricted due to intrinsic limitations of this method. HPHT substrates used for electronic devices are usually type Ib due to their relatively low cost and low dislocations density of about 10^5 cm^{-2}, but type IIa substrates can achieve even lower dislocations density ($<10^3$ cm^{-2}) with drawbacks in terms of complex fabrication process and cost.

Table 2.1. Classification of Diamond crystals based on the type and amount of impurities. Impurities are usually measured with IR techniques.

<table>
<tr><th colspan="3">Diamond Substrates</th></tr>
<tr><td rowspan="3">Type I
It has enough Nitrogen concentration (0.3%-0.5%) which can be measured with Infrared (IR) spectrometry.</td><td rowspan="2">Type Ia
Nitrogen (N) atoms replace Carbon (C) atoms in the lattice (N atoms are in substitutional lattice sites) and they tend to aggregate together.</td><td>Type IaA
A specific type of Ia with N atoms pairs which occupy neighboring lattice site.</td></tr>
<tr><td>Type IaB
Cluster of 4 substitutional N atoms symmetrically surround a vacancy in the lattice structure.</td></tr>
<tr><td colspan="2">Type Ib
N atoms replace C atoms in the lattice, but they are isolated from each other. A great part of HPHT diamond substrates is type Ib.</td></tr>
<tr><td rowspan="2">Type II
It is characterized by a low Nitrogen concentration which cannot be detected with IR. (usually $<10^{17}$ cm^{-3})</td><td colspan="2">Type IIa
Very low Boron and Nitrogen concentration which makes this form one of the purest diamond crystals available. Diamond gemstone can be included in this category.</td></tr>
<tr><td colspan="2">Type IIb
Boron concentration is higher than nitrogen. It has p-type semiconducting properties.</td></tr>
</table>

Commercially available HPHT substrates can be found in 2x2 mm^2 up to a maximum value of 10x10 mm^2 for IIa HPHT which has been recently commercialized by NDT Russia [74].

CVD growth has less limitations on the size of the substrate, despite the fact that it does not achieve the same crystalline quality of HPHT technique. Currently, microwave plasma CVD (MPCVD) and hot filament CVD (HFCVD) are the two main techniques for growing diamond layers. However, there exists more than 10 different ways to obtain CVD growth. Commercially available CVD substrates are currently available from E6, Sumitomo and several other companies and their size can reach up to 0.5 inch. Over 2 inches CVD substrates can be found in a mosaic configuration but the bonding boundaries between the wafers can restrict the electrical characteristics of the devices and increase strain and defects in the structure [75]. An alternative technique to homoepitaxial growth is the heteroepitaxial growth of diamond on Iridium (Ir) and other similar substrates [76, 77]. This process allows to reach over 3 inches substrates but the high number of dislocation density (10^7-10^9) needs to be addressed prior the fabrication of high-performance electronic devices on such substrates.

Conversely, as diamond devices can exhibit better electrical performance (i.e. current density, BV, switching speed, etc.) compared with other semiconductor-based devices, small area substrates could still represent an attractive solution which will allow to simultaneously reduce the overall price per Ampere and avoid the dicing price of large area substrates. These key features will be examined in greater detail in chapter 6.

2.2.2. Doping and defects in diamond

When compared to other semiconductors, diamond is characterized by a much more complex doping process. As an example, due to the peculiar lattice structure and material strength, only shallow doping profiles (<10 nm) can be obtained by means of high energy ion implantation process [78, 79] . Recently, thermal doping diffusion has been proven and a diamond p-n diode based on this doping technique has been fabricated and characterized [80, 81]. However, this technique requires further investigations prior to becoming a reliable method for fabricating diamond devices. Therefore, the incorporation of substitutional dopant species during the growth of

diamond layers still leaves some open issues and it is mainly realized simultaneously with the CVD growth. Low boron concentrations (10^{15} cm^{-3}) are relatively easy to implement but fabrication of thick doped p-type layers remains challenging due to the loss of the crystallinity. While boron forms an acceptor level at 0.38 eV from the maximum energy level of valence band (Ev), nitrogen and phosphorus n-type dopants result in a much deeper energy level with the respect to the minimum energy level of the conduction band (1.7 eV and 0.57 eV from Ec, respectively). Nitrogen which can be also found in a great variety of diamond substrates has the advantage of having a similar radius to Carbon and therefore does not introduce strain and stresses in the diamond lattice. However, its high activation energy makes these dopants practically unsuitable for electronic applications both for the low dopant efficiency and for the slow dynamics of the carriers. Growth of phosphorous doped diamond layer ensures the lower resistivity for n-type layers but it requires high and controlled temperature during the whole growth process [82]. Though it is possible to obtain a relatively wide doping window, heavy n-type (>$5x10^{19}$ cm^{-3}) doping still remains challenging (table 2.2) [83]. Several other dopant species such as Li, Na and As have been investigated in the literature as potential shallow dopant candidates for diamond. If these dopant species occupied substitutional positions in the lattice, they would allow for a lower ionization energy (0.1 eV,0.3 eV and 0.4 eV, respectively). Unfortunately, the donor-like behavior was only confirmed for arsenic (As) which, unfortunately, requires a more complex doping process than the classical incorporation during the CVD growth.

In addition, the crystal orientation also plays a key role in determining the quality of the doped and intrinsic layers. <100> orientation is the most common one for growing diamond layers, but it is still complicated to grow n-type layers and there are still limitations in the efficiency of p-type doping. Conversely, in the <111> directions n-type phosphorous dopants can be incorporated much easier and it is possible to achieve one of the highest concentration of boron [84]. Nevertheless, one of the significant drawbacks of the <111> orientation is the formation of macroscopic defects which leads to a poorer quality of the material [85]. On <110> faces boron concentration can be improved if compared with <100> but the reduced surface area hampers the benefits due to the enhanced doping control. Other orientations like <113> which have not been deeply investigated, may result in enhanced control and speed for the doping process of diamond layers. Macroscopic and microscopic defects are also playing a key role in

determining the properties of diamond electronic devices [86, 87]. Non epitaxial crystallites, which are a typical feature of homoepitaxial grown diamond, have already been demonstrated to affect the performance of MESFET and Schottky diamond diodes [88-90]. Contaminants which propagate during the growth of the drift layer and originate from the diamond substrate can indeed modify the Schottky barrier uniformity [91, 92] and lead to enhanced leakage current. It has been proven that diodes with a larger active area typically characterized by an increased number of defects which leads, in turn, to higher leakage currents [93-95]. Improved and controlled growth conditions have also shown a reduction of non-epitaxial crystallites in SBDs [96].

Table 2.2. Available doping windows for the doping of diamond electronic devices.

	Available		**Under development / required**	
	min	***max***	***min***	***max***
N-type doping concentration	~ $3x10^{15}$ cm^{-3}[97]	~ $8x10^{19}$ cm^{-3} [98]	~$1x10^{14}$ cm^{-3}	>$1x10^{20}$ cm^{-3}
N-type layer thickness	<100 nm [97, 99]	~ 5µm[82]	<1nm	>50 µm
P-type doping concentration	~ $1x10^{15}$ cm^{-3} [100]	>$1x10^{21}$$cm^{-3}$ [101]	< $1x10^{14}$ cm^{-3}	>1e21 cm^{-3}
P-type layer thickness	<10 nm	~ 100µm [101]	<1nm	>200 µm

Shockley type dislocations are known to be responsible for lifetime killing in SiC bipolar devices. They limit the scaling of drift layers for power electronics applications and similar effects may also be present in diamond. However, the effect of atomic scale defects such as dislocations and planer defects on the device' performance is still under investigation and still not well understood for diamond layers. Characterization techniques such as cathodoluminescence (CL), Electron beam induced current (EBIC), Raman spectroscopy and X-ray topography are typically performed for the estimation of diamond defects. For a complete review of diamond defects and their characterization techniques, the reader can refer to [102].

2.2.3. Device and surface termination

The surface termination of diamond layers has a crucial impact on the electro-chemical properties of the final devices. The termination creates new electronic states which

have different properties when compared to the bulk. Among the key aspects, the presence of surface electronic states inside the bandgap may give rise to Fermi-level-Pinning (FLP) effects and to surface dipoles which can vary the electron affinity of the diamond semiconductor.

2.2.3.1. Oxygen termination

Oxygen termination is generally used to improve the adhesion of oxide and diamond layers and it induces a positive electron affinity (PEA) of 1.7 eV. One of the main drawbacks of such passivation is the high FLP effects generated by the presence of high density interface states which can affect the electrical properties of metal oxide semiconductor (MOS) structures fabricated on such layers [103], as it will be discussed in chapter 3. Ozone treatment and immersion in hot mixed acid are the most common treatments adopted by researchers to induce O-termination in diamond layers [104].

Several species (C=O, C-OH, C-O-C, C-O-O-C) can be formed at the surface during the oxygen termination depending on the treatment and the method adopted. Oxygen terminated (O-terminated) diamond is also exploited for the removal of the hole-type conductive layer which is generated at the hydrogen terminated diamond surface and for the passivation of diamond layers [21].

2.2.3.2. Hydrogen termination

On hydrogen terminated (H-terminated) diamond surfaces, both a negative electron affinity (NEA) of > -1 eV and a strong FLP are induced [105, 106]. Diamond H-terminated surfaces, which can be obtained by either hot filament or plasma treatment, have been widely explored due to their unique property of surface conductivity. Even though the origin of surface conductivity is still not well understood, the presence of adsorbates on C-H diamond surface and the local exchange of charge with the diamond valence band is the most likely explanation for the formation of the 2DHG. Recently, 2DHG has been demonstrated on C-H surfaces passivated with Al_2O_3 oxide [107]. As the adsorbates are removed with in-situ technique, the origin of the 2DHG on passivated C-H surfaces is probably induced by negative charging of the unoccupied levels such as Al vacancies or oxygen point defects, as discussed in [108]. One can

also note that these properties have been also presented with polycrystalline diamond [109] or heteroepitaxial grown diamond [110].

2.2.3.3. Heterojunctions with Diamond

Among the possibilities which allow to obtain at room temperature (RT) fully activated diamond channel, heterojunctions of diamond and group III nitrides (AlN, GaN and BN) are among the most promising and attractive configurations. As the growth of GaN layers on diamond surfaces is complicated, AlN and BN have been identified as the key materials for diamond heterojunctions. Kuech et al. [111] reported an H-terminated diamond surface with an AlN passivation layer and the first demonstration of a AlN/diamond heterojunction np diode was successfully carried out by Miskys et al. [112] by using a MBE (Molecular Beam Epitaxy) technique. As the H-terminated surface results in a poor attachment to the AlN layer, an O-terminated diamond surface was adopted for the first AlN/Diamond heterojunction FET realized by Imura et al. [113, 114] with a metal organic vapor phase epitaxy technique. The calculated hole density profile reached its peak of about $3.6x10^{18}$ cm^{-3} at about 1.5 nm from the heterojunction interface and good carrier confinement was demonstrated. The hole sheet density integrated by depth from 0 nm to 7 nm (with the origin at the diamond/AlN interface) is evaluated to be 1.2×10^{11} cm^{-2}.

2.2.4. Bulk and surface mobility

Carrier mobility is one of the key parameters for semiconductor-based electronic devices. It describes the relationship between the carrier velocity and the electric field. In diamond, several measurements and studies have been performed in order to estimate the value of hole/electron mobility and the principal scattering mechanisms. The different techniques implemented for the diamond mobility measurement are typically classified in optical excitation measurements (such as time-resolved cyclotron resonance (TRCR) and time-of-flight (TOF)), Hall measurements of CVD diamond layers and indirect measurements from FETs characteristics. Discrepancies between the TRCR,TOF and Hall measurements have generated confusion about the

real value of diamond carrier mobility with overestimations for hole and electron mobility at RT (7300 $cm^2/(Vs)$ for electron and 5300 $cm^2/(Vs)$ for holes [115]). However, recent measurements tend to agree on the RT values for electron/hole mobilities [116, 117].

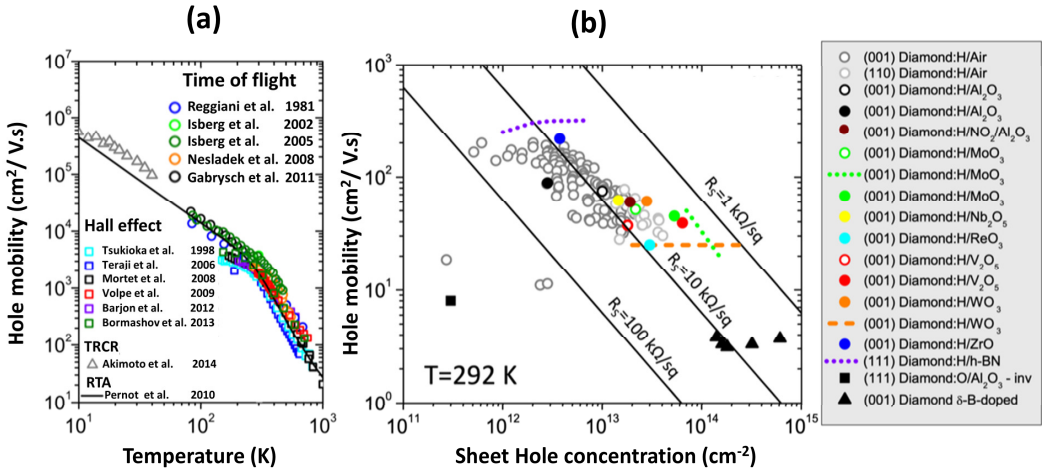


Figure 2.2: (a) Hole mobility vs temperature for bulk diamond (experimental and theoretical) for low boron concentration $<1x10^{16}$ cm^{-3}. The gray rectangle corresponds to typical room temperature 2DHG mobility in diamond FET, (b) Hole mobility for H-terminated diamond FETs, O-terminated diamond FETs and delta B-doped diamond. Data from [118] (references therein) and [119].

Regarding the electron mobility in n-type layers, intra-valley phonon scattering with a $T^{-a(T)}$ (with a(T)>2) dependence is dominating the high temperature range (regardless of the doping level of the layer) while the interaction with the intra-valley acoustic phonon is the main scattering mechanism in the middle temperature range with a $T^{3/2}$ dependence [118, 120]. In the low temperature range, ionized impurity and neutral impurity scattering with a $T^{3/2}$ and no temperature dependence, respectively, are the main mechanisms affecting the electron mobility of diamond. In detail, as the high activation energy of boron and phosphorous doped diamond layers results in a low ionization ratio at RT (especially for medium-highly doped layers), a great part of the dopant atoms is electrically neutral and their scattering with electrons cannot be neglected like in Silicon or other low bandgap materials. Hall electron mobility values calculated at RT oscillate around 1000 $cm^2/(Vs)$ whilst TOF performed by Isberg et al.[121] shows higher electron mobility, an overestimation which may be caused by the approximation of Hall scattering factor, as suggested by Pernot [118].

On the other hand, while hole mobility is subjected to the same scattering mechanisms in the low temperature range, intra-band and inter-band acoustic phonon scattering are

dominating the medium range and the interaction with the optical phonon is the main mechanism responsible for the mobility at high temperature (HT). Some discrepancies between TOF, TRCR and Hall measurements still persist with values ranging between 3800 $cm^2/(Vs)$ and 2100 $cm^2/(Vs)$ at RT with a tendency of measurements to confirm the 2100 $cm^2/(Vs)$ value [118, 122] (figure 2.2(a)).

Such mobility values can be reached in pure or low doped diamond, where the limiting mobility mechanism is purely intrinsic due to phonon scattering mechanisms. In some power devices, moderately doped and highly doped material will be needed in order to perform active layer or contacts. In that case, the impurities will be the limiting process of the mobility. Detailed analysis of the mobility dependence versus doping level concerning phosphorus doped n-type [120] and boron doped p-type [123-125] materials have been reported. In uncompensated and highly doped material, the neutral impurity scattering is the dominant scattering mechanism because of the large ionization energy of the donor and acceptor dopants.

Few studies have analyzed the mobility in hydrogen terminated diamond surfaces. In general, extraction of the conductivity (carrier sheet density and mobility) is obtained during the electrical characterization of the 2DHG FETs. Besides, values of surface channel p-type channel FETs rarely exceed 200-300 $cm^2/(Vs)$ due to surface roughness, ionized impurity scattering, and the high surface electric field generated by the presence of the negatively charged acceptors which are causing the confinement of the 2D hole gas (figure 2.2(b)). Recently, Li et al.[126] calculated the 2DHG mobility as function of the temperature and the hole gas density and then compared their theoretical results with a variety of experiments. The extracted data showed that the surface impurity scattering mechanism controls the mobility of 2DHG for a significant temperature and hole density range while the high temperature mobility is affected by the nonpolar optical phonon scattering.

Mobility extraction has also been performed on delta doped FETs showing that the predicted enhanced mobility in such layers cannot be achieved and values rarely overcome 20 $cm^2/(Vs)$ [127]. On C-OH diamond surfaces, the mobility of the inversion layer on lateral MOSFET have been estimated to be 8 $cm^2/(Vs)$ due to the non-optimal quality of the diamond/Al_2O_3 oxide interface [128]. Another effect which needs to be addressed in order to fully capture diamond device' properties is the

mobility of minority carriers (i.e. electrons in p-type layer and holes in n-type layer) which will be crucial in determining the properties of bipolar mode devices.

2.3 TCAD tools and challenges

This section aims to address the main physical models and parameters used for the finite element simulations of oxygen and hydrogen terminated diamond devices based on the most recent experimental results.

2.3.1. Physical models for oxygen terminated diamond

2.3.1.1. Literature review

Finite element modelling of diamond devices finds its roots in the early work of Shin et al. [129] in which a diamond p-type MESFET was simulated and compared with GaAs MESFETs for RF applications. Successively, Kawakami, Aleksov, Tsugawa et al. [130-133] used finite element simulations to investigate the current distribution and the temperature profile in p-i-p type diamond metal–insulator–semiconductor field effect transistors , JFETs and delta doped FETs. In these early works, the finite element simulations were only employed to extract trends rather than for confirming experimental results or analysis and they mainly included a constant value for mobility, activation energy and the other critical parameters. Only in the works of Brezeanu et al. and Rashid et al. [72, 134-136] a more systematic and reliable approach for technology computer aided design (TCAD) simulations of oxygen terminated diamond power devices can be found. A compact model for the doping and temperature dependent mobility, which was fitted from TOF measurements of Isberg et al. [121, 137], and an advanced model for the partial activation of the dopants were both included in the simulation deck. In addition, a set of temperature independent impact ionization coefficients and the main values for electron affinity and bandgap were included to perform the finite element simulations. This set of parameters was able to correctly match a series of diamond Schottky metal-insulator-p-type (MIP) diodes with different geometries and Schottky metals and, concurrently, to predict the electric field evolution with planar and ramp field plate terminations in diamond Schottky MIP diodes. A variable series resistance was added in order to simulate

interface effects, imperfections and the 300 μm-thick p+ substrate. Nawawi et al. [138-140] optimized the matching technique proposed by Rashid et al. and included a more complete set of parameters for incomplete ionization, high field effect mobility, a new set of breakdown voltage coefficients and also an interface layer (between diamond and the Schottky metal) which was able to explain the peculiar temperature behavior observed by Rashid et al. for some MIP diodes. Nevertheless, new mobility and impact ionization measurements and the discovery of some specific phenomena such as the hopping conduction mechanisms (not negligible at low temperatures and for high doping concentration (see section 2.3.1.2)) resulted in a modification and an overall refinement of the previous set of TCAD parameters. Marechal et al. [141] implemented those new models in order to reproduce the behavior of a diamond p-n diode junction. The hopping mobility was included in the finite element simulations and correctly allowed to estimate the value of the additional parasitic resistance which was required for an accurate matching of the I-V characteristics of the diode' characteristics. Several other works attempted to include more accurate physical models also for the generation-recombination process, leakage current mechanisms and for a temperature dependent impact ionization set of coefficients [142-145]. Despite the incomplete ionization, high and low field mobility, hopping mobility, effective mass and bandgap models have been improved during the last decade, the lack of a compact model for the generation and recombination process and for the impact ionization still remains a major issue for the matching and prediction of oxygen terminated diamond device characteristics. Furthermore, as the variations of the process usually impact the electrical performance of the final devices with the creation of multiple defects, non-uniform Schottky barrier, interface and bulk traps, it is impossible to find a unique set of parameters and physical models able to exactly match and predict the performance of all the oxygen terminated diamond devices. Therefore, while some of the main models (i.e low field mobility, bandgap, incomplete ionization, hopping mobility) can be considered identical in all the simulations, other coefficients and physical models (such as avalanche, recombination, leakage current) need to be adjusted to the specific process via a "matching technique" prior the simulation of new and optimized diamond power device structures. Such a matching technique mainly involves the fitting of the main static and dynamic device electrical characteristics (such as threshold voltage, breakdown voltage, saturation current, inductive and resistive switching waveforms etc.).

2.3.1.2 TCAD modelling

The finite element analysis and simulations of diamond devices require the availability of a Technology computer aided design (TCAD) software. This category of software allows to predict the behaviour of semiconductor-based devices based on the resolution of the Poisson and current equations. To provide numerical solutions, both the equations and the semiconductor device are discretized (finite element approach). The device structure is usually discretized with a triangular mesh and the "box discretization method" is employed for the resolution of the semiconductor equations. The commercially available tool used in this study is Sentaurus from Synopsys, which also allows to simulate opto-mechanical properties and includes a process simulation tool. Despite the fact that diamond is still not defined in the material database of this commercially available software, a custom parameter file with the physical models defined in this section has been developed. As it has already been mentioned, several other models and parameters not defined and addressed in this chapter (i.e. lifetime, leakage mechanisms, etc.) are still subject to discussion and are usually adjusted depending on the specific device structure.

Bandgap and DOS

In semiconductor devices, a significant number of electrical properties are determined by the value of the bandgap and the definition of the density of states in the valence and conductance band. Diamond is a semiconductor with an indirect bandgap in which the bandgap is defined as the energy difference between the minimum conduction band energy level at the X-point and the maximum valence band energy at the Γ-point of the Brillouin zone. The bandgap (E_G) and its temperature (T) dependence have been modelled as in equation (1), with the set of parameters from table 2.3. α and β are fitting parameters.

$$E_G(T) = E_G(300\ K) + \alpha\frac{T_0^2}{\beta+T_0} - \alpha\frac{T^2}{\beta+T} \quad (1)$$

Table 2.3. Parameters used for fitting equation (1) with the experimental results in [146](see fig. 2.3)

Symbol	E_G(300 K)	T_0	α	β
Unit	eV	K	eV K^{-1}	K
Value	5.47	300	0.033	1e5

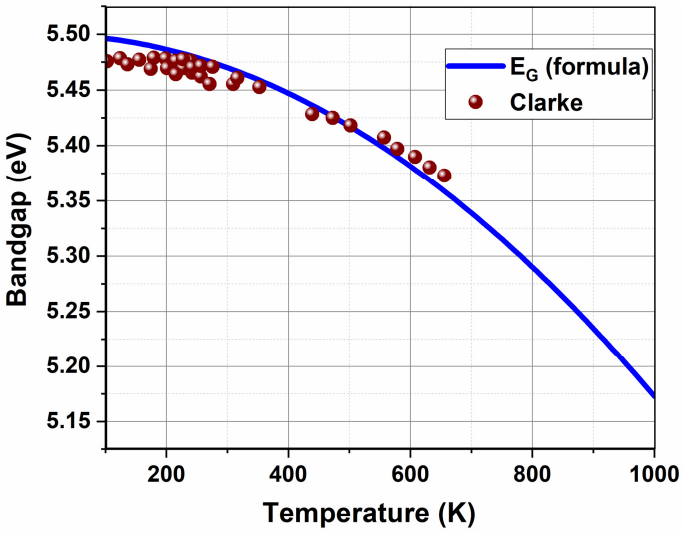


Figure 2.3: Diamond bandgap vs temperature and its comparison with the results from Clark et al.[146].

The formula defined by (1) is in good agreement with the experimental results reported by Clark et al. in 1964 [146] (see figure 2.3). Strictly connected to the energy-momentum band structure is the definition of effective mass for electron and holes. In the hypothesis of parabolic approximation, the effective density of states for both the conduction and the valence band (N_C and N_V, respectively) can be defined as a function of the electron and hole effective mass, respectively as in formula (2a-b). In (2a-b) m_e^* (m_h^*) is the effective electron (hole) mass, k is the Boltzmann constant and h is the Planck constant.

$$N_C = \frac{2(2\pi m_e^* kT)^{3/2}}{h^3} \tag{2a}$$

$$N_V = \frac{2(2\pi m_h^* kT)^{3/2}}{h^3} \tag{2b}$$

The electron (m_e^*) and hole (m_h^*) effective mass are function of the crystallographic orientation and can be defined as in equations 3(a-d) (parameters can be found in table 2.4). m_{hh}^*, m_{lh}^* and m_{so}^* are the values of the hole effective mass in the heavy hole, light hole and spin orbit band under the assumption of the three-valence parabolic band structure. These value are averaged along the <100> and <110> directions according to [125, 147]. For electrons the spin-orbit is assumed negligible and the effective mass can be calculated as in (3d), where $m_\perp$ and $m_\parallel$ are the electron transvers and longitudinal mass, respectively.

$$m_{hh}^* = \left[m_{hh}^{<100>}\left(m_{hh}^{<110>}\right)^2\right]^{1/3} \tag{3a}$$

$$m_{lh}^{*} = \left[m_{lh}^{<100>}\left(m_{lh}^{<110>}\right)^{2}\right]^{1/3} \quad (3b)$$

$$m_{h}^{*} = \left[m_{hh}^{*\,3/2} + m_{lh}^{*\,3/2} + m_{so}^{*\,3/2}\right]^{1/3} \quad (3c)$$

$$m_{e}^{*} = \left[m_{\perp}^{2} \cdot m_{\parallel}\right]^{1/3} \quad (3d)$$

Under this approximation, and by using coefficients from [148], the equations (2a) and (2b) can be simplified as in (4a-b), in which $N_{V0} \sim 2e10^{19}$ cm^{-3} and $N_{C0} \sim 5x10^{19}$ cm^{-3}.

$$N_V = N_{V0}\left(\frac{T}{300K}\right)^{3/2} \quad (4a)$$

$$N_C = N_{C0}\left(\frac{T}{300K}\right)^{3/2} \quad (4b)$$

Table 2.4. Parameters for equation 3(a-d). References included in the table.

	Electrons		Holes				
Reference	$m_{\perp}$	$m_{\parallel}$	$m_{hh}^{<100>}$	$m_{hh}^{<110>}$	$m_{lh}^{<100>}$	$m_{lh}^{<110>}$	m_{so}^{*}
Naka [148]	0.28	1.56	0.54	0.7	0.288	0.255	0.375
Willatzen [149]	0.34	1.5	0.427	0.69	0.366	0.276	0.394

With the effective density of states defined as in (4a-b), the intrinsic carrier concentration (n_i) is uniquely determined defined as shown in (5). Figure 2.4 shows the intrinsic carrier concentration for diamond and its comparison with other semiconductors. The parameters for Silicon and 4H-SiC have been extracted from [150].

$$n_i = \sqrt{N_V N_C} \cdot \exp\left(-\frac{E_G}{2kT}\right) \quad (5)$$

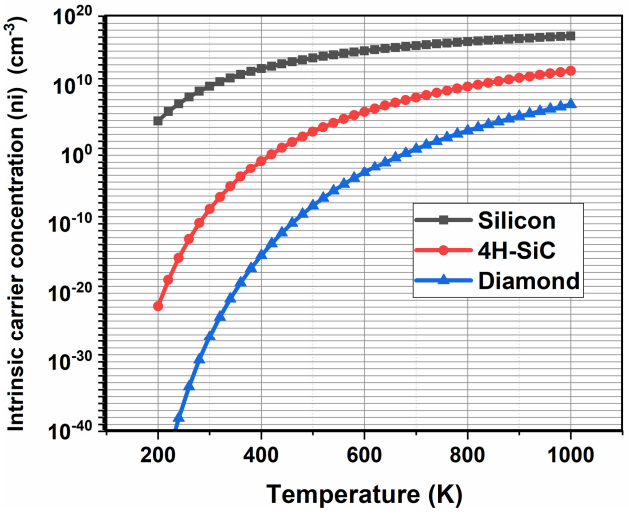


Figure 2.4: Intrinsic carrier concentration(n_i) as function of the temperature for different semiconductors.

Mobility

Recent Hall effect measurements for hole and electron mobility [123] have been successfully implemented in Sentaurus TCAD with the Arora Model [150, 151] (see figure 2.5). This mobility model (6a-c) takes simultaneously into account the temperature, the doping dependence, and different values of compensation doping. The values of the parameters for holes and electrons adopted in the set of equations (6) are available in [141] and are also reported in table 2.5. In equations 6(a-c), $N_{imp}=N_{A0}+N_{D0}$ is the total level of impurities. N_{A0} and N_{D0} represents the compensation level concentration for n-type and p-type layers, respectively. In 6(a-c), $\beta_{min,max}$, N_β , γ_β , γ_μ , N_μ are fitting parameters.

$$\mu(T, N_{imp}) = \mu(300, N_{imp}) \cdot \left(\frac{T}{300}\right)^{-\beta(N_{imp})} \quad (6a)$$

$$\mu(300, N_{imp}) = \mu_{min} + \frac{\mu_{max}-\mu_{min}}{1+\left(\frac{N_{imp}}{N_\mu}\right)^{\gamma_\mu}} \quad (6b)$$

$$\beta(N_{imp}) = \beta_{min} + \frac{\beta_{max}-\beta_{min}}{1+\left(\frac{N_{imp}}{N_\beta}\right)^{\gamma_\beta}} \quad (6c)$$

Table 2.5. Parameters for equations 6(a-c)) taken from [141].

Symbol	β_{min}	β_{max}	N_β	γ_β	μ_{min}	μ_{max}	N_μ	γ_μ
Unit	----	----	cm^{-3}	---	cm^2 /Vs	cm^2 /Vs	cm^{-3}	----
Hole	0	3.11	4.1e18	0.617	0	2016	3.25e17	0.73
Electron	0	2.17	3.75e17	0.585	0	1030	9.9e16	0.564

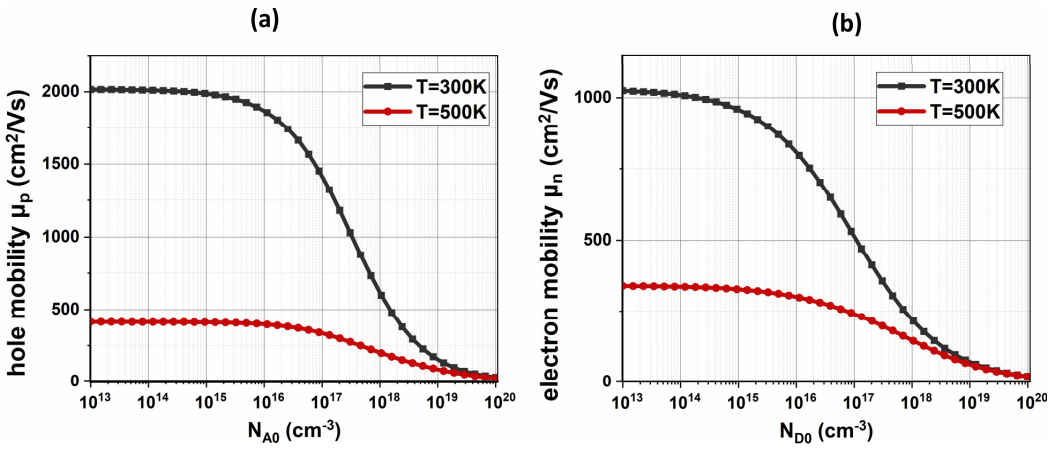


Figure 2.5: Hole mobility vs doping for boron (a) and phosphorous (b) doped diamond for T=300/500K.

Incomplete ionization

The wide bandgap (and the small dielectric constant) of diamond results in the formation of deep levels for donors and acceptors (see section 2.2.2). The equations and parameters for the incomplete ionization of the dopants have been extensively defined and discussed in chapter 5. The electro-thermal balance equation which can be solved in the scenario of the Fermi-statistics[152, 153] has been plotted in figure 2.6 for boron doped diamond at different operating temperature and for different compensation ratios and doping concentration. For nitrogen doped and phosphorous doped diamond, similar equations and plots can be derived.

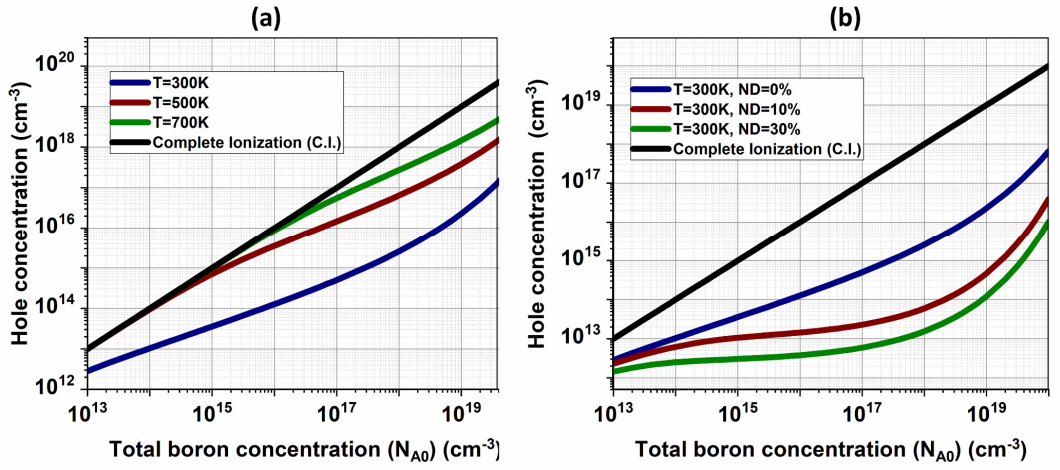


Figure 2.6: (a) Active boron dopants at the thermodynamic equilibrium vs total boron concentration for T=300 /500/700 K and (b) effect of different compensation levels (N_D=N_{D0}) on the boron activation at T=300 K. For the formulas used in the calculation, refer to chapter 5.

High field saturation

Under the influence of high electric field (E), the mobility degradation can be modelled through the high field saturation model based on Canali model and on the Caughey Thomas Law (equation 7 and figure 2.7) [39].

The reduction of the saturation velocity(v_{sat}) at high temperature has been modelled as in equation (8). In the literature, the saturation velocity of carriers in CVD diamond which has been determined by means of Monte-Carlo simulations and experimental measurements, have exhibited a significant variation from 0.96×10^7 cm/s up to 2.3×10^7 cm/s [2], [40]. In this thesis, we assumed $v_{sat,0} = 2\times10^7$ cm/s [41] and b = 6, where the coefficient b has been adopted as a fitting parameter for the high temperature

transfer curve of the normally-on JFETs (chapter 4). In equations 7-8, v is the carrier velocity, α and β are fitting parameters.

$$v(E) = E \cdot \mu(E) = \frac{E \cdot (\alpha+1)\mu(T,N_{imp})}{\alpha + \left[1 + \left(\frac{(\alpha+1)\cdot E \cdot \mu(T,N_{imp})}{v_{sat}}\right)^{\beta}\right]^{1/\beta}} \quad (7)$$

$$v_{sat} = v_{sat,0}\left(\frac{300K}{T}\right)^{b} \quad (8)$$

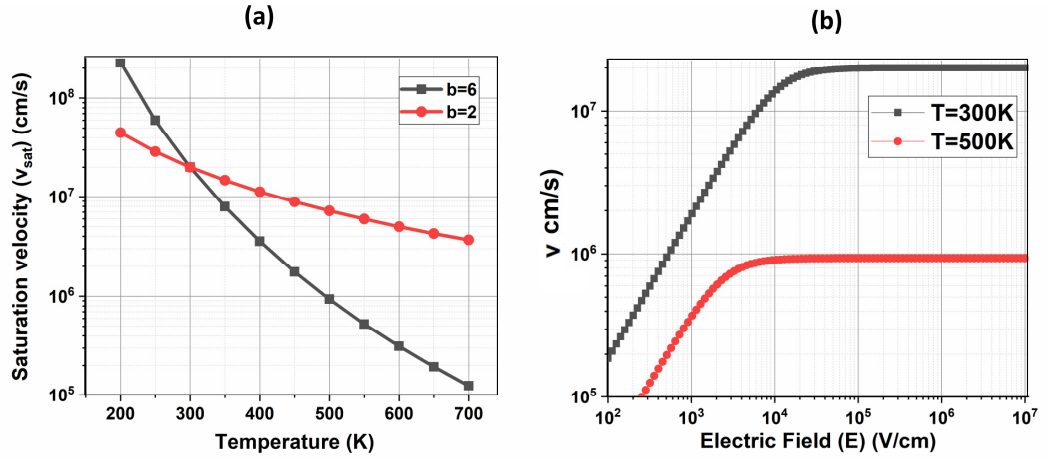


Figure 2.7:(a) Saturation velocity vs temperature for different b exponent (equation 8) and (b) equation (7) plotted for different temperatures in case of boron doped diamond with $N_{imp}=N_{A0}=1e16cm^{-3}$.

Hopping mobility

For high doping level (below the metal-insulator transition) and for low temperature, hopping conduction dominates the conduction mechanism in both boron doped and phosphorous doped diamond layers. Different types of hopping conduction occur for boron and phosphorous doped diamond. More specifically, in nearest neighbor hopping (NNH), occurring for phosphorous doped diamond, carriers are transported by tunneling among a single dopant level. Conversely, in variable range hopping (VRH), occurring for boron diamond, carriers are transported inside a dopant band originated by the wave function overlapping of dopant levels (figure 2.8). The equations and the parameters for electron hopping mobility have been defined in (9a-d) and table 2.6. One can note that as the activated phosphorous concentration (N_D) is needed for such a calculation (and not the total doping level N_{D0}), the computation of (9) requires a more complex implementation in the finite element simulator. This could be obtained by means of the physical model interface (PMI) with the definition of a dedicated C-based language code for the hopping mobility(μ_{hop}). The runtime

resolution of equations 9(a-d) can usually lead to convergence issues of the TCAD simulations, and therefore, it will be neglected unless specified in this manuscript. In formulas 9a-d, $n_{hop}=N_{D0}-n_B$, where n_B is the electron concentration in the conduction band, σ_n is the conductivity of the n-type layer, μ_{eq} is the equivalent mobility of the n-type layer, μ is the bulk mobility, R_{hop} is the hopping tunnelling length, v_{ph} is the phonon scattering probability, α is electronic wavefunction overlap parameter, W_{hop} is the hopping activation energy.

$$\sigma_n = q\left(\mu\, n_B + \mu_{hop}\, n_{hop}\right) \tag{9a}$$

$$\sigma_n = q\,\mu_{eq} n_B \tag{9b}$$

$$\mu_{eq} = \mu + \frac{n_{hop}}{n_B}\mu_{hop} \tag{9c}$$

$$\mu_{hop} = \frac{1}{6}\frac{qR_{hop}^2}{kT} v_{ph}\left(-2\alpha R_{hop} - \frac{qW_{hop}}{kT}\right) \tag{9d}$$

Table 2.6. Parameters for equations 9(a-d) taken from [141].

Symbol	R_{hop}	α^{-1}	v_{ph}	W_{hop}
Unit	cm	nm	s^{-1}	10^{-3} x eV
Value	$\sim N_{D0}^{-1/3}$	1.8	2e11	51

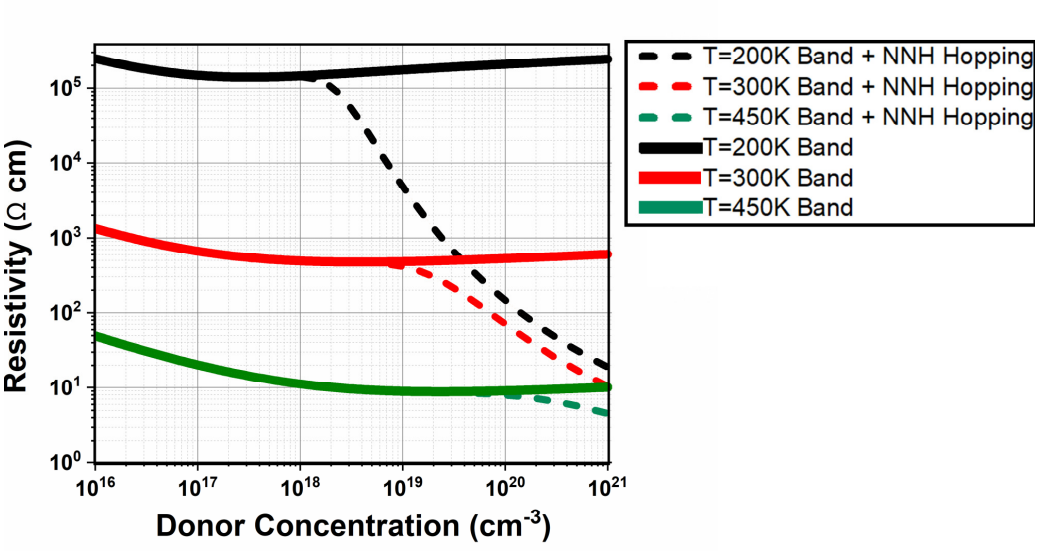


Figure 2.8: Simulated resistivity vs doping concentration for a diamond n-type layer at different operating junction temperature.

2.3.2. Physical models for hydrogen terminated diamond

2.3.2.1 Literature review

Despite the numerous works on the subject, the nature of the 2DHG in H-terminated diamond structures is still controversial. TCAD simulations of HFETs have been mainly based on two different models for the implementation of the two-dimensional hole gas in the structure (figure 2.9). One of the first models proposed by Tsugawa et al. [130] called as "surface acceptor model" "(fig.2.9(a)) consisted in an ultra-thin (0.2 nm) highly doped p-type layer (10^{20} cm^{-3}) where full activation of acceptors was considered. This model was able to effectively reproduce the exponential 2D distribution of holes, typical of H-terminated diamond FETs. In the same work, Tsugawa also introduced a "diffused acceptor model", in which holes were three dimensionally distributed from the surface according to a Gaussian profile. The diffused acceptor model was able to reproduce the formation of some 2DHG in which the hole density peak was located at a certain depth from the surface region (~20nm). Successively, Oishi, Fu, Zhou [154-157] included the surface acceptor model to match experimental HFETs devices and to explain the unusual double transconductance peak occurring in HFETs. Recently, Kawarada et al. [108] successfully reproduced the behavior of HFETs by adopting a second model for the 2DHG formation, named "charge sheet model"(fig.2.9(b)). This model was already known in the literature and it allowed to correctly estimate and reproduce the characteristics of AlGaN/GaN FETs by means of a positive sheet of fixed charge. Such charges which were generated by interface polarization were able to create a 2DEG at the AlGaN/GaN interface. Similarly, the inclusion of negative fixed charges at the diamond/oxide interface (such as diamond/Al_2O_3) is able to accumulate a 2DHG at the interface even at zero bias. Nevertheless, despite the fact that the charge sheet model allowed for an easier and more physically sounded modelling (2DHG might be formed by the presence of negatively charged sites near the interface), some of the HFETs characteristics could not be matched. For this reason, Wong et al. [158] introduced a double charge sheet model "(fig.2.9(c)) in order to simultaneously match the transfer characteristics, the ON state current and the Hall measurements for such devices. In detail, an additional layer of negative charge is sandwiched between the oxide and the interfacial layer, which could be formed during a non-ideal hydrogen surface termination. Fu et al. [159]

recently presented a new 2DHG model, which consists of a positive and negative fixed charge layer spaced of about 0.2 nm in order to correctly reproduce the C-H dipole at the interface(fig.2.9(d)). This allowed for an effective matching of the ON state and transfer characteristics of HFETs based on both single crystal and polycrystalline diamond. It is worth mentioning that the value of the hole mobility for H-FETs simulations is usually varied in order to match the device' characteristics at room temperature.

However, as already discussed in paragraph 2.2.4, hole mobility for 2DHG depends upon temperature, the hole gas density concentration and other scattering mechanisms. Thus, a more consistent model, not yet available in the literature, is essential to correctly estimate the electro-thermal characteristics of the next generation of HFETs. Together with that, as hydrogen terminated diamond exhibits the NEA property, a precise modelling of this physical parameter is fundamental to predict the correct band alignment between diamond and oxide layers, but also to simulate the electron emission from vacuum switches devices.

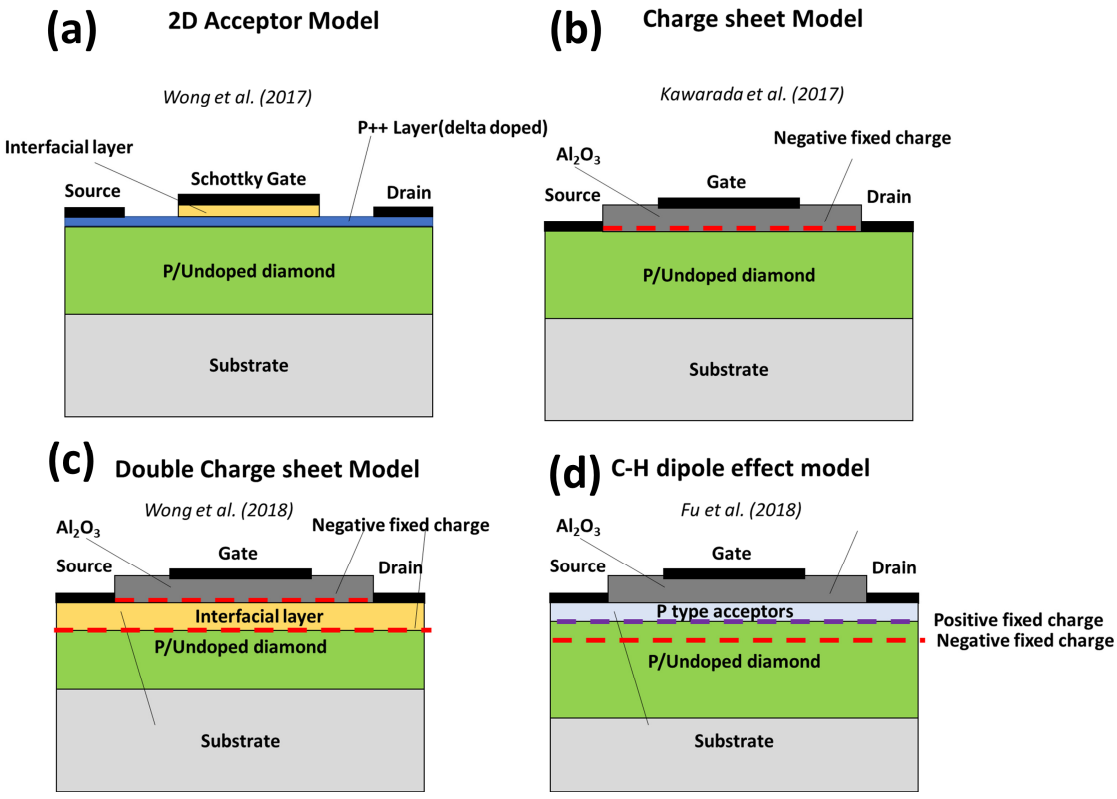


Figure 2.9: Different charge sheet models for diamond HFETs used in Wong et al. [158, 160], Fu et al. [159] and Kawarada et al. [108]. (a) 2D acceptor model, (b) charge sheet model, (c) double charge sheet model, (d) C-H dipole effect model.

2.3.2.2 TCAD modelling for 2DHG Mobility

Regarding the finite element modelling of the 2DHG-based devices simulated in chapter 4, a temperature-doping dependent 2DHG mobility has been implemented within the "charge sheet model" of Kawarada et al. The simplified formulas which are defined in the set of equations (10a-b) with the parameters of table 2.7 have been matched from the theoretical analysis of the scattering models carried out by Li et al.[126] and implemented for the finite element simulations (figure 2.10). In (10), N_{2DHG} is the charge sheet concentration (cm^{-2}), T the temperature and all the other symbols are fitting parameters.

Table 2.7. Parameters used for fitting equations (10a-b) with the model described in [126].

Symbol	a_{2DHG}	b_{2DHG}	c_{2DHG}	d_{2DHG}	γ_{2DHG}
Unit	cm^2 /Vs	cm^2 /Vs	cm^{-2}	-------	-------
Value	33.78	1.442e4	1e10	0.7796	-0.4895

$$\mu_{2DHG}(T, N_{2DHG}) = \mu_{2DHG}(300, N_{2DHG}) \cdot \left(\frac{T}{300}\right)^{\gamma_{2DHG}} \quad (10a)$$

$$\mu_{2DHG}(300, N_{2DHG}) = a_{2DHG} + \frac{b_{2DHG} - a_{2DHG}}{1 + \left(\frac{N_{2DHG}}{c_{2DHG}}\right)^{d_{2DHG}}} \quad (10b)$$

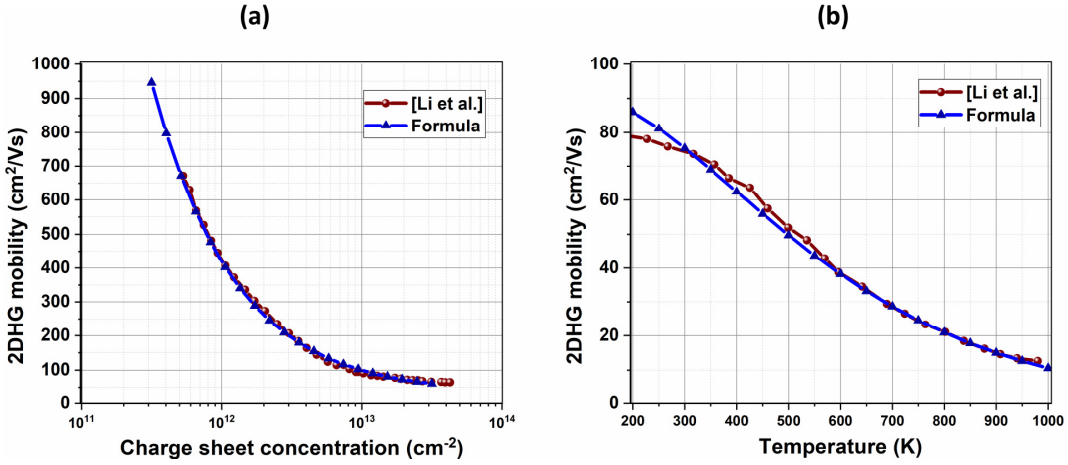


Figure 2.10: 2DHG mobility model with formula (10a-b) and its comparison with the model of Li et al. at T=300 K for different charge sheet concentration (a) and for different operating temperature for a fixed 2DHG sheet concentration of $1.8x10^{13}$ cm^{-2}.

2.3.3. Physical models for the breakdown voltage of diamond

When comparing different devices, a sound definition and criterion for a correct extraction of the breakdown voltage is extremely important. In diamond, the high density of defects and the non-optimized growth process can usually lead to premature breakdown with a leakage current that reaches a value comparable with the ON state current. Only rarely, some diamond devices tend to exhibit a breakdown voltage triggered by the impact ionization effect. Therefore, for a correct approximation of the OFF state performance of diamond devices, both the leakage current and the impact ionization need to be correctly modelled in TCAD. Regarding the impact ionization coefficients, several works have attempted to extract a unique set of avalanche coefficients for diamond by means of ab-initio simulations, TCAD matching simulations, charge multiplication experiments and theoretical studies. The majority of those models rely on the Chynoweth model (equation 11-12) and do not account for the temperature dependence of the breakdown (except for [144]). Some of these models assume a unique value of coefficients for holes and electrons, an assumption validated by adopting the geometric average of the values for holes and electrons as the common value (table 2.8). In equations 11-12, $\alpha_{n,p}$ is the electron(hole) impact ionization rate, $K_{1n,p}$ and $K_{2n,p}$ are the impact ionization coefficients, E is the electric field, x is the position with reference to a 1D p-n junction, X_{BEG} identifies the position of the metallurgical junction, V the applied voltage, SCR is the space charge region, F(V) is the ionization integral.

$$\begin{cases} \alpha_n(x,V) = K_{1n} \cdot e^{-\frac{K_{2n}}{|E(x,V)|}} \\ \alpha_p(x,V) = K_{1p} \cdot e^{-\frac{K_{2p}}{|E(x,V)|}} \end{cases} \tag{11}$$

$$F(V) = \int_{SCR(V)} e^{-\int_{x_{Beg}(V)}^{x} [\alpha_n(x',V) - \alpha_p(x',V)]dx'} \cdot \alpha_n(x,V)dx \tag{12}$$

Table 2.8. Impact ionization coefficient for equation (11) and (12).

	Unit	Silicon	Diamond (Hiraiwa)[161, 162]	Diamond (Kamakura)[163]	Diamond (Watanabe)[164]
K_{1n}	cm^{-1}	7.03e5	1.46e5	3.7e6	4.62e5
K_{2n}	$V \cdot cm^{-1}$	1.231e6	2.4e7	5.8e7	7.59e6
K_{1p}	cm^{-1}	1.582e6	6.1e4	4.2e6	1.93e5
K_{2p}	$V \cdot cm^{-1}$	2.036e6	1.39e7	2.1e7	4.41e6

It is worth mentioning that leakage current mechanisms have been included in finite element simulations for diamond Schottky diodes [140, 165], for MOS structures [166] and for hydrogen terminated devices [158, 160]. In detail, Driche et al. [165] implemented a thermionic emission field enhanced model and the Tsu-Esaki model for the hole tunnelling in order to reproduce the reverse characteristics of lateral diamond Schottky barrier diodes (figure 2.11).

The simulation results reproduced in figure 2.11(b), clearly point out that different avalanche coefficients modifies the electric field distribution and its peak in the device (for additional details about doping, thickness, etc. please refer to [165]). This, in turn, affects the overall level of leakage current which is dependent upon the value of the electric field at the Schottky/diamond interface.

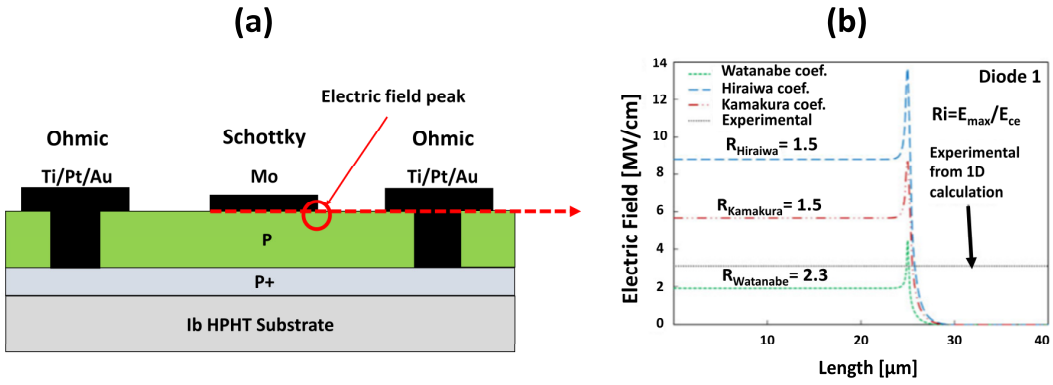


Figure 2.11: (a) Schematic cross section of lateral SBD and (b) simulated 2D electric field distribution with different impact ionization coefficients (table 10) along the red cut shown in (a) at the experimental value of the BV (~296 V). The peak electric field is located at the edge of the Schottky metal, as schematically illustrated in (a). In figure (b), R_i is the ratio of the peak electric field and the constant value under the central part Schottky contact. Figure (b) reproduced from [165].

Conversely, Nawawi et al. [140] adopted an interfacial layer for the modelling of non-ideal characteristics of Schottky diodes and a hole tunnelling mechanisms was introduced to allow for the current flow from the p-type layer to the Schottky metal. Furthermore, Marechal et al. [166] identified a multi-step mechanisms which was responsible for the asymmetric leakage current mechanisms in diamond p-type MOS capacitor, and implemented a thermionic emission model together with a trap assisted and Fowler -Nordheim tunnelling for the TCAD matching of experimental results on Al_2O_3, ZrO_2 and HfO_2 MOS capacitors. Such a mechanism was then described in more

detail by Pham et al. [167]. Regarding hydrogen terminated devices, Wong et al. [158] employed a simple direct tunnelling model in order to reproduce the leakage current mechanisms of hydrogen terminated diamond MESFET at the Schottky interface.

2.4 Conclusions

A thorough investigation of the state-of-the-art material properties and TCAD modelling has been carried out in this chapter. The accurate analysis of diamond properties allows to derive precise and concise electrical models for the finite element simulations of diamond-based devices. The physical models defined in this chapter will be then used for the optimization of diamond devices, as it will be shown in chapter 4.

3 REVIEW OF DIAMOND DEVICES FOR POWER ELECTRONICS

3.1 Introduction

This chapter provides an extensive literature review of the state-of-the-art diamond devices for power applications. Particular attention is paid to the classification of different diamond devices and their comparison in terms of conduction loss, breakdown voltage and associated switching and reliability issues. The chapter concludes with a review of the high voltage termination design for diamond devices and an assessment of the thermal management and packaging techniques for the next generation of diamond electronics.[1]

3.2 Overview of diamond device architectures

3.2.1. Diodes

Power diodes are key components in power converters, especially in DC /DC applications such as buck/boost topologies but also in AC/DC and DC/AC power conversion schemes in which they are required to work together with transistors (like

[1] The material in this chapter has been the object of the following publication: Donato, Nazareno, et al. "Diamond power devices: State of the art, modelling and figures of merit." Journal of Physics D: Applied Physics (accepted on 17th October 2019).

MOSFETs and IGBTs), as rectifiers, free-wheeling diodes or part of the filters. Diodes structures can be classified as unipolar or bipolar, based on the type of conduction mechanisms occurring in the ON state. Due to the low incorporation of phosphorous and the high activation energies for n-type dopants, diamond Schottky diodes have been mainly fabricated on boron doped layers. The superior high temperature performance of boron doped diamond (i.e. resistivity, critical electric field, saturation velocity, etc.) can indeed allow for a better R_{on_spec} vs BV trade-off when compared with other semiconductors compound (figure 1.2). Less benefits would be obtained with bipolar mode devices due the high built-in voltage of the p-n junctions (table 1.1), which will result in a significant ON state voltage drop. The bipolar mode could only be of use in ultra-high voltage applications (above 10 kV) and low-medium frequency applications, as already reported for 4H-SiC devices [27] and discussed in chapter 6. In addition, even if bipolar diodes are not attractive in most of the applications, a study of bipolar diodes is still relevant to investigate breakdown properties of diamond[161, 162], carrier lifetime engineering and set a reference for the leakage current. Manufactured diodes have been reported both featuring unipolar action such as Schottky, Metal-Intrinsic-P (MIP), Schottky p-n diode (SPND) and bipolar action such as p-n junctions and PIN diodes (figure 3.1 and table 3.1). Diamond Schottky diodes have first been disclosed at the beginning of 1990s [168-170], when the first successful CVD growths of boron doped diamond layers were obtained. High blocking voltages (up to 10 kV [171]) and critical electric field (7.7 MV/cm [20]) have been reported in the literature but a significant non uniformity in the material quality has resulted in discrepancies for the reported experiments. On top of that, the breakdown voltage was found to be limited mainly by the increase of the leakage current due to thermionic emission and tunneling mechanisms through the Schottky barrier [91] rather than avalanche. There is also a clear lack of efficient Junction Termination Extension (JTE) techniques for diamond devices which would reduce edge effects. Nevertheless, field plates and floating metal rings have been used (discussed in paragraph 3.3), but their effectiveness is less than the state-of-the-art JTE or floating field ring architectures commonly used in Silicon and 4H-SiC. As a result, the breakdown voltage of the actual devices in diamond is far from that predicted by the 1D avalanche theory. Improvements are still required to reduce leakage currents at high temperatures (>400 K) and to design out the edge effects due to sharp curvatures. Record currents of several Ampere have been measured for a few packaged diodes [70] and high

temperature operations (over 525 K) have been experimentally demonstrated with no observed degradation of the Schottky properties [20, 88, 100, 104, 172-177]. Despite the fact that vertical structures are more common in power electronics applications (higher scalability, smaller area, better electric field management, etc.), the difficulties in obtaining large size of self-standing low-resistive single crystal have resulted in the development of pseudo vertical diamond structures (figure 3.1), in which the p++ layers, on which the ohmic contact is deposited, is grown on top of the HPHT substrate. Various metals (W, Zr, Cu, etc.) and surface treatments have been explored in order to optimize the rectification behavior [178-180], to improve the uniformity of the Schottky metal [88] and to reduce the leakage currents which result in premature breakdown [93, 104, 181]. The best trade-off obtained so far has been achieved with Zr [20]. In order to reduce the leakage current, Kubovic et al. [182] have attempted to fabricate a JBSD with a 10 nm nitrogen doped layer. However, the presence of a high number of defects in the device structure showed no real improvements in terms of breakdown voltage. It is also worth noting that the advances achieved in the growth of phosphorous doped layers have allowed the fabrication of p-n junctions in diamond[85]. However, as the incorporation ratio is relatively high only for some specific crystallographic orientations (i.e. <100> and <111>, as discussed in chapter 2), the choice of the correct substrate is important if one wants to avoid the lateral growth of the n-type layer. Iwasaki et al. [183] have fabricated and investigated p-n junctions with n-type layers grown on <111> as a building block for JFET devices (discussed in paragraph 3.2.5) while vertical PIN diodes have been successfully reported in [184-187]. The use of highly doped n-type and p-type exploits the hopping conductivity mechanisms (p-type metallic transition occurs only at $5x10^{20}$ cm^{-3} [188]) and for that reason such devices exhibit a very low specific ON state resistance.

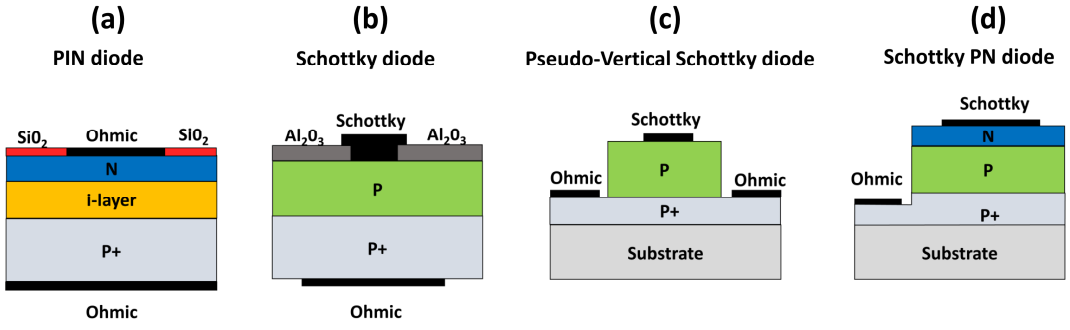


Figure 3.1: Different device structures for diamond diodes. PIN diode (a), vertical Schottky (b), pseudo-vertical Schottky (c), SPND(d). Best values for different devices are reported in the table 3.1.

Table 3.1. State-of-the-art parameters and key features for diamond diodes depicted in figure 3.1. ON state current and current density has been extracted and reported for different bias conditions.

Device	PIN Diode	Vertical Schottky	Pseudo-vertical Schottky	Schottky PN diode
Conduction mode	**Bipolar**	**Unipolar**	**Unipolar**	**Unipolar**
ON state Current	<100 mA at V=5 V with T=300 K [184, 185, 189]	20 A at V=1.8 V with T=300 K >20 A at 1.2 V with T=500 K [190]	~100 mA at V=5 V with T=300 K [88, 191]	<100 mA at V=7 V with T=300K [192]
Breakdown voltage	>11 kV [193]	>1.8 kV at T=300 K [194]	>1.6 kV at T=300 K [94]	>55 V at T=300 K [195]
Current Density	>100 A/cm^2 at V=30 V <10 A/cm^2 at V=10 V with T=300 K [185] >100 A/cm^2 at V=10 V with T=500 K [184])	>100 A/cm^2 at V=2 V with T=300 K [196] ~100 A/cm^2 at V=1.2 V with T=500 K [190]	<100 A/cm^2 at V=2 V 4500 A/cm^2 at V=7 V with T=300 K [20, 88] >200 A/cm^2 at V=2V (after Zr annealing at T=750 K)	<10 A/cm^2 at V= 2V >60 kA/cm^2 at V= 6V with T=300 K [195]
Notes	High built-in voltage. Need long lifetime for minority carriers (state-of-the-art value is estimated to be 6ns for holes [197]) and highly doped n+ region). Positive temperature coefficient of the BV [185]. Employed as slow neutrons detector [186].	When the drift region is lowly doped the device is known as MIP+ diode. MIP+ diode shows Space charge limited current behavior. High scalability and fast turn OFF (~ns). BV limited by defects.	Low scalability of the BV and the R_{on_spec}. Highest dielectric field strength reported (7.7 MV/cm). Schottky metal stable up to 700 K. Etching of p+ is needed to avoid common substrate issues [198]. Used as temperature sensor [198].	No theoretical trade-off between BV and R_{on_spec}. Positive temperature coefficient for the ON state current. High switching speed ~ 10 ns for low reverse voltage (~-5V) [199]. Thickness and doping of the n-type layer set a limit for the scalability. Thermionic emission current dominates below flat-band voltage [192].

The carriers injected from the highly doped layers reduce the total resistivity of the drift region where only residual boron and nitrogen dopants are present. Nevertheless, the lack of a controllable minority carrier lifetime poses some serious questions on the scalability of the drift layer of the PIN diodes. Together with the lack of carrier lifetime control, reproducibility and uniformity, the high built-in voltage of the p-n junction (even when operated at high temperature) represents a limiting factor in the development of this device structure [200]. To overcome some of the previously mentioned issues, Schottky p-n type diodes have been suggested [192, 195, 199, 201]. The Schottky metal on top of the n-type layer is able to deplete the n-type (nitrogen or phosphorous) doped layer in both the ON state and OFF state, allowing for holes to be injected from the p+ layer in the ON state and at the same time support the reverse voltage. Record current densities higher than 10^4 A/cm^2 at 6 V and a BV not scaling with the R_{on_spec} have been demonstrated for this device structure. However, the breakdown voltage is still limited by the maximum depletion layer width which would allow for correct operation in the ON state (i.e. a fully depleted n-type layer) [202].

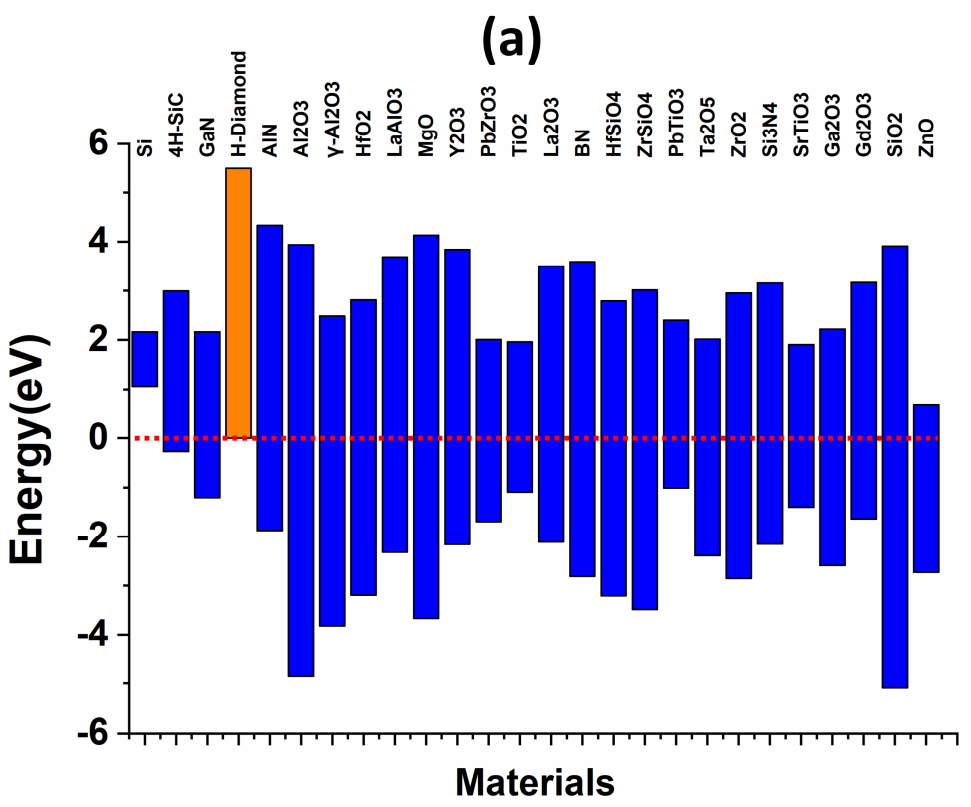
3.2.2. Metal-Oxide-Semiconductor devices

The successful fabrication of any MOSFETs, such as those based on deep depletion, inversion and accumulation, requires a reliable and high-quality metal oxide semiconductor interface. Compared to Silicon where the high quality native SiO_2 oxide has played a major role in the success of this material, the use of SiO_2 on SiC still results in low performance interface properties due to the presence of a high number of interface states which negatively impact on the carrier mobility at the oxide-semiconductor interface. Multi stack oxides and other technological techniques are now under investigation in order to improve the mobility of 4H-SiC MOSFET which still remains a major issue in the field[203]. The situation is even more complicated in Diamond and other WBG material such as GaN, which have no native oxides available. Numerous diamond oxide interfaces have been studied in the last few years: WO_3 ,Ta_2O_5, Al_2O_3, $Al_2O_3/LaAlO_3$,ReO_3 , NO_2/Al_2O_3, HfO_2,MO_3, Nb_2O_5,V_2O_5 and ZrO_2 [204, 205]. The choice of the best oxide depends upon the surface termination

(hydrogen or oxygen) and on the deposited gate metal and it is in general linked to the behavior of the gate leakage current.

3.2.2.1. Comparative study of MOS stack on oxygen and hydrogen terminated diamond

The Ideal MOS structure requires an electrostatic potential barrier which hinders the carrier transport from the semiconductor to the gate metal. Depending on the carrier transport and on the specific characteristics of the device, it could also be possible to provide a single potential barrier with respect to the conduction or the valence band. This is the case of H-terminated diamond FETs where due to the low electron carrier concentration in the bulk, only a single barrier for 2D hole gas is required[206]. Several oxides and transition oxides have been suggested for H-terminated diamond interfaces with the multiple roles of increasing the carrier density, improving the time-temperature stability of the interface and ensuring a good offset with the diamond valence band [207-209]. Double and triple oxide stacks have also been investigated on H-terminated diamond surfaces and their electrical properties (i.e. hysteresis, band offset, leakage) accurately reviewed in [204].



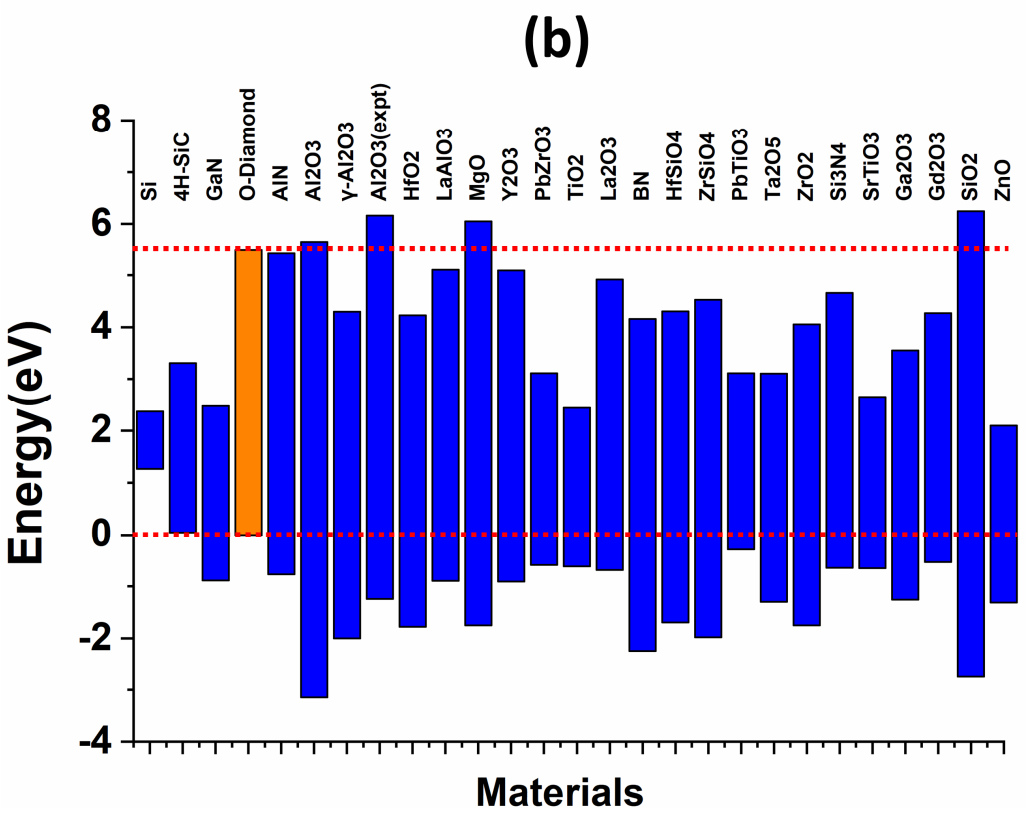


Figure 3.2: Band alignment of H-terminated (a) and O-terminated (b) diamond with several oxides. Calculation is based on the parameters and the procedure adopted by Robertson and Monch [210, 211]. The NEA for H-terminated diamond results in a negative conduction band offset (i.e. no barrier for electrons). Experimental Al_2O_3/O-Terminated diamond alignment reported in [212] has been included in figure 3.2(b). The experimental bandgap of Al_2O_3 on diamond is smaller compared to the experimental value reported by Robertson in [210]. The band offsets shown in (a) and (b) only refer to the material highlighted in orange (i.e. H-diamond(a) and O-diamond(b)) and cannot be used for band offset comparison between materials highlighted in blue. This is due to the difference in terms of Schottky barrier pinning factor used in the calculation. For additional details please refer to [210]

It is worth mentioning that different types of charges in the oxide may lead to different interface properties of the H-terminated diamond layer which could exhibit normally-OFF behavior when a specific oxide stack is deposited [213, 214], as it will be discussed in paragraph 3.2.6.

A schematic band alignment computed with the procedure and the parameters defined in [210, 211], has been plotted in figure 3.2 for both H-terminated(a) and O-terminated(b) diamond. As it can be noted, only few oxides (like SiO_2, Al_2O_3) would allow for a dual barrier with the conduction and valence band of O-terminated diamond whereas, for H-terminated diamond, none of the listed materials assures a positive conduction band offset ($E_{c,oxide}$-$E_{c,DIAMOND}$).

3.2.2.2. Oxygen terminated diamond MOS regimes and reliability

Experimental results have shown that Al_2O_3 exhibits the best performance in controlling O-terminated diamond interfaces for both accumulation and inversion regime. This is due to two main factors: (i) the high value of the band offset (with both conduction and valence band) and (ii) the low level of interface states. The electrical properties and the band alignment of this stack have been reported in [212]. Leakage current mechanism occurring in Diamond/Al_2O_3/Al has also been investigated by Pham et al. [167]. Authors suggested a 4-step mechanism responsible for the negative bias leakage current which originates from the hole carriers accumulated at the interface and it involves trap-to-trap tunneling in the oxide and charge transfer with the interface states. In fact, evidences from C-V-f (capacitance-voltage-frequency) analysis have also shown the presence of high density of interface states (Dit) of ~10^{12} cm^{-2} located at around 0.6 eV from the valence band maximum which are mainly responsible for FLP at very high negative bias (-8V). This effect prevents the accumulation of majority carriers at the interface during normal operation of MOS based devices. Observations of post-process high temperature (> 770 K) annealing have shown an improvement in the C-V characteristics and a significant reduction of the FLP. Only recently, a few reliability studies have been reported for diamond MOS stacks. In [215], Loto et al. have observed a strong impact of the interface defects in the flat band voltage shift by means of time dependent bias stress. In addition, it has been demonstrated that the post process annealing improves the electrical performance of the MOS capacitor, with a clear accumulation regime observed even at relatively low negative bias and with a negligible gate leakage current value.

3.2.3. Deep depletion MOSFETs

Among the properties correlated with the wide value of the diamond' bandgap (5.47 eV at RT), the small value of the intrinsic carrier concentration at room and high temperature (10^{-27} cm^{-3} at RT) is for sure one of the most interesting features. On one hand, this has a positive effect on reducing the theoretical value of the leakage current in reverse conduction regime; on the other hand, the small amount of minority carriers

availability clearly hinders the creation of inversion regime formed by thermal generation in the MOSFET device [216]. The time constant for the thermal generation of minority carriers from a mid-gap states can be easily calculated with the formula described by Pham et al. [167, 216, 217] and has been plotted in figure 3.3. Therefore, if minority carriers are not provided by source and drain regions or by UV light exposure, a deep depletion regime can be obtained for a long and stable duration. The concept of temperature-time stable deep depletion effect observed and demonstrated for diamond devices is different from the dynamic effect described in other semiconductors like Silicon [218-221].

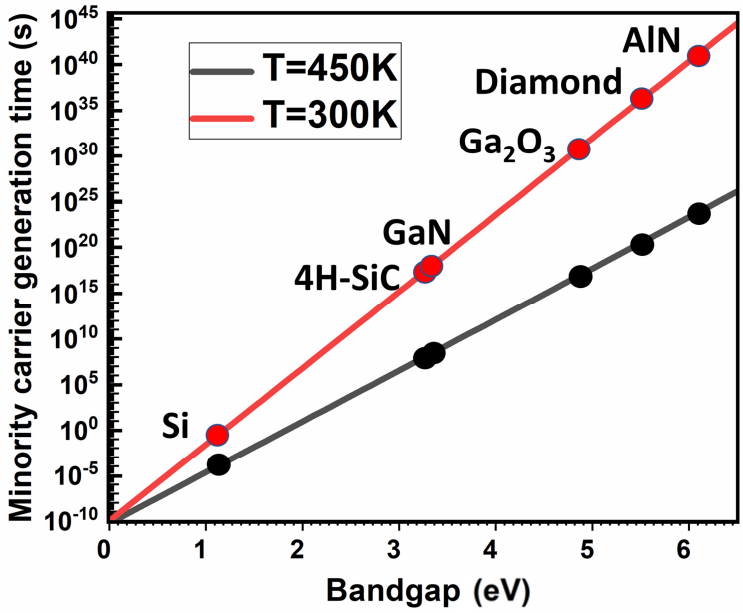


Figure 3.3: Minority carrier generation time from a mid-bandgap state for different semiconductors. Picture reproduced from the formula described by Pham et al. [216] with the inclusion of the temperature dependence for the density of states.

In that case, the inversion layer is much more sensitive to time and temperature effects, making deep depletion only a transient effect able to improve the dynamic BV. In β-Ga_2O_3, a similar effect has been exploited for the realization of depletion mode FETs [57, 222]. Experimental deep depletion diamond MOSFETs rely on the Al_2O_3/(Ti/Pt/Au) stack. High breakdown fields of 4 MV/cm have been measured for a lateral normally-ON device schematically depicted in figure 3.4. Good modulation of the drain current has been achieved and a threshold voltage (Vth) of ~7 V demonstrated for a 230 nm thick boron doped layer of 1.75×10^{17} cm^{-3} grown on Ib HPHT substrate. The main benefit of these devices is the volume conduction, taking the full benefits of

high hole mobility in bulk diamond and the possibility to have a thick channel. However, the maximum current density observed in [223] is several orders of magnitude lower than the one reached for H-terminated FETs due to the un-optimized process which will require, as an example, selective growth of p++ regions prior the deposition of the source and drain ohmic contacts in order to reduce the parasitic series resistance [224]. In addition, high temperature operations which will result in an enhanced boron activation, may be beneficial for the current density' improvement of deep depletion FETs, as illustrated in [224], where authors demonstrated drain current density of 10mA/mm at VDS=-5 V for VGS=0 V and an operating temperature of ~523 K (R_{on_spec}=50 Ωcm) with a 175 V BV (measured at RT). Recent reports have demonstrated the possibility of realizing deep depletion diamond Fin-FET with CVD boron doping on a <100> 3x3 mm^2 HPHT undoped substrate.

Table 3.2. State-of-the-art parameters and key features for diamond depletion mode MOSFETs depicted in figure 3.4.

Device	Vertical Fin-FET	Lateral Deep depletion MOSFET
Breakdown voltage	>16 V at T=300 K [225]	> 200 V at T=300 K [217, 226]
Current Density*	< 1 mA/mm at T=300 K <10 mA/mm at T=450 K with VDS=-15 V and VGS=-16 V [225] <0.05 mA/mm T=300 K < 2 mA/mm at T=450 K with VGS=-10 V VDS=-1 V	~0.1 mA/um at T=300 K with VDS=-15 V and VGS=-16 V [226] <10^{-3} mA/um at T=300 K ~$5x10^{-3}$ mA/um at T=450 K with VGS=-10 V VDS=-1 V With selective growth of P+: ~3 mA/um at T=523 K with VGS=0 V VDS=-1 V
Notes	Fin channel allows for normally-OFF operation. Breakdown voltage measurements are not reported. However, Gate and drain overlap limits the max BV. Max observed drain current is limited to 838 nA for VGS=VDS=-16 V at T=300 K and 29 uA at 450 K [225].	Normally-ON. High temperature operation increases the current and reduce the threshold voltage. Scaling of the R_{on_spec} and BV is an issue. Field Plates are needed to improve the BV. Current density is limited by the incomplete ionization at RT.

*Values reported for the Fin-FET are assuming the true width of the current transport path.

E-beam lithography and O_2 dry etching have been used to fabricate the Fin-FET structure depicted in figure 3.4. The device exhibits an ON/OFF ratio of above 3000 and a maximum current density of 30 mA/mm at 425 K (with VDS=-15 V and VGS=-16 V), a value 35 times higher than the one at RT (table 3.2). The low value of the boron concentration in the channel ($5x10^{16}$ cm^{-3}) together with the 45nm of SiO_2 oxide and the small metal workfunction of Al (~4.08 eV) result in a depletion width of about 55 nm. As the depletion region width is more than half the Fin channel width, the device exhibits normally-OFF behavior with a threshold voltage at -2.74 V which also shows a dependence upon the drain bias.

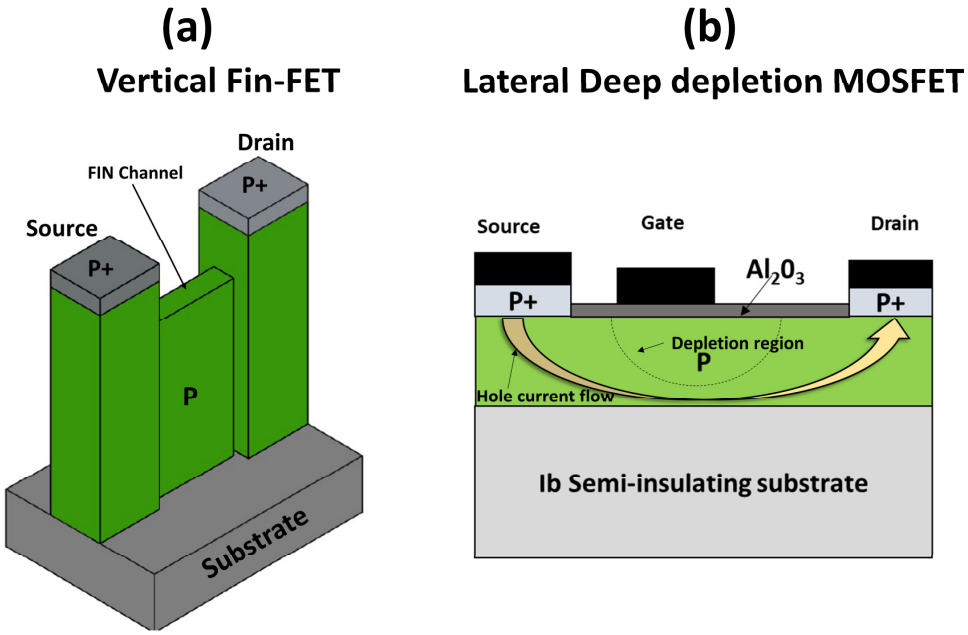


Figure 3.4: 3D Schematic of the diamond depletion mode MOSFET in vertical FinFet configuration(a) and cross section of a lateral deep depletion MOSFET(b). The gate dielectric and metal surrounds the whole FIN channel (not shown in the picture).

3.2.4. Inversion MOSFETs

High quality Phosphorous doped n-type diamond body/Al_2O_3 interface obtained by wet annealing has resulted in the first diamond Inversion type lateral MOSFET on a <111> HPHT substrate (figure 3.5), as reported by Matsumoto et al. [128]. A maximum drain current density of 1.6 mA/mm and channel field effect mobility of 8 cm^2/Vs have been extracted from the experimental data at VGS=-12 V and VD=-5 V (table 3.3). This proof of concept for an inversion mode MOSFET resulted in a

normally-OFF behavior, with a negative threshold voltage (Vth) of about -6.3 V. This high Vth value for the inversion regime is a clear signature of high level of interface traps (with a density estimated to be above 6e12 $cm^{-2}eV^{-1}$).

This first proof of concept focused solely on the experimental achievement of the inversion regime, but future developments will eventually lead to the addition of a lateral p-type drift region. This modification would allow high voltage blocking capability. In addition, the effect of the parasitic p-n-p bipolar transistor on the breakdown voltage, leakage current and safe operating area would need to be determined.

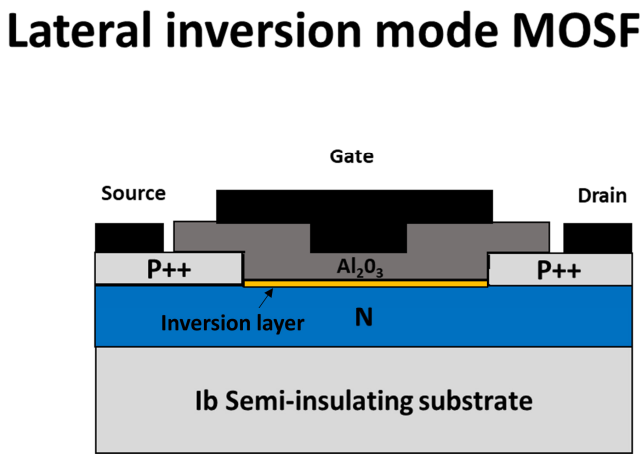


Figure 3.5: Schematic cross section of a diamond inversion mode MOSFET in lateral configuration.

Table 3.3. State-of-the-art parameters and key features for diamond inversion mode MOSFET illustrated in figure 3.5.

Device	Lateral inversion mode MOSFET
Breakdown voltage	<50 V at T=300 K [128]
Current Density	<1 mA/mm at T=300 K With VGS=-5 V VDS=-1 V [128]
Notes	Normally-OFF. Low interface mobility. High density of traps. Low breakdown voltage. First proof of concept.

3.2.5. JFETs, MESFETs and Bipolar Transistors

FETs based on metal semiconductor junction (MESFET) or p-n junction (JFET) are highly reliable for power electronics applications due to the absence of the gate oxide layer which tends to generate high density interface states and trapping/de-trapping mechanisms (figure 3.6). Umezawa et al. [227] have fabricated several diamond MESFETs, exploring different Schottky gate metals (Mo, Pt, Al) and observed a maximum current density of 1.2 mA/mm at high temperature (T=600 K) with VGS=0 V and VDS=-20 V due to the enhanced boron activation in the conduction region. High breakdown voltages above 2 kV with a gate to drain distance of 50 μm [228]) have been shown for diamond MESFETs which usually exhibit normally-ON characteristics with a high threshold voltage (Vth). Good scalability of the breakdown voltage with the gate drain distance has been proven for diamond MESFETs as illustrated in [227]. Diamond MESFETs have been also realized in reverse blocking (RB) configurations with a Schottky metal for the gate and the drain contacts and exhibited a maximum BV of 3 kV and a maximum ON state current of 1 μA [229]. Due to the Schottky gate, diamond MESFETs must have a lightly doped region in the channel to limit the gate leakage which occurs especially at high temperature. One should note that the ON state resistance is reduced at elevated temperatures due to increased ionization of boron. Consequently, these structures rely currently on drift and channel regions with a low boron concentration ($<10^{16}$ cm^{-3}), which is more suitable for breakdown voltages above 5 kV [103]. As a consequence of their low doping in the drift region, the Vth is around 20-30 V and the theoretical ON state resistance of such MESFETs below 5 kV is higher than that of MOSFETs with insulated gate and higher doping levels. On the other hand, improvements in the lateral growth of n-type diamond layer in the <111> direction have enabled the fabrication of high quality diamond p-n+ junction with high rectification ratio and breakdown voltages close to 1 kV [83, 85, 98, 183, 230]. These p-n+ junctions have been used as the building block of diamond Junction FET fabricated by Hosino et al. [85]. The p-type conductive channel which has been obtained by means of Inductively Coupled Plasma (ICP) etching and electron beam (EB) lithography is sandwiched between two highly doped n-type layers grown on the <111> direction, as schematically illustrated

in figure 3.6. Different channel width and doping levels have resulted in both normally-ON and normally-OFF devices demonstrated in unipolar and bipolar conduction mode. Regarding the unipolar normally-ON devices, steep subthreshold swings of 120 mV/decade have been obtained with current densities exceeding 10 A/cm^2 at RT and close to 450 A/cm^2 at 673 K for a VDS=-1 V and VGS=-3 V [98]. Threshold voltages for such normally-ON JFETs range from 30 V to 5 V depending on the channel width and doping which in turns influence also the R_{on_spec} of the device (table 3.4). The BV measured at different junction temperatures shows a positive coefficient, according to the increase of the phonon scattering and consequent reduction of the avalanche multiplication coefficient [230]. In addition, a critical electric field of 6.2 MV/cm has been calculated for the case of an abrupt and ideal p-n+ junction. Normally-OFF JFETs (with a Vth around -1.2 V) have been manufactured by implementing a parallel reduction of the doping concentration and the channel width (0.2 μm) in order to pinch-off the channel at zero bias. Devices show a good rectification ratio but a much smaller current density due to the higher resistivity of the channel region[231]. Despite the current density increases at HT, a positive shift of the threshold voltage with the temperature, which has been also confirmed by TCAD simulations and experimental results[144, 232], may however result in normally-ON operations at elevated temperature. Improvements in terms of current densities (table 3.4) have been achieved with both normally-ON and normally-OFF JFET operating in bipolar mode, with the injection of minority carriers (electrons) in the p-type region. However, the bipolar conduction also increases the number of carriers in the channel and this would result in a slower turn OFF of the device. Furthermore, a more complex gate driving technique is required for bipolar mode JFETs. The recent progress in the n-type doping technology has also allowed the fabrication of bipolar junction transistors (BJTs) [233-235]. Preferential growth of phosphorous doped layers on the <111> direction as the base region was adopted in order to fabricate the heavily doped n+ layer which is fundamental for the correct operation of the BJT. Indeed, early fabrication processes have failed to demonstrate the bipolar mode operation due to the high resistivity of the n-type base layer (around 10^{18} cm^{-3}) and the low diffusion length of minority carriers (holes) in the base region. The introduction of the n+ layer has enabled both the hopping conductivity and the reduction of the series resistance due to the ohmic contact of the base.

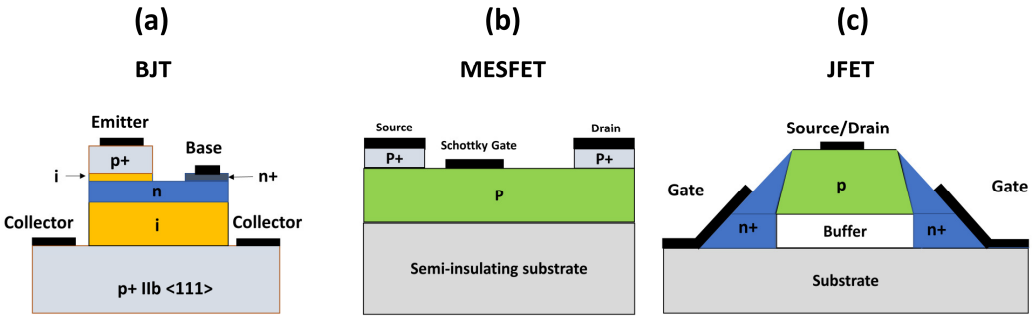


Figure 3.6: Schematic cross sections of a diamond BJT(a), MESFET(b) and JFET(c).

Table 3.4. State-of-the-art parameters and key features for diamond BJTs, MESFETs and JFETs shown in figure 3.6.

Device	BJT	MESFET	JFET
Breakdown voltage	>100 V at T=300 K[234]	>2 kV at T=300 K[228] ~3 kV at T=300 K for RB MESFET [229]	>600 V at T=300 K [230]
Current Density *	Not reported. Max current ~uA at V_{EB}>6 V [233].	~2 mA/mm at T=500 K with VDS=-20 V VGS=0 V [236] ~0.14 mA/mm at T=300 K with VDS=-20 V VGS=0 V [236] Max current ~30 mA at T>550 K [67] ~ 0.1 mA/mm at VDS=-1 V VGS=0 V at T=600 K [227, 236]	max current (~2 uA) at T=573 K with VDS<-10 V [232, 237] 600 A/cm^2 at T=500 K 40 A/cm^2 at T=300 K with VDS=-1 V and Ig=2 nA (bipolar mode) [232, 237] ~3.5 kA/cm^2 at T=500 K with VDS=-20 V and Ig=1 uA (bipolar mode) [237]
Notes	Need good doping control of both n-type and p-type layer. Lifetime control is needed for high current gain. Low BV.	Radiation hardness even at high junction temperature. Easy fabrication process (only requires p-type doping). Good scaling of the BV with the drift layer length.	Bipolar mode operations and normally-OFF demonstrated. Positive temperature coefficient of the breakdown voltage. Requires n+ doping.

*The reported current density for diamond lateral JFET is usually normalized with the cross-sectional area.

Furthermore, the reduction of the base width together with the improvements in the growth' conditions have enabled a more efficient injection of holes from the p+ emitter. Maximum collector currents of few μA have been demonstrated and the current gain h_{fe} (defined as the ratio of the collector and base currents) of ~10 has been reported for high V_{EB} voltage (~6.2 V) by Kato et al. [233]. However, scalability of these devices is highly limited due to the low diffusion length, which was estimated to

be around 400 nm for a diamond BJT with a phosphorous doping concentration for the base region of ~10^{18} cm^{-3} [234].

3.2.6. 2DHG FETs

Two-dimensional hole gas (2DHG) formation near the hydrogen terminated diamond surfaces provides an innovative way to obtain an almost zero activation energy for a hole channel. This effect, which was revealed in the early 1990s in the studies of Grot, Landstrass, Albin and Shiomi [169, 238-241], has been discovered to be useful for the fabrication of surface channel FETs [105]. On top of that, the maximum measured channel mobility typically around 100 cm^2/Vs and the sheet hole density which oscillates between 10^{12} cm^{-2} up to 10^{14} cm^{-2} (with NO_2 adsorption [107, 242]) are promising electrical properties for the next generation of diamond power devices [243]. Record current densities > 1.3 A/mm with a specific ON state resistance of 4 Ωmm have been reported at VGS=-5 V and VDS=-12 V [244], even at room temperature where competitive bulk FETs suffer from incomplete ionization and therefore reduced carrier concentration (table 3.5). Despite the high ON state performance and the high breakdown voltage (~500 V) have been demonstrated for C-H terminated diamond FETs by Kawarada et al. [245], time and temperature stability have been a great concern in the diamond community for over 20 years. Atomic layer deposition (ALD) of Al_2O_3 have been proven to be a new way to uniformly induce the hole accumulation layer and improve the overall reliability and stability of the HFETs [107, 246]. Compared to the surface adsorbates, the insulating layer possess some unoccupied orbitals or fixed negative charges which are responsible for the formation of the 2DHG at the interface [108]. In the case of Al_2O_3, these unoccupied levels have been reported to be present in the bandgap below the valence band maximum of diamond and they can give rise to a valence band offset which oscillates between 2.9 eV and 3.9 eV. Lateral normally-ON HFET with a high breakdown voltage (over 1.5 kV) and high temperature (>725 K) stability have been reported in the literature [109, 213, 247-251]. A good scalability has been demonstrated for increasing gate-drain distance (L_{gd}) and a maximum breakdown field of 3 MV/cm was estimated [108, 243]. Lateral triple-gate HFETs which allow carrier to flow in both lateral and planar directions have illustrated higher current density and more promising downscaling

scenarios compared to classic lateral HFETs [252]. Despite the fact that the majority of diamond HFETs reported in the literature exhibits a relatively high threshold voltage (~10-20 V) with a normally-ON behavior, normally-OFF HFETs have also been fabricated by some research groups. Several solutions have been implemented to avoid the formation of the 2DHG under the gate region and achieve the enhancement mode behavior. For example, Liu et al. [213, 214] deposited a double high-k layer oxide to avoid the formation of unoccupied levels and remove the 2DHG from the gate region, while Kitayabashi et al. [21] obtained the normally-OFF operations with the partial oxidation of channel region with C-O bounds. While for the double high-k oxide solution Vth has been found to be highly dependent on the oxide deposition and on the overall fabrication process, its stability dramatically improved with the device concept adopted by Kitayabashi et al. (were the Vth oscillated between -2/-4 V). In such device, the breakdown voltage has been experimentally found to be >2000 V (an existing record for diamond HFETs) and in general driven by several mechanisms depending on the gate and drain current leakage behavior [21].

Because the hole sheet created at the diamond interface is not based on piezo-polarization effects as in AlGaN/GaN interfaces, it can be formed in non-planar structure (i.e. vertical trenches), as it has already been reported by Inaba et al. and Oi et al. [253, 254] (figure 3.7).

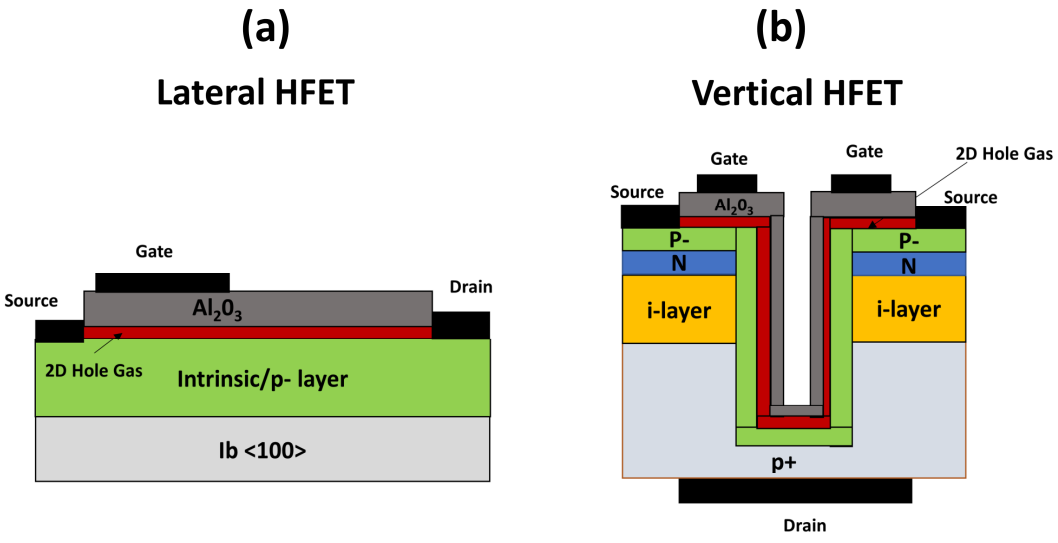


Figure 3.7: Schematic cross sections of diamond lateral (a) and vertical HFET (b).

Table 3.5. State-of-the-art parameters and key features for diamond lateral and vertical HFET depicted in figure 3.7.

Device	Lateral HFET	Vertical HFET
Breakdown voltage	>2 kV at T=300 K [21]	~ 350 V at T=300 K [253, 254]
Current Density	1.3 A/mm at T=300 K with VGS=-5 V and VDS=-12V [244] 0.2 A/mm at T=300 K with VGS=-5 V and VDS=-1 V [244]	>0.2 A/mm at T=300 K and T=600 K with VDS=-50 V and VGS=-20 V [253] <10 mA/mm for VDS=-1 V and VGS=-5 V [253]
Notes	Lateral current flow limits the scalability of the ON state resistance. BV scalability is limited. Beneficial for RF applications [249, 255]. Normally-OFF has been demonstrated. Fabricated with both poly and mono crystalline diamond.	The beneficial vertical current spreading only starts from the p+ layer. BV is limited. Complex fabrication process which requires deep etching. N-type layer specifications are crucial to reduce vertical leakage current.

The trench side wall was regrown after the etching of the MESA structure, showing a high mobility 2DHG with performance almost similar to the reported lateral HFETs. However, temperature dependence of the leakage current still remains a fundamental issue with HFETs due to the residual doping concentration in the bulk region and the lack of proper isolation. In-situ annealing performed prior the oxide deposition of the hydrogenated diamond surface at ~775 K was found to be crucial to enhance long-term doping stability of HFETs fabricated on MoO_3 and V_2O_5, as reported by Crawford et al. [207]. This evidence opens a promising route for the high temperature applications and for the possible future commercialization of diamond HFETs.

3.2.7. Vacuum Switches

Hydrogen terminated diamond interfaces are well known to exhibit a unique property renowned in the literature as NEA (Negative Electron Affinity), already discussed in chapter 2. More specifically, in NEA interfaces, the vacuum energy level (E_O) lies below the minimum energy level of the conduction band (E_c). This feature is very

attractive for the realization of electron emitters as , from a theoretical point of view, electrons excited from the valence band or injected from contacts into the conduction band could be efficiently emitted in vacuum from the surface without any increase of the device temperature [256-260]. Experiments have confirmed electron emission from diamond p-n and PIN diodes with an efficiency oscillating around 2%. Such devices are known as "vacuum switches" as they rely on the same principle of classical vacuum tubes.

A schematic representation of the diamond vacuum switch fabricated in [257, 260] is illustrated in the figure 3.8. When the voltage is higher than the built-in voltage of the pin junction , the PIN diode is switched ON and the anode voltage dramatically drops from the OFF state value (10 kV in [260]) to around 160 V, which is the Vth of the vacuum switch. The voltage difference 10 kV-160 V is therefore applied to the load through which current flows. Nevertheless, the current is very limited at the state of the art (µA) due to the lack of large size diamond substrates. Only further improvement in the efficiency to values up to 10% and the increase in the current may allow the future commercialization of this power device (table 3.6).

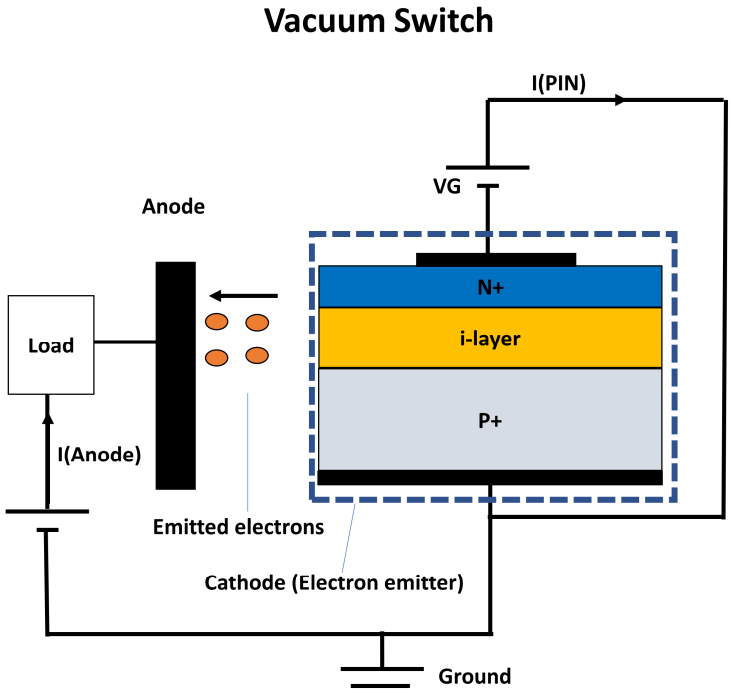


Figure 3.8: Schematic cross sections of diamond Vacuum switch and its control circuitry.

Table 3.6. State-of-the-art parameters and key features for diamond vacuum switch illustrated in figure 3.8.

Device	Vacuum Switch
Breakdown voltage	10 kV at T=300 K [257]
Current Density	4 A/cm^2 at VG<-20 V at T=300 K [259]
Notes	Unique device concept. Efficiency and output capacitance (C_{oss}) need to be improved. Gate drivers may result in non-conventional designs for power electronics.

3.3 Diamond devices with field relief designs

Edges and finite dimensions of electrodes are well known to generate crowding of the electrostatic potential lines which then results in a spatially localized increase of the electric field. The use of field relief structures is therefore required in order to improve the breakdown voltage capability and also to suppress the detrimental effects of the device termination on the field-enhanced leakage current mechanisms. Several termination techniques and structures have been suggested, simulated and implemented for diamond diodes and transistors, as illustrated in figure 3.9.

Without field relief designs, the typical vertical peak electric field at breakdown in diamond devices is limited to 1 to 2.5 MV/cm as presented in [67, 94, 102, 176]. These values suggest that large improvements are possible towards values above 10 MV/cm with suitable and efficient protections.

For unipolar mode diamond devices like SBDs, field plate structures (figure 3.9(a)) have been more often adopted in the literature [135, 174, 175, 177, 261]. With this technique, the field enhancement at the Schottky contact can be relaxed with the deposition of an oxide layer between the Schottky contact and the diamond surface. Several oxides such as Al_2O_3 and SiO_2 have been deposited for single layer field plate termination in diamond devices.

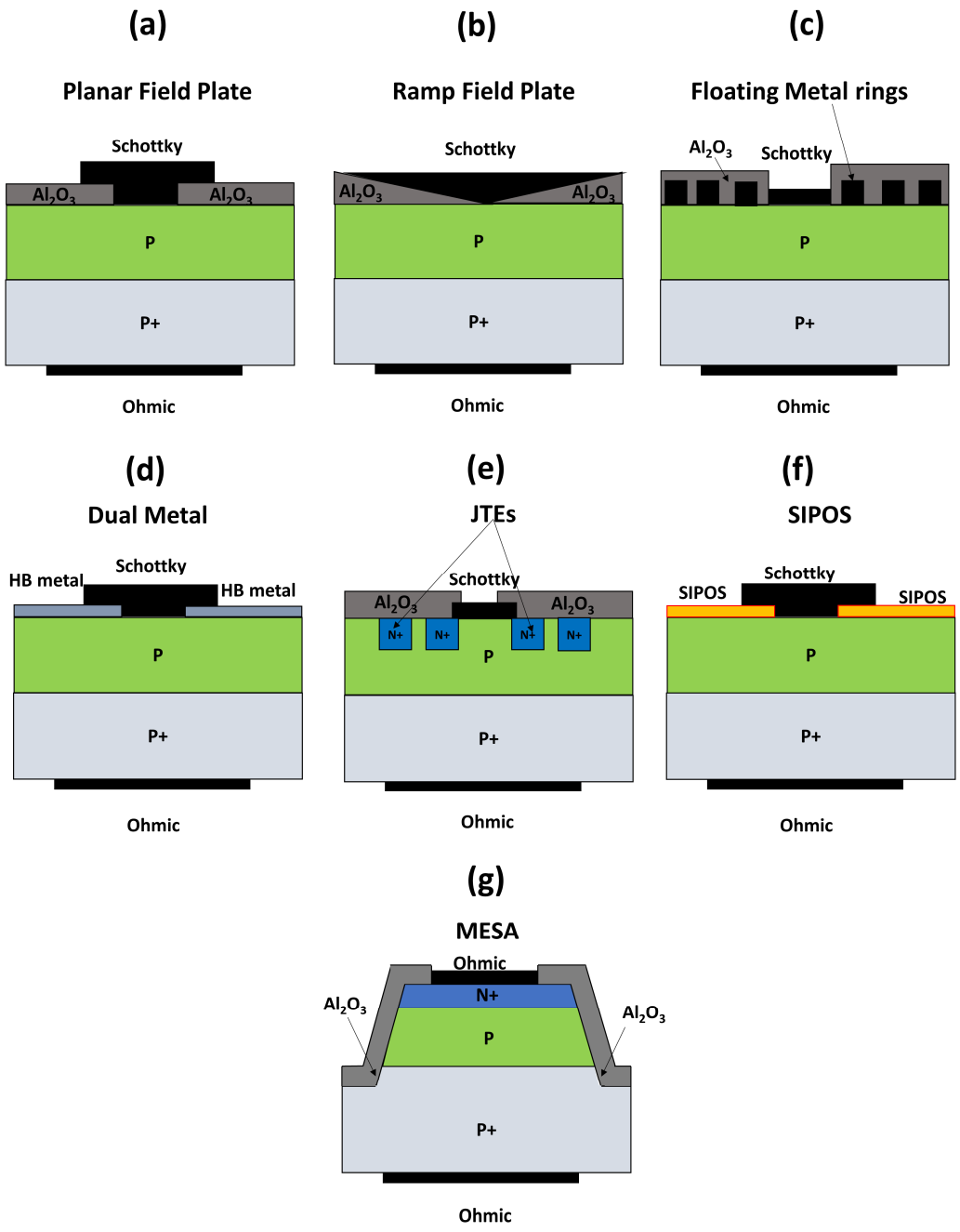


Figure 3.9: Different topologies for diamond terminations applied to the case of diodes. (a) Planar field plate, (b) Ramp field plate, (c) Floating metal rings, (d) Dual metal, (e) JTEs, (f) SIPOS, (g) MESA. Al_2O_3 has been used as oxide only as an example.

Theoretical optimization for a single layer FP structure has been carried out by Ikeda et al. [176], showing that for a BV reached at a maximum leakage current density of 10^{-4} A/cm^2, an optimum oxide thickness can be obtained for Al_2O_3 and SiO_2 (figure 10(a)). TCAD simulations on vertical boron doped (doped at 1.5×10^{15} cm^{-3} and 5 µm thick) revealed that the Al_2O_3 thickness has to be almost 1.7 times bigger than the

optimum value for SiO_2 (0.9 µm), but it allows to reach higher breakdown voltages, as depicted in figure 3.10.

Experimental results on vertical diamond SBDs have illustrated both a reduction of the leakage current and an improvement of the BV by using 0.2 µm Al_2O_3 on top of a 10 µm p-type boron doped layer [102]. The degradation of the blocking capability and leakage current for large area electrodes is usually explained by the increase of surface and bulk defects with the active area of the device. Low dependence of the leakage current upon the contact size after the FP deposition may be explained with the surface passivation effect of Al_2O_3. Ramp field plate oxides have been suggested to be one of the most effective ways to reduce the peak electric field in SBDs (figure 3.9(b)). Calibration of the FP termination by means of TCAD simulation has been performed by Brezeanu et al. [135] and shown an almost ideal BV (92% of efficiency) with 5.7° tilt angle and with a length and thickness of 25 µm and 3 µm, respectively (figure 3.10). Multi-step field plate terminations have also been investigated by Isoird et al. [261, 262] for a pseudo vertical diamond Schottky diodes.

Despite the optimization leads to a reduction of the field in the diamond, the high electric field observed in Al_2O_3 gradual FP termination (over 20 MV/cm) may seriously lead to time dependent dielectric breakdown (TDDB), an issue which has usually been neglected in state-of-the-art diamond power device terminations.

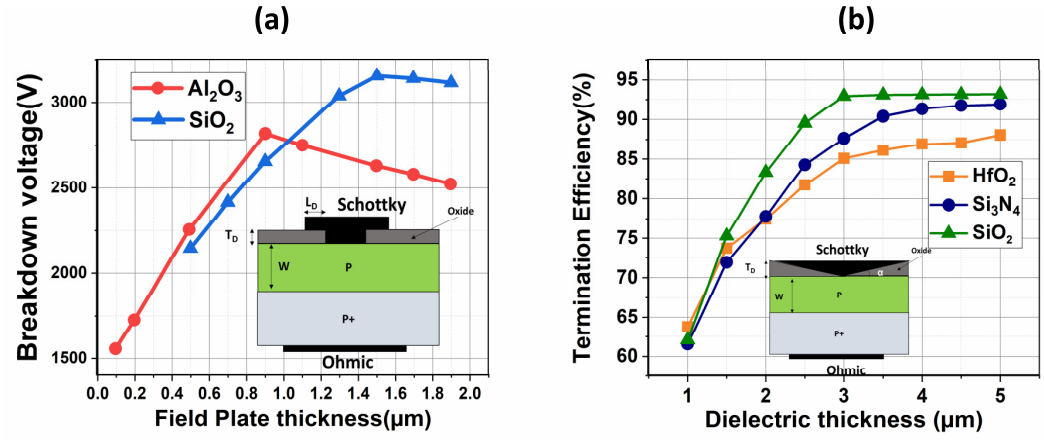


Figure 3.10: (a) BV vs field plate thickness(T_D) for a planar field plate (reproduced from Ikeda et al.[263]). (b) simulation' results of oxide ramp termination simulations' efficiency reproduced from Brezeanu et al. [135]. The results obtained in figure (b) assume a W=18 µm, α<10° and T_D>3 µm while figure (a) assumes W=10 µm (doping equal to $5x10^{15}$ cm^{-3}) and L_D=15 µm. Termination efficiency in (b) is defined as the ratio of the 2D BV and the ideal 1D BV which is equal to 3171 V (calculated for a critical electric field of 10 MV/cm). In both pictures, the time dependent breakdown of the oxide layer was not considered.

Diamond Schottky diodes with floating metal rings (figure 3.9(c)) have also been manufactured by Driche et al. [264] and their efficient reduction of the electrostatic potential crowding has been confirmed by EBIC measurement. The spacing between the different rings (Ws in figure 3.11) and the number of rings influence the peak electric field and the shape of the lateral depletion. Due to the high field gradients in diamond, the reduced spacing of such rings induces a high stress on fabrication and lithography. Conversely to other semiconductors, floating rings in diamond are mainly realized on Schottky contacts due to the previous mentioned issues connected to the n-type doping. The high conductivity of the Schottky metal is able to uniformly distribute the electric field profile under the rings if compared to a classic p-n ring termination and is therefore a promising method for terminating diamond FETs and diodes. However, as presented in figure 3.11, the spacing between the first metal ring and the Schottky contact must ≤150 nm to create an attenuation of the peak electric field and to reach about 93% of efficiency. In diamond SBDs, the reverse leakage current, which is mainly due to the thermionic field emission effect [91, 265], can be reduced by means of a double metal termination, as shown in figure 3.9(d). Such design can be obtained with two different Schottky metals, one deposited in the active area and the other one in the termination region (metals such Au or Pt can be used). The high metal/semiconductor barrier (HB) in the termination region allows to suppress the value of the OFF state current; conversely, the low barrier (LB) region in the active area avoids any increase of the threshold voltage and does not affect the ON state performance.

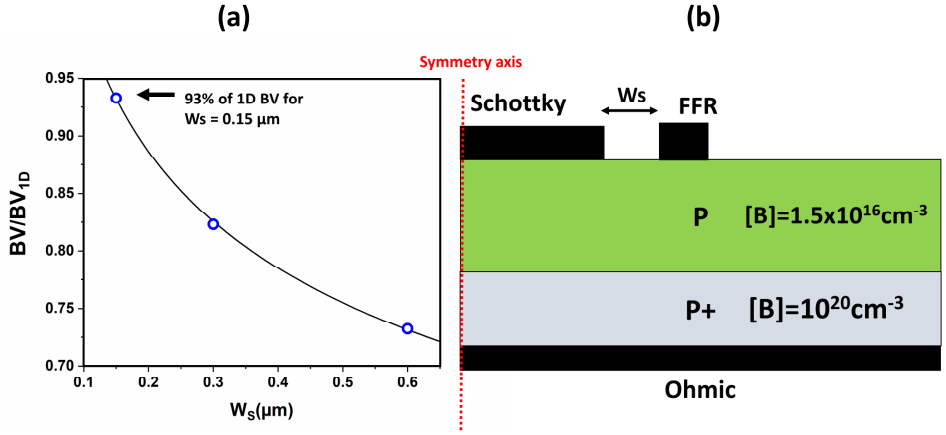


Figure 3.11: (a) Simulated 2D breakdown voltage vs 1D breakdown voltage (BV/BV1D) ratio plotted against the spacing of the first Floating field ring (FFR) and(b) schematic cross section of the SBD with a floating metal ring termination used for the TCAD simulations. Picture reproduced from [266]. Best fit curve has been included in (a).

Junction termination extensions (JTEs) have been widely used for both improving the electric field profile and the ON state current in JBS diodes for other power semiconductor devices. However, the lack of an efficient n-type doping and the issues arising from the ion implantation have made this technique less effective in diamond (figure 3.9(e)). Kubovic et al. [182] did not observe any improvement after the 10 nm of n+ type nitrogen doped layer while Huang et al. [267] tried to obtain the same effect through H+ ion implantation to increase the resistivity, reporting a breakdown voltage of about 3.7 kV.

Semi-insulating polycrystalline silicon (SIPOS) terminations provide a more uniform distribution of the field at the expense of an increased surface ohmic leakage (figure 3.9(f)). This kind of termination technique has been experimentally demonstrated for diamond SBDs and MESFETs [268]. After X-ray irradiation, in which the increasing irradiation doses generated a rise of the leakage current due to enhanced conduction through point defects or to the increase in the adsorbates in Al_2O_3, improvement in the BV was observed with no evidence of damage in the device. This clearly illustrates the potential of diamond for space and harsh environment applications.

MESA etching termination technique (figure 3.9(g)) has been widely used for Silicon based and 4H-SiC power bipolar devices due to the low complexity of the fabrication process. Almost ideal breakdown voltage has been obtained in 4H-SiC as the MESA structure limits the lateral expansion of the depletion layer in the p- region due to the etching process. Such a termination technique could be adopted for diamond p-n junctions, as already suggested in [139, 193] However, one has to note that the optimal drift region thickness in diamond is larger than 10 µm for breakdown voltages above 3 kV [269] (theoretical) and etching thick diamond is a difficult process as the whole drift region must be etched. There is also the possibility of sidewall leakage induced by defects during etch, usually performed by Deep reactive-ion etching (DRIE). These considerations currently limit the possibility of MESA termination in the context of high voltage diamond devices. In conclusion, due to the current process limitations (especially the lack of controllable n-type doping), planar field plates and floating metal rings seems the most promising termination techniques for diamond devices.

3.4 Packaging, thermal management and reliability

Switching and conduction losses are less prone to generate thermal runaway effects in diamond power devices due to its exceptional thermal conductivity, the small intrinsic carrier concentration and the negative temperature coefficient of the R_{on_spec}. Nevertheless, some factors may limit the power-current handling capability of diamond at high junction temperatures. These factors can be identified in the Schottky contact temperature' limit and, most of all, in the packaging and passivation material.

Due to the novel nature of diamond devices, no dedicated packaging technique has been developed yet. A suggested package solution for efficient thermal dissipation and its equivalent Spice-type DC thermal network for a diamond power semiconductor has been illustrated in figure 3.12.

Cu is usually adopted as standard baseplate material for high power package topology, such as the SOT-227 [270]. However, the thermal expansion coefficient (TEC) of diamond need to be matched with the one of the baseplates. In the case of Cu, the mis-match between the TEC values could result in the lift-off of the die from the baseplate after several thermal cycles. Moreover, the ceramic substrate, which provides the electrical isolation for the device and the rest of the package, needs to be able to withstand high operating temperatures.

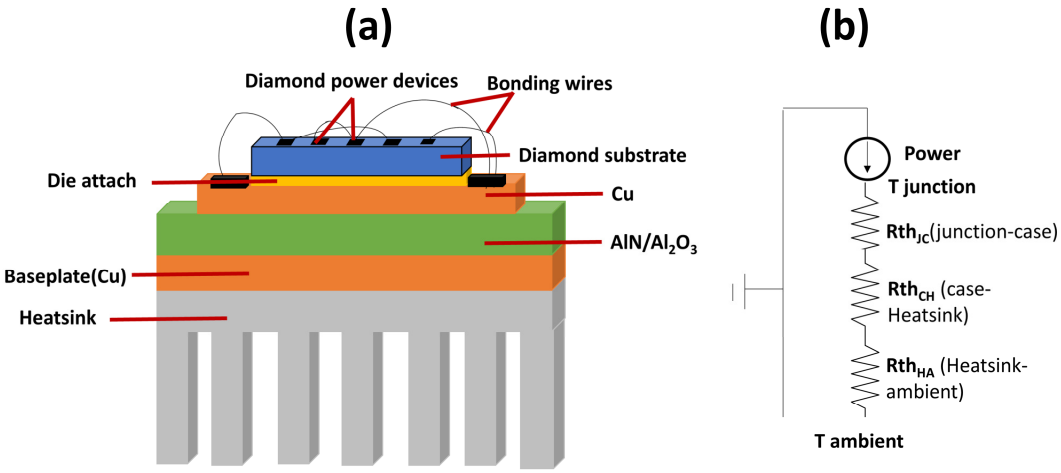


Figure 3.12: Schematic example of a package for a diamond device (a) and its Spice-type DC thermal equivalent circuit (b).

The choice of the solder alloy also plays a key role together with the protecting encapsulant which performance needs to be reliable for harsh environment

applications (i.e. high temperature but also high pressure). In the literature, few diamond devices have been packaged and tested in power circuits. MESFETs in [174] have been packaged on a typical metal-ceramic package where the device was bonded with Au and molded with a resin. In [70], vertical type Schottky diodes have been packaged with a silicone-based resin which has been then hermetically sealed by the stainless-steel cover. Similarly to lateral devices in GaN, lateral or pseudo-vertical diamond devices on insulating diamond substrates introduce a back side contact only for thermal interface and not as an electrical electrode.

As mentioned in chapter 2, diamond devices based on doped layers suffer from incomplete ionization of the dopants at room temperature. As a consequence, the R_{on_spec} has a negative temperature coefficient (NTC) when the total R_{on_spec} is governed by the "lightly doped" drift region. As demonstrated experimentally in [71], the switching losses are not affected much by increased temperatures. As a consequence, the total losses of diamond devices as Schottky diodes, MESFETs, depletion mode MOSFET and JFET have a NTC up to a high temperature where the losses are minimized (see chapter 6 for additional details). This important NTC modifies the design of the heatsink with diamond devices, where self-heating can be used to increase the temperature junction and to reduce losses at the same time. Consequently, the Rth_{CA}, equal to $Rth_{CH} + Rth_{HA}$ (figure 3.12), can be largely increased with diamond devices, leading at the same time to lower power losses and smaller and lighter heatsink, which is unprecedented at this scale in other materials. Nevertheless, as with other power devices with NTC coefficients, the thermal runaway and current focusing possibility are potential (and serious) issues. As an example, the parallelization of such devices can be challenging, especially when the diamond dies are poorly thermally coupled. Spice simulations carried out in [271] for diamond SBDs show that a small 10% dispersion in terms of R_{on} (due to process dispersion) for two diamond diodes can lead to current focusing effect due to the separate thermal heatsink. Moreover, the different current focusing on the two diamond diode results in different self-heating effects for the two diamond diodes with a sever imbalance in terms of temperature (>200 K) and power loss dissipation. Improved current sharing and temperature distribution could be obtained with a higher Rth_{CA}. However, this solution is not recommended to mitigate the characteristics dispersions between diodes, as it would lead to higher junction temperatures and limited surge current

capabilities. The consequences of this simple example are that diamond devices must be thermally coupled in the best possible way and that specific thermal simulations must be investigated to optimize the paralleling of diamond devices and for diamond power modules. On the same diamond die, one can expect that active cells paralleling will not be an issue due to the highest thermal conductivity of diamond, albeit with further investigations still required.

Reliability is one of the main concerns in diamond devices. Indeed, as the future generation of diamond power circuits is supposed to be working in extreme temperature conditions and for high frequency and voltage at the same time, the requirements on the overall system stability are even more strict than those for Silicon. Spin coated polyimide materials and other gels have been investigated for packaging high voltage SiC devices with a junction temperature exceeding 600 K and appear to be suitable also for packaging diamond devices [272]. Nevertheless, some gels exhibit quick degradation after a few thermal cycles at high temperatures, leading to cracks and a dramatic decrease on dielectric properties [273, 274]. Time dependent dielectric breakdown needs to be properly addressed as the increase of the electric field in the structure due to the high voltage ratings may lead to a time dependent failure of the protective layers. TDDB is a well-known effect in GaN devices where specific tests have been developed in order to assess the long-term reliability of oxide layers. Solutions adopted for HEMTs' lateral geometries have usually resulted in over engineering of the device with an increase of the lateral size of the unit cell in order to better redistribute the electric field in the structure. High frequency performance with fast dV/dt and dI/dt could be limited by stray inductances and capacitances with possible enhanced oscillations which may result in malfunctions or delay in the turn ON/OFF of the devices. Additionally, dynamic effects due to the non-zero activation energy of dopant species can seriously affect the switching performance of diamond devices and lead to charge imbalance effects with delayed turn OFF and local junction temperature' increase [153].

For these reasons, appropriate Gate driving techniques and the reduction of parasitics also need to be considered in the design of diamond devices. A more accurate evaluation of these effects will be provided in chapter 6.

3.5 Conclusions

This chapter has clearly highlighted that diamond vertical diodes are slowly approaching the competitors SiC and Si diodes in terms of ON state current density and breakdown voltage capability. Conversely, the majority of diamond FETs do not currently deliver useful performance at any temperature due to their poor current rating and their lateral structure. Vertical HFETs could be a valid solution to overcome such a limitation but issues related with the ON state resistance scalability, the relatively low BV and the complexity of the fabrication process could still represent an obstacle for the further development of this device. Several device termination techniques have been analysed in the second part of this chapter with FFRs and ramp field plate structures predicting >90% of efficiency.

Reliability and thermal issues of diamond have been examined. For bulk devices, in which the partial ionization of the dopants occurs also at RT, the effects and the drawbacks of operating at high temperature have been addressed. While a high operating temperature is advantageous in terms of conduction loss' reduction, this could possibly lead to enhanced leakage current and dielectric layer degradation.

4 DESIGN AND MODELLING OF UNIPOLAR MODE DIAMOND DEVICES

4.1 Introduction

Predicting the electrical characteristics and developing new device architectures is fundamental for advancing research in diamond power devices. In this chapter, three different categories of diamond unipolar mode FETs have been numerically analysed and modelled by means of finite element simulations.

Firstly, an improved normally-OFF design has been identified through an extensive design of experiments (DOEs) based on two dimensional TCAD simulations (section 4.2). The superior performance of the designed enhancement mode p-type JFET has been assessed at different operating temperatures and compared with that of the state-of-the-art diamond JFETs.[2] Secondly, a thorough investigation of deep depletion diamond MOSFETs' limits and capabilities has been carried out (paragraph 4.3). The impact of the Ib semi-insulating substrate and of the incomplete ionization on the electrical performance has been evaluated. Moreover, a novel dual gate device that allows a normally-OFF diamond deep depletion MOSFET is presented.

[2] The material in this chapter has been the object of the following publication: " Design of a normally-off diamond JFET for high power integrated applications," Diamond and Related Materials, *78*, pp.73-82, 2017.

In conclusion, a novel hybrid normally-OFF diamond MOSFET which merges together the deep depletion MOSFET concept and the surface channel conduction has been numerically analysed (section 4.4).

4.2 Junction Field effect transistors (JFETs)

A complete review of state-of-the-art diamond JFETs can be found in chapter 3. Here, we briefly recall the schematic working principle of a JFET working in the unipolar mode. For a more complete analysis of this device, the reader can refer to [152]. Figure 4.1(a) shows a typical 2D view of a normally-ON JFET with a conductive p-type channel region.

The two n-type gates control the depletion region width in the channel. In the unipolar mode, the gate-source and gate-drain junction are always reverse biased or shorted. The source potential (V_S) is typically grounded while the drain terminal has to be driven with a negative voltage (V_D). More specifically, the application of a positive voltage on the drain terminal would switch on the gate-drain junction and no current will flow between the drain and the source contacts. If a positive bias (V_G) is applied to the gate terminals (unipolar mode), the increased depletion region width allows to reduce the conductivity of the device.

Eventually, the pinch-OFF of the channel occurs when the depletion region width reaches half the channel thickness (W/2). This simplified assumption allows to derive a simple expression for the threshold voltage but is only valid for long channel JFETs (L>>W).

Different considerations need to be done in case of short channel JFETs in which the drain induced barrier lowering (DIBL) effect significantly modifies the band diagram in the channel region. Figure 4.1(b) shows the generic I-V characteristics of the JFET.

The drain I-V characteristics can be divided into three main regions: (a) The “linear” region observed at small drain bias where the drain current (I_D) can be considered proportional to the drain bias (V_D); (b) the “nonlinear” region, which encloses the pinch-OFF of the channel; (c) the “saturation” region where the current remains constant independently of V_D. In the last region, the drift velocity is not anymore

proportional to the longitudinal electric field and saturation occurs. This effect is more pronounced for short channel devices due to the higher internal electric field.

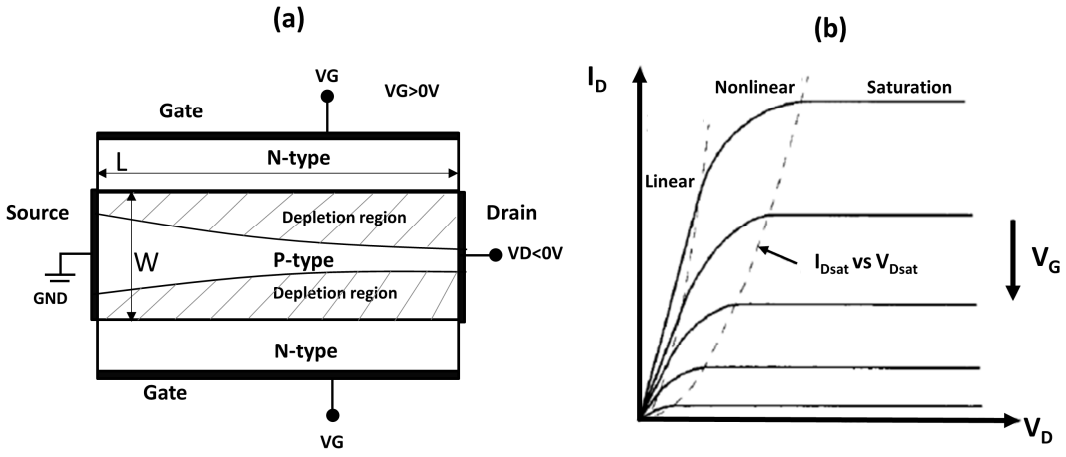


Figure 4.1: (a) Schematic 2D top view of a JFET driven in unipolar mode conditions and (b) general I-V characteristics[152].

4.2.1. Optimization of unipolar mode diamond JFET

In this section, normally-ON (depletion mode) and normally-OFF (enhancement mode) diamond Junction Field Effect Transistors (JFETs) have been analysed by means of a commercially available TCAD software[144]. Firstly, the ON- and OFF-state electrical characteristics have been simulated and matched with a set of available experimental data. The physical models and parameters used for the matching have been widely described in chapter 2 (mobility, high field dependence, impact ionization, etc.) and in chapter 5 (incomplete ionization).

4.2.1.1. Matching

In this section, experimental data for unipolar normally-on JFET [230] were compared with two-dimensional TCAD simulations. To reduce the computational time and optimize the TCAD simulations, a simplified 2D unit cell has been defined, shown in figure 4.2.

The choice of the simplified unit cell in figure 2 (left) is based on the fact that the device in [230] is symmetrical to a cut along the p-channel and the two lateral n+ gates are driven simultaneously (for power electronic applications). However, such

simplified 2D structure does not take into consideration some aspects of the real device structure.

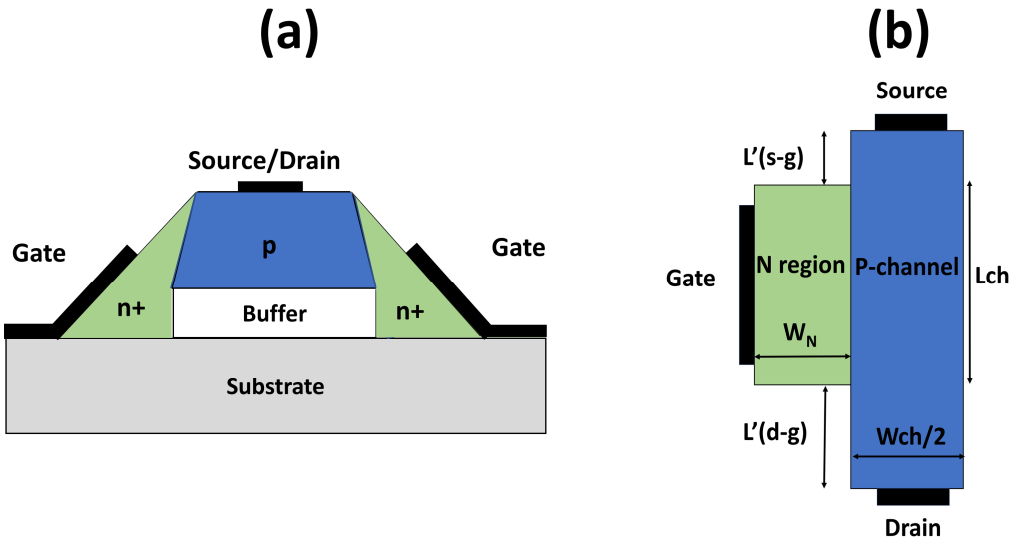


Figure 4.2: (a) Cross sectional view of the real JFET structure fabricated in [230].(b)Schematic 2D unit cell (top view) used for the TCAD simulations of the normally-on p-type diamond JFET. N region doping (phosphorous) is 8×10^{19} cm^{-3}, p-channel doping (boron) 1×10^{17} cm^{-3}, the channel length (L_{ch}) is 7 µm and the channel width (W_{ch}) is 0.5 µm. The drain, source and gate contacts have been defined with an ohmic boundary condition. Additional details about the structure can be found in [144, 230].

The buffer layer region is in fact not modelled in the 2D unit cell and the n-regions (phosphorus doped) are defined as rectangles whilst in the reality they have a trapezoidal shape due to the selective growth of n-diamond on the sidewalls of the p-channel(see fig. 4.2(a)). The simulations using the impact ionization (II) coefficients in the literature [162, 163] (and listed in paragraph 2.3.3) do not fit the reported JFET results.

Therefore, the values listed in Table 4.1 are adopted in this study. They, however, do not rule out other choices of a_p and b_p that result in the same breakdown voltage (BV), as projected by the scaling law [161, 162]. For this study, the impact ionization rates are assumed equals for both holes and electrons, as widely discussed also in [162]. This assumption is validated as an approximation by adopting the geometric average of the values for holes and electrons as the common value.

Additionally, a temperature dependence of the ionization coefficients has been included, as shown in the equation (13a) through the parameter γ (see equation 13b).

This parameter expresses the temperature dependence of the phonon gas against with holes and electrons are accelerated [150, 275].

Table 4.1. Diamond impact ionization coefficients for the Chynoweth model (1a) used for the matching of experimental JFET data.

Impact ionization Coefficients	a_p (/cm)	a_n (/cm)	b_p (V/cm)	b_n (V/cm)
	5.48×10^6	5.48×10^6	6.5×10^7	6.5×10^7

$$\alpha_{n,p} = \gamma a_{n,p} \exp\left(-\gamma \frac{b_{n,p}}{E}\right) \tag{13a}$$

$$\gamma = \frac{\tanh\left(\frac{h\omega_{op}}{2kT_0}\right)}{\tanh\left(\frac{h\omega_{op}}{2kT}\right)} \tag{13b}$$

In (13b), T_0 is the room temperature (300 K) and $h\omega_{op}$ is the optical phonon energy assumed equal to 0,063 eV [150, 275], which is the default value for Silicon. Figure 4.3 shows the breakdown voltage obtained from the numerical simulation of the 2D cell at different temperatures and its comparison with the measurement data, showing a good agreement at T=300 K and a slight overestimation at higher temperatures (T=473 K).

For the OFF-state simulations, a constant background carrier generation rate of 1×10^{12} /cm^{3}s^1 has been added to improve the convergence.

Additionally, an external specific contact resistance of 1×10^{11} Ωμm has been attached to the drain metal to facilitate the convergence at the onset of the impact ionization phenomenon. The simulated breakdown current shows a steeper variation compared to the measured one [230] in correspondence of the voltages at which the leakage current increases with the reverse drain voltage. Indeed, the constant value of the simulated leakage current is fixed by the previous mentioned background carrier concentration and it is much lower than the experimental value of the leakage current which could be mainly caused by defects and impurities.

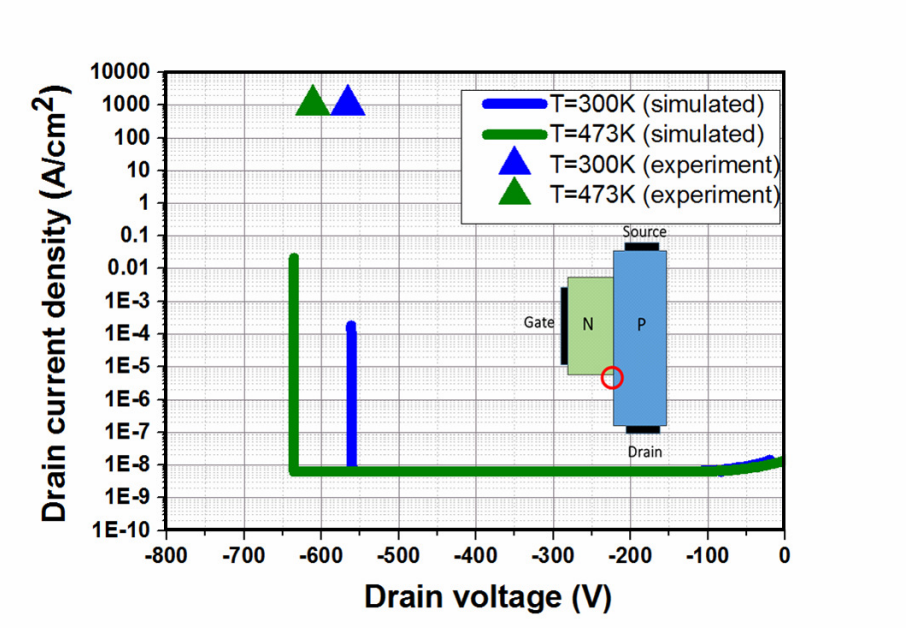


Figure 4.3: Breakdown voltage simulations for the normally-on JFET with the set of avalanche coefficients of table 4.1 at two different operational temperatures (300 K and 473 K). In these simulations, the gate voltage (V_G) has been fixed at 20 V. The breakdown voltage has been extracted by visual inspection of the drain current (when this value increases of more than 3 orders of magnitude compared to the simulated leakage current) and compared with the experimental results [230]. The point where the highest electric field is reached is located near the p-n junction in correspondence of the red circle.

Moreover, the breakdown simulation stops converging after the current density increases of 4 to 5 orders of magnitude, before reaching the experimental value of ~1×10^3 A/cm^2. One can note from figure 4.3 a positive temperature coefficient of the breakdown voltage. This is a clear signal that the breakdown occurs as a consequence of the impact ionization phenomenon (see equations 13a-b) as opposed to the punch-through, which is expected to give a negative temperature coefficient. Additionally, a plot of the electric field in the structure (figure 4.4) displays the maximum electric field at the breakdown voltage which is located at the Drain-Gate junction in agreement with the experimental results reported in [230]. ON-state simulations at room and high temperature were carried out (figures 4.5 and 4.6) to verify the reliability of the proposed physical models. The small mismatch between the experimental results and the simulations in figures 4.5-4.6 can be mainly attributed to the non-uniform doping concentration in the p-channel of the real device and to the not uniform width of the channel [98, 183, 230] which has not been considered in this 2D design. For VG lower than -5 V the bipolar action of the JFET occurs and minority

carriers (electrons) are injected in the channel from the n+ regions, so increasing the total conductivity of the JFET, as reported in [232].

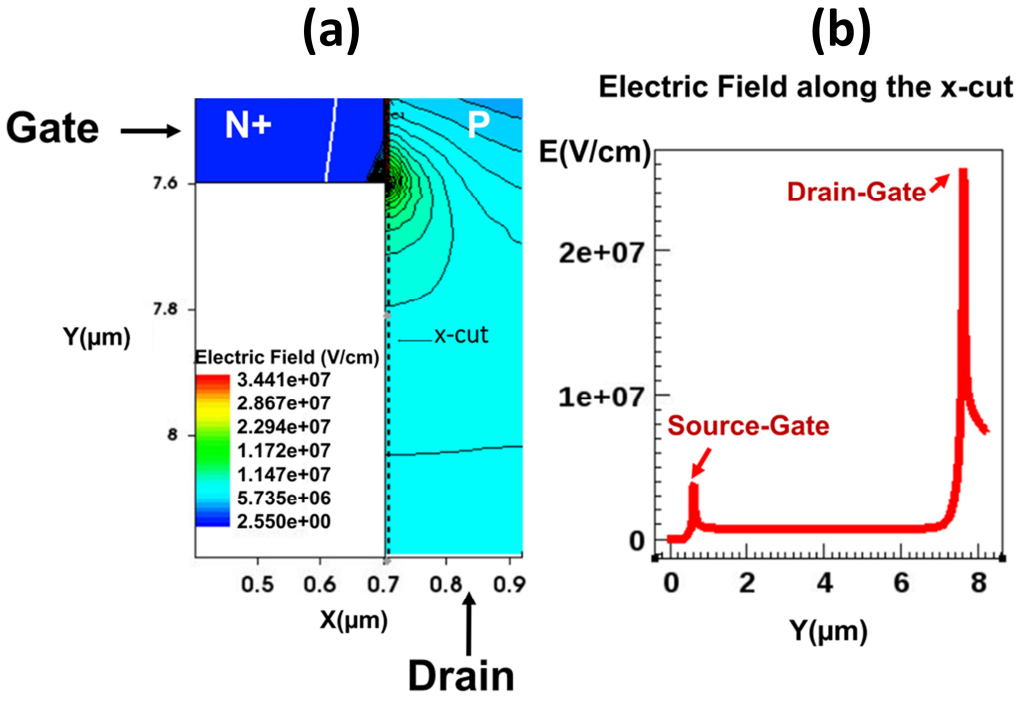


Figure 4.4: Electric field distribution at the gate-drain corner (a) at the RT breakdown voltage (V_{DS}=-570 V, V_G=20 V and T=300 K). The electric field distribution along an x cut (at x=0.7 μm) shows that the peak electric field value is located at the Drain-Gate corner (b), where a maximum value >20 MV/cm is reached.

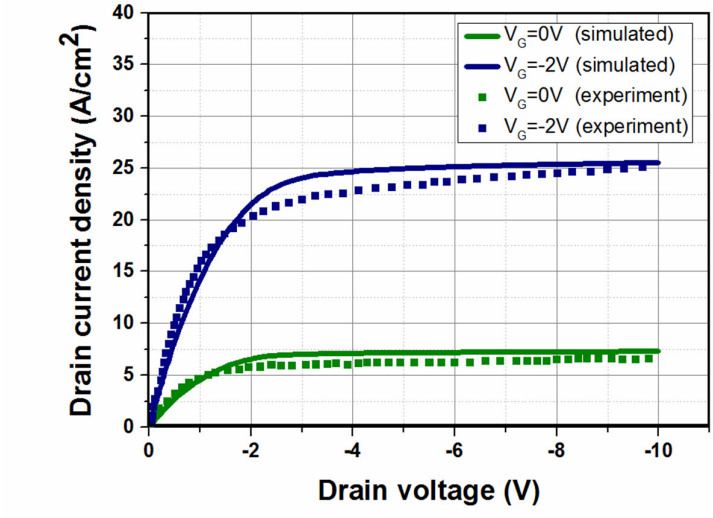


Figure 4.5: Measured [230] and simulated output characteristics for the structure in figure 2 for V_G= 0 and -2 V, and at T=300 K.

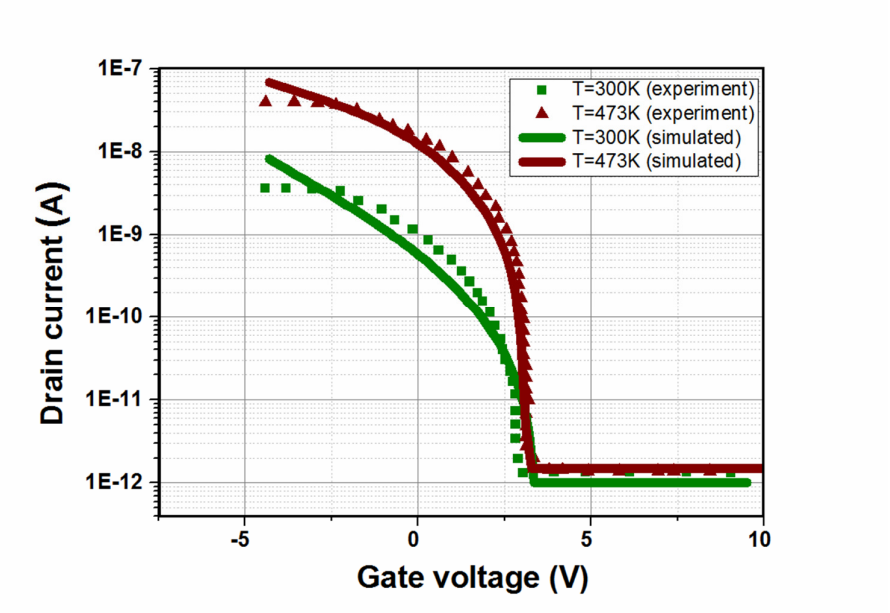


Figure 4.6: Experimental [230] and simulated transfer curves for the structure in figure 2 at T=300 K and 473 K (V_{DS}=-0.1 V).

To fully understand the potentials and the limits of the bipolar action in diamond JFET, a better insight into the recombination process and carrier lifetime is needed. However, this goes beyond the purpose of this work.

4.2.1.2. Design technique for a Normally-OFF JFET

Normally-OFF JFETs [152, 276, 277] are preferable over the normally-ON technologies as they are easier to drive due to the fact that they are less prone to unexpected behaviour during the switching. A possible way to convert a normally-on technology into a normally-OFF is via the cascode configuration where the high voltage normally-ON FET is connected in series with a low voltage FET [278]. However, this configuration has several drawbacks such as a higher specific ON-state resistance (R_{on_spec}), larger form factor due to unmatched voltage rating, and higher losses. Normally-OFF devices are therefore preferable to any normally-on based technology. On the other hand, in order to ensure a normally-OFF operation in diamond-based FETs, the channel width together with the channel doping have to be reduced. This is detrimental in terms of R_{on_spec} [279]. A recent publication demonstrates the first attempt to realize a normally-OFF diamond JFET device [231]. In the proposed device, the submicron channel allows the depletion regions to touch

each other when the gate is at zero bias and provides the normally-OFF behavior. This device is the first experimental demonstration of a normally-OFF FET in diamond and some improvements in the design are still possible. The ON-state current density (R_{on_spec}~20 Ωcm^2 at V_G=-4 V) is more than two orders of magnitude lower than those of the normally-on JFET devices proposed in literature and the small channel width (0.2 μm) makes it difficult to control the uniformity of the channel in terms of geometry and doping profile. The work illustrated in this chapter proposes an improved design of this first normally-OFF JFET, taking into considerations the physical and technological limitations of diamond. It is worth noting that contrary to the conventional definition [280], the R_{on_spec} for diamond JFETs proposed in [230-232] has been calculated adopting the cross sectional area and not the planar one. Such approach can be validated only after the vertical operation is realized. For the design technique, we have used an extensive set of TCAD simulations based on the models discussed in chapters 2 and 5. Firstly, we defined a simplified 2D unit cell as already done for the normally-ON JFET, neglecting in this way some of the 3D effects which occur in the real device (see figure 4.2).

The main targets of the procedure are listed below:

- Normally-OFF operation at high temperatures.
- Minimum R_{on} specific (R_{on_spec}) per unit cell.
- Avoid Punch-Through breakdown.
- Breakdown target: 2 kV.

The breakdown voltage target has been chosen to be 2 kV. This value is comparable with the state-of-the-art breakdown voltage of other diamond FETs [21, 227, 281]. Then, we defined the input parameters (table 4.2) which are the gate doping (n-doping), the gate-to-source distance (L'(s-g)) and the gate width (W_N). The n-gate doping has been fixed at the value adopted for all the manufactured diamond JFETs (both in normally-on and in normally-OFF configurations) and it is equal to 8×10^{19} cm^{-3}; L'(s-g) is fixed at 1 μm.

This value guarantees a safe margin for the source contact deposition without an unnecessary increase in the drift resistance and it is of the same order of magnitude (μm) of the values reported for other JFETs in the literature [98, 183, 230]; the gate width W_N, is fixed at 0.7 μm.

Table 4.2. Fixed parameters for the design technique.

n-doping	W_N	L'(s-g)
8×10^{19} cm^{-3}	0.7 µm	1 µm

From these assumptions, we propose a technique to define an optimum value for the channel width (W_{ch}), the drain-to-gate distance (L'(d-g)), the doping of the channel (p-doping), the channel length (L_{ch}) and the optimal operational temperature (Topt). The steps involved are described below:

Range definition

Step 1: identification of the optimal junction temperature. The choice is based on the minimum value of the resistivity. The optimal temperature has been chosen to be lower or equal to the maximum one (Topt ≤ Tmax).

Step 2: analysis of the channel doping due to the technological limitations and the requirements of the design ($P_1 \leq$ p-doping $\leq P_2$).

Step 3: evaluation of the limits imposed for the channel width in order to ensure the normally-OFF operation until the optimal temperature ($W_1 \leq W_{ch} \leq W_2$).

Step 4: TCAD simulations varying the channel length ($L_1 \leq L_{ch} \leq L_2$), the channel width and the doping of the channel are carried out based on the technological and physical limitations discussed in the previous steps. The influence of the channel length on the performances of the device is here discussed.

Optimization

Step 5: selection of the best design based on the principal targets. First, designs were selected for their capability to avoid Punch-through breakdown (>2kV) between RT and Topt. Then, designs with normally-ON operation before Topt have been discarded, and the best performing design in terms of minimum R_{on_spec} in the range RT ≤ T ≤ Topt, has been selected. Successively, the gate-to-drain distance (L'(d-g)) has been varied, to fulfil the target on the breakdown voltage (2kV). If the selected design does not allow to reach the required breakdown voltage specification, the "second best performing design" is considered and so on, until all the targets of the procedure have been satisfied.

STEP 1

Ensuring normally-OFF operation for a diamond JFET is not an easy task at high temperatures. This is because the doping activation increases with temperature, hence decreasing the depletion region extent in the channel. The risk is therefore that the device can become normally-on at high temperatures. This risk is enhanced also by the reduction of the built-in potential. In addition to this effect, higher temperature operations can lead to an increased p-n junction leakage current [98] which could reduce the breakdown voltage of the JFET. For these reasons, the design of a diamond normally-OFF JFET should be done keeping in mind the temperature effect. Moreover, the combined effect of the incomplete ionization and the hole mobility leads to an optimum resistivity (ρ) window. The resistivity (ρ) has been calculated as $(N_A(T)\cdot q \cdot \mu(T))^{-1}$, where q is the electron charge. As illustrated in figure 4.7, where the resistivity of p-type diamond has been sketched as a function of the temperature for different acceptor doping levels (N_{A0}) and a negligible value of the donor compensation doping (less than 1×10^{10} cm^{-3}), an optimum resistivity window can be identified between 450 K and 600 K. Since it is difficult to ensure normally-OFF operation up to 600 K without sacrificing too much the ON-state resistance (reducing the channel width and the p-doping) and without significantly increasing the gate leakage current, T=450 K has been selected as the optimum temperature (Topt) for this design.

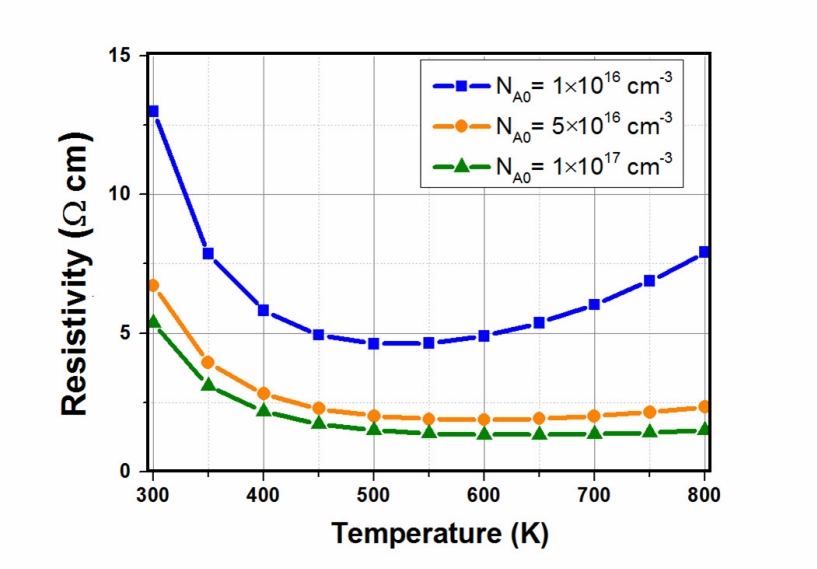


Figure 4.7: Resistivity of p-diamond vs temperature for different acceptor concentration (N_{A0}).

During the choice of the best performing design (step 5), we will guarantee that the optimal temperature is lower or equal to the maximum junction temperature (Tmax) at which the designed normally-OFF JFET becomes normally-ON (Topt ≤ Tmax).

STEP 2

Regarding the channel doping, which in this design is equal to the drift region doping, two main limitations can be identified. The first limitation is technological: it is not possible to accurately control the p-doping in diamond layers for values below 1×10^{15} cm^{-3}. This evidence sets a lower limit for the channel doping (P_1). On the other hand, when the doping is increased the electric field distribution in the drift region can easily become NPT (Non-Punch Through) and it could be not possible to fulfil the specification on the breakdown. Additionally, by increasing the drift region doping, the design of a normally-OFF JFET becomes more difficult since the channel width (W_{ch} in figure 4.2) has to be dramatically reduced in order to ensure normally-OFF operation. For all these reasons, the upper limit (P_2) for the channel doping has been fixed at 1×10^{17} cm^{-3}. The suggested channel doping window is therefore between 1×10^{15} cm^{-3} and 1×10^{17} cm^{-3}.

STEP 3

The lower and higher possible channel width values are here discussed. It is in fact necessary that the channel width is sufficiently small to be fully depleted at zero gate bias but at the same time it has to be wide enough to ensure current flow through the channel before the p-n+ junction switches on. This imposes two limitations: (i) the half channel width cannot exceed the depletion region at zero bias in order to be normally-OFF (limit W_1); (ii) the channel width cannot be lower than the depletion region calculated before the onset of the p-n junction in order to prevent the bipolar mode regime and ensure a safe voltage control of the gate (limit W_2). In this technique, the margin W_2 has been evaluated in order to provide at least 0.5 V before the onset of the bipolar mode (since we are dealing with a unipolar mode JFET). When the drain voltage is at zero bias, the depletion region can be calculated according to equations (14a-b), where the dependence of the built-in potential on the temperature and of the activated doping on the electric field and temperature have been included. For a uniform doping of the p-type channel and when the potential difference between source and drain is zero (V_{DS}=0 V), the depletion region width (W_D) in the channel, can be considered as independent on the position [152] and evaluated as in (14a-b). In

the formula ε_s is the dielectric constant of diamond, Ψ_{bi} is the built-in voltage, N_V and N_C are the density of states for the valence and conduction band and E is the electric field.

$$W_D = \sqrt{\frac{2\varepsilon_S[\psi_{bi}(T)+V_G]}{qN_A(T,E)}} \quad (14a)$$

$$\psi_{bi}(T) = \frac{kT}{q}\ln\left(\frac{N_A N_D}{N_V N_C}\right) + \frac{E_G}{q} \quad (14b)$$

In the space charge region (SCR) where the electric field (E) is significant, the number of activated dopants is higher compared to the one in the neutral region. Simulation results revealed that the effective width of the depletion region in the channel for the JFET cannot be theoretically evaluated taking into account a total activation in the SCR (N_A=N_{A0}) and TCAD simulations are so necessary for a correct design. Indeed, it is worth noting that the incomplete ionization phenomenon and the reduction of the built-in voltage slightly reduce the effective channel width at high temperatures, complicating the normally-OFF operations of diamond JFETs at high temperatures. Further analysis and details of this effect will be provided in chapter 5. Furthermore, the limits illustrated in figure 4.8 do not take into account the potential barrier lowering induced by the drain voltage. This phenomenon leads to the reduction of the electrostatic potential barrier in the channel region for increasing drain voltage. The reduced potential barrier can then allow for a significant hole current in the channel area even when the device should be in the OFF state.

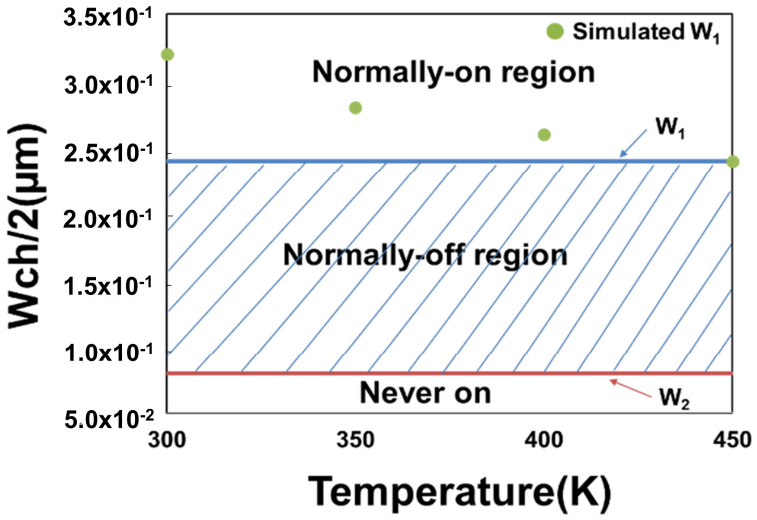


Figure 4.8: Channel width limitations for a p-type JFET calculated with formula (14a-b) for a channel doping of 5×10^{16} cm^{-3} and comparison with TCAD simulations (green points). W_1 (blue line) and W_2 (red line) have been calculated considering full activation and substituting V_G=0 V and $\Psi_{bi}(T)+V_G$=0.5 V in equation (14a) respectively.

The effect of the drain induced barrier lowering (DIBL) is more pronounced for short channel devices. The DIBL effect can switch on a device which should be "never on" and make it conduct a significant amount of current at high drain voltages.

STEP 4

TCAD simulations were performed based on the previous considerations in order to fulfil the primary targets (min R_{on_spec}, punch-through breakdown avoided and high temperature normally-OFF operation). In this set of simulations (table 4.3), a value of L'(d-g) is fixed at 2 µm and the avalanche generation has been disabled. As it will be explained later on, the L'(d-g) distance slightly influences only the on-state performances of the device and does not affect at all the PT (punch-through) breakdown which is mainly regulated by the channel length L_{ch}.

Table 4.3. JFET's parameters varied in the TCAD simulations.

L_{ch}	0.5 µm to 5 µm.
$W_{ch}/2$	0.1 µm to 0.5 µm.
p-doping	1×10^{15} cm^{-3} to 1×10^{17} cm^{-3}.

The channel length has a key role in the design of the normally-OFF JFET. This is because a high value of this parameter ensures a high blocking voltage avoiding the PT breakdown as shown in figure 4.9.

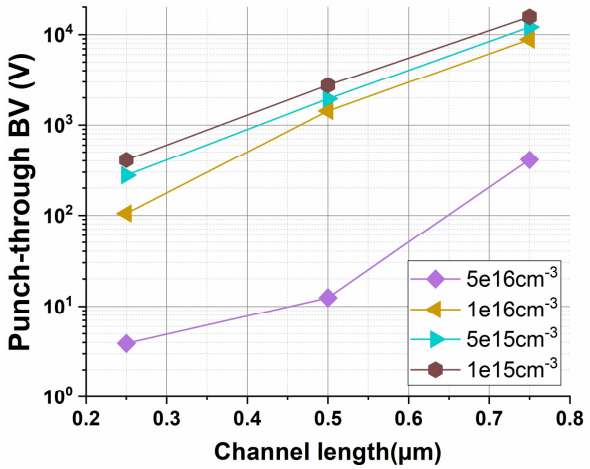


Figure 4.9: Punch-through (PT) breakdown vs channel length for different doping concentrations and for a fixed $W_{ch}/2$ of 0.2 µm. Punch through breakdown occurs when the potential energy barrier in the channel region lowers at high drain voltage and allows the flow of carriers (holes) from the source to the drain contact. This effect must not be confused with the PT design of the gate-drain region[152].

On the other hand, from TCAD simulations it has been found that the main contribution of the R_{on_spec} [280] is given by the specific channel resistance, R_{ch_spec} (more than 90% of the total R_{on_spec}). As shown in the equation (15a), R_{ch_spec} is proportional to the channel length (L_{ch}), the channel mobility (μ_{ch}) and the number of activated dopants in the channel (function of the gate voltage) $N_{ch}(V_G)$. Additionally, the specific drift resistance R_{drift_spec} (15b), which is the sum of the gate-source and drain-source specific resistance (R_{GS_spec} and R_{GD_spec}, respectively), is proportional to the total drift length (L_{drift}) which is the sum of L'(s-g) and L'(d-g), the drift mobility (μ_{drift}) and the number of activated dopants in the drift region (N_{drift}). The total R_{on_spec} (15c) is the sum of the specific resistance of the drift region (R_{drift_spec}), the channel region (R_{ch_spec}) and the contacts (R_{cont_spec}). Nevertheless, the resistance of the gate, drain and source contacts (R_{cont_spec}) has been neglected in this study.

$$R_{ch\_spec} = \frac{L_{ch}}{q\mu_{ch}N_{ch}(V_G)} \quad (15a)$$

$$R_{drift\_spec} = \frac{L_{drift}}{q\mu_{drift}N_{drift}} = R_{GS\_spec} + R_{GD\_spec} \quad (15b)$$

$$R_{on\_spec} = R_{ch\_spec} + R_{drift\_spec} + R_{cont\_spec} \quad (15c)$$

Since the R_{on_spec} is mainly due to the channel resistance, increasing L'(d-g) in PT can push upwards the BV (primary target) until PT ends up NPT, without lowering the ON-state performance. It is worth noting that the set of equations (15a-c) for the specific on-state resistance applies to vertical JFETs and it has been calculated adopting the cross sectional area instead of the planar one[280].

STEP 5

Designs which did not guarantee normally-OFF characteristics until Topt and were subjected to the PT breakdown have been discarded in this step of the optimization. Then, the selection of the best performing device has been based on the minimum R_{on_spec} at RT and at Topt. In the end, the L'(d-g) distance has been increased to fulfil the specification on the minimum breakdown voltage. At the end of the procedure, the final design has the following features (table 4.4):

Table 4.4. Final specifications for the optimized normally-OFF JFET.

W_{ch}	p-doping	L_{ch}	L'(d-g)	Topt
0.4 µm	$5\times10^{16}cm^{-3}$	1 µm	5 µm	450 K

Table 4.5. Avalanche breakdown as a function of the temperature and the gate-drain length. The 1D minimum length of the drift region (2 µm) does not allow to reach a BV=2 kV because of the 2D effects occurring at the D-G junction.

L'(d-g)	2 µm	5 µm	10 µm
T=300 K	BV=1.4 kV	BV=2.1 kV	BV=2.1 kV
T=450 K	BV=1.6 kV	BV=2.7 kV	BV=2.7 kV

An optimum value of 5 µm for this dimension has been found for a p-doping concentration of 5×10^{16} cm^{-3}. Increasing L'(d-g) over 5 µm has only detrimental effects in terms of R_{on_spec} (primary target) and does not improve the breakdown capability of the JFET (table 4.5). Further simulations with small variations of the parameters around the optimum configuration set have been conducted. However, a small reduction of the channel length, which is the main component of the R_{on_spec}, is detrimental for the PT breakdown as much as an increase of the channel width or of the channel doping.

4.2.1.3. TCAD results and discussion

Once the optimum design has been identified, TCAD simulations have been carried out in order to analyse the on-state and OFF-state performance of the final device. In figure 4.10, the RT on-state characteristics confirm that the device effectively behaves as a normally-OFF JFET.

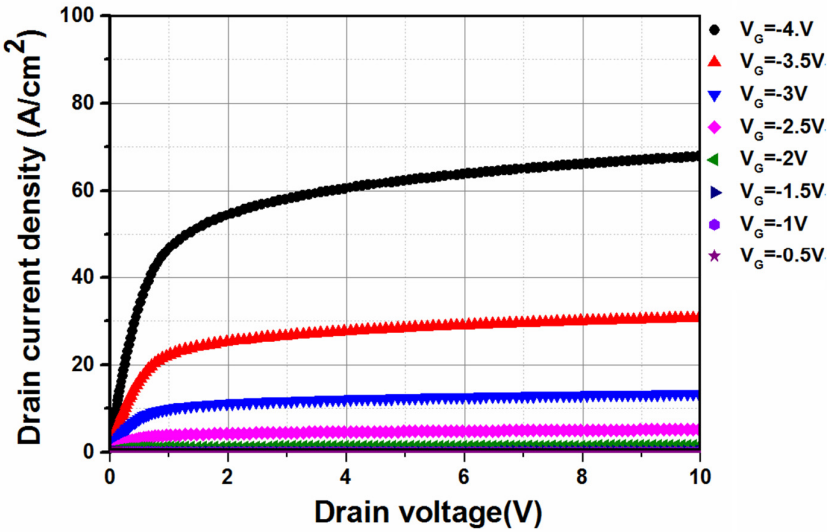


Figure 4.10: RT J_D-V_{DS} ON state characteristics of the optimum normally-OFF JFET for different gate bias.

The transfer characteristic in figure 4.11 illustrates that the optimum design is normally-OFF until the maximum temperature of 600 K (which allows to be inside the optimal resistivity window) and the threshold voltage ensures a good control in the unipolar mode (before the p-n junction turns on). For the same design specifications, the R_{on_spec} of a normally-OFF JFET with $L_{ch}=2L_{ch}$ (optimum) is almost doubled, confirming the predominance of the channel resistance on the total R_{on_spec}.

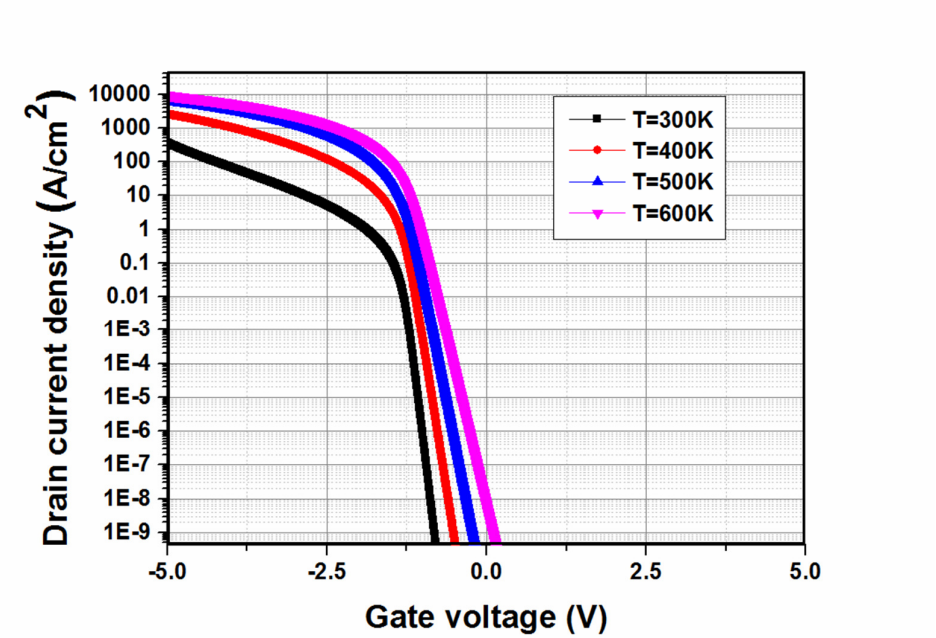


Figure 4.11: Transfer characteristics J_D-V_{GS} of the JFET at different temperatures for a fixed V_{DS}=-10 V. As it can be observed from the curves, the device becomes normally-on at 600 K (maximum temperature) since the threshold voltage becomes negative. The threshold voltage (Vth) is ~1V at RT and it reduces until ~0.4 V at the Topt , so guaranteeing a margin similar to the device reported in [232]. The threshold voltage has been defined as the gate voltage at which the drain current reaches the value of $1x10^{-9}$ A/cm^2 (constant current method [282]).

Breakdown voltage simulations showed that the avalanche phenomenon was responsible for the high increase in the current density (figure 4.12) and that the PT breakdown was effectively avoided by a correct design of the device (in terms of channel length and channel doping) also at high temperature.

The positive coefficient of the breakdown voltage (table 4.5) is indeed a clear signal of the avalanche phenomenon. In fact, the acceleration of minority carriers in the N+P (gate-channel) junction is reduced at high operational temperature because of the decreased impact ionization rate (equations 13). In the bar charts of figures 4.13,4.14

and 4.15 the performances of the normally-OFF device were compared with other diamond JFETs (in both unipolar/bipolar mode and normally-ON/OFF configurations).

At RT(fig.4.13), the R_{on_spec} of the optimized enhancement mode JFET shows only a small reduction if compared with the bipolar mode JFET [237] and a reduction if compared with the state-of-the-art unipolar mode normally-ON diamond JFET [98, 230].

At a high temperature of T=450 K (fig.4.14), the optimized JFET shows similar performances if compared with the bipolar mode JFET and it outperforms the other normally-on configurations.

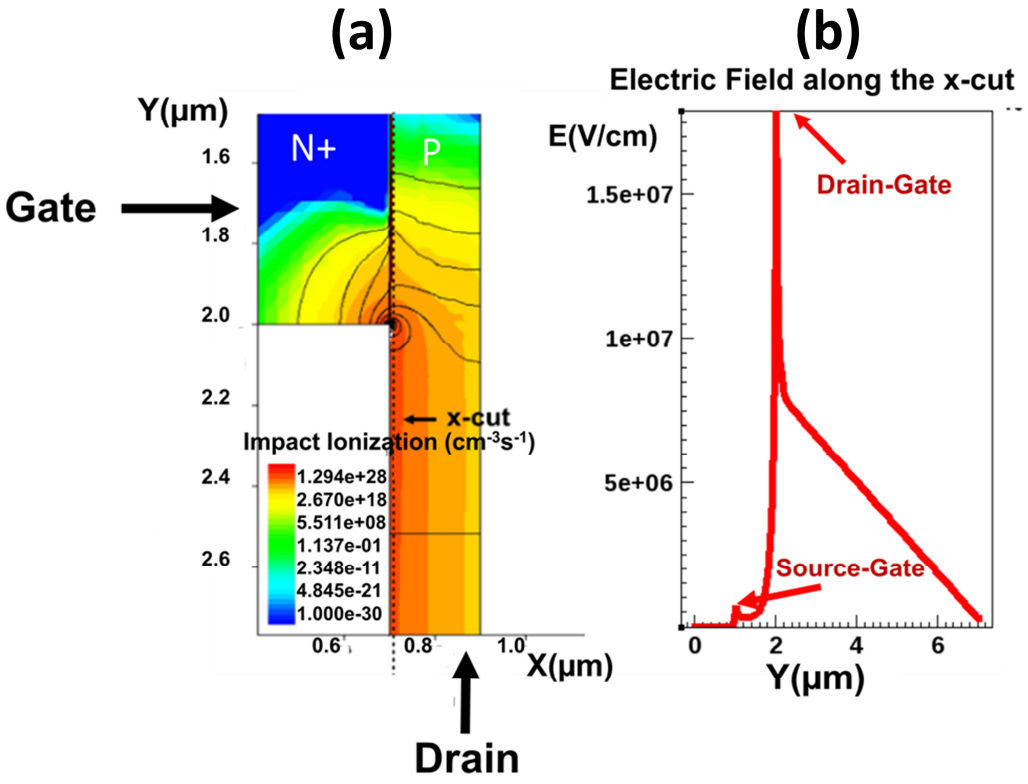


Figure 4.12: (a) 2D electric field distribution and impact ionization at the RT breakdown voltage (2.1 kV) for the normally-OFF optimum JFET. The peak of the electric field is located near the gate-drain junction, where the avalanche generation occurs. (b) The electric field reaches 0 V/cm before the drain contact, confirming the NPT design of the gate drain region, as it can be also deduced from the results of table 4.6.

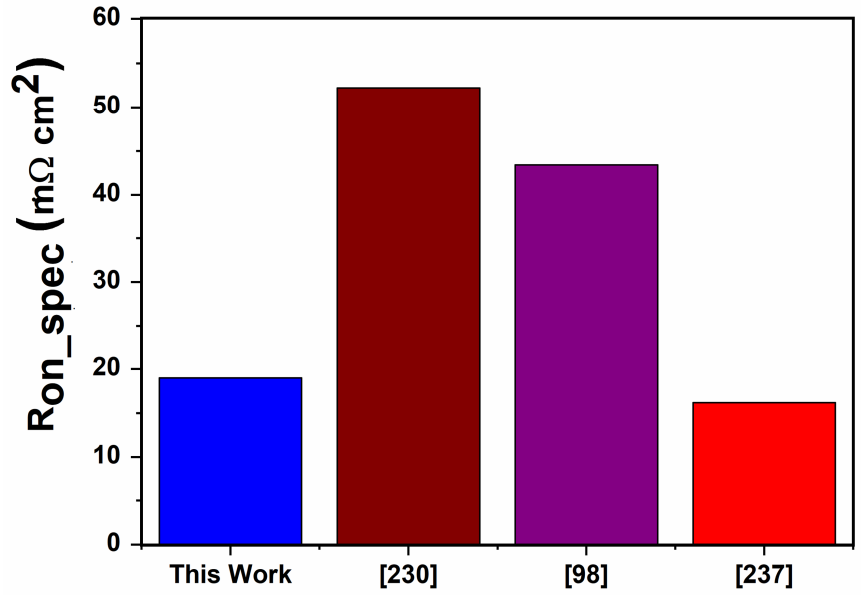


Figure 4.13: R_{on_spec} comparison between experimental results of diamond JFETs[98, 230, 237] and the optimised theoretical value for normally-OFF JFET at RT. R_{on_spec} has been calculated with the reference to the cross section and it applies to future vertical JFETs.

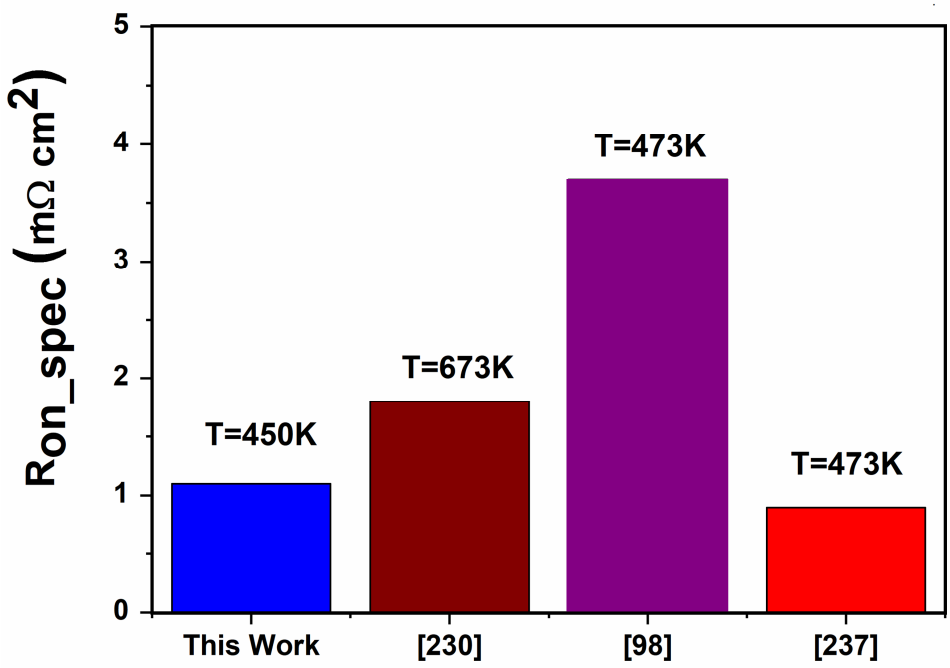


Figure 4.14: R_{on_spec} comparison between experimental results of diamond JFETs [98, 230, 237] and the optimised theoretical value for normally-OFF JFET at a high temperature of T=450 K.

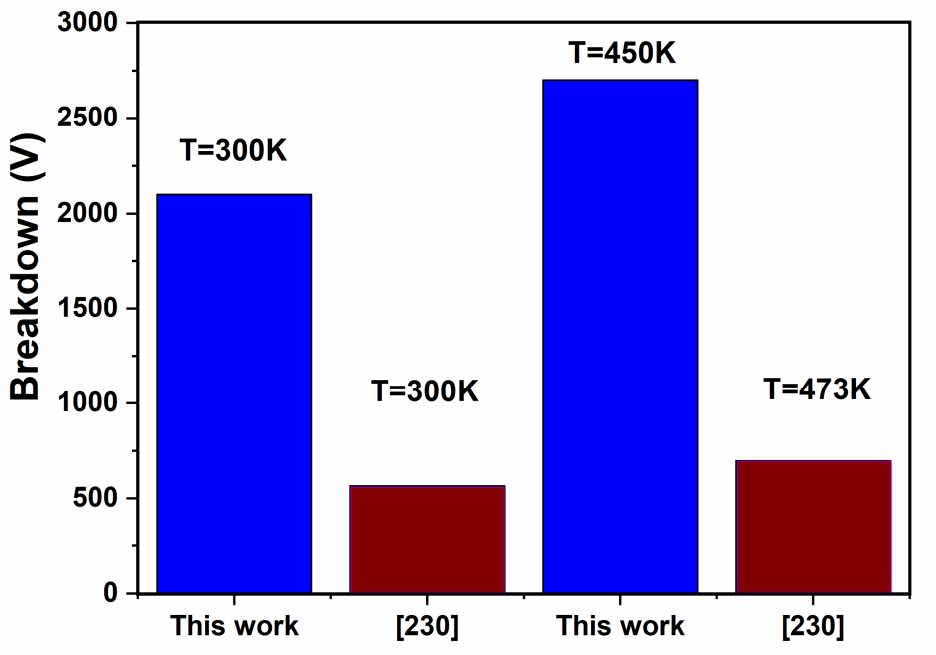


Figure 4.15: Breakdown voltage comparison of our theoretical optimized device and the diamond normally-ON JFET reported in [230].

4.3 Deep depletion MOSFETs

4.3.1. Introduction

The conventional surface inversion does not represent the only way to control the channel conductivity of MOS-based devices. An efficient solution for ultra-wide bandgap semiconductors (such as β-Ga_2O_3, Diamond, etc.) is the deep depletion MOSFET' concept, previously discussed in chapter 2. The physical operation of the deep depletion MOSFET resembles the Silicon based-buried channel MOSFET, a device analysed and experimentally demonstrated in the 1980-90s [152].

One of the intrinsic benefits of deep depletion FETs is the possibility of fabricating the device by employing a single doping type (either p or n). This can only be possible if the device is grown on a semi-insulating substrate (as the type Ib substrate for diamond) which permits to safely switch-OFF the device.

In this context, the lack of an efficient n-type doping in diamond and p-type doping in β-Ga_2O_3, perfectly matches with the configuration of the deep depletion MOSFET. However, some intrinsic limitations can hamper the development of this structure for power electronic applications and cause several reliability issues: the typical normally-ON (depletion mode) operation mode and the influence of the deep levels in the semi-insulating substrate. These issues will be discussed in the following paragraphs.

4.3.2. Diamond normally ON deep depletion MOSFET: analysis

A schematic cross section of a diamond lateral deep depletion MOSFET is shown in figure 4.16. To reduce the contact resistance, selective p+ growth could be performed prior the source and drain contact deposition as already demonstrated in [224]. The selected gate oxide is Al_2O_3, due to the good band alignment already mentioned in chapter 2. The gate metal is made of a single layer of Ti (WF=4.3eV) defined with a Schottky boundary condition in the simulations. To assess the limits of deep depletion diamond MOSFET technology, 2D TCAD simulations have been carried out. The experimental device structure fabricated in [226], has been defined in the TCAD device simulator (L_G=4 μm, tox=20 nm, Wp=0.23 μm, p-doping= $1.75x10^{17}$ cm^{-3}, L_{GS}=5 μm, L_{GD}=5 μm, for additional details on the structure the reader can refer to [216, 226]).

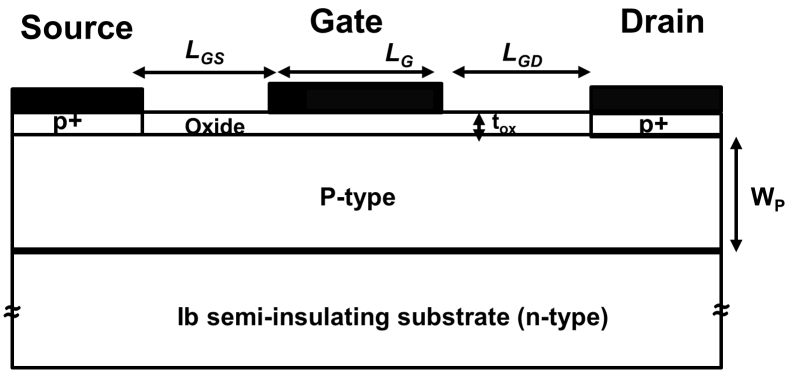


Figure 4.16: Schematic cross section of a deep depletion diamond MOSFET. Al_2O_3 properties have been modelled following [210], assuming a bandgap (E_G) of 8.8 eV, a low-frequency dielectric constant(ε) of 9 and an electron affinity (χ) of 1. These properties correspond to the α-Al_2O_3 phase. In diamond, the synthesis of Alumina usually leads to the formation of γ-Al_2O_3, which properties differ from the α-Al_2O_3 phase (for γ-Al_2O_3, E_G =6.3 eV-7.4 eV, χ~3 eV, ε~9). This can often lead to a different band alignment with both the conduction and valence band. Such a modification can have a high influence on gate-leakage current, as already addressed in [283]. For the purposes of this study, gate leakage mechanisms have been neglected.

The p+ regions have a thickness of ~10 nm and are doped with a boron concentration of $1x10^{20}$ cm^{-3}. The physical models defined in chapter 2 and 5 have been used for the finite element simulations illustrated in this section. If the Ib semi-insulating substrate is not modelled, ON state transfer characteristics (I_D-V_{GS}) have been shown in figure 4.17. As can be observed, the incomplete ionization effect reduces the effective carrier concentration and, therefore, the total current density.

Furthermore, the partial ionization also affects the behaviour of the device at higher operating temperature. More specifically, at high operating temperature, the threshold voltage (Vth) becomes more positive and the current density increases due to the enhanced ionization of the boron dopants. When the semi-insulating substrate is included in the simulations, an additional depletion region is generated at the substrate/channel region. The depletion region at the substrate/channel interface modifies the available conduction path for holes and affects the threshold voltage (Vth). These effects are clearly shown in the I_D-V_{GS} (figure 4.18).

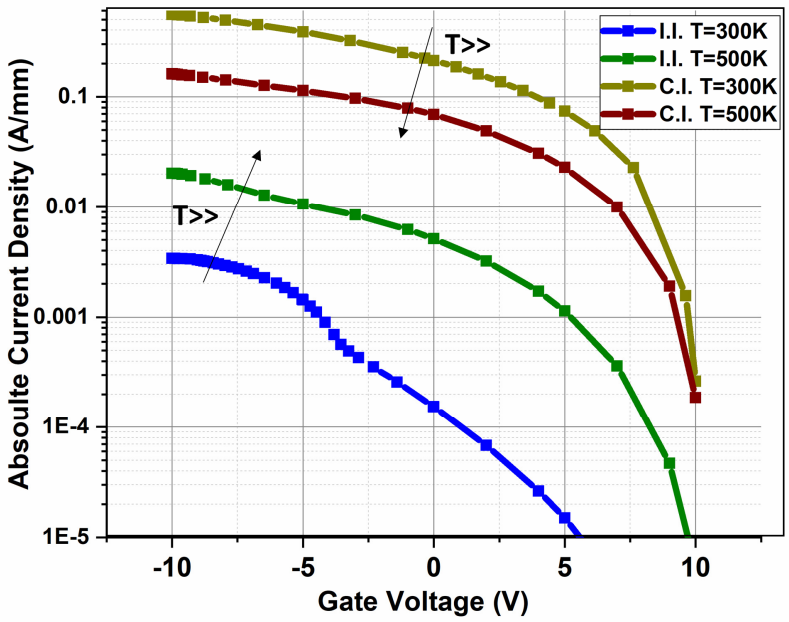


Figure 4.17: I_D-V_{GS} (V_{DS}=-10 V, V_S=0 V) characteristics for a diamond deep depletion MOSFET (figure 4.16) without the Ib semi-insulating substrate with the incomplete ionization (I.I.) and with the complete ionization (C.I.) model. The high field saturation model with the parameters described in chapter 2 has also been included. Thermal effects are neglected, and the drain current (y-axis) is normalized to the gate width.

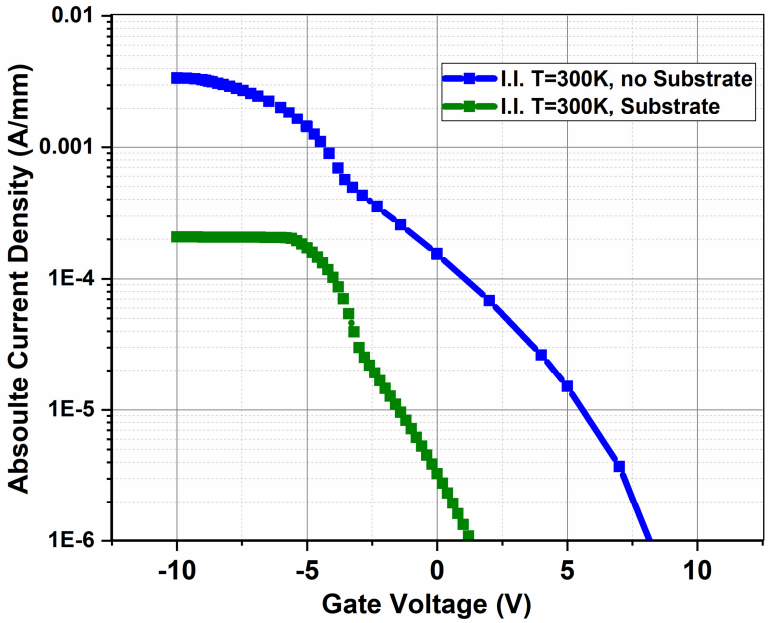


Figure 4.18: I_D-V_{GS} (VDS=-10 V, V_S=0 V) at T=300 K for the device in figure 4.16 with and without the semi-insulating substrate region. The HPHT Ib substrate has a typical thickness of hundreds of µm (usually ~300 µm). In the TCAD simulations, the simulated thickness has been reduced to 2 µm to optimize the computational time. The substrate is nitrogen doped (activation energy of 1.7 eV and with doping concentration of $3x10^{19}$ cm^{-3}) which leads to a very small percentage of free electrons. It is here worth mentioning that without any electrical contact deposited, the substrate only acts as a thermal interface. At T=300 K a negative threshold voltage of ~ 1.2 V has been extracted (normally ON device). Vth has been defined at a constant current density level of $1x10^{-6}$ A/mm here and in the following part of this chapter.

Hence, the sub-micrometer nature of the p-type conductive region does not allow to neglect this additional effect of the substrate. This could be understood from the equations (16a-c) which define the depletion regions at the MOS interface (W_{DS}) and at the channel/substrate interface (W_{DN}) (in case of floating substrate). $|V_{FB}| + \Psi_{bi}$ in equation (16a) is the modified "flatband voltage". The flatband condition is here identified with reference to the n-type substrate). As it can be understood from (16a), the substrate represents a virtual gate which can further control the width of the depletion region. In the eventuality that the substrate is electrically contacted, the expression $\Psi bi+V_B$ (where V_B is the substrate bias) replaces Ψbi in equation (16b).

$$W_{DS} = \sqrt{\frac{2\varepsilon_{ox}}{qN_A}(V_{FB} + \Psi_{bi} + V_G) + \frac{{\varepsilon_s}^2}{{C_{ox}}^2}} - \frac{\varepsilon_s}{C_{ox}} \tag{16a}$$

$$W_{DN} = \sqrt{\frac{2\varepsilon_s \Psi_{bi}}{qN_A}\left(\frac{N_D}{N_A+N_D}\right)} \tag{16b}$$

$$x_s = W_{DN} + W_{DS} \tag{16c}$$

In equations 16(a-c), ε_s is the semiconductor (low) frequency dielectric constant, ε_{ox} is the low frequency dielectric constant of the insulating layer (Al_2O_3), C_{ox} is the oxide capacitance, V_{FB} is the flatband voltage, x_s is the total depletion region width, N_A the doping of the p-type channel area and N_D the doping of the semi-insulating substrate.

In case of long channel device L_G>>Wp, a simple expression can be obtained for the Vth, which corresponds to the gate voltage (V_G) at which Wp=xs(V_G). Like for the inversion MOSFET theory [152], the equations for total current in the ON state can be derived with the channel charge approach. However, when the gate length (L_G) is reduced the drain induced barrier lowering (DIBL) effect occurs. This mechanism modifies the value of the Vth and it becomes much more difficult to derive an analytical solution. A few considerations can be done at this stage:

A) In principle, it is possible to control the ON/OFF performance of the deep depletion MOSFET with the substrate bias (V_B). This approach is well known for Si-based buried devices in which this specific substrate effect is employed for pinching-OFF thick channel devices (with large Wp). The substrate polarization is sometimes used as an alternative or in conjunction to the workfunction control to achieve normally-OFF behaviour for buried channel MOSFET. For this class of Si-based devices, there exists a maximum depletion width (and a maximum allowed gate voltage) before the inversion layer is generated. Nonetheless, it is not advisable to control the deep depletion FET with a back contact deposited on a semi-insulating substrate, even when a good ohmic contact can be formed. Indeed, due to the high activation energy (1.7eV) of Nitrogen, the dynamic ionization of the donor impurities will result in several reliability' issues such as gate and drain lag, extensively studied for GaAs MESFETs [284, 285]. A possible alternative to alleviate such issues consists in the deposition of a highly doped phosphorous layer before the channel growth. The lower activation energy of Phosphorus species allows for reduced dynamic issues due to the reduced ionization/de-ionization time constant (as it will be discussed in chapter 5). However, this solution requires the availability of an accurate n-type doping control.
B) The maximum current density in figure 4.18 is several orders of magnitude lower than the maximum value reported for diamond H-FETs (~1 A/mm for the same bias conditions). High temperature and thicker channel region could

increase the total current density value but at the expense of an increased gate leakage and change in the threshold voltage. In particular, this last effect does not allow to easily design normally-OFF deep depletion MOSFETs.

C) The bulk conduction of deep depletion FET, which is one of the principal benefits of such a configuration, only occurs for low gate voltages. At higher gate voltages (the typical operation regime for a power MOSFET), surface conduction can dominate the transport mechanism, as already demonstrated for Si buried devices.

All these considerations push the research towards new device architectures which are able to alleviate the previous mentioned issues.

4.3.3. Diamond normally-OFF deep depletion MOSFET: the dual gate structure

A simple approach to obtain a deep depletion normally-OFF device consists in uniformly reducing the p-type layer width (Wp in figure 4.16) until the device is pinched OFF at V_G=0 V. One can note that, this configuration does not represent the optimal solution in terms of R_{on_spec}. A novel dual gate configuration, as the one depicted in figure 4.19, could alleviate this intrinsic trade-OFF between Vth and R_{on_spec} (figure 4.20). The recessed channel allows to obtain a normally-OFF configuration without using any substrate bias, while the thick p-region allows for a reduced R_{on_spec} if compared with a fully-recessed structure. Additionally, the thick p-region withstands the reverse voltage.

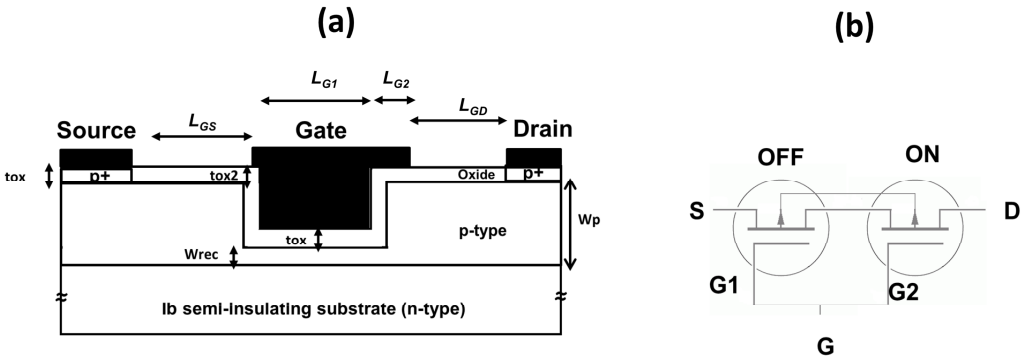


Figure 4.19: (a) Schematic cross section of the dual gate deep depletion diamond FET and (b) its equivalent schematic. The device in (a) can be seen as the series of a normally OFF FET and a normally ON FET (hence the definition of "dual gate").

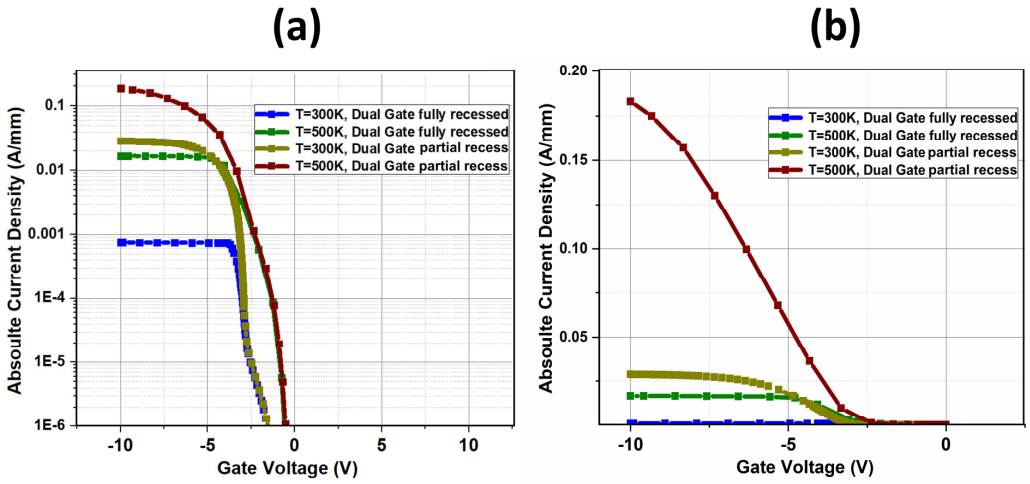


Figure 4.20: I_D-V_{GS} transfer curve (VDS=-10 V, V_S=0 V) in log (a) and linear (b) scale for the device illustrated in figure 4.19(a). tox=20 nm, tox2=0.2 µm, L_{GS}=1 µm, L_{G2}=0.5 µm, L_{G1}=0.25 µm, L_{GD}=5 µm. The p-region is uniformly doped at $2.5x10^{17}$ cm^{-3}, Wp=Wrec=0.1 µm for the dual gate fully recessed structure whilst Wrec=0.1 µm and Wp=2 µm for the Dual gate (with partial recess). The partial recess does not alter the Vth and has a positive effect on the total drain current density due to the current spreading effect. Vth is ~-1.55 V at T=300 K and it reduces to ~-0.55 V at T=500 K (extracted at a constant current density of $1x10^{-6}$ A/mm).

Regarding the fabrication process of the double gate deep depletion MOSFET depicted in figure 4.19(a), an additional etching step for the p-type region (in the channel area) is required. Alternatively, it is also possible to perform a localized etch followed by the regrowth of the channel area. One of the potential drawbacks of the device in fig. 4.19(a) is the increased electric field in the corners at the bottom of the trench.

The latter fabrication step, which is well-known for other semiconductors' technologies [286] and also in diamond [253], generally improves the semiconductor/oxide interface' quality. With the re-growth of the channel area, an additional degree of freedom is introduced in the design of the dual gate MOSFET. In particular, it is possible to decouple the channel doping and the drift region one.

More specifically, the doping of the p-channel (typically one of the most resistive regions in the device) can be increased whilst the doping of the drift region area, which needs to withstand the reverse voltage, can be reduced. The superior ON-state performance of the dual gate structure has been compared with a fully-recessed solution in figure 4.20. The inclusion of a mobility degradation model at the interface (default set of Lombardi degradation model and parameters for Silicon [150]) provides a more realistic value of the channel mobility at the Al_2O_3/diamond interface. The results with the mobility degradation model have been plotted in figure 4.21.

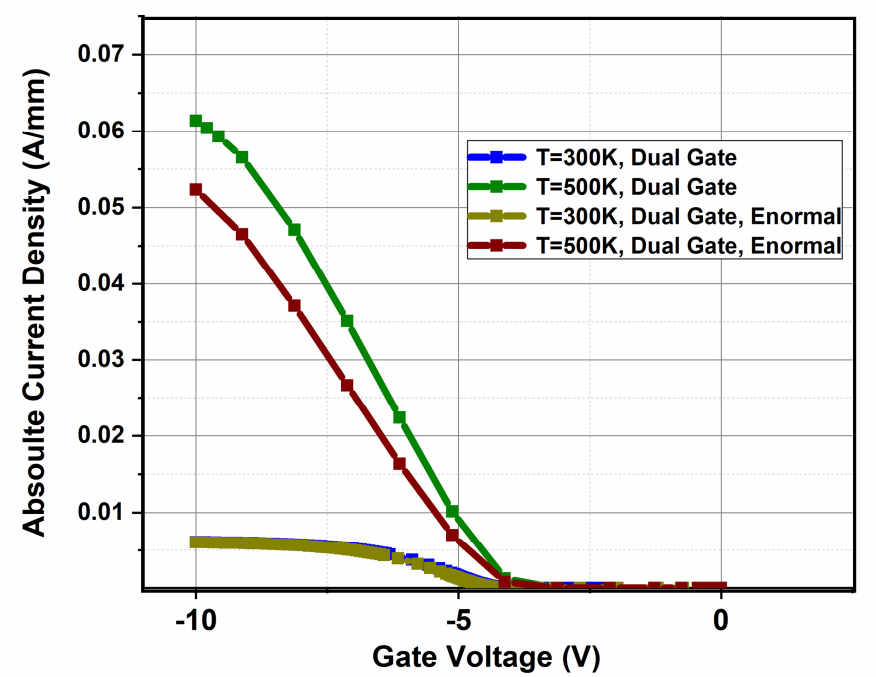


Figure 4.21: I_D-V_{GS} (VDS=-10V) with and without the degradation mobility model at the interface (Lombardi model). tox=20 nm, tox2=0.2 µm, L_{GS}=1 µm, L_{G2}=0.5 µm, L_{G1}=0.25 µm, L_{GD}=5 µm, Wrec=0.1 µm, Wp=2 µm and the p-region is uniformly doped at $5x10^{16}$ cm^{-3}.With this choice for the p-doping, Vth is ~-3.85 V at T=300 K and it reduces (in absolute value) to ~-3.3 V at T=500 K (extracted at a constant current density of $1x10^{-6}$ A/mm). This improvement for the Vth is paid in terms of maximum current density (reduced of about 50% if compared with the device simulated in figure 4.20).

Regarding the OFF-state performance, it has been found that quasi-stationary simulations fail to predict the real punch-through capability of the device shown in figure 4.19(a). Indeed, due to the presence of deep levels (i.e. nitrogen), the dynamic activation of donors in Ib semi-insulating substrates cannot be neglected even when small dV/dt are applied to the device.

"Slow" transient simulations (see additional details in the caption of figure 4.22) show that the presence of the Ib substrate leads to a premature breakdown due to the punch-through of the device. According to the usual punch-through breakdown mechanism (i.e. in the absence of deep levels), a negative temperature coefficient of the breakdown voltage (BV) can be observed.

The transient BV due to punch-through effect is caused by the reduced number of activated nitrogen ions in the substrate. This decrease leads to a weaker potential barrier at the channel/substrate interface (figure 4.23).

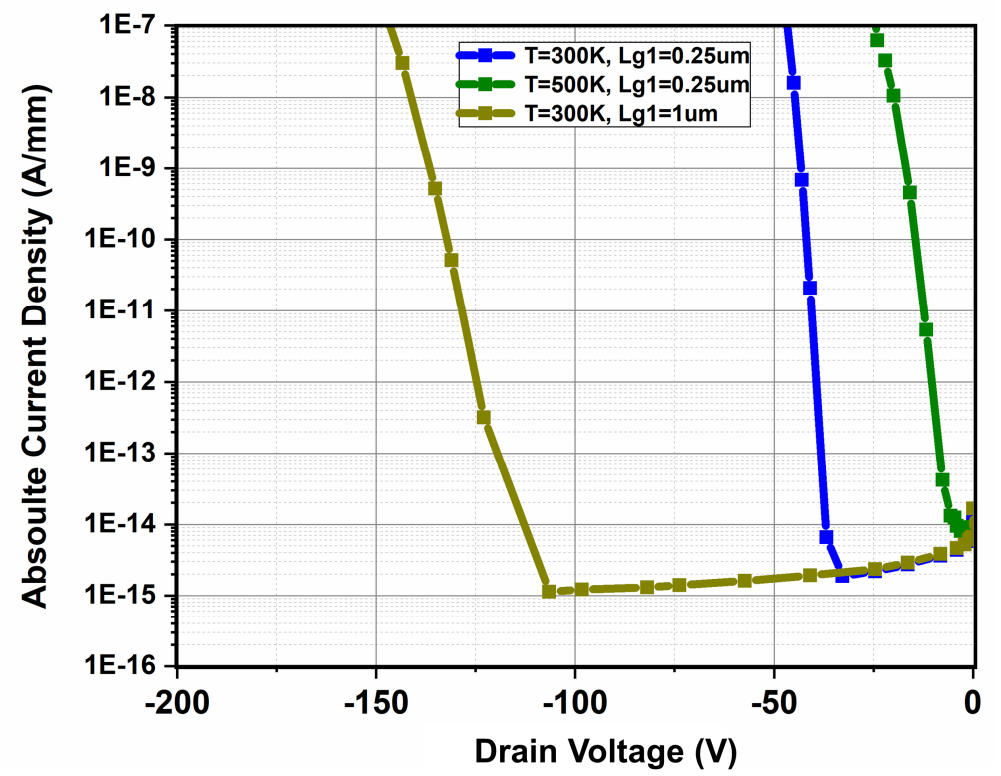


Figure 4.22: Transient ID-VDS (V_G=0 V) simulations for the device depicted in fig. 4.19(a) (details of the structure in the caption of figure 4.21). The slow dV/dt applied at the drain contact is 1 V/100 s. Avalanche is deactivated in these simulations. A longer gate length improves the PT BV resistance of the device. Due to the extremely high activation energy of Nitrogen, temperature has only a minor effect on the ionization/deionization time constant.

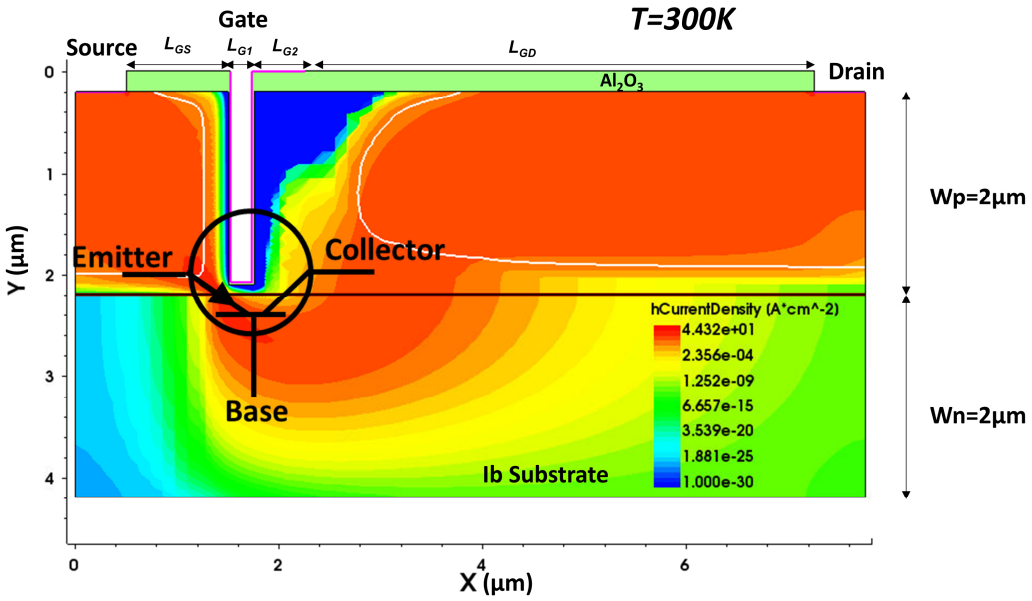


Figure 4.23: PT mechanisms for L_{G1}=0.25 µm at RT (details of the structure in fig. 4.21). As it can be seen from the plot, holes overcome the electrostatic potential barrier in the channel and are injected in the substrate before reaching the drain terminal. The parasitic p-n-p BJT (with floating base) has been schematically depicted.

The occurrence of the premature breakdown voltage due to punch-through in the device, can be efficiently tackled with the growth of a highly doped phosphorous doped layer on top of the semi insulating substrate (upto T=500 K). The comparison in terms of punch-through BV has been plotted in the figure 4.24. As it can be seen, the presence of a phosphorous layer counteracts the occurrence of the premature breakdown due to the PT effect.

Nevertheless, two main drawbacks of this approach can be recognized: the difficulty in growing high-quality diamond phosphorous doped layer and the increase in terms of R_{on_spec}. In particular, due to the increased electrostatic potential barrier in the sub-micrometer channel area, the R_{on_spec} (and the total current density for the same bias conditions) is higher if compared to the structure illustrated in figure 4.16(a) (see figure 4.25(b)).

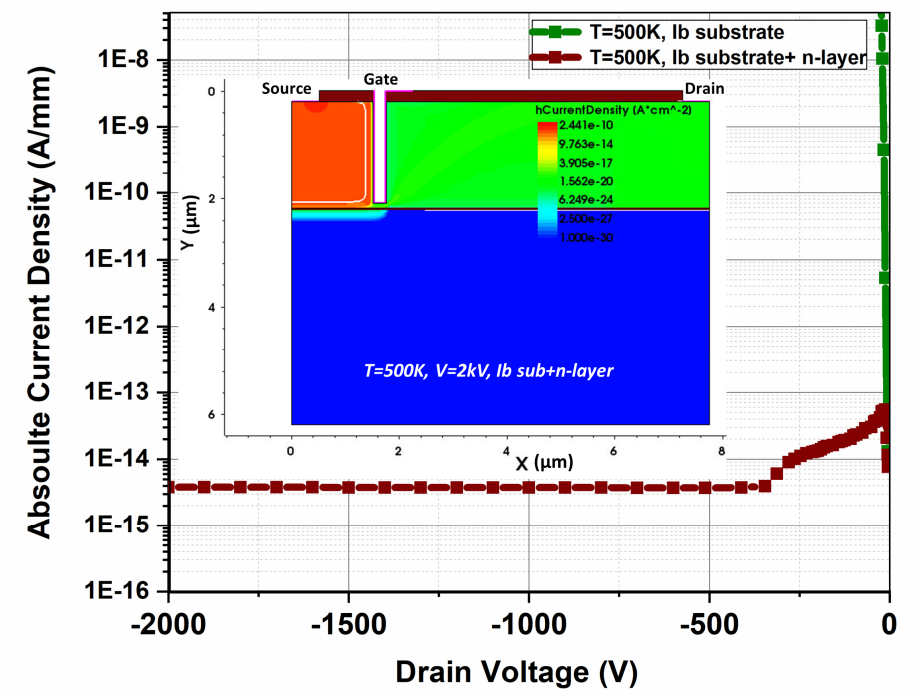


Figure 4.24: Reverse I_D-V_{DS} at T=500 K with and without the n-layer. The presence of an n-layer with shallow donors on top of the semi insulating substrate improves the PT resistance at high temperature. This is also demonstrated by means of the schematic cross section of the device, where the hole current density has been efficiently suppressed by the n-layer with a shallow donor level.

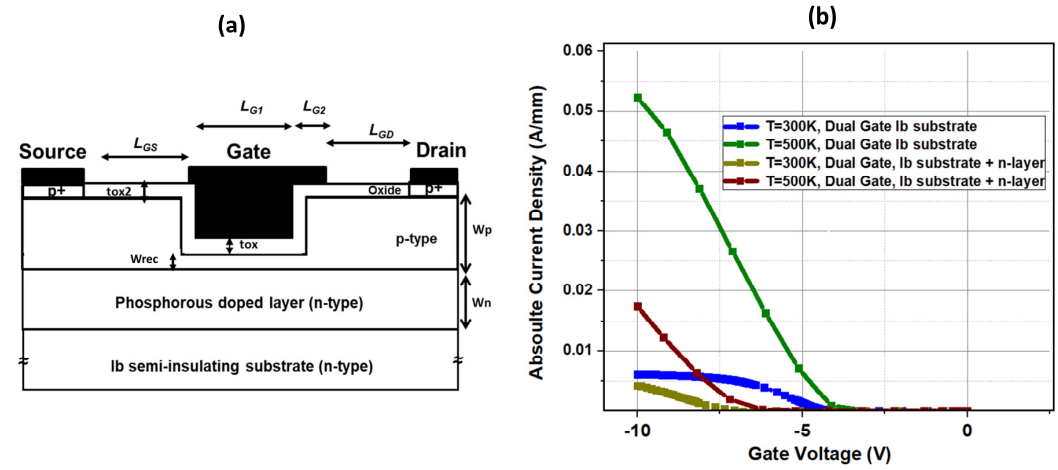


Figure 4.25: (a) Cross section of the dual gate deep depletion MOSFET with a phosphorous doped (n-type) layer and (b) comparison with the device illustrated in figure 4.16(a). The details of the structures can be found in caption of figure 4.21. The phosphorous doped layer is assumed to be 2 µm and doped at the same level of the nitrogen one ($3x10^{19}$ cm^{-3}). Vth=-6 V at T=300 K and Vth=-5.2 V at T=500 K with the additional n-layer.

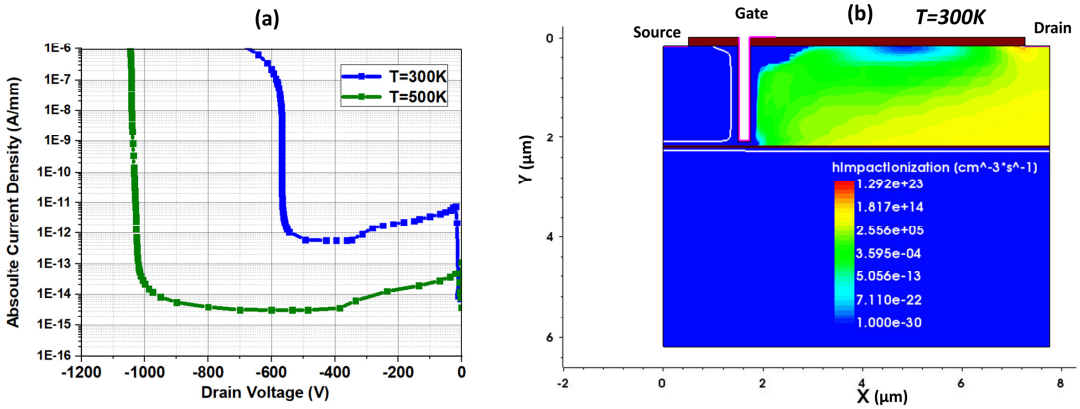


Figure 4.26: (a) ID-VDS at T=300/500 K and (b) hole impact ionization at T=300K at the BV for the structure defined in figure 4.25. The BV is ~600 V at RT and it increases to a value >1 kV at T=500 K. According to the simulations in the previous section, a constant carrier generation value has been defined in the simulations to improve the convergence. The reduced current density at T=500 K (which could be unphysical due to the presence of other leakage mechanisms [21, 108]) in figure (a) is due to the improved channel/substrate barrier due to enhanced ionization of phosphorus dopants.

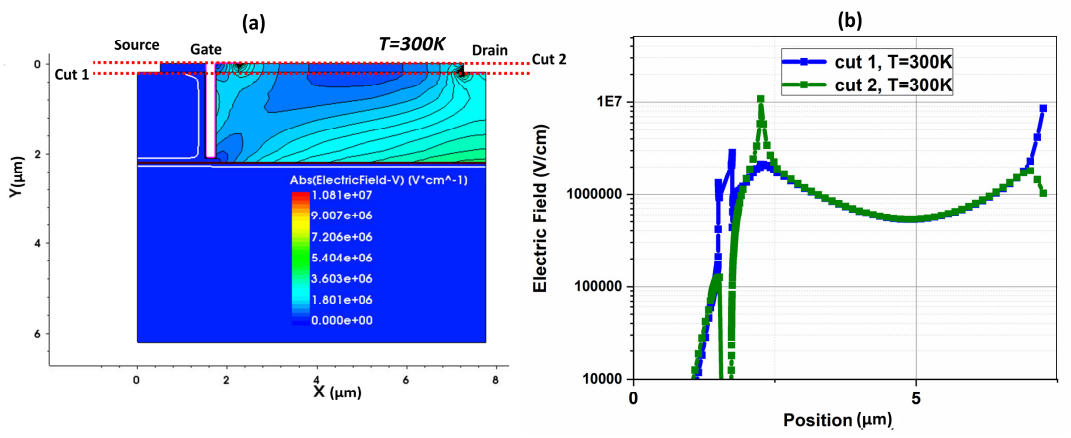


Figure 4.27: (a) Absolute electric field at V_{DS}~600 V (BV) at RT and (b) electric field cuts at the diamond/oxide interface (cut 1) and at the top oxide layer (cut 2).

To assess the avalanche capability of the proposed structure (in figure 4.25(a)), reverse bias simulations were performed with the avalanche coefficients defined in table 4.1. The reverse I_D-V_{DS} curves shows a positive temperature coefficient of the BV (figure 4.26) and the onset of the impact ionization near the drain contact (figure 4.26(b)).

The electric field at the BV (~600 V at T=300 K) has been plotted in figure 4.27, shows that the peak electric field reaches a value of ~1x10^7 V/cm in the oxide layer. This value is close to the maximum electric field in Al_2O_3 (1x10^7 V/cm) and should be kept as small as possible in order to avoid TDDB breakdown or oxide failure which may happen before the onset of the impact ionization. Nevertheless, it is worth mentioning that a more advanced device structure with a thicker passivation layer, longer gate-drain distance and a field plate structure could improve the avalanche capability of the device and, at the same time, reduce the stress in the oxide.

4.3.4. A hybrid normally-OFF configuration

The analysis carried out in the previous section has pointed out that the lack of shallow p-type and n-type dopant species is the main cause of the poor (simulated) performance of the diamond normally-ON and of the normally-OFF dual gate deep depletion MOSFET. As mentioned in chapters 2 and 3, one of the current issues of diamond HFETs is the scarce reproducibility of the device due to the high variation in terms of surface charge sheet concentration. This issue does not only cause dissimilarities in terms of current density, but, most of all, a huge reproducibility' problem for the

threshold voltage. Figure 4.28 shows the impact of the charge sheet concentration on the current density and on the Vth (see details in the picture). As it can be observed, doubling the charge sheet concentration leads to a huge variation >3.5V in terms of Vth.

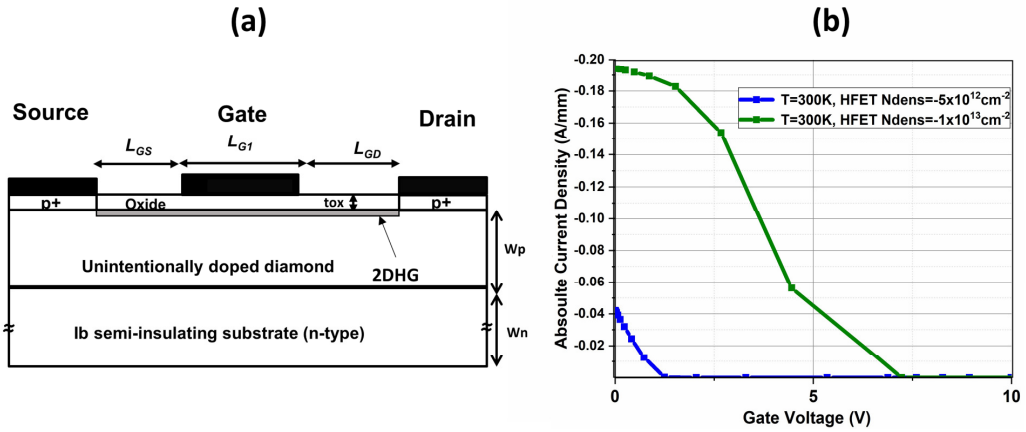


Figure 4.28: (a) Schematic cross section of the normally-ON HFET and its transfer curve (b). Vth=1.5V and Vth=5.45V for Ndens=-5x10^{12} cm^{-2} and Ndens=-1x10^{13} cm^{-2}, respectively. Vth has been extracted with the constant current method (J=1x10^{-6} A/mm). The specifications of the structure in (a) are Wp=0.2µm, p-dop=1x10^{15} cm^{-3} (unintentionally doped layer), Ib semi-insulating substrate is nitrogen doped with a thickness Wn of 2 µm and a doping concentration of 3x10^{19} cm^{-3}, tox=0.2 µm, L_{GS}=1 µm, L_{G1}=0.5 µm, L_{GD}=5 µm. The p+ layer is modelling the low-resistivity TiC usually forming at the hydrogen diamond/metal interfaces. In (b) VDS=-10 V and the Ndens represents the amount of interface fixed charge used to reproduce the effect of the 2DHG.

In [21], Kitayabashi et al. suggested a partial O-termination to control the performance of diamond HFETs, which are usually normally ON devices (see chapter 3 for additional details). The device fabricated by Kitayabashi et al. is a normally-OFF device and shows ON/OFF state performance similar to normally ON HFETs realized by the same research' group[243]. Nevertheless, it is not clear if the device works in inversion or depletion mode. The "unintentionally" doped substrate, on which the h-termination and the partial o-termination have been performed, contains a level of nitrogen impurities <1x10^{16} cm^{-3} and boron doping <1x10^{14} cm^{-3}. This probably suggests that an inversion layer is formed at this diamond/Al_2O_3 interface. The presence of a dominant deep level (nitrogen) in the channel/drift region of the device can however give rise to several undesirable effects during transient conditions, as widely discussed in chapter 5. It is also important to note another crucial aspect, more specifically, that diamond "unintentionally undoped" layers can have a significant doping level. Keeping in mind that hydrogen termination induces a surface channel also in vertical trenches, a similar idea could be applied to the device shown in figure

4.16(a). Figure 4.29(a) shows the schematic cross section of a dual gate deep depletion with hydrogen termination. A possible fabrication route of this structure would only require an extra fabrication step (compared to the device depicted in figure 4.25) in order to ensure the hydrogen termination of the areas depicted in figure 4.29. The inclusion of hydrogen terminated regions increases the ON state performance but with a possible drawback on the increased electric field profile in the OFF state. TCAD simulations have been carried out to further investigate the electrical performance of this structure. To reproduce the surface channel effect at the diamond/Al_2O_3 interface the charge sheet model of Kawarada et al. [108] has been used. The h-diamond mobility model, matched from experimental results (see chapter 2), has been included to correctly estimate the doping-temperature dependent mobility of the 2DHG. In figure 4.27(b) the superior ON state performance of the device have been illustrated. The reduction of the maximum drain current density at high temperatures due to the mobility reduction of the 2DHG. The threshold voltage follows the same trend of the deep depletion MOSFET, confirming that the Vth is regulated by the oxygen terminated interface.

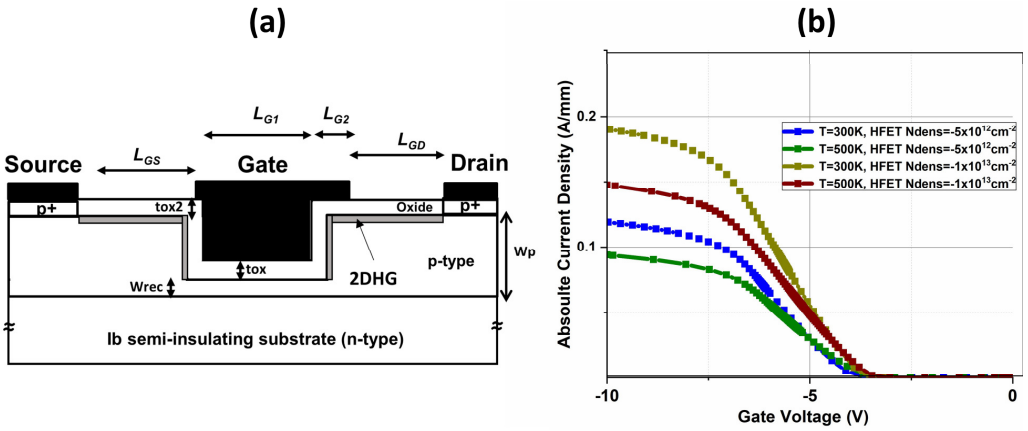


Figure 4.29: (a) Schematic cross section of the hybrid FET idea and (b) its I_D-V_{GS}((VDS=-10 V)). The extraction of Vth for different 2DHG concentrations in figure (b) leads to an identical Vth ~ -3.25 V at T=300 K and a Vth ~ -2.75 V at T=500 K (with the constant current method). This confirms the stability of the threshold if compared with the device in figure 4.28. tox=20 nm, tox2=0.2 µm, L_{GS}=1 µm, LG_2=0.5 µm, LG1=0.25 µm, L_{GD}=5 µm, Wrec=0.1 µm, Wp=2 µm. The drift p-region (unintentionally doped) is uniformly doped at $1x10^{15}$ cm^{-3} whilst the p-channel area is doped at $5x10^{16}$ cm^{-3}.

According to what demonstrated in the previous section, PT breakdown occurs for this structure in the absence of an n-type layer with a donor impurity level shallower than nitrogen (i.e. phosphorous). Nevertheless, the inclusion of a phosphorous layer only

leads to small reduction in terms of current density for this structure, as it can be observed in figure 4.28(a).

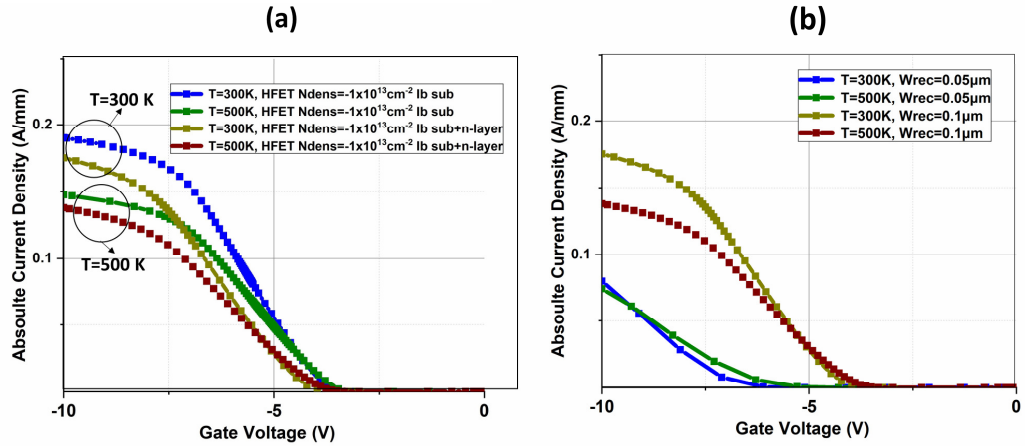


Figure 4.30: (a) I_D-V_{GS} with different 2DHG concentration at different temperatures and (b) the effect of Wrec on the ID-VGS (Ndens=-1x10^{13} cm^{-2}) of the Hybrid FET in figure 4.27(a) with Ib substrate and a phosphorous doped layer (2µm doped at 3x10^{19} cm^{-3}). In (a) the constant current method leads to Vth ~ -3.45 V at T=300 K and a Vth ~ -3.1 V at T=500 K with the n-layer. This value is higher than the one extracted without the n-layer, according to what demonstrated in the previous section.

One could note that in figure 4.30(b), the maximum current density of the hybrid solution is almost 2 orders of magnitude higher than the one in figure 4.25 (b) and it is also comparable with the state-of-the-art diamond normally-ON HFET. This confirms the great potential of this structure.

BV simulations have been carried out to assess the avalanche capability of the device. The reverse ID-VDS of the device in figure 4.29(a) (Ndens=1x10^{13} cm^{-2} and with the additional phosphorous layer) shows a positive onset due to the impact ionization effect with a BV=800 V at RT and >1.3 kV at T=500 K. The increase in terms of BV (compared to the device in figure 4.27) is due to the reduction of the drift region doping which is now made of an unintentionally doped region (boron concentration ~1x10^{15} cm^{-3}). Nevertheless, due to the presence of a fixed charge layer, which is required to model the 2DHG at the diamond interface, the electric field peak reaches a value >1x10^{7} V/cm. This could cause premature breakdown and can be tackled by increasing the oxide thickness (tox2= 400 nm), as shown in figure 4.31(b). This increase in terms of oxide thickness only leads to negligible discrepancies in terms of BV due to the impact ionization phenomenon.

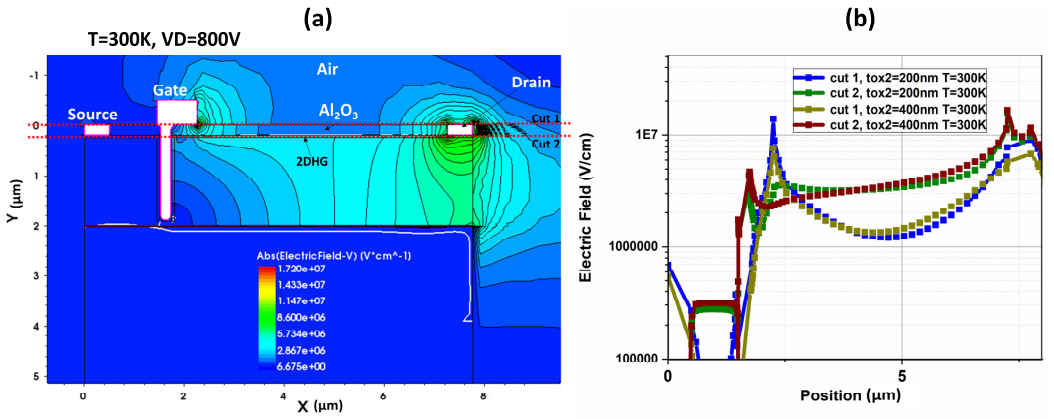


Figure 4.31: (a) Electric field distribution at the BV (T=300 K, VDS~800 V) for tox2=200 nm and (b) electric field cut at the diamond/air interface (cut 1) and diamond/ Al_2O_3 interface (cut 2). Ndens=-1x10^{13} cm^{-2} for the simulated device. Thicker Al_2O_3 helps the reduction of the maximum electric field in the oxide layer (<1x10^7 V/cm). A more realistic shape has been defined for the gate, source and drain metallization (with rounded corners). As the drain and source contact touch both the oxide and the semiconductor, the metal has been defined with a Schottky boundary condition and the hole-tunnelling has been activated at the source and drain interfaces. This is a common approach also for lateral GaN HEMT devices.

Nevertheless, it is worth noting that the breakdown and the reliability issues of the insulating layers become a major problem with diamond lateral FETs. More specifically, due to the high dielectric strength of diamond, the onset of the semiconductor breakdown (due to the impact ionization) usually occurs at very high voltage. At these extreme drain voltages, the peak electric field in the oxide has usually exceeded its critical value. This is also the case for high voltage diamond Schottky diodes[261].

Further modifications such as a longer gate-drain distance, the inclusion of a source field plate and a second passivation layer allow to improve the BV of the device while keeping the maximum electric field in the oxide lower than its critical value. This is shown in figure 4.32, in which a source field plate structure with a second passivation layer (made of Al_2O_3) helps to reduce the peak electric field in the oxide. However, this improvement is paid in terms of R_{on_spec} (figure 4.33) and turn on/OFF behaviour of the HFET (due to the additional field plate capacitance). An accurate analysis of all these issues goes beyond the purpose of this work.

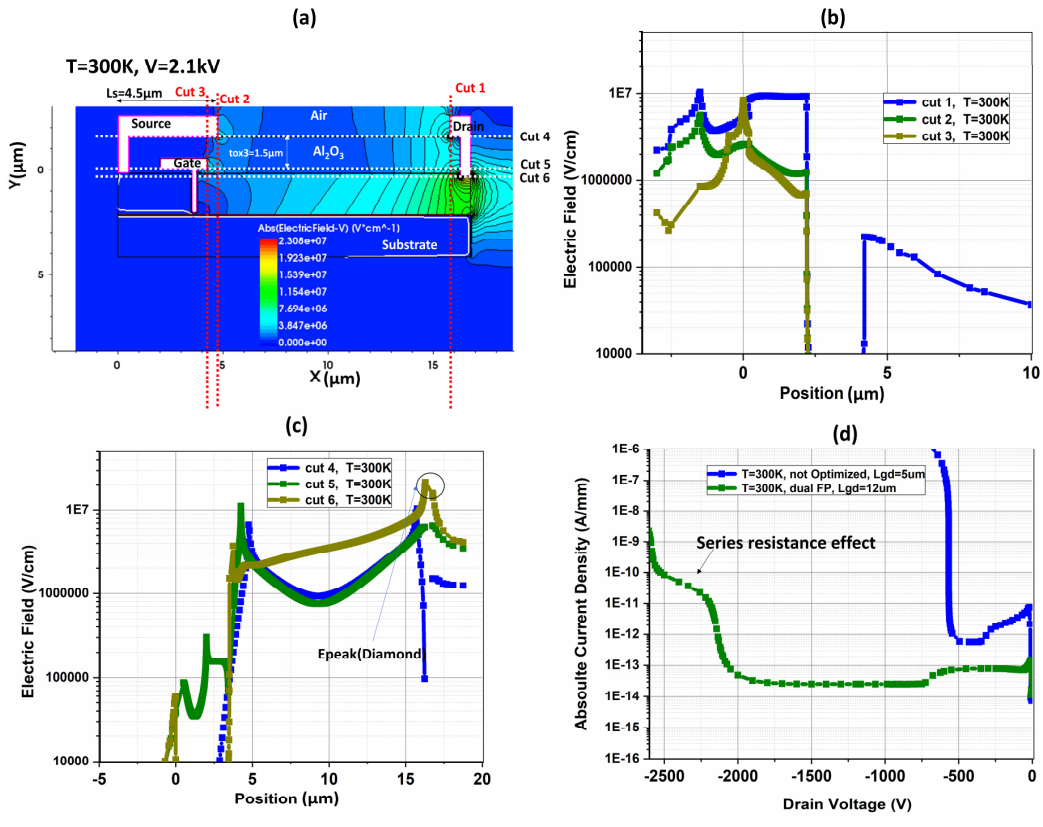


Figure 4.32: (a) Electric field distribution at the room temperature BV (~2.1 kV) with the dual field plate (FP) structure. The electric field profile along the vertical and horizontal cuts shown in figure (a) has been plotted in figure (b) and (c). Figure (d) shows the onset of the impact ionization (at RT) for the dual FP structure and its comparison with an unoptimized structure. The dual FP has a longer gate-drain distance (L_{GD})=12 µm and a second passivation layer made of Al_2O_3 (tox3=1.5 µm). The electric field peak is observed inside diamond and the peak field in the oxide is ≤1x10^7 V/cm. The structure has a dual field plate: one on the source and one on the gate.

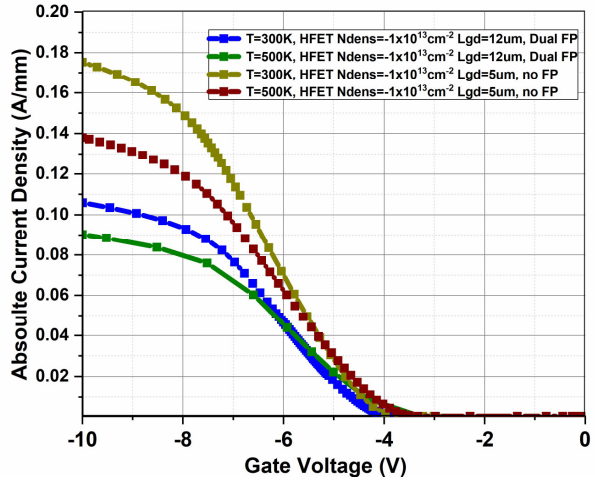


Figure 4.33: Dual FP ON state and its comparison with the unoptimized structure. Longer L_{GD} is the main cause for the reduction in the ON-state current.

In table 4.6 the performance of the simulated hybrid FET has been compared with the state-of-the-art diamond HFETs and GaN FETs. As it can be seen, the proposed device structure has the main drawback of increasing the R_{on_spec} if compared to GaN HEMTs, but shows an improved BV and threshold voltage (even at high temperature).

Table 4.6. Comparison of different lateral FETs made with diamond and GaN with the designed hybrid FET discussed in this section. R_{on_spec} has been calculated or extracted in the linear region (|VDS|=1 V and high overdrive voltage >5 V).

	R_{on_spec} x 10^{-3} (Ω · mm)	BV (V)	L_{GD} (µm)	Vth (V)
Dual FP Hybrid HFET (This work)	0.083 at T=300 K 0.1 at T=500 K	>2 kV at T=300 K ~2.35 kV at T=500 K	12	-3.5V V at T=300K -3.15 V at T=500K
Unoptimized Hybrid HFET (This work)	0.04 at T=300 K 0.055 at T=500 K	>800 V at T=300 K ~1.3 kV at T=500 K	5	-3.45 V at T=300K -3.1V at T=500 K
Diamond HFET Normally ON [108]	0.4 at T=300 K	1700 V at T=300 K	16	>20 V at T=300 K
Diamond HFET Normally OFF [21]	2.85 at T=300 K	2000 V at T=300 K	24	Between -2.5 V and -4 V at T=300 K
GaN HEMT normally ON[287]	0.025 at T=300 K	1700 V at T=300 K	10	~ -4 V at T=300 K
GaN HEMT normally OFF[288]	0.0123 at T=300 K	1200 V at T=300 K	15	~1 V T=300 K

4.4 Conclusions

In this chapter, the advantages and drawbacks of employing semiconducting diamond for lateral FETs configurations have been widely studied and assessed by means of finite element simulations. The main concepts and the findings of this study could be also extended to vertical configuration of diamond power FETs, the fabrication of which is currently limited by technological issues.

The temperature effect on the incomplete ionization of the dopants has proven to be the main limiting factor in designing diamond JFETs with normally-OFF behavior. A TCAD model was calibrated against existing data and an optimized structure was proposed which shows substantial improvement over the reported state of the art JFETs.

Similar considerations can be drawn for the deep-depletion MOSFET, which has been studied in the second part of this chapter. The reduced carrier activation due to the incomplete ionization effect limits the maximum achievable current density. Additionally, the lack of a shallow donor level in the semi-insulating substrate represents a serious risk for the punch-through breakdown of normally-OFF deep depletion MOSFET devices.

However, the hybrid operation of hydrogen and oxygen terminated diamond FET with the inclusion of a phosphorous doped layer, has demonstrated superior simulated performance compared to a standard deep-depletion MOSFET. Nevertheless, the improvements in terms of current density are paid in terms of an increase in the electric field in the oxide layer due to the presence of the 2DHG. These issues could be tackled with more advanced field plate terminations and the inclusion of a second passivation layer. In conclusion, the performance of the proposed FET has been assessed against the state of the art WBG-lateral FETs.

5 STATIC AND DYNAMIC EFFECTS OF INCOMPLETE IONIZATION IN DIAMOND AND WBG SEMICONDUCTORS

5.1 Introduction

The presence of deep dopant levels seriously affects the electro-thermal properties and the performance of wide bandgap (WBG) semiconductors-based devices. The outstanding research progress in this class of materials have been often hampered by the lack of shallow dopant impurities of one (as in GaN) or both types (as in Diamond), with an inherent difficulty in obtaining high carrier concentration levels. Contrary to Silicon, in which the shallow ionization energies of the dopant species allow to neglect this physical effect within a wide temperature-doping window, a more accurate modelling is mandatory for WBG semiconductors based electronic devices.

In this chapter, the impact of deep dopant levels modelled by means of the incomplete ionization equations is accurately studied. Firstly, the physical models and the static effects of the partial ionization of the dopants which lead to temperature-electric field activated impurities are systematically investigated with the reference to a 1D p-n junction. Secondly, the consequences of the dynamic ionization are considered for a 2D Superjunction (SJ) device structure, and a detailed examination of the time-dependent charge balance and of the temperature profile distribution within the unit

cell is presented.[3] Thirdly, the impact of the incomplete ionization on the C-V characteristics of MOS capacitors is reviewed.

Lastly, the dynamic ionization effects are commented for the device' termination regions and for the case of structures suffering of dynamic punch-through.

5.2 Physics of the incomplete ionization

The modelling of the incomplete ionization phenomenon can be done by conceiving the dopant species as acceptors and donors' impurities coupled with the valence and conductance band, respectively, within the framework of the electrothermal drift-diffusion model [152]. In case of 4H-SiC, it is worth noting that different activation energies may arise from different positions in the lattice crystal, i.e. hexagonal (Hex) or cubic (K) sites (table 5.1). The presence of deep level impurities can be treated with the Fermi-Dirac distribution, also known as steady-state Gibbs distribution, as illustrated in (17a-e).

Table 5.1. Activation energies for different dopant atoms in WBG Semiconductors.

Material	Dopant species	Activation energy
4H-SiC	B (p-type)	0.293 eV [289, 290]
	Al (p-type)	0.265 eV[291]
	N (n-type)	0.07 eV(Hex) 0.12 eV (K) [292]
	P (n-type)	0.055 eV(Hex) 0.102 eV (K) [293]
GaN	Mg (p-type)	0.16 eV[294]
	C (p-type)	0.9 eV[295]
Diamond	B (p-type)	0.37 eV[296]
	P (n-type)	0.57 eV[297]
	N (n-type)	1.7 eV[298]

[3] Some of the material in this chapter has been the object of the following publication: Static and dynamic effects of the incomplete ionization in SuperJunction devices," *IEEE Transactions on Electron Devices,* vol. 65, pp. 4469-4475, 2018.

$$N_D = \frac{N_{D0}}{1+g_D \cdot \exp\left(\frac{E_{FN}-E_D}{kT}\right)} \quad (17a)$$

$$N_A = \frac{N_{A0}}{1+g_A \cdot \exp\left(\frac{E_A-E_{FP}}{kT}\right)} \quad (17b)$$

$$N_X = N_{X0} \qquad \text{if } N_{x0} > N_{x_{critic}} \quad (17c)$$

$$E_x = E_{x0} - \xi_x N_x^{1/3} \quad (17d)$$

$$g_x = g_{x0} + k_x \cdot \exp\left(\frac{-\Delta_{gx}}{kT}\right) \quad (17e)$$

Where E_{FN} (E_{FP}) is the quasi-Fermi energy level for electrons (holes), g_D (g_A) is the degeneracy factor for donors (acceptors), N_D (N_A) is the activated number of donors (acceptors), N_{D0} (N_{A0}) is the total number of donors (acceptors), E_D(E_A) is the energy level for donors (acceptors), ξ_A (ξ_D) is the Pearson-Bardeen coefficient of acceptors (donors) which takes into account of the activation energy' reduction for high doping levels, k_A (k_D) and Δ_{gA} (Δ_{gD}) are constants that determine the variation of the degeneracy factor with the temperature, T is the absolute temperature in Kelvin and k the Boltzmann constant. In table 5.1, the activation energy is defined as E_C-E_D for donors and E_A-E_V for acceptors, where E_C and E_V are the minimum and the maximum energy level of the conductance and valance band, respectively.

When a certain critical acceptor dopant concentration $N_{Acritic}$ (or $N_{Dcritic}$ for donors) is reached, full activation can be considered (i.e. N_A=N_{A0} for $N_{A0}\geq N_{Acritic}$ and N_D=N_{D0} when $N_{D0}\geq N_{Dcritic}$). In formulas (17a-b), the variation of the activation energy due to the Poole-Frenkel effect has been neglected whilst the Pearson and Bardeen formula which accounts for a reduction of the activation energy at high doping concentration has been considered, as shown in (17d). The equilibrium concentrations in a semiconductor bulk region can be evaluated by finding the Fermi energy level E_F (E_{FN}=E_{FP}=E_F at the equilibrium) which simultaneously satisfies the charge neutrality condition ($n+N_A=p+N_D$) for electrons (n) and holes (p) and the equations (17a) and (17b). This merging, together with the law of mass action ($p\text{-}n=n_i^2$), leads to the formula (18a) and (18b), for n-type and p-type bulk regions respectively. Formula (18b) has been plotted in figure 5.1 for the case of boron doped diamond (see parameters in Table 5.2)

$$\frac{n(n+N_{A0})-n_i^2}{N_{D0}-N_{A0}-n+\frac{n_i^2}{n}} = \frac{N_C}{g_D}\cdot\exp\left(-\frac{E_C-E_D}{kT}\right) \quad (18a)$$

$$\frac{p(p+N_{D0})-n_i^2}{N_{A0}-N_{D0}-p+\frac{n_i^2}{p}} = \frac{N_V}{g_A}\cdot\exp\left(-\frac{E_A-E_V}{kT}\right) \quad (18b)$$

In (18a-b) n_i is the intrinsic carrier concentration (in cm^{-3}), N_V(N_C) the density of states in the valence (conductance) band and N_{A0} (N_{D0}) in formula 18a (18b) indicates the amount of compensation doping which has been considered as fully activated (i.e. N_A=N_{A0} for 18(a) and N_D=N_{D0} for 18(b)). It is worth noting that the parameters n_i,N_V,N_C are all assumed to be temperature dependent.

Table 5.2. Parameters for the incomplete ionization model for acceptors (boron) and donors (phosphorous) dopants in CVD Diamond.

x	E_{x0} (eV)	$N_{xcritic}$ (cm^{-3})	ξ_x (eV cm)	g_{x0}	kx	Δ_{gx} (meV)
A (Acceptors)	0.37 [296, 299]	4.5×10^{20} [188]	4.7×10^{-8} [296]	4 [296]	2 [300]	6 [300]
D (Donors)	0.57 [297]	1×10^{20}	0 [301]	2 [302]	0	0

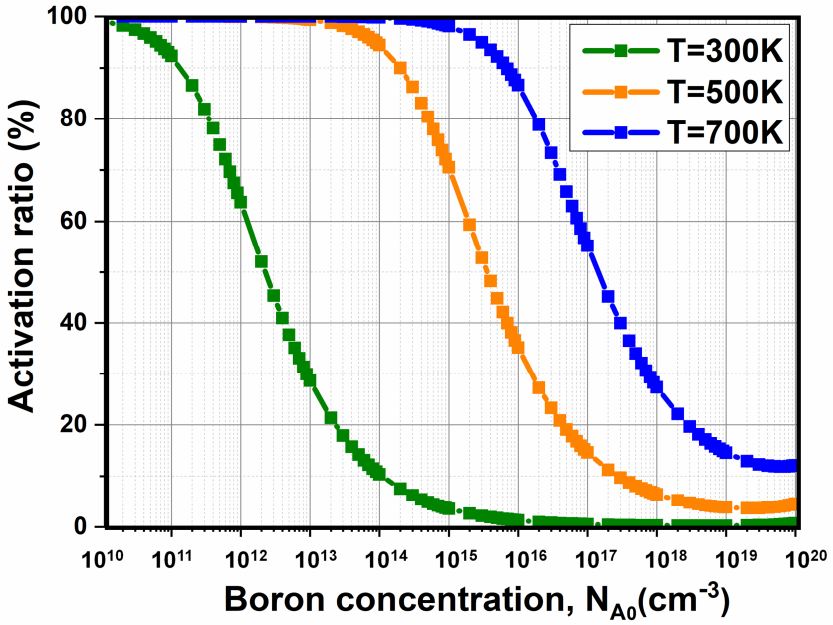


Figure 5.1: Hole activation rate (N_A/N_{A0}) in p-type Diamond as function of the boron concentration (N_{A0}) at three different operating temperatures with a compensation level of N_{D0}=0 cm^{-3}. For N_{A0}>4.5×10^{20} cm^{-3} the activation ratio becomes 100% (see equation 17(c) and table 5.2).

In the non-neutral regions (such as depletion regions), where the electrostatic potential Ψ is not negligible and in general given by the Poisson equation, the charge neutrality condition does not hold anymore, and the concentration can be evaluated as in (19a) and (19b).

$$N_D = \frac{N_{D0}}{1+g_D \cdot \exp\left(\frac{E_{FN}-E_D}{kT}\right)\cdot \exp\left(\frac{q\Psi}{kT}\right)} \tag{19a}$$

$$N_A = \frac{N_{A0}}{1+g_A \cdot \exp\left(\frac{E_A-E_{FP}}{kT}\right)\cdot \exp\left(-\frac{q\Psi}{kT}\right)} \tag{19b}$$

Where E_{FN}, E_{FP}, E_A and E_D are the energy levels in the neutral region, which coincide with the ones calculated at zero bias and under the charge neutrality condition. With reference to a classic p-n junction, in the depletion region the electrostatic potential Ψ is positive in the p-side (negative in the n-side) with respect to the p-type (n-type) bulk[152]. When a reverse voltage is applied to the junction, both the potential barrier and the width of the depletion regions increase. For this reason, the denominator of (19a) and (19b) approaches the unity and $N_D \sim N_{D0}$ such as $N_A \sim N_{A0}$ in the n-side and p-side, respectively, so causing a full activation of the dopant species. Whereas the electrostatic of the incomplete ionization is mainly governed by the set of equations (17)-(19), the dynamic time response is highly dependent on the capture and emission rates, as shown in equations (20a-d)[303]. In these equations, t is the time, v_{th_e} (v_{th_h}) are the electron (hole) thermal velocity, σ_D (σ_A) is the cross section for donors (acceptors) species.

$$\frac{\partial N_D}{\partial t} = v_{th\_e} \cdot \sigma_D \left[\frac{n_1}{g_D} N_{D0} - \left(n + \frac{n_1}{g_D}\right) N_D\right] \tag{20a}$$

$$n_1 = N_C \cdot \exp\left(-\frac{E_C-E_D}{kT}\right) \tag{20b}$$

$$\frac{\partial N_A}{\partial t} = v_{th\_h} \cdot \sigma_A \left[\frac{p_1}{g_A} N_{A0} - \left(p + \frac{p_1}{g_A}\right) N_A\right] \tag{20c}$$

$$p_1 = N_V \cdot \exp\left(-\frac{E_A-E_V}{kT}\right) \tag{20d}$$

The main idea behind the dynamic model of the incomplete ionization is that acceptor and donor dopants can be viewed as donor and acceptor traps respectively. In reality, the carriers' dynamic shown in equations (20a-d) is a generalization of the Shockley-Read-Hall (SRH) model in case of transient conditions[304]. This means that depending on their position in the bandgap, these states can capture/emit carriers

(hole/electrons), a process which could be also seen as ionization/deionization of the dopants. With reference to the finite element simulation tool adopted for this manuscript (Sentaurus TCAD[150]), in the case of donor traps (defined as uncharged when unoccupied and positive when occupied), the emission of an electron to the conduction band corresponds to the ionization of the dopant atom while the capture of an electron from the same band corresponds to the deionization process. On the other hand, the capture of an electron from the valence band (i.e. a hole is created in the valence band), corresponds to the ionization of an acceptor state (defined as uncharged when unoccupied and negative when occupied) whilst the emission process is related to the deionization of this state. However, despite the carrier equations for the dynamic of the incomplete ionization model are identical to the trap model included in Sentaurus TCAD[150], no generation-recombination process with the conduction/valence band or between two energy trap levels is associated to the acceptor/donor level in the incomplete ionization model. Therefore, the two models can provide the same results only when the generation-recombination processes associated to that specific energy level can be neglected. It is possible to rewrite the equation (20c) and then define a time constant for the incomplete ionization model, as illustrated in (21a-b) in case of acceptor dopants. This time constant (τ_p) is highly dependent on the capture and emission rates defined in (22a-b) and for this reason, it depends on the activation energy, temperature, cross section, etc. The same derivations can be done for donor impurities.

$$\frac{\partial N_A}{\partial t} = -\left(e_p + c_p p\right)N_A + e_p N_{A0} \tag{21a}$$

$$\tau_p = \frac{1}{e_p + c_p p} \tag{21b}$$

If the device under test (DUT) is subjected to a dynamic process (i.e. dV/dt or dI/dt) with a time constant smaller than the ionization/deionization, the static equations in (17a-e) do not hold anymore and equations (20a-d) have to be solved.

$$c_p = v_{th\_h} \cdot \sigma_A \tag{22a}$$

$$e_p = v_{th\_h} \cdot \sigma_A \cdot N_V \cdot g_A^{-1} \cdot \exp\left(-\frac{E_A - E_V}{k\,T}\right) \tag{22b}$$

The evolution of the carrier activation with time is then governed by the incomplete ionization time constant. Inside the space charge region (SCR), the time constant defined in (21b) modifies into (23) as no free carriers are present in the structure.

$$\tau_p = \frac{1}{e_p} \tag{23}$$

Under this specific condition, the time constant does not depend upon the capture rate and it can be easily evaluated as shown in figure 5.2 for boron doped diamond layer (a) and 4H-SiC(b). It is worth noting that the cross section (assumed constant in figure 5.2 and hereafter in this chapter) can be electric field and temperature dependent.

While the temperature dependence has been typically parametrized in the literature by means of the cascade capture model ($\sigma = T^{-2}\sigma_0$)[305], the more complex electric field dependence has been modelled with the Hurkx model[306], the Poole-Frenkel model [307] and other physical models[150].

Nonetheless, experimental measurements have often failed to obtain a precise derivation of the capture cross section (and its temperature-electric field dependence) due to presence of multiple traps levels which are interacting with each other. Consequently, this extrapolation has been typically performed analytically by means of calibrated Monte-Carlo simulations which offer a better insight into the capture/emission process at the microscopic level[308].

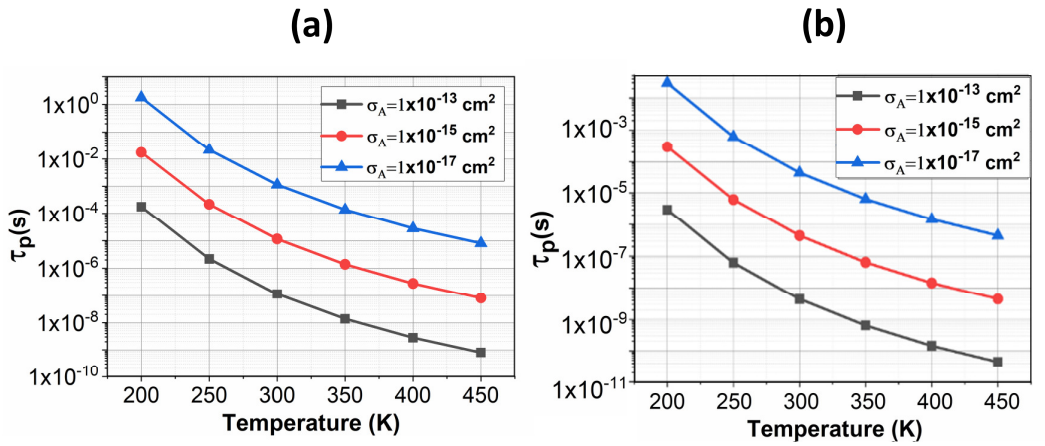


Figure 5.2: Ionization time constant (23) vs temperature for three different values of the cross section for a diamond boron doped layer (a) and a 4H-SiC boron doped layer (b). In equation (22b), N_V and v_{th_h} are both assumed temperature dependent.

Besides, the incomplete ionization models presented in equations (17a-e) predicts an abrupt increase of the activated number of donors and acceptors when the critical

dopant concentration is reached. Several alternative and more advanced models [309, 310] have been presented in the literature for Silicon and related materials in order to take into account a smoother variation of the activation rate (figure 5.1) at the metal-semiconductor transition.

As an example, for increasing doping concentration close to the metal-semiconductor transition region, two different effects due to the enlarged coulombic interaction need to be considered: the widening of the acceptor (donor) energy level which tends to generate a continuous acceptor (donor) band and the Fermi energy levels E_{FP} (E_{FN}) which are approaching the valence (conduction) band faster than the energy levels E_D(E_A).

As discussed in [311], the second effect causes localized activation of acceptor (donor) states with a consequent reduction in the activation ratio. In diamond, the metal-semiconductor transition region is usually dominated by hopping conduction mechanisms, as already mentioned in chapter 2.

The unusual effects of the hopping conduction mechanisms are usually modelled with an increase in the hopping mobility [141] rather than with a raise in the number of ionized species[136].

5.3 Static effects of the incomplete ionization

While the equations which allow to compute the electro-thermal equilibrium solution have been addressed in the previous section, we now focus on understanding the incomplete ionization' effects on the space charge regions and on the carrier density for different doping concentration and operational temperature.

5.3.1. Carrier profiles: the case of a p-n junction

To capture the main physical effects derived by the incomplete ionization under quasi-stationary assumptions (i.e. whenever equations 20-22 can be neglected), a simple 1D model of a p-n junction has been considered in this paragraph (figure 5.3(a)).

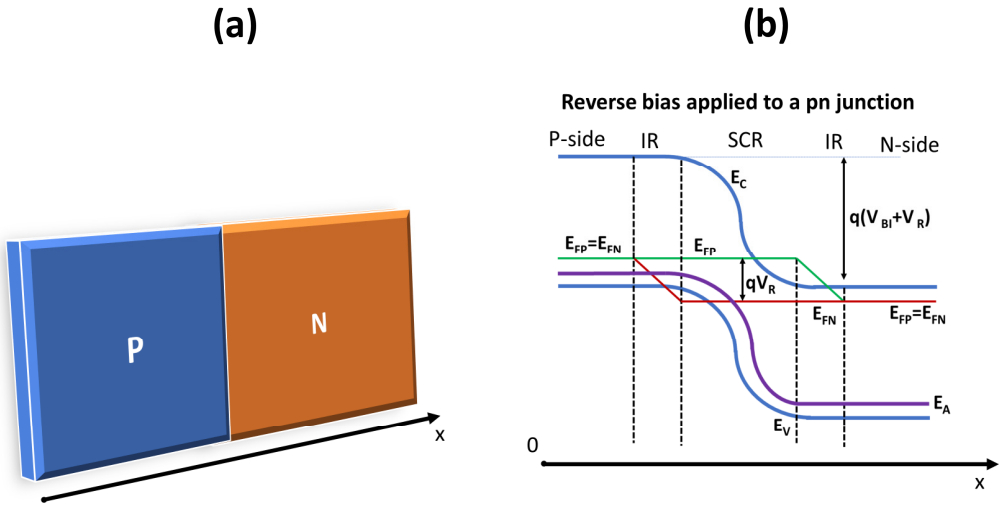


Figure 5.3: (a) Schematic picture of a 1D p-n junction and (b) its equivalent band diagram in reverse bias condition ($V=V_R$). The acceptor level E_A represents the main dopant level for the p-side while it only acts as a compensation level for the n-side. In the figure, IR and SCR represent the intrinsic and the space charge region, respectively.

In figure 5.3(b) a schematic band diagram of the reverse p-n junction with an acceptor level (E_A) graphically demonstrates the meaning of equations 5.3(a-b) which predict an abrupt change for the ionization rate in proximity of the space charge regions (where the Fermi levels change). However, it is not trivial to derive easy formulas which help to understand the discrepancies observed in terms of depletion region and space charge between the incomplete and complete ionization mechanisms (see figure 5.4(a) and (b)), an effect already mentioned in the JFET modelling described in chapter 4. When shallow/ultra-shallow dopant impurities are employed, the depletion layer width and the space-charge region modulation can be easily obtained by monitoring the absence of the majority mobile carriers at each side of the junction. Conversely, the presence of deep level impurities needs a much more thorough analysis. An accurate study which allows to predict the band bending effects in the case of the incomplete ionization, has been described in[294, 312]. The first important phenomenon described in [312], concerns the existence of a transition region which separates the ionized impurities and the profile of majority free carrier in the bulk (see figure 5.4(c)). With the reference to a 1D p-n+ junction (figure 5.4) and by approximating the ionized acceptor concentration and employing a Taylor expansion to approximate the exact solution of the Poisson equation, it is possible to derive an expression of the potential Ψ in the transition region (24a).

$$\Psi \propto \exp(-x/L_D) \tag{24a}$$

$$L_D = \sqrt{\frac{\varepsilon KT}{q^2(2p_0+N_D)}} \tag{24b}$$

The electrostatic potential Ψ is found to be dependent upon a "modified" Debye length L_D (24b) which is function of the temperature(T), the equilibrium bulk concentration (p_0) and the carrier compensation level (N_D). Then, calculating the two margins of the transition region (see figure 5.4(c-d)) as the point of complete absence of mobile holes (x_{NA}) and the point in which the hole concentration reaches half of the bulk value (x_p), an approximated value for the transition region' width (λp) can be derived (25). A similar expression holds for the case of an n-side region of a more generic p-n junction in which both sides are affected by the incomplete ionization [312].

$$\lambda p = L_D * \ln\left\{\frac{\ln(N_{A0}/(p_0+N_D)}{\ln(2)}\right\} \tag{25}$$

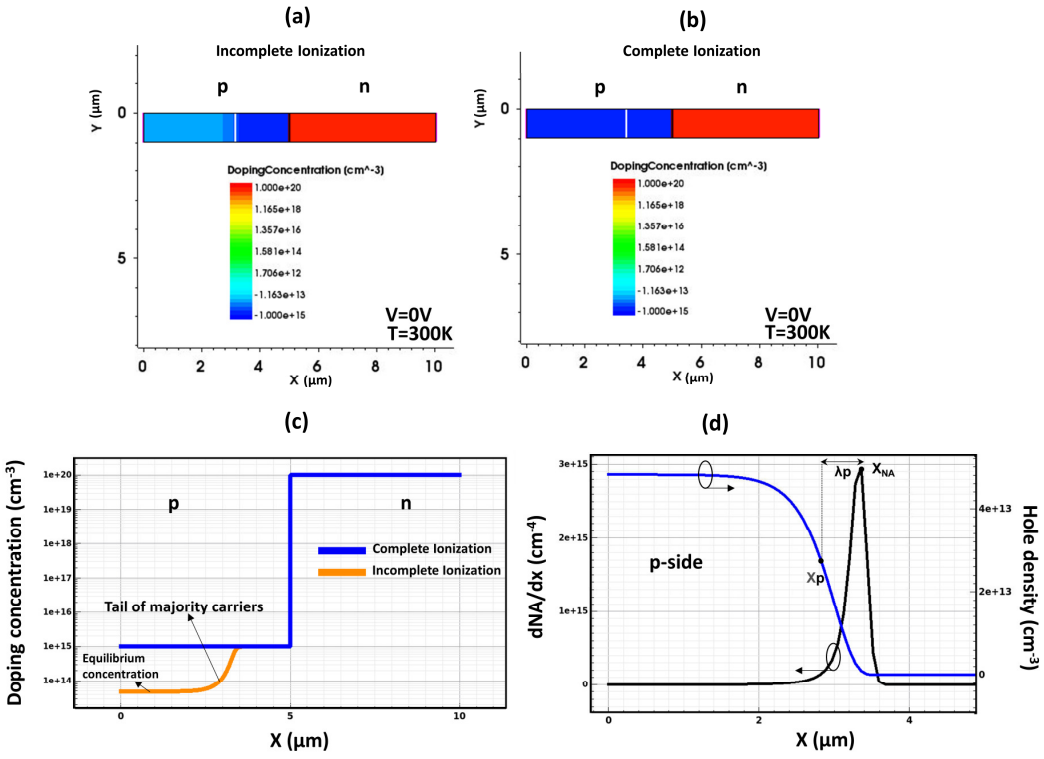


Figure 5.4: 1D model of a semiconducting diamond p-n+ junction in which the n-side (phosphoruous doped) is considered to be fully activated (N_{D0}=1x10^{20} cm^{-3}) and the p-side (boron doped) N_{A0}=1x10^{15} cm^{-3} is modelled with the incomplete (a) and complete (b) ionization. Doping concentration at RT with and without the incomplete ionization (c) and hole density and first order derivative of the activated acceptors as function of the position in the p-side of the junction which identify the boundaries of λp (d).

The importance of (25) is soon revealed: if one defines the width of the depletion region at each side of the junction as the position at which the majority carrier concentration reaches the half of the bulk concentration [294, 312], the enlarged depletion region for the case of the incomplete ionization is simply the sum of (25) and of the depletion region' width calculated for the complete ionization case (which coincides with the position x_{NA}).This powerful (but approximated) expression allows for a thorough investigation of this effect for different operational temperature and doping concentration (figure 5.5 and 5.6). As an example, in the case of a p-n+ diamond junction, the variation of λp has been plotted as function of the temperature and doping levels (figure 5.5). Some discrepancies between TCAD simulations and the formula (25) can be observed for high temperature and high doping concentration. Such an incongruity is due to simplified assumption which have led to formula (25), and, especially, to the simplified expression which has been implemented for the field dependent ionized concentration in [294].

Besides, the simplified assumption, which is useful to derive a closed form solution for equations (24-25), leads to higher discrepancies for increased activation energies, as in the case of phosphorous doping in a diamond p-n junction (figure 5.6).

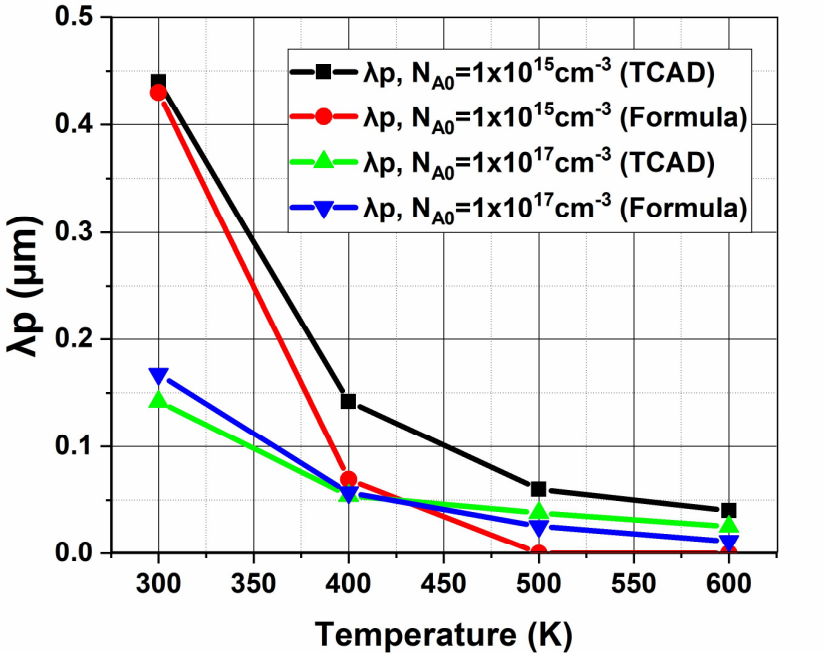


Figure 5.5: λp for 1d p-n+ junction for different temperatures and boron doping concentration (phosphorous concentration is fixed at $1x10^{20}$ cm^{-3}). Comparison of TCAD simulations and the analytical formula (25).

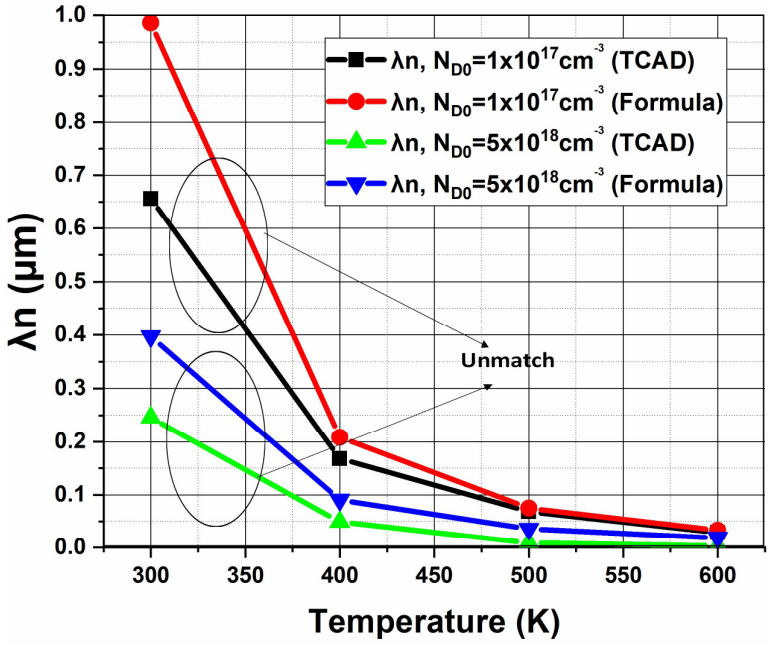


Figure 5.6: λn for 1d p-n junction for different temperatures and phosphorous doping concentration (boron doping is fixed at 1x10^{15} cm^{-3}). Comparison of TCAD simulations and the analytical formula.

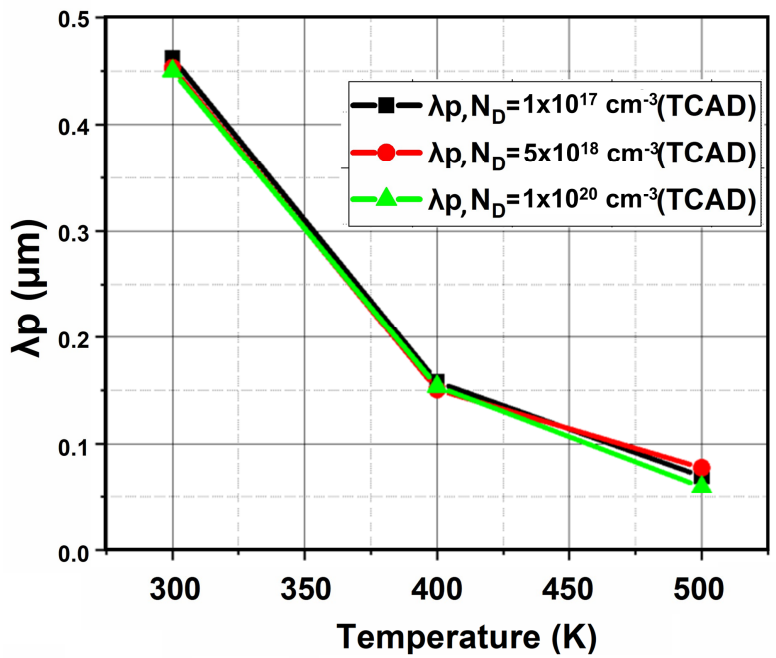


Figure 5.7: λp for 1d p-n+ junction for different temperatures and phosphorous doping concentration (boron doping is fixed at 1x10^{15} cm^{-3}).

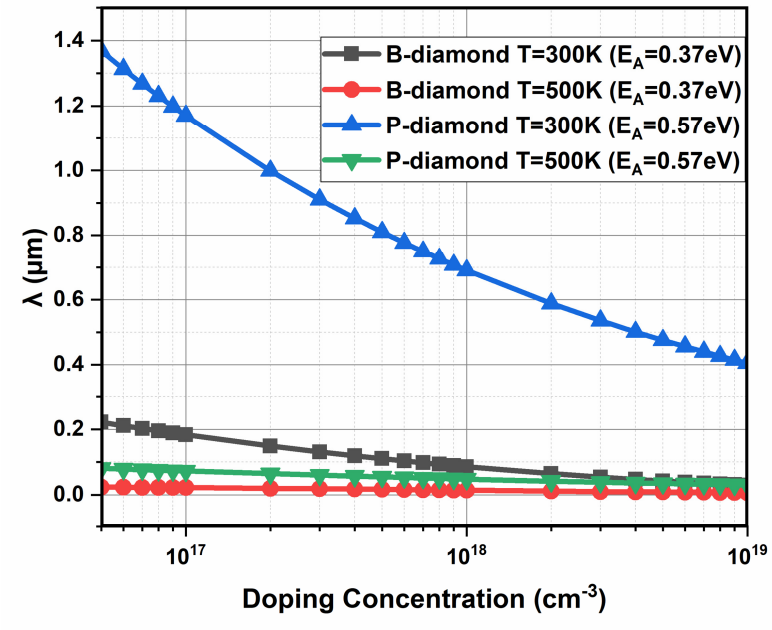


Figure 5.8: **λp, n** (analytical) vs doping concentration for boron doped diamond (B-diamond) and Phosphorous doped diamond (P-diamond) for T=300 K and T=500 K. Compensation has been neglected.

In a more general situation in which the incomplete ionization of the impurity atoms affects both side of the junction, some additional considerations can be done. For example, considering the case of a diamond p-n junction in which the doping of the p-type region is fixed, it is interesting to observe that the effect of an increase/reduction of the n-type dopant concentration does not play any significant role in modulating the transition region length λp (figure 5.7). This effect confirms the evidence that in the case of a unipolar mode diamond JFET, the doping and the activation energy of the n-type region do not significantly modify the depletion region in the channel region in quasi-stationary conditions (i.e., if the junction remains of the p-n+ type). Formula (25) has also been plotted for a wide range of doping concentration (figure 5.8), clearly pointing out that incomplete ionization has a big impact on the depletion region for high activation energies and in the low doping-temperature range.

5.4 Dynamic effects of the incomplete ionization

Whereas the electro-thermal equilibrium conditions do not hold anymore, equations 20-22 correctly allow to evaluate the dynamic activation of acceptor/donor species. This dynamic evolution of the activated species has several important consequences

on the semiconductor device' modelling[153]. These issues will be detailed illustrated in this section.

5.4.1. Charge imbalance in SJ devices

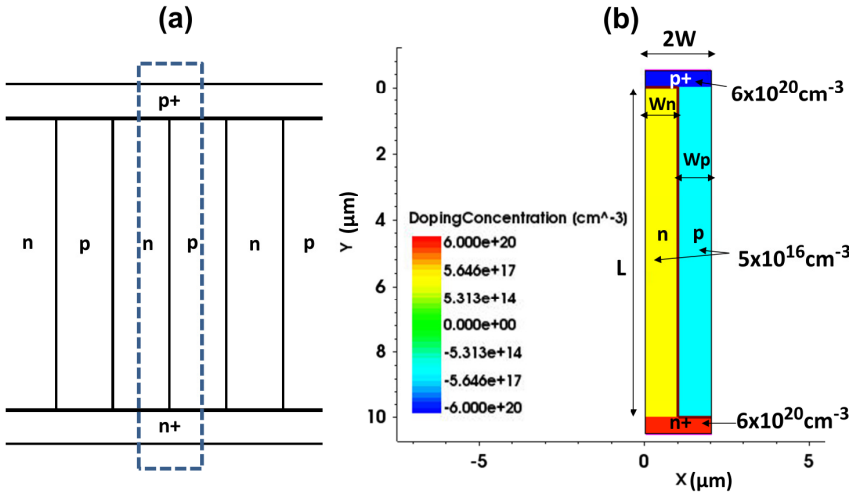


Figure 5.9: Cross section of 4H-SiC SJ diode structure (a) and unit cell adopted for the TCAD simulations(b). The dopant concentration of the p-type and n-type pillar (N_{A0},N_{D0} respectively) has been fixed at $5x10^{16}$ cm^{-3} for both pillars, whilst the concentration of the n+ and p+ regions is set at $6x10^{20}$ cm^{-3}. The aspect ratio (L/W) of the structure is 10 (L=10 µm and W=Wp=Wn=1 µm).

In structures in which the charge balance plays a key role (i.e. SJ based devices), the dynamic ionization may lead to charge imbalance effects which may cause a premature breakdown if the device is not able to restore the balance condition in time. This particular effect of the incomplete ionization will be discussed in this paragraph with reference to a 2D model of a 4H-SiC SJ diode. In this investigation, we assume a constant value of σ ($1x10^{-15}cm^2$) for boron doped 4H-SiC, a mean value according to several DLTS measurements reported in [313, 314]. The cross-sectional view for the unit cell of the 4H-SiC SJ diode is shown in figure 5.9. The critical value of the dopant concentration after which the total activation occurs has been fixed at $1x10^{22}$ cm^{-3}. The values for the other parameters adopted for the TCAD simulations (mobility, impact ionization, bandgap etc.) can be found in default 4H-SiC parameter file [150]. The dopant species are nitrogen (N) for the n-type layers (Hex site) and boron (B) for the p-type layers. B has been chosen as p-type dopant instead of Al for the TCAD simulations, but all the considerations done for this dopant species may be applied also for the case of Al dopant or for other WBG semiconductors SJ devices, in which the incomplete ionization' effect cannot be neglected (i.e. Diamond, GaN, βGa_2O_3, etc).

If one assumes that Wp=Wn=W and N_{A0}=N_{D0} (as in figure 5.9(b)), and then solves (18a) and (18b) to evaluate the activated number of acceptor (N_A) and donor dopants (N_D), the theoretical imbalance ratio between the n-type pillar and the p-type pillar at different temperature can be easily calculated, as shown in figure 5.10(a). An imbalance ratio between the SJ pillars, would lead to a drastic reduction of the breakdown capability of the device, a well-known effect in the classic SJ theory[315], as also illustrated in figure 5.10(b). However, if the SJ diode is properly designed, a full lateral and vertical depletion of the device' structure occurs before the BV (which is due to the avalanche generation under our assumptions). In particular, if the electric field is high enough in all the structure (i.e. the device is all depleted), it may be able to activate all the dopants (i.e. N_A~N_{A0} and N_D~N_{D0}), as already discussed in the paragraph 5.2. Indeed, if one balances the SJ structure assuming total ionization in both pillars while satisfying the charge balance condition (as in device shown in figure 5.9(b)), the breakdown voltage is identical with and without the incomplete ionization model, meaning that the electric field is actually able to activate virtually all of the dopants during the off-state. This means that the static BV for the device depicted in figure 5.9(b) corresponds to the value shown in figure 5.10(b) for an imbalance ratio of 0%. Regarding the on-state (figure 5.11), if the conductive pillar is the one affected by the incomplete ionization, the current density is highly reduced, and the risk may be a total depletion of the p-type pillar with consequential no current flowing in the device.

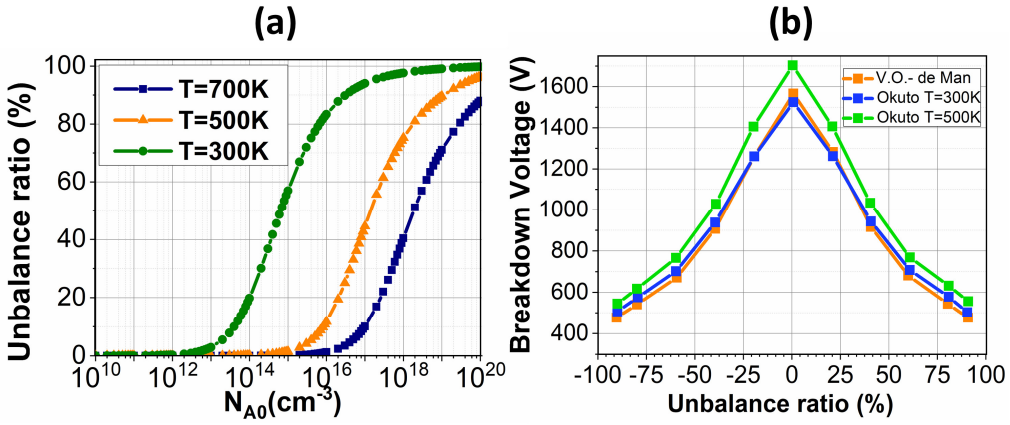


Figure 5.10: (a) (Theoretical) Imbalance ratio vs dopant concentration (N_{A0}, which is assumed equal to N_{D0}) for three different operating temperatures of the device depicted in figure 5.9(b). The imbalance ratio for the device structure in figure 5.9(b) has been defined as 100*abs(N_A-N_D)/max(N_A,N_D). (b)Simulated BV vs Imbalance ratio for the device structure shown in figure 5.9(b) with two different impact ionization models (Van Overstraeten-de

Man and Okuto[150, 316, 317]). Okuto model, which takes into account a positive temperature coefficient of the breakdown voltage, has been selected as the avalanche model for this study.

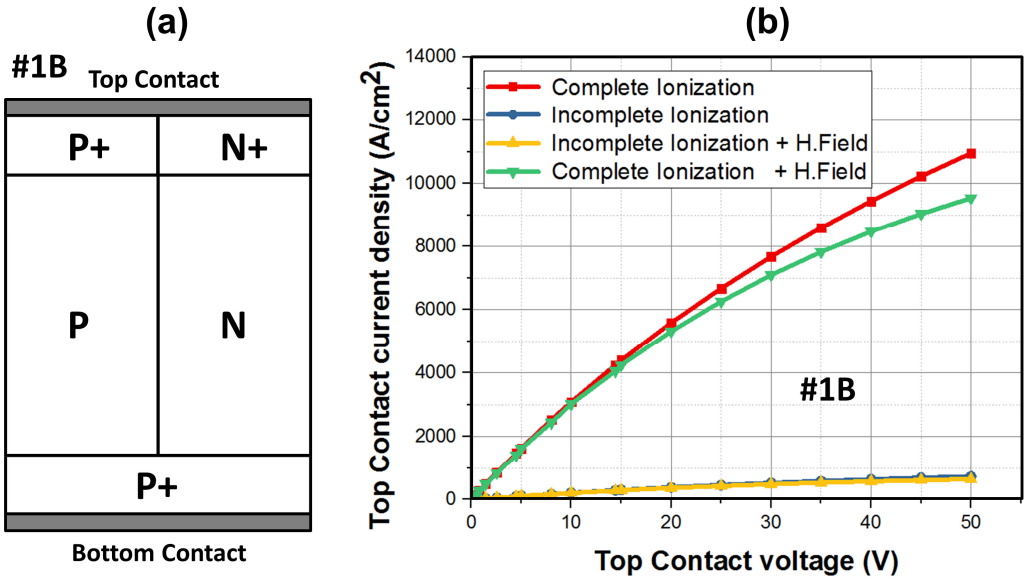


Figure 5.11: Cross section of the device structure #1B adopted for the on-state simulation (a) and on-state current density simulations (b).

The device adopted for the on-state simulation is shown in figure 5.11(a) where a top p+ layer has been introduced for structure #1B in order to emulate the flow of the majority carriers which occurs in a real MOSFET structure. It is also evident that the high field dependence model[318] which accounts for a reduction of the mobility for high electric field` values, also plays a key role in the on-state, emphasizing the JFET effect[319].

5.4.1.2 The dynamic imbalance

As already discussed in the theory section (5.2), the ionization/deionization process is not only temperature but also time dependent. So, if a reverse bias pulse is applied to the structure and the rise time of this pulse is around one order of magnitude lower than the ionization time constant, not all the dopants are activated by the high electric field [303, 320]. In the specific case of a the 4H-SiC SJ diode, this dynamic ionization effect may lead to a charge imbalance situation (such as the one predicted in figure 5.10(a)) and reduce the real breakdown capability of the SJ. In order to investigate the possible consequences of the dynamic ionization, a reverse pulse of 1 kV amplitude and rise time of 10ns (1 kV/10 ns) has been applied to the structure (figure 5.12). The

rise time has been chosen taking into account the ionization time constant plotted in figure 5.1 in order to trigger the dynamic of the incomplete ionization.

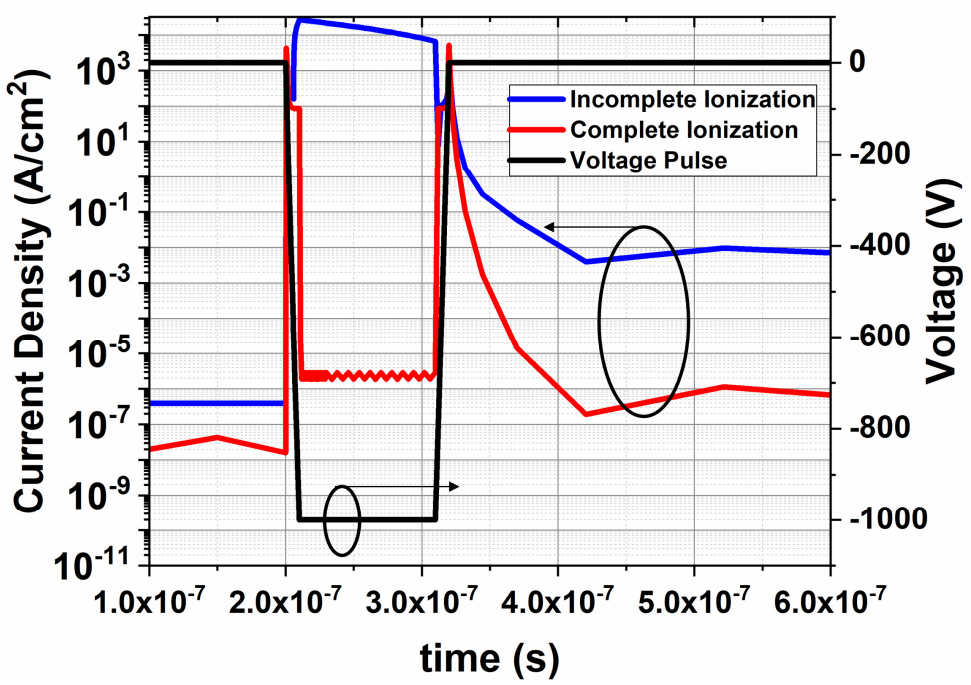


Figure 5.12: Current density vs time with and without the incomplete ionization model. The rise time and the fall time of the reverse pulse are fixed at 10ns (tr=tf=10 ns) and the duration of the pulse is set at 100ns (ton=100ns).

In practice, in devices such as MOSFETs, such high dV/dt are unacceptable due to other effects such as system oscillations or retriggering of on-state conduction via the Miller capacitance and gate resistance [321]. However, this value is comparable with the maximum dV/dt ruggedness reported in several datasheets of commercially available SiC devices[322, 323]. It is worth mentioning that the voltage applied to the SJ diode in this simulation is much lower than the static breakdown voltage (figure 5.10(b)) obtained in case of perfect balance (around 1.5 kV at RT). The simulation results of the current density vs time clearly show that if the incomplete ionization is included in the simulation set, the SJ diode operates in avalanche condition for the whole duration of the pulse. The simulated current density is comparable with the on-state current density (figure 5.11). When the voltage pulse is removed, the SJ slightly recovers to its initial balanced condition and the current is mainly capacitive. To confirm the avalanche operation and the loss of the charge balance in reverse condition, the electric field has been plotted at the end of the rise time of the pulse (V=1 kV and $t=2.1\times10^{-7}$s) in figure 5.13.

As the time passes the boron dopant activation increases and therefore the imbalance is dynamically lowered. This is also confirmed by the current density decrease over the time (constant slope of the blue curve in figure 5.12).

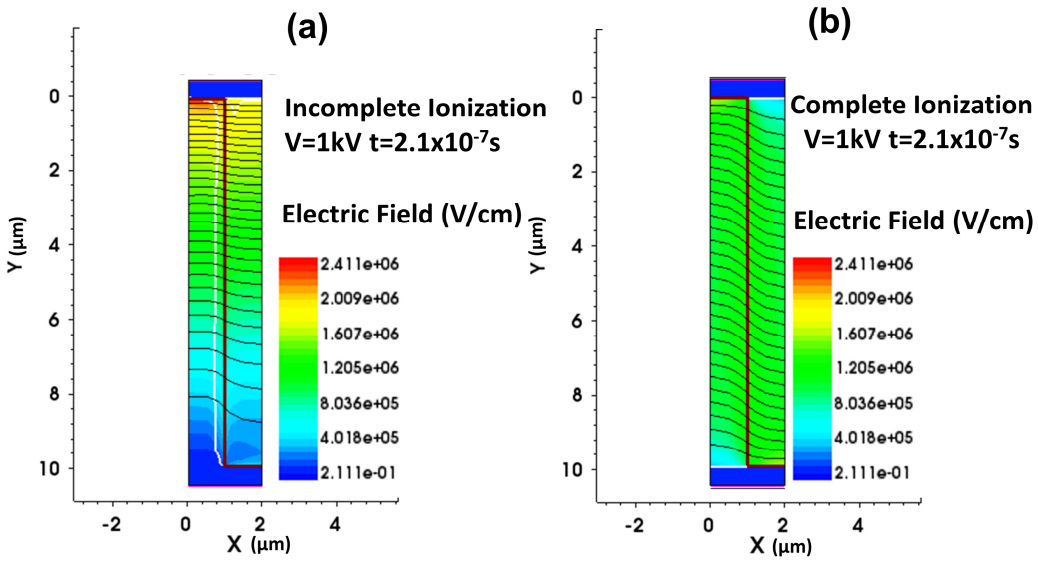


Figure 5.13: Electric field and electrostatic potential contour at the end of the rise time of the pulse with (a) and without (b) incomplete ionization. With the incomplete ionization model, a clear imbalance can be deduced from both the non-uniform electrostatic potential contour and the higher electric field.

5.4.1.3. Temperature effects: single and multiple pulse

In the previous set of simulations, the Poisson and the current` equations have been computed without simultaneously solving the temperature equations at runtime. This assumption does not allow for investigating self-heating effects in the device which is operating under avalanche condition for the whole duration of the reverse pulse and is therefore subjected to high current density and applied voltage. In order to explore the possible electro-thermal effects, two thermal resistances of a fixed value have been connected at the anode and cathode of the DUT, as schematically shown in figure 5.14. Sentaurus TCAD, the commercially-available software adopted for this simulations' work, provides several physical models to compute the lattice temperature in a device structure. The easiest one is the self-heating model [324] which evaluates the overall temperature of a device based on the power dissipated (P=IV) at each time step.

However, despite this model being the fastest with the lowest less convergence issues, it does not allow to calculate the temperature in each mesh points. Moreover, the self-heating model does not couple the equations for the temperature with the Poisson and current equations.

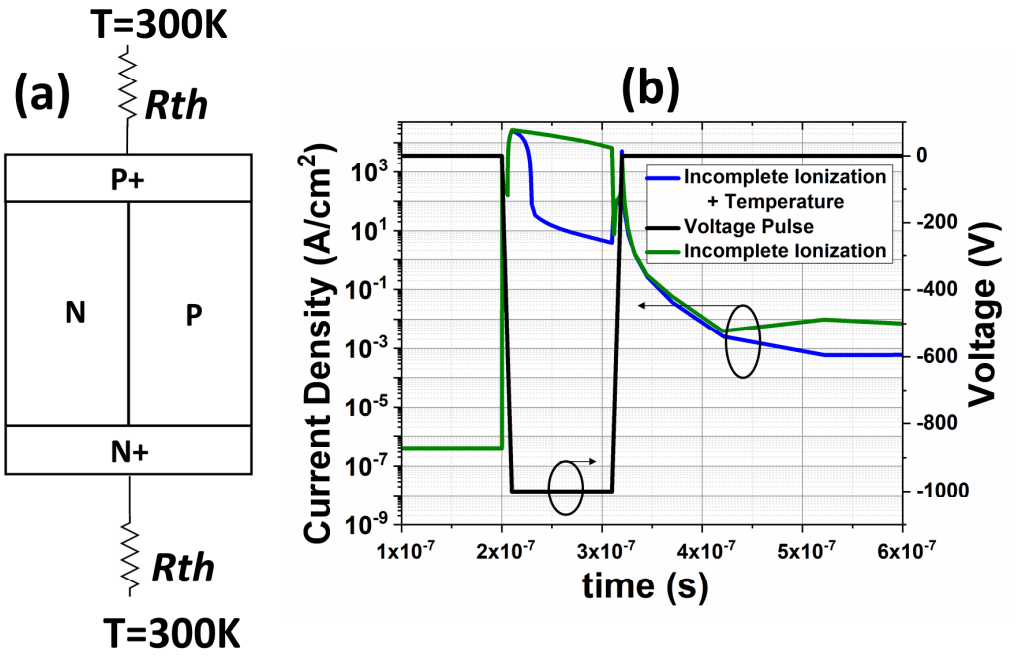


Figure 5.14: (a)Schematic unit cell structure adopted for the TCAD electro-thermal simulations. A fixed value of the thermal resistance has been chosen for the top and bottom contact (0.1 K/W). (b) current density vs time with and without the thermodynamic model. The specifications of the pulse are identical to figure 5.12.

The thermodynamic model [150, 325] which allows to compute the temperature equations in each mesh point, has been adopted for the simulations shown in this work. The equations which govern this model are shown in (26a-c).

$$\frac{\delta}{\delta t}(c_L T) - \nabla\cdot(\kappa\nabla T) = -\nabla\cdot\left[(\Phi_n + P_n T)\,\overrightarrow{J_n} + (\Phi_p + P_p T)\,\overrightarrow{J_p}\right] - \frac{1}{q}\left(E_C + \frac{3}{2}\,k\,T\right)\left(\nabla\cdot\overrightarrow{J_n} - qR_{net,n}\right) - \frac{1}{q}\left(-E_V + \frac{3}{2}\,k\,T\right)\left(-\nabla\cdot\overrightarrow{J_p} - qR_{net,p}\right) + \hbar\omega G^{opt} \quad (26a)$$

$$\overrightarrow{J_n} = -nq\mu_n(\nabla\Phi_n + P_n\nabla T) \quad (26b)$$

$$\overrightarrow{J_p} = -pq\mu_p(\nabla\Phi_p + P_p\nabla T) \quad (26c)$$

Where c_L is the lattice heat capacity, κ is the thermal conductivity, P-n(P_p) is the absolute thermoelectric power, $\Phi_n(\Phi_p)$ the electron(hole) quasi-Fermi potential, Jn (Jp) the current density for electron (holes) computed as in (26b-c), $R_{net,n}(R_{net,p})$ the

electron (hole) net recombination rate, ħ is the reduced Plank constant, G^{opt} is the optical generation rate of photons of frequency ω. The current densities in equations (26b-c) are a generalization of the standard drift-diffusion model[152] with the inclusion of the temperature gradient as a driving term. The RHS of (26a) is the total heat and in the stationary case its second and third term disappear from the equation. In figure 5.14(b), the simulation results of the fast reverse pulse applied to the SJ have been compared with and without the thermodynamic model, whilst the lattice temperature has been plotted in figure 5.15.

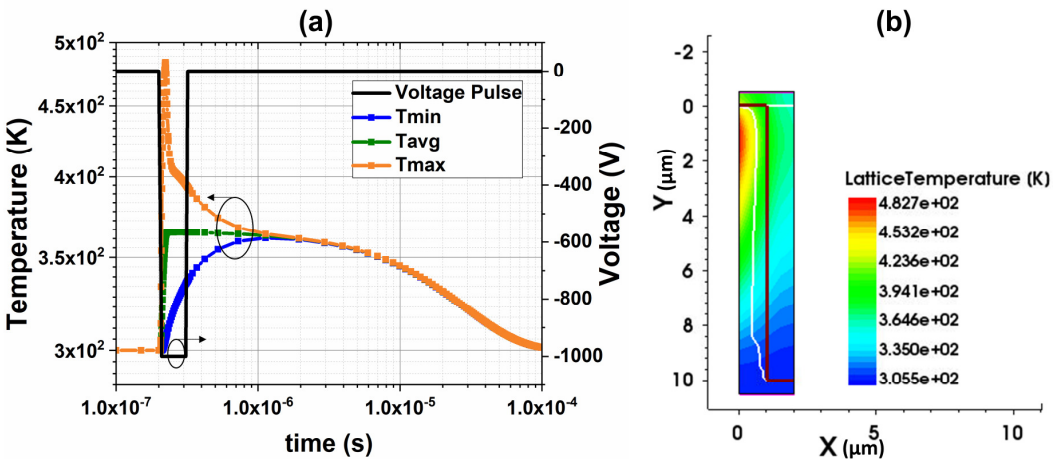


Figure 5.15: Temperature evolution in the structure as function of the time(a). The maximum temperature (Tmax) is observed at t~2.24x10^{-7} s close to the maximum electric field point (b). Tmax slowly converges to the minimum (Tmin) and the average temperature (Tavg) for t≥1 us. The device reaches RT only after 0.1 ms.

The current density observed with the thermodynamic model dynamically reduces much faster than the one computed with the simple Poisson equation and the standard drift-diffusion model. Regarding the temperature, the maximum temperature is obtained at t~2.24x10^{-7} s and it is equal to 482 K. This maximum temperature is observed, as expected, near the electric field peak point (figure 5.15).

While the temperature rises due to the high power density (P=IV), the carrier activation increases much faster as it can be deduced from equations (17-20), the ionization time constant reduces exponentially as it can be observed from equation (23) and figure 5.2(b), and the avalanche generation is also reduced (avalanche is an electro-thermal stable phenomenon in the Okuto model). All these 3 effects combined, lead to an overall decrease of the transient current density as the balance is restored much faster.

In figure 5.16, the carrier activation is compared with and without the thermodynamic model. The evolution of the temperature is observed also in case of a double pulse applied to the structure. As it can be observed from figure 5.17, the imbalance effects observed during the second pulse are much smaller than the one during the first pulse. Indeed, during the second dV/dt, the ionization time constant is smaller than during the first pulse because of the increased average temperature which also improves the breakdown voltage and the carrier activation in the structure, as previously discussed.

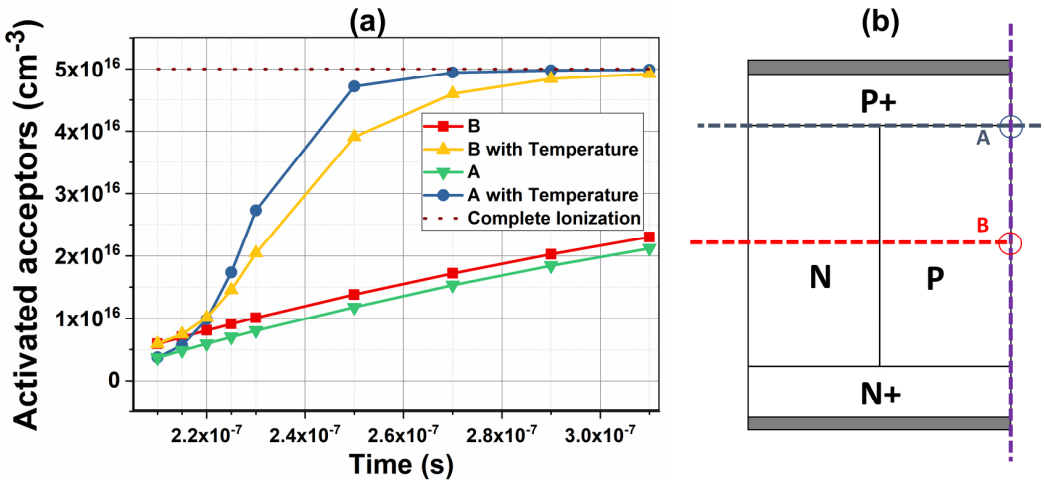


Figure 5.16: Activated acceptors as function of time in two different points of the device structure with and without the thermodynamic model. The slope of the carrier activation vs time loses its linearity with the thermodynamic model.

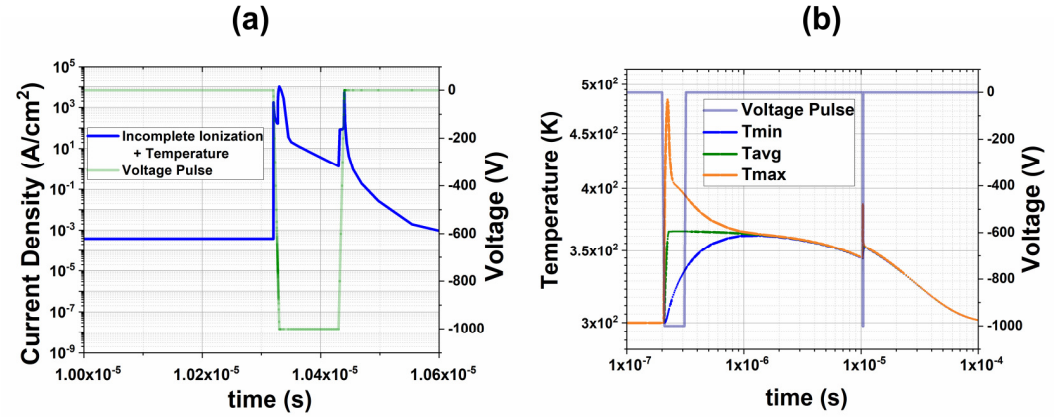


Figure 5.17: (a) Transient evolution of the current density during the second pulse. The specifications of each pulse are the same of the single pulse (tr,tf,ton) and the dead time (tdead) between the two pulses has been chosen to be 10 µs. (b) Temperature observed in the case of a double pulse applied to the SJ diode. The application of a second pulse does not play a significant role in increasing the maximum temperature of the device which has a smaller peak (380 K) compared to the one observed during the first transient (482 K).

If multiple pulses are applied to the structure the same conclusions can be drawn. To sum up, the main dynamic effects of the incomplete ionization are the delay of the device turn-off as the charge balance condition has to be restored in the device and the increase of the junction temperature. To tackle all these issues, the SJ diode unit cell could be redesigned.

5.4.1.4 Redesign the superjunction for improved dynamic charge balance

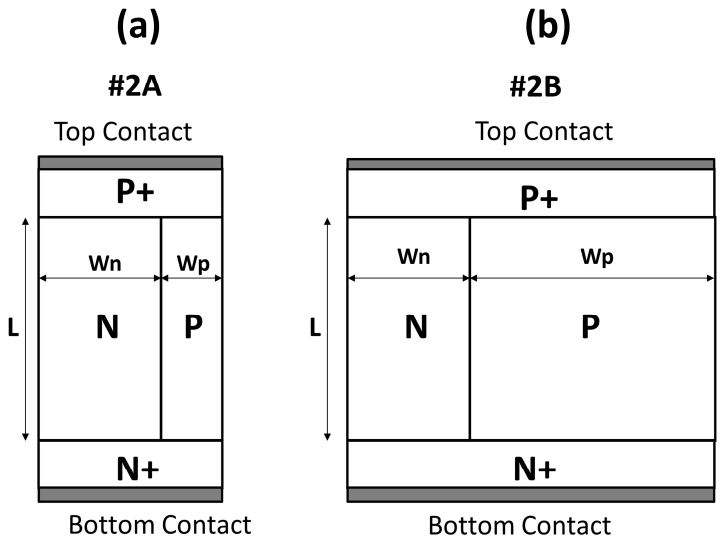


Figure 5.18: Cross sections of the redesigned balanced SJ. The doping and the width of the n-type pillar have been fixed for all the different designs (as for the S-SJ in figure 2) in order to perform a proper comparison of the performance. (a) #2A has N_{A0}=1 x10^{17} cm^{-3} and Wp=0.5 µm and (b) #2B has N_{A0}=2.5 x10^{16} cm^{-3} and Wp=2 µm.

In the SJ theory the optimum breakdown voltage condition is met in the case of perfect balanced condition. This means that if the width and the doping of one of the two pillars are not fixed, it is possible to obtain a balanced SJ with an asymmetric device structure. Figure 5.18 shows two different ways to redesign the SJ balance in order to tackle the dynamic imbalance. The charge balance condition is thus met for both structures and the static breakdown voltage is identical to the Symmetric SJ (S-SJ). The aspect ratio for all the different structures has been kept quite similar in order to maintain an identical breakdown voltage [326]. Figure 5.20 shows that the maximum, minimum and average temperature reached during the dynamic pulse is much higher for structure #2A which has also a higher dynamic current density peak compared to the S-SJ and #2B, as illustrated in figure 5.19. This happens because for higher doping

concentration the imbalance ratio is much more significant, as it can be clearly deducted from figure 5.10(a). For this reason, the device operates in avalanche condition with a much higher imbalance ratio compared to the standard design and it heats up much faster as the avalanche current is also much higher.

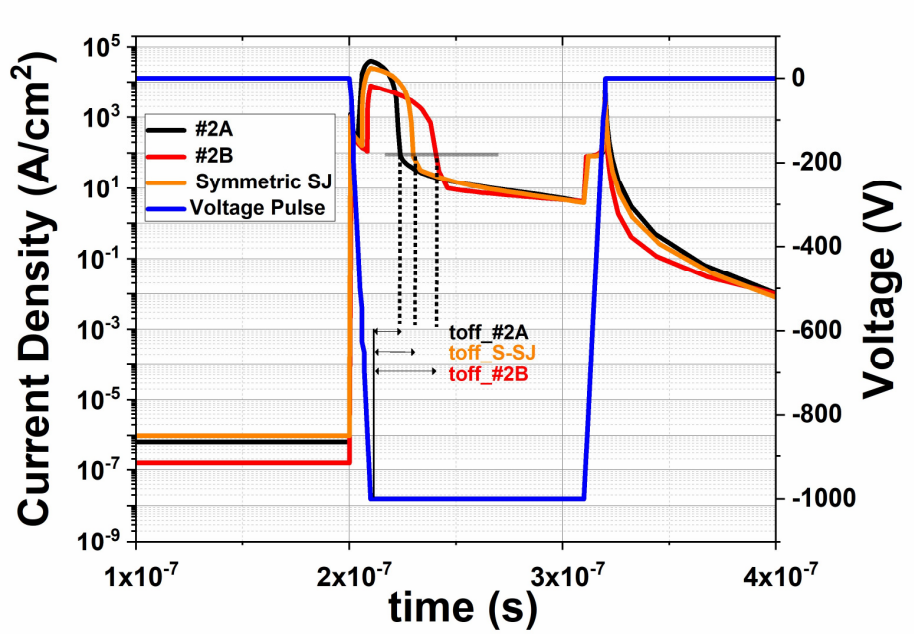


Figure 5.19: Current density vs time for the 3 different SJ design. The turn-off time(toff), defined as the time where the current density reaches the value of 10^2 A/cm^2 (horizontal black line in the figure), of #2A is much smaller than the other structures(toff(#2A)=135 ns, toff(#2B)=310 ns, toff(S-SJ)=195 ns). However, the dynamic current density peak obtained with #2A is much higher.

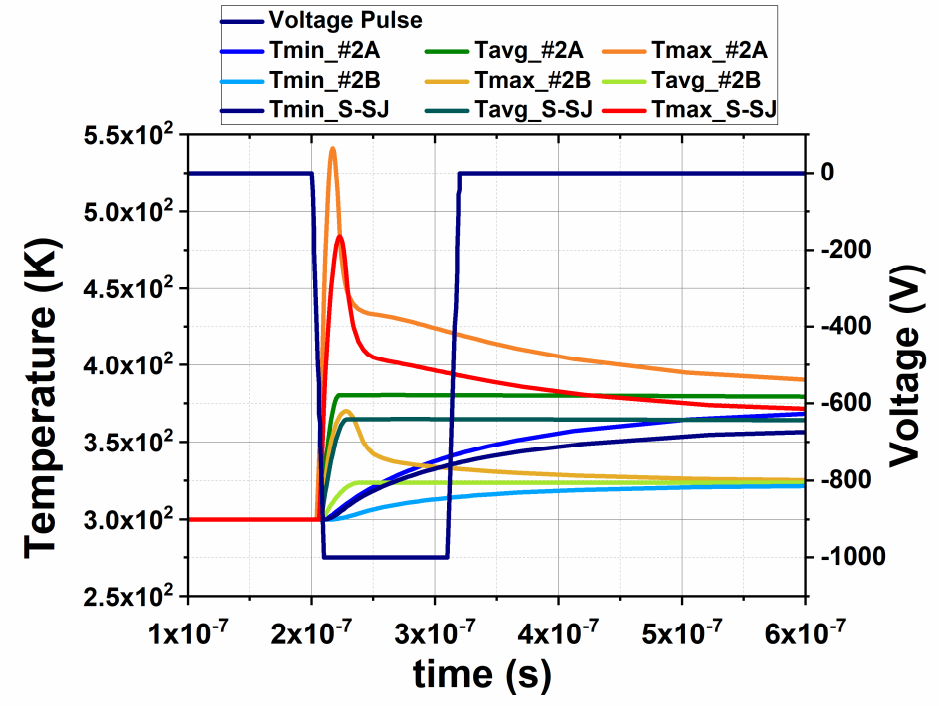


Figure 5.20: Temperature vs time for the 3 different SJ design. The maximum temperature is observed for #2A and it is ~550 K. The average temperatures for #2A, #2B and S-SJ are 375 K,325 K, 360 K, respectively. These discrepancies arise from the different self-heating effect which is related to the current density behavior shown in fig 5.19.

On the other hand, the enhanced self-heating is able to restore balance condition much faster than in the S-SJ and #2B. Therefore, if the instantaneous junction temperature and current density increment can be considered as non-destructive mechanisms, it is possible to state that #2A reacts better to the dynamic imbalance with a reduction of the turn-off time defined as in figure 5.19. A fair performance comparison needs to include also the on-state current density.

The cross-sectional structures adopted for the on-state simulations are similar to figure 5.18, but an n+ top layer (of 1 μm) has been inserted. The total current of structure #2B will be much higher than the others as the depletion region mainly extends in the non-conductive pillar.

However, the comparison needs to be performed by inspecting the R_{on_spec}. The R_{on_spec} has been calculated in the linear region at room temperature (RT), as illustrated in the figure 5.21(a). #2A has the lowest R_{on_spec} (0.34 $m\Omega \cdot cm^2$) compared to #1 (0.44 $m\Omega \cdot cm^2$) and #2B (0.62 $m\Omega \cdot cm^2$) at RT. In addition, also if R_{on_spec} is calculated at the average junction temperature reached by the device under transient condition (figure 5.13), #2A outperforms the other device structures (figure 5.21(a)).

Distinct considerations need be done in case the incomplete ionization cannot be neglected in both pillars (as in diamond devices). In that specific circumstance, a more complex dynamic recovery takes place and the ionization time constants for both dopant species contribute to the rebalancing and the temperature distribution in the device.

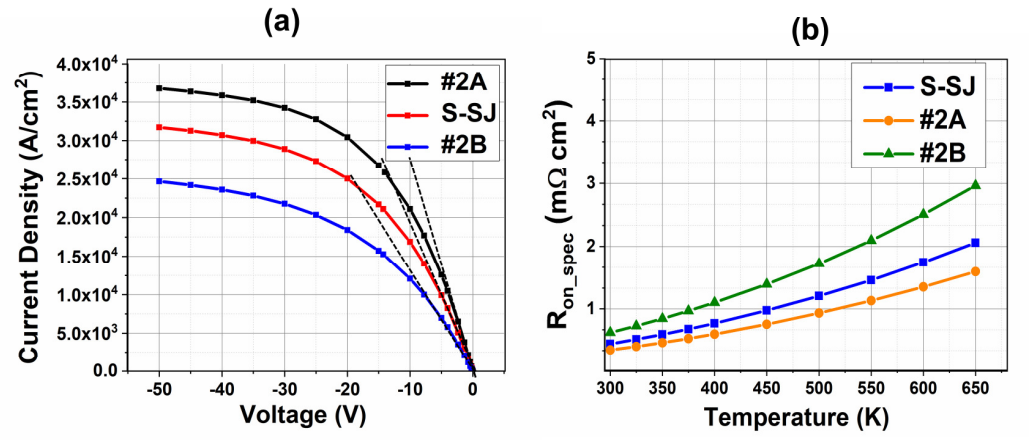


Figure 5.21: RT on-state current density for the 3 SJ design (a) and specific on-state resistance vs Temperature (b).

5.4.2. Kink effect in MOS capacitors

The advent of wide bandgap semiconductors has led to the discovery of unique power device structures such as HEMT for lateral GaN devices and junction barrier Schottky field effect transistors (JBSFETs) for SiC. At the same time, previous Si-based device architectures have been fabricated with this new class of materials (i.e. inversion/depletion MOSFETs, IGBTs,etc.) showing exceptional performance when compared with the previous class of Si-based devices. In both cases, a good percentage of these structures relies on a fundamental physical component which role is crucial in determining the electro-thermal performance of the final device: the metal-oxide-semiconductor (MOS) stack. Among the properties that more influence the electrical behaviour of WBG MOS stacks, the incomplete ionization is undoubtedly one of the most interesting one. Only few studies have been dedicated to the analysis of the incomplete ionization in WBG MOS-based devices. Arnold [327], extended the well-known charge sheet model, based on the analytical solution of the Poisson equation, to SiC devices. The main findings of that study revealed that the relationship between the inversion charge concentration and the Fermi level potential in the case of deep level impurities had the main effect of a threshold voltage (Vth) shift which was more pronounced for low temperatures and higher activation energies. On another hand, Raynaud et al. [328] focused their attention on the effects of deep level impurities on the C-V curve of SiO_2/SiC based MOS capacitors which were responsible of an abnormal "kink" effect near the flatband voltage (V_{FB}). Nevertheless, the non-ideal

semiconductor-insulator interface with the presence of multiple energy trap levels has usually screened the effects of the incomplete ionization on the Vth and especially on the Kink effect in the CV curve. In this section, a systematic study of the kink effects due to the incomplete ionization on the C-V measurements/simulations with reference to diamond MOS capacitors is carried out. The frequency-temperature dependence of this effect is accurately analysed by means of TCAD simulations providing new insights in the nature, effects and usefulness of this phenomenon.

5.4.2.1. The MOS capacitor physics and CV modelling

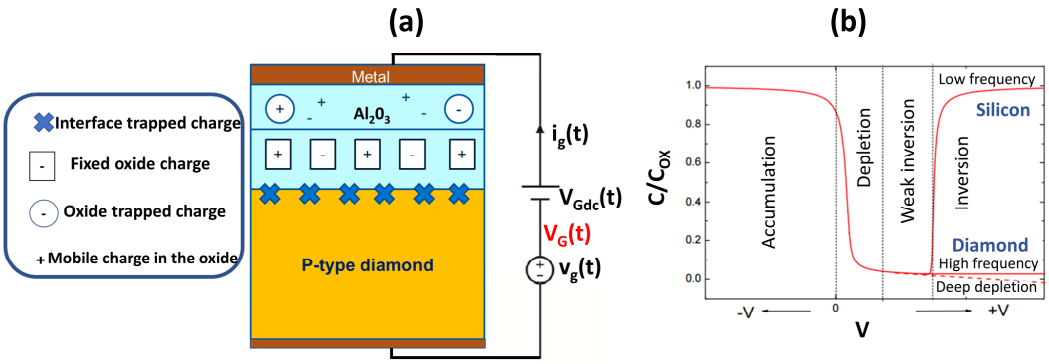


Figure 5.22: (a) Schematic of a p-type diamond MOS capacitor with the driving schematic for the small signal ac analysis and (b) typical regimes observed in the CV curves for Si and diamond p-type MOS capacitor. Even a low frequency ac signal is not able to generate an inversion layer in diamond (due to its wide bandgap).

Experimental CV measurements for MOS structures are typically obtained by applying a DC signal overlapped with an AC signal (typically a sinusoid) between the gate-bulk contacts (figure 5.22(a)). The resulting signal applied to the structure, $V_G(t)= V_{Gdc}+ vg(t)$, is therefore able to bias the device at a specific voltage (with the DC component) and evaluate the response of the charge (in the semiconductor and in the oxide) by means of the AC signal. The amplitude and the frequency of the AC signal are crucial parameter for the CV analysis: on one hand, the amplitude of the signal needs to be "small" with the respect to the DC bias and voltage step; on another hand, the chosen ac frequency of the signal has a tremendous impact on the traps' response and on the ability of the carriers in the semiconductor to follow the applied ac signal. In an ideal case (no interface/oxide traps, fixed charge, etc.) the total impedance is the

series of the oxide capacitance (Cox) and the semiconductor resistance (Rs) and capacitance (Cs), which is function of the surface potential (Ψs) and, hence, of the specific operation regime (accumulation, depletion, inversion, deep depletion). An extensive analysis of the MOS stack can be found in [152, 220] and it is beyond the purpose of this work. It is however worth mentioning that in the case of WBG semiconductors, due to the low intrinsic carrier concentration and the high minority carrier generation time from a mid-gap state at RT, the inversion regime is not visible in MOS capacitors (without an oxide overlapping the source and drain regions and in the absence of UV light excitation) even when a low ac signal frequency is employed (figure 5.22(b)). Additionally, the presence of interface states and of oxide tunnelling leakage current radically modifies the equivalent circuit and influences the impedance measurement [167], as schematically illustrated in the figure 5.23. Consequently, the interpretation of the CV measurements for MOS stacks necessarily passes through the complete understanding of the gate leakage current and in general the dynamic and the nature of traps at the interface.

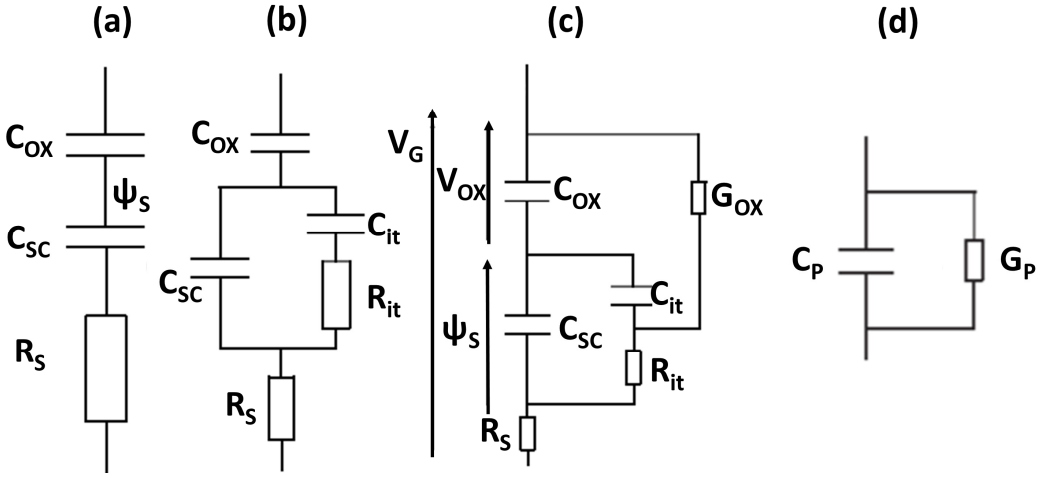


Figure 5.23: (a) Equivalent small signal circuit of a MOS capacitor depicted in figure without interface states and leakage current; (b) equivalent circuit in the case of interface states modelled with a complex impedance Zit=Rit+1/jωCit; (c) equivalent circuit in the case of a gate oxide leakage mechanisms similar to the one described in [167] where the injected carriers from the gate metal then interact with the valence band ; (d) schematic representation of the measured impedance. As illustrated in (b) and (c), the measured Cp could be much more complex that the simple series of Cox and Csc (a).

TCAD small signal analysis simulations adopt a different approach if compared with the experimental setup. The assumption at the basis of the ac analysis in Sentaurus TCAD is similar to the case of Spice-like simulators. In general, the input voltage signal amplitude is assumed to be so small that its application results in the absence of

harmonic content at the output. Consequently, after the DC operating point solution is computed, the nonlinear circuit equations are expanded in a Taylor series about the DC operating point and only the first order terms are kept.

In detail, when an ac analysis is performed, the simulator computes the admittance matrix (Y-matrix) which describes how the currents (δi) in a circuit would react if the applied voltages at different contact nodes of the circuit receive a small perturbation δv (27).

$$\delta i = Y \cdot \delta v = (A + j \cdot \omega \cdot C) \cdot \delta v \tag{27}$$

The Y-matrix is composed of two parts, the real part (A) which is called the conductance matrix and the imaginary part (C) called the capacitance matrix. The matrix Y has been shown in (28a-b) for the case of 2 and 4 terminals, respectively. In other words, A measures the in-phase response of the current with the respect to the voltage whilst C measures the out of phase response.

$$\begin{bmatrix} i(g) \\ i(d) \\ i(s) \\ i(b) \end{bmatrix} = \left(\begin{bmatrix} a(g,g) & a(g,d) & a(g,s) & a(g,b) \\ a(d,g) & a(d,d) & a(d,s) & a(d,b) \\ a(s,g) & a(s,d) & a(s,s) & a(s,b) \\ a(b,g) & a(b,d) & a(b,s) & a(b,b) \end{bmatrix} + j\omega \begin{bmatrix} c(g,g) & c(g,d) & c(g,s) & c(g,b) \\ c(d,g) & c(d,d) & c(d,s) & c(d,b) \\ c(s,g) & c(s,d) & c(s,s) & c(s,b) \\ c(b,g) & c(b,d) & c(b,s) & c(b,b) \end{bmatrix} \right) \begin{bmatrix} v(g) \\ v(d) \\ v(s) \\ v(b) \end{bmatrix} \tag{28a}$$

$$\begin{bmatrix} i(g) \\ i(b) \end{bmatrix} = \left(\begin{bmatrix} a(g,g) & a(g,b) \\ a(b,g) & a(b,b) \end{bmatrix} + j\omega \begin{bmatrix} c(g,g) & c(g,b) \\ c(b,g) & c(b,b) \end{bmatrix} \right) \begin{bmatrix} v(g) \\ v(b) \end{bmatrix} \tag{28b}$$

One of the intrinsic properties of the Y-matrix is its internal symmetry (i.e. $x_{jy}=x_{yj}$). In the case of a 2 terminals circuit such as the one under investigation, the diagonal terms are also equal and opposite to the antidiagonal terms.

5.4.2.2. TCAD analysis of the Kink effect

A simple 1D TCAD model of the MOS stack has been defined in order to capture the peculiar effects of the incomplete ionization on the CV characteristics of MOS-based devices. A metal workfunction of 4.2 eV (corresponding to the theoretical value of Al) has been used for the gate metal contact while the oxide region consists of 40nm (tox) of Al_2O_3. Interface states, fixed charges and other non-idealities which may affect the

simulations and the measurements have been neglected at this stage. Under these simplified assumptions, the gate voltage (V_G) is related to the surface potential (Ψs) by the expression $V_G = V_{FB} + \Psi s - Qsc/Cox$, where $Cox = A^* \varepsilon_{ox}/tox$ is the oxide capacitance and Qsc is the semiconductor charge. If one assumes a p-type diamond boron doped layer (modelled with the incomplete ionization equations shown in 5.2. and with a temperature-electric field independent cross section $\sigma=1x10^{-12}$ cm^2) of thickness=0.5 µm and doping=$1x10^{17}$ cm^{-3}, and then performs an ac small signal analysis at f=1 kHz, a clear kink effect due to the presence of deep dopant levels is observable close to the V_{FB} (figure 5.24(a)). Such an effect is highly dependent on many parameters, such as the dopant concentration, the operational temperature, etc. As illustrated in 5.24(b) higher dopant concentration broaden the capacitance peak due to the incomplete ionization. This is a clear consequence of the results depicted in figure 5.1, which shows a reduced activation ratio for increased dopant concentration (at a fixed operational temperature).

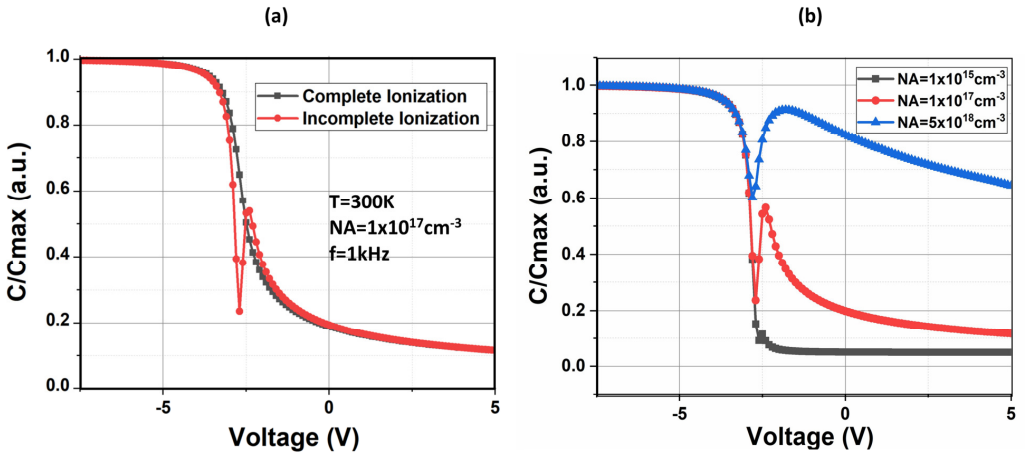


Figure 5.24: (a) RT CV characteristics showing the comparison between full and partial ionization (b)effects of different dopant concentration on the kink effects at RT. Cross section has been fixed at $\sigma=1x10^{-12}$ cm^2.

The occurrence of the kink effect can be understood by looking at the equation (19a) and (19b) (for donor and acceptor impurities, respectively). When the device goes from accumulation to depletion the electric field at the interface abruptly changes and so does the total level of ionized impurities. In detail, for V_G slightly smaller than the V_{FB} the electric field at the interface is significantly reduced if compared to the accumulation regime and the CV behaves like the CV corresponding to a MOS stack with a semiconductor doping close to the one calculated at the thermodynamic equilibrium condition.

After the V_{FB} the band banding changes and so does the electric field which becomes negative and allows full ionization of acceptor at the interface. Therefore, the kink effect connects two different MOS regions, namely the accumulation and the depletion regime in which the change in the band bending allows, within a small voltage range, a significant variation in the total level of ionized impurities. This can also be clearly understood from figure 5.25(b) in which the variation of the electric field around the kink (refer to the 1D model in figure 5.24(a)) has been plotted. As it can be observed a smaller electric field at V_G= -2.75 V due to the proximity to the V_{FB} is responsible for a reduced acceptor activation.

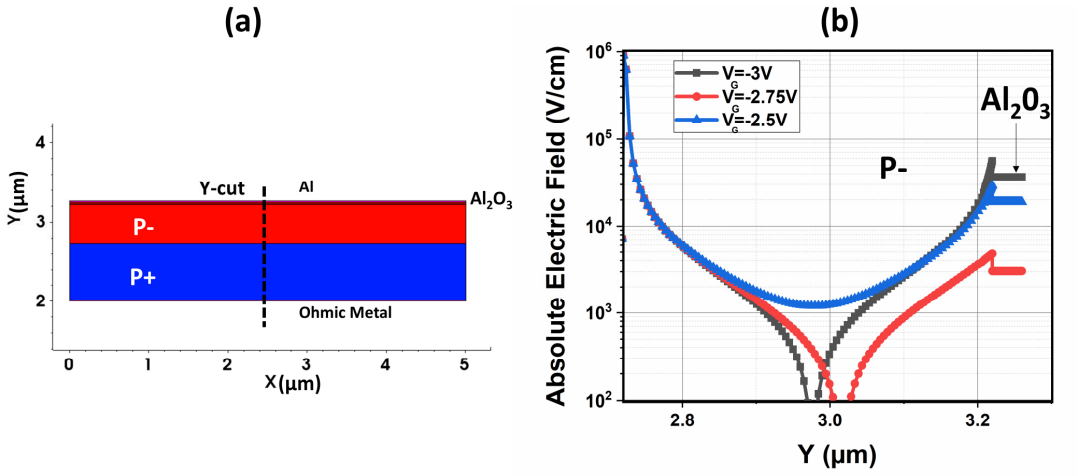


Figure 5.25: (a) Schematic cross section of the simulated p-type diamond MOS stack and (b) RT electric field distribution in the device for different gate voltages.

Temperature is another aspect which must be accurately discussed. A rise in the device' temperature has as a main consequence the increase of the activation ratio calculated at the thermodynamic equilibrium, which hence reduces the kink in the CV. On the other hand, the enhanced carrier freeze-out at lower temperature shows an amplified kink effect which eventually vanishes for very low temperatures (~100 K). The low temperature behaviour illustrated in figure 5.26 is however highly dependent on the dynamic of the incomplete ionization.

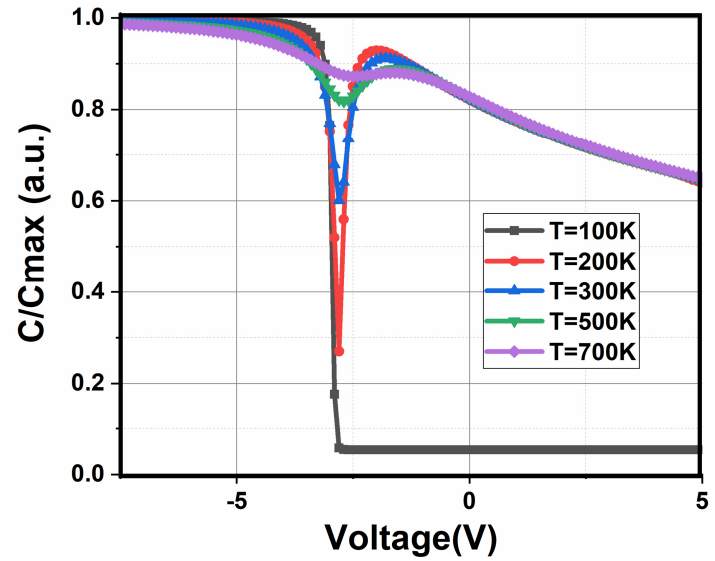


Figure 5.26: Temperature effects on the CV characteristics for a MOS capacitor with a doping level of $5x10^{18}$ cm^{-3} at f=1 kHz.

With the exponentially reduced time constants at cryogenic device temperatures (see figure 5.27), if the reciprocal of the ac small signal frequency is smaller than the ionization/deionization time constant (equation 23), the carrier dynamic is not able to instantaneously follow the ac signal modulation and the total acceptor concentration remains close the thermodynamic value (calculated at that specific temperature).

Such a frequency dependence has been usually neglected in the previous analysis of the kink effect in Si and Si based MOS capacitors[328].

In figure 5.27, the impact of the cross section on the kink effect is clearly demonstrated. Smaller cross sections increase the time constant of the dopant species which will eventually not follow the ac signal and fails to modulate the semiconductor capacitance in the depletion/deep depletion regime. In real devices, interface traps and fixed charges, which usually lead to an equivalent small signal circuits similar to the one depicted in figure 5.23(c), have often screened this peculiar effect of the incomplete ionization. Additionally, the presence of a gate leakage path complicates the overall impedance analysis and can sometimes lead to measured capacitance which do not reflect the real value of the semiconductor capacitance [167].

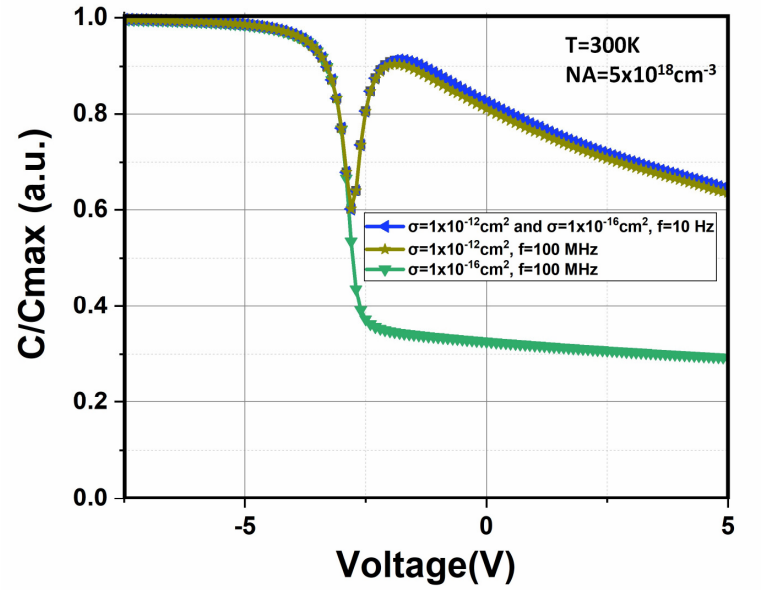


Figure 5.27: CV characteristics for a MOS capacitor for different frequencies and cross sections.

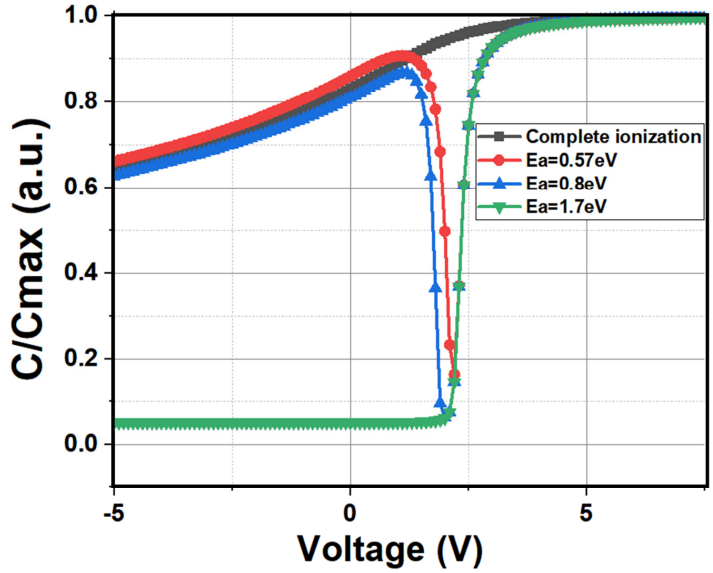


Figure 5.28: CV characteristics for a n-type MOS capacitor at RT for different activation energies.

In low temperature-frequency CV of indium-based Si MOS capacitor [329], the kink effect has sometimes been recognised and correctly attributed to the presence of deep dopant impurities rather than interface traps. In SiC and other WBG, the poor interface quality with interface state density (Dit) > $1x10^{13}$ cm^{-2} has usually resulted in CV peaks which cannot be attributed to the incomplete ionization.

Consequently, a clear distinction between interface (deep) traps and incomplete ionization' effects on the kink in the CV curves is therefore difficult to obtain due to

the complexity and non-uniformity of the traps distribution and their temperature-field dependent cross section. Improvements in the interface quality may allow to correctly recognize the incomplete ionization kink effect which will be more evident for low frequency, low temperature, high activation energies (figure 5.28) and high doping concentration (figure 5.24(b)) with such domain limited by the specific time constant of the deep dopant species. In particular, when the quality of the semiconductor/oxide interface will be improved, the kink effect could be adopted as a powerful instrument to measure several important features of WBG MOS-based devices, such as the effective equilibrium hole/electron concentration, the activation energy of the dopant species and the time constant of the deep impurities[330].

5.4.3. Device terminations and dynamic punch through

Other physical mechanisms due to the dynamic activation of the deep level dopants can have serious consequences on the transient behaviour of semiconductor devices. For example, if a reverse voltage pulse is applied to an asymmetrical p-n junction in which the incomplete ionization effect takes place in the lowly doped region, and the rise time of the pulse is smaller or comparable with the ionization time constant, the width of the depletion layer becomes function of the time.

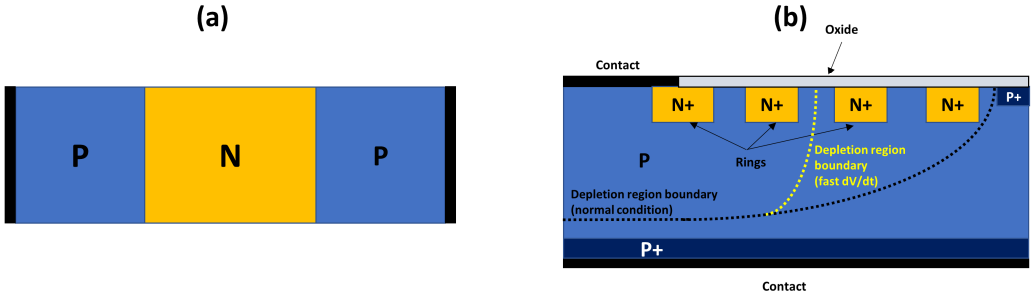


Figure 5.29: (a) Schematic cross section of p-np stack in which dynamic Punch-through mechanisms could be triggered by the dynamic of the incomplete ionization which affects the n-type layer. (b) Fast dV/dt effects of termination region in which the depletion region boundary' extension is limited the fast voltage pulse.

In detail, as already discussed in [320], the maximum depletion region width (Wd) is observed at the end of the rise time of the reverse pulse since the number of activated dopants is at its smallest dynamic value ($Wd \propto \sqrt{\mathbf{N}}$, where N is the doping of the lowly doped region) and it recovers to the static (and minimum) value with a time constant which is proportional to the ionization time constant , like the one defined in (23) for acceptors. This dynamic extension of the depletion region could generate a "dynamic Punch-Through (PT)" effect in p-n-p (figure 5.29(a)) regions which are present in devices like MOSFETs, BJTs,etc.

In Thyristors, this dynamic PT could trigger latch up phenomenon which can be prevented with a redesign of the device structure (i.e. anode shorts, etc.) [313, 320, 331]. Lades et al.[320] have demonstrated that prolonged switching from ON to OFF state can be generated in cryogenic operation of 4H-SiC double implanted MOSFET in which boron doping is used for a deep implanted base profiles. The slight increase in the device' temperature and the occurrence of a highly localized current flow can however be compensated with a double base implant. While the threshold voltage is regulated by the channel implant, the increase of the base-width and doping through the second implant (body implant) counteract the dynamic punch-through effect while, at the same time, avoids the triggering of the bipolar BJT.

On the other hand, Van Brunt et al.[332] have demonstrated the detrimental effects of fast dV/dt ramps on the catastrophic failure of 4H-SiC SBDs. The destruction point was identified in the edge termination area in contrast with the typical active area breakdown occurring in avalanche tests. In this scenario, a limited expansion rate of the depletion region due to the dynamics of Al could be responsible for the premature destruction of the device.

These effects will be even more detrimental in case of junction termination of diamond devices made with n-type dopants (figure 5.29(b)), so suggesting that floating metal rings could be more resistant to fast dV/dt and avoid the issues related to the time dependent depletion region expansion. In addition, the optimization of Junction termination extension (JTE), which is highly sensitive to the implanted dose, could be radically transformed by the additional considerations deriving from the application of fast dV/dt. In this context, TCAD simulations could represent a useful tool for the prediction of the electro-thermal behaviour of the devices affected by the dynamic of deep impurity levels.

However, only a correct choice of the thermal model and the inclusion of the energy-temperature dependent carrier relaxation time for that specific material would allow for a correct estimation of the device' characteristics under avalanche conditions.

5.5 Conclusions

The physics and the main consequences of deep dopant levels have been addressed in this chapter. Extended depletion region widths due to the incomplete ionization have been studied for the case of a simple 1D p-n junction and a theoretical model has been assessed and compared with TCAD simulations.

The charge imbalance effects of the partial ionization have been analysed with reference to the design of 4H-SiC SJ diode. The static breakdown voltage is not influenced by the incomplete ionization effect as the high reverse electric field is able to activate all the dopants in the structure. However, when a very fast reverse pulse is applied to the SJ structure the dynamic ionization leads to an imbalance charge condition which has the effect of increasing the total current density and the local device temperature (up to 500K in the example considered). It has been shown that it is possible to redesign the SJ diode, while maintaining the ideal charge balance, in order to simultaneously improve the specific on-state resistance and the dynamic resistance to the charge imbalance due to incomplete ionization.

A peculiar kink effect due to the incomplete ionization model in CV curves of MOS capacitors has been presented and its effects distinguished by the kinks generated by interface traps and levels. Finally, the detrimental effects of dynamic punch-through and fast dV/dt applied to device termination have been described and reviewed.

Due to their reliability' issues, it is therefore possible to conclude that the transient effects of the incomplete ionization should be avoided whenever possible. There may however exist situations in which due to the lack of other dopant atoms (as in diamond) or due to the lack of better dopant species to perform deep implanted profiles (as in SiC), the use of deep dopants cannot be avoided.

In such cases, the incomplete ionization effects cannot be neglected, and they should be both considered and in the finite element modelling and in the analysis of the experimental results.

6 FIGURES OF MERIT, COMPARISON AND BENCHMARK OF DIAMOND DEVICES

6.1 Introduction

Benchmarking diamond devices against other WBG semiconductor-based devices is of the utmost importance to identify the power-frequency-temperature domain in which diamond is capable to outperform the existing class of semiconductor power devices. In this chapter, limits and usefulness of figures of merits (FOMs) applied to diamond and other semiconductors are discussed in detail. Key parameters such as the breakdown voltage, the switching loss and the device surface have been defined and a more global approach for comparing power devices has been introduced. Based on this approach, a comparison between vertical diamond FETs, 4H-SiC and GaN FETs for a breakdown voltage of 6.5 kV is provided. Successively, a thorough theoretical comparison between optimized diamond Schottky barrier diodes and bipolar diodes is carried out. This analysis points out the effects of different operating temperature and switching frequency on the performance of different diamond diodes and allows to identify the optimal device structure depending on the specific application. In the second part of the chapter, the system level benefits of diamond FETs and diodes are

accurately analysed. The chapter concludes with the future perspective of diamond and a roadmap with the future challenges for this material.[4]

6.2 Limits of existing figures of merits and their application to diamond power devices

Power semiconductor devices are assessed against each other by conduction, switching and OFF state losses. A perfect figure of merit would take each contribution into account, with specific interactions at the system level (i.e. thermal, driving, electromagnetic compatibility, reliability, sourcing and cost). Unfortunately, it is almost impossible to compare different devices based on different technologies and/or materials based on a simple figure of merit. As an example, switching losses are not only dependent on the power device itself but also on the driving circuit, the topology employed (e.g. based on soft or hard switching) and parasitic associated with packaging. The existing figures of merit have failed to predict this system-level impact from the physical parameters of the power devices [9], mainly due to the complex requirements and peculiarities of each application whereas figures of merit target a global comparison. In this context, paragraph 6.2.4. will introduce a system-level benchmark for diamond power devices.

One of the most used figure of merit in power semiconductor devices is Baliga's Figure of Merit (BFOM) defined in [3] and equation (29). This BFOM has been derived from the specific ON state resistance (equation 30), which can be expressed by equation 29 in the case of several assumptions. Consequently, equation 31 introduces the BFOM in the typical trade-off between the specific ON state resistance R_{on_spec} and the breakdown voltage BV. However, the assumptions required to directly relate the BFOM with the R_{on_spec} cannot apply in the context of diamond power devices; in diamond bulk devices, the incomplete ionization of dopants, and in 2DHG devices, the sheet carrier concentration and specific 2DHG mobility must be considered.

[4] The material in this chapter has been the object of the following publication: Donato, N., Rouger, N., Pernot, J., Longobardi, G., & Udrea, F. (2019). Diamond power devices: State of the art, modelling and figures of merit. Journal of Physics D: Applied Physics, (accepted on 17th October 2019).

Consequently, equation (31) is no longer valid and the specific R_{on_spec} is no longer derived by the BFOM. As a summary of this discussion, the list of assumptions used to define the BFOM is as follows:

1. Unipolar type devices (i.e., no minority carrier injection mechanisms);

2. Complete ionization of dopants (i.e., $N_D=N_{D0}$ or $N_A=N_{A0}$);

3. Non-Punch-through (NPT) design of the drift region;

4. 1D BV due to a constant critical electric field (Ec);

5. Fixed value of mobility and critical electric field;

6. Uniform doping distribution in the drift region;

7. R_{ON} is only due to the resistance of the drift region (e.g., the series and contact resistances are neglected);

8. 1D current spreading in ON state (e.g., no cell effect or no 2D/3D current spreading);

9. Bulk drift region (i.e., no superjunction or floating islands).

In equations (29-31), μ_n is the mobility for electrons (μ_p for holes), ε is the dielectric permittivity of the semiconductor, Ec is the critical electric field, ρ is the resistivity, S is the active area, L is the length of the drift region, n(p) the activated electrons(holes) concentration and q is the electron charge.

$$BFOM = \mu_{n,p} \cdot \varepsilon \cdot Ec^3 \tag{29}$$

$$R_{ON\_spec} = R_{ON}S = \rho \cdot L = \frac{L}{q \cdot (\mu_{n,p} \cdot n,p)} \tag{30}$$

$$R_{on\_spec} = \frac{4 \cdot BV^2}{\mu_{n,p} \cdot \varepsilon \cdot Ec^3} \tag{31}$$

Consequently, the specific ON state resistance (R_{on_spec}) is used as a figure of merit to compare different devices or materials, for a given range of breakdown voltages. The ON state resistance is typically measured by pulsed I-V or calculated based on analytical formula or numerical analyses. The device area is extracted from the active area or device area, including or not the termination region. The breakdown voltage is measured or calculated based on specific hypotheses. These points and the related assumptions will be briefly described in the following subsections. There are mainly four issues with the direct comparison of the R_{on_spec} value among different devices or

materials at the same breakdown voltage and the use of R_{on_spec} as a figure of merit: the lack of direct switching loss estimation, the different assumptions related to Ron, S and BV between devices or materials, the lack of link with the thermal conductivity and the scalability of Ron with the surface. The junction temperature at which the comparison is carried out must also be discussed. Other related figures of merit have been used, such as A or mA per gate width or A/cm² as (i.e. the maximum current or current density values), which are similar to R_{on_spec} and the forward bias must be given. In the case of MOS devices, a fair comparison must also include the transconductance, the threshold voltage and gate voltage range. In order to relate the figure of merit to the switching losses, other figures of merit such as Ron·Qg, Ron·Qgd or Ron·Qoss have been introduced [4, 333, 334]. These figures of merit are clearly more complex than the R_{on_spec} FOM alone, albeit harder to predict for diamond power devices. Indeed, actual diamond power devices still have small active areas which makes difficult a precise measurement of the capacitors related to the active area. These figures of merits are best suited for unipolar devices but cannot be used in the context of bipolar devices due to recovery charges and their impact on switching losses. Specific studies are required on diamond power devices optimization and measurements, to further demonstrate low Qg (gate charge), Qgd (gate-drain charge) and Qoss (output charge), whereas most of the recent achievements concentrated on reductions in R_{on_spec}. Accordingly, the control of the Miller ratio between Qgd and Qgs is also an important criterion to consider. Immunity to dV/dt and dI/dt and the maximum turn ON and turn OFF switching speeds are equally relevant. Besides these parameters, the gate leakage must also be considered.

6.2.1. Breakdown voltage

To compare and benchmark different devices and materials, the breakdown voltage must be similar. Unfortunately, the breakdown voltage might not be limited by avalanche as in the case of Silicon or Silicon-Carbide devices but by the maximum level of leakage current (mA ou µA per cm², nA per gate width). This is especially the case if the device is used in harsh environments at elevated ambient temperatures [93, 181]. The main issues with high leakage currents are related to the losses in the OFF state and possible thermal runaway. A fair limitation for the leakage current is that the

OFF state losses at high temperature represent only a few percent of the total conduction and switching losses. Typically, the OFF state leakage current at the highest junction temperature should not exceed 10 µA/cm² to 1 mA/cm² for breakdown voltage above 1 kV. For the theoretical analysis of diamond power devices, this limit of leakage current must be considered, at the same time as the critical electric field computation in OFF state. Simplified figures of merit consider a maximum peak of the electric field.

This is not ideal when comparing power devices at different breakdown voltages. Indeed, the maximum critical electric field is a function of the drift region doping level, as presented in figure 6.1, when considering the avalanche breakdown for an asymmetric 1D p-n junction. As mentioned by Chicot et al., the 3D electric field could reduce the peak electric field in the drift region, and more assumptions are required to take the junction termination efficiency into account [269]. In the case of Silicon and Silicon Carbide, such a junction termination efficiency can be typically above 90% for vertical devices [335, 336], whereas optimizations for diamond are still required. As a summary, precautions must be observed for the breakdown voltage definition both in experiments and in theory with Diamond power devices.

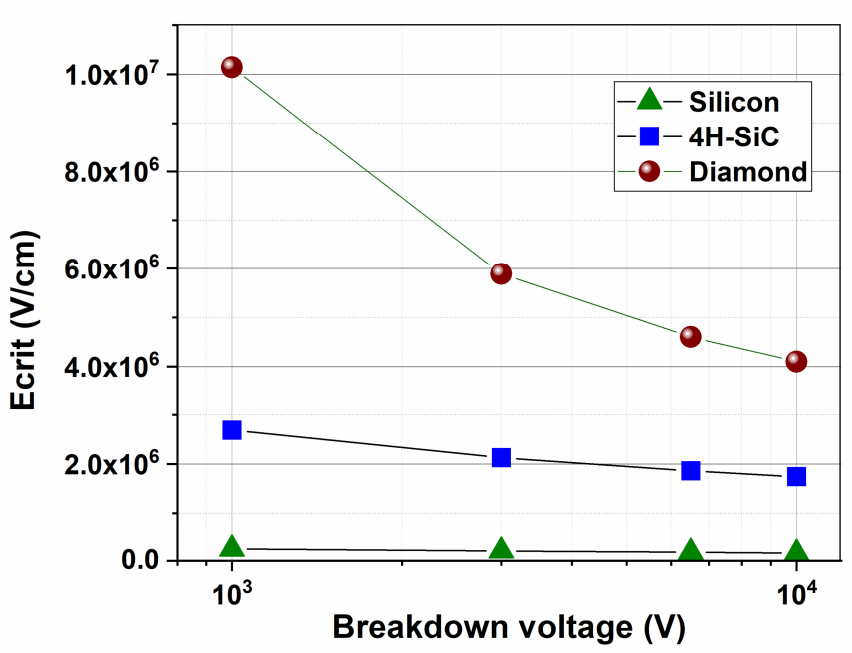


Figure 6.1: Calculated 1D critical electric field (Ec) as the function of breakdown voltage, for Si, SiC and Diamond in NPT condition. The avalanche breakdown with state of the art impact ionization coefficients is assumed [337]

6.2.2. Current rating and device surface

The surface used for the current per area or the specific ON state resistance figures of merit is debatable. In the case of pseudo vertical devices such as diamond Schottky diodes, the surface of the Schottky contact is considered most of the time, albeit a larger surface is required to have the actual device. In the best case, the termination and contact areas are mentioned, additionally to the active area which allows a proper scaling of the performance and defining appropriate figures of merit. Similarly to other power devices, the current rating of diamond power devices is typically governed by thermal considerations. A maximum power density must be fixed to calculate the ON state current and current density. This power loss density is typically fixed between 50 and 300 W/cm², taking into account conduction losses with or without switching losses. However, in the case of diamond devices, the diamond substrate can be used as an efficient thermal spreader. In this context, the limit of 300 W/cm² can be increased and must be further investigated in a close relationship with the dicing capability of diamond devices. Once the operating point of the power device is fixed by this thermal limit, the ON state current and ON state voltage drop could be determined. In the case of FET devices, the relationship between the Ron and the ON state current is straight forward, and the Ron can be scaled easily with the active area (while neglecting additional contact pad areas and junction termination area). However, for the devices with a barrier or subject to resistivity modulation, an equivalent "unipolar Ron" (defined as the voltage/current ratio at a specific operating point, i.e. Ron=Von/I(Von)) must be extracted, which does not scale linearly with the active area [9]. As an example, figure 6.3 shows the ON state current density of diamond vertical power devices at the limit of 500 W/cm² for different breakdown voltages and junction temperatures. It is assumed that only the drift region accounts for the total ON state resistance. The models used for figure 6.2 and 6.3 (defined in chapter 2 and 5) are incomplete ionization, doping and temperature dependent mobility, avalanche breakdown under NPT condition, only conduction loss (i.e. duty cycle equal to 1 and no switching losses). These values are the highest possible with diamond, based on the 1D breakdown voltage calculation described hereinbefore. The conclusion is that a unipolar diamond device operating at a high temperature of 570 K and with a breakdown voltage capability of 3.3 kV can have a current density ~400 A/cm².

Consequently, a 3 mm x 3 mm 3.3 kV diamond vertical device can have a current rating of 20+ A at 57 0K, which is unprecedented with other materials.

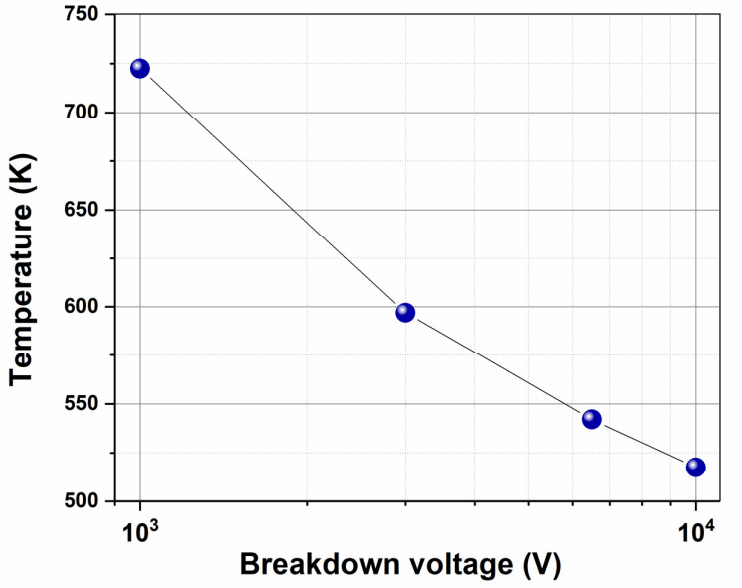


Figure 6.2: Optimal temperature vs BV in NPT conditions for p-type diamond drift region. The optimization procedure calculates the critical electric field (Ec) in NPT conditions and then determine the thickness and doping level of the drift region. Successively, the optimal temperature at which the R_{on_spec} is minimum, is extracted. The incomplete ionization includes additional temperature dependent parameters such as degeneracy factor, density of states and bandgap. Leakage current mechanisms and dielectric degradation are not considered in this procedure.

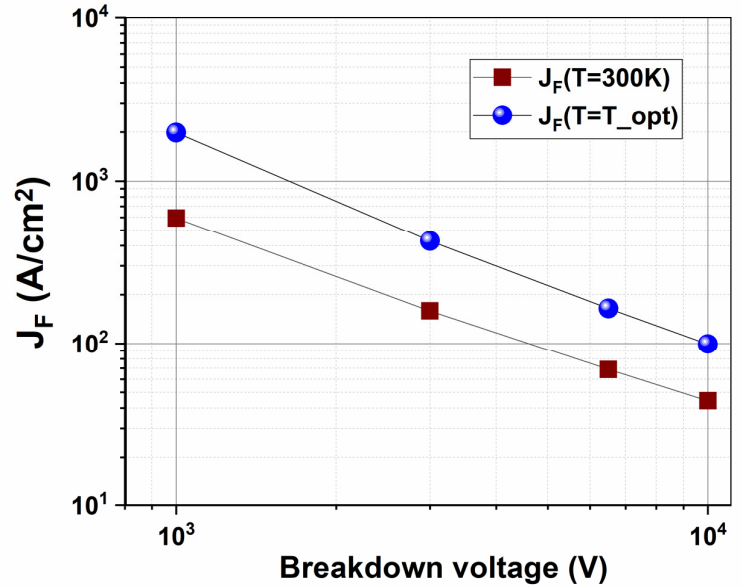


Figure 6.3: ON state current density (J_F) for vertical unipolar p-type diamond devices, as a function of breakdown voltage and for a maximum conduction loss density ($P= J_F^{\,2} \cdot R_{on\_spec}$) of 500 W/cm². Red squares are at room temperature and blue circles at the optimal temperature for each breakdown voltage (see figure 6.2), where the incomplete ionization of Boron and the hole mobility minimize the ON state resistance.

At 10kV, the maximum current density is ~90 A/cm² at the optimal temperature (~500 K). This means that a 9 mm² diamond device could have 8+ A current rating. The advantages of diamond power devices are clearly highlighted in the context of high power, high temperature and higher switching speeds.

6.2.3. Switching and total losses

For a fair comparison between different power devices, it is also important to consider the switching losses. While estimating the conduction loss is straightforward with appropriate conduction models, the prediction of switching losses highly depends on multiple parameters such as the parasitic capacitors, the gate driver associated to the power transistors parameters (e.g. transconductance, min and max gate voltage) and circuit elements (e.g. parasitic inductances and capacitances). A fair comparison for switching losses must include similar electromagnetic compatibility (EMC)/electromagnetic interference (EMI) constraints, as large gate currents in MOSFET will lead to reduced switching losses but very high dV/dt and dI/dt values. Such high transient values can have negative impacts on motors, cables, common mode filters [338], and can cause false switching through the Miller capacitor [339]. Consequently, the high frequency harmonics must be either filtered or damped down thanks to the gate driver. The optimization of the loss versus EMI trade-off is therefore dependent on the application, with constraints on volume, mass, efficiency, packaging technologies and EMC standards. Moreover, there is no report yet on the power switching loss measurements using diamond FETs, mainly due to the limited availability and small size of the previously reported diamond FETs. Such a complete comparison between materials will be specific to each application and it is almost impossible to provide a fair and realistic case study. There are however several characterizations of diamond diodes in power commutation cells [340-342], mainly on SBD diamond diodes showing small recovery-like currents due to the diode intrinsic transition capacitor. The main difficulties in the experiments are to associate small size diamond diodes with power FETs having similar voltage capability and parasitic capacitors. The small signal and large signal characterization of diamond FETs are then highly desired to be able to benchmark accurately the performances of diamond power devices.

The expected realistic benefits for power electronics with unipolar diamond or ultra-wide band gap devices are to be able to match the conduction loss level of Silicon bipolar devices. Given the unipolar conduction and the absence of excess charge in the ON-state, the switching losses could be dramatically reduced. As it will be presented in paragraph 6.3, the benefits of bipolar diamond devices with an efficient resistivity modulation will be limited to ultra-high voltage and low switching frequency, due to the large built-in potential in diamond and short carrier lifetimes. Consequently, unipolar diamond devices are expected to have the highest impact at system level in the short- to mid-term. Despite the issues related to switching loss predictions with diamond power devices discussed hereinbefore, one can assume several hypotheses to predict the switching performances of diamond unipolar (and vertical) power FETs; the turn OFF losses with diamond FETs will be neglected as the channel current is turned OFF very quickly thanks to the smaller input capacitor (smaller active area) and the high transconductance, the turn ON losses are not limited by EMI issues and the drift region is considered in NPT configuration. Additionally, any other parasitic capacitance, contact resistance and device region (except the drift region) are neglected. As a result, the lowest possible switching losses in a power FET are governed by the stored electric charge in the output capacitor (C_{oss}) during the switching transition, where the C_{oss} as a function of V_{DS} can be expressed by eq (32) and (33). In equation (32), $C_{OSS(V)}$is the output capacitor as a function of the bias, which is typically the transition capacitor $C_{T(V)}$exhibiting a square root dependence with bias when the drift region is in NPT condition. At the breakdown voltage, the transition capacitor $C_{T(BV)}$ is calculated by equation (33), with $\epsilon_0 \times \epsilon_r$ the permittivity of diamond, S the active area, d the thickness of the drift region. Whereas two FETs or one FET and one diode will be associated in a power commutation cell, the active area of each power device can be different as a function of the duty cycle. As a consequence, only the C_{oss} of one power FET can be considered for the estimation of the minimum power losses $P_{sw.on}$, as proposed for example in [343] and equation (34), where V is the switched voltage and f_{sw} the switching frequency.

$$C_{OSS(V)} = C_{T(V)} = C_{T(BV)}\sqrt{\frac{BV}{V_{DS}}} \quad (32)$$

$$C_{T(BV)} = \epsilon_0 \times \epsilon_r \times \frac{S}{d} = C^*_{T(BV)} \times S \quad (33)$$

$$P_{sw.on}(V) = \frac{2}{3} \times C_{T(BV)} \times \sqrt{BV} \times V^{3/2} \times f_{sw} \quad (34)$$

In an actual application the best power device is the one minimizing total losses (35) while respecting key constraints (e.g. maximum junction temperature and power density). Therefore, the optimal device area minimizing the sum of switching losses ($P_{SW,on}$) and conduction losses (P_{on}) can be determined for a fixed set of specifications thanks to the models and discussions presented in this section and in other articles such as [343]. In equation (35) δ is the duty cycle and Ion is the total ON state current. Equation (35) could be optimized in terms of "optimal active area" S (when all the other parameters have been fixed).

$$P = P_{sw.on} + P_{on} = \frac{2}{3} \times C_{T(BV)} \times \sqrt{BV} \times V^{3/2} \times f_{sw} + \frac{\delta \times Ron_{spec} \times Ion^2}{S} \quad (35)$$

In figure 6.4, the total power losses (35) has been plotted versus the active area for a diamond p-type FET (considering the losses only for the NPT drift region) switching 5 kV (with a BV=6.5 kV),10A at 20 kHz and at a duty cycle of 0.5 for a fixed operating temperature (T=300 K). The doping and drift region thickness are extracted in NPT conditions by solving the ionization integral with the coefficients from[161] (see also table 6.2).

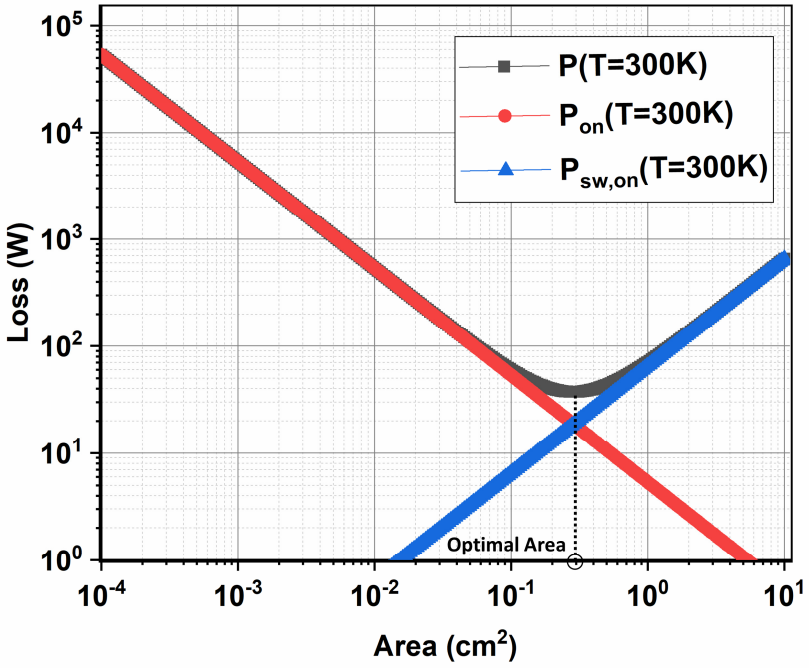


Figure 6.4: Conduction(red), switching(blue) and total (grey) power loss for a NPT diamond drift region switching 5 kV (with a BV=6.5 kV),10 A at 20 kHz and at a duty cycle of 0.5 at T=300 K. At the intersection point conduction and switching loss have an identical value.

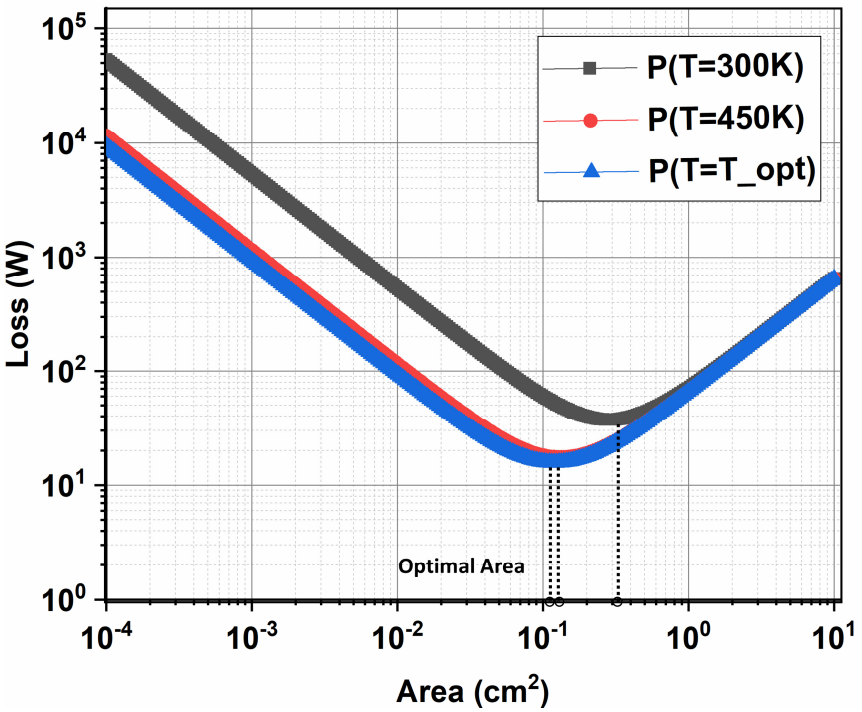


Figure 6.5: Total power loss for a NPT diamond drift region switching 5kV (with a BV=6.5 kV),10 A at 20 kHz and at a duty cycle of 0.5 at T=300 K ,T=450 K and T_opt(~540 K see figure 6.2).

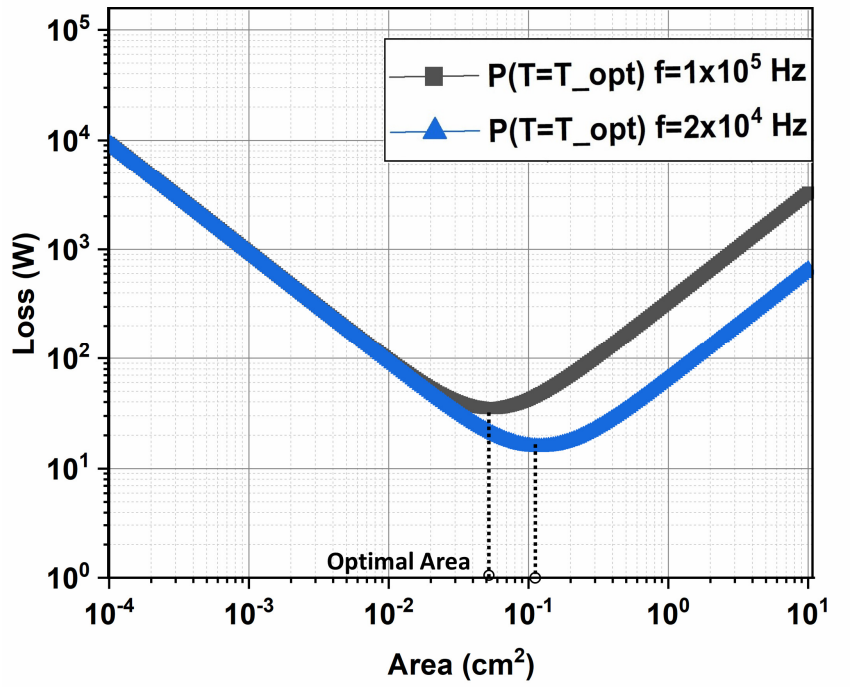


Figure 6.6: Total power loss for a NPT diamond drift region switching 5 kV (with a BV=6.5 kV),10 A at f=20 kHz and f=100 kHz and at a duty cycle of 0.5 at T=300 K.

As it can be noted from figure 6.4, an optimal active area, which arises from the different trends for switching losses and ON state losses, can be identified (at the

intersection between the two curves). At the optimal active area, both the conduction, switching and total loss can be extracted.

Moreover, the current and power loss density can be obtained by dividing the total current and loss with the optimized active area. These results have been reported in table 6.1. Figure 6.5-6.6 report the optimization of the total loss for different operating temperature and for high switching frequency (100 kHz). Higher temperature is beneficial in terms of reduction of the optimal area and total power loss. This peculiar trend is due to the decrease of the R_{on_spec} due to the incomplete ionization effect.

Conversely, as it can be seen in figure 6.6 (and table 6.1), high switching frequency (100 kHz) will increase the total power density and total loss values. These values can possibly overcome the limits imposed by the maximum system specifications and, more in general, will put a higher constraint on the thermal management. Increasing the diamond active area above the optimal area will increase the total loss (especially the switching loss), while slightly decreasing the power density (see table 1 the "not optimized" design). As reported in table 6.1, switching 5 kV (with a BV=6.5 kV),10 A at 100 kHz and at a duty cycle of 0.5 is extremely challenging in terms of power density loss (even at high operating temperature). The results shown in table 1 can be also visualized in a spider chart (see figure 6.7). Figure 6.7 shows a more global approach with a figure of comparison which allows to compare the performance of different diamond FETs designed for switching 5 kV (with a BV=6.5 kV),10 A and a duty cycle of 0.5. This spider graph also allows to compare different semiconductor-based FETs (see next paragraph and also [9]) for a specific application. The main parameter of this more global comparison is the total loss at the optimal active area, for a fixed set of specifications. The current rating or switching frequency can be de-rated as a function of the maximum allowed thermal power density, or a larger active area with larger total losses must be chosen to reduce the power density, if needed (as in the case of high switching frequency) and possible. For the heatsink volume (V) , natural convection is considered with a volumetric resistance (V_R) of 500 cm^3 °C/W[344] (equation 36). This value typically overestimates the heatsink volume, whereas forced air solutions can reduce the heatsink volume by a factor of 5 to 10.

$$V = V_R \times P/(T - T_{AMB}) \quad (36)$$

Table 6.1. Comparative study between different diamond designs for switching 10 A,5 kV with a duty cycle of 0.5.

5000V (BV 6500V) 10A 0.5 duty cycle		Diamond 20kHz T=300K	Diamond 20kHz T=450K	Diamond 100kHz T=300K	Diamond 100kHz T=450K	Diamond 100kHz T=450K (Not optimized)
Optimal Area	cm^2	0.29	0.13	0.13	0.06	0.30
Conduction Loss	W	18.72	8.70	41.36	19.45	3.84
Switching loss	W	18.72	8.70	41.36	19.45	98.4
Total loss	W	37.45	17.4	83.73	38.90	102.24
Junction Temperature	K	300	450	300	450	450
Current density	A/cm^2	34.48	76.92	76.92	166.67	33.33
Power loss density	W/cm^2	129.14	133.84	644.07	648.33	340
Heatsink Volume	cm^3	---------	58	----------	130	340

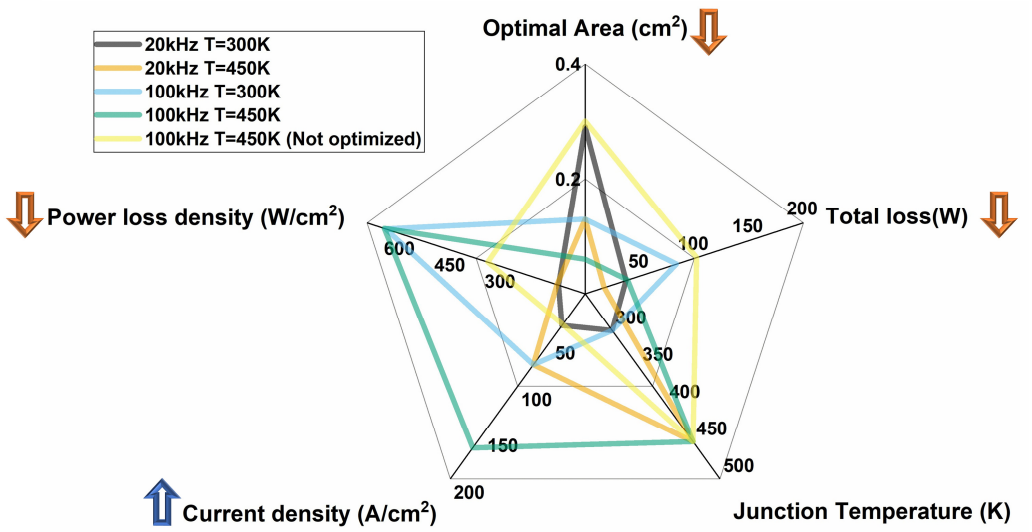


Figure 6.7: Spider chart highlighting the approach to compare the performance of different diamond designs (in terms of active area, switching frequency, junction temperature) for switching 5 kV,10 A with a duty cycle of 0.5. In the spider chart, for a fixed junction temperature, the optimal area, the total loss and the power loss density should be kept as small as possible while the current density should be as high as possible. Heatsink volume could be added in the spider chart (as shown in fig. 6.11)

However, this assumption will allow a quantitative benchmark on diamond devices versus other materials such as GaN and SiC power devices. The ambient temperature (T_{AMB}) will be set to 300K.

6.2.4. Benchmarking of Diamond devices against 4H-SiC and GaN: the 6.5 kV case

In this paragraph, we will compare the specific ON state resistance, total semiconductor losses, junction temperature, heatsink volume, semiconductor active area, current density and power loss density of bulk Diamond devices against vertical GaN on GaN and 4H-SiC power devices. A single case study will be considered for 6.5 kV rated breakdown and the method illustrated in the previous section will be employed. The same procedure can be applied for a different voltage rating. In this comparative analysis, only unipolar devices will be considered. For this study, the switching loss model has been set as the energy loss in the non-linear drift region parasitic capacitor, as introduced in previous paragraph. For the 6.5 kV devices, the switched voltage and current are 5 kV and 10 A, respectively. Duty cycle and switched frequency are fixed at 0.5 and 20 kHz and the study is conducted at both room temperature and at high temperature (T=450 K).

The models and basic assumptions for diamond devices are based on those used in the previous paragraphs, including incomplete Boron ionization, simplified switching loss model, NPT drift region, doping and temperature dependent mobility, impact ionization coefficients for breakdown voltage.

Regarding 4H-SiC and vertical GaN the same assumptions have been considered with the exclusion of the incomplete ionization (i.e. n-type drift region GaN region and 4H-SiC doped region have been assumed). The parameters for the non-punch-through drift region design of GaN and SiC have been summarized in the table 6.2. The state-of-the-art impact ionization coefficients [316, 345] has been assumed for the calculation of the ionization integral and the temperature-doping dependent mobility models [150, 346, 347] are assumed for the calculation of the R_{on_spec}.

The parasitic output capacitor (Coss) and the ON state resistance are assumed to be due only to the drift region.

Table 6.2. Device parameters used for the 6.5kV comparison. The parameters for bulk diamond are the same assumed in the previous paragraph.

6.5kV (NPT design)	Drift region Thickness	Drift region doping	Max. Electric Field	R_{on_spec} (300K)	R_{on_spec} (450K)
Bulk Diamond P-type	28.2µm	$4.95x10^{15}cm^{-3}$	4.6MV/cm	107mOhm.cm²	23.1mOhm.cm²
Bulk GaN on GaN N-type	59.5µm	$1.83\ x10^{15}cm^{-3}$	2.18MV/cm	10.2mOhm.cm²	44.8mOhm.cm²
4H SiC N-type	57µm	$2.18\ x10^{15}cm^{-3}$	2.28MV/cm	14.7mOhm.cm²	37.5mOhm.cm²

The comparison is presented in table 6.3 and figure 6.8-6.11. Key elements can be highlighted:

- At room temperature both vertical GaN and 4H-SiC outperform diamond devices in terms of total loss (reduction of ~73% and ~65% respectively).

Furthermore, the achievable current density at T=300K is much higher for GaN and 4H-SiC if compared with diamond and the required (optimal) active area is reduced by ~35% with GaN and ~59% with 4H-SiC. As it can be noted, GaN outperforms SiC at room temperature.

- At T=450K, the boron activation allows to reduce the conduction loss and diamond becomes advantageous.

Compared to 4H-SiC a reduction of ~28% for the active area and ~17% of saving in terms of power loss can be achieved. Moreover, the heatsink volume of a diamond FET can be reduced by ~17%. At this operating temperature, 4H-SiC outperforms vertical GaN FET. This is due to the significant mobility reduction of GaN at high temperature.

The results highlighted in this section clearly point out that the lack of a shallow dopant (both p-type and n-type) is the main reason behind the poor performance of diamond FET at RT. High operating temperature can reduce the switching loss but results in lower carrier mobility.

This effect does not allow the HT diamond p-type FET' performance (for the 6.5 kV target) to beat the RT performance of competitors semiconductors FETs (GaN and SiC).

Table 6.3. Comparative case study between GaN on GaN and 4H-SiC for the same specifications. The relative parameters for diamond can be found in table 1. The calculated heatsink volume for diamond at T=450K is 57.99cm^{-3}.

5000V (BV 6500V) 10A 0.5 duty cycle		**GaN vertical 20kHz T=300K**	**GaN vertical 20kHz T=450K**	**4H-SiC vertical 20kHz T=300K**	**4H-SiC vertical 20kHz T=450K**
Optimal Area	cm²	0.10	0.21	0.12	0.18
Conduction Loss	W	5.10	10.68	6.54	10.42
Switching loss	W	5.10	10.68	6.54	10.42
Total loss	W	10.21	21.36	13.07	20.85
Junction Temperature	K	300	450	300	450
Current density	A/cm²	101	47.61	83.3	55.5
Power loss density	W/cm²	103.1	101.71	108.92	115.83
Heatsink Volume	cm^3	---------	71.21	----------	69.5

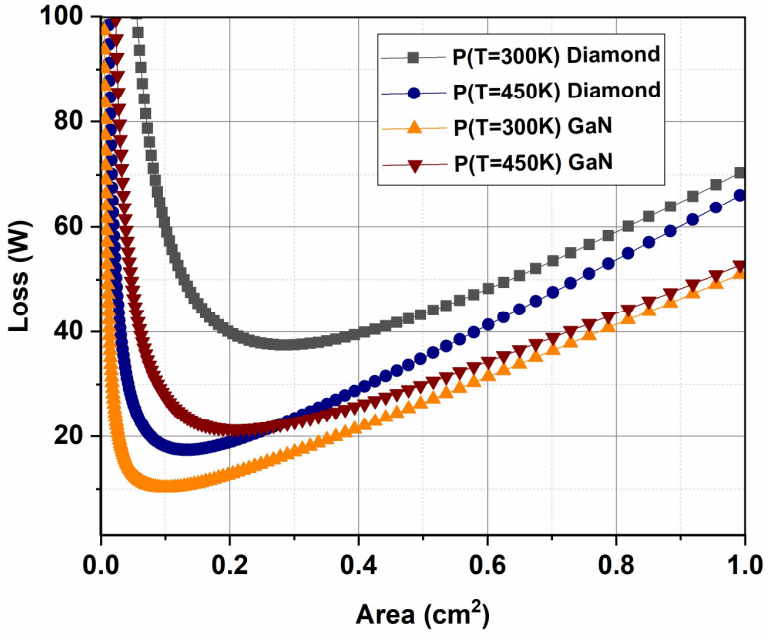


Figure 6.8: Semiconductor loss as function of the active area for diamond and vertical GaN FETs for switching 10 A at 5 kV (BV=6.5 kV) with a duty cycle of 0.5 at f=20 kHz for T=300 K/450 K.

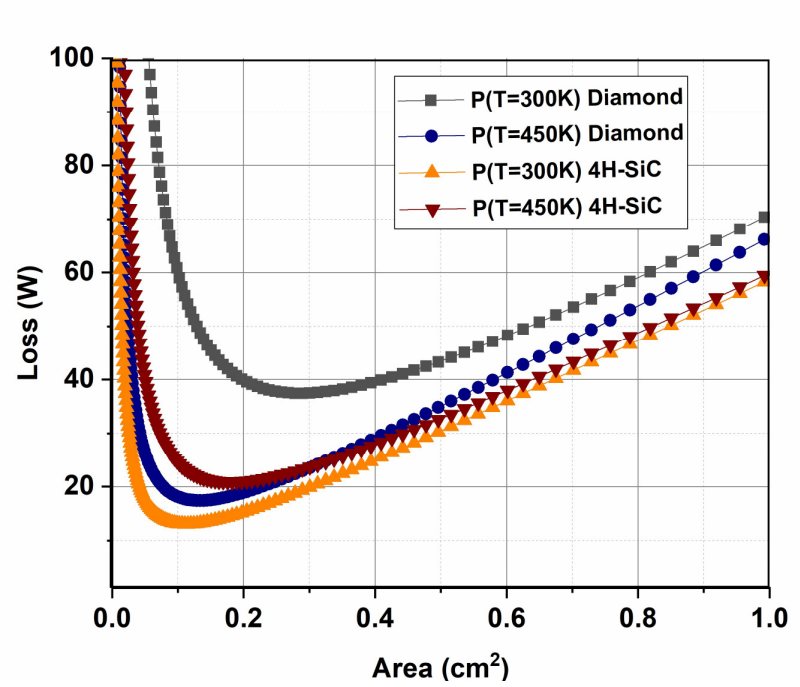


Figure 6.9: Semiconductor loss as function of the active area for diamond and vertical 4H-SiC FETs for switching 10 A at 5 kV (BV=6.5 kV) with a duty cycle of 0.5 at f=20 kHz for T=300 K/450 K.

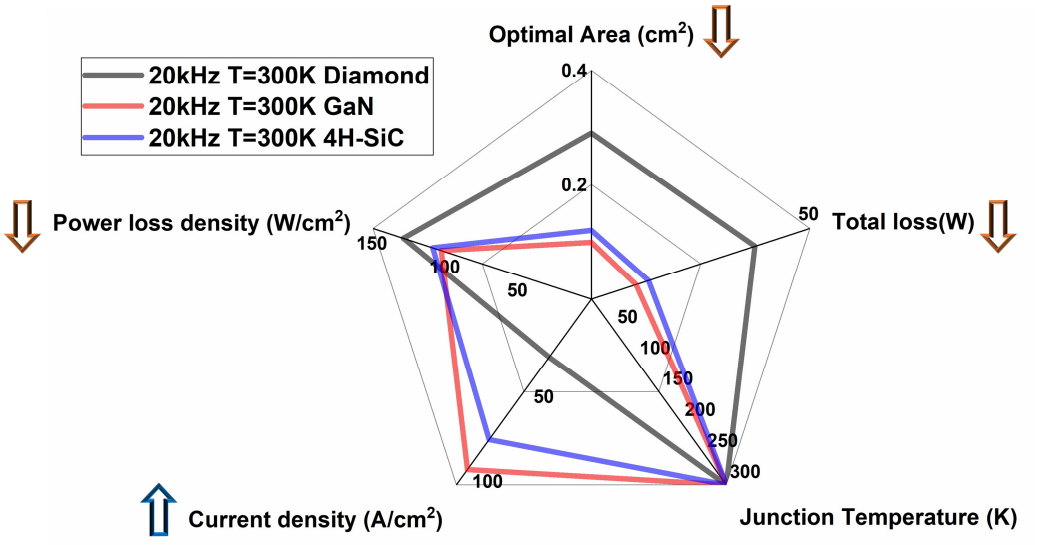


Figure 6.10: RT comparison of diamond, GaN and 4H-SiC vertical FETs switching 5 kV,10 A with a duty cycle of 0.5 at f=20 kHz.

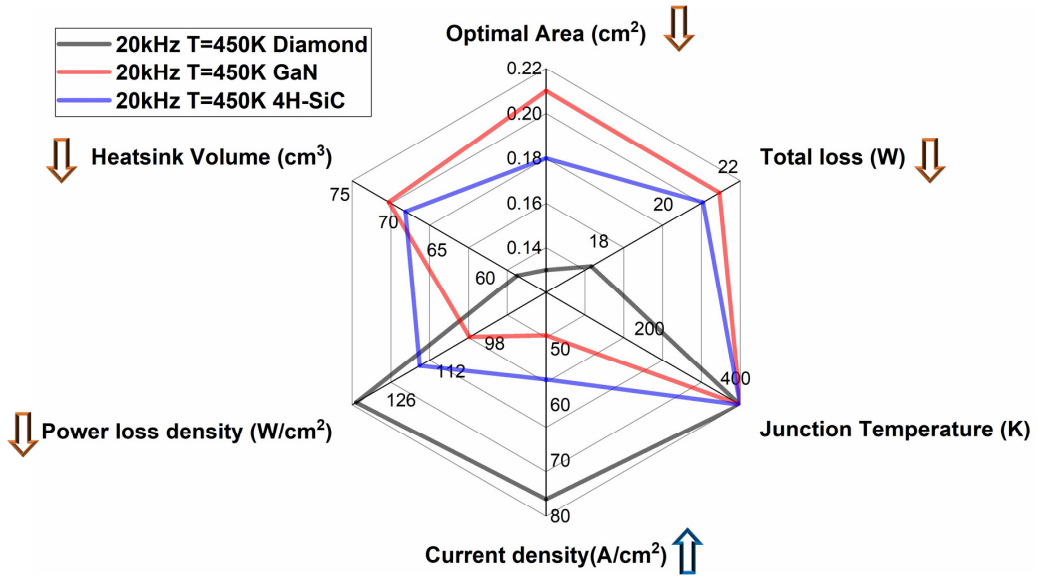


Figure 6.11: Comparison of diamond, GaN and 4H-SiC vertical FETs switching 5 kV,10 A with a duty cycle of 0.5 at f=20 kHz at T=450 K.

6.3 Unipolar vs Bipolar diamond diodes

Although the selection of the most appropriate p-type diamond FET is still a subject of discussions and would typically depend upon the converter class, the system specifications, etc., some simplified assumptions can be made for a useful benchmark of diamond diodes.

With many factors impacting on the electro-thermal performance (i.e. package, cost of the chip, power efficiency, switching frequency, etc.) and different physical mechanisms involved in the electron-hole current transport, the optimal choice between unipolar and bipolar devices for power electronics' applications needs be carefully carried out [27, 348]. One of the most accurate approaches to follow is the one described by Morisette et al. [27] for SiC diodes. This optimization is principally based on maximizing the available current density at a fixed breakdown voltage and switching frequency for a bipolar PIN diode and Schottky barrier diode. If one assumes that the package and the cooling system cost between the two devices can be assumed identical, the only significant cost' difference is linked to the die. Therefore, higher current densities will allow for a reduced die area (for a fixed ON state current) and lower cost for that specific device.

Applying a similar procedure to the specific case of diamond, it is possible to compare PIN diodes and Schottky (figure 6.12) for different switching frequencies, BV rating and temperature.

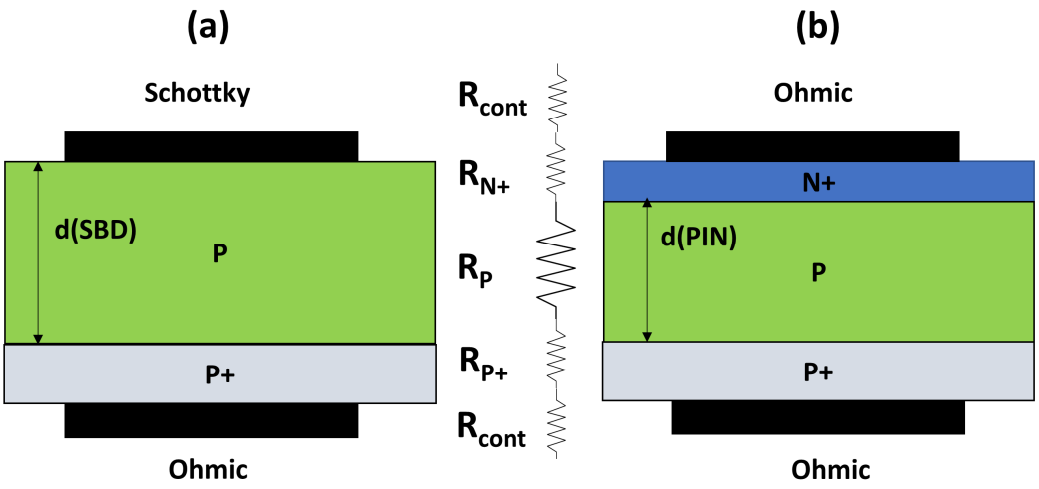


Figure 6.12: (a) Schottky diode and (b) PIN diode considered in the analysis. The resistance of the contact (R_{cont}), N+ and P+ type layers is neglected in this study (R_{N+},R_{P+}). The doping of the N+ and P+ region is assumed to be 10^{20} cm^{-3} (i.e. the incomplete ionization of these layers can be neglected). A p-type (boron doped) drift layer has been considered for this study. Regarding the Schottky diodes, the p-type layer exhibits a lower resistivity if compared with an n-type diamond layer. It should be noted that while n-type drift regions could still be theoretically used in PIN diodes, the state-of-the-art n-type diamond layers have higher defects densities and, possibly, shorter minority carrier lifetime which leads to lower bipolar carrier injection.

In the analysis presented in this paragraph, a simple inductive load switching circuit is considered and the energy dissipated by the main switch (a FET like a MOSFET or an IGBT) is assumed to be directly based on the charge stored in the diode.

Under these assumptions, the static (P_{static}) and dynamic ($P_{dynamic}$) power density components for a power diode can be written as shown in equation (37) and (38)[3]:

$$P_{static} = J_F V_F \delta + J_R V_R (1 - \delta) \quad (37)$$

$$P_{dynamic} = f(E_{on} + E_{off}) \quad (38)$$

Where J_F is the current density in the ON state, V_F is the forward voltage drop, $\boldsymbol{\delta}$ is the duty cycle (assumed equal to 0.5 in this study), J_R is the reverse current density, V_R is the reverse voltage (assumed equal to the BV in this simplified analysis), f is the switching frequency, and E_{on} and E_{off} are the energies loss densities by the diode during the turn ON and turn OFF transient of the diode. In addition, V_F can be expressed as the sum of the built-in voltage (V_{bi}) and the specific ON state resistance of the diode (R_P) multiplied by the forward current density for the PIN diode. In the equation (39), the built-in voltage (V_{bi}) is function of the bandgap(E_G), the impurity concentration of the P, P+ and N+ type layers, the density of states in the valence and conduction band (Nv and Nc) and the operating temperature(T)[152]. A different (but similar) expression holds for SBDs, as shown in (40)[93, 152]. In (40), n is the ideality factor of the diode (here assumed equal to 1), V_{bn} is the barrier height between the p-type semiconductor and the Schottky metal, k is the Boltzmann constant, q the electron charge, A* the Richardson constant (assumed equal to 88 A/cm^{2}K^2 [93, 181]).

$$V_{F(PIN)} = J_F R_P(PIN) + V_{bi}(T, N) \quad (39)$$

$$V_{F(SBD)} = J_F R_P(SBD) + nV_{bn}(T, N) + \frac{nkT}{q} \ln\left(\frac{J_F}{A^* T^2}\right) = J_F R_P(SBD) + V_{bi}(SBD) \quad (40)$$

Regarding the specific ON state resistance of the p region for the Schottky Barrier diode (SBD), the absence of minority carriers results in the expression (41) - where p is the active carrier concentration calculated by means of the incomplete ionization formula at different P-doping(N_P) and junction temperatures(T), μ_p is the mobility for p-type diamond which is assumed to be both doping and temperature dependent and d(SBD) is the optimal punch-through thickness calculated for a specific reverse voltage target by means of the procedure described in [269].

$$R_p(SBD) = \frac{d(SBD)}{qp\mu_p} \quad (41)$$

Regarding the bipolar PIN diode, the specific ON state resistance can be expressed as in (42):

$$R_p(PIN) = \frac{d(PIN)}{qpu_p + \frac{(\mu_p+\mu_n)J_F\tau}{d(PIN)}} \quad (42)$$

where d(PIN) is the optimum drift layer thickness, q is the electron charge, μ_n is the electron mobility in the p-type layer and τ is the ambipolar lifetime.

Unlike in the SBD, the best set of coefficients (d(PIN), N_P) cannot be obtained with a closed form optimization and an iterative technique by means of TCAD simulations is therefore needed. For the purpose of this study, d(PIN) has been calculated by solving the ionization integral with the coefficients from [161, 162] and extracting the minimum thickness which gives a specific BV for a fixed N_P concentration of $5x10^{14}cm^{-3}$. This choice of the doping concentration has been carried out to allow a good level of conductivity modulation in the p-type layer. Besides, the chosen doping is not far from the minimum achievable with the current technique.

With the previous assumptions in mind, the charge density stored in the PIN diode (Qs) can be expressed as the product $J_F * \tau$ and the energy density associated with the reverse recovery of the PIN diode during the turn OFF can be expressed by (43):

$$E_{off}(PIN) = \tau J_F V_R \quad (43)$$

For the purpose of this study, E_{on}, which is the energy dissipated by the diode during its turn ON, has been neglected for both the Schottky and the PIN diode. Furthermore, the E_{off} component of the diamond SBD has been neglected as no significant stored charge needs to be removed from the p-type layer, which is only composed of majority carriers (holes in this specific example). Nonetheless, high switching frequencies (>100 kHz) could have an impact on the dynamic power dissipations with the flow of the displacement current in the diode. This component (P_{disp}) has been taken into account for both devices, as shown in equation (44) where ε is the dielectric permittivity of diamond which has been assumed frequency independent.

$$P_{disp} = \frac{f}{3}\sqrt{\frac{\varepsilon q N_P}{2}}(V_F + V_R)^{\frac{3}{2}} \quad (44)$$

Bearing in mind all the previous assumptions, the total power dissipation (static and dynamic) for both devices can be expressed as in (45) and (46):

$$P_{(SBD)} = (J_F V_{bi}(SBD) + J_F^2 R_p(SBD)\,)\,\delta + J_R V_R(1-\delta) + P_{disp}(SBD) \quad (45)$$

$$P_{(PIN)} = (J_F V_{bi}(PIN) + J_F^2 R_p(PIN)\,)\,\delta + J_R V_R(1-\delta) + f\tau J_F V_R + P_{disp}(PIN) \quad (46)$$

For the purpose of this study, the component J_R has been neglected in both formulas. In detail, for the PIN diode, J_R is mainly due to thermal generation-recombination process and can be ignored if one assumes a good quality of the material (low leakage current due to dislocations and defects). Regarding the SBD, such a component of the leakage current needs to be carefully considered as it can be significant for high electric field due to the thermionic field emission process. For the purpose of this study, the maximum level of the leakage current for SBD has been fixed at 1 μA/cm^2 and the optimal V_{bn} has been extracted using the procedure illustrated in [93] at different operating temperatures. The optimal V_{bn} allows to minimize the ON state voltage drop and at the same time to maintain the desired leakage current density value for a specific reverse voltage (V_R). Moreover, the ambipolar lifetime value τ has been optimized in order to minimize the power density expressed in (46) by setting the first derivative of $P_{(PIN)}$ equal to zero (figures 6.13, 6.14, 6.15).

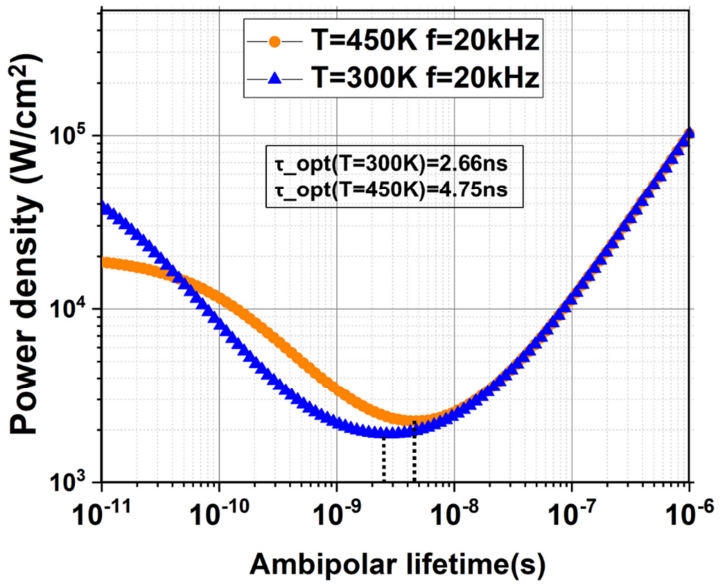


Figure 6.13: Power density vs ambipolar lifetime for PIN diode plotted with formula (46). For the plot it has been assumed a BV=10 kV, f=20 kHz and constant J_F of 500 A/cm^2.

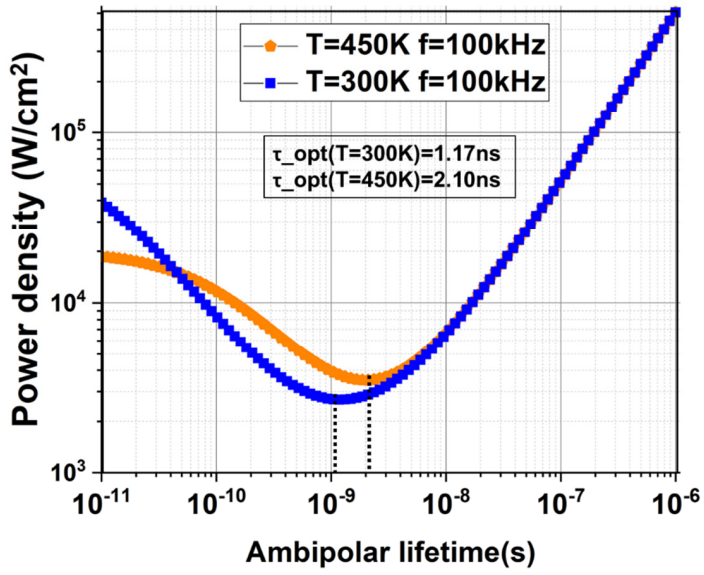


Figure 6.14: Power density vs ambipolar lifetime for PIN diode plotted with formula (46). For the plot it has been assumed a BV=10 kV, f=100 kHz and constant J_F of 500 A/cm^2.

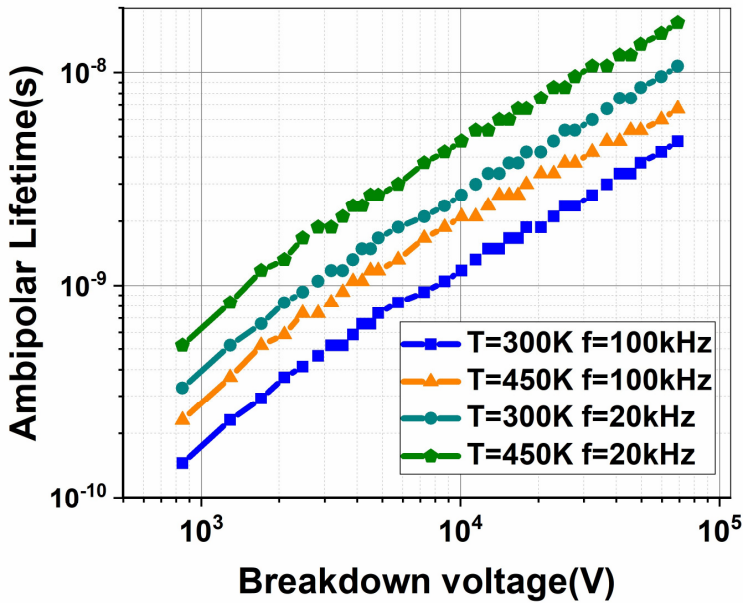


Figure 6.15: Optimal ambipolar lifetime(τ) as function of two different junction temperatures (300 K and 450 K) at f=20/100 kHz. For increased temperature and with the R_p(PIN) calculated by means of formula (42), τ increases. This is caused by the low acceptor concentration adopted for the drift layer (5x10^{14} cm^{-3}) in which the increase of the carrier activation with the temperature does not counterbalance the reduction of the electron/hole mobility (in contrast with the SBD behaviour, formula (41)).It is worth mentioning that high temperature may result in increased injection levels from the n+ and p+ region. Such a component has been neglected in a first order approximation.

The optimal value of the lifetime (τ_opt) emerges from the trade-off between the static power dissipation which is reduced for high values of lifetime thanks to the

conductivity modulation effect and the increased dynamic power dissipation which increases for larger stored charge (Qs).

Once the set of optimal parameters has been extracted, the procedure can be concluded by fixing a value for the maximum power density and by maximizing the J_F for each device by using formulas (45) and (46). The value of the maximum allowable power density typically depends upon the package capability (especially on the thermal spreader design) and it oscillates between 50-300 W/cm^2 for commercial devices. In this paragraph, this value has been chosen to be 500 W/cm^2, a value which is justified by the increased thermal capability of diamond devices.

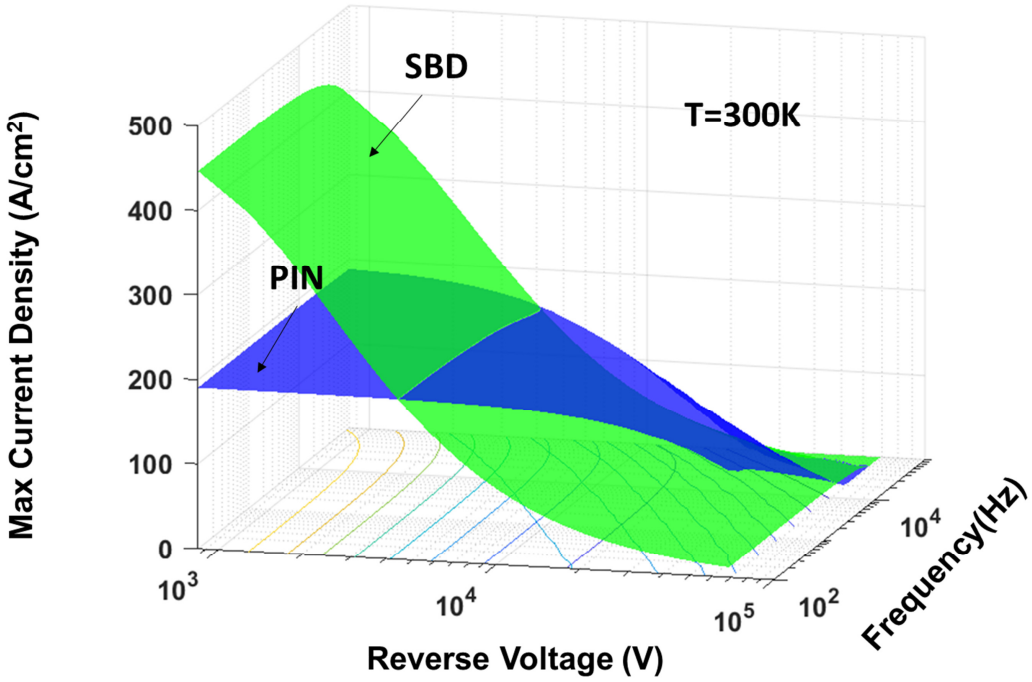


Figure 6.16: 3D plot of the frequency vs voltage vs current domain for a fixed junction temperature for the SBD and the PIN diode obtained with equations (45) and (46).

As one can note from the 3D plot in figure 6.16, with the inclusion of the displacement current, that both the PIN and the SBD exhibit a reduction in the maximum current density at higher switching frequencies. At RT and for low breakdown voltage (<4 kV), the current density for SBDs is higher than PIN diode and the SBD is the preferred device for the whole range of frequencies (figure 6.17).

As the BV increases, the trend changes and the “optimized” conductivity modulation occurring in the PIN diode allows for reduced power losses compared to the Schottky

diodes for a wide range of operating frequencies. For ultra-high BV (>20 kV) and for switching frequencies >10 kHz, the SBD becomes again superior to the PIN diode.

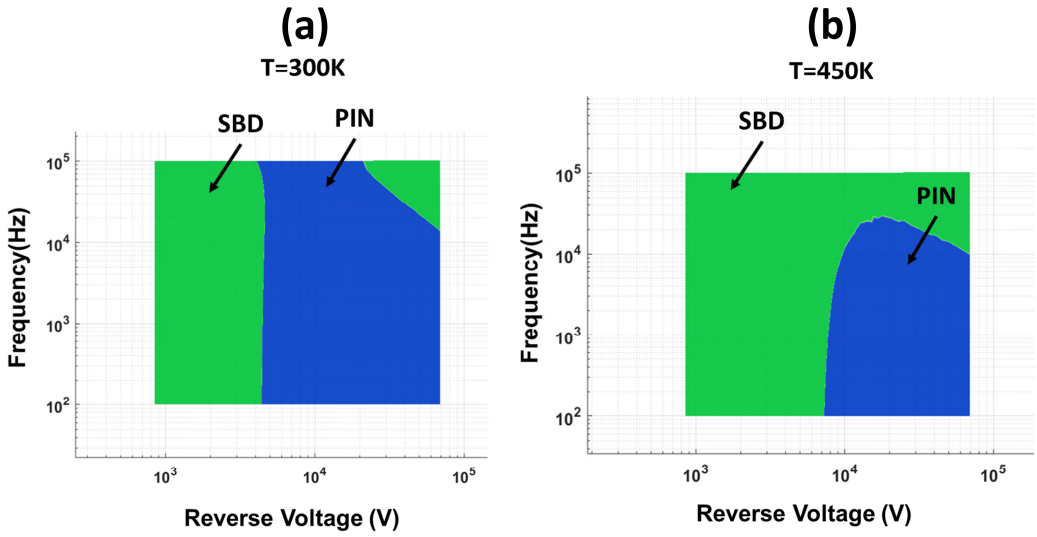


Figure 6.17: 2D top view of figure 38 of the frequency vs reverse voltage domain for two different operating junction temperatures (T=300/450K). The areas in green are the ones where the SBD is a better choice that the PIN diode due to the higher current density which will allow for a reduced die area.

At higher junction temperature (T=450 K) the trade-off between the two devices is modified due to the dependence of the leakage current upon the temperature, the carrier activation, the carrier mobility, density of states etc. which modify the set of optimal parameters for the analysis. The voltage vs frequency area in which the SBD displays higher current density compared to the SBD is widened and the PIN diode becomes a better choice only for reverse voltage >7 kV and f<10 kHz. At ultra-high voltages (>10 kV) and high frequency (>20 kHz), the lower SBD dynamic power dissipations makes this device again a better solution compared to the PIN.

6.4 System level benefits and challenges

P-type transistors and diodes are the most promising diamond devices for future commercialization. Precisely, the absence of high-performance p-type FETs in the existing power electronics market could open a specific opportunity for diamond. As an example, the smart integration of diamond FETs with other FETs based on GaN, β-Ga_2O_3, AlN and 4H-SiC could represent an innovative solution to simultaneously

simplify the complexity of the gate driving circuit and reduce the parasitics due to the interconnections [9, 108].

However, there exists some challenges for diamond before this material can meet commercial expectations.

Despite the fact that diamond devices would have lower total losses than other semiconductors, the power density losses are increased. Consequently, there is a higher stress on thermal spreader, accentuated by the higher junction temperatures of diamond devices. The system level benefits and challenges of diamond devices can be summarized as follow:

Benefits

- Reduced total semiconductor losses thanks to lower ON-state losses.
- Increased switching frequency thanks to smaller active areas and very fast switching. Therefore, the volume and weight of passive elements used in filters can be reduced.
- Higher junction temperatures, leading to smaller and lighter heatsinks or moving from liquid cooling to forced air or even natural convection.

Challenges

- Higher power loss density, requiring efficient thermal spreaders and thermal interfaces (i.e. complex thermal management).
- Reduced maximum diamond device area.
- Efficient device parallelization.
- Reliability and reproducible performance.

6.5 Power converters with diamond devices

Diamond devices are usually small in size and therefore can conduct only low currents. From this perspective, parallelization becomes an essential technique for increasing the current flowing through diamond devices.

Examples of diamond diode parallelization in a buck dc/dc converter have already been studied in the literature. In [71], the diamond pseudo-vertical Schottky diodes

were connected to a common anode and had isolated cathodes. A high side commercially available Si MOSFET was implemented in the experimental setup for the double pulse test in order to match the requirement of current/voltage of the diodes under test. The presence of the Si MOSFET limited the maximum switching speed of the system together with the parasitics (i.e. capacitances and stray inductances). However, it is critical to have similar output capacitors between the high side device (Silicon transistor) and the low side device (diamond Schottky diodes in parallel). Coupling parallel diamond devices with high breakdown voltage (>100 V or >1 kV) and a very low current capability (<1 mA) on the high side with other power devices made of silicon, SiC or GaN on the low side while maintaining similar output capacitors is very challenging. In [60], a high switching speed was observed (tens of V/ns) with reduced oscillations mainly due to the low value of the switching current and significantly high on-state resistances. Such a parallelization of diamond devices was also analysed for an interleaved configuration which eased the increase of switching frequency with benefits related to the output filter design and control bandwidth (figure 6.18). The interference between the diamond diodes integrated on the same chip highlighted the importance of device isolation.

The interleaved setup may represent a promising configuration for the next generation of diamond converters with the on-chip integration of parallel p-type FETs on the same substrate. Besides, asynchronous DC/DC buck converter could benefit with the addition of a diamond p-channel FET due to the simplified gate driving technique (for the high side switch). However, imbalances between the different devices may impact negatively on the overall speed and current of the final converter, as already pointed out for diamond SBDs [337].

Bridge converters with an integrated diamond solution would ideally require n-type FETs to simplify the gate driving technique. Nonetheless, a smart on-chip integration of a gate driver for the low side p-type diamond FETs could partially solve the issue arising from the absence of n-type diamond FETs. Finally, isolated p-type diamond converters made with only p-type FETs and diodes could offer a different solution to tackle the gate driving' issues of bridge configurations and other converters' typologies.

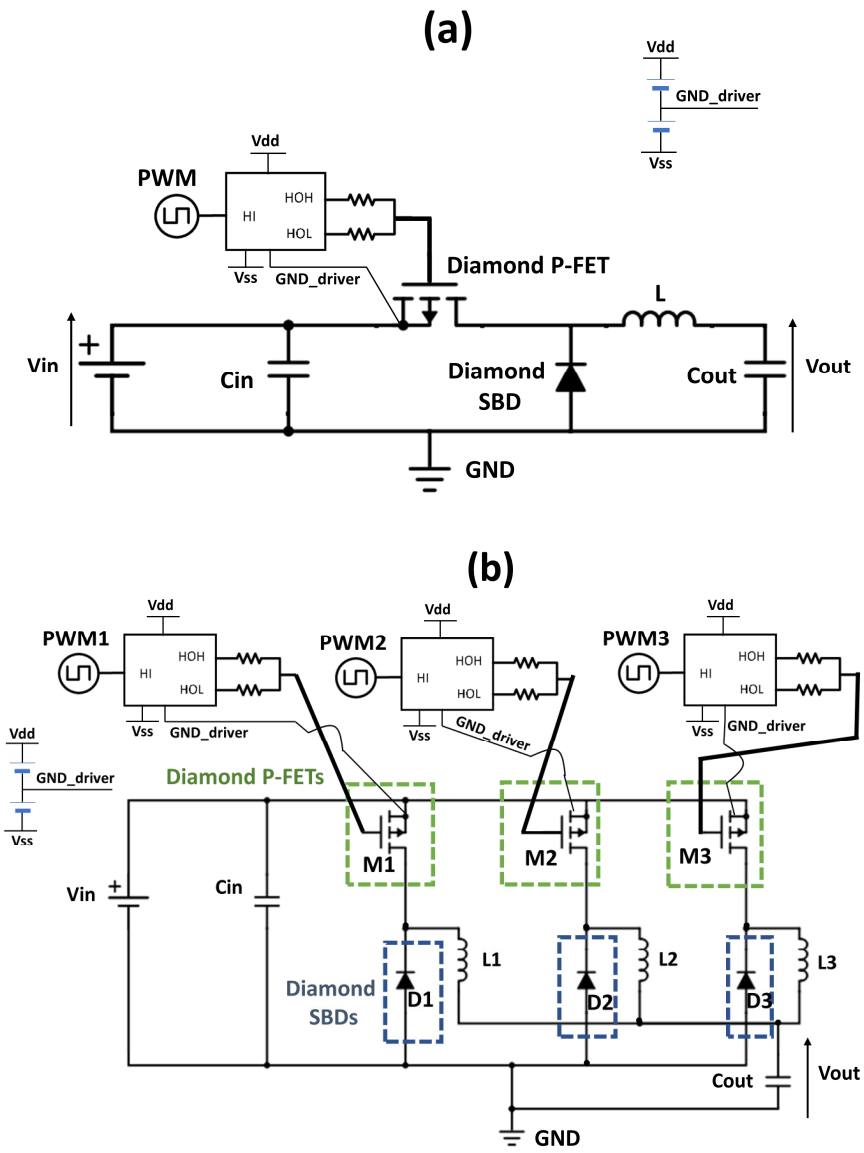


Figure 6.18: Schematic of (a) DC/DC buck converter and(b) interleaved converted with diamond p-type FETs and Schottky diodes. Depending on the switch, Vss can be positive and Vdd can be negative. 3 separate gate drivers have been represented for the interleaved converter in figure (b). Alternatively, a single gate driver with separate inputs and outputs and one GND driver can be implemented.

6.6 Future perspectives and roadmap of diamond power devices

This section aims at summarising the main challenges for the success of diamond in the power device field. These challenges can be organised in five categories: (i) material, (ii) devices, (iii) packaging, (iv) reliability, and (v) integration, as shown in table 6.4.

Table 6.4. Current status and challenges for diamond devices in power electronics.

	Challenge	Current Status	Breakthroughs and future prospective
Material	Wafer size	< 1 inch	> 2 inches
	Cost	> 400$ per <1inch wafer	Dependent on the BV (see discussion below (i)).
	Defects	High dislocation density	Lower dislocation density for increasing wafer size
	Interface quality	Medium-High interface states and defects density compared to Si devices.	Optimized annealing techniques for improving the quality.
	Doping	p-type with Boron (deep acceptor level), lack of reliable n-type.	Lower activation energy dopant species, new conduction mechanisms.
Devices	High BV and current FETs	~2kV for lateral technologies.	>10kV, >10A for vertical technologies, high transconductance, low threshold voltage, low Ron_spec transistors.
	High Power p-type SBDs	>1kV, >5A	Improve the BV (field terminations, thick and high-quality drift region, etc.) without affecting the ON state current (target >10kV, >10A).
	N-type FET	Not available.	Development of techniques for low resistive n-type layers.
	Leakage current	- Dominated by defects. - Limiting factor for high BV.	Improve material quality.
	Lifetime	<10ns	>100ns
	Termination	Not optimized and may lead to TDDB	New solution for high voltage passivation.
	Fast switching	Limited to diodes	>100V/ns
	Novel device structures	N/A	SuperJunctions, floating islands, new techniques.
Packaging	High temperature packaging	N/A	Unique packaging technique for high temperature operation (i.e. 175°C for 10kV, >200°C for 3kV).
	Ultra-high voltage packaging	N/A	New passivation methods, secondary passivation techniques, etc.
Reliability	Ageing	No ageing test have been conducted so far	Lifetime of diamond devices is still an open issue.
	Yield	N/A	Improve the repeatability and reproducibility of devices
	Harsh environment	Only few tests have been performed	Show suitability to harsh environments with more standard tests
	High switching	N/A	Resistance to high dI/dt and dV/dt. New switching model. EMI/EMC would need specific filters design.
Integration	Passive components	N/A	On-chip Integrated capacitors ,resistances, inductances to reduce parasitics.
	Active devices	Limited to logic devices	Isolated transistors and/or diodes
	Integrated gate driver	N/A	Smart gate driving for p-type FETs would improve the switching frequency.

(i) Material: the size of the diamond substrate is currently limited to <1 inch diameter due to the quality of the material. Only improvements in the HPHT and CVD techniques and the development of novel growth and doping methods would allow fabrication of large area wafers with higher current levels. The decrease in the defects and dislocation density together with the enhancement of the interface quality would also enable the reduction of leakage currents and achieve breakdown voltage levels closer to their theoretical predictions. The high-cost of the substrate is another crucial aspect to take into account for the commercialisation of diamond power devices. In this context, the reduction of the specific ON state resistance more than the decrease of the total cost and the increase of the total area of each diamond wafer, appears to be the best strategy to enable the commercialization of diamond.

(ii) Devices: Technological progress in the wafer and processing quality will also have to focus on four key aspects related to device technology and performance: (a) the development of vertical devices and novel structures, (b) carrier lifetime control, (c) device termination optimisation which could benefit from the fabrication of multi-layer passivation based on high-k materials, and (d) enhanced slew rate. Switching speeds above 200 V/ns, (not possible in silicon), have already been demonstrated for GaN devices. By efficiently tackling the carrier dynamics due to the incomplete ionization of the dopant species, diamond promises to deliver even faster slew rates at the device level. In addition, the demonstration of a high-performance diamond n-type FET would also lead to smart integration of a key components, such as protection, drive and possibly R,L,C passives within the same chip. Further developments will be required especially for diamond FETs, which do not deliver the same performance of diamond diodes.

(iii) Packaging: Packaging of diamond devices is an area where significant development will be required in particular to accommodate the very high slew rates or the operation in harsh environment applications. It is therefore apparent that unique packaging technique, not compatible with those available for other WBG materials, need to be put forward. Research on this topic is still at an early stage.

(iv) Reliability: As a further step towards the commercialization, diamond devices will need to pass reliability tests which can guarantee the guarantee the device performance over a specified time period and give an estimation of device lifetime in standard and harsh environment conditions. It is very likely that as the development of diamond-

based devices progresses, dedicated standards and reliability tests will be defined for diamond, following the same approach adopted for 4H-SiC and GaN for which dedicated JEDEC subcommittee have just been formed.

(v) Integration: Wafer integration of parasitic and smart gate driving circuits will enable low-volume diamond converters and improve dV/dt and the di/dt for the packaged devices. The smart integration of diamond and other WBG/UWBG semiconductors (figure 6.19) could represent one of the possible applications of diamond p-type FETs in a monolithic high-speed converter.

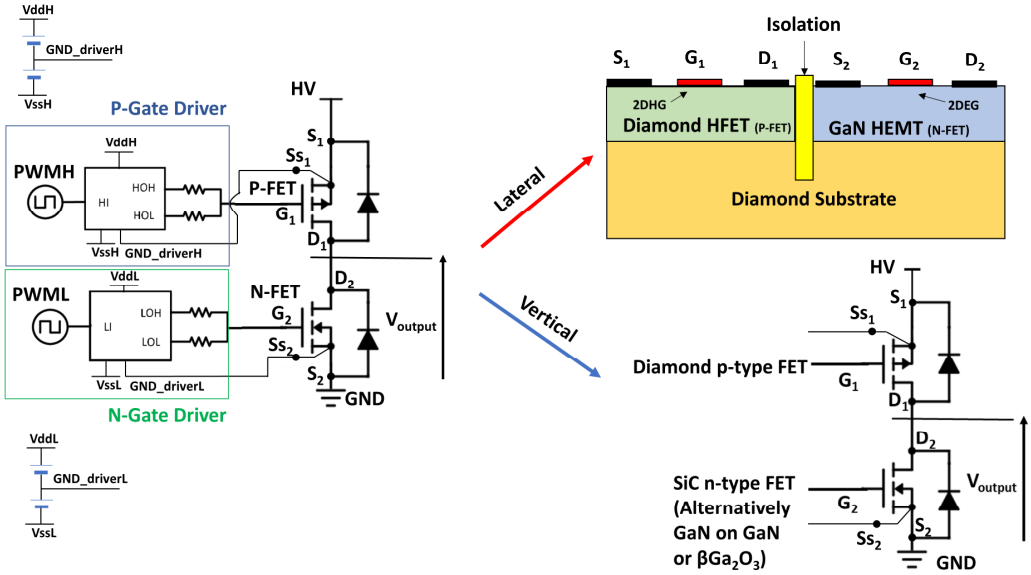


Figure 6.19: Schematic of a possible monolithic implementation of diamond and other WBG/UWBG semiconductors. The integration of diamond p-type FET and other n-type FET grown on the same diamond substrate allows for the reduction of parasitics and better thermal performance. (through the common diamond substrate). Kelvin sources have been added to both FETs in view of the fast switching speed achievable by using such a configuration.

6.7 Conclusions

A thorough comparison of boron doped diamond diodes and FETs against the state-of-the-art GaN and SiC devices has been carried out in this chapter. This analysis has clearly shown that p-type diamond FETs are able to outperform current WBG semiconductor FETs only for high operating temperature. Such a limitation is due to a fundamental limit of the incomplete ionization of the dopants. Alternative technologies, such as 2DHG based FETs, addressed in the last paragraph and in

previous chapters, may enable the full potential of diamond even at room temperature. Nevertheless, this improvement could only lead to commercial devices if reliability, reproducibility and also scalability of the devices are properly addressed. These issues will be further commented in the conclusions of this thesis.

7 CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

Remarkable advantages of diamond for power electronics have always been accompanied by many drawbacks and limiting factors. While some of the challenges which have hampered for years the development of this material have been recently addressed, other questions still remain unanswered. The main goal of the research carried out in this thesis has been to contribute to the understanding and the design of diamond devices for power electronic applications. State-of-the-art diamond power devices have been carefully reviewed and the power-frequency domain where the future generation diamond devices could compete against the current power device technologies has been identified. By means of finite element simulations carried out with Sentaurus TCAD (from Synopsys) and accurate theoretical analysis, optimized and novel device structures have been presented and studied in detail.

To sum up, the work presented in this manuscript can be summarized as follows:

- The unique material properties of diamond, the details of the state-of-the-art fabrication process and its related issues have been carefully examined. To be able to give a deep insight into the complex phenomena behind the behaviour of the diamond devices, an advanced TCAD model has been built based on experimental data found in literature. A complete description of the modelling of the main physical and electrical properties such as the electron-hole mobility, the surface termination, the impact ionization effect, etc. has also been provided.

- A systematic review of the state-of-the-art diamond power electronic devices with an accurate description of their main electrical performance has been carried out. The peculiar properties of vacuum switches and hydrogen terminated diamond FETs have been reviewed and their performance assessed against several other bulk diamond devices such as deep depletion MOSFETs, JFETs etc. The current state of diamond field relief termination has been analysed and the different techniques which help to avoid the premature breakdown voltage compared with each other.

- An optimization procedure for a normally-OFF diamond unipolar mode JFET has been presented. The limits and the issues arising from the incomplete ionization of the dopants have been carefully taken into account. It has been found that the parallel reduction of the built-in voltage and the effect of the partial ionization are the main limiting factors to achieve normally-OFF operation with diamond JFET at high junction temperature. An improved device structure which allows to reach low specific ON state resistance and, at the same time, high breakdown voltage has been designed by means of a design of experiments.

- The potential and the limitations of deep depletion diamond FETs have been carefully examined. A novel lateral normally-OFF diamond FET has been proposed and its performance simulated. By merging the diamond hydrogen FET concept and the deep depletion control of the channel, the proposed structure is capable to outperform the state-of-the-art WBG and diamond lateral FET for high temperature application with a significant enhancement in the threshold voltage control.

- Moreover, the physics and the equations governing the incomplete ionization effect of the dopants have been reviewed in detail. Static and dynamic consequences of the partial ionization have been carefully examined for superjunction based devices, MOS capacitors and p-n junctions. For the specific case of superjunction devices, charge imbalance effects due to the fast reverse dV/dt applied to the device have been extensively studied. Electro-thermal simulations have revealed that the local increase of the junction temperature can help the device to recover from the imbalance condition and that an accurate designed asymmetric SJ can favour such rebalancing mechanism.

- Diamond unipolar and bipolar mode diodes have been compared for a wide frequency-voltage range, showing that diamond bipolar PIN diodes are advantageous

for low-medium frequency and high voltage applications. A more global approach which allows to compare different diamond FET has been introduced. The results, which have been shown for a 6.5kV application, have clearly pointed out that bulk diamond FETs cannot overperform GaN and SiC devices at room temperature. This is a fundamental limit caused by the low free majority carrier concentration due to the partial ionization of the dopant species. Nevertheless, high temperature operation, which is beneficial for the carrier activation from deep dopant levels, shows enhanced performance for diamond bulk devices. This result emphasizes one of the peculiar findings of this study: diamond bulk FETs can only be competitive with other WBG semiconductor-technologies for harsh environment applications.

- In conclusion, a roadmap of diamond devices with the future perspective of this material has been presented. The possible implementation of p-type diamond FETs as high side switches in power converters would allow to simplify the driving scheme of for half and full bridge circuits. Furthermore, the necessity of improving reproducibility and reliability of diamond devices has been identified as the main challenge for the successful commercialization of diamond devices.

7.2 Future work

The work carried out in this thesis could be extended in several directions:

- The first direction is concerned with the dynamic ionization of the dopants. On one hand, experimental demonstrations of the imbalance effects occurring in WBG SJ devices would help to assess the real dV/dt and dI/dt resistance of this emerging class of power semiconductor devices. Such an experimental verification would only be possible when optimized SiC, GaN or diamond SJ based devices would be available. On the other hand, predicting the dynamic charge imbalance consequences on the device termination regions (i.e. with floating islands or junction termination techniques) could provide useful guidelines which will help to mitigate the drawback of the dynamic imbalance. This peculiar mechanism will need to be further investigated with more advanced electro-thermal simulations based on the hydrodynamic model.
- The second direction concerns the further development of lateral and vertical diamond FETs. The fabrication of the suggested hybrid configuration which

merges h-terminated and o-terminated diamond, vertical deep depletion or inversion MOSFETs,etc. could open a whole new scenario for diamond electronics showing the real potential of semiconducting-diamond for high-temperature and frequency applications. In addition, more advanced harsh environment experiments of diamond devices could provide useful information on the actual performance of diamond diodes and MOSFETs in environments where GaN and SiC devices still fail to deliver useful performance.

- Finally, with the increasing success of GaN on diamond technologies, the smart integration of diamond p-type FETs with GaN HEMT could represent a valid integrated alternative for half and full bridge configurations. Such a solution which should be firstly investigated and optimized with finite element analysis could lead to simplification of gate driving techniques, the reduction of parasitics and better thermal performance also for the GaN HEMT.

LIST OF PUBLICATIONS

Donato, N., Antoniou, M., Napoli, E., Amaratunga, G. and Udrea, F., 2015, October. On the models used for TCAD simulations of Diamond Schottky Barrier Diodes. In *2015 International Semiconductor Conference (CAS)* (pp. 223-226). IEEE., Sinaia (Romania), 12th-14th October 2015

Donato, N., Pagnano, D., Napoli, E., Longobardi, G. and Udrea, F., 2017. Design of a normally-off diamond JFET for high power integrated applications. *Diamond and Related Materials*, *78*, pp.73-82.

Loto, O., Florentin, M., Masante, C., **Donato, N**., Hicks, M.L., Pakpour-Tabrizi, A.C., Jackman, R.B., Zuerbig, V., Godignon, P., Eon, D. and Pernot, J., 2018. Gate Oxide Electrical Stability of p-type Diamond MOS Capacitors. *IEEE Transactions on Electron Devices*, *65*(8), pp.3361-3364.

Rouger, N., **Donato, N.** and Udrea, F., "Diamond devices in power converters: needs, constraints, and impact at system level", *Power Electronics Device Applications of Diamond Semiconductors*, pp.400-431, Woodhead Publishing Series:Cambridge, June 2018.

Donato, N. and Udrea, F., 2018. Static and dynamic effects of the incomplete ionization in SuperJunction devices. *IEEE Transactions on Electron Devices*, *65*(10), pp.4469-4475**.**

Donato, N., Rouger, N., Pernot, J., Longobardi, G., & Udrea, F. (October 2019). Diamond power devices: State of the art, modelling and figures of merit. Journal of Physics D: Applied Physics. (manuscript accepted on 17/10/2019)

BIBLIOGRAPHY

[1] I. M. P. S. I. Service. (2017). *Annual Power Semiconductor Market Share Report 2017 – The power semiconductor market recovered in 2016*. Available: https://technology.ihs.com/595076/annual-power-semiconductor-market-share-report-2017-the-power-semiconductor-market-recovered-in-2016, accessed on 31/10/2019.

[2] G. Deboy, M. Treu, O. Haeberlen, and D. Neumayr, "Si, SiC and GaN power devices: An unbiased view on key performance indicators," presented at the Electron Devices Meeting (IEDM), 2016 IEEE International, 2016, pp. pp.20.2.1-4, San Fransisco(USA), December 2016.

[3] B. J. Baliga, *Fundamentals of power semiconductor devices, Second edition*: Springer Nature: Gewerbestrasse 11, 6330 Cham, Switzerland, 2019.

[4] T. P. Chow, I. Omura, M. Higashiwaki, H. Kawarada, and V. Pala, "Smart Power Devices and ICs Using GaAs and Wide and Extreme Bandgap Semiconductors," *IEEE Transactions on Electron Devices,* vol. 64, pp. 856-873, 2017.

[5] S. Fujita, "Wide-bandgap semiconductor materials: For their full bloom," *Japanese Journal of Applied Physics,* vol. 54, p. 030101, 2015.

[6] J. Millan, P. Godignon, X. Perpina, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Transactions on Power Electronics,* vol. 29, pp. 2155-2163, 2014.

[7] L. Spaziani and L. Lu, "Silicon, GaN and SiC: There's room for all: An application space overview of device considerations," in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2018, pp. 8-11.

[8] E. A. Jones, F. F. Wang, and D. Costinett, "Review of commercial GaN power devices and GaN-based converter design challenges," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 4, pp. 707-719, 2016.

[9] N. Rouger, N. Donato, and F. Udrea, *Diamond devices in power converters: needs, constraints, and impact*: Woodhead Publishing Series: Cambridge (UK), June 2018.

[10] G. Longobardi, "GaN for power devices: Benefits, applications, and normally-off technologies," in *Semiconductor Conference (CAS), 2017 International, , Sinaia (Romania), 11th-14th October 2017*, pp. 11-18.

[11] N. Kaminski and O. Hilt, "SiC and GaN devices–wide bandgap is not all the same," *IET Circuits, Devices & Systems,* vol. 8, pp. 227-236, 2014.

[12] E. Gheeraert, "Power electronic devices performances based on diamond properties," *Power Electronics Device Applications of Diamond Semiconductors, Woodhead Publishing Series: Cambridge (UK),* pp. 191-200, 2018.

[13] S. Yang, S. Han, R. Li, and K. Sheng, "1 kV/1.3 mΩ· cm 2 vertical GaN-on-GaN Schottky barrier diodes with high switching performance," in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2018, pp. 272-275, IEEE, Chicago, May 2018.

[14] I. Abuishmais and T. M. Undeland, "SiC devices for renewable and high performance power conversion applications," *Advances in Power Electronics,* vol. vol. 2012, pp.1-5, 2012.

[15] A. Nakagawa, "Theoretical investigation of silicon limit characteristics of IGBT," presented at the Power Semiconductor Devices and IC's, 2006. ISPSD 2006. IEEE International Symposium on, 2006, pp. pp.1-4, Naples (Italy) 4-8 June 2006.

[16] H. Zhong, Y. C. Liang, G. S. Samudra, and X. Yang, "Practical superjunction MOSFET device performance under given process thermal cycles," *Semiconductor Science and Technology,* vol. 19, p. 987, 2004.

[17] N. Miura, K. Fujihira, Y. Nakao, T. Watanabe, Y. Tarui, S.-I. Kinouchi, M. Imaizumi, and T. Oomori, "Successful Development of 1.2 kV 4H-SiC MOSFETs with the Very Low On-Resistance of 5 m Ω cm2," presented at the 2006 IEEE International Symposium on Power Semiconductor Devices and IC's, 2006, pp. pp.1-4, Naples (Italy) 4-8 June 2006.

[18] Q. Zhang, J. Wang, C. Jonas, R. Callanan, J. J. Sumakeris, S.-H. Ryu, M. Das, A. Agarwal, J. Palmour, and A. Q. Huang, "Design and characterization of high-voltage 4H-SiC p-IGBTs," *IEEE Transactions on Electron Devices,* vol. 55, pp. 1912-1919, 2008.

[19] D. Sheridan, A. Ritenour, V. Bondarenko, P. Burks, and J. Casady, "Record 2.8 mΩ-cm 2 1.9 kV enhancement-mode SiC VJFETs," in *2009 21st International Symposium on Power Semiconductor Devices & IC's*, 2009, pp. 335-338.

[20] A. Traore, P. Muret, A. Fiori, D. Eon, E. Gheeraert, and J. Pernot, "Zr/oxidized diamond interface for high power Schottky diodes," *Applied Physics Letters,* vol. 104, p. 052105, 2014.

[21] Y. Kitabayashi, T. Kudo, H. Tsuboi, T. Yamada, D. Xu, M. Shibata, D. Matsumura, Y. Hayashi, M. Syamsul, and M. Inaba, "Normally-off C–H diamond MOSFETs with partial C–O channel achieving 2-kV breakdown voltage," *IEEE Electron Device Letters,* vol. 38, pp. 363-366, 2017.

[22] M. Holz, G. Hultsch, T. Scherg, and R. Rupp, "Reliability considerations for recent Infineon SiC diode releases," *Microelectronics Reliability,* vol. 47, pp. 1741-1745, 2007.

[23] Infineon, "IDH08G120C5," *5th Generation CoolSiC™ 1200 V SiC Schottky Diode,* [Datasheet] Rev. 2.1 2017-07-21, 2017.

[24] Rohm, "SiC Power devices," vol. vol.3, 2013), https://www.rohm.com/documents/11308/2420552/SiC_power_device-catalog.pdf, (accessed on 31/10/2019).

[25] G. Liu, B. R. Tuttle, and S. Dhar, "Silicon carbide: A unique platform for metal-oxide-semiconductor physics," *Applied Physics Reviews,* vol. 2, p. 021307, 2015.

[26] J. Hayes, W. A. Curbow, B. Sparkman, D. Martin, K. Olejniczak, A. Wijenayake, and T. McNutt, "Dynamic Characterization of Next Generation Medium Voltage (3.3 kV, 10 kV) Silicon Carbide Power Modules," presented at the PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of, 2017, pp. 1-7, May 16-18, 2017.

[27] D. T. Morisette and J. A. Cooper, "Theoretical comparison of SiC PiN and Schottky diodes based on power dissipation considerations," *IEEE Transactions on Electron Devices,* vol. 49, pp. 1657-1664, 2002.

[28] T. Tamaki, G. G. Walden, Y. Sui, and J. A. Cooper, "Optimization of on-state and switching performances for 15–20-kV 4H-SiC IGBTs," *IEEE Transactions on Electron Devices,* vol. 55, pp. 1920-1927, 2008.

[29] M. Marinella, D. Schroder, T. Isaacs-Smith, A. Ahyi, J. Williams, G. Chung, J. Wan, and M. Loboda, "Evidence of negative bias temperature instability in 4 H-SiC metal oxide semiconductor capacitors," *Applied Physics Letters,* vol. 90, p. 253508, 2007.

[30] J. O. Gonzalez and O. Alatise, "Bias temperature instability and condition monitoring in SiC power MOSFETs," *Microelectronics Reliability,* vol. 88, pp. 557-562, 2018.

[31] G. Longobardi, F. Udrea, S. Sque, J. Croon, F. Hurkx, E. Napoli, and J. Šonský, "Modelling 2DEG charges in AlGaN/GaN heterostructures," presented at the CAS 2012 (International Semiconductor Conference), pp. 363-366, Sinaia (Romania), October 2012.

[32] Y. Uemoto, Masahiro Hikita, Hiroaki Ueno, Hisayoshi Matsuo, Hidetoshi Ishida, Manabu Yanagihara, Tetsuzo Ueda, Tsuyoshi Tanaka, and Daisuke Ueda, "Gate injection transistor (GIT)—A normally-off AlGaN/GaN power transistor using conductivity modulation," *IEEE Transactions on Electron Devices,* vol. 54, pp. 3393-3399., 2007.

[33] M. Kuraguchi, Y. Takada, T. Suzuki, M. Hirose, K. Tsuda, W. Saito, Y. Saito, and I. Omura, "Normally-off GaN-MISFET with well-controlled threshold voltage," *physica status solidi (a),* vol. 204, pp. 2010-2013, 2007.

[34] H. Amano, Y. Baines, E. Beam, M. Borga, T. Bouchet, P. R. Chalker, M. Charles, K. J. Chen, N. Chowdhury, and R. Chu, "The 2018 GaN power electronics roadmap," *Journal of Physics D: Applied Physics,* vol. 51, p. 163001, 2018.

[35] M. Asif Khan, A. Bhattarai, J. Kuznia, and D. Olson, "High electron mobility transistor based on a GaN-Al x Ga1− x N heterojunction," *Applied Physics Letters,* vol. 63, pp. 1214-1215, 1993.

[36] GaN System. (2018). *GS61008P* [Datasheet]. Available: https://gansystems.com/wp-content/uploads/2018/04/GS61008P-DS-Rev-180420.pdf, accessed on 31/10/2019.

[37] Infineon. (2018). *IGO60R070D1* [Datasheet]. Available: https://www.infineon.com/dgdl/Infineon-IGO60R070D1-DS-v02_01-EN.pdf?fileId=5546d46265f064ff016685f053216514, accessed on 31/10/2018

[38] GaN System. (2018). *GS66516T* [Datasheet]. Available: https://gansystems.com/wp-content/uploads/2018/04/GS66516T-DS-Rev-180422.pdf, accessed on 31/10/2019.

[39] Transphorm. (2017). *TP90H180PS* [Datasheet]. Available: https://www.transphormusa.com/en/document/datasheet-tp90h180ps-900v-gan-fet/, accessed on 31/10/2019.

[40] S. A. Ahsan, S. Ghosh, K. Sharma, A. Dasgupta, S. Khandelwal, and Y. S. Chauhan, "Capacitance modeling in dual field-plate power GaN HEMT for accurate switching behavior," *IEEE Transactions on Electron Devices,* vol. 63, pp. 565-572, 2016.

[41] E. Bahat-Treidel, O. Hilt, F. Brunner, V. Sidorov, J. Würfl, and G. Tränkle, "AlGaN/GaN/AlGaN DH-HEMTs breakdown voltage enhancement using multiple grating field plates (MGFPs)," *IEEE Transactions on Electron Devices,* vol. 57, pp. 1208-1216, 2010.

[42] Y. Dora, A. Chakraborty, L. McCarthy, S. Keller, S. DenBaars, and U. Mishra, "High breakdown voltage achieved on AlGaN/GaN HEMTs with integrated slant field plates," *IEEE Electron Device Letters,* vol. 27, pp. 713-715, 2006.

[43] S. Karmalkar and U. K. Mishra, "Enhancement of breakdown voltage in AlGaN/GaN high electron mobility transistors using a field plate," *IEEE Transactions on Electron Devices,* vol. 48, pp. 1515-1521, 2001.

[44] D. Kinzer and S. Oliver, "Monolithic HV GaN power ICs: performance and application," *IEEE Power Electronics Magazine,* vol. 3, pp. 14-21, 2016.

[45] G. Longobardi and F. Udrea, "On the Time-Dependent Transport Mechanism Between Surface Traps and the 2DEG in AlGaN/GaN Devices," *IEEE Transactions on Electron Devices,* vol. 64, pp. 4415-4423, 2017.

[46] P. Moens, P. Vanmeerbeek, A. Banerjee, J. Guo, C. Liu, P. Coppens, A. Salih, M. Tack, M. Caesar, and M. Uren, "On the impact of carbon-doping on the

dynamic Ron and off-state leakage current of 650V GaN power devices," in *Proc. ISPSD*, 2015, pp. 37-40.

[47] M. J. Uren, J. Moreke, and M. Kuball, "Buffer design to minimize current collapse in GaN/AlGaN HFETs," *IEEE Transactions on Electron Devices,* vol. 59, pp. 3327-3333, 2012.

[48] D. Pagnano, G. Longobardi, F. Udrea, J. Sun, M. Imam, R. Garg, H. Kim, and A. Charles, "On the impact of substrate electron injection on dynamic Ron in GaN-on-Si HEMTs," *Microelectronics Reliability,* vol. 88, pp. 610-614, 2018.

[49] N. Posthuma, S. You, S. Stoffels, D. Wellekens, H. Liang, M. Zhao, B. De Jaeger, K. Geens, N. Ronchi, and S. Decoutere, "An industry-ready 200 mm p-GaN E-mode GaN-on-Si power technology," in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Chicago 13-17 May 2018, pp. 284-287.

[50] S. Kaneko, M. Kuroda, M. Yanagihara, A. Ikoshi, H. Okita, T. Morita, K. Tanaka, M. Hikita, Y. Uemoto, and S. Takahashi, "Current-collapse-free operations up to 850 V by GaN-GIT utilizing hole injection from drain," presented at the 2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD), 2015, pp. pp. 41-44, Hong Kong, 10-15 May 2015.

[51] H. Ohta, K. Hayashi, F. Horikiri, M. Yoshino, T. Nakamura, and T. Mishima, "5.0 kV breakdown-voltage vertical GaN p–n junction diodes," *Japanese Journal of Applied Physics,* vol. 57, p. 04FG09, 2018.

[52] T. Hayashida, T. Nanjo, A. Furukawa, and M. Yamamuka, "Vertical GaN merged PiN Schottky diode with a breakdown voltage of 2 kV," *Applied Physics Express,* vol. 10, p. 061003, 2017.

[53] J. Hu, Y. Zhang, M. Sun, D. Piedra, N. Chowdhury, and T. Palacios, "Materials and processing issues in vertical GaN power electronics," *Materials Science in Semiconductor Processing,* 2017.

[54] T. Oka, T. Ina, Y. Ueno, and J. Nishii, "1.8 mΩ· cm2 vertical GaN-based trench metal–oxide–semiconductor field-effect transistors on a free-standing GaN substrate for 1.2-kV-class operation," *Applied Physics Express,* vol. 8, p. 054101, 2015.

[55] T. Oka, Y. Ueno, T. Ina, and K. Hasegawa, "Vertical GaN-based trench metal oxide semiconductor field-effect transistors on a free-standing GaN substrate with blocking voltage of 1.6 kV," *Applied Physics Express,* vol. 7, p. 021002, 2014.

[56] J. Tsao, S. Chowdhury, M. Hollis, D. Jena, N. Johnson, K. Jones, R. Kaplar, S. Rajan, C. Van de Walle, and E. Bellotti, "Ultrawide-Bandgap Semiconductors: Research Opportunities and Challenges," *Advanced Electronic Materials,* vol. 4, p. 1600501, 2018.

[57] M. Higashiwaki, K. Sasaki, A. Kuramata, T. Masui, and S. Yamakoshi, "Gallium oxide (Ga2O3) metal-semiconductor field-effect transistors on

single-crystal β-Ga2O3 (010) substrates," *Applied Physics Letters,* vol. 100, p. 013504, 2012.

[58] S. Krishnamoorthy, Z. Xia, C. Joishi, Y. Zhang, J. McGlone, J. Johnson, M. Brenner, A. R. Arehart, J. Hwang, and S. Lodha, "Modulation-doped β-(Al0. 2Ga0. 8) 2O3/Ga2O3 field-effect transistor," *Applied Physics Letters,* vol. 111, p. 023502, 2017.

[59] M. Higashiwaki, K. Sasaki, H. Murakami, Y. Kumagai, A. Koukitu, A. Kuramata, T. Masui, and S. Yamakoshi, "Recent progress in Ga2O3 power devices," *Semiconductor Science and Technology,* vol. 31, p. 034001, 2016.

[60] E. Chikoidze, A. Fellous, A. Perez-Tomas, G. Sauthier, T. Tchelidze, C. Ton-That, T. T. Huynh, M. Phillips, S. Russell, and M. Jennings, "P-type β-gallium oxide: A new perspective for power and optoelectronic devices," *Materials Today Physics,* vol. 3, pp. 118-126, 2017.

[61] S. Pearton, J. Yang, P. H. Cary IV, F. Ren, J. Kim, M. J. Tadjer, and M. A. Mastro, "A review of Ga2O3 materials, processing, and devices," *Applied Physics Reviews,* vol. 5, p. 011301, 2018.

[62] J. Yang, F. Renl, M. Tadjer, S. J. Pearton, and A. Kuramata, "2.3 kV Field-Plated Vertical Ga 2 O 3 Schottky Rectifiers and 1 a Forward Current with 650 V Reverse Breakdown Ga 2 O 3 Field-Plated Schottky Barrier Diodes," in *2018 76th Device Research Conference (DRC)*, 2018, pp. 1-2.

[63] K. Konishi, K. Goto, H. Murakami, Y. Kumagai, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, "1-kV vertical Ga2O3 field-plated Schottky barrier diodes," *Applied Physics Letters,* vol. 110, p. 103506, 2017.

[64] H. Tokuda, M. Hatano, N. Yafune, S. Hashimoto, K. Akita, Y. Yamamoto, and M. Kuzuhara, "High Al composition AlGaN-channel high-electron-mobility transistor on AlN substrate," *Applied Physics Express,* vol. 3, p. 121003, 2010.

[65] H. Fu, I. Baranowski, X. Huang, H. Chen, Z. Lu, J. Montes, X. Zhang, and Y. Zhao, "Demonstration of AlN Schottky barrier diodes with blocking voltage over 1 kV," *IEEE Electron Device Letters,* vol. 38, pp. 1286-1289, 2017.

[66] H. Okumura, S. Suihkonen, J. Lemettinen, A. Uedono, Y. Zhang, D. Piedra, and T. Palacios, "AlN metal–semiconductor field-effect transistors using Si-ion implantation," *Japanese Journal of Applied Physics,* vol. 57, p. 04FR11, 2018.

[67] H. Umezawa, "Recent advances in diamond power semiconductor devices," *Materials Science in Semiconductor Processing,* 78, pp.147-156, 2018.

[68] S. Shikata, "Single crystal diamond wafers for high power electronics," *Diamond and Related Materials,* vol. 65, pp. 168-175, 2016.

[69] J. Achard and A. Tallaire, "1.1 Growth of thick CVD diamond films on different crystalline orientations: defects and doping," *Power Electronics Device Applications of Diamond Semiconductors,* pp. 1-27, 2018, Woodhead Publishing Series: Cambridge (UK).

[70] S. Tarelkin, V. Bormashov, S. Buga, A. Volkov, D. Teteruk, N. Kornilov, M. Kuznetsov, S. Terentiev, A. Golovanov, and V. Blank, "Power diamond vertical Schottky barrier diode with 10 A forward current," *physica status solidi (a),* vol. 212, pp. 2621-2627, 2015.

[71] G. Perez, P. Lefranc, P.-O. Jeannin, D. Eon, and N. Rouger, "Parallel and interleaved structures for diamond Schottky diodes," in *Power Electronics and Applications (EPE'17 ECCE Europe), 2017 19th European Conference on*, 2017, pp. P. 1-P. 10, 11-14 September 2017, Warsaw (Poland).

[72] S. J. Rashid, "High voltage packaging technology for wide bandgap power semiconductor devices," University of Cambridge, 2008, Ph.D. Dissertation.

[73] L. F. Dobrzhinetskaya, "Microdiamonds—Frontier of ultrahigh-pressure metamorphism: A review," *Gondwana Research,* vol. 21, pp. 207-223, 2012.

[74] A. Tallaire, V. Mille, O. Brinza, T. N. T. Thi, J. Brom, Y. Loguinov, A. Katrusha, A. Koliadin, and J. Achard, "Thick CVD diamond films grown on high-quality type IIa HPHT diamond substrates from New Diamond Technology," *Diamond and Related Materials,* vol. 77, pp. 146-152, 2017.

[75] H. Yamada, A. Chayahara, Y. Mokuno, Y. Kato, and S. Shikata, "A 2-in. mosaic wafer made of a single-crystal diamond," *Applied Physics Letters,* vol. 104, p. 102110, 2014.

[76] M. Schreck and J.-C. Arnault, "1.4 Heteroepitaxy of diamond on Ir/metal-oxide/Si substrates," *Power Electronics Device Applications of Diamond Semiconductors,* p. 58, 2018, Woodhead Publishing Series: Cambridge (UK).

[77] M. Schreck, H. Roll, and B. Stritzker, "Diamond/Ir/SrTiO 3: A material combination for improved heteroepitaxial diamond films," *Applied Physics Letters,* vol. 74, pp. 650-652, 1999.

[78] M. S. Dresselhaus and R. Kalish, *Ion implantation in diamond, graphite and related materials* vol. 22: Springer Science & Business Media, 2013.

[79] N. Tsubouchi, "2.3 Ion implantation doping of diamond," *Power Electronics Device Applications of Diamond Semiconductors,* pp. 137-153, 2018, Woodhead Publishing Series: Cambridge (UK).

[80] Z. Ma and J.-H. Seo, "Thermal diffusion doping of diamond," 2017, U.S. Patent No. 9,605,359.

[81] J.-H. Seo, H. Wu, S. Mikael, H. Mi, J. P. Blanchard, G. Venkataramanan, W. Zhou, S. Gong, D. Morgan, and Z. Ma, "Thermal diffusion boron doping of single-crystal natural diamond," *Journal of Applied Physics,* vol. 119, p. 205703, 2016.

[82] S. Koizumi, "2.2 n-Type diamond growth and the semiconducting properties," *Power Electronics Device Applications of Diamond Semiconductors,* pp. 117-137, 2018, Woodhead Publishing Series: Cambridge (UK).

[83] T. Iwasaki, Y. Hoshino, K. Tsuzuki, H. Kato, T. Makino, M. Ogura, D. Takeuchi, T. Matsumoto, H. Okushi, and S. Yamasaki, "Diamond junction

field-effect transistors with selectively grown n+-side gates," *Applied Physics Express,* vol. 5, p. 091301, 2012.

[84] T. Grotjohn, D. Tran, M. Yaran, S. Demlow, and T. Schuelke, "Heavy phosphorus doping by epitaxial growth on the (111) diamond surface," *Diamond and Related Materials,* vol. 44, pp. 129-133, 2014.

[85] Y. Hoshino, H. Kato, T. Makino, M. Ogura, T. Iwasaki, M. Hatano, and S. Yamasaki, "Electrical properties of lateral p–n junction diodes fabricated by selective growth of n+ diamond," *physica status solidi (a),* vol. 209, pp. 1761-1764, 2012.

[86] S. Ohmagari, T. Teraji, and Y. Koide, "Non-destructive detection of killer defects of diamond Schottky barrier diodes," *Journal of Applied Physics,* vol. 110, p. 056105.,2011.

[87] H. Umezawa, H. Gima, K. Driche, Y. Kato, T. Yoshitake, Y. Mokuno, and E. Gheeraert, "Defect and field-enhancement characterization through electron-beam-induced current analysis," *Applied Physics Letters,* vol. 110, p. 182103, 2017.

[88] H. Umezawa, Y. Mokuno, H. Yamada, A. Chayahara, and S.-i. Shikata, "Characterization of Schottky barrier diodes on a 0.5-inch single-crystalline CVD diamond wafer," *Diamond and Related Materials,* vol. 19, pp. 208-212, 2010.

[89] M. Kasu, M. Kubovic, A. Aleksov, N. Teofilov, Y. Taniyasu, R. Sauer, E. Kohn, T. Makimoto, and N. Kobayashi, "Influence of epitaxy on the surface conduction of diamond film," *Diamond and Related Materials,* vol. 13, pp. 226-232, 2004.

[90] T. Shimaoka, T. Teraji, K. Watanabe, and S. Koizumi, "Characteristic Luminescence Correlated with Leaky Diamond Schottky Barrier Diodes," *physica status solidi (a),* vol. 214, p. 1700180, 2017.

[91] T. Teraji, A. Fiori, N. Kiritani, S. Tanimoto, E. Gheeraert, and Y. Koide, "Mechanism of reverse current increase of vertical-type diamond Schottky diodes," *Journal of Applied Physics,* vol. 122, p. 135304, 2017.

[92] P. Muret, A. Traoré, A. Maréchal, D. Eon, J. Pernot, J. Pinẽro, M. d. P. Villar, and D. Araujo, "Potential barrier heights at metal on oxygen-terminated diamond interfaces," *Journal of Applied Physics,* vol. 118, p. 204505, 2015.

[93] H. Umezawa, T. Saito, N. Tokuda, M. Ogura, S.-G. Ri, H. Yoshikawa, and S.-i. Shikata, "Leakage current analysis of diamond Schottky barrier diode," *Applied Physics Letters,* vol. 90, p. 073506, 2007.

[94] R. Kumaresan, H. Umezawa, N. Tatsumi, K. Ikeda, and S. Shikata, "Device processing, fabrication and analysis of diamond pseudo-vertical Schottky barrier diodes with low leak current and high blocking voltage," *Diamond and Related Materials,* vol. 18, pp. 299-302, 2009.

[95] T. Iwasaki, T. Suwa, J. Yaita, H. Kato, T. Makino, M. Ogura, D. Takeuchi, S. Yamasaki, and M. Hatano, "Observation of interface defects in diamond lateral

p-n-junction diodes and their effect on reverse leakage current," *IEEE Trans. Electron Devices,* vol. 64, pp. 3298-3302, 2017.

[96] T. Teraji, "Ultrapure Homoepitaxial Diamond Films Grown by Chemical Vapor Deposition," *ECS Transactions,* vol. 80, pp. 271-276, 2017.

[97] H. Kato, M. Ogura, T. Makino, D. Takeuchi, and S. Yamasaki, "N-type control of single-crystal diamond films by ultra-lightly phosphorus doping," *Applied Physics Letters,* vol. 109, p. 142102, 2016.

[98] T. Iwasaki, Y. Hoshino, K. Tsuzuki, H. Kato, T. Makino, M. Ogura, D. Takeuchi, H. Okushi, S. Yamasaki, and M. Hatano, "High-Temperature Operation of Diamond Junction Field-Effect Transistors With Lateral p-n Junctions," *IEEE Electron Device Letters,* vol. 34, pp. 1175-1177, 2013.

[99] M. Dutta, F. Koeck, R. Nemanich, and S. Chowdhury, "Pin diodes enabled by homoepitaxially grown phosphorus doped diamond with breakdown electric field> 1.25 MV/cm," in *2015 73rd Annual Device Research Conference (DRC), 21-24 June 2015, Columbus, Ohio, USA.*, 2015, pp. 184-184.

[100] J. Butler, M. Geis, K. Krohn, J. Lawless Jr, S. Deneault, T. Lyszczarz, D. Flechtner, and R. Wright, "Exceptionally high voltage Schottky diamond diodes and low boron doping," *Semiconductor Science and Technology,* vol. 18, p. S67, 2003.

[101] S. Ohmagari, "2.1 Growth and characterization of heavily B-doped p1 diamond for vertical power devices," *Power Electronics Device Applications of Diamond Semiconductors,* pp. 99-117, 2018, Woodhead Publishing Series: Cambridge (UK).

[102] "4 - Key technologies for device fabrications and materials characterizations," in *Power Electronics Device Applications of Diamond Semiconductors*, S. Koizumi, H. Umezawa, J. Pernot, and M. Suzuki, Eds., ed: Woodhead Publishing, 2018, pp. 219-294.

[103] G. Chicot, A. Maréchal, R. Motte, P. Muret, E. Gheeraert, and J. Pernot, "Metal oxide semiconductor structure using oxygen-terminated diamond," *Applied Physics Letters,* vol. 102, p. 242108, 2013.

[104] T. Teraji, Y. Garino, Y. Koide, and T. Ito, "Low-leakage p-type diamond Schottky diodes prepared using vacuum ultraviolet light/ozone treatment," *Journal of Applied Physics,* vol. 105, p.126109., 2009.

[105] H. Kawarada, "Hydrogen-terminated diamond surfaces and interfaces," *Surface Science Reports,* vol. 26, pp. 205208-206259, 1996.

[106] J. Cui, J. Ristein, and L. Ley, "Electron affinity of the bare and hydrogen covered single crystal diamond (111) surface," *Physical Review Letters,* vol. 81, p. 429, 1998.

[107] K. Hirama, H. Sato, Y. Harada, H. Yamamoto, and M. Kasu, "Thermally stable operation of H-terminated diamond FETs by NO2 adsorption and Al2O3 passivation," *IEEE Electron Device Letters,* vol. 33, p. 1111, 2012.

[108] H. Kawarada, T. Yamada, D. Xu, H. Tsuboi, Y. Kitabayashi, D. Matsumura, M. Shibata, T. Kudo, M. Inaba, and A. Hiraiwa, "Durability-enhanced two-dimensional hole gas of CH diamond surface for complementary power inverter applications," *Scientific Reports,* vol. 7, p. 42368, 2017.

[109] Z. Ren, G. Yuan, J. Zhang, L. Xu, J. Zhang, W. Chen, and Y. Hao, "Hydrogen-terminated polycrystalline diamond MOSFETs with Al2O3 passivation layers grown by atomic layer deposition at different temperatures," *AIP Advances,* vol. 8, p. 065026, 2018.

[110] M. Syamsul, N. Oi, S. Okubo, T. Kageura, and H. Kawarada, "Heteroepitaxial Diamond Field-Effect Transistor for High Voltage Applications," *IEEE Electron Device Letters,* vol. 39, pp. 51-54, 2018.

[111] D. Kueck, J. Scharpf, W. Ebert, M. Fikry, F. Scholz, and E. Kohn, "Passivation of H-terminated diamond with MOCVD-aluminium nitride–a key to understand and stabilize its surface conductivity," *physica status solidi (a),* vol. 207, pp. 2035-2039, 2010.

[112] C. Miskys, J. Garrido, C. Nebel, M. Hermann, O. Ambacher, M. Eickhoff, and M. Stutzmann, "AlN/diamond heterojunction diodes," *Applied Physics Letters,* vol. 82, pp. 290-292, 2003.

[113] M. Imura, R. Hayakawa, H. Ohsato, E. Watanabe, D. Tsuya, T. Nagata, M. Liao, Y. Koide, J.-i. Yamamoto, and K. Ban, "Development of AlN/diamond heterojunction field effect transistors," *Diamond and Related Materials,* vol. 24, pp. 206-209, 2012.

[114] M. Imura, R. Hayakawa, E. Watanabe, M. Liao, Y. Koide, and H. Amano, "Demonstration of diamond field effect transistors by AlN/diamond heterostructure," *physica status solidi (RRL)–Rapid Research Letters,* vol. 5, pp. 125-127, 2011.

[115] I. Akimoto, N. Naka, and N. Tokuda, "Time-resolved cyclotron resonance on dislocation-free HPHT diamond," *Diamond and Related Materials,* vol. 63, pp. 38-42, 2016.

[116] J. Barjon, E. Chikoidze, F. Jomard, Y. Dumont, M. A. Pinault-Thaury, R. Issaoui, O. Brinza, J. Achard, and F. Silva, "Homoepitaxial boron-doped diamond with very low compensation," *physica status solidi (a),* vol. 209, pp. 1750-1753, 2012.

[117] V. Bormashov, S. Tarelkin, S. Buga, M. Kuznetsov, S. Terentiev, A. Semenov, and V. Blank, "Electrical properties of the high quality boron-doped synthetic single-crystal diamonds grown by the temperature gradient method," *Diamond and Related Materials,* vol. 35, pp. 19-23, 2013.

[118] J. Pernot, "2.5 Carrier mobility in diamond: from material to devices," *Power Electronics Device Applications of Diamond Semiconductors,* pp. 174-189, 2018, Woodhead Publishing Series: Cambridge (UK).

[119] Y. Sasama, K. Komatsu, S. Moriyama, M. Imura, T. Teraji, K. Watanabe, T. Taniguchi, T. Uchihashi, and Y. Takahide, "High-mobility diamond field

effect transistor with a monocrystalline h-BN gate dielectric," *APL Materials,* vol. 6, p. 111105, 2018.

[120] J. Pernot and S. Koizumi, "Electron mobility in phosphorous doped {111} homoepitaxial diamond," *Applied Physics Letters,* vol. 93, p. 052105, 2008.

[121] J. Isberg, J. Hammersberg, E. Johansson, T. Wikström, D. J. Twitchen, A. J. Whitehead, S. E. Coe, and G. A. Scarsbrook, "High carrier mobility in single-crystal plasma-deposited diamond," *Science,* vol. 297, pp. 1670-1672, 2002.

[122] J. Pernot, C. Tavares, E. Gheeraert, E. Bustarret, M. Katagiri, and S. Koizumi, "Hall electron mobility in diamond," *Applied Physics Letters,* vol. 89, p. 122111, 2006.

[123] P.-N. Volpe, J. Pernot, P. Muret, and F. Omnès, "High hole mobility in boron doped diamond for power device applications," *Applied Physics Letters,* vol. 94, p. 2102, 2009.

[124] A. Traoré, S. Koizumi, and J. Pernot, "Effect of n-and p-type doping concentrations and compensation on the electrical properties of semiconducting diamond," *physica status solidi (a),* vol. 213, pp. 2036-2043, 2016.

[125] J. Pernot, P.-N. Volpe, F. Omnès, P. Muret, V. Mortet, K. Haenen, and T. Teraji, "Hall hole mobility in boron-doped homoepitaxial diamond," *Physical Review B,* vol. 81, p. 205203, 2010.

[126] Y. Li, J. F. Zhang, G. P. Liu, Z. Y. Ren, J. C. Zhang, and Y. Hao, "Mobility of Two-Dimensional Hole Gas in H-Terminated Diamond," *physica status solidi (RRL)–Rapid Research Letters,* vol. 12, p. 1700401, 2018.

[127] J. E. Butler, A. Vikharev, A. Gorbachev, M. Lobaev, A. Muchnikov, D. Radischev, V. Isaev, V. Chernov, S. Bogdanov, and M. Drozdov, "Nanometric diamond delta doping with boron," *physica status solidi (RRL)-Rapid Research Letters,* vol. 11, 2017.

[128] T. Matsumoto, H. Kato, K. Oyama, T. Makino, M. Ogura, D. Takeuchi, T. Inokuma, N. Tokuda, and S. Yamasaki, "Inversion channel diamond metal-oxide-semiconductor field-effect transistor with normally off characteristics," *Scientific Reports,* vol. 6, 2016.

[129] M. Shin, R. Trew, and G. Bilbro, "High temperature DC and RF performance of p-type diamond MESFET: comparison with n-type GaAs MESFET," *IEEE Electron Device Letters,* vol. 15, pp. 292-294, 1994.

[130] K. Tsugawa, K. Kitatani, H. Noda, A. Hokazono, K. Hirose, M. Tajima, and H. Kawarada, "High-preformance diamond surface-channel field-effect transistors and their operation mechanism," *Diamond and Related Materials,* vol. 8, pp. 927-933, 1999.

[131] E. Kohn, M. Adamschik, P. Schmid, A. Denisenko, A. Aleksov, and W. Ebert, "Prospects of diamond devices," *Journal of Physics D: Applied Physics,* vol. 34, p. R77, 2001.

[132] A. Aleksov, M. Kubovic, N. Kaeb, U. Spitzberg, A. Bergmaier, G. Dollinger, T. Bauer, M. Schreck, B. Stritzker, and E. Kohn, "Diamond field effect transistors—concepts and challenges," *Diamond and Related Materials,* vol. 12, pp. 391-398, 2003.

[133] N. Kawakami, Y. Yokota, K. Hayashi, T. Tachibana, and K. Kobashi, "Device operation of pip type diamond metal–insulator–semiconductor field effect transistors with sub-micrometer channel," *Diamond and Related Materials,* vol. 14, pp. 509-513, 2005.

[134] S. Rashid, A. Tajani, L. Coulbeck, M. Brezeanu, A. Garraway, T. Butler, N. Rupesinghe, D. Twitchen, G. Amaratunga, and F. Udrea, "Modelling of single-crystal diamond Schottky diodes for high-voltage applications," *Diamond and Related Materials,* vol. 15, pp. 317-323, 2006.

[135] M. Brezeanu, M. Avram, S. Rashid, G. Amaratunga, T. Butler, N. Rupesinghe, F. Udrea, A. Tajani, M. Dixon, and D. Twitchen, "Termination structures for diamond Schottky barrier diodes," in *Power Semiconductor Devices and IC's, 2006. ISPSD 2006, Naples, Italy, 4 - 8 June*, 2006, pp. 1-4.

[136] S. Rashid, A. Tajani, D. Twitchen, L. Coulbeck, F. Udrea, T. Butler, N. Rupesinghe, M. Brezeanu, J. Isberg, and A. Garraway, "Numerical parameterization of chemical-vapor-deposited (CVD) single-crystal diamond for device simulation and analysis," *IEEE Transactions on Electron Devices,* vol. 55, pp. 2744-2756, 2008.

[137] J. Isberg, A. Lindblom, A. Tajani, and D. Twitchen, "Temperature dependence of hole drift mobility in high-purity single-crystal CVD diamond," *physica status solidi (a),* vol. 202, pp. 2194-2198, 2005.

[138] A. Nawawi, K. J. Tseng, R. Rusli, and G. A. Amaratunga, "Switching characteristics of diamond-based mi-p+ diodes in power electronic applications," in *2011 IEEE Energy Conversion Congress and Exposition*, 2011, pp. 2676-2680.

[139] A. Nawawi, K. Tseng, G. Amaratunga, H. Umezawa, and S. Shikata, "Design and optimization of planar mesa termination for diamond Schottky barrier diodes," *Diamond and Related Materials,* vol. 36, pp. 51-57, 2013.

[140] A. Nawawi, K. Tseng, G. Amaratunga, H. Umezawa, and S. Shikata, "Modeling and simulation of non-ideal characteristics of vertical Mo/diamond Schottky barrier diode based on MIS model," *Transactions of the Materials Research Society of Japan,* vol. 39, pp. 297-303, 2014.

[141] A. Maréchal, N. Rouger, J.-C. Crebier, J. Pernot, S. Koizumi, T. Teraji, and E. Gheeraert, "Model implementation towards the prediction of J (V) characteristics in diamond bipolar device simulations," *Diamond and Related Materials,* vol. 43, pp. 34-42, 2014.

[142] N. Donato, M. Antoniou, E. Napoli, G. Amaratunga, and F. Udrea, "On the models used for TCAD simulations of Diamond Schottky Barrier Diodes,"

presented at the Semiconductor Conference (CAS), 2015 International, 2015, pp. pp. 223-226, October 2015.

[143] R. Hathwar, M. Dutta, F. A. Koeck, R. J. Nemanich, S. Chowdhury, and S. M. Goodnick, "Temperature dependent simulation of diamond depleted Schottky PIN diodes," *Journal of Applied Physics,* vol. 119, p. 225703, 2016.

[144] N. Donato, D. Pagnano, E. Napoli, G. Longobardi, and F. Udrea, "Design of a normally-off diamond JFET for high power integrated applications," *Diamond and Related Materials,* 2017.

[145] D.-W. Kang, H. N. Chang, and M.-W. Ha, "Numerical simulation of p-type diamond Schottky barrier diodes for high breakdown voltage," *Japanese Journal of Applied Physics,* vol. 56,06GE09, 2017.

[146] C. Clark, P. Dean, and P. Harris, "Intrinsic edge absorption in diamond," *Proceedings of the Royal Society of London. Series A. Mathematical and Physical Sciences,* vol. 277, pp. 312-329, 1964.

[147] A. l. Maréchal, "Metal-oxide-semiconductor capacitor for diamond transistor: simulation, fabrication and electrical analysis," PhD Dissertation, Grenoble Alpes, 2015.

[148] N. Naka, K. Fukai, Y. Handa, and I. Akimoto, "Direct measurement via cyclotron resonance of the carrier effective masses in pristine diamond," *Physical Review B,* vol. 88, p. 035205, 2013.

[149] M. Willatzen, M. Cardona, and N. Christensen, "Linear muffin-tin-orbital and k· p calculations of effective masses and band structure of semiconducting diamond," *Physical Review B,* vol. 50, p. 18054, 1994.

[150] (2016). *Sentaurus TCAD Manual, Synopsys (Mountain View)*.

[151] N. D. Arora, J. R. Hauser, and D. J. Roulston, "Electron and hole mobilities in silicon as a function of concentration and temperature," *IEEE Transactions on Electron Devices,* vol. 29, pp. 292-295, 1982.

[152] S. M. Sze and K. K. Ng. (2006). *Physics of semiconductor devices, John wiley & sons: New York*.

[153] N. Donato and F. Udrea, "Static and dynamic effects of the incomplete ionization in SuperJunction devices," *IEEE Transactions on Electron Devices,* vol. 65, pp. 4469-4475, 2018.

[154] Y. Fu, Y. Xu, R. Xu, J. Zhou, and Y. Kong, "Physical-based simulation of DC characteristics of hydrogen-terminated diamond MOSFETs," in *Electrical Design of Advanced Packaging and Systems Symposium (EDAPS), 2017 IEEE, 14-16 December, Zhejiang University(China)*, 2017, pp. 1-3.

[155] X. Zhou and S. Albin, "A new capacitance-voltage model for hydrogen-terminated diamond Mosfet," *ECS Transactions,* vol. 66, pp. 287-296, 2015.

[156] X. Zhou and S. Albin, "Device Simulation of Hydrogen-Terminated Diamond Mosfet and Extraction of Small-Signal Parameters," in *Meeting Abstracts*, 2015, pp. 2194-2194.

[157] T. Oishi, R. Higashi, K. Harada, Y. Koga, M. Kasu, and K. Hirama, "Simulation study of NO 2-exposed H-terminated diamond FETs with Al2O3 insulator gate," in *Future of Electron Devices, Kansai (IMFEDK), 2015 IEEE, Kyoto, Japan. 4 – 5 June 2015*, 2015, pp. 34-35.

[158] H. Y. Wong, N. Braga, and R. Mickevicius, "Prediction of highly scaled hydrogen-terminated diamond MISFET performance based on calibrated TCAD simulation," *Diamond and Related Materials,* vol. 80, pp. 14-17, 2017.

[159] Y. Fu, R. Xu, Y. Xu, J. Zhou, Q. Wu, Y. Kong, Y. Zhang, T. Chen, and B. Yan, "Characterization and Modeling of Hydrogen-Terminated MOSFETs with Single-crystal and Polycrystalline Diamond," *IEEE Electron Device Letters,* 2018: 39(11), 1704-1707.

[160] H. Y. Wong, N. Braga, and R. Mickevicius, "A physical model of the abnormal behavior of hydrogen-terminated Diamond MESFET," in *Simulation of Semiconductor Processes and Devices (SISPAD), 2017 International Conference on*, 2017, pp. 333-336.

[161] A. Hiraiwa and H. Kawarada, "Figure of merit of diamond power devices based on accurately estimated impact ionization processes," *Journal of Applied Physics,* vol. 114, p. 034506, 2013.

[162] A. Hiraiwa and H. Kawarada, "Blocking characteristics of diamond junctions with a punch-through design," *Journal of Applied Physics,* vol. 117, p. 124503, 2015.

[163] Y. Kamakura, T. Kotani, K. Konaga, N. Minamitani, G. Wakimura, and N. Mori, "Ab initio study of avalanche breakdown in diamond for power device applications," in *Electron Devices Meeting (IEDM), 2015 IEEE International*, 2015, 7-9 December 2015, Washington (USA), pp. 5.2. 1-5.2. 4.

[164] T. Watanabe, M. Irie, T. Teraji, T. Ito, Y. Kamakura, and K. Taniguchi, "Impact excitation of carriers in diamond under extremely high electric fields," *Japanese Journal of Applied Physics,* vol. 40 L715, 2001.

[165] K. Driche, H. Umezawa, N. Rouger, G. Chicot, and E. Gheeraert, "Characterization of breakdown behavior of diamond Schottky barrier diodes using impact ionization coefficients," *Japanese Journal of Applied Physics,* vol. 56 04CR12, 2017.

[166] A. Marechal, G. Chicot, N. Rouger, P. Muret, J. Pernot, and E. Gheeraert, "Leakage current conduction mechanisms in atomic layer deposited HfO2, ZrO2 and Al2O3 on O-terminated diamond," in *International Conference on Diamond and Carbon Materials, Madrid (Spain) September 7-11, 2014*, 2014.

[167] T. Pham, A. Maréchal, P. Muret, D. Eon, E. Gheeraert, N. Rouger, and J. Pernot, "Comprehensive electrical analysis of metal/Al2O3/O-terminated diamond capacitance," *Journal of Applied Physics,* vol. 123, p. 161523, 2018.

[168] M. Geis, D. Rathman, D. Ehrlich, R. Murphy, and W. Lindley, "High-temperature point-contact transistors and Schottky diodes formed on synthetic

boron-doped diamond," *IEEE Electron Device Letters,* vol. 8, pp. 341-343, 1987.

[169] H. Shiomi, H. Nakahata, T. Imai, Y. Nishibayashi, and N. Fujimori, "Electrical characteristics of metal contacts to boron-doped diamond epitaxial film," *Japanese journal of applied physics,* vol. 28, p. 758, 1989.

[170] G. S. Gildenblat, S. Grot, C. Wronski, A. Badzian, T. Badzian, and R. Messier, "Electrical characteristics of Schottky diodes fabricated using plasma assisted chemical vapor deposited diamond films," *Applied Physics Letters,* vol. 53, pp. 586-588, 1988.

[171] P.-N. Volpe, P. Muret, J. Pernot, F. Omnès, T. Teraji, Y. Koide, F. Jomard, D. Planson, P. Brosselard, and N. Dheilly, "Extreme dielectric strength in boron doped homoepitaxial diamond," *Applied Physics Letters,* vol. 97, p. 223501, 2010.

[172] V. Blank, V. Bormashov, S. Tarelkin, S. Buga, M. Kuznetsov, D. Teteruk, N. Kornilov, S. Terentiev, and A. Volkov, "Power high-voltage and fast response Schottky barrier diamond diodes," *Diamond and Related Materials,* vol. 57, pp. 32-36, 2015.

[173] K. Ueda, K. Kawamoto, and H. Asano, "High-temperature and high-voltage characteristics of Cu/diamond Schottky diodes," *Diamond and Related Materials,* vol. 57, pp. 28-31, 2015.

[174] H. Umezawa, S.-i. Shikata, and T. Funaki, "Diamond Schottky barrier diode for high-temperature, high-power, and fast switching applications," *Japanese journal of applied physics,* vol. 53, p. 05FP06, 2014.

[175] H. Umezawa, Y. Kato, and S.-i. Shikata, "1 Ω on-resistance diamond vertical-Schottky barrier diode operated at 250° C," *Applied Physics Express,* vol. 6, p. 011302, 2012.

[176] K. Ikeda, H. Umezawa, and S. Shikata, "Schottky diamond semiconductor device and manufacturing method for a Schottky electrode for diamond semiconductor device," ed: Google Patents, 2012.

[177] M. Brezeanu, "Diamond Schottky barrier diodes," University of Cambridge, Ph.D Dissertation, 2008.

[178] M. Wade, P. Muret, F. Omnès, and A. Deneuville, "Technology and electrical properties of ohmic contacts and Schottky diodes on homoepitaxial layers grown on (100) diamond surfaces," *Diamond and Related Materials,* vol. 15, pp. 614-617, 2006.

[179] Y. Garino, T. Teraji, S. Koizumi, Y. Koide, and T. Ito, "p-type diamond Schottky diodes fabricated by vacuum ultraviolet light/ozone surface oxidation: Comparison with diodes based on wet-chemical oxidation," *physica status solidi (a),* vol. 206, pp. 2082-2085, 2009.

[180] P. Muret, P.-N. Volpe, T.-N. Tran-Thi, J. Pernot, C. Hoarau, F. Omnès, and T. Teraji, "Schottky diode architectures on p-type diamond for fast switching,

high forward current density and high breakdown field rectifiers," *Diamond and Related Materials,* vol. 20, pp. 285-289, 2011.

[181] H. Umezawa, N. Tokuda, M. Ogura, S.-G. Ri, and S.-i. Shikata, "Characterization of leakage current on diamond Schottky barrier diodes using thermionic-field emission modeling," *Diamond and Related Materials,* vol. 15, pp. 1949-1953, 2006.

[182] M. Kubovic, H. El-Hajj, J. Butler, and E. Kohn, "Diamond merged diode," *Diamond and Related Materials,* vol. 16, pp. 1033-1037, 2007.

[183] T. Iwasaki, Y. Hoshino, K. Tsuzuki, H. Kato, T. Makino, M. Ogura, D. Takeuchi, T. Matsumoto, H. Okushi, and S. Yamasaki, "Diamond semiconductor JFETs by selectively grown n+-diamond side gates for next generation power devices," in *Electron Devices Meeting (IEDM), 2012 IEEE International*, 2012, pp. 7.5. 1-7.5. 4, San Francisco(USA), 10-13 December 2012.

[184] M. Dutta, F. A. Koeck, W. Li, R. J. Nemanich, and S. Chowdhury, "High voltage diodes in diamond using (100)-and (111)-substrates," *IEEE Electron Device Letters,* vol. 38, pp. 600-603, 2017.

[185] M. Suzuki, T. Sakai, T. Makino, H. Kato, D. Takeuchi, M. Ogura, H. Okushi, and S. Yamasaki, "Electrical characterization of diamond PiN diodes for high voltage applications," *physica status solidi (a),* vol. 210, pp. 2035-2039, 2013.

[186] J. Holmes, M. Dutta, F. A. Koeck, M. Benipal, J. Brown, B. Fox, R. Hathwar, H. Johnson, M. Malakoutian, and M. Saremi, "A 4.5 μm PIN diamond diode for detecting slow neutrons," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment,* vol. 903, pp. 297-301, 2018.

[187] K. Oyama, S.-G. Ri, H. Kato, M. Ogura, T. Makino, D. Takeuchi, N. Tokuda, H. Okushi, and S. Yamasaki, "High performance of diamond p+-i-n+ junction diode fabricated using heavily doped p+ and n+ layers," *Applied Physics Letters,* vol. 94, p. 152109, 2009.

[188] T. Klein, P. Achatz, J. Kacmarcik, C. Marcenat, F. Gustafsson, J. Marcus, E. Bustarret, J. Pernot, F. Omnes, and B. E. Sernelius, "Metal-insulator transition and superconductivity in boron-doped diamond," *Physical Review B,* vol. 75, p. 165313, 2007.

[189] A. Traoré, A. Nakajima, T. Makino, D. Kuwabara, H. Kato, M. Ogura, D. Takeuchi, and S. Yamasaki, "Reverse-recovery of diamond pin diodes," *IET Power Electronics,* vol. 11, pp. 695-699, 2017.

[190] V. Bormashov, S. Terentiev, S. Buga, S. Tarelkin, A. Volkov, D. Teteruk, N. Kornilov, M. Kuznetsov, and V. Blank, "Thin large area vertical Schottky barrier diamond diodes with low on-resistance made by ion-beam assisted lift-off technique," *Diamond and Related Materials,* vol. 75, pp. 78-84, 2017.

[191] H. Umezawa, K. Ikeda, N. Tatsumi, K. Ramanujam, and S.-i. Shikata, "Device scaling of pseudo-vertical diamond power Schottky barrier diodes," *Diamond and Related Materials,* vol. 18, pp. 1196-1199, 2009.

[192] N. Ozawa, T. Makino, H. Kato, M. Ogura, Y. Kato, D. Takeuchi, H. Okushi, and S. Yamasaki, "Temperature dependence of electrical characteristics for diamond Schottky-p-n diode in forward bias," *Diamond and Related Materials,* vol. 85, pp. 49-52, 2018.

[193] M. Suzuki, "High voltage diamond pin diodes: Feasibility study on ultimate properties of diamond toward ultimate power devices," *OYO BUTURI,* vol. 85 n.3, pp. 218-222, 2016.

[194] H. Umezawa, M. Nagase, Y. Kato, and S.-i. Shikata, "High temperature application of diamond power device," *Diamond and Related Materials,* vol. 24, pp. 201-205, 2012.

[195] T. Makino, H. Kato, N. Tokuda, M. Ogura, D. Takeuchi, K. Oyama, S. Tanimoto, H. Okushi, and S. Yamasaki, "Diamond Schottky-p-n diode without trade-off relationship between on-resistance and blocking voltage," *physica status solidi (a),* vol. 207, pp. 2105-2109, 2010.

[196] D. Zhao, C. Hu, Z. Liu, H.-X. Wang, W. Wang, and J. Zhang, "Diamond MIP structure Schottky diode with different drift layer thickness," *Diamond and Related Materials,* vol. 73, pp. 15-18, 2017.

[197] M. Dutta, S. Mandal, R. Hathwar, A. M. Fischer, F. A. Koeck, R. J. Nemanich, S. M. Goodnick, and S. Chowdhury, "Determination of Minority Carrier Lifetime of Holes in Diamond pin Diodes Using Reverse Recovery Method," *IEEE Electron Device Letters,* vol. 39, pp. 552-555, 2018.

[198] G. Perez, G. Chicot, Y. Avenas, P. Lefranc, P.-O. Jeannin, D. Eon, and N. Rouger, "Integrated temperature sensor with diamond Schottky diodes using a thermosensitive parameter," *Diamond and Related Materials,* vol. 78, pp. 83-87, 2017.

[199] T. Makino, S. Tanimoto, Y. Hayashi, H. Kato, N. Tokuda, M. Ogura, D. Takeuchi, K. Oyama, H. Ohashi, and H. Okushi, "Diamond Schottky-p-n diode with high forward current density and fast switching operation," *Applied Physics Letters,* vol. 94, p. 262101, 2009.

[200] M. Saremi, R. Hathwar, M. Dutta, F. A. Koeck, R. J. Nemanich, S. Chowdhury, and S. M. Goodnick, "Analysis of the reverse IV characteristics of diamond-based PIN diodes," *Applied Physics Letters,* vol. 111, p. 043507, 2017.

[201] T. Matsumoto, T. Mukose, T. Makino, D. Takeuchi, S. Yamasaki, T. Inokuma, and N. Tokuda, "Diamond Schottky-p-n diode using lightly nitrogen-doped layer," *Diamond and Related Materials,* vol. 75, pp. 152-154, 2017.

[202] T. Makino, H. Kato, D. Takeuchi, M. Ogura, H. Okushi, and S. Yamasaki, "Device design of diamond Schottky-p-n diode for low-loss power electronics," *Japanese Journal of Applied Physics,* vol. 51 090116, 2012.

[203] D. Okamoto, H. Yano, K. Hirata, T. Hatayama, and T. Fuyuki, "Improved inversion channel mobility in 4H-SiC MOSFETs on Si face utilizing phosphorus-doped gate oxide," *IEEE Electron Device Letters,* vol. 31, pp. 710-712, 2010.

[204] J. Liu and Y. Koide, "An Overview of High-k Oxides on Hydrogenated-Diamond for Metal-Oxide-Semiconductor Capacitors and Field-Effect Transistors," *Sensors,* vol. 18, p. 1813, 2018.

[205] D. Araujo and J. Pernot, "5.1. 3 Metal oxide semiconductor interface and transmission electron microscopy characterization," *Power Electronics Device Applications of Diamond Semiconductors,* pp. 323-346, 2018.

[206] S. Yamasaki, E. Gheeraert, and Y. Koide, "Doping and interface of homoepitaxial diamond for electronic applications," *MRS Bulletin,* vol. 39, pp. 499-503, 2014.

[207] K. G. Crawford, D. C. Qi, J. McGlynn, T. G. Ivanov, P. B. Shah, J. Weil, A. Tallaire, A. Y. Ganin, and D. A. J. Moran, "Thermally Stable, High Performance Transfer Doping of Diamond using Transition Metal Oxides," *Scientific Reports,* vol. 8, p. 3342, 2018.

[208] Z. Yin, M. Tordjman, Y. Lee, A. Vardi, R. Kalish, and J. A. del Alamo, "Enhanced transport in transistor by tuning transition-metal oxide electronic states interfaced with diamond," *Science advances,* vol. 4, p. eaau0480, 2018.

[209] Z. Yin, M. Tordjman, A. Vardi, R. Kalish, and J. A. del Alamo, "A Diamond: H/WO 3 Metal–Oxide–Semiconductor Field-Effect Transistor," *IEEE Electron Device Letters,* vol. 39, pp. 540-543, 2018.

[210] J. Robertson, "Band offsets of wide-band-gap oxides and implications for future electronic devices," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena,* vol. 18, pp. 1785-1791, 2000.

[211] W. Mönch, "Empirical tight-binding calculation of the branch-point energy of the continuum of interface-induced gap states," *Journal of Applied Physics,* vol. 80, pp. 5076-5082, 1996.

[212] A. Maréchal, M. Aoukar, C. Vallée, C. Riviere, D. Eon, J. Pernot, and E. Gheeraert, "Energy-band diagram configuration of Al2O3/oxygen-terminated p-diamond metal-oxide-semiconductor," *Applied Physics Letters,* vol. 107, p. 141601, 2015.

[213] J. Liu, M. Liao, M. Imura, T. Matsumoto, N. Shibata, Y. Ikuhara, and Y. Koide, "Control of normally on/off characteristics in hydrogenated diamond metal-insulator-semiconductor field-effect transistors," *Journal of Applied Physics,* vol. 118, p. 115704, 2015.

[214] J. Liu, M. Liao, M. Imura, and Y. Koide, "Normally-off HfO2-gated diamond field effect transistors," *Applied Physics Letters,* vol. 103, p. 092905, 2013.

[215] O. Loto, M. Florentin, C. Masante, N. Donato, M.-L. Hicks, A. Pakpour-Tabrizi, R. Jackman, V. Zuerbig, P. Godignon, and D. Eon, "Gate Oxide

Electrical Stability of p-type Diamond MOS Capacitors," *IEEE Transactions on Electron Devices,* vol. 65, pp. 3361-3364, 2018.

[216] T. Pham, N. Rouger, C. Masante, G. Chicot, F. Udrea, D. Eon, E. Gheeraert, and J. Pernot, "Deep depletion concept for diamond MOSFET," *Applied Physics Letters,* vol. 111, p. 173503, 2017.

[217] T.-T. Pham, J. Pernot, G. Perez, D. Eon, E. Gheeraert, and N. Rouger, "Deep-depletion mode boron doped monocrystalline diamond metal oxide semiconductor field effect transistor," *IEEE Electron Device Letters,* 2017.

[218] E. Napoli and F. Udrea, "Substrate deep depletion: an innovative design concept to improve the voltage rating of SOI power devices," in *Power Semiconductor Devices and IC's, 2006. ISPSD 2006. IEEE International Symposium on*, 2006, pp. 1-4.

[219] A. Rusu and C. Bulucea, "Deep-depletion breakdown voltage of silicon-dioxide/silicon MOS capacitors," *IEEE Transactions on Electron Devices,* vol. 26, pp. 201-205, 1979.

[220] E. H. Nicollian and J. R. Brews, *MOS (metal oxide semiconductor) physics and technology* vol. 1987: Wiley: New York, 1982.

[221] A. Goetzberger, "Behavior of MOS inversion layers at low temperature," *IEEE Transactions on Electron Devices,* vol. 14, pp. 787-789, 1967.

[222] M. Higashiwaki, K. Sasaki, T. Kamimura, M. Hoi Wong, D. Krishnamurthy, A. Kuramata, T. Masui, and S. Yamakoshi, "Depletion-mode Ga2O3 metal-oxide-semiconductor field-effect transistors on β-Ga2O3 (010) substrates and temperature dependence of their device characteristics," *Applied Physics Letters,* vol. 103, p. 123511, 2013.

[223] T.-T. Pham, J. Pernot, G. Perez, D. Eon, E. Gheeraert, and N. Rouger, "Deep-depletion mode boron-doped monocrystalline diamond metal oxide semiconductor field effect transistor," *IEEE Electron Device Letters,* vol. 38, pp. 1571-1574, 2017.

[224] J. P. Cédric Masante , Juliette Letellier , David Eon , Nicolas Rouger ,, "Diamond Deep Depletion Metal Oxide Semiconductor Field Effect Transistor (D3MOSFET) for power electronics," in *ICDCM* Dubrovnik Dubrovnik 2-6 September 2018.

[225] B. Huang, X. Bai, S. K. Lam, and K. K. Tsang, "Diamond FinFET without Hydrogen Termination," *Scientific Reports,* vol. 8, p. 3063, 2018.

[226] T. Pham, J. Pernot, C. Masante, D. Eon, E. Gheeraert, G. Chicot, F. Udrea, and N. Rouger, "200V, 4MV/cm lateral diamond MOSFET," in *Electron Devices Meeting (IEDM), 2017 IEEE International*, 2017, pp. 25.4. 1-25.4. 4, San Francisco, December 2-6, 2017.

[227] H. Umezawa, T. Matsumoto, and S.-I. Shikata, "Diamond Metal–Semiconductor Field-Effect Transistor With Breakdown Voltage Over 1.5 kV," *IEEE Electron Device Letters,* vol. 35, pp. 1112-1114, 2014.

[228] H. U. Khaled Driche, Toshiharu Makino, Masahiko Ogura, Hajime Okumura, Etienne Gheeraert, "Diamond based metal-semiconductor field effect transistor with over 2 kV breakdown voltages," presented at the EMRS 2018 Fall Meeting, Warsaw, 2018.

[229] H. U. Khaled Driche, Toshiharu Makino, Masahiko Ogura, Hajime Okumura, Etienne Gheeraert, "High voltage diamond Reverse Blocking type MESFET with breakdown capabilities up to 3 kV," presented at the EMRS 2018 Fall Meeting, Warsaw, 2018.

[230] T. Iwasaki, J. Yaita, H. Kato, T. Makino, M. Ogura, D. Takeuchi, H. Okushi, S. Yamasaki, and M. Hatano, "600 V Diamond Junction Field-Effect Transistors Operated at 200," *IEEE Electron Device Letters,* vol. 35, pp. 241-243, 2014.

[231] T. Suwa, T. Iwasaki, K. Sato, H. Kato, T. Makino, M. Ogura, D. Takeuchi, S. Yamasaki, and M. Hatano, "Normally-Off Diamond Junction Field-Effect Transistors With Submicrometer Channel," *IEEE Electron Device Letters,* vol. 37, pp. 209-211, 2016.

[232] T. Iwasaki, H. Kato, T. Makino, M. Ogura, D. Takeuchi, S. Yamasaki, and M. Hatano, "High-Temperature Bipolar-Mode Operation of Normally-Off Diamond JFET," *IEEE Journal of the Electron Devices Society,* vol. 5, pp. 95-99, 2017.

[233] H. Kato, "5.2 Technical aspects of diamond p-n junction and bipolar junction transistor formation," *Power Electronics Device Applications of Diamond Semiconductors,* pp. 359-369, 2018.

[234] H. Kato, T. Makino, M. Ogura, D. Takeuchi, and S. Yamasaki, "Fabrication of bipolar junction transistor on (001)-oriented diamond by utilizing phosphorus-doped n-type diamond base," *Diamond and Related Materials,* vol. 34, pp. 41-44, 2013.

[235] H. Kato, K. Oyama, T. Makino, M. Ogura, D. Takeuchi, and S. Yamasaki, "Diamond bipolar junction transistor device with phosphorus-doped diamond base layer," *Diamond and Related Materials,* vol. 27, pp. 19-22, 2012.

[236] D. Eon and H. Umezawa, "5.1 Unipolar devices," *Power Electronics Device Applications of Diamond Semiconductors,* pp. 295-311, 2018.

[237] T. Iwasaki, H. Kato, J. Yaita, T. Makino, M. Ogura, D. Takeuchi, H. Okushi, S. Yamasaki, and M. Hatano, "Current enhancement by conductivity modulation in diamond JFETs for next generation low-loss power devices," in *2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, 2015, pp. 77-80.

[238] S. Grot, G. S. Gildenblat, C. Hatfield, C. Wronski, A. Badzian, T. Badzian, and R. Messier, "The effect of surface treatment on the electrical properties of metal contacts to boron-doped homoepitaxial diamond film," *IEEE Electron Device Letters,* vol. 11, pp. 100-102, 1990.

[239] M. Landstrass and K. Ravi, "Hydrogen passivation of electrically active defects in diamond," *Applied Physics Letters,* vol. 55, pp. 1391-1393, 1989.

[240] S. Albin and L. Watkins, "Electrical properties of hydrogenated diamond," *Applied Physics Letters,* vol. 56, pp. 1454-1456, 1990.

[241] H. Shiomi, Y. Nishibayashi, and N. Fujimori, "Field-effect transistors using boron-doped diamond epitaxial films," *Japanese journal of applied physics,* vol. 28, p. L2153, 1989.

[242] S. Gi, K. Tashiro, S. Tanaka, T. Fujisawa, H. Kimura, T. Kurosu, and M. Iida, "Hall effect measurements of surface conductive layer on undoped diamond films in NO2 and NH3 atmospheres," *Japanese journal of applied physics,* vol. 38, p. 3492, 1999.

[243] H. Kawarada, "5.1. 4 High voltage p-channel MOSFETs using two-dimensional hole gas," *Power Electronics Device Applications of Diamond Semiconductors,* pp. 347-359, 2018.

[244] K. Hirama, H. Sato, Y. Harada, H. Yamamoto, and M. Kasu, "Diamond field-effect transistors with 1.3 A/mm drain current density by Al2O3 passivation layer," *Japanese Journal of Applied Physics,* vol. 51 090112, 2012.

[245] H. Kawarada, T. Yamada, D. Xu, H. Tsuboi, T. Saito, and A. Hiraiwa, "Wide temperature (10K–700K) and high voltage (~ 1000V) operation of CH diamond MOSFETs for power electronics application," in *Electron Devices Meeting (IEDM), 2014 IEEE International*, 2014, pp. 11.2. 1-11.2. 4.

[246] M. Kasu, H. Sato, and K. Hirama, "Thermal stabilization of hole channel on H-terminated diamond surface by using atomic-layer-deposited Al2O3 overlayer and its electric properties," *Applied Physics Express,* vol. 5, p. 025701, 2012.

[247] Y.-F. Wang, X. Chang, X. Zhang, J. Fu, S. Fan, R. Bu, J. Zhang, W. Wang, H.-X. Wang, and J. Wang, "Normally-off hydrogen-terminated diamond field-effect transistor with Al 2 O 3 dielectric layer formed by thermal oxidation of Al," *Diamond and Related Materials,* vol. 81, pp. 113-117, 2018.

[248] J. Liu, M. Liao, M. Imura, H. Oosato, E. Watanabe, and Y. Koide, "Electrical characteristics of hydrogen-terminated diamond metal-oxide-semiconductor with atomic layer deposited HfO2 as gate dielectric," *Applied Physics Letters,* vol. 102, p. 112910, 2013.

[249] S. A. Russell, S. Sharabi, A. Tallaire, and D. A. Moran, "Hydrogen-terminated diamond field-effect transistors with cutoff frequency of 53 GHz," *IEEE Electron Device Letters,* vol. 33, pp. 1471-1473, 2012.

[250] D. A. Moran, O. J. Fox, H. McLelland, S. Russell, and P. W. May, "Scaling of hydrogen-terminated diamond FETs to sub-100-nm gate dimensions," *IEEE Electron Device Letters,* vol. 32, pp. 599-601, 2011.

[251] M. Kubovic and M. Kasu, "Improvement of hydrogen-terminated diamond field effect transistors in nitrogen dioxide atmosphere," *Applied Physics Express,* vol. 2, p. 086502, 2009.

[252] J. Liu, H. Ohsato, X. Wang, M. Liao, and Y. Koide, "Design and fabrication of high-performance diamond triple-gate field-effect transistors," *Scientific Reports,* vol. 6, p. 34757, 2016.

[253] N. Oi, M. Inaba, S. Okubo, I. Tsuyuzaki, T. Kageura, S. Onoda, A. Hiraiwa, and H. Kawarada, "Vertical-type two-dimensional hole gas diamond metal oxide semiconductor field-effect transistors," *Scientific Reports,* vol. 8, p. 10660, 2018.

[254] M. Inaba, T. Muta, M. Kobayashi, T. Saito, M. Shibata, D. Matsumara, T. Kudo, A. Hiraiwa, and H. Kawarada, "Hydrogen-terminated diamond vertical-type metal oxide semiconductor field-effect transistors with a trench gate," *Applied Physics Letters,* vol. 109, p. 033503, 2016.

[255] K. Ueda, M. Kasu, Y. Yamauchi, T. Makimoto, M. Schwitters, D. Twitchen, G. Scarsbrook, and S. Coe, "Diamond FET using high-quality polycrystalline diamond with f/sub T/of 45 GHz and f/sub max/of 120 GHz," *IEEE Electron Device Letters,* vol. 27, pp. 570-572, 2006.

[256] D. Takeuchi, S. Koizumi, T. Makino, H. Kato, M. Ogura, H. Ohashi, H. Okushi, and S. Yamasaki, "Negative electron affinity of diamond and its application to high voltage vacuum power switches," *physica status solidi (a),* vol. 210, pp. 1961-1975, 2013.

[257] D. Takeuchi, T. Makino, H. Kato, M. Ogura, H. Okushi, H. Ohashi, and S. Yamasaki, "High-voltage vacuum switch with a diamond p–i–n diode using negative electron affinity," *Japanese Journal of Applied Physics,* vol. 51 090113, 2012.

[258] D. Takeuchi, T. Makino, H. Kato, H. Okushi, and S. Yamasaki, "Electron emission from diamond p–i–n junction diode with heavily P-doped n+ top layer," *physica status solidi (a),* vol. 208, pp. 2073-2078, 2011.

[259] D. Takeuchi, H. Kawashima, D. Kuwabara, T. Makino, H. Kato, M. Ogura, H. Ohashi, H. Okushi, S. Yamasaki, and S. Koizumi, "4 A/cm 2, 7kV normally-off diamond-emitter vacuum switch," in *Power Semiconductor Devices & IC's (ISPSD), 2015 IEEE 27th International Symposium on*, 2015, pp. 197-200.

[260] D. Takeucni, S. Koizumi, T. Makino, H. Kato, M. Ogura, H. Okusni, H. Onasni, and S. Yamasaki, "A 10kV vacuum switch with negative electron affinity of diamond pin electron emitter," in *Electron Devices Meeting (IEDM), 2012 IEEE International*, 2012, pp. 7.6. 1-7.6. 4.

[261] H. Arbess, K. Isoird, S. Hamady, M. Zerarka, and D. Planson, "Original Field Plate to Decrease the Maximum Electric Field Peak for High-Voltage Diamond Schottky Diode," *IEEE Transactions on Electron Devices,* vol. 62, pp. 2945-2951, 2015.

[262] H. Arbess and K. Isoird, "Field plate termination for high voltage diamond Schottky diode," in *2013 25th International Conference on Microelectronics (ICM)*, 2013, pp. 1-4.

[263] K. Ikeda, H. Umezawa, and S. Shikata, "Edge termination techniques for p-type diamond Schottky barrier diodes," *Diamond and Related Materials,* vol. 17, pp. 809-812, 2008.

[264] K. Driche, S. Rugen, N. Kaminski, H. Umezawa, H. Okumura, and E. Gheeraert, "Electric field distribution using floating metal guard rings edge-termination for Schottky diodes," *Diamond and Related Materials,* vol. 82, pp. 160-164, 2018.

[265] T. Teraji, S. Koizumi, Y. Koide, and T. Ito, "Electric field breakdown of lateral Schottky diodes of diamond," *Japanese Journal of Applied Physics,* vol. 46 L196, 2007.

[266] K. D. Aurélien Maréchal, Juliette Letellier, David Eon, Nicolas Rouger, Etienne Gheeraert, Hitoshi Umezawa, "Edge termination design for high breakdown voltage Schottky barrier diodes," in *European Materials Research Society 2018, Warsaw*, 2018.

[267] W. Huang, T. Chow, J. Yang, and J. Butler, "High-voltage diamond vertical Schottky rectifiers," in *Power Semiconductor Devices and ICs, 2005. Proceedings. ISPSD'05. The 17th International Symposium on*, 2005, pp. 319-322.

[268] H. Umezawa, S. Ohmagari, Y. Mokuno, and J. H. Kaneko, "Characterization of X-ray radiation hardness of diamond Schottky barrier diode and metal-semiconductor field-effect transistor," in *Power Semiconductor Devices and IC's (ISPSD), 2017 29th International Symposium on*, 2017, pp. 379-382.

[269] G. Chicot, D. Eon, and N. Rouger, "Optimal drift region for diamond power devices," *Diamond and Related Materials,* vol. 69, pp. 68-73, 2016.

[270] Microsemi, "Mounting Considerations for the SOT-227 Package," *Application Note 1818,* 2012.

[271] G. Perez, "Diamond semiconductor performances in power electronics applications," *IEEE Transaction on Power Electronics,* (Submitted) 2018.

[272] S. Zelmat, M.-L. Locatelli, T. Lebey, and S. Diaham, "Investigations on high temperature polyimide potentialities for silicon carbide power device passivation," *Microelectronic Engineering,* vol. 83, pp. 51-54, 2006.

[273] M.-L. Locatelli, R. Khazaka, S. Diaham, C.-D. Pham, M. Bechara, S. Dinculescu, and P. Bidan, "Evaluation of encapsulation materials for high-temperature power device packaging," *IEEE Transactions on Power Electronics,* vol. 29, pp. 2281-2288, 2014.

[274] R. Khazaka, L. Mendizabal, D. Henry, and R. Hanna, "Survey of high-temperature reliability of power electronics packaging components," *IEEE Transactions on Power Electronics,* vol. 30, pp. 2456-2464, 2015.

[275] R. Van Overstraeten and H. De Man, "Measurement of the ionization rates in diffused silicon p-n junctions," *Solid-State Electronics,* vol. 13, pp. 583-608, 1970.

[276] P. Spirito, A. G. Strollo, and A. Caruso, "Two-dimensional analysis of the IV characteristics of normally-off bipolar-mode FET devices," *Solid-State Electronics,* vol. 33, pp. 1401-1417, 1990.

[277] J. H. Zhao, P. Alexandrov, J. Zhang, and X. Li, "Fabrication and characterization of 11-kV normally off 4H-SiC trenched-and-implanted vertical junction FET," *IEEE Electron Device Letters,* vol. 25, pp. 474-476, 2004.

[278] B. J. Baliga, *Power semiconductor devices*: PWS publishing company: New York City (USA), 1996.

[279] R. Malhan, Y. Takeuchi, M. Kataoka, A.-P. Mihaila, S. Rashid, F. Udrea, and G. Amaratunga, "Normally-off trench JFET technology in 4H silicon carbide," *Microelectronic engineering,* vol. 83, pp. 107-111, 2006.

[280] W. Saito, I. Omura, T. Ogura, and H. Ohashi, "Theoretical limit estimation of lateral wide band-gap semiconductor power-switching device," *Solid-State Electronics,* vol. 48, pp. 1555-1562, 2004.

[281] H. Kawarada, T. Yamada, D. Xu, Y. Kitabayashi, M. Shibata, D. Matsumura, M. Kobayashi, T. Saito, T. Kudo, and M. Inaba, "Diamond MOSFETs using 2D hole gas with 1700V breakdown voltage," in *Power Semiconductor Devices and ICs (ISPSD), 2016 28th International Symposium on*, Prague (Czech Republic) June 12–16, 2016, pp. 483-486.

[282] A. Ortiz-Conde, F. G. Sánchez, J. J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, "A review of recent MOSFET threshold voltage extraction methods," *Microelectronics Reliability,* vol. 42, pp. 583-596, 2002.

[283] J. Cañas, J. Piñero, F. Lloret, M. Gutierrez, T. Pham, J. Pernot, and D. Araujo, "Determination of alumina bandgap and dielectric functions of diamond MOS by STEM-VEELS," *Applied Surface Science,* vol. 461, pp. 93-97, 2018.

[284] M. Ogawa and T. Kamiya, "Correlation between the backgating effect of a GaAs MESFET and the compensation mechanism of a semi-insulating substrate," *IEEE Transactions on Electron Devices,* vol. 32, pp. 571-576, 1985.

[285] C. Lee, S. Lee, and B. Welch, "Carrier injection and backgating effect in GaAs MESFET's," *IEEE Electron Device Letters,* vol. 3, pp. 97-98, 1982.

[286] I. Ben-Yaacov, Y.-K. Seck, U. K. Mishra, and S. P. DenBaars, "AlGaN/GaN current aperture vertical electron transistors with regrown channels," *Journal of Applied Physics,* vol. 95, pp. 2073-2078, 2004.

[287] T. Nanjo, A. Imai, Y. Suzuki, Y. Abe, T. Oishi, M. Suita, E. Yagyu, and Y. Tokuda, "AlGaN channel HEMT with extremely high breakdown voltage," *IEEE Transactions on Electron Devices,* vol. 60, pp. 1046-1053, 2013.

[288] R. Hao, W. Li, K. Fu, G. Yu, L. Song, J. Yuan, J. Li, X. Deng, X. Zhang, and Q. Zhou, "Breakdown enhancement and current collapse suppression by high-resistivity GaN cap layer in normally-off AlGaN/GaN HEMTs," *IEEE Electron Device Letters,* vol. 38, pp. 1567-1570, 2017.

[289] T. Stiasny and R. Helbig, "Impurities in 4H and 6H SiC crystals, characterized by thermoluminescence and thermally stimulated conductivity," *SILICON CARBIDE AND RELATED MATERIALS 1995,* vol. 142, pp. 389-392, 1996.

[290] G. Pensl, V. Afanas' ev, M. Bassler, M. Schadt, T. Troffer, J. Heindl, H. Strunk, M. Maier, and W. Choyke, "Electrical properties of silicon carbide polytypes," in *Institute of Physics Conference Series*, 1996, pp. 275-280.

[291] A. Koizumi, J. Suda, and T. Kimoto, "Temperature and doping dependencies of electrical properties in Al-doped 4 H-Si C epitaxial layers," *Journal of Applied Physics,* vol. 106, p. 013716, 2009.

[292] S. Kagamihara, H. Matsuura, T. Hatakeyama, T. Watanabe, M. Kushibe, T. Shinohe, and K. Arai, "Parameters required to simulate electric characteristics of SiC devices for n-type 4H–SiC," *Journal of Applied Physics,* vol. 96, pp. 5601-5606, 2004.

[293] S. Rao, T. P. Chow, and I. Bhat, "Dependence of the ionization energy of Phosphorous Donor in 4H-SiC on Doping Concentration," in *Materials Science Forum, September 18-23, 2005 Pittsburgh*, pp. 597-600, Trans Tech Publications: Switzerland, 2006.

[294] P. Kozodoy, S. P. DenBaars, and U. K. Mishra, "Depletion region effects in Mg-doped GaN," *Journal of Applied Physics,* vol. 87, pp. 770-775, 2000.

[295] C. Seager, A. Wright, J. Yu, and W. Götz, "Role of carbon in GaN," *Journal of Applied Physics,* vol. 92, pp. 6553-6560, 2002.

[296] J.-P. Lagrange, A. Deneuville, and E. Gheeraert, "Activation energy in low compensated homoepitaxial boron-doped diamond films," *Diamond and Related Materials,* vol. 7, pp. 1390-1393, 1998.

[297] S. Koizumi, T. Teraji, and H. Kanda, "Phosphorus-doped chemical vapor deposition of diamond," *Diamond and Related Materials,* vol. 9, pp. 935-940, 2000.

[298] R. Samlenski, C. Haug, R. Brenn, C. Wild, R. Locher, and P. Koidl, "Incorporation of nitrogen in chemical vapor deposition diamond," *Applied Physics Letters,* vol. 67, pp. 2798-2800, 1995.

[299] K. Nishimura, K. Das, and J. Glass, "Material and electrical characterization of polycrystalline boron-doped diamond films grown by microwave plasma chemical vapor deposition," *Journal of Applied Physics,* vol. 69, pp. 3142-3148, 1991.

[300] F. Fontaine, "Calculation of the hole concentration in boron-doped diamond," *Journal of Applied Physics,* vol. 85, pp. 1409-1422, 1999.

[301] E. Gheeraert, S. Koizumi, T. Teraji, H. Kanda, and M. Nesladek, "Electronic states of phosphorus in diamond," *Diamond and Related Materials,* vol. 9, pp. 948-951, 2000.

[302] T. Kociniewski, J. Barjon, M. A. Pinault, F. Jomard, A. Lusson, D. Ballutaud, O. Gorochov, J. Laroche, E. Rzepka, and J. Chevallier, "n-type CVD diamond doped with phosphorus using the MOCVD technology for dopant incorporation," *physica status solidi (a),* vol. 203, pp. 3136-3141, 2006.

[303] G. Wachutka, "Consistent treatment of carrier emission and capture kinetics in electrothermal and energy transport models," *Microelectronics Journal,* vol. 26, pp. 307-315, 1995.

[304] A. Schenk, "A model for the field and temperature dependence of Shockley-Read-Hall lifetimes in silicon," *Solid-State Electronics,* vol. 35, pp. 1585-1596, 1992.

[305] M. Lax, "Cascade capture of electrons in solids," *Physical Review,* vol. 119, p. 1502, 1960.

[306] G. Hurkx, D. Klaassen, and M. Knuvers, "A new recombination model for device simulation including tunneling," *IEEE Transactions on Electron Devices,* vol. 39, pp. 331-338, 1992.

[307] L. Colalongo, M. Valdinoci, G. Baccarani, P. Migliorato, G. Tallarida, and C. Reita, "Numerical analysis of poly-TFTs under off conditions," *Solid-State Electronics,* vol. 41, pp. 627-633, 1997.

[308] A. Palma, J. Jiménez-Tejada, A. Godoy, and J. Carceller, "Monte Carlo Simulation of Carrier Capture at Deep Centers for Silicon and Gallium Arsenide Devices," in *Simulation of Semiconductor Devices and Processes*, ed: Springer, 1995, pp. 380-383, Nuremberg September 6-8 (1995).

[309] P. P. Altermatt, A. Schenk, and G. Heiser, "A simulation model for the density of states and for incomplete ionization in crystalline silicon. I. Establishing the model in Si: P," *Journal of Applied Physics,* vol. 100, p. 113715, 2006.

[310] A. Schenk, P. P. Altermatt, and B. Schmithusen, "Physical model of incomplete ionization for silicon device simulation," in *2006 International Conference on Simulation of Semiconductor Processes and Devices*, 2006, pp. 51-54, Monterey, September 6-8, 2006.

[311] H. Steinkemper, M. Rauer, P. Altermatt, F. D. Heinz, C. Schmiga, and M. Hermle, "Adapted parameterization of incomplete ionization in aluminum-doped silicon and impact on numerical device simulation," *Journal of Applied Physics,* vol. 117, p. 074504, 2015.

[312] Y. Koide, "Peculiarity of depletion region in diamond p-n-junction," *Japanese Journal of Applied Physics,* vol. 42, p. 6800, 2003.

[313] W. Kaindl, M. Lades, N. Kaminski, E. Niemann, and G. Wachutka, "Experimental characterization and numerical simulation of the electrical properties of nitrogen, aluminum, and boron in 4H/6H-SiC," *Journal of Electronic Materials,* vol. 28, pp. 154-160, 1999.

[314] A. V. Los and M. S. Mazzola, "Influence of carrier freeze-out on SiC Schottky junction admittance," *Journal of Electronic Materials,* vol. 30, pp. 235-241, 2001.

[315] H. Wang, E. Napoli, and F. Udrea, "Breakdown voltage for superjunction power devices with charge imbalance: An analytical model valid for both punch through and non punch through devices," *IEEE Transactions on Electron Devices,* vol. 56, pp. 3175-3183, 2009.

[316] H. Niwa, J. Suda, and T. Kimoto, "Temperature dependence of impact ionization coefficients in 4H-SiC," in *Materials Science Forum,*, 2014, pp. 461-466, Trans Tech Publications: Switzerland.

[317] T. Hatakeyama, T. Watanabe, T. Shinohe, K. Kojima, K. Arai, and N. Sano, "Impact ionization coefficients of 4 H silicon carbide," *Applied Physics Letters,* vol. 85, pp. 1380-1382, 2004.

[318] C. Canali, G. Majni, R. Minder, and G. Ottaviani, "Electron and hole drift velocity measurements in silicon and their empirical relation to electric field and temperature," *IEEE Transactions on Electron Devices,* vol. 22, pp. 1045-1047, 1975.

[319] D. Disney and G. Dolny, "JFET depletion in superjunction devices," in *Power Semiconductor Devices and IC's, 2008. ISPSD'08. 20th International Symposium on*, 2008, pp. 157-160.

[320] M. Lades, W. Kaindl, N. Kaminski, E. Niemann, and G. Wachutka, "Dynamics of incomplete ionized dopants and their impact on 4H/6H-SiC devices," *IEEE Transactions on Electron Devices,* vol. 46, pp. 598-604, 1999.

[321] L. Efthymiou, G. Camuso, G. Longobardi, T. Chien, M. Chen, and F. Udrea, "On the Source of Oscillatory Behaviour during Switching of Power Enhancement Mode GaN HEMTs," *Energies,* vol. 10, p. 407, 2017.

[322] Cree. (2016). *Z-Rec® Rectifier* [Datasheet] , C3D02060E Silicon Carbide SchottkyDiode,Available:https://www.wolfspeed.com/downloads/dl/file/id/116/product/82/c3d02060e.pdf , Accessed on 31/10/2019 .

[323] Rohm Semiconductor, "SiC Power Devices and Modules—Application Note, http://rohmfs.rohm.com/en/products/databook/applinote/discrete/sic/common/sic_appli-e.pdf, accessed on 31/10/2019," *Issue of August,* 2014.

[324] K. Kells and H. Baltes, "General electrothermal semiconductor device simulation," ETH Zurich, 1994, Ph.D. Dissertation.

[325] G. K. Wachutka, "Rigorous thermodynamic treatment of heat generation and conduction in semiconductor device modeling," *IEEE transactions on computer-aided design of integrated circuits and systems,* vol. 9, pp. 1141-1149, 1990.

[326] L. Yu and K. Sheng, "Modeling and optimal device design for 4H-SiC super-junction devices," *IEEE Transactions on Electron Devices,* vol. 55, pp. 1961-1969, 2008.

[327] E. Arnold, "Charge-sheet model for silicon carbide inversion layers," *IEEE Transactions on Electron Devices,* vol. 46, pp. 497-503, 1999.

[328] C. Raynaud, "Calculation of theoretical capacitance–voltage characteristics of 6H–SiC metal–oxide–semiconductor structures," *Journal of Applied Physics,* vol. 88, pp. 424-428, 2000.

[329] N. Hizem, A. Fargi, A. Kalboussi, and A. Souifi, "Analysis of the relationship between the kink effect and the indium levels in MOS transistors," *Materials Science and Engineering: B,* vol. 178, pp. 1458-1463, 2013.

[330] P. Bouillon, R. Gwoziecki, T. Skotnicki, J. Alieu, and P. Gentil, "Universal impurity ionization parameters in MIS CV freeze-out characteristics and direct extraction of surface doping concentration," *IEEE Transactions on Electron Devices,* vol. 47, pp. 871-877, 2000.

[331] K. Ebihara, K. Kawahara, H. Watanabe, S. Nakata, and S. Yamakawa, "The effect of incomplete ionization on SiC devices during high speed switching," in *Materials Science Forum*, 2017, pp. 467-470, Trans Tech Publ: Switzerland.

[332] E. Van Brunt, G. Wang, J. Liu, V. Pala, B. Hull, J. Richmond, and J. Palmour, "Operation of 4H-SiC Schottky diodes at dV/dt values over 700 kV/μs," in *2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2016, pp. 67-70, Prague (Czech Republic) June 12–16.

[333] A. Hopkins, N. McNeill, P. Anthony, and P. Mellor, "Figure of merit for selecting super-junction MOSFETs in high efficiency voltage source converters," in *Energy Conversion Congress and Exposition (ECCE), 2015 IEEE*, 2015, pp. 3788-3793, Montreal 20-24 September.

[334] I.-J. Kim, S. Matsumoto, T. Sakai, and T. Yachi, "New power device figure of merit for high-frequency applications," in *Power Semiconductor Devices and ICs, 1995. ISPSD'95., Proceedings of the 7th International Symposium on*, 1995, pp. 309-314, Yokohama 23-25 May

[335] T. Kimoto and Y. Yonezawa, "Current status and perspectives of ultrahigh-voltage SiC power devices," *Materials Science in Semiconductor Processing,* 78 (2018): 43-56, 2017.

[336] T. Kimoto, "Material science and device physics in SiC technology for high-voltage power devices," *Japanese Journal of Applied Physics,* vol. 54, p. 040103, 2015.

[337] G. Perez, J. Letellier, A. l. Maréchal, D. Eon, G. Chicot, P.-O. Jeannin, N. Rouger, and J.-L. Schanen, "Diamond Schottky barrier diodes for power electronics applications," presented at the ECCE, Oregon(USA), September 2018.

[338] V. Dos Santos, B. Cougo, N. Roux, B. Sareni, B. Revol, and J.-P. Carayon, "Trade-off between Losses and EMI Issues in Three-Phase SiC Inverters for Aircraft Applications," in *Electromagnetic Compatibility & Signal/Power Integrity (EMCSI), 2017 IEEE International Symposium on*, 2017, pp. 55-60, Gaithersburg 8-12 April (2017).

[339] ((2018)). *GaN Systems Inc ,GN001 Application Guide Design with GaN Enhancement mode HEMT, https://gansystems.com/wp-content/uploads/2018/02/GN001_Design_with_GaN_EHEMT_180228-1.pdf, accessed on 31/10/2019* [Datasheet].

[340] T. Funaki, "6.1 Switching behavior of diamond devices and prospective applications in power electronics," *Power Electronics Device Applications of Diamond Semiconductors,* pp. 383-400, 2018.

[341] T. Funaki, M. Hirano, H. Umezawa, and S. Shikata, "High temperature switching operation of a power diamond Schottky barrier diode," *IEICE Electronics Express,* vol. 9, pp. 1835-1841, 2012.

[342] T. Funaki, K. Kodama, H. Umezawa, and S. Shikata, "Characterization of fast switching capability for diamond Schottky barrier diode," in *Materials Science Forum*, 2011, pp. 820-823, Trans Tech Publ: Switzerland.

[343] J. Kolar, F. Krismer, Y. Lobsiger, J. Muhlethaler, T. Nussbaumer, and J. Minibock, "Extreme efficiency power electronics," in *Integrated Power Electronics Systems (CIPS), 2012 7th International Conference on*, 2012, pp. 1-22, Nuremberg, March 6-8 (2012).

[344] X. C. Tong, *Advanced materials for thermal management of electronic packaging* vol. 30: Springer Science & Business Media: Berlin, 2011.

[345] L. Cao, J. Wang, G. Harden, H. Ye, R. Stillwell, A. J. Hoffman, and P. Fay, "Experimental characterization of impact ionization coefficients for electrons and holes in GaN grown on bulk GaN substrates," *Applied Physics Letters,* vol. 112, p. 262103, 2018.

[346] M. E. Levinshtein, S. L. Rumyantsev, and M. S. Shur, *Properties of Advanced Semiconductor Materials: GaN, AIN, InN, BN, SiC, SiGe*: John Wiley & Sons: New York (USA), 2001.

[347] L. Zhu and T. P. Chow, "Analytical modeling of high-voltage 4H-SiC junction barrier Schottky (JBS) rectifiers," *IEEE Transactions on Electron Devices,* vol. 55, pp. 1857-1863, 2008.

[348] J. He, X. Zhang, Y. Wang, and X. Xi, "Optimum design of punch-through junction used in bipolar and unipolar high voltage power devices," *Solid-State Electronics,* vol. 46, pp. 847-851, 2002.