Subthreshold Schottky-barrier thin film transistors with ultralow power and high intrinsic gain

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Abstract (<125 words): The quest for low power becomes highly compelling in newly emerging application areas related to wearable devices in the Internet of Things. Here, we report on a Schottky-barrier In-Ga-Zn-O thin-film transistor operating in the deep sub-threshold regime (i.e., near the OFF-state) at low supply voltages (< 1 volt) and ultra low power (< 1 nanowatt). By using a Schottky-barrier at the source and drain contacts, the current-voltage characteristics of the transistor were virtually channel-length independent with an infinite output resistance. It exhibited high intrinsic gain (> 400) that was both bias- and geometry-independent. The transistor reported here is useful for sensor interface circuits in wearable devices where high current sensitivity and ultra low power are vital for battery-less operation.

One Sentence Summary: A thin film transistor in the almost OFF-state with ultra low power and high signal amplification for battery-less operation in wearables.

Main Text (<2000 words): Thin-film transistors (TFTs) based on amorphous oxide semiconductors (AOSs), such as indium-gallium-zinc-oxide (i.e. In-Ga-Zn-O or IGZO), have been shown to be a highly promising candidate for large-area electronics because of their high mobility, low-temperature processability, and wide band-gap, hence high transparency and low OFF-current, compared with the ubiquitous silicon thin-film technology and more recently the organic family (1-8). For deployment of TFTs in mobile devices, such as wearables, low voltage and low power are crucial since the operation of the wearable device is challenged by the limited battery lifetime even if it is augmented with energy harvesting (9-12). Other TFT technologies are unlikely to meet these requirements because of their higher quiescent power (table S2) (1-8, 13-16).

The approach used here to achieve ultra low-power is to operate the transistor in the deep sub-threshold regime, i.e., near the OFF-state. Within this regime, the saturation drain current (I_{DS}) of the Schottky-barrier (SB) TFT is independent of drain voltage (V_{DS}), yielding an infinite output resistance (i.e., $r_o = \partial V_{DS}/\partial I_{DS} \rightarrow \infty$). Indeed, the magnitude of the current is scaled geometrically only by the channel width (W) as opposed to the ratio of channel width-to-length (W/L) as in conventional transistors (see inset of Fig.1B). The insulated gate provides an effective means of modulating the SB height at the source contact and hence the thermionic emission (TE) and thermionic field emission (TFE) properties. Thus, the emission current into the channel is determined by the reverse saturation current of the Schottky diode at the source, which in turn is modulated by the gate voltage. As a result, the SB-TFT yields a large intrinsic gain that is independent of both geometry and bias. This bias independence of intrinsic gain and zero input current by virtue of the insulated gate makes the SB-TFT, operating near the OFF-state, capture the best of the bipolar junction transistor (BJT) and metal-oxide-semiconductor field-effect transistor (MOSFET) technology families (table S4) (16-18).

In order to form a Schottky contact at the source/drain contact of the IGZO TFT, we decreased the electron concentration of the IGZO film by using a high oxygen-gas partial pressure against argon-gas, i.e., $P_{ox} = O_2/(O_2 + Ar)$, during the RF sputtering process, with subsequent thermal annealing for a more reliable contact (Fig.1A, fig.S1). Here, a high P_{ox} was a means to compensate oxygen vacancies (V_{ox}) which act as electron donors (7,19,20). Indeed, in the measured output characteristics, the MC-IGZO TFT (at P_{ox} = 15%) provided Schottky characteristics at low V_{DS} whereas the LC-IGZO TFT (at P_{ox} = 4%) showed the usual ohmic behaviour (fig.S2). At higher V_{DS}, both devices show current saturation (Fig.1B). More importantly, the SB-TFT (i.e., MC-IGZO TFT) has a much flatter output curvature compared to the ohmic device, yielding a much higher r_o. In particular, the output characteristics of the ohmic device had a L-dependence (fig.S4). In contrast, the output characteristics of the SB-TFT were almost independent on L (Fig.1B). This can be explained with the saturation drain-current (I_{sat}) relation as (21-23),

$$I_{sat} = A_J J_{sat}(V_{GS}) \exp\left(-\frac{\varphi_{B0}}{v_{th}}\right)\left(1-\exp\left(-\frac{V_{DS}}{n v_{th}}\right)\right), \quad (1)$$

where n is the ideality factor (~ 1.7 of the examined device), A_J the contact area where electrons are emitted through TE-TFE rather than the drift-diffusion process, v_{th} the thermal voltage (i.e., $k_B T/q$, where k_B is Boltzmann's constant, T the absolute temperature, and q the elementary charge), and J_{sat} the saturation current density as a function of a gate voltage (V_{GS}). Note that I_{sat} is linearly proportional to A_J, and scales with W. In addition, the term $(1-\exp(-V_{DS}/nv_{th}))$ is almost unity in the saturation regime since $V_{DS} >> nv_{th}$ at 300 K, thus independent of V_{DS}. These are consistent with the results in Fig.1B. Besides, Figs.1C-1E show input characteristics, in which a conceptual colour-bar of output power-consumption (P_{out}) for 1-volt-supply, normalized with W, is shown, clearly indicating each operational regime (Fig.1F). In particular, as seen in Fig.1D, the SB-TFT has a higher transconductance (g_m). This can be explained with its smaller SS ~ 0.28 V/dec compared to the ohmic device (Fig.1D, fig.S2, table S1). Since the intrinsic gain (A_i) of a transistor is defined as $g_m r_o$, the SB-TFT provides a higher A_i associated with its higher r_o and g_m compared to the ohmic device (table S3).

To theoretically explain the results of the SB-TFT, we describe its operating principle is described in Fig.2. At a given V_{GS}, the non-linear response of the drain current at V_{DS} < the transition voltage (V_{tran}) suggests a forward-biased Schottky diode at the drain junction (Fig.2A). Here, the electron emission is modulated with V_{GS} through an effective SB-lowering at the drain side ($\Delta\varphi_{BD}$) (Fig.2B). When $V_{DS} > V_{tran}$, I_{DS} becomes firmly saturated because of the reverse-biased Schottky diode at the source (Fig.2C). Note that this regime satisfies the condition of $L >> W_D$, suggesting a negligible image-charge effect from the drain to source, where W_D is the depletion width at the drain (Fig.2C, fig.S5A). Thus, the SB-lowering at the source ($\Delta\varphi_{BS}$) is mainly a function of V_{GS} modulating the current density expressed as,

$$J_{sat}(V_{GS}) = J_0 \exp\left(\frac{\Delta\varphi_{BS}(V_{GS})}{v_{th}}\right). \quad (2)$$

Here, J_0 is a reference current density. As seen in Fig.2D, the intercept ($\Delta\varphi_0$) ~ 0.165 volt can be considered as an initial SB-lowering corresponding to the reference current level at V_{GS} = the reference voltage (V_{ref}). Note that an effective SB-lowering (e.g. $\Delta\varphi_{BS}$) approximation is used to account for changes in the SB-width (W_S) and hence, the degree of the quantum mechanical tunneling (fig.S5C) (23).

Based on the theory discussed with Fig.2, the output characteristics of the SB device for different V_{GS} (ranging from 0 to 1 volt, in steps of 0.1 volts) were measured (movie S1) and modeled (Fig.3A). It shows good agreement with each other. Fig.3B shows the transfer characteristics for V_{DS} of 0.5 volts and 1 volt. They are virtually identical, implying current saturation for $V_{DS} > V_{tran} \sim 0.48$ volts. Also, it shows an exponential dependency on V_{GS}, which can be explained with Eq.2 where $\Delta\varphi_{BS}(V_{GS}) = \zeta_0(V_{GS}\text{-}V_{ref}) + \Delta\varphi_0$. Note that ζ_0 is a coefficient that describes the sensitivity of barrier lowering to V_{GS}. The retrieved r_o and g_m for V_{DS} = 1 volt are shown as a function of V_{GS} (Fig.3C). Both follow an exponential law with an opposite proportionality on V_{GS}, as described in Eqs.3 and 4. Their product gives a signal amplification factor, i.e. intrinsic gain (A_i):

$$r_o = n\frac{v_{th}}{A_J J_{B0}}\exp\left(\frac{-\zeta_0(V_{GS}-V_{ref})-\Delta\varphi_0}{v_{th}}\right)\exp\left(\frac{v_{sat}}{nv_{th}}\right), \tag{3}$$

$$g_m = \zeta_0\frac{A_J J_{B0}}{v_{th}}\exp\left(\frac{\zeta_0(V_{GS}-V_{ref})+\Delta\varphi_0}{v_{th}}\right), \tag{4}$$

$$A_i = \zeta_0 n\exp\left(\frac{v_{sat}}{nv_{th}}\right), \tag{5}$$

where $J_{B0} = J_0\exp(-\varphi_{B0}/v_{th})$ (eqs.S17-S21). As seen in Eq.5, A_i is not a function of either bias (e.g., V_{GS}, V_{DS}) or geometry (e.g., W and L), but a function of intrinsic parameters (e.g., ζ_0, n, v_{th}, and a saturation voltage v_{sat}). So, it is just a constant unlike the ohmic device. With Eq.5, A_i is calculated as ~ 450 with the retrieved values of intrinsic parameters (fig.S6), which is consistent with measurements (Fig.3D). Here, A_i of the SB-TFT is at least an order of magnitude higher compared to the ohmic IGZO TFT (table S3) and a typical Si-MOSFET (17,18). Because the SB-TFT operates at low voltage and low current, it is also electrically stable for over time (fig.S7). The low-power and high-gain performance of the SB-TFTs were applied to a common source amplifier as demonstrated in Fig.4 (movie S1). As seen in Figs.4A and 4B, the TFT-2 (load), whose V_{ref} was shifted to negative because of light stress, was used as a depletion load (fig.S8) (24). Alternatively, a TFT with a larger W as a design parameter can also be employed (fig.S9A). As shown in Fig.4D, the circuit exhibits a high voltage gain (A_V) > 220, and its output-power consumption (P_{out}) is very low < 150 picowatts (Fig.4D and 4F). Thus, it can even be driven by a nano-watt power source.

Our deep sub-T operating SB-TFT is fundamentally an ultra low-power and high-gain device which opens up possibilities for innovative system design in many applications, including wearables and implantable devices, where low power and low current analog signal-processing are essential requirements. In addition, the operating principle of the SB-TFT in the deep sub-T regime (i.e., near-OFF-state) brings together the best of two transistor families: the bias independence of gain of the BJT and zero input current of the MOSFET (table S4). Thus, the SB-TFT will bring about a new design paradigm for near-OFF-state sensor interfaces and analog front-end circuits (figs.S10-S12).

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Figure Legends:

Fig.1. Device structure and basic electrical characteristics. (**A**) Schematic cross-section of the examined device (inset: schematic illustrations of atomic structures for less compensated (LC) - and more compensated (MC) - IGZO films, respectively). (**B**) Measured I_{DS}/W vs. V_{DS} for MC and LC devices (inset: I_{DS}/W *vs.* L). Measured input characteristics of each device: (**C**) in linear-scale indicating the threshold voltage (V_T), and (**D**) in log-scale indicating V_{ref}, respectively (I_G is a gate leakage current). (**E**) Measured g_m/W of each device along with the ratio between them. (**F**) Conceptual colour-bar of P_{out} normalized with W for 1 V supply.

Fig.2. Operating principle of the deep sub-T SB-TFT. (**A**) Band diagram along L when $V_{DS} < V_{tran}$. Inset: an equivalent circuit representation. (**B**) Retrieved $\Delta\varphi_{BD}$ at drain contact as a function of V_{GS} calibrated with V_{ref}, i.e. V_{GS}-V_{ref}. (**C**) Band diagram along L when $V_{DS} > V_{tran}$. Inset: an equivalent circuit representation. (**D**) Extracted $\Delta\varphi_{BS}$ at source contact as a function of V_{GS} -V_{ref}. Here, E_C and E_F denote the conduction band minima and Fermi level, respectively.

Fig.3. Modulation characteristics and small signal parameters of the SB-TFT in the deep sub-T regime. (**A**) Measured I_{DS} vs. V_{DS} for a different V_{GS} along with theory. Here, V_0 is a threshold at which the source-side Schottky diode starts dominating. (**B**) Transfer characteristics for V_{DS} = 0.5 and 1 V. (**C**) Experimental values of r_o and g_m as a function of V_{GS} along with theory (dot lines). (**D**) Measured A_i of the SB-TFT as a function of V_{GS}.

Fig.4. Circuit-level demonstrations with the presented SB-TFTs. (**A**) Transfer characteristics of TFT-1 (driver) and TFT-2 (depletion load due to light stress), where I_B and V_B are determined as ~90 pA and ~0.5 V, respectively. (**D**) Common-source circuit diagram and its 3-D view. (**C**) Measured output voltage (V_{out}) as a function of input voltage (V_{in}) while using 2 V supply (V_{DD}), (**D**) A_V, (**E**) output current (I_{out}), and (**F**) P_{out} vs. V_{in}, respectively.

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Supplementary Materials:

Materials and Methods

Supplementary Text

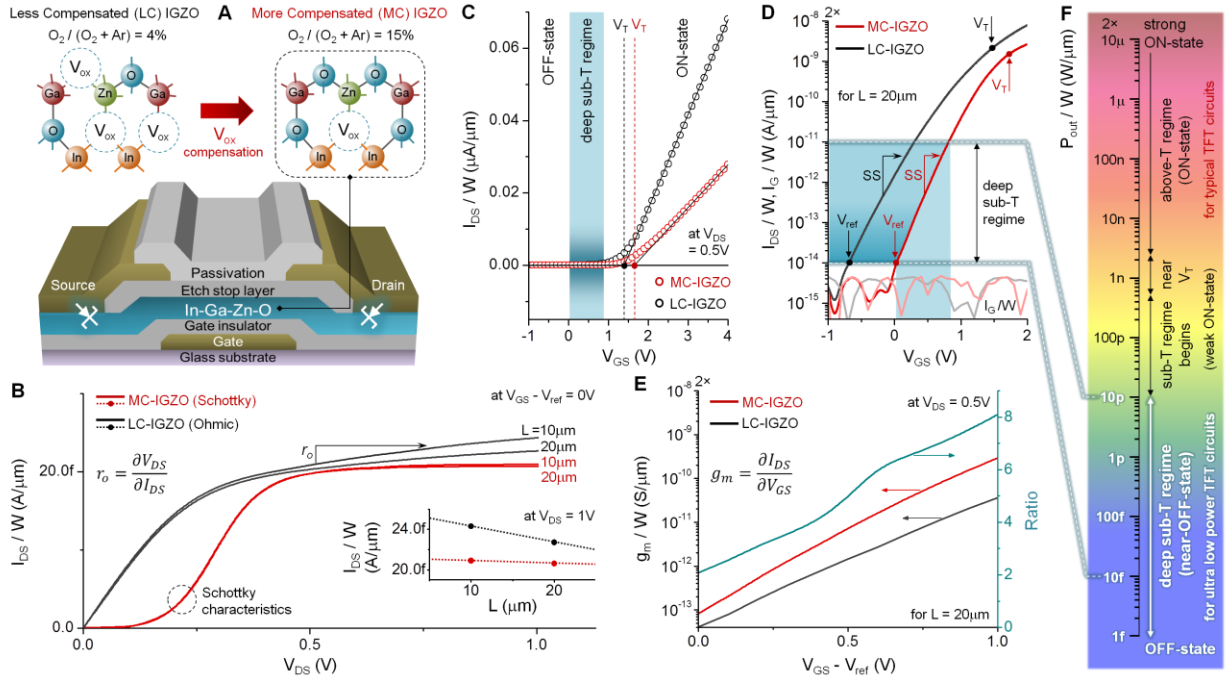
Figures S1-S12

Tables S1-S4

Movies S1-S2

References (25-38)

Figure 1:



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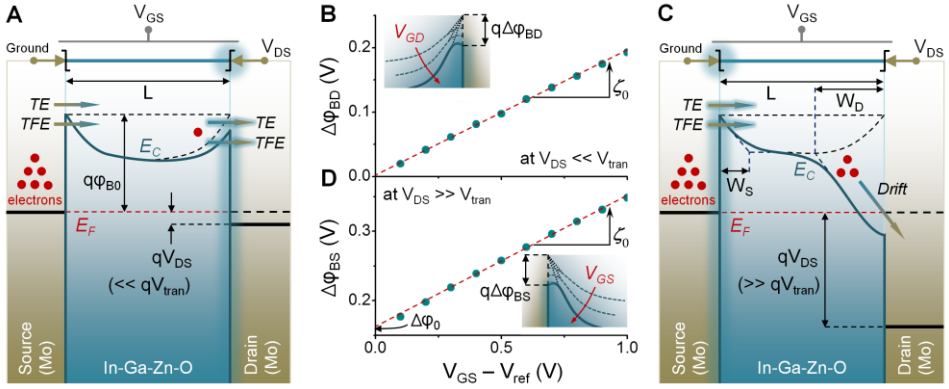

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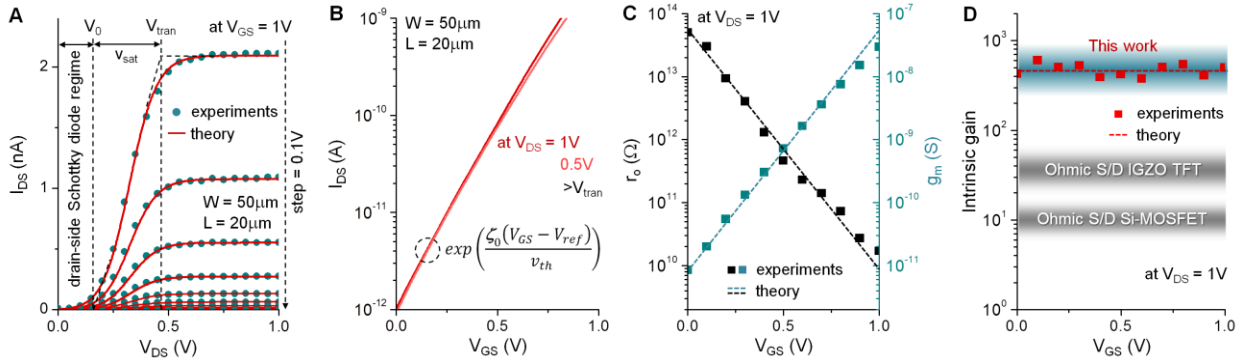

Figure 4: