A Novel DC-DC Converter for Photovoltaic Applications

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This dissertation is submitted for the degree of

Doctor of Philosophy

Corpus Christi College September 2018

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Abstract

Growing concerns about climate change have led to the world experiencing an unprecedented push towards renewable energy. Economic drivers and government policies mean that small, distributed forms of generation, like solar photovoltaics, will play a large role in our transition to a clean energy future. In this thesis, a novel DC-DC converter known as the 'Coupled Inductors Combined Cuk-SEPIC' (CI-CCS) converter is explored, which is particularly attractive for these photovoltaic applications. A topological modification is investigated which provides several benefits, including increased power density, efficiency, and operational advantages for solar energy conversion.

The converter, which is based on the combination of the Cuk and SEPIC converters, provides a bipolar output (i.e. both positive and negative voltages). This converter also offers both step-up and step-down capabilities with a continuous input current, and uses only a single, ground-referenced switching device. A significant enhancement to this converter is proposed: magnetic coupling of the converter's three inductors. This can substantially reduce the CI-CCS converter's input current ripple – an important benefit for maximum power point tracking (MPPT) in photovoltaic applications. The effect of this coupling is examined theoretically, and optimisations are performed – both analytically and in simulations – to inform the design of a 4 kW prototype CI-CCS converter, switched at a high frequency (100 kHz) with a silicon carbide (SiC) MOSFET. Simulation and experimental results are then presented to demonstrate the CI-CCS converter's operation and highlight the benefits of coupling its inductors. An efficiency analysis is also undertaken and its sources of losses are quantified.

The converter is subsequently integrated into a domestic photovoltaic system to provide a practical demonstration of its suitability for such applications. MPPT is integrated into the CI-CCS DC-DC converter, and a combined half bridge/T-type DC-AC converter is developed and paired with the CI-CCS converter to form an entirely transformerless single-phase solar energy conversion system. The combination of the CI-CCS converter's bipolar DC output with the combined half bridge/T-type converter's bipolar DC input allows grounding at both the photovoltaic panels and the AC grid's neutral point. This eliminates high frequency common mode voltages from the PV array, which in turn prevents leakage currents. The entire system can be operated in grid-connected mode - where the objective is to maximise power extracted from the photovoltaic system, and is demonstrated in stand-alone mode - where the objective is to match solar generation with the load's power demands.

Declaration

This dissertation is the result of my own work and includes nothing which is the outcome of work done in collaboration except as declared in the Preface and specified in the text.

It is not substantially the same as any that I have submitted, or, is being concurrently submitted for a degree or diploma or other qualification at the University of Cambridge or any other University or similar institution except as declared in the Preface and specified in the text. I further state that no substantial part of my dissertation has already been submitted, or, is being concurrently submitted for any such degree, diploma or other qualification at the University of Cambridge or any other University or similar institution except as declared in the Preface and specified in the text.

It does not exceed the prescribed word limit for the Engineering Degree Committee.

Kumaran Saenthan Nathan

September 2018

Acknowledgements

This PhD has been made possible with the support of a number of people, and it's my pleasure to convey my appreciation to them in this humble acknowledgement.

First and foremost, I'd like to express my sincere gratitude to my academic supervisor, Dr Teng Long. Without your invaluable expertise, encouragement, and patience, this PhD would not have been possible. Your guidance at all hours has allowed me to spend my time efficiently and produce the best work I am capable of.

Next, I would like to thank the co-authors on my publications, all the members in my research group, and the workshop staff, for the stimulating discussions, brainstorming sessions, encouragement, and assistance in the lab during the course of this degree. There is one person in particular who merits a special mention – Saikat Ghosh. I have learned an incredible amount from you, and without your help this thesis would still be a distant target. I'll certainly miss working with you in the future.

Many thanks also go to my sponsors — the General Sir John Monash Foundation, the Origin Foundation, the Cambridge Trust, Cambridge Australia Scholarships, and Mr Charles Allen. You have enabled an incredible journey for me academically, professionally, and personally. My time in Cambridge has been transformative, and it would not have been possible without your generosity.

Outside of the academic sphere, there have been countless people in Cambridge who have made the past four years truly memorable. My ice hockey teammates have been a cornerstone of my time in Cambridge. It has been an honour and privilege to battle alongside you on the ice. Outside of hockey, I've learned so much from each and every one of you. We've made countless incredible memories and I can't wait to see what the future has in store for us.

My friends from Corpus Christi College have also been a defining feature of my life here. I've been lucky to live with such an amazing group of people. The toughest

times in Cambridge were made bearable knowing that I'd come home to a flat full of friends every night. From our quiet dinners at home to our exciting travels abroad, the experiences we've shared will forever be cherished.

To the other incredibly special people I've met here – you know who you are. You've made my years in Cambridge some of the best in my life. I'll forever be grateful that our paths crossed during our transient time in this beautiful city. My life is indescribably better for having had you in it.

Unfortunately, some of the most amazing people in my life are on the other side of the world. To my friends back in Australia, I've missed you. It's been tough being away from you for so long, and seeing your lives continue without me. I've often regretted not being better at staying in touch, though I've always appreciated that when I come home it feels like not a day has passed. I can't wait to be back home and see you all again.

And to the most important people of all – my mum, my dad, and my brother. Thanks for always being there for me – not only during my PhD, but throughout my life. I'm proud of the person that I am, and that's undoubtedly a result of how your influences have shaped me.

List of Publications

During my PhD I have authored or co-authored the publications listed here. Note that the *Journal of Engineering* articles are associated with the papers presented at *The 9th International Conference on Power Electronics, Machines and Drives (PEMD 2018)*.

Journal Articles

- **K. S. Nathan**, S. S. Ghosh, Y. P. Siwakoti, and T. Long, "A New DC-DC Converter for Photovoltaic Systems: Coupled-Inductors Combined Cuk-SEPIC Converter," *IEEE Transactions on Energy Conversion*, 2018
- **K. S. Nathan**, S. S. Ghosh, P. R. Tripathi, Y. P. Siwakoti, T. J. Flack, X. Li, and T. Long, "Benefits of the Coupled Inductors Combined Cuk-SEPIC (CI-CCS) Converter," *Journal of Engineering*, 2018
- S. S. Ghosh, **K. S. Nathan**, Y. P. Siwakoti, and T. Long, "Dual Polarity DC-DC Converter Integrated Grid-tied Single-Phase Transformer Less Inverter for Solar Application," *Journal of Engineering*, 2018
- T. Long, S. S. Ghosh, **K. S. Nathan**, M. Southall, and M. Louati, "Derivation and analysis of a novel bi-directional non-isolated multi-level DC-DC (MLDC) converter," *Journal of Engineering*, 2018

Conference Proceedings

- **K. S. Nathan**, S. S. Ghosh, P. R. Tripathi, Y. P. Siwakoti, T. J. Flack, X. Li, and T. Long, "Benefits of the Coupled Inductors Combined Cuk-SEPIC (CI-CCS) Converter," in *The 9th International Conference on Power Electronics, Machines and Drives (PEMD 2018)*, April 2018

- S. S. Ghosh, **K. S. Nathan**, Y. Siwakoti, and T. Long, "Dual Polarity DC-DC Converter Integrated Grid-tied Single-Phase Transformer Less Inverter for Solar Application," in *The 9th International Conference on Power Electronics, Machines and Drives (PEMD 2018)*, April 2018

- T. Long, S. S. Ghosh, **K. S. Nathan**, M. Southall, and M. Louati, "Derivation and analysis of a novel bi-directional non-isolated multi-level DC-DC (MLDC) converter," in *The 9th International Conference on Power Electronics, Machines and Drives (PEMD 2018)*, April 2018

- S. S. Ghosh, **K. S. Nathan**, P. R. Tripathi, Y. P. Siwakoti, and T. Long, "Single Phase Integrated Cuk Transformerless SiC Inverter for Grid-Connected PV Systems," in *IEEE Workshop on Wide Bandgap Power Devices and Applica- tions in Asia (WiPDA Asia 2018)*, May 2018

"We are at the very beginning of time for the human race. It is not unreasonable that we grapple with problems. But there are tens of thousands of years in the future. Our responsibility is to do what we can, learn what we can, improve the solutions, and pass them on."

— Richard P. Feynman

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Nomenclature

AC	Alternating Current
ADC	Analog-to-Digital converter
C	Capacitance
C_C	Cuk Transfer Capacitor
CCM	Continuous Conduction Mode
CCS	Combined Cuk-SEPIC (converter)
CI-CCS	Coupled Inductor Combined-Cuk SEPIC (converter)
C_N	Negative Output Capacitor
C_P	Positive Output Capacitor
C_S	SEPIC Transfer Capacitor
CV	Constant Voltage
DAC	Digital-to-Analog converter
D_C	Cuk Output Diode
DC	Direct Current
DCM	Discontinuous Conduction Mode
D	Duty cycle
DPP	Differential Power Processing

D_S	SEPIC Output Diode
DSP	Digital Signal Processing
DSR	Demand Side Response
DTS	Distributed Temperature Sensing
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
ESS	Energy Storage System
EV	Electric Vehicle
f_s	Switching Frequency
GaN	Gallium Nitride
HERIC	Highly Efficient and Reliable Inverter Concept
IC	Incremental Conductance, or Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
i_{load}	Load currents
IPC	Association Connecting Electronics Industries, formerly the Institute for Printed Circuits
i_{source}	Source currents
k	Coupling factor
L_C	Cuk Inductor
L_{in}	Input Inductor
L	Inductance
LOM	Loss of Mains (Protection)
L_S	SEPIC Inductor

MCU	Microcontroller
MIC	Module Integrated Converter
MLPE	Module-Level Power Electronics
M	Mutual inductance
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
NPC	Neutral-Point Clamped
PCB	Printed Circuit Board
PCC	Point of Common Coupling
PID	Potential Induced Degradation
P_{in}	Input power
PLL	Phase-Locked Loop
P&O	Perturb & Observe
P_{out}	Output power
PV	Photovoltaics
PWM	Pulse-Width Modulation
RCD	Residual Current Device
RCMU	Residual Current Monitoring Unit
rms	Root Mean Square
SAR	Successive Approximation Register
SDFM	Sigma-Delta Filter Module
SDM	Single Diode Model

SEPIC	Single-Ended Primary-Inductor Converter
SiC	Silicon Carbide
SMPS	Switched-Mode Power Supply
STC	Standard Test Conditions
THD	Total Harmonic Distortion
T_s	Switching period
UNFCCC	United Nations Framework Convention on Climate Change
V2G	Vehicle-to-Grid
V_{AC}	AC grid voltage
VAr	Volt-Ampere reactive
V_{DC}	DC bus voltage
V_{in}	Input voltage
V_{NEG}	Negative terminal output voltage
V_{PCC}	AC bus voltage at the point of common coupling
V_{POS}	Positive terminal output voltage
V_{PV}	Photovoltaic array voltage
VSC	Voltage Source Converter
WBG	Wide-Bandgap

Chapter 1

Motivation and Objectives

This chapter provides a brief history of energy usage to provide context to the challenges presently faced by the energy industry and to establish the importance of this thesis. The chapter then provides a brief explanation of the changes that are currently taking place to address some of the presently identified major issues. Next, the objectives of this thesis are stated with an explanation of how these aims address the aforementioned obstacles, and how the work fits into the broader context of research in this area. Finally, the chapter concludes with an outline of the structure of this thesis.

1.1 The Path to Now

1.1.1 The World Before Electricity

Since the discovery of fire, the prevalent sources of energy have changed gradually over time as part of broader technological, social, economic, and political developments. The implications of the changing nature of energy sources cannot be understated. Almost every facet of technology and human life evolves as a result of improvements in harnessing energy.

The controlled use of fire represented a mastery of a source of energy, and a turning point in human history. Fire allowed humans to cook food, keep warm, make weapons, and continue activity into the night.

As humans progressed and moved towards production and trade, another important shift in obtaining energy was observed as draft animals took over some of the work. The next major change in energy use is best seen in the Greeks and Romans

dominance over the seas, using wind - an inexhaustible, free source of energy - to fill their sails.

In the Middle Ages, the watermill provided a source of localised mechanical energy, and with appropriate gearing could be used to grind, crush, hammer, saw, and power bellows. This change was revolutionary and led to the development of new industries along rivers for flour, glass, paper, textiles, and more. This was followed by the development of the windmill which followed a similar principle of operation but with wind as its primary source of energy, and allowed industries to flourish without such strict constraints on location.

During the 15th-17th centuries, wood and charcoal became increasingly used for metallurgy, heating, and construction, but a major change was about to come from under the ground. The Industrial Revolution began in Great Britain, largely due to the abundance of its coal supplies. This concentrated form of energy, which was easy to store and transport, led to the development of high-yield steam engines that united humanity's most important discoveries of fire and the wheel. Everywhere, these engines replaced other power sources and transformed the textile and metal industries, and led to the development of steamships and locomotives to transport people and goods. Kerosene, a liquid extracted from coal, was widely used for lighting, and gasoline, a by-product of the refining, would soon change the world again. The invention of the internal combustion engine led to the development of the automobile. This private means of transportation meant that freedom of movement greatly increased, as did the world's dependence on fossil fuels.

1.1.2 Developments in Electricity Generation

With the invention of the electric generator and the incandescent light bulb in the 1800s, electricity entered factories and offices. As networks grew, electricity spread to homes and began powering motors. The increasing use of electric lighting blurred the distinction between day and night with the simple touch of a hand. The 'War of the Currents' in the late 1880s saw the transition from Edison's DC distribution system to Tesla's AC distribution system, primarily driven by the ability to utilise transformers to substantially reduce transmission losses through the use of higher voltages. This enabled energy to be transmitted over longer distances, and allowed the interconnection of central stations to balance loads and improve generator load factors. Power generation was able to be moved towards areas that were more beneficial in terms of proximity to fuel sources and cooling water.

While most areas of science, engineering, and technology have been evolving rapidly, the design of electrical transmission and distribution networks has remained largely unchanged for more than 100 years. Our present day electricity network shares the same basic structure as the original transmission system: large generators, step-up transformers, high voltage transmission lines, step-down transformers, low voltage distribution circuits, and loads. This network assumes a predominantly unidirectional flow of energy due to limited power generation outside bulk generation sites.

Wind and water have been used to generate electricity since the late 19th century, but the majority of electricity was generated from fossil fuels. The discovery of energy at the core of matter drove nuclear fission research, which was first used for military applications, with the atomic bomb, and later for civilian applications, with nuclear reactors. This source of energy marked a radical change, and the development of an industry requiring advanced scientific knowledge, significant financial resources, and strong government involvement.

Electricity supply systems around the world use a diverse range of bulk generation technologies reliant upon coal, gas, oil, and uranium, as well as less concentrated renewable sources including hydro, wind, solar, tidal, and biomass. The specific mix of generation technologies is dependent upon a country's economic, political, and technological choices. Today, these systems are facing new challenges, primarily arising from environmental concerns.

1.2 The Road Ahead

1.2.1 Industry Challenges

Substantial changes are expected in the electricity industry in the coming years which will impact everything from generation through to consumption. Growing concerns about climate change have placed a strong focus on carbon dioxide (CO_2) emissions. If not addressed properly, climate change has the potential to have dangerous consequences, including frequent extreme weather events and damage to wildlife [16]. Humans contribute to climate change predominantly through the emission of greenhouse gasses, so with the aim of tackling climate change the UK has set the world's first legally binding carbon budgets. The Climate Change Act 2008 set a target of an 80% reduction in CO_2 by 2050, relative to 1990 levels [17]. More recently, the Paris Agreement, established at COP21 in December

2015, has been signed by almost 195 members of the United Nations Framework Convention on Climate Change (UNFCCC). Article 6 of this agreement establishes the Paris Agreement as a framework for a global carbon market by outlining the approaches that parties can take to achieve their nationally determined CO_2 emissions reduction targets [18]. The parties which have ratified or acceded to the Paris Agreement represent more than 87% of global greenhouse gas emissions [18]. The sheer number of signatories legitimises the magnitude of this issue, and the need for global decarbonisation efforts.

Though part of this decarbonisation can be achieved through emission reductions in aviation, shipping, surface transportation, agriculture, and manufacturing, as well as with geosequestration technologies which remove CO_2 directly from the atmosphere, these changes are typically very difficult and costly to implement. The sector with the most potential for reductions in CO_2 emissions, however, is that of electricity generation. Thus, complete decarbonisation of electricity will play a key role in meeting the aforementioned target. This can largely be obtained through transitioning from CO_2-emitting methods of electricity generation (e.g. unabated coal and gas-fired power stations) to clean, low-carbon methods of generation (e.g. wind, solar, and hydro power). In addition to this, low-carbon electricity generation also facilitates decarbonisation of other sectors of the economy.

In the coming years, large amounts of the UK's existing generation capacity will need to be replaced as a result of a 2015 decision by the UK Government to close all coal-fired power stations by 2025 [19]. This presents a challenge in maintaining a secure electricity supply, but it also provides an exciting opportunity to move towards a clean and sustainable energy future. Technology options for generation low-carbon electricity can be broadly classified into three categories: renewables, nuclear, and carbon capture and storage (CCS). One of the biggest challenges in planning for 2050 involves determining a portfolio of these technologies that is cost-effective, safe, secure (in terms of intermittency and variability of generation, as well as dependence on imported fuels), able to meet demand without a significant capacity excess, and maintains a diversity of generation methods.

Carbon-free electricity generation gives the ability to significantly decarbonise other sectors by reducing dependence on fossil fuels. In the transport sector, an uptake in electric vehicles will dramatically reduce carbon emissions, as will the electrification of heating and cooking. A 2011 WWF report stated that the UK will need 1.7 million EVs by 2020, and the take-up would need to triple again by 2030 to meet climate change targets [20].

To encourage electrification, public policies have been implemented by govern-

ments at all levels [21]. The UK government is providing over £900 million to position the UK at the forefront of ultra-low emission vehicles development, manufacture, and use [22]. Several European countries offered €5,000 subsidies in order to grow EV markets [23]. Norway and Denmark have removed vehicle purchase tax on EVs (potentially in excess of €10,000) [23]. The Japanese government has set a target that by 2020, 20% of all vehicles in use should be hybrid, electric, or fuel cell vehicles. In 2011, Barack Obama established a goal of putting one million EVs on the road by the end of 2015, and the Recovery Act of 2009 included $2.4 billion funding to support electric vehicles [24]. Despite substantial efforts to reduce electricity consumption, a significant uptake in electric vehicles will certainly cause a large increase in electricity consumption. Due to the predominantly homogeneous nature of people's daily schedule, this is also likely to cause a massive increase in peak electricity demand, unless mitigation strategies are implemented. According to National Grid's annual Future Energy Scenarios report, the number of electric vehicles in the UK could rise from 90,000 today to 11 million by 2030. This could drive an increase in peak demand of between 5 and 8 GW, representing a 9% to 14% rise from the 2017 peak electricity demand of 57 GW.

The world is also experiencing unprecedented population growth, from 6 billion in 2000, to over 7.5 billion today, and the world population is expected to reach an estimated 9-11 billion by 2050 [25]. Increasing amounts of energy are required to meet the development needs of emerging nations in Africa, Asia, and Latin America. With major concerns around the depletion of non-renewable energy sources and climate change, it is necessary to determine better ways to manage energy, regulate global demand, influence people's behaviour, and design sensible energy systems that take geopolitical, economic, ecological, and technical factors into account.

Though it takes a lot to overcome the inertia of established energy systems, the aforementioned challenges are spurring a paradigm shift in the industry towards smarter, more efficient grids. This advancement is further accelerated by the ever-decreasing cost of power electronics and storage technologies. Changes are happening in:

1. *Generation:* With a move towards low-carbon technologies
2. *Transmission and distribution:* With a move towards more efficient grids
3. *Consumption:* With a move towards reducing both average and peak power demand by implementing demand side response (DSR) techniques.

1.2.2 Changes in Generation

Technology options for generation low-carbon electricity can be broadly classified into three categories:

- *Renewables:* Distributed microgeneration (e.g rooftop solar) and large-scale plants (e.g. onshore and offshore wind farms, solar farms). Many of these generation sources are intermittent (e.g. solar, wind, tidal) but some are also steady and controllable (e.g. hydro, geothermal, biomass). The integration of a large amount of variable generation poses challenges in maintaining security of supply.
- *Nuclear:* Well-suited for baseload generation, but potentially alarming in terms of possible environmental impacts and public perception. A lot of research is being undertaken in fusion reactors, which would be much safer than traditional fission reactors.
- *Carbon Capture & Storage (CCS):* This modifies traditional fossil fuel-based generators and can capture up to 90% of the CO_2 that would otherwise be emitted. CCS-enabled gas generators could potentially be used to provide peaking power.

1.2.3 Changes in Transmission and Distribution

Smart grid technologies in transmission and distribution increase the reliability of supply, and allow infrastructure to be better utilised, reducing the need for costly over-engineering. Some popular smart grid technologies include:

- *Microgrids:* Microgrids are localised power grids which have their own generation, loads, and possibly storage. These small-scale grids are normally connected to the main network, though are able to function independently.
- *Self-Healing Networks:* With the use of an increasing number of protection and isolation devices on the network, it is possible for control systems to automatically localise and isolate faults, and dynamically adjust network configurations to maintain power to unaffected areas. The supply can be restored in fractions of a second rather than minutes or hours, as would traditionally be required.
- *Advanced Volt-VAr Control (AVVC):* The use of on-load tap-changing (OLTC) transformers, reactive power devices (e.g. shunt capacitors, STATCOMs),

and other smart devices allows voltage profiles to be controlled within specified tolerances. By shifting the voltage provided to consumers towards the lower allowable limit, the overall power drawn will decrease.

  - *Wide-Area Measurement System (WAMS):* Phasor measurement units (PMUs) are used to monitor the network state and respond to changing system conditions rapidly. It is believed that the 2003 blackout in the Northeast of the US could have been contained if this type of system was available at the time [26].

- *Dynamic Line Rating:* Distributed temperature sensing (DTS) enables continuous temperature measurements and real-time rating of underground power cables, instead of conservative ratings which are used in the absence of more accurate information.

- *High Voltage DC (HVDC):* HVDC transmissions links allow the transmission of bulk electrical power over long distances with lower losses than conventional AC transmission systems. HVDC systems are being driven by renewable energy integration, including transmission links to offshore wind developments which can have significant charging currents due to the capacitance of underwater power cables.

1.2.4 Changes in Consumption

DSR can be used to moderate peak demand on the electrical grid. One technique involves utilities controlling consumer equipment (e.g. air conditioning) with the provision of appropriate economic incentives. Smart meters are being deployed to facilitate real-time pricing and automated meter reading. Consumption habits can also be modified with price incentives (and penalties) through the implementation of this 'time-of-use' pricing. This may help to distribute electric vehicle charging throughout the day in order to avoid massive peaks.

Another method which provides considerably more flexibility and numerous other benefits is the utilisation of electricity storage. By using sufficiently sized batteries, the overall electricity demand profile can be shifted in time without any alteration of actual usage patterns.

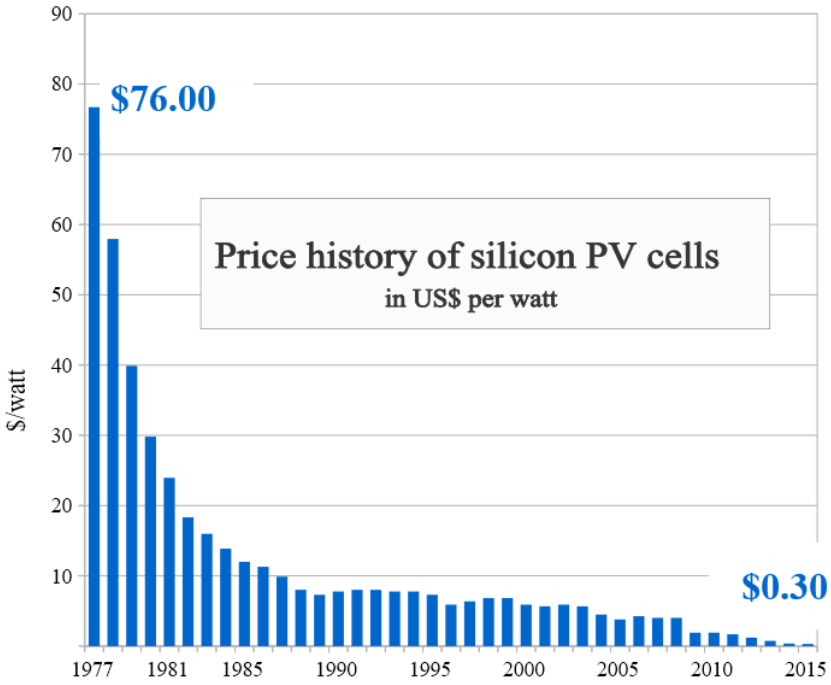


Figure 1.1: Historical trends in the price per per Watt of PV panels [1].

1.3 The Role of Solar Photovoltaics

One of the renewable generation technologies mentioned previously, solar photovoltaics (PV), is the major application considered within this thesis due to its growing importance in the global future energy mix. The photovoltaic effect was discovered in 1839 by Alexandre Edmond Becquerel, though it would be more than 100 years before Russell Ohl invented the p-n junction, which forms the basis of modern solar cells [27–29]. A decade later, in 1954, Bell Laboratories demonstrated the first practical silicon solar cell. These original solar cells had an efficiency of just 4%, and due their high cost they were primarily used in satellite applications. Technological progress and growing interest helped reduce the price of PV cells in the 1970s. One particularly significant breakthrough was made by Exxon and Elliot Berman, who discovered that the price could be brought down fivefold (from $100 per Watt to approximately $20 per Watt) if silicon from multiple crystals (polycrystalline solar) was used instead of silicon from a single crystal (monocrystalline), albeit with an associated energy efficiency penalty [30].

In the years since, the price has continued to drop, as shown in Figure 1.1 [1], and today PV modules can be obtained for around $0.30 per Watt [31], with expectations this will fall to $0.24 by the end of 2018 [32]. These price decreases follow Swanson's law, which is an observation that the price of PV modules tends to drop by 20% for every doubling of cumulative shipped volume. This is shown on a log-log scale in Figure 1.2 [2], where the blue line shows module prices (in

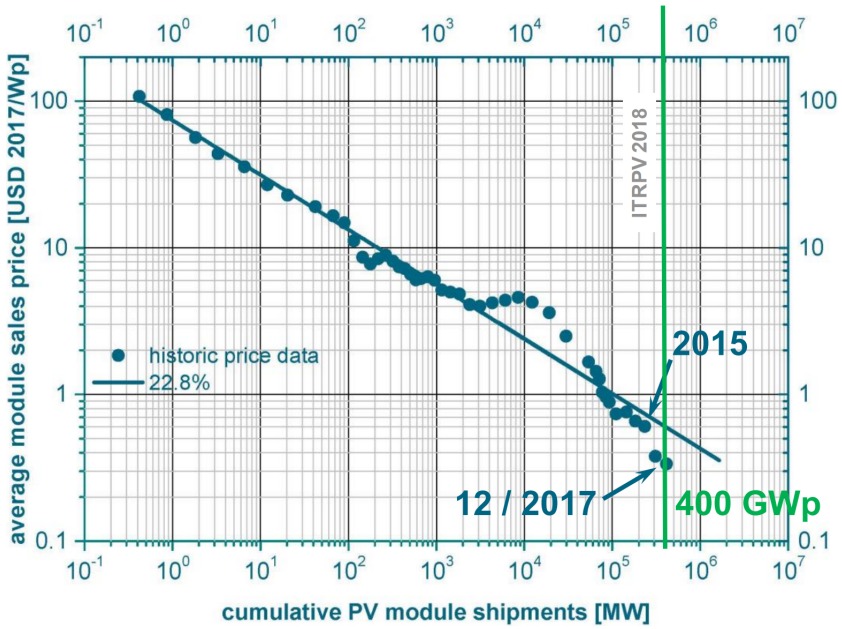


Figure 1.2: Swanson's Law: 20% reductions in price for every doubling of cumulative shipped volume [2].

2017 US dollars) as a function of worldwide module shipments. The first data point in 1976 has a price per Watt of $104, compared to the graph's final data point which has a price per Watt of $0.34 in 2017.

This decreasing cost of PV modules, combined with other factors, has sparked a significant growth in global PV capacity, as shown in Figure 1.3 [3–8]. In 2014, solar PV overtook solid biofuels to become the second largest source of non-hydro renewable electrical energy in OECD Europe, with a share of 17.3% [33].

This installed solar PV capacity can be segmented into small-scale and large-scale generation. Within the US, most of the solar PV capacity is in large-scale solar plants (those with a capacity in excess of 1 MW), as shown in Figure 1.4. Outside of this large-scale generation sector, the residential sector is growing more quickly than the commercial sector [34], and it overtook the commercial sector in installed capacity in 2015, as shown in Figure 1.5. This rapid growth in residential solar PV generation is not limited to the US, but can be seen in many countries around the world. This growth is driven by a range of factors including:

- Government programs to incentivise solar installations
- Decreasing solar PV module costs
- Decreasing power electronics-based converter costs
- Increasing levels of environmental awareness

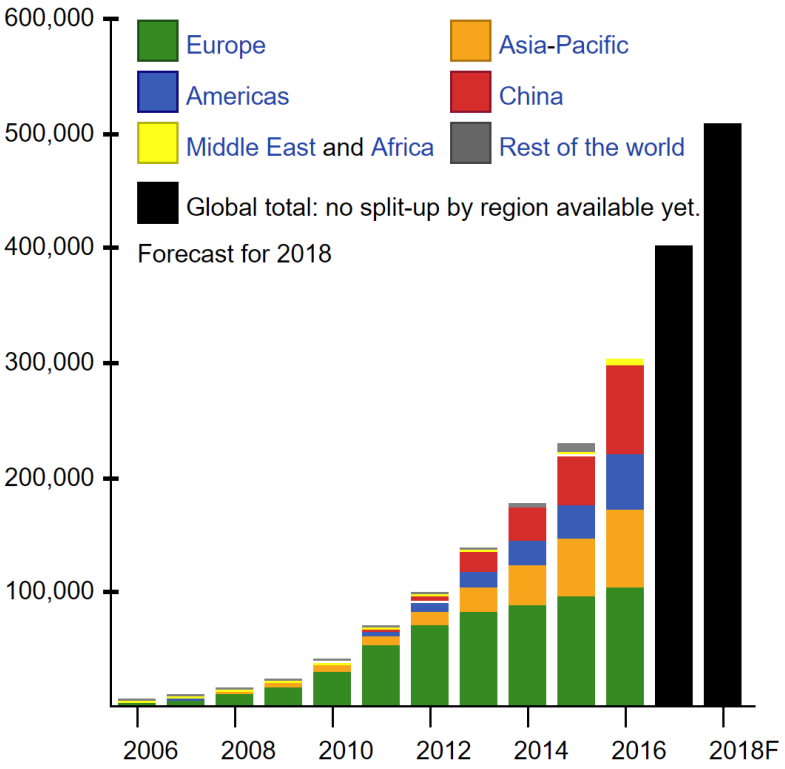


Figure 1.3: Global cumulative PV capacity from 2016 to 2018 (forecast) [3–8].

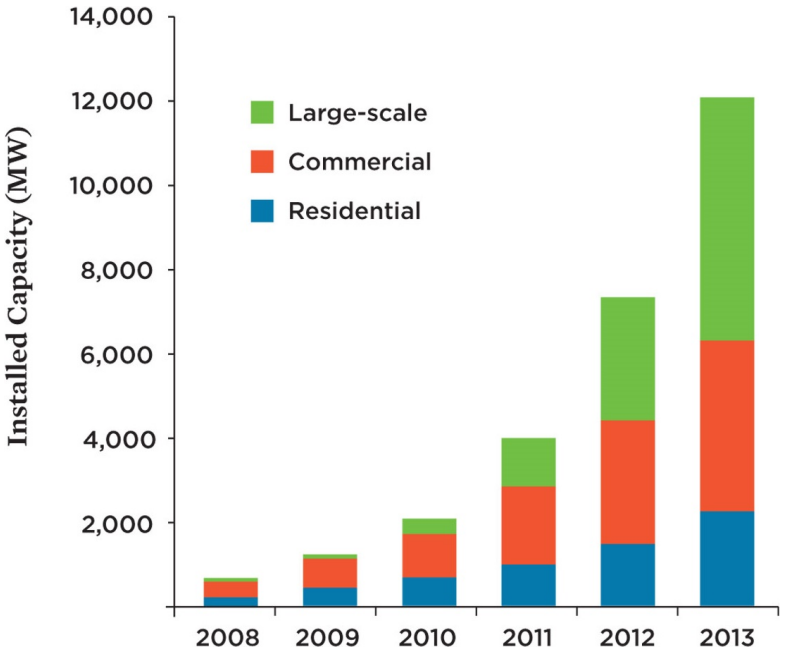


Figure 1.4: Trends in the US installed solar PV capacity by sector from 2008 to 2013 [9].

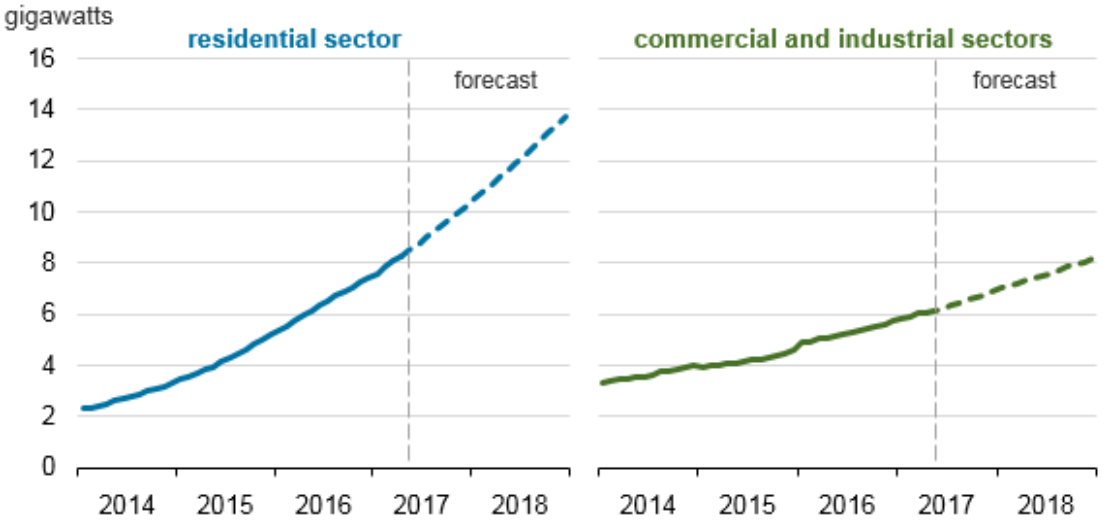


Figure 1.5: Comparison of small-scale PV generation capacity trends in the US from 2014 to 2018 (forecast) [10].

- Rising costs of fossil fuel-based generation.

Domestic solar PV generation is also expected to play a critical role in developing nations where existing infrastructure is lacking. Due to decreasing costs and increasing lifespans, the levelised cost of energy (LCOE) of off-grid solar systems with storage is becoming competitive with diesel generation in many areas - in some cases less than 20 cents per kWh for solar systems compared with 60 cents per kWh for small diesel and petrol generators [35].

It is clear that storage is required in off-grid solar PV applications to maintain a continuous energy supply between sunset and sunrise. In addition to this, storage can also play an important role in grid-connected renewable energy applications due to the peakiness and variability associated with common forms of renewable generation including solar PV and wind power.

Due to the rapid global growth in domestic solar PV generation, the potential benefits it can bring, and the interesting challenges in this area, this application is chosen to be the focus of this thesis.

1.4 Research Objectives

In this thesis, a new DC-DC converter topology is investigated which has benefits for many applications, though the focus here is on domestic solar PV applications. The development of the converter is guided by a recognition of the factors most relevant to domestic solar PV applications - cost and performance (maximising

power extracted from the PV array). Other factors are also discussed, including efficiency, reliability, volumetric power density, and gravimetric power density.

The proposed converter produces a bipolar voltage output (with a grounded midpoint) from a unipolar input, using only a single, ground-referenced switching device. This allows common mode voltages and leakage currents to be eliminated without the use of bulky and lossy transformers or common mode chokes. Another key feature of the proposed converter is its extremely low input current ripple, enabling the PV array to remain close to its optimal operating point. The converter is able to operate over a wide voltage conversion ratio range, which includes both step-up and step-down operational modes.

The design and operation of the proposed converter is examined analytically, in simulation studies, and experimentally. A discussion of its limitations is provided, which is followed by a modification to the converter to address these issues. The converter is assessed with a range of tests in order to determine its performance with closed-loop control, measure its efficiency, and assess its operation under non-ideal load conditions.

In order to demonstrate its suitability for the intended domestic solar PV applications, a single-phase grid-tie inverter is developed specifically to interface with the proposed DC-DC converter. This system is used to examine the converter's maximum power point tracking (MPPT) performance, and demonstrate the complete power flow from the PV input to the AC output.

1.5 Thesis Outline

This thesis is organised into seven chapters. Each chapter begins with a very brief summary of the thesis to that point, and an outline of the aims of the chapter. This is included to help with the readability of the thesis and allow any chapter to be read independently of the rest of the thesis.

- **Chapter 1** gives some historical background to provide the context and motivation for this thesis, followed by an outline of the objectives.
- **Chapter 2** investigates the technical background of the topics relevant to this thesis, including reviews of the latest developments in these areas.
- **Chapter 3** analyses the CCS converter and its benefits for solar PV applications. The chapter includes the design, simulation studies, and experimental results for a 4 kW prototype converter.

- **Chapter 4** explores the concept of inductor coupling and its application to the CCS converter. It then provides analytical derivations, optimisations, simulation studies, and experimental results to demonstrate the benefits of inductor coupling.
- **Chapter 5** provides an analysis of the CI-CCS converter in terms of its control and performance, including the closed-loop current controller, efficiency studies, and operation under non-ideal load conditions.
- **Chapter 6** examines the proposed converter's implementation in a full PV system, focusing on the CI-CCS converter's integration with bipolar DC input inverters. The system's coordinated control structure is examined, the DC links' power flows are studied, and simulation and experimental results demonstrate the AC power generated.
- **Chapter 7** summarises the work done, focusing on the key contributions and how they address the original research objectives. The chapter concludes with suggestions for future research to build on the outcomes of this thesis.

Chapter 2

Literature Review

The previous chapter provided the historical and global context of the energy industry, the challenges it faces, and changes that are taking place. This chapter provides a technical overview of the topics relevant to this thesis, including reviews of the latest research developments aiming to address some of the major issues identified.

2.1 Solar Photovoltaic Systems

The importance and growing role of domestic solar PV systems have been clearly demonstrated in Chapter 1, driven primarily by concerns about climate change. This chapter investigates the technical background of domestic solar PV systems, discusses the challenges they face, and reviews the latest research in addressing these problems. This chapter is divided into the three segments which domestic solar systems typically comprise of:

- Solar PV arrays
- DC-DC converters
- DC-AC converters (inverters)

The background information presented in this chapter forms the starting point for the work undertaken in this thesis.

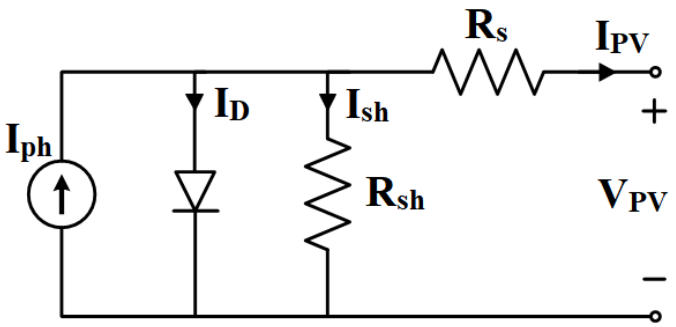


Figure 2.1: PV cell single diode model [11].

2.2 Solar Photovoltaic Arrays

2.2.1 Photovoltaic Cell Characteristics

Solar PV arrays are composed of numerous PV modules, each consisting of a number of PV cells. These PV cells are usually wired in series then encased within tempered glass, and modules commonly contain 36, 48, 60, or 72 cells, with a maximum output power of 100 W - 300 W [36]. Each PV cell is a thin semiconductor wafer consisting of two layers which are usually made of crystalline silicon. Most cells will be either monocrystalline (mono-Si or single crystalline) or polycrystalline (poly-Si or multicrystalline), with the more expensive monocrystalline cells having efficiencies up to 26.7% compared with polycrystalline's efficiency of up to 22.3% [36].

It is useful to model a PV module as a black box with two connections providing a current depending on the terminal voltage. Each cell can be modelled as a simple circuit, known as the single diode model (SDM) [11, 37], with four components as shown in Figure 2.1. The current source output depends largely on the incoming irradiance, and the non-linear diode element reflects the dependence on the band gap and losses to recombination, and regulates the cell voltage. R_{sh} represents the cell's shunt (leakage) resistance and the series resistance, R_s, represents the internal cell resistance.

For this SDM, Equation 2.1 can be used to approximate the output cell current,

I_{PV}, for a given cell voltage, V_{PV} [11]:

$$I_{PV} = \underbrace{\frac{G}{G_{ref}}\left(I_{ph,ref} + \mu_{sc}\left(T - T_{ref}\right)\right)}_{I_{ph}=\text{photocurrent}} - \underbrace{I_s\left(\exp\left[\frac{q\left(V_{PV} + R_s I_{PV}\right)}{nkT}\right] - 1\right)}_{I_D=\text{diode current}} - \underbrace{\frac{V_{PV} + R_s I_{PV}}{R_{sh}}}_{I_{sh}=\text{shunt current}} \quad (2.1)$$

where

G is the irradiance

T is the cell temperature

I_s is the reverse saturation current

R_s is the series resistance

R_{sh} is the shunt resistance

G_{ref} is the irradiance at standard test conditions (STC)

$I_{ph,ref}$ is the photocurrent at STC

μ_{sc} is the coefficient temperature of short-circuit current

T_{ref} is the cell temperature at STC

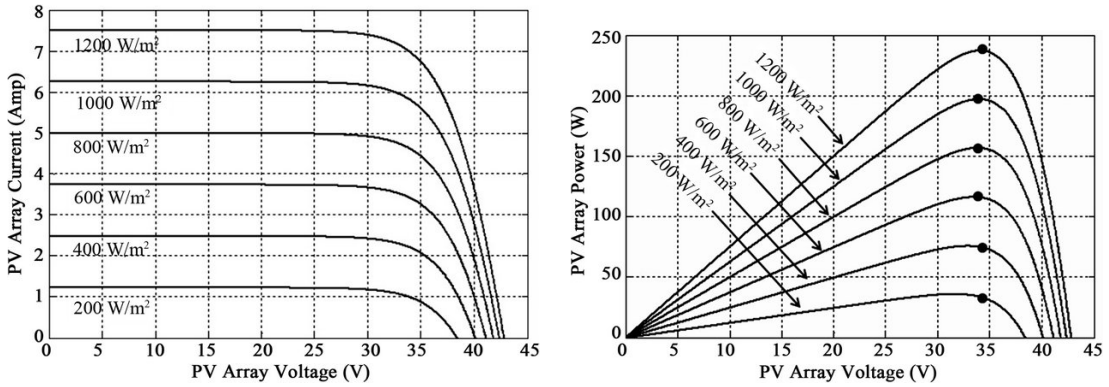
q is the electron charge

n is the diode quality factor

k is the Boltzmann constant

Unfortunately, the parameters used in Equation 2.1 are not commonly provided by manufacturers, making the equation somewhat limited in terms of practical value. A number of approaches have been proposed to apply some simplifying assumptions and derive an expression that is based on typical datasheet information.

Figure 2.2a shows typical current (I-V) curves for a 250 W PV array, and Figure 2.2b shows the corresponding power (P-V) curves. When scaling the cell equation up to the module level, the voltage increases with the number of series-connected cells, and the current increases with the number of parallel-connected cells. The incoming irradiance primarily affects the short-circuit current (the



(a) I-V curves for various irradiance conditions. (b) P-V curves for various irradiance conditions.

Figure 2.2: Solar array characteristics for various irradiance conditions [12].

y-axis intercept, where $V_{PV} = 0$), and cell temperature primarily affects the open-circuit voltage (the x-axis intercept, where $I_{PV} = 0$) [38–40].

2.2.2 Maximum Power Point Tracking

To maximise the energy generated by the solar modules, it is desired to maintain operation at the highest point on the P-V curve, known as the maximum power point (MPP). Since the P-V curve varies with irradiance and cell temperature, a MPPT controller should be used to ensure the module is connected at the optimal voltage to deliver the best possible performance. It is possible for partial shading to create multiple local maxima so MPPT controllers should make sure they do not settle at these points instead of the global maximum [15]. A comparison of various MPPT techniques is given in Table 2.1. The most common types of MPPT control strategies are:

- *Perturb and Observe (P&O):* This controller operates by varying the PV voltage and measuring the change in output power [41].
- *Hill climbing:* Hill climbing is similar to P&O, but introduces perturbations in the duty ratio ratio instead of the PV voltage [42].
- *Three-Point Weight Comparison:* Variation of P&O where the current point is compared to the two preceding ones to ensure the MPP is tracked even under sudden irradiance changes [43].
- *Incremental Conductance (IC):* Compares instantaneous with incremental conductance to determine which side of MPP the current operating point is on. This controller allows the operating point to be maintained at the MPP instead of oscillating around it like the P&O method [44].

Table 2.1: Main characteristics of various MPPT techniques [15].

MPPT Technique	PV Array Dependent?	True MPPT?	Analog or Digital?	Periodic Tuning?	Convergence Speed	Implementation Complexity	Sensed Parameters
Hill-climbing/P&O	No	Yes	Both	No	Varies	Low	Voltage, Current
IncCond	No	Yes	Digital	No	Varies	Medium	Voltage, Current
Fractional V_{OC}	Yes	No	Both	Yes	Medium	Low	Voltage
Fractional I_{SC}	Yes	No	Both	Yes	Medium	Medium	Current
Fuzzy Logic Control	Yes	Yes	Digital	Yes	Fast	High	Varies
Neural Network	Yes	Yes	Digital	Yes	Fast	High	Varies
RCC	No	Yes	Analog	No	Fast	Low	Voltage, Current
Current Sweep	Yes	Yes	Digital	Yes	Slow	High	Voltage, Current
DC Link Capacitor Droop Control	No	No	Both	No	Medium	Low	Voltage
Load I or V Maximization	No	No	Analog	No	Fast	Low	Voltage, Current
dP/dV or dP/dI Feedback Control	No	Yes	Digital	No	Fast	Medium	Voltage, Current
Array Reconfiguration	Yes	No	Digital	Yes	Slow	High	Voltage, Current
Linear Current Control	Yes	No	Digital	Yes	Fast	Medium	Irradiance
I_{MPP} & V_{MPP} Computation	Yes	Yes	Digital	Yes	N/A	Medium	Irradiance, Temperature
State-based MPPT	Yes	Yes	Both	Yes	Fast	High	Voltage, Current
OCC MPPT	Yes	No	Both	Yes	Fast	Medium	Current
BFV	Yes	No	Both	Yes	N/A	Low	None
LRCM	Yes	No	Digital	No	N/A	High	Voltage, Current
Slide Control	No	Yes	Digital	No	Fast	Medium	Voltage, Current

- *Fractional Open-Circuit Voltage:* Set the PV current momentarily to zero and measure the open circuit voltage, then set the reference voltage to around 71-78% (commonly 76%) of the open circuit voltage. This works due to the near linear relationship between the MPP voltage and the open circuit voltage [15].

- *Fractional Short-Circuit Current:* Similarly to the fractional open-circuit voltage method, this is based on the fact that the MPP current is roughly proportional to the short circuit current (approximately 78-92%) [45].

- *Current Sweep:* Perform a periodic sweep to obtain the array I-V characteristics and use this to compute the location of the MPP [46].

- *Others:* Constant Voltage (CV), IC and CV Combined, Short-Current Pulse, Temperature Method, Fuzzy Logic Control, Neural Networks [15]

2.2.3 Photovoltaic Current Ripple Requirements

To ensure maximum utilisation and provide optimal MPPT performance, the solar PV panels should be operated with a continuous output current and voltage. The shape of the I-V curve means that changes in current also affect the PV voltage and greatly impact the power [47], as shown in Figure 2.3. Thus, relatively modest levels of input current ripple can cause a drastic decrease in the total energy produced [13].

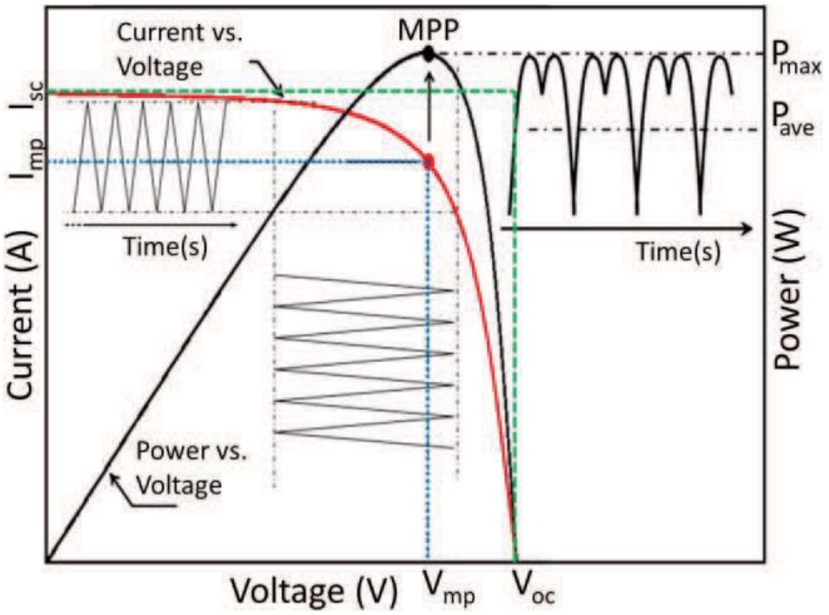
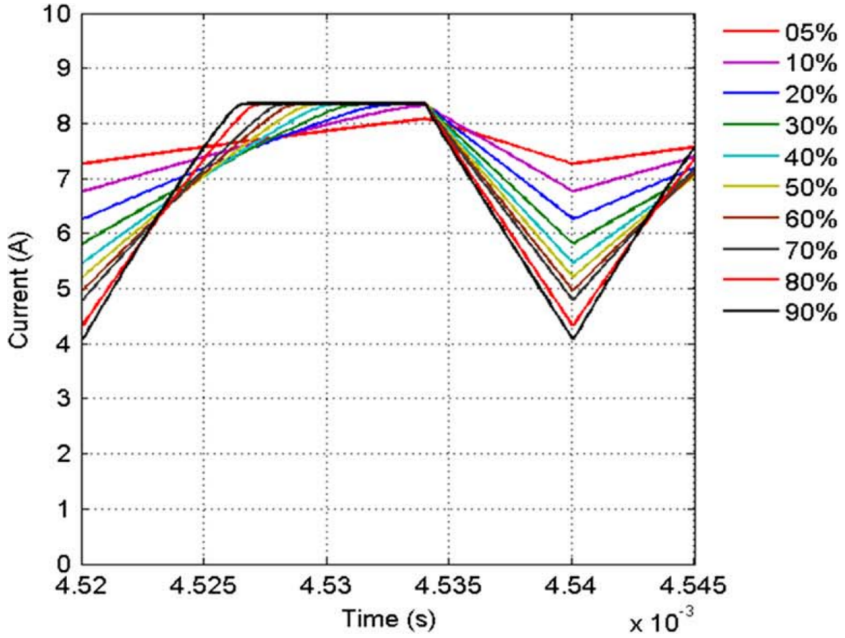


Figure 2.3: The impact of current ripple on I-V and P-V curves [13].

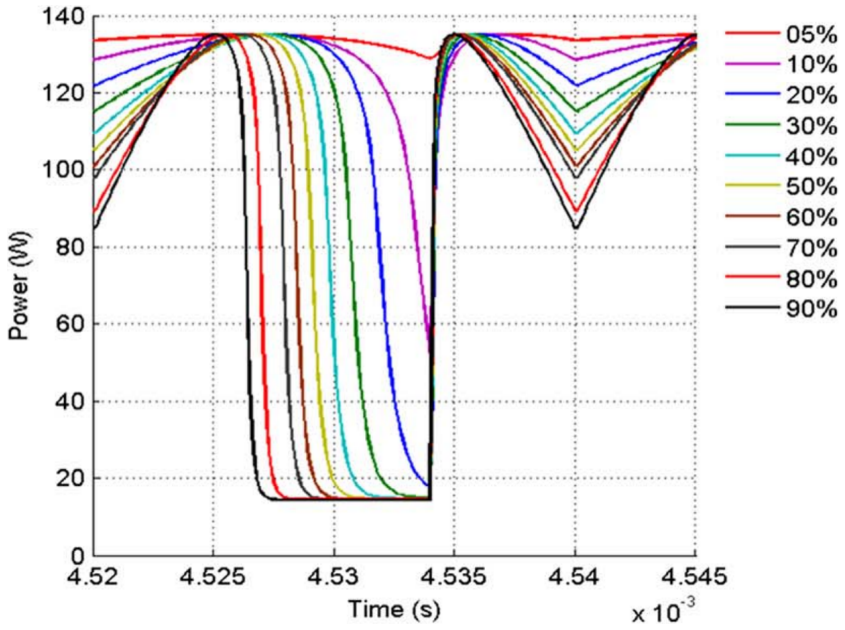
As these panels are typically connected to power electronics-based converters (discussed in Section 2.2.4), it is possible to use an LC or C filter to flatten the current drawn from the PV array, since most converters do not have a particularly smooth input current [48]. The capacitors in these filters are called 'decoupling capacitors', and they become especially large when converters with discontinuous input currents are used. The use of these filters not only increases costs, weight, volume, and losses, but causes another substantial issue - greatly decreased reliability. This is because these large decoupling capacitors tend to be electrolytic capacitors, which generally are the components most prone to failure, and hence are usually the limiting factor in the overall lifetime of the system.

The impact of current ripple on the average PV output power depends on many factors including the irradiance level, fill factor, and weather conditions. The effect of input current ripple is greater at low irradiance levels (and therefore lower at high irradiance levels) [49]. Figure 2.4a shows varying levels of PV current ripple (from 5% to 90% of I_{SC}), and Figure 2.4b shows the power output of the PV module corresponding to each of these current ripple conditions [13]. It can be seen that there is a substantial power ripple introduced when the current ripple is greater than 5%.

Table 2.2 shows the numerical relationship between the PV current ripple and average output power, confirming the large drops in average output power as the current ripple exceeds 5% [13]. Due to this, it is therefore desired to limit the ripple of the PV current to 5%.



(a) Varying levels of PV current ripple [13].



(b) PV power at varying levels of current ripple. [13].

Figure 2.4: Various levels of PV current ripple and the corresponding variations in PV output power [13].

Table 2.2: Relationship between current ripple and PV power [13].

Current ripple (%)	Average PV power (W)	PV efficiency (%)
5	133.3	98.0
10	127.7	93.9
20	118.1	86.8
30	109.5	80.5
40	102.8	75.6
50	97.6	71.8
60	92.8	68.3
70	89.1	65.4
80	81.9	60.2
90	77.6	57.1

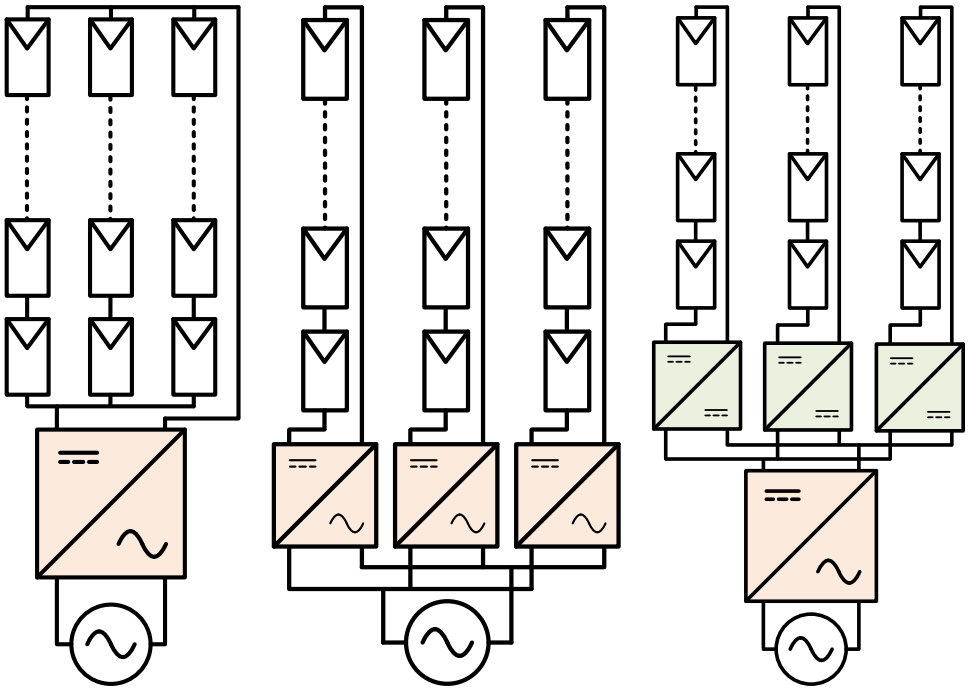
2.2.4 System Configuration Options

This section analyses a number of system configurations and compares them in terms of the number of power processing stages, converter efficiency, and system impacts when panels are in uneven conditions (e.g. partially shaded).

A string is a series connection of PV modules that, by definition, has a higher output voltage (which is useful for easier power conversion), and equal current though every module. Partial shading on any module will limit its current output, which in turn limits the current (and hence power output) for all modules on the same string, unless the shaded module is short-circuited out with the use of a bypass diode. Three string-based topologies are first examined (central inverters, string inverters, multi-string inverters), followed by module-based topologies (microinverters, parallel DC-DC converters, cascaded DC-DC converters, delta converters). The module-based technologies are newer and are commonly known as module integrated converters (MICs) or module-level power electronics (MLPE) devices. MICs aim to solve the problem of individual module parameters (e.g. partial shading) affecting the entire string by further increasing the number of MPPT controllers from a per-string to a per-panel basis. The additional flexibility of MICs also simplifies the design of PV systems by removing challenges such as string sizing and array layout.

2.2.4.1 Central Inverter

A central inverter takes an entire array of strings in parallel as a single DC input then converts it for export to the AC network, as shown in Figure 2.5a. This conversion may be done with a single DC-AC stage, though an extra DC-DC stage



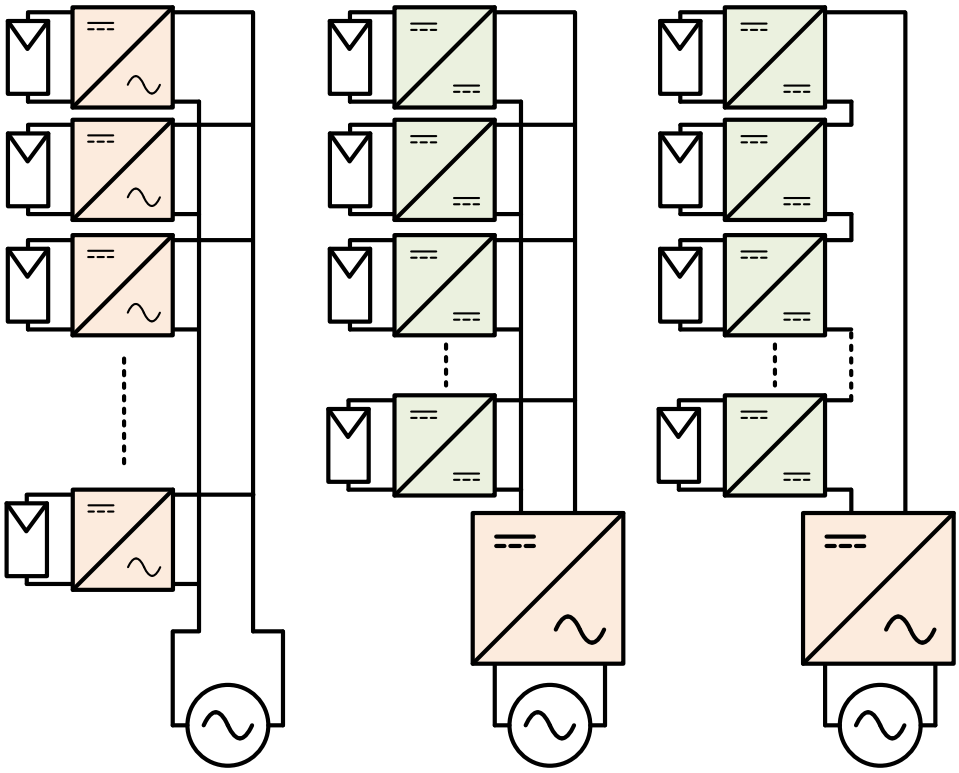
(a) Central inverter. (b) String inverters. (c) Multi-string inverter.

Figure 2.5: String-based solar PV system configurations.

should be added if the input voltage is not high enough, or if the inverter is designed to operate with a regulated DC voltage [45, 50]. A single MPPT controller is implemented on the entire solar array, meaning any orientation, manufacturing, or irradiance differences will result in a suboptimal output for the entire system. Additionally, since all strings are connected in parallel, the DC voltage set by the MPPT controller is equal across all strings meaning that individual strings may also not be operating at their MPP [43, 51].

2.2.4.2 String Inverter

A string inverter is similar to the central inverter, however in an effort to increase the number of MPPT controllers each inverter only operates on a single string (to ensure more panels operate closer to their MPP), as shown in Figure 2.5b. Each of these inverters may be a single DC-AC inverter, though again a step-up DC-DC stage can be added if the string voltage is not sufficiently high for direction inversion, or if the inverter's DC input requires tighter regulation. In order to expand the system, additional PV strings and inverters will be added, connected in parallel directly to the AC network [43, 45, 50, 51].



(a) Microinverters. (b) Parallel DC-DC MICs. (c) Cascaded DC-DC MICs.

Figure 2.6: MIC/MLPE-based solar PV system configurations.

2.2.4.3 Multi-String Inverter

A multi-string inverter combines the previous two ideas of a central inverter and per-string MPPT controllers. This is done with the use of multiple DC-DC converters performing MPPT on individual strings, with their outputs connected in parallel to a common DC bus. This power is then processed by a single inverter for connection to the AC network [43, 45, 50, 51], as shown in Figure 2.5c.

2.2.4.4 Microinverters

The first of the module integrated converters (MICs) examined is the microinverter. The microinverter has a converter on each module which performs MPPT and outputs directly to AC mains, as shown in Figure 2.6a. In practice, this is achieved with a high step-up ratio DC-DC converter followed by an inverter. To achieve such a high step-up ratio, the DC-DC converter will often incorporate a high frequency transformer. The key drawbacks of this topology are more expensive and less efficient converters compared with a large central inverter [50, 52].

2.2.4.5 Parallel DC-DC Converters with Central Inverter

The parallel DC-DC MIC topology aims to combine module-level MPPT with a large, efficient central inverter. It achieves this by placing high step-up ratio DC-DC MPPT converters (sometimes known as 'power optimisers') on each module, with all their outputs connected in parallel to a single DC bus which is then connected to the AC network by a single inverter. This configuration is shown in Figure 2.6b. Like the microinverter, these DC-DC converters will often incorporate transformers, leading to relatively lower efficiencies and higher costs than transformerless converters [53, 54].

As the voltage output of each DC-DC converter must be the same, the current output of each DC-DC converter is proportional to its module power.

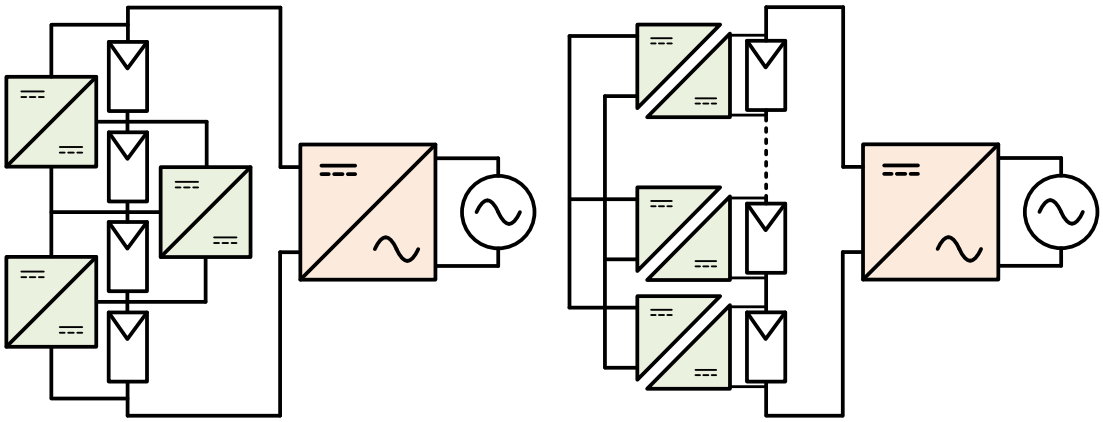
2.2.4.6 Cascaded DC-DC Converters with Central Inverter

The cascaded DC-DC MIC topology, like the parallel topology, aims to combine module-level MPPT with a large, efficient central inverter. Rather than utilising high step-up ratio converters, it utilises DC-DC converters (sometimes known as 'power optimisers') with modest voltage ratios, which are more efficient. These DC-DC converters have their outputs connected in series with a fixed output voltage, which then feeds a central inverter as shown in Figure 2.6c. The individual DC-DC converters may be step-up or buck-boost type converters depending on the number of modules in the string.

The controller complexity is greatly increased as each module needs to communicate its maximum power level, all of which are then summed. 'SolarEdge Power Optimizers' use power line communication (PLC) to achieve this coordinated control using the existing PV power cables [55]. The output current is obtained by dividing the total module power by the bus voltage, giving the series current that must flow through the output of the DC-DC converters. Each DC-DC converter is then controlled with this same output current, giving an output voltage proportional to its module power.

The main benefits of this topology are

- More efficient DC-DC converters (resulting from the lower voltage gain ratios of each DC-DC converter)
- Independence of the string output voltage from the individual module voltages



(a) DPP configuration 1. (b) DPP configuration 1.

Figure 2.7: DPP-based solar PV system configurations.

- A simpler inverter design inverter (as its input will always be a fixed DC bus voltage).

This topology can be expanded by adding more of these strings in parallel [56].

2.2.4.7 Differential Power Processing

The final topology examined uses the concept of differential power processing (DPP), which aims to increase the system efficiency of the cascaded DC-DC converters by processing less power. The previous topologies all require 100% of the output power to be processed at every stage, but the DPP strategy only processes a fraction of the output power. When the modules are operating around a similar power level it is possible to have most of the current flowing in series through the modules with only the fractional differential power being processed. These converters can be cheaper and less efficient as they only process substantial power when module conditions are significantly different. This can be achieved in a number of ways, including:

- Using bidirectional "delta" converters to shuffle power between modules such that the excess power (compared with the average) in certain modules is injected into underperforming modules [57], as shown in Figure 2.7a. A key drawback of this topology is that power is accumulated and processed by consecutive converters as it moves between high and low power modules.

- Using very simple analogue controllers with no communications to equalise all module voltages by having bidirectional DC-DC converters connected in parallel to an isolated DC-DC bus with a control objective of 1:1 voltage

ratio [51], as shown in Figure 2.7b. This will cause high performing modules to feed power into the bus while underperforming modules take power from the bus. Having all modules at an equal voltage will not achieve the true MPP of all modules, but the overall energy extracted is around 99% of the theoretical maximum in most conditions [51].

These DPP configurations move the overall MPPT to the central inverter, which is simpler because this process guarantees a single global maximum rather than multiple local maxima. Unlike the cascaded DC-DC converter topology, this creates a variable DC bus voltage and strings must all have the same number of modules in order to be connected in parallel.

Despite the rapid growth in popularity of the MLPE-based configurations, string-based configurations are still by far the most commonly used globally and comprise the vast majority of the world's inverter market [58]. Regardless of which configuration is used, it can be seen that DC-DC converters play a vital role in PV applications. The DC-DC converter proposed in this thesis is designed for a string-based configuration, though could also be used in MLPE-based configuration, as discussed in Section 7.4.

For all solar configurations, attention needs to be paid to grounding considerations for reasons that will be discussed in the following section.

2.2.5 System Grounding Considerations

The mechanical structure of PV modules and their installation on grounded support frames creates a parasitic capacitance to ground. This capacitance increases with the area of the conductive surfaces present in the PV array, meaning bigger systems have larger parasitic capacitances. This capacitance also becomes more problematic if the PV panels are damp (e.g. from rain or condensation) [59]. The parasitic capacitance, C_{PV}, can be calculated using Equation 2.2:

$$C_{PV} = \frac{\epsilon_0 \epsilon_r A}{d} \tag{2.2}$$

where:

ϵ_0 is the permittivity of free space (8.854×10^{-12} F/m)

ϵ_r is the relative permittivity of the material (usually glass)

A is the effective surface area of the capacitor (PV panel)

d is the distance between the capacitor plates (PV panel surface to the film, module frame, or support frame)

This parasitic capacitance varies widely depending on the weather conditions, module type (e.g. crystalline or thin-film), and mounting frame structure, though values of 60 to 160 nF/kW could reasonably be expected for damp arrays [59–63], though even capacitances as high of 1000 nF/kW are possible in some circumstances [61].

Domestic solar PV systems are usually connected to single-phase, earthed AC grids. Some grid-tie inverters exhibit time-varying common mode voltages on the DC bus as part of their operation (discussed in Section 2.4). There are two main causes of these common mode voltages:

- *High frequency common mode voltages*: Due to the switching PWM operation of inverters
- *Low frequency common mode voltages:* Due to the double line frequency ripple present on the DC bus of single-phase inverters

These common mode voltages can cause leakage currents (also known as displacement currents) to flow through the PV system's parasitic capacitance. Considering the difference in frequency and magnitude of these common mode voltage, the leakage currents due to the inverter's high frequency switching operation are often much greater than the grid frequency leakage currents. If the total leakage current exceeds the threshold of the residual current device (RCD) or residual current monitoring unit (RCMU), as shown in Figure 2.8, then this protection device will trip [59]. This causes the PV system to be disconnected from the grid, leading to significant production losses, reduced financial benefit for the owner, decreased confidence in PV technology, and potential safety issues if owners are tempted to suppress the RCD or increase the disconnection threshold. The threshold value for RCDs is extremely low, because currents as low as 30 mA can send the heart into ventricular fibrillation, so RCDs must reliably trip at this point. RCDs are designed not to operate below 15 mA, as otherwise nuisance tripping would occur (since there is often some level of leakage current associated with most electrical installations), so in practice RCDs will trip somewhere between 15 mA and 30 mA [61].

RCDs differ from overcurrent protection devices (e.g. fuses) in that RCDs are implemented to prevent harm from electric shocks, whereas overcurrent protection

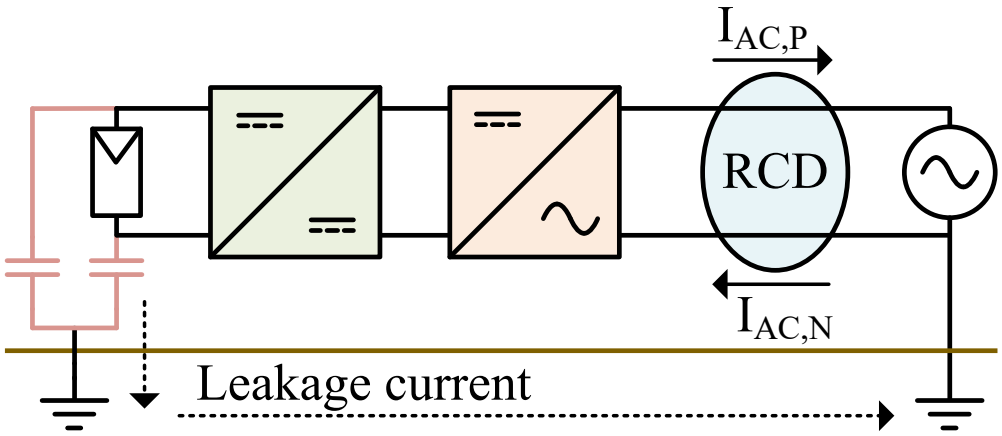


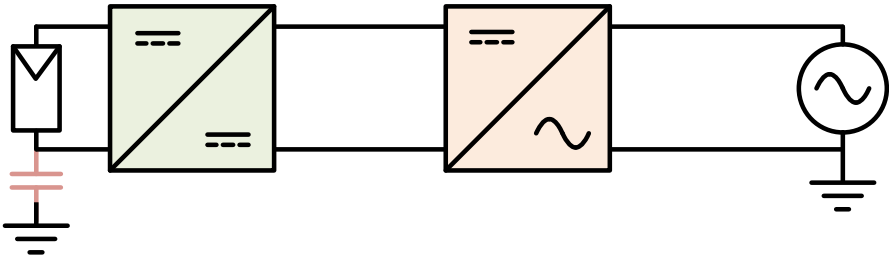
Figure 2.8: Leakage currents through the parasitic capacitance can cause RCDs to trip.

devices are intended to protect electrical wiring and equipment. Thus, the 'main fuses' used in domestic applications are usually rated in the tens of amps.

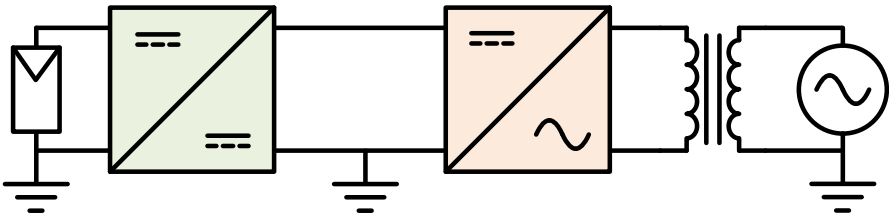
A block diagram of a generic system where these common mode voltages are present at the PV array terminals is shown in Figure 2.9a. The common mode voltages are introduced by the inverter on the DC bus by inverters like the full bridge inverter (discussed in Section 2.4). Since most standard DC-DC converters have the negative terminals of their inputs and outputs connected, the common mode voltage will also be present on the PV array, where the parasitic capacitance may be significant, as shown in Figure 2.10a. In addition to causing leakage currents, the common mode voltages present on the PV array and DC-DC converter also create safety hazards and contribute to increased losses and failure rates.

One method of mitigating this issue is to use an isolation transformer between the PV array and the grid. This can be achieved by using a line-frequency transformer between the inverter and the grid, allowing the PV system to be grounded, as shown in Figure 2.9b, with the corresponding AC equivalent common mode circuit shown in Figure 2.10b. This solution is not without its disadvantages: line-frequency transformers are bulky, heavy, use a lot of iron and copper, and negatively impact the system's efficiency.

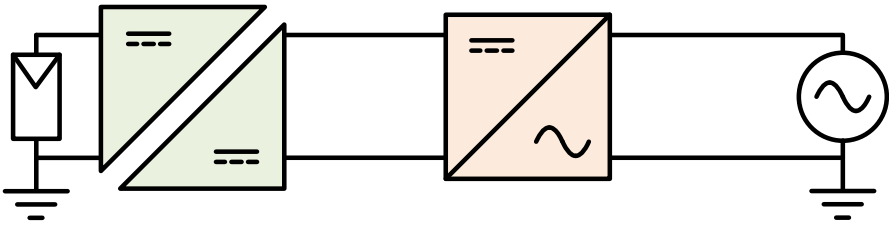
High frequency isolation transformers by comparison are significantly smaller, lighter, often iron-free, and more efficient than equivalently rated line-frequency isolation transformers. Figure 2.11a shows a side-by-side comparison of a 50 Hz and high frequency 5 kVA isolation transformer at standard mains voltage [64]. It should be noted that the power density increases do not increase linearly with frequency (demonstrated in Figure 2.11b), as at higher frequencies the insulation distance requirements start to dictate the overall dimensions [65]. Such a high



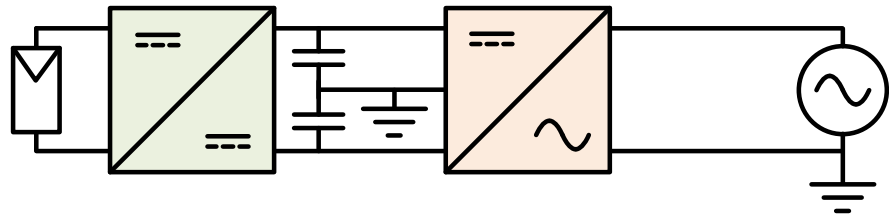
(a) Unipolar DC output without transformer causing leakage currents.



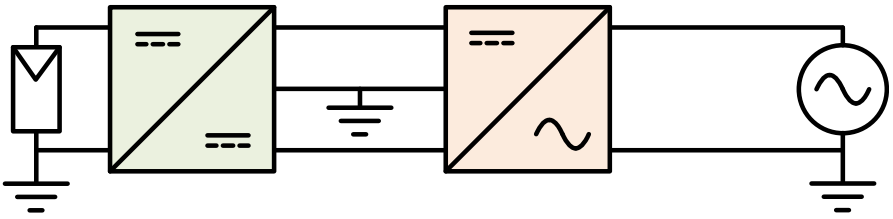
(b) Unipolar DC output with line frequency transformer.



(c) Isolated DC-DC converter with unipolar output.

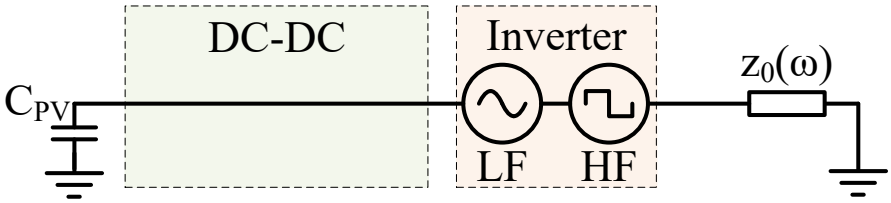


(d) Unipolar DC output with grounded bipolar input inverter.

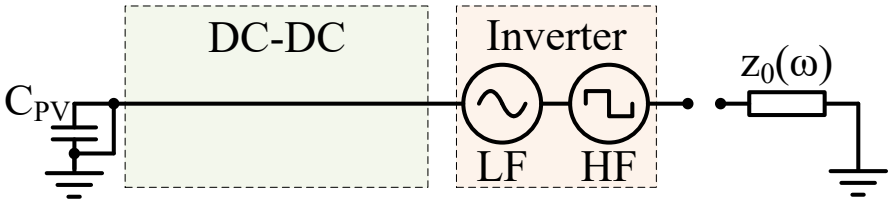


(e) Bipolar DC output with grounded bipolar input inverter.

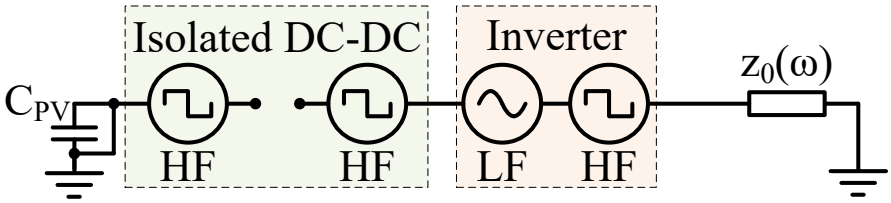
Figure 2.9: Grounding options for single-phase solar PV systems.



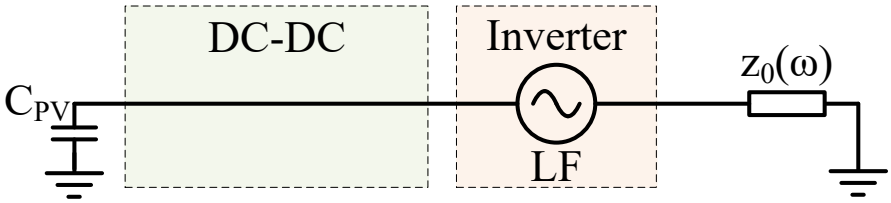
(a) Unipolar DC output without transformer causing leakage currents.



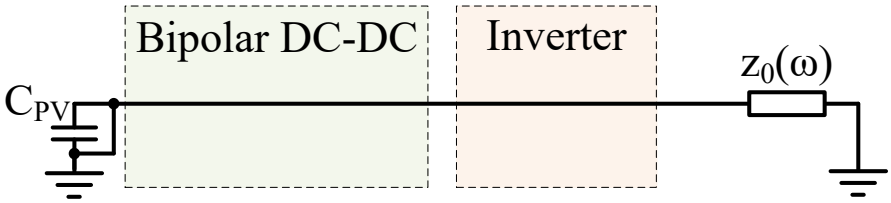
(b) Unipolar DC output with line frequency transformer.



(c) Isolated DC-DC converter with unipolar output.



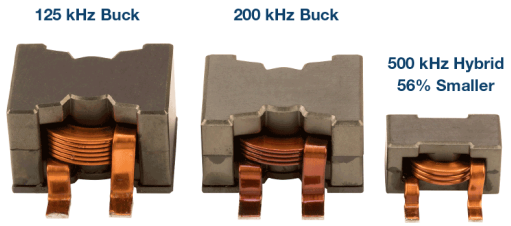
(d) Unipolar DC output with grounded bipolar input inverter.



(e) Bipolar DC output with grounded bipolar input inverter.

Figure 2.10: AC equivalent common mode circuits of the systems in Figure 2.9.

(a) Size comparison of 50 Hz three-phase and 20 kHz single-phase 5 kVA transformers [64].



(b) Size comparison of 125 kHz, 200 kHz, 500 kHz 300 W transformers [65].

Figure 2.11: Size comparison of transformers at different frequencies, voltages, and powers.

frequency isolation transformer can be integrated within the DC-DC converter to form an isolated DC-DC converter, which will be discussed in Section 2.3. The system configuration with an isolated DC-DC converter is shown in Figure 2.9c (with the corresponding AC equivalent common mode circuit shown in Figure 2.10c), and again allows the PV array to be grounded, solving the leakage current issue with a higher volumetric and gravimetric power density than with a line-frequency isolation transformer. The downside of using an isolated DC-DC converter is that they have an increased number of switching devices and diodes than non-isolated converters, and the inclusion of an isolation still negatively impacts the efficiency. The increased cost of the extra components is undesirable for domestic PV applications which are particularly price-sensitive.

In contrast, transformerless topologies are generally cheaper, more efficient, and more reliable [66]. DC decoupling methods have been investigated in recent years to reduce the leakage current without the use of transformers. These methods work by disconnecting the PV panels from the grid at the switching frequency, either on the DC bus or on the AC side [67]. Fundamentally these methods reduce leakage currents by changing the impedance of the current path (by creating an open circuit with power electronic switches), rather than removing the common mode voltages. Inverters such as the HERIC, H5, and H6 (reviewed in Section 2.4) have been used, however additional switching devices must be employed which increase the losses, cost, and complexity of the system.

An alternative to transformers and these DC decoupling methods is to eliminate these high frequency common mode voltages by using an inverter with a grounded bipolar DC input (reviewed in Section 2.4). Figure 2.9d shows how it is possible to use a standard unipolar output DC-DC converter to create this grounded bipolar DC bus, however prohibitively large capacitances must be used, and both the converter and PV array will be referenced to the negative DC bus voltage. Referencing the PV array to the negative DC bus means that the double power frequency ripple (100 Hz) associated with single-phase inverters will still be present between the array and grounded support frames, so only the switching frequency common mode voltages are eliminated, as shown in the AC equivalent common mode circuit in Figure 2.10d.

The solution explored in this thesis uses a DC-DC converter that produces a bipolar output from a unipolar input, as shown in Figure 2.9e. This method fundamentally addresses the leakage current issue without the use of transformers or high current-carrying capacitors, whilst also providing grounding for both the PV system and DC-DC converter, as shown in the AC equivalent common mode

circuit in Figure 2.10e. This grounding provides a range of benefits, including:

- Easing isolation requirements for the DC-DC converter
- Allowing a non-isolated gate driver to be used in the DC-DC converter
- Solving the 'potential induced degradation' (PID) problem associated with PV cells.

The PID effect is caused by dielectric polarisation in PV cells. In addition to the previously-discussed leakage currents which are caused by time-varying voltages, there are also tiny DC currents that flow through the insulators between the PV panels and the grounded mounting frames. These DC currents cause a dielectric polarisation in the material, which can build up electric fields that weaken the fields within the solar cells, or create local short circuits within cells, resulting in decreased voltages and hence efficiencies [68]. In order to prevent the PID effect, the entire array should have the same polarity potential to ground: positive for p-doped cells, and negative for n-doped cells [69]. For non-grounded PV arrays, some parts of the array have a positive potential to ground, and other parts have a negative potential to ground, meaning that parts of the array will suffer from the PID effect if the same panels are used for the entire array. If the PV array can be negatively grounded (as in Figure 2.9e), then a positive potential exists between all panels and ground, completely eliminating the PID effect when p-doped cells are used.

2.3 DC-DC Power Converters

The previous sections describing the various solar PV system configurations clearly demonstrate the essential role that DC-DC converters play in nearly all domestic solar PV applications. These converters generally serve two key roles:

- Perform MPPT on the PV array
- Regulate the voltage provided to the inverter

For solar PV applications, these DC-DC converters are only required to support unidirectional power flow. Beyond this, there are some properties which are desirable for domestic solar PV applications:

- Low cost

- Low input current ripple, to improve MPPT performance as described in Section 2.2.3
- Wide voltage conversion ratios (including both step-up and step-down), to provide flexibility in the number of series-connected panels, and to support a wide range of PV panel conditions (e.g. temperature has a significant impact on the MPP voltage).

Some other desirable characteristics which aren't as critical include: high efficiency, high reliability, high volumetric power density, high gravimetric power density. This section provides a review of the following DC-DC converters which are used in solar PV applications:

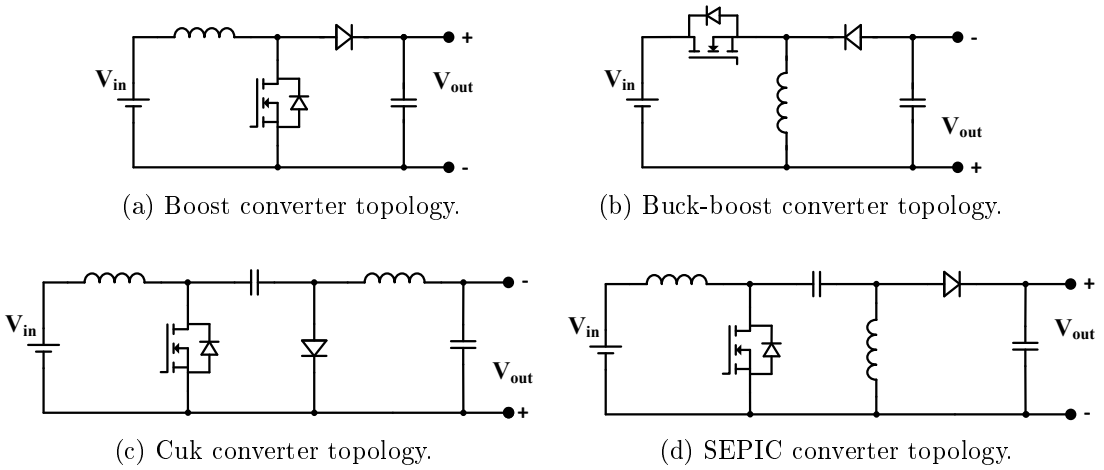
- Boost converter
- Buck-boost converter
- Isolated DC-DC converters
- Cuk converter
- SEPIC converter

It should be noted that there are a number of variations of these converters which are modified to include interleaving, resonant and soft-switching, and many other topological changes. In this application, only moderate voltage change ratios are required as the series voltage of a solar PV string is similar to the DC bus voltage required by the grid-interface inverter. A summarised comparison of the above DC-DC converters is provided in Table 2.3, in addition to the converter proposed in this thesis. The component ratings for the converters are largely similar, so the primary factor influencing the cost of these converters is their component count, shown in Table 2.3. The primarily losses in non-isolated DC-DC converters are power electronic device losses, inductor core losses (eddy current and hysteresis), copper losses (inductor windings), and capacitor ESR losses. The non-isolated converters in Table 2.3 all have an equal switch count so the power electronic device losses will be similar. For isolated converters, the additional switches and transformers cause higher losses and hence lower efficiencies.

The inductor core, winding, and power electronic device losses are lower for the proposed converter because the reduced input current ripple decreases both the size of the hysteresis loop and peak inductor current, however its increased capacitor count will increase the converter's ESR losses. For PV applications, it is also important to distinguish between the DC-DC converter's efficiency and the overall

Table 2.3: DC-DC converters commonly used in solar applications.

Converter	Voltage output	Input current	V_{out}/V_{in}	# switches	# diodes	# inductors	# capacitors
Boost	Unipolar	Continuous	$1/(1-D)$	1	1	1	1
Buck-Boost	Unipolar	Discontinuous	$D/(1-D)$	1	1	1	1
Isolated DC-DC	Various	Various	Various	1 - 4	1 - 4	1 - 5	1
Cuk	Unipolar	Continuous	$-D/(1-D)$	1	1	2	2
SEPIC	Unipolar	Continuous	$D/(1-D)$	1	1	2	2
(CI-)CCS	Bipolar	Continuous	$2D/(1-D)$	1	2	3	4



(a) Boost converter topology.

(b) Buck-boost converter topology.

(c) Cuk converter topology.

(d) SEPIC converter topology.

Figure 2.12: Topologies of various DC-DC converters commonly used in PV applications.

system efficiency. The low input current ripple in the proposed converter will keep the PV system closer to its MPP, further improving the overall power extracted. Further discussion of the proposed converter's efficiency is left for Section 5.2.

2.3.1 Boost Converter

As the name suggests, the standard boost converter (shown in Figure 2.12a) is capable of producing an output voltage which is higher than its input voltage. They have the lowest component count of the DC-DC converters covered in this section, making them very cost effective. The boost converter's switch is ground-referenced, further reducing its gate driver cost, and input structure gives rise to a continuous input current - a benefit for solar PV applications. One drawback of this converter when compared with other converters in this section is the voltage conversion ratio, restricting the converter from providing a reduced output voltage and thus limiting its application flexibility.

2.3.2 Buck-Boost Converter

The single-switch buck-boost converter (shown in Figure 2.12b) addresses the limitation of the boost converter by performing step-down voltage changes, into addition to step-up. One key difference is that the output voltage is inverted in polarity with respect to the input voltage. Buck-boost converters have the same low component count as the standard boost converter, however the switching device is not ground-referenced, increasing the cost and complexity of its gate

driver. The major drawback of this converter for solar PV applications is its discontinuous input current - necessitating a large decoupling capacitor to ensure smooth current flow from the PV array in order to operate close to the MPP.

2.3.3 Isolated DC-DC Converter

There are several isolated DC-DC converter topologies, including the forward, flyback, push-pull, isolated full bridge, and isolated half bridge [70–75]. Most of these topologies are capable of providing both step-up and step-down voltage change ratios [76–78]. The nature of the input current (continuous or discontinuous) and the size of the ripple are dependent on the topology [79–81]. The number of active switching devices ranges from one to four, and the magnetics can range from a single inductor to four-winding transformers [82–84]. The inclusion of an isolation transformer and extra power devices increases the costs of these converters and decreases their efficiencies [85–87].

2.3.4 Cuk Converter

The Cuk converter (shown in Figure 2.12c) is capable of both step-up and step-down voltage change ratios, though the output is inverted in polarity with respect to the input, as with the single-switch buck-boost converter [88]. Unlike the buck-boost converter however, its input current is continuous, alleviating the need for a bulky decoupling capacitor between the PV array and the Cuk converter's input. Another advantage of the Cuk converter over the buck-boost converter is that the switch is ground-referenced, allowing a cheap, simple gate driver to be used. This converter does have a higher component count however, with an extra inductor and capacitor required. The magnitude of the input current ripple may be a problem for solar PV applications, though the Cuk converter's inductors may be coupled to reduce this - a concept that will be examined closely in Chapter 4.

2.3.5 SEPIC Converter

The SEPIC converter (shown in Figure 2.12d) shares many similarities with the Cuk converter - both converters have the same component count, ground-referenced switch, voltage gain ratio, and continuous input current shape [88]. The most notable operational difference between the two converters is the polarity of the output voltage: the SEPIC converter has a positive magnitude output voltage, in contrast

to the negative polarity output voltage produced by the Cuk converter. Again, the size of the input current ripple may be problematic in solar PV applications, though the SEPIC converter's inductors may be coupled to reduce this - a concept that will be examined closely in Chapter 4.

2.4 DC-AC Power Converters

Following power processing by DC-DC converters, most solar PV applications will involve conversion of the generated power from DC to AC, either for export to an AC grid, or for self-consumption in AC loads in off-grid applications. When connecting to the utility network, the converters must comply with grid connection standards, including harmonic distortion, DC injection, and anti-islanding. Inverters used in PV applications only need to support unidirectional power flow, and the type of inverter selected depends largely on the power level of the system, which can broadly be classified into two categories:

- *Distributed generation:* These are small-scale, decentralised energy systems typically used in residential and small commercial/industrial applications. The majority of these PV systems are mounted on rooftops, and have a generation capacity of up to 150 kW [36]. Generally, residential installations are small enough that they would not require modifications to the utility network.

- *Utility-scale solar farms:* These systems are generally not intended to reduce self-consumption, but rather as a commercial ventures in themselves. The peak power output of these systems are typically measured in megawatts, with the largest system in the world capable of producing a staggering 1547 MW [89].

Two characteristics that differentiate the inverter requirements between these applications are that the small-scale systems normally connect to low-voltage grids, and generally require a single-phase output, whereas large-scale systems typically connect to the grid at medium-voltage or high-voltage, and require three-phase outputs. Large-scale systems would commonly use several two-level three-phase voltage source converters (VSC) and transformers, or larger multilevel inverters such as the diode clamped inverter (also known as the neutral point clamped inverter), or the flying capacitor inverter (also known as the capacitor clamped inverter) [90–92]. This thesis focuses on small-scale systems, so the converters presented in this section are the:

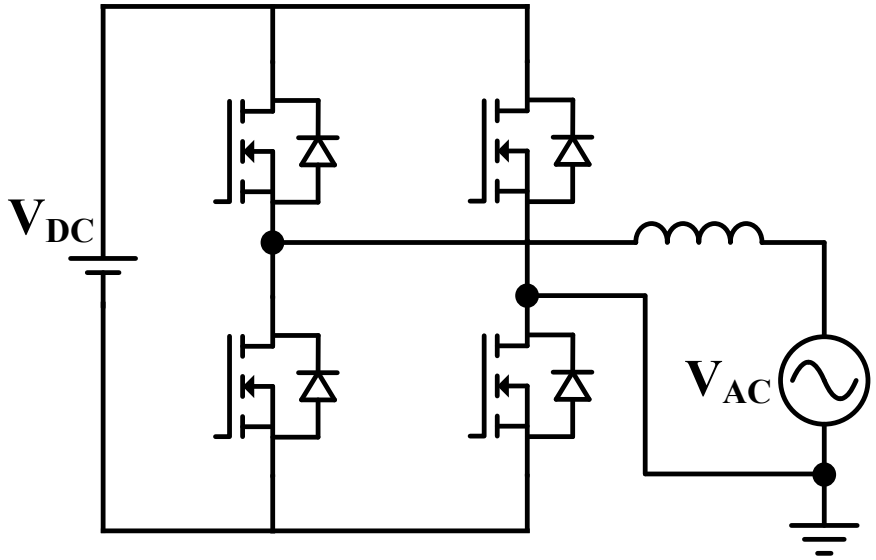


Figure 2.13: Full bridge (H bridge) inverter topology.

- Full bridge inverter (also commonly known as the H bridge inverter or the H4 inverter)
- Half bridge inverter
- Single-phase T-type inverter
- Decoupling inverters (HERIC, H5, H6)

A summarised comparison of the above inverters is provided in Table 2.4. This section then examines appropriate output filters to use with these inverters, and looks at the ability to use these inverters to control not only the active power, but also the reactive and harmonic in order to achieve voltage regulation, power factor correction, and harmonic cancellation.

2.4.1 Full Bridge Inverter

The single-phase full bridge inverter (Figure 2.13) has two inverter legs, each with two switching devices (typically MOSFETs or IGBTs) in series. The output filter and AC network are connected between the midpoints of each inverter leg. The inverter can be switched with bipolar or unipolar modulation schemes. With a bipolar modulation scheme, the available output voltages are $\pm V_{DC}$, and the effective switching frequency (seen by the AC network) is equal to the switching frequency of the individual semiconductor devices. With a unipolar modulation scheme, the available output voltages are $+V_{DC}$, 0, $-V_{DC}$, and the effective switching frequency is double the switching frequency of the individual semiconductor

Table 2.4: Summary of grid-interface inverters for domestic solar PV applications.

	Full Bridge	Half Bridge	T-Type	HERIC	H5	H6
Number of switching devices	4	2	4	6	5	6
- High frequency switches (f_s)	4	2	2	4	3	4-6
- Low frequency switches (f)	0	0	2	2	2	0-2
DC-side ground connection?	No	Yes	Yes	No	No	No
Common mode issues?	Yes	No	No	No	No	No
Minimum DC bus voltage	$\hat{V_{grid}}$	$2\hat{V_{grid}}$	$2\hat{V_{grid}}$	$\hat{V_{grid}}$	$\hat{V_{grid}}$	$\hat{V_{grid}}$

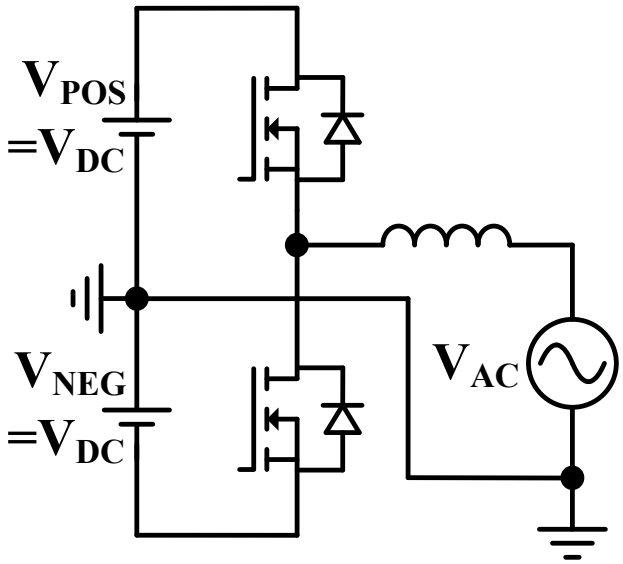


Figure 2.14: Half bridge inverter topology.

devices, meaning that a smaller, cheaper output filter can be used.

The converter's voltage output is required to be at least as big as the peak grid voltage (before considering voltage drops across the output filter and required overhead), so the DC bus voltage must be greater than $\widehat{V_{grid}}$. Compared with the half bridge and single-phase T-type inverters, the full bridge has the best DC bus utilisation, as the full DC bus voltage can be used to generate positive or negative output voltages.

The main drawback of the full bridge inverter for solar PV applications is the common mode voltage present on the DC bus. In Figure 2.13, as the right-hand leg (connected to the grid neutral point) switches, the positive and negative DC bus rails become alternately grounded. Thus, the positive DC bus rail jumps between $+V_{DC}$ and 0 V at the switching frequency, and the negative DC bus jumps between 0 V and $-V_{DC}$ (with respect to the AC grid's ground) [66, 93]. In addition to this high frequency component, the DC bus voltage contains a double power frequency ripple component, resulting from the nature of instantaneous power in single-phase inverters.

2.4.2 Half Bridge Inverter

The single-phase half bridge converter (Figure 2.14) utilises only a single inverter leg, consisting of two series-connected semiconductor switches (usually IGBTs, though MOSFETs are used at lower powers), and the output filter and AC network are connected between the midpoint of the inverter leg and the midpoint of the

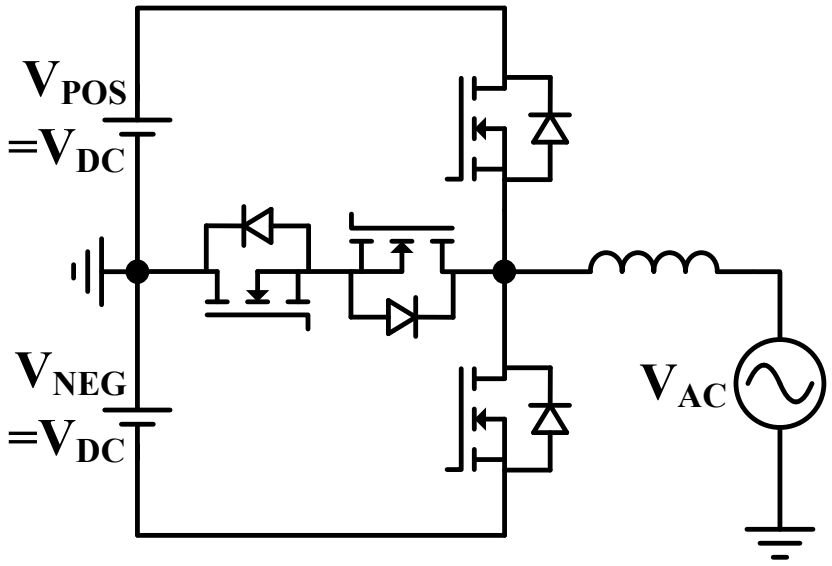


Figure 2.15: Single-phase T-type inverter topology.

DC bus. The keys benefit of this topology are a low number of semiconductor switches and the provision of a ground connection at the midpoint of the DC bus - fundamentally addressing the high frequency common mode voltage issue associated with the full bridge inverter [66, 93].

The half bridge inverter has two possible output states: $\pm V_{DC}$. As before, the converter's voltage output is required to be at least as big as the peak grid voltage, so the DC bus voltage must be greater than $2\widehat{V_{grid}}$, twice that of the full bridge inverter. This is one of the half bridge inverter's main disadvantages compared to the full bridge inverter. As power is drawn alternately from each bus during the positive and negative grid half cycles, there is also an added challenge in ensuring that both capacitors remain relatively balanced. If a bipolar input inverter has unequal positive and negative DC bus voltages then care must be taken when switching the inverter to prevent a DC offset in the output voltage. Current UK regulations limit DC current injection to 0.25% of the AC current rating (e.g. a DC limit of 22 mA for a 2 kW inverter connected to 230 V mains), because even small DC currents can saturate distribution transformers and electric machines. The lack of the zero output state in the half bridge inverter increases the harmonics present in the generated PWM output voltage, increasing the output filter requirements.

2.4.3 T-Type Inverter

The single-phase T-type inverter (shown in Figure 2.15) is similar to the half bridge inverter, however an 'AC switch' is added between the inverter output terminal and

ground. This AC switch - generally comprised of two back-to-back MOSFETs or IGBTs, each with an anti-parallel diode - allows for current conduction and voltage blocking in both directions [94]. The inclusion of this AC switch enables a zero voltage state to be produced in addition to $\pm V_{DC}$. This extra output voltage state reduces the harmonic content of the generated PWM output waveform, reducing the output filter size requirements. Thus, the size requirements of the T-type converter's output filter lie somewhere between that of the half bridge inverter and the full bridge inverter operated with a unipolar modulation scheme. The DC bus voltage requirements for the T-type inverter are equivalent to that of the half bridge inverter (and roughly double that of the full bridge inverter), but the DC bus capacitance requirements are slightly smaller. The reason for this will be discussed in Section 6.1. Like the half bridge inverter, the T-type inverter's grounded DC bus midpoint removes the high frequency common mode voltage issue associated with the full bridge inverter.

The two switches forming the inverter leg switch at high frequency (as with the half bridge inverter), however the extra two devices in the AC switch branch only operate at the grid frequency (in unity power factor operation). The operation of this inverter is detailed in [94].

Which converter is 'better' between the half bridge and single-phase T-type inverter depends largely on the application. The half bridge inverter has half as many switching devices, but the T-type inverter has lower output filter and DC bus capacitance requirements. The importance placed on these trade-offs will vary between applications, and a complete analysis for the domestic solar PV system considered in this thesis is provided in Section 6.1.

2.4.4 Decoupling Inverters

To address leakage current issues without the use of transformers, modified full bridge inverter topologies have been developed which decouple the DC input from the AC output at the switching frequency [67]. This decoupling can be on the AC side or on the DC side. Three popular topologies have been developed, which are studied in this section: the HERIC inverter (AC side decoupling), the H5 inverter (DC side decoupling), and the H6 family of inverters (DC side decoupling).

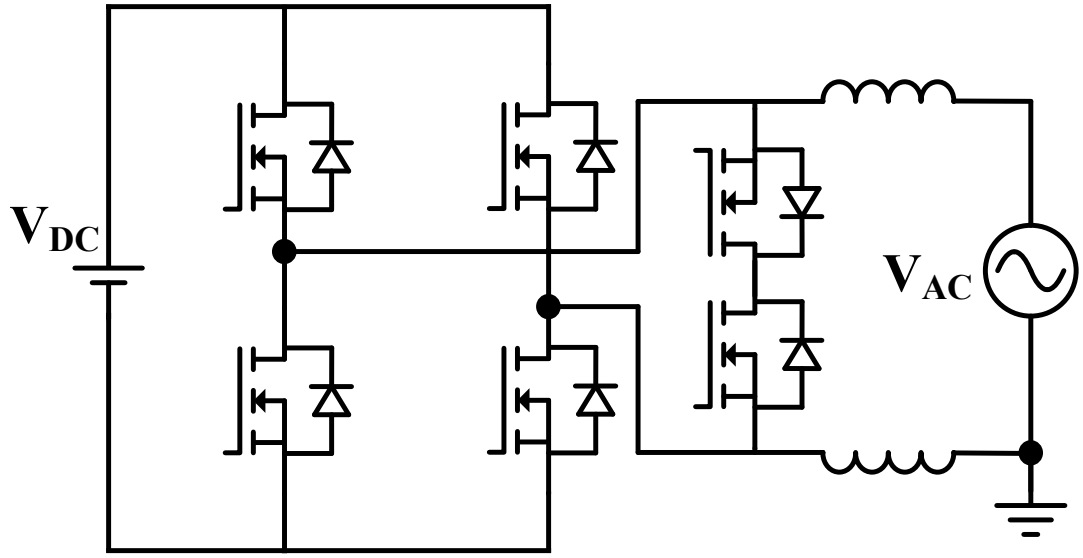


Figure 2.16: HERIC inverter topology.

2.4.4.1 HERIC Inverter

The 'Highly Efficient and Reliable Inverter Concept' (HERIC) converter, commercialised by Sunways, is a modification of the full bridge inverter aimed at maintaining its high efficiency and three output voltage states, while minimising the ground leakage currents [95, 96]. The full bridge is modified by adding an AC switch (also known as an AC bypass leg) in across the inverter's PWM output terminals, as shown in Figure 2.16. Like the T-type inverter, this AC switch is comprised of two back-to-back MOSFETs or IGBTs, each with an anti-parallel diode, allowing for current conduction and blocking in both directions. In the HERIC converter, these two power devices only switch at grid frequency. It is also possible to form this AC switch with two parallel branches, each consisting of a power device in series with a diode [97, 98]. The inclusion of the AC bypass branch has two important functions:

- Decoupling the PV array from the grid [99]
- Preventing reactive power exchange between the filter inductors and the DC bus capacitance during the zero voltage state, increasing the converter's efficiency [100, 101].

The power devices in the standard two inverter legs operate at switching frequency, however the power devices in the AC switch only operate at grid frequency (in unity power factor operation). The full operational details of the HERIC inverter are detailed in [97].

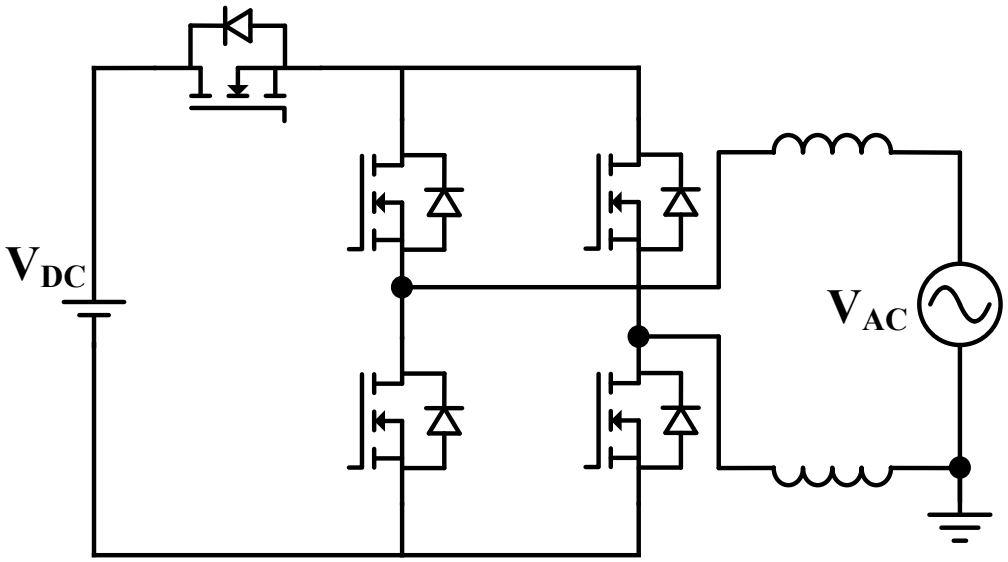


Figure 2.17: H5 inverter topology.

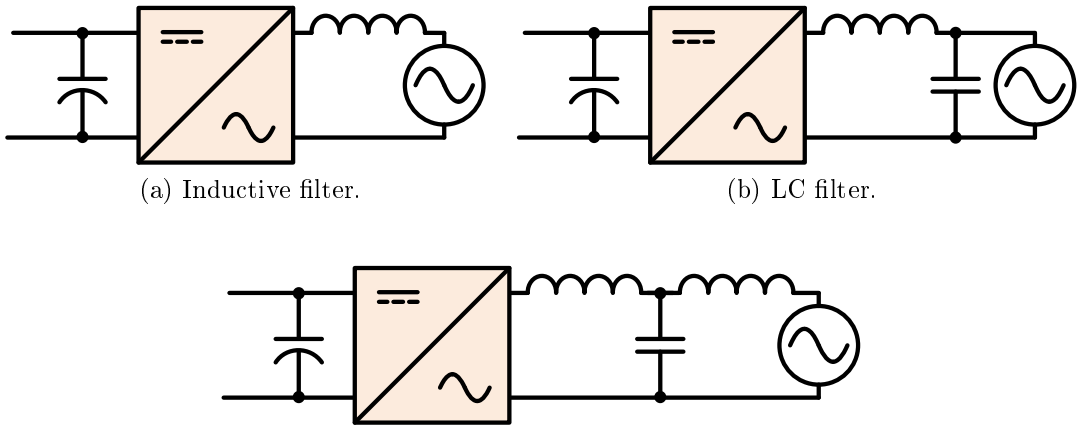
2.4.4.2 H5 Inverter

The H5 inverter, originally proposed in [102], is another modification of the full bridge inverter, formed by adding an additional switch between the positive terminal of the DC bus capacitance and the top of the inverter legs, as shown in Figure 2.17. The additional switch in the DC bus serves the same functions as the AC switch in the HERIC converter - namely isolating the PV array from the grid at specific times, and preventing reactive power exchange between the grid filter and the DC bus capacitance [103].

The top switches in each leg operate at grid frequency, and the lower switches operate at switching frequency. The additional DC bus switch also operates at switching frequency [104]. Even though the H5 inverter has fewer power devices than the HERIC inverter, the H5 inverter suffers from higher conduction losses due to the series association of three switches during the active phase [105]. It is also possible to operate the H5 inverter with reactive power, though this requires a modified switching strategy which further increases losses [97, 98].

2.4.4.3 H6 Inverter Family

Unlike the previous inverters, 'H6' refers to a family of transformerless inverters, rather than a single inverter topology, all based on the full bridge inverter [97, 106–110]. They all have six actively switched power devices, though the location of these changes between topologies. In [107], the two extra switches (in addition to the four full bridge switches) are placed on the positive and negative DC bus



(a) Inductive filter.

(b) LC filter.

(c) LCL filter.

Figure 2.18: Commonly-used AC grid filters.

nodes, between the full bridge and the DC link capacitors. In [97], two different H6 topologies are shown:

- One topology has the two extra switches between the bottom full bridge switches and the negative DC bus
- One topology has the extra switches on the positive and negative DC bus nodes, in between the full bridge legs.

In [111] and [112], a H6 inverter topology is shown which has one extra switch on the positive DC bus between the full bridge and DC link capacitor (as with the H5), and the other between either of the leg outputs and the positive terminal of the DC bus capacitor.

In general, H6-type inverters have lower conduction losses than the H5 inverter, but higher conduction losses than the HERIC inverter [97].

2.4.5 Grid Filter

All of the grid-connected inverter topologies studied in this section must be connected to the AC grid through an output filter to allow the linearisation of the stepped PWM voltage so that a smooth, sinusoidal current can be achieved. This is necessary as utilities around the world have requirements relating to power quality and total harmonic distortion (THD). As the switching frequency is increased, the filter requirements decrease, however this ease of filter design comes at the cost of increased switching losses.

The most commonly used filter is a purely inductive filter (shown in Figure 2.18a) due to its cost and control simplicity. It is straightforward to develop the dead-beat equation for this filter. A more advanced filter is the LCL filter (shown in Figure 2.18c), which reduces the grid current THD compared with a purely inductive filter [93]. This filter also allows the converter to be controlled as a voltage source largely decoupled from the load, in addition to a current source. The main drawback of the LCL filter is the resonance induced. This must be damped either passively through the use of a resistor which increases the difficulty of the filter design process, or actively with the use of complex control strategies [113]. The LC filter (Figure 2.18b) also allows the converter to be controlled as a voltage source, however it doesn't face the resonance challenges of the LCL filter. Its filtering capabilities are between that of the purely inductive filter and the LCL filter.

2.4.6 Reactive Power Control and Harmonic Cancellation

As inverter ratings are dependent on the current and voltage magnitude, ratings are generally given in kVA rather than kW. Grid-connected converters used for solar PV applications will typically operate at unity power factor, however when the converter is not using the full rating for real power, it is possible to utilise the spare kVA capacity to control the reactive output. This reactive power can be used for two main purposes:

- *Voltage regulation:* The grid voltage can be boosted by injecting reactive power into the network, or conversely the voltage can be reduced by making the converter act as reactive power sink. At low voltage, UK regulations specify that the supply must remain between 230 V -6% and +10%. National Grid and UK Power Networks are collaboratively working on the Power Potential project, which aims to create a new reactive power market for distributed energy resources. Voltage regulation works best on longer feeders as it relies on the grid's impedance.

- *Power factor correction:* By measuring the downstream current from the point of common coupling (PCC), the reactive power of the downstream can be calculated. By injecting this same reactive power (or as much as possible with the remaining converter capacity), the combined load of the converter and downstream network will look purely real. By reducing the reactive power flowing through the network, real power losses are reduced since the magnitude of the current is smaller. This also has the potential

to increase active power capacity as transmission and distribution lines are rated in current (or kVA at a given voltage), so a larger kW can be carried if the kVAr is reduced.

Controlling line-frequency reactive power alone will not entirely improve the power factor to unity because harmonics form part of the calculation in addition to the displacement power factor. It is also possible to monitor current harmonics on the network and cancel them by injecting anti-phase harmonics into the network.

2.5 Chapter Conclusion

This chapter introduced the technical concepts, challenges, and research in domestic solar PV systems. These systems were divided into three separate categories: PV arrays, DC-DC converters, and inverters. Some of the key issues identified include:

- Current ripple on PV panels negatively affecting the average power output
- Irradiance and PV module temperature variations requiring highly flexible power converters
- Common mode voltages introduced on the DC bus by grid-interface inverters
- Leakage currents flowing through the large parasitic capacitances associated with PV arrays
- DC leakage currents degrading PV panels due to dielectric polarisation.

The information presented this chapter forms the knowledge base for the rest of this thesis. The aim now is to develop a low cost, highly efficient, highly reliable DC-DC converter that addresses these issues in order to be seriously considered as an alternative to existing converters in an already well-established area.

Chapter 3

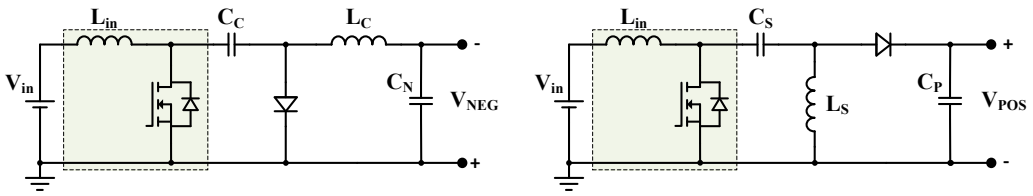
Combined Cuk-SEPIC Converter

The previous chapters illustrated the growing importance of solar photovoltaics and the challenges associated with harnessing the energy produced. This chapter examines the Combined Cuk-SEPIC converter and discusses its performance benefits, particularly for these solar photovoltaic applications. It then explains some design principles and provides simulation results for a 4 kW converter. Finally, it demonstrates the hardware design process for an experimental prototype, and presents its results.

3.1 Introduction to the CCS Converter

3.1.1 CCS Converter Topology and Features

The Combined Cuk-SEPIC (CCS) converter is based on the Cuk and SEPIC converters described in Section 2.3, and shown in Figure 3.1a and Figure 3.1b respectively. The information about these converters that is most pertinent to the CCS converter can be summarised as:



(a) Cuk converter (b) SEPIC converter

Figure 3.1: Topology of the Cuk and SEPIC converters.

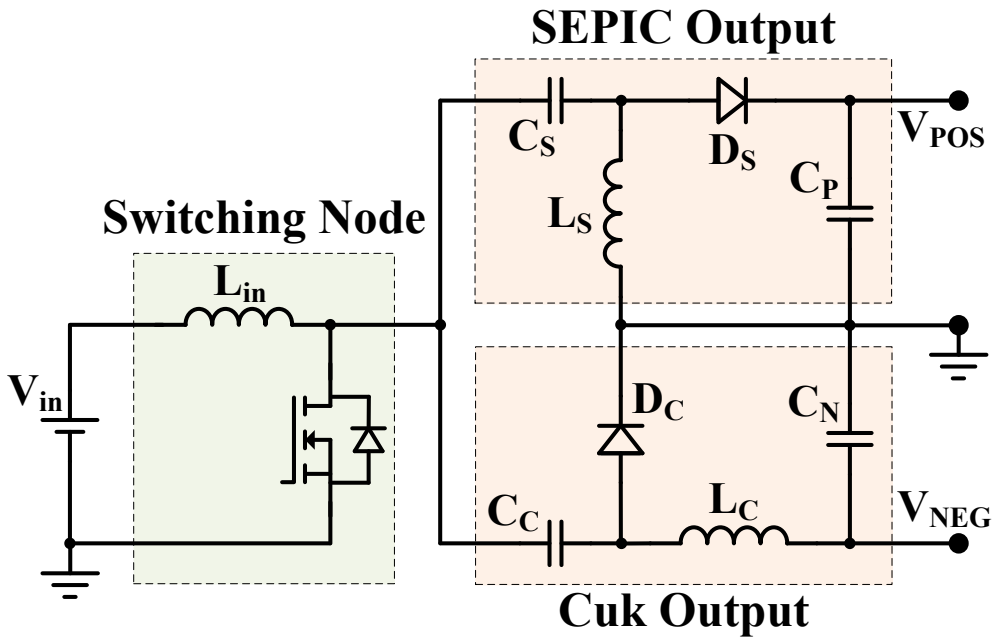


Figure 3.2: Topology of the CCS converter.

- They both produce an equal magnitude output voltage for a given input voltage and duty cycle, as they both operate with a voltage gain ratio of $\left|\frac{V_{out}}{V_{in}}\right| = \frac{D}{1-D}$
- The polarity of the output voltage is negative for the Cuk converter, and positive for the SEPIC converter
- They both have an identical input structure, as shown in Figure 3.1.

The CCS converter is formed by combining the input stages of the Cuk and SEPIC converters, and connecting their output stages in parallel [114–116], as shown in Figure 3.2. The CCS converter topology contains:

- *One switching device:* a ground-reference switching device in the input stage
- *Two diodes:* one for each of the Cuk and SEPIC outputs
- *Three inductors:* an input inductor plus an additional inductor for each of the Cuk and SEPIC outputs
- *Four capacitors:* an energy transfer capacitor plus an output capacitor for each of the Cuk and SEPIC outputs.

The CCS converter has not been used in solar PV applications before, but it has many characteristics that make it particularly well-suited for domestic single-phase applications:

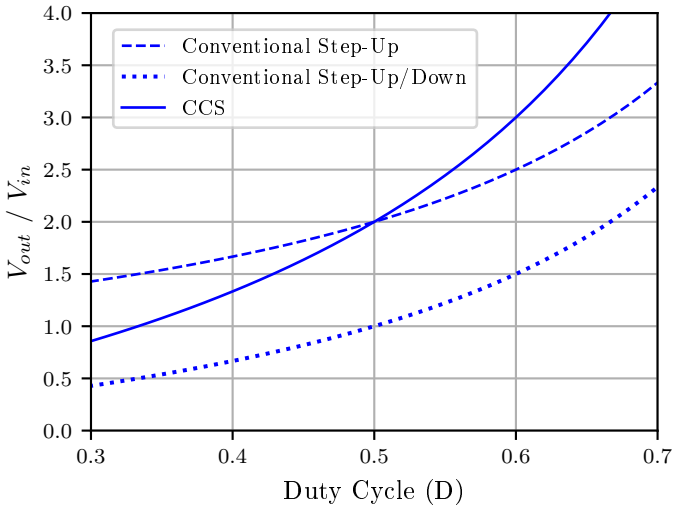


Figure 3.3: Voltage gain ratios for various converter types.

- *Low cost:* the converter only has one actively switched device, reducing the component cost and control complexity. This switch is ground-referenced, allowing a cheap, simple gate drive circuit to be used.
- *Leakage current elimination:* the converter is able to produce a balanced bipolar output, fundamentally addressing the PV grounding challenges outlined in Section 2.2.5.
- *Wide voltage transfer range:* the converter is capable of operating in both step-up and step-down modes, allowing regulation of the widely varying input voltages associated with PV systems. This large input voltage range stems from variations in the number of series-connected panels between PV systems, in addition to the time-varying irradiance conditions which change the PV array's I-V characteristics and MPP voltage.

The CCS converter can provide large step-up, as well as step-down voltage conversion ratios. The converter has an output/input ratio of $^{D}/_{(1-D)}$ for each of the positive and negative DC output terminals, providing step-up conversion for duty ratios greater than 1/2, and operating in step-down mode for duty ratios below 1/2. The converter's overall gain (i.e. considering the output voltage as the positive-to-negative voltage) is $^{2D}/_{(1-D)}$. This distinct output/input voltage ratio allows regulation of larger input voltage variations with the same duty cycle range, or alternatively allows the converter to handle the same input voltage variation with a narrower duty cycle range, allowing for smaller inductors to be used. Figure 3.3 shows the gain provided by different converter types for a range of duty cycles.

One drawback of this converter is its relatively large input current ripple, which

is equal to that of a boost converter with the same parameters (i.e. input voltage, input inductance, duty cycle, and switching frequency). This current ripple leads to reduced PV utilisation, or creates large input inductor or decoupling capacitor requirements, as described in Section 2.2.3. A solution to this issue is presented in Chapter 4.

3.1.2 Operation of the CCS Converter

The next step in the CCS converter analysis involves examining the converter topology in its different switching states. Like most DC-DC converters, the CCS converter can be operated in continuous conduction mode (CCM) or discontinuous conduction mode (DCM). DCM operation does have some advantages including higher efficiency (due to zero current turn-on), smaller inductors, and stability improvements. What constitutes DCM operation in the CCS converter is not immediately obvious. Most DC-DC converters have a single inductive element and two switched elements (usually a switch and a diode for unidirectional DC-DC converters). In these converters, the definition of DCM operation is quite simple: when the current in the sole inductor falls to zero during the 'off' state (referring to the switch being off and the diode being on). In DCM operation, the converter has a three switch states:

1. Switch on, diode off
2. Switch off, diode on
3. Switch off, diode off.

For converters like the Cuk and SEPIC converters, DCM operation is slightly more complicated, but still quite intuitive. The additional complexity arises because these converters have two inductive components, so the question arises whether these converters enter DCM when their input inductor current falls to zero or when their output inductor current falls to zero. In fact, neither of these define DCM. The converter must enter a third switch state to operate in DCM, so for these converters the diode current must fall to zero. This occurs when the sum of the two inductor currents is zero, and only then does the diode turn off, producing the DCM switch state [117].

Now it is clear why defining DCM operation in the CCS converter is not straightforward. The difficultly comes not just from the presence of three inductors, but from the additional switching device. Having one switch and two diodes produces

not three, but five feasible switch states, which can occur in nine ways depending on the inductor currents:

1. *Switch on, both diodes off:* Shown in Figure 3.4a
2. *Switch off, both diodes on*: Achievable in five ways - shown in Figures 3.4b-3.4f
3. *Switch off, SEPIC diode on, Cuk diode off:* Shown in Figure 3.4g
4. *Switch off, SEPIC diode off, Cuk diode on:* Shown in Figure 3.4h
5. *Switch off, both diodes off:* Shown in Figure 3.4i.

Here, there are three possible DCM states relating to the last three switch states listed. Within a single switching subinterval, it is clearly not possible to enter both the third and fourth switch states listed, and which of these is entered depends on various converter parameters, including the load connected to each output, and the size of the passive devices in the converter.

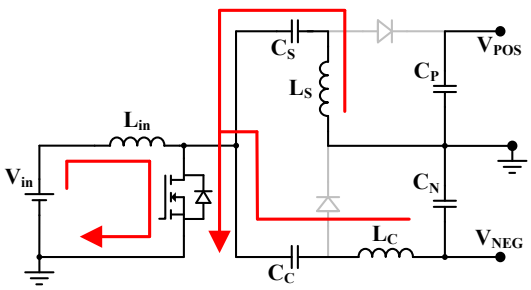
For the solar PV application considered in this thesis, CCM operation should be maintained. From the input current perspective, the importance of maintaining low ripple has been outlined in Section 2.2.3. From the output current perspective, maintaining CCM ensures that the output voltage does not become load-dependent, and helps reduce capacitor size requirements. Thus, only the first two switch states are considered.

While in CCM, the CCS converter can be separated and analysed in two operational states:

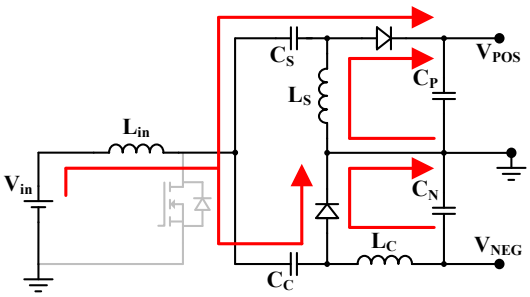
1. The switch 'on' state, shown in Figure 3.4a, where the switching device closed (treated as a short circuit) and both diodes are reverse-biased (treated as open circuits).
2. The switch 'off' state, shown in Figure 3.4b, where the switching device open (treated as an open circuit) and both diodes are forward-biased (treated as short circuits).

The steady-state CCM operation is explained as follows (assuming ideal components to improve clarity):

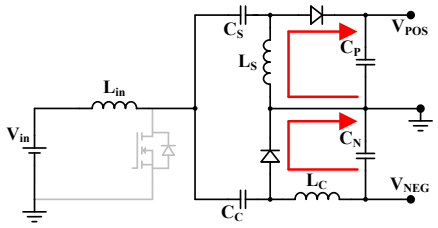
1. *Switch 'on' state (Figure 3.4a):* During the switch 'on' state, the right-hand side of the input inductor is shorted to ground, causing its current to rise according to $V_{in} = L_{in}\frac{di_{in}}{dt}$ and increasing the energy stored in its magnetic field according to $E_{L_{in}} = \frac{1}{2}L_{in}i_{in}^2$.



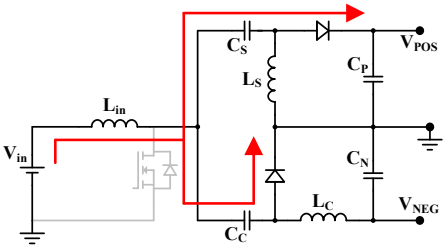
(a) 'On' state.



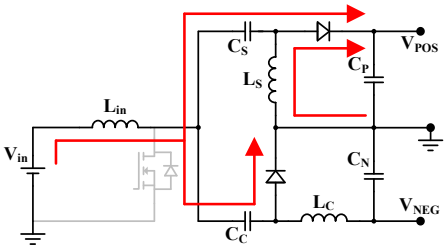
(b) 'Off' state.



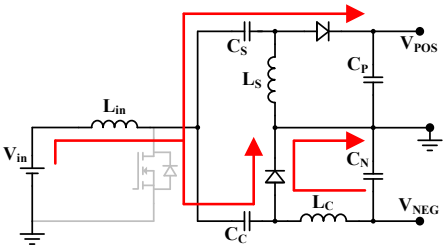
(c) Switch state 3.



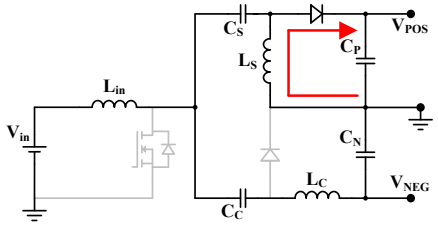
(d) Switch state 4.



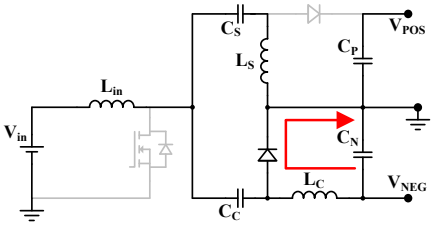
(e) Switch state 5.



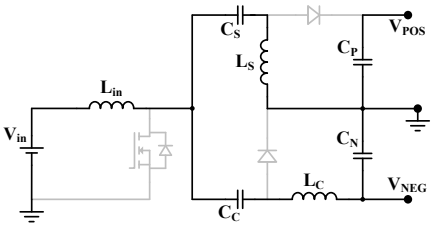
(f) Switch state 6.



(g) Switch state 7.



(h) Switch state 8.



(i) Switch state 9.

Figure 3.4: Operational states of the CCS converter.

2. *Switch 'off' state (Figure 3.4b):* When the switch is turned off, the inductor tries to maintain its current flow by generating a positive voltage across it. As the left-hand side of the inductor is clamped at the input voltage, the voltage on the right-hand side of the inductor is above the input voltage. This causes the inductor current to flow into the Cuk and SEPIC transfer capacitors, and through the now forward-biased diodes. In this process, the inductor is transferring some of the energy stored in its magnetic field to the capacitors, causing their voltages to rise according to $I = C\frac{dV}{dt}$ and $E = \frac{1}{2}CV^2$, while the input inductor current falls because the voltage across the inductor is now negative due to the right-hand side voltage being greater than the input voltage (i.e. it is discharging).

   (a) In the SEPIC (positive) output stage, this current flows through the now forward-biased diode to the output terminal, charging the capacitor and supplying the load.

   (b) In the Cuk (negative) output stage, this current flows through the diode to ground.

3. *Switch 'on' state (Figure 3.4a):* The positive terminals of both the Cuk and SEPIC energy transfer capacitors are now grounded through the switch, meaning that their right-hand side terminals are at a negative potential with respect to ground.

   (a) As the SEPIC inductor is connected between this capacitor's negative potential terminal and ground, a positive voltage appears across it causing current to rise its current to increase. This current flows from its ground-connected terminal, through the inductor, through the SEPIC energy transfer capacitor, and through the switch to ground. This causes the energy stored in the SEPIC energy transfer capacitor to be transferred to the SEPIC inductor. Since the SEPIC diode is reverse-biased, the positive output capacitor is supplying the load, causing its voltage to drop as it discharges.

   (b) A negative amplitude square wave voltage has been created at the right-hand side of the Cuk energy transfer capacitor. This voltage is applied to the LC filter which averages this square wave voltage to produce a smooth negative DC output voltage. During this switch 'on' state, the voltage on the left-hand side of the output inductor has a greater magnitude than the voltage on the right-hand side of the inductor, causing its current to increase. This causes energy stored in the Cuk

Table 3.1: Summary of component behaviour in steady-state CCM operation of the CCS converter.

	Switch 'on' state	Switch 'off' state
L_{in}	Charging	Discharging
L_S	Charging	Discharging
L_C	Charging	Discharging
C_S	Discharging	Charging
C_C	Discharging	Charging
C_P	Discharging	Charging
C_N	Both (LC circuit)	Both (LC circuit)

energy transfer capacitor to be transferred to the Cuk inductor.

4. *Switch 'off' state (Figure 3.4b):* The current through both output inductors continues to flow, however rather than flowing through the transfer capacitors, the inductors instead discharge their energy through the diodes to the output.

   (a) In the SEPIC output, the inductor not only supplies the output, but also recharges the positive output capacitor.

   (b) In the Cuk output, the capacitor recharges and discharges out of phase with the current, as an LC circuit is present.

In reality, this four-step process is actually just two steps, and the extra steps listed here have been provided simply to provide clarity in explaining the operation. A summary of the above is provided in Table 3.1.

The CCS converter also solves an issue faced by Cuk, SEPIC, and boost converters when their loads are disconnected. If any of these converters are left unloaded then energy is continually 'forced' into their capacitors, causing their voltage to rise until a component fails due to overvoltage. In the CCS converter, either of the outputs can be left unconnected without causing these same problems (if the other output has a load connected). This is because an energy transfer path exists to the other output, preventing energy from continually being 'forced' into the capacitors of the unloaded output. This aspect will be studied in Section 5.3, where the converter's performance is analysed under unbalanced output conditions.

Table 3.2: Design specifications for the CCS converter.

(a) Performance requirements.

Nominal input voltage (V_{in})	360 V
Input voltage range	294 V to 440 V
Nominal output voltage (V_{out})	±360 V
Output power (P_{out})	4 kW (2 kW per output)
Input current ripple ($\Delta i_{L_{in_{max}}}\%$)	40% peak-peak (at rated power)
Output voltage ripple ($\Delta v_{C_{P/N_{max}}}\%$)	2% peak-peak (at rated power)

(b) Design objectives.

Switching frequency (f_s)	100 kHz
L_S and L_C current ripple ($\Delta i_{L_{S/C_{max}}}\%$)	40% peak-peak (at rated power)
C_S and C_C voltage ripple ($\Delta v_{C_{S/C_{max}}}\%$)	10% peak-peak (at rated power)

3.2 CCS Converter Design

3.2.1 Specifications and Constraints

The first step of the CCS converter design process is to define the specifications, which can be broadly separated into two categories:

1. *Performance (primary) requirements:* These are the criteria required by the end-user's application, and are visible *external* to the converter. These criteria *must* be met, and typically relate to the converter's input and output performance, but could also include physical properties, such as size and weight.

2. *Design (secondary) objectives:* These are guiding design parameters that are *internal* to the converter and hence are not directly visible to the end-user's application. These criteria are therefore more flexible, and typically relate to constraining the design to reduce cost and increase efficiency.

Summaries of these primary and secondary objectives are provided in Table 3.2a and Table 3.2b respectively. These specifications have been obtained as follows, but as this is intended as a proof of concept, the specifications are arbitrary to some degree:

- *Output power:* The final aim is to have a 1 kW output from the inverter. The explanation of how this translates to a 4 kW DC-DC converter output power is provided in Section 3.2.2.

- *Nominal output voltage:* As this converter is paired with a bipolar input inverter, each DC bus voltage is required to be at least as large as the peak AC voltage. Adding a 10% buffer gives ±360 V ($230\sqrt{2} + 10\% \approx 360$).

- *Input voltage:* Producing a 1 kW output using 40 W series-connected PV panels requires 25 panels. Each panel has a voltage range of 12 V - 17 V, giving an overall voltage range of 300 V - 425 V. With the 360 V nominal output, this corresponds to a duty cycle range of D ≈ 0.459 to D ≈ 0.545. Adding some buffer and extending this slightly to D = 0.5 ± 10% (with 0.5 as nominal) gives an input voltage range of 294 V to 440 V, with a nominal input voltage of 360 V. The input current range for a 1 kW output is 2.3 A to 3.4 A, and for a 4 kW output the input current range is to 9.1 A to 13.6 A.

- *Input current ripple:* In Section 2.2.3, it was determined that the PV array should operate with a current ripple of less than 5% to ensure high levels of energy extraction. Despite this, a more relaxed target (40%) is set for now, for reasons that are explained in Section 3.2.3.

- *Output voltage ripple:* DC-DC converters commonly have output voltage ripples of between 2% and 5%. In this application, a 2% target was selected to demonstrate the converter is capable of performing similarly to other converters with practical component values.

- *Switching frequency:* To reduce the size of the magnetic components and capacitors, a high switching frequency is necessary. In this application a 100 kHz switching frequency has been selected to produce practical inductances and capacitors (discussed in Section 3.2.4), and to justify exploring new power device and magnetic core technologies (discussed in Section 3.4).

- *SEPIC and Cuk inductor current ripple:* The internal inductor (L_S and L_C) current ripple is set with similar principles to the input current ripple.

- *SEPIC and Cuk capacitor voltage ripple:* The energy transfer capacitor (C_C and C_S) voltage ripple is not as constrained as the output voltage ripple, since it is internal to the converter. Smaller capacitors may be used with a more relaxed ripple target, however the ripple must still be sufficiently small to use linear approximations when analysing the circuit. Thus, a target of 10% has been selected.

It should be noted that the ripple percentages are given at at the full output power (4 kW). The magnitude of the current ripple is largely constant for a given input

voltage, and so the percentage ripple will increase at lower power outputs.

In particular, the design objectives (switching frequency, internal inductor current ripple, internal capacitor voltage ripple) have large degrees of flexibility, as these are parameters selected by the designer and not determined by the application. Here, values have been selected somewhat arbitrarily to guide the design, but Section 4.5 provides a discussion of how these could be changed to meet other objectives.

Finally, with these design specifications, it is necessary to determine the required inductances and capacitances, as well as the voltage and current ratings for all passive and active components.

3.2.2 Converter Rating Analysis

The peak power ratings of both the DC-DC converter and inverter for single-phase grid-connected PV systems are important considerations. Figure 3.5 shows the CI-CCS converter feeding a bipolar input inverter, with some energy storage present on the DC bus to decouple the 100 Hz power fluctuations caused by the single-phase system. For a 1 kW average AC output power, the peak instantaneous power will be 2 kW, since the instantaneous power is given by $P_{out}(t) = \sqrt{2}V_{rms}\sin(\omega t)\,\sqrt{2}I_{rms}\sin(\omega t) = \widehat{v_{AC}}\widehat{i_{AC}}\sin^2(\omega t)$.

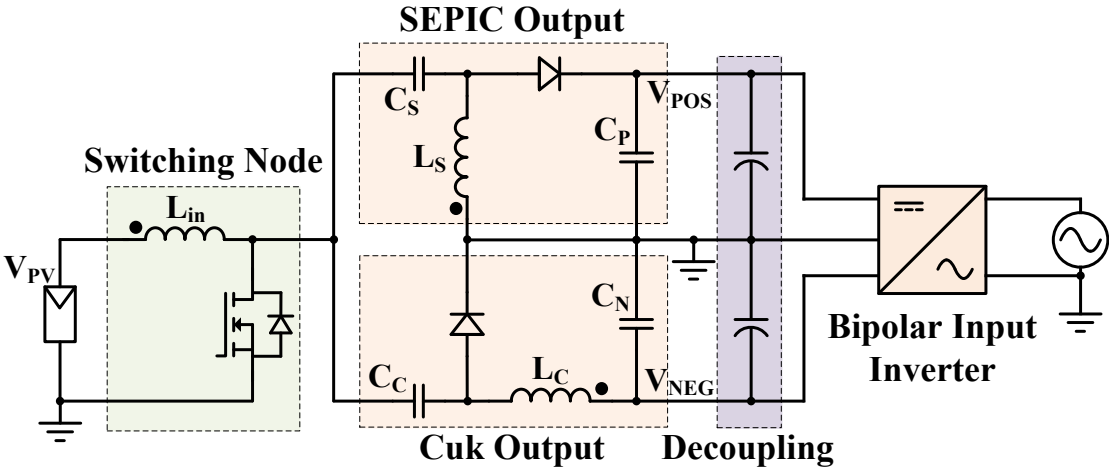


Figure 3.5: CCS converter feeding a bipolar input inverter.

If there is no storage present on the DC bus, then the CCS converter needs to be capable of supplying this 2 kW peak power on both of its positive and negative outputs (since this peak occurs in both the positive and negative cycles of the grid voltage). If there is no cyclical power de-rating of the CCS converter (i.e. its

continuous rating is conservatively set to the temporary peak power requirements) and if we pessimistically ensure that it can supply this peak power on both outputs simultaneously, then the converter must be rated to a total of 4 kW (i.e. 2 kW for each output). In this case, the power supplied to the DC input of the CCS converter will not be constant, but rather follow the same shape as the instantaneous AC output power. Thus, in this worst case scenario the power rating ratio of the CCS converter to inverter will be 4:1.

In reality, enough capacitance should be included in between the CCS converter and the inverter to decouple the 100 Hz ripple from the PV array, allowing it to produce a constant power output and maintain operation at its MPP. In this scenario, with the same 1 kW average AC output power, the input to the CCS converter will be a continuous 1 kW. This is supplied alternatively to the positive and negative outputs in each grid half cycle. Again, without cyclical power de-rating and ensuring the converter can supply 1 kW on both outputs simultaneously, the converter should be rated to a total of 2 kW (i.e. 1 kW for each output). Thus, in this scenario the power rating ratio of the CCS to inverter will be 2:1.

If the converter's rating is adjusted to account for the cyclical nature of the power supplied, then the power rating ratio of the CCS to inverter will be 1:1, since the average power supplied by the CCS converter is 1 kW, despite this coming alternately from each output.

Thus, the CCS converter's rating must be between 1x and 4x the inverter's average output power, depending on the storage present between the converters, and the level of de-rating applied. In this thesis, the converter prototype is conservatively designed for the worst case scenario (i.e. 4 kW peak power), but tested at 2 kW since sufficient capacitance is provided to ensure 100 Hz decoupling between the PV array and the grid.

3.2.3 Input Current Ripple Analysis

The input current of the DC-DC converter is equal to the current of the PV array (assuming no input decoupling capacitor is present). Thus, to ensure high levels of PV energy extraction, the input current ripple of the CCS converter should be 5% or less, as determined in Section 2.2.3.

Achieving such a small input current ripple would require an excessively large input inductor (discussed in Section 3.2.4), so a more relaxed target (40%) is set for now. If a 5% input current ripple target were enforced, then the input

inductance would need to be 8 times larger. Since the inductors form a large part of the converter's volume, an eightfold increase in the input inductance would massively increase the overall size of the converter. In the next chapter, the CCS converter will be modified in such a way that allows it to have drastically reduced input current ripple with the same inductance values.

Excessively large input current ripples have diminishing returns in inductor size reductions, and also increase the capacitor ESR losses (higher ripple currents through inductors must flow into the capacitors), inductor copper losses (higher rms current), inductor core losses (larger hysteresis loop size), and semiconductor losses (due to the high rms currents increasing conduction losses and the higher peak currents affecting switching losses) [118].

The 'ripple factor' (the ratio of peak-to-peak to average current, also known as the 'ripple current ratio') is defined as:

$$\gamma = \frac{\Delta i_L}{\overline{i_L}} \tag{3.1}$$

For the CCS converter, the peak-to-peak input current ripple can be calculated by considering the voltage across it during the switch 'on' state. Applying this, the ripple factor can written as:

$$\gamma = \frac{V_{in} D}{\overline{i_{L_{in}}} L_{in} f_s} \tag{3.2}$$

This should be written in terms of the output voltage (as this is the parameter typically being regulated). If the converter is assumed to be lossless, then the input power, $P_{in} = V_{in} I_{in}$, is equal to the output power, $P_{out} = 2V_{out} I_{out}$ (because of the bipolar DC bus). Thus, the ripple factor can be re-written as:

$$\gamma = \frac{V_{out}^2 (1 - D)^2}{P_{out} L_{in} D f_s} \tag{3.3}$$

The size of the inductor is related to its energy handling capacity, which is proportional to the 'area product' (AP) of the core, defined as [118]:

$$AP = \frac{L i_{peak} i_{rms}}{k_w J B_m} \tag{3.4}$$

where

L is the inductance

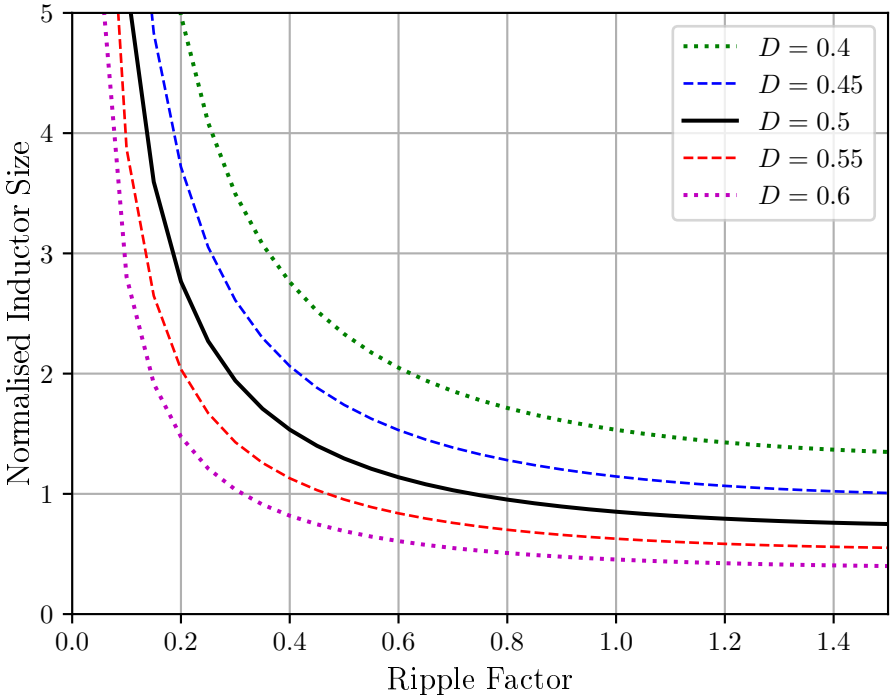


Figure 3.6: Normalised core size as a function of ripple factor and duty cycle.

i_{peak} is the peak inductor current, given by $i_{peak} = i_{average} + \frac{\Delta i}{2}$

i_{rms} is the rms inductor current, given by $i_{rms} = \sqrt{i^2_{average} + \frac{\Delta i^2}{12}}$

k_w is the fill factor of the core

J is the current density of the conductor

B_m is the maximum flux density of the core.

Using Equation 3.3, it is possible to re-write Equation 3.4 as:

$$AP = \frac{P_{out}}{4k_w J B_m f_s} \frac{(1-D)^2}{D} \frac{\sqrt{\left(1+\gamma+\frac{\gamma^2}{4}\right)\left(1+\frac{\gamma^2}{\sqrt{12}}\right)}}{\gamma} \tag{3.5}$$

Taking out the constant terms out of Equation 3.5, the normalised core size (relative to $\frac{P_{out}}{4k_w J B_m f_s}$) for the CCS converter's input inductor can be plotted as a function of the ripple factor, for a range of duty cycles, as shown in Figure 3.6. The knee point of the curves present a balanced trade-off between the inductor size and ripple factor.

It will be shown in Section 3.2.4 that the worst case input current ripple occurs at the highest input voltage (440 V) which produces the nominal output voltage (360 V) at a duty cycle of 0.45. The knee point for this curve is near a ripple

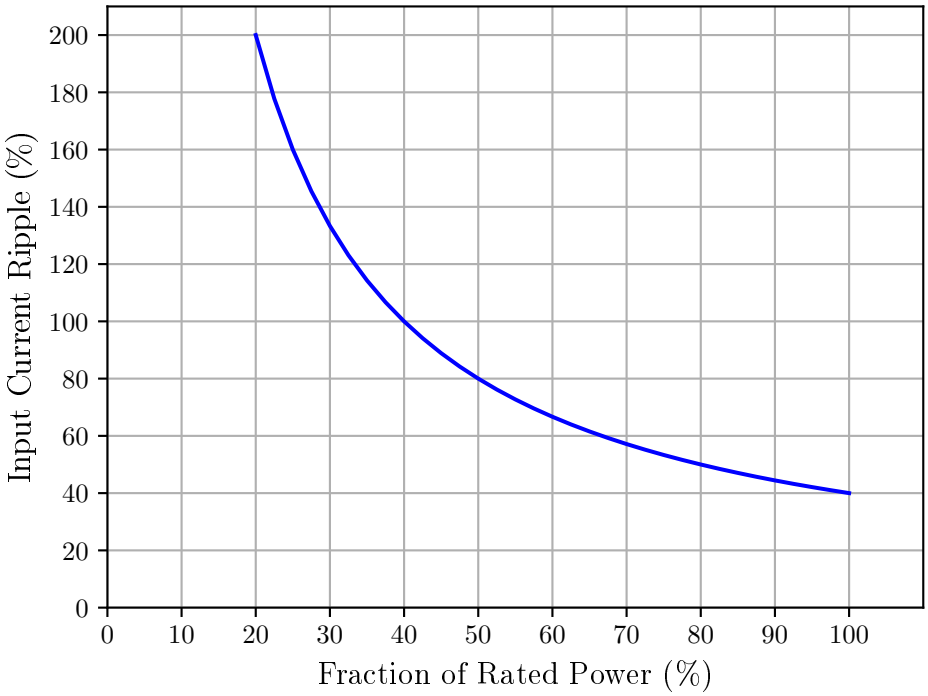


Figure 3.7: Input current ripple (%) as a function of output power.

factor of 0.4, producing the 40% peak-to-peak ripple target (of average current at rated load). The normalised inductor size is approximately 2, however if the peak-to-peak ripple target were set to 5% then the normalised inductor size would rise to almost 14.

Note that this 40% input current ripple target is specified at full load (4 kW) because the magnitude of the ripple is constant with input voltage and independent of output power. Thus, at lighter load conditions, the percentage ripple will increase, as shown in Figure 3.7, up to a maximum of 200% (as this is where the inductor current goes to zero).

This relatively relaxed input current ripple target also allows the benefits of the modified converter (introduced in the next chapter) to be clearly demonstrated.

3.2.4 Passive Component Sizing

Given a set of design specifications, it is possible to determine equations to size each of the inductors and capacitors. Analysing the CCS converter in the 'on' and 'off' states yields equations that describe the voltages across, and currents through, each of the various components. In steady-state operation, the principles of inductor volt-second balance and capacitor charge (amp-second) balance both hold, meaning that the change in inductor currents and capacitor voltages during

the switch 'on' state must directly oppose the changes during the switch 'off' state. Thus, using equations from either of these states in combination with the inductor and capacitor equations ($V = L\frac{di}{dt}$ and $I = C\frac{dv}{dt}$), produces expressions for inductances and capacitances as a function of other known parameters.

As there are seven of these components, these equations would be of a prohibitively high order (up to seven), so a simplifying assumption is needed. For this purpose, small ripple approximations can be applied, meaning that the ripple components of the waveforms can be neglected and the waveforms can be treated as their average values. It is also beneficial to assume ideal components, as this greatly reduces the complexity of these equations without significantly impacting their results.

This process results in the Equations 3.6 - 3.12:

$$L_{in_{min}} = \frac{V_{in}^2 V_{out}}{(V_{in} + V_{out})\, P_{out} f_s \left(\Delta i_{L_{inmax}}\%\right)} \tag{3.6}$$

$$L_{S_{min}} = \frac{2V_{in} V_{out}^2}{(V_{in} + V_{out})\, P_{out} f_s \left(\Delta i_{L_{S_{max}}}\%\right)} \tag{3.7}$$

$$L_{C_{min}} = \frac{2V_{in} V_{out}^2}{(V_{in} + V_{out})\, P_{out} f_s \left(\Delta i_{L_{C_{max}}}\%\right)} \tag{3.8}$$

$$C_{S_{min}} = \frac{P_{out}}{2V_{in}\,(V_{in} + V_{out})\, f_s \left(\Delta v_{C_{S_{max}}}\%\right)} \tag{3.9}$$

$$C_{C_{min}} = \frac{P_{out}}{2\,(V_{in} + V_{out})^2\, f_s \left(\Delta v_{C_{C_{max}}}\%\right)} \tag{3.10}$$

$$C_{P_{min}} = \frac{P_{out}}{2\,(V_{in} + V_{out})\, V_{out} f_s \left(\Delta v_{C_{P_{max}}}\%\right)} \tag{3.11}$$

$$C_{N_{min}} = \frac{P_{out} T_S \left(\Delta i_{L_{C_{max}}}\%\right)}{16 V_{out}^2 \left(\Delta v_{C_{N_{max}}}\%\right)} \tag{3.12}$$

Two important observations can be made from these equations:

1. As the converter is designed to operate with a range of input voltages, the worst case value of V_{in} should be used for each component. This means the maximum input voltage for inductors, and the minimum input voltage for capacitors.

2. Similarly, it should also be noted that P_{out} appears in the denominator for the inductor equations and the numerator for the capacitor equations. This means that the inductances required will be largest at the *minimum* output power, and the capacitances required will be largest at the *maximum* (rated) output power. Here, we will only consider performance at rated power,

Table 3.3: Passive component values for the CCS converter.

L_{in}	545 μH	C_S	1.04 μF
L_S	891 μH	C_C	0.47 μF
L_C	891 μH	C_P	4.25 μF
		C_N	0.39 μF

rather than over a defined output power range.

With the specifications given in Table 3.2, the passive sizing equations produce the component sizes listed in Table 3.3. In addition to determining the inductances and capacitances required, it is also necessary to know the peak currents and voltages they experience so that the components can be appropriately rated.

3.2.5 Component Current and Voltage Ratings

The previous section provided equations to determine the seven inductances and capacitances required to meet the design specifications for the CCS converter. This section provides twenty additional equations which describe the peak voltages and currents experienced by each of the ten devices in the converter (four capacitors, three inductors, two diodes, and one switch).

3.2.5.1 Peak Currents

The maximum currents in the input, SEPIC and Cuk inductors occur at the end of the switch 'on' state, and are equal to:

$$\widehat{I_{L_{in}}} = \frac{P_{out}}{V_{in}} + \frac{V_{in}V_{out}}{2\left(V_{in}+V_{out}\right)L_{in}f_s} \tag{3.13}$$

$$\widehat{I_{L_S}} = \frac{P_{out}}{2V_{out}} + \frac{V_{in}V_{out}}{2\left(V_{in}+V_{out}\right)L_{S}f_s} \tag{3.14}$$

$$\widehat{I_{L_C}} = \frac{P_{out}}{2V_{out}} + \frac{V_{in}V_{out}}{2\left(V_{in}+V_{out}\right)L_{C}f_s} \tag{3.15}$$

The maximum current flowing through the switch occurs at the end of the switch 'on' state and is equal to the sum of the input current and both output inductor currents:

$$\widehat{I_{switch}} = \widehat{I_{L_{in}}} + \widehat{I_{L_S}} + \widehat{I_{L_C}} \tag{3.16}$$

The maximum current flowing through the Cuk and SEPIC diodes occurs immediately upon entering the switch 'off' state (when both inductors have charged to

their maximum values and these currents are summed through the diodes). It is possible to assume the current is shared equally between both diodes, and is equal to:

$$\widehat{I_{D_s}} = \frac{\widehat{I_{L_{in}}}}{2} + \widehat{I_{L_s}} \tag{3.17}$$

$$\widehat{I_{D_C}} = \frac{\widehat{I_{L_{in}}}}{2} + \widehat{I_{L_C}} \tag{3.18}$$

With the assumption that the input current is shared equally between both outputs, the maximum current flowing through the Cuk and SEPIC energy transfer capacitors may occur at either the transition from the switch 'on' state to the switch 'off' state (where the current is half the input current), or the transition from the switch 'off' state to the switch 'on' state (where the current is the peak output inductor current):

$$\widehat{I_{C_S}} = \max\left\{\frac{\widehat{I_{L_{in}}}}{2}, \widehat{I_{L_S}}\right\} \tag{3.19}$$

$$\widehat{I_{C_C}} = \max\left\{\frac{\widehat{I_{L_{in}}}}{2}, \widehat{I_{L_C}}\right\} \tag{3.20}$$

The peak current in the positive output capacitor occurs at the beginning at the switch 'off' state, and the peak current in the negative output capacitor occurs as an LC circuit with the Cuk inductor:

$$\widehat{I_{C_P}} = \frac{P_{out}}{2V_{out}} + \frac{P_{out}^2}{8\left(V_{in}+V_{out}\right)V_{out}^2 C_P f_s} \tag{3.21}$$

$$\widehat{I_{C_N}} = \frac{V_{in}V_{out}}{2\left(V_{in}+V_{out}\right)L_C f_s} \tag{3.22}$$

3.2.5.2 Peak Voltages

The maximum voltage across the SEPIC and Cuk capacitors is equal to their average voltage plus half the peak-to-peak ripple voltage they experience. The ripple component is caused by the current flowing through the capacitors during the 'on' or 'off' state, and is obtained by rearranging $I = C\frac{dv}{dt}$. If we consider the 'off' state, and assume that the input inductor current splits evenly between the Cuk and SEPIC outputs - which is valid assumption when the outputs are balanced, and if they are not then the currents can simply be split in proportion

to each output power - then the following derivation can be made:

$$\widehat{V_{C_{S/C}}} = \overline{V_{C_{S/C}}} + \frac{V_{C_{S/C_{peak-peak}}}}{2} \tag{3.23}$$

$$= \overline{V_{C_{S/C}}} + \frac{\overline{i_{L_{IN}}} T_{off}}{4C} \tag{3.24}$$

$$= \overline{V_{C_{S/C}}} + \frac{P_{out}\left(1-D\right)}{4V_{in}C_{S/C}f_s} \tag{3.25}$$

$$\widehat{V_{C_{S/C}}} = \overline{V_{C_{S/C}}} + \frac{P_{out}}{4\left(V_{in}+V_{out}\right)C_{S/C}f_s} \tag{3.26}$$

Substituting their voltages, the peak voltages experienced by the SEPIC and Cuk capacitors can be expressed by:

$$\widehat{V_{C_S}} = V_{in} + \frac{P_{out}}{4\left(V_{in}+V_{out}\right)C_S f_s} \tag{3.27}$$

$$\widehat{V_{C_C}} = V_{out} + V_{in} + \frac{P_{out}}{4\left(V_{in}+V_{out}\right)C_C f_s} \tag{3.28}$$

Next, observing the circuit in the 'off' state reveals that the switch voltage is equal to the Cuk transfer capacitor voltage (neglecting the diode forward voltage drop). The switch voltage is at its maximum at the end of the 'off' state (when the capacitor has charged to its maximum voltage), so the peak switch voltage is equal to the peak Cuk transfer capacitor voltage:

$$\widehat{V_{switch}} = V_{out} + V_{in} + \frac{P_{out}}{4\left(V_{in}+V_{out}\right)C_C f_s} \tag{3.29}$$

Similarly, observing the circuit in the 'on' state reveals that the Cuk diode voltage is equal to the Cuk transfer capacitor voltage (neglecting the voltage drop across the switch). The Cuk diode voltage is at its maximum at the beginning of the 'on' state (before the capacitor has started to discharge), so the peak Cuk diode voltage is equal to the peak Cuk transfer capacitor voltage:

$$\widehat{V_{D_C}} = V_{out} + V_{in} + \frac{P_{out}}{4\left(V_{in}+V_{out}\right)C_C f_s} \tag{3.30}$$

The input inductor voltage is equal to the input voltage during the 'on' state, and is equal to the switch voltage minus the input voltage during the 'off' state:

$$\widehat{V_{L_{IN}}} = \max\left\{V_{in}\,,\, V_{out} + \frac{P_{out}}{4\left(V_{in}+V_{out}\right)C_C f_s}\right\} \tag{3.31}$$

The SEPIC inductor voltage is equal to either the SEPIC or positive output capacitor voltage, depending on whether the converter is in the switch 'on' or switch

'off' state, and similarly the Cuk inductor voltage may be equal to the difference between the Cuk and negative output capacitor voltages, or the negative output capacitor voltage itself depending on the converter's state:

$$\widehat{V_{L_S}} = \max\left\{\widehat{V_{C_P}}\,,\,\widehat{V_{C_S}}\right\} \tag{3.32}$$

$$\widehat{V_{L_C}} = \max\left\{\widehat{V_{C_N}}\,,\,\widehat{V_{C_C}} - \widehat{V_{C_N}}\right\} \tag{3.33}$$

The peak voltage across the positive output capacitor occurs at the transition between the switch 'on' and 'off' states, when the capacitor has charged to its maximum value, and the peak voltage across the negative output capacitor occurs as an LC circuit with the Cuk inductor:

$$\widehat{V_{C_P}} = V_{out} + \frac{P_{out}}{4\left(V_{in} + V_{out}\right) C_P f_s} \tag{3.34}$$

$$\widehat{V_{C_N}} = V_{out} + \frac{V_{in} V_{out}}{16\left(V_{in} + V_{out}\right) L_C C_N f_s^2} \tag{3.35}$$

The peak SEPIC diode voltage is equal to the difference between the SEPIC and positive output capacitor voltages, and occurs at the start of the switch 'on' state when these capacitors have charged to their maximum voltages:

$$\widehat{V_{D_S}} = V_{in} + V_{out} + \frac{P_{out}\left(C_S + C_P\right)}{4\left(V_{in} + V_{out}\right) C_S C_P f_s} \tag{3.36}$$

3.3 Simulation Results

Simulations of the CCS converter have been carried out using the Saber simulation platform to illustrate the converter's operation. All simulations in this thesis have been conducted with ideal components (i.e. zero resistance for the inductors, capacitors, and switch; no diode forward voltage drops; no switching losses; no blocking/leakage currents). The results are divided into three sections to validate the various explanations and derivations provided thus far in this chapter:

- *Operational waveforms:* Section 3.3.1 will provide waveforms to qualitatively validate the CCS converter's operation as explained in Section 3.1.2.
- *Passive sizing:* Section 3.3.2 will provide quantitative validation of the inductor and capacitor sizing expressions derived in Section 3.2.4.
- *Component ratings:* Section 3.3.3 will provide quantitative validation of the peak voltage and current expressions derived in Section 3.2.5.

3.3.1 Operational Waveforms

The component parameters used are those obtained in Section 3.2.4. The key waveforms at the nominal input voltage (360 V) and full output power (4 kW) are presented in Figure 3.8, demonstrating the process described in Section 3.1.2.

The plots on the left side show the full-scale currents and voltages, and the plots on the right side provide a vertical zoom into these same waveforms. It can be seen that the voltage output is a ±360 V bus with little imbalance and ripple. Both output inductor currents (I_{L_S} and I_{L_C}) are the same, and are each half the magnitude of the input current. The current ripple of the input is significant, and will be discussed in more detail in the sections and chapters to come. The voltages across all three inductors are plotted together and largely follow each other. The Cuk capacitor voltage (V_{C_C}) is roughly double that of the other three capacitors (V_{C_S}, V_{C_P}, V_{C_N}), which all experience approximately the same peak voltage. The large peak voltage experienced by the Cuk capacitor voltage appears to be similar to that experienced by both diodes (V_{D_S}, V_{D_C}) and the switch (V_{DS}).

With the operation of the CCS converter validated, it is necessary to check the accuracy of the expressions used to generate the inductance and capacitance values required to meet the design specifications.

3.3.2 Design Specification Verification

The converter has also been simulated at the limit voltages (294 V and 440 V) using the component values listed in Table 3.3, and the ripple components in these scenarios, along with the nominal input voltage scenario, are presented in Table 3.4. In this table, the maximum ripple value for each component is in bold, and the specifications are listed in the rightmost column.

It can be seen that for all targets, the ripple values measured are very close to theoretical expectations. It can be seen that the simulated ripples slightly exceed the specifications for i_{L_C}, v_{C_S}, v_{C_P}. These differences, along with all others seen in Table 3.4, arise primarily due to the small ripple approximation being applied during the derivation process. This approximation neglected high order ripple components which cause the discrepancies observed. Overall, the values obtained from the expressions are accurate and provide a solid foundation from which the design can be further optimised, if desired.

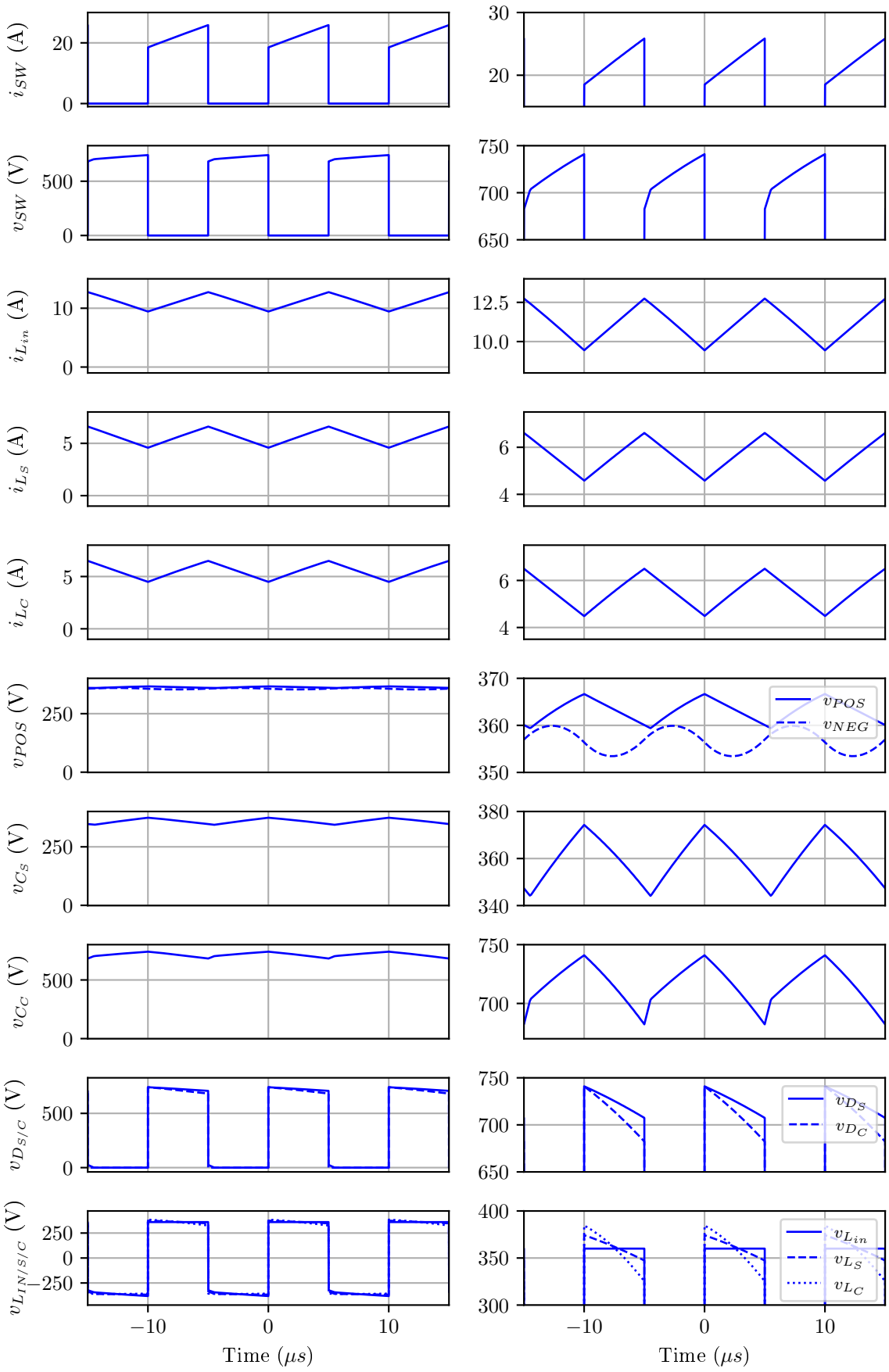


Figure 3.8: Switch current (i_{DS}), switch voltage (v_{DS}), $i_{L_{in}}$, i_{L_S}, i_{L_C}, v_{C_S}, v_{C_C}, $v_{POS/NEG}$, $v_{D_{S/C}}$, $v_{L_{in/S/C}}$ with $V_{in} = 360\,V$.

Table 3.4: Current and voltage ripple results from simulations at nominal and limit input voltages.

	Input Voltage			
	294 V	360 V	440 V	Target
$\Delta i_{L_{in}}$	21.80%	29.71%	**39.97%**	40%
Δi_{L_S}	32.53%	36.22%	**39.88%**	40%
Δi_{L_C}	32.88%	36.58%	**40.23%**	40%
Δv_{C_S}	**11.17%**	8.36%	6.22%	10%
Δv_{C_C}	**9.93%**	8.20%	6.64%	10%
Δv_{C_P}	**2.18%**	2.00%	1.81%	2%
Δv_{C_N}	1.63%	1.81%	**1.99%**	2%

Table 3.5: Peak currents and voltages with 4 kW output power and $V_{IN} = 360\,V$: simulations vs. theory.

	Peak current (A)			Peak voltage (V)		
	Simulations	Theory	Deviation	Simulations	Theory	Deviation
Switch	25.852	25.894	0.16%	741.0	749.551	1.14%
L_{in}	12.744	12.762	0.14%	381.0	389.551	2.20%
L_S	6.6097	6.566	0.67%	374.31	373.355	0.26%
L_C	6.4983	6.566	1.03%	384.57	385.99	0.37%
D_S	16.185	12.947	25.01%	741.0	736.623	0.59%
D_C	25.723	12.947	98.68%	741.0	749.551	1.14%
C_S	6.6097	6.566	0.67%	374.31	373.355	0.26%
C_C	6.4983	6.566	1.03%	741.0	749.551	1.14%
C_P	5.6587	5.606	0.94%	366.68	363.268	0.94%
C_N	1.0166	1.010	0.65%	359.96	362.686	0.75%

3.3.3 Component Rating Verification

The peak voltages and currents measured in the nominal input voltage case (with $P_{out} = 4$ kW) are shown in Table 3.5, which compares these measurements with the values theoretically expected using the equations obtained analytically in Section 3.2.5 in order to verify the accuracy of the derived expressions.

The results show that the percentage deviations from the theoretically derived values are small - just 0.88% for the peak voltages, and just 0.66% for the peak currents (with the exception of the diode currents).

The reason for the discrepancy in the diode peak currents, is that the theoretical approach assumed that both diodes started conducting simultaneously, immediately following the switch turn-off. In this scenario, the switch current is split equally between both diodes, so their peak is half of the switch's peak current. In reality, one diode will start conducting before the other, taking the full current

momentarily before sharing it with the other diode. Which diode turns on first, and the length of time before the other diode conducts, depends on the relative capacitance of the energy transfer capacitors. Thus, even though both diodes should ideally only conduct half of the peak switch current, in reality they should both be rated to handle the full peak switch current.

These results provide a strong validation of the equations previously derived. The minor discrepancies present stem primarily from the small ripple approximations made when deriving the equations, so the inductance and capacitance values should be tweaked slightly to ensure that the targets are met, starting from the base values obtained from the derived equations.

With these simulations results largely validating the theoretical design process, it is desirable to develop a prototype to experimentally verify these outcomes.

3.4 Experimental Prototype Design

It is necessary to design a prototype of the CCS converter in order to obtain experimental results. This section explains this design process with details of semiconductor technology selection, capacitor type selection, inductor design, and an exploration of the printed circuit boards (PCBs) used for the power circuit, gate driving, sensing, and control.

3.4.1 Semiconductor Technology Selection

The most popular semiconductor switch technologies presently used in SMPS applications are the silicon (Si) MOSFET and IGBT. MOSFETs and IGBTs are cheap, reliable and well understood. MOSFETS are faster than IGBTs, and offer good performance in lower power applications. They suffer high conduction losses above 100 V and are typically rated to a maximum of 600 V. CoolMOS superjunction MOSFETs have been developed to reduce conduction losses, though issues exist with their switching performance (primarily peak reverse recovery).

In recent years, wide bandgap (WBG) devices have gained interest and popularity - specifically using semiconductor materials like silicon carbide (SiC) and gallium nitride (GaN). These WBG devices can withstand higher voltages and temperatures, and can switch much faster than conventional semiconductor devices.

Due to the high voltages in this application, standard silicon MOSFETs were

Table 3.6: Performance summary of transistor technologies.

	Si MOSFET	IGBT	GaN	SiC
Conduction	Poor	Fair	Excellent	Good
Switching frequency	Fair	Poor	Excellent	Good
Temperature stability	Good	Fair	Fair	Good
Electrothermal robustness	Good	Good	Poor	Excellent
Reliability	Good	Good	Poor	Fair
Cost	Excellent	Good	Poor	Poor
Common voltage rating	600 V	1.7 kV	650 V	1.2 kV

Table 3.7: Performance summary of diode technologies.

	P-N	SiC
Conduction	Good	Medium
Switching	Medium	Good
Temperature stability	Medium	Good
Electrothermal robustness	Medium	Good
Reliability	Good	Medium
Cost	Good	Medium

deemed unsuitable. Next, IGBTs were ruled out due to their relatively low switching speeds, therefore limiting the switching frequency and thus increasing the size requirements of the passive components. Despite the promising potential of GaN transistors, gate driving challenges and reliability questions are still impeding their widespread uptake.

Thus, SiC MOSFETs are chosen for this application, due to their high voltage ratings and switching frequencies. The specific switching device selected is the ROHM SCT3030KL (1.2 kV, 72 A, 30 mΩ) N-channel SiC power MOSFET. SiC power devices are efficient and are capable of high power densities. One drawback of SiC MOSFETs is their cost, though this is expected to decrease over time and SiC is expected to surmount the IGBT in 600 V to 3.3 kV applications. Another problem of SiC power devices is their negative bias temperature instability, which causes a reduction in the threshold voltage leading to potential catastrophic device failure in high current modules with parallel devices [119]. A summary of some of these key properties is provided in Table 3.6.

The other type of semiconductor device required in this converter is the power diode. The most common power diode technologies used in SMPS applications are the Schottky, fast, ultrafast, soft and SiC diodes. The main properties differentiating these diodes are their reverse blocking voltage, their forward voltage drop (determining on-state losses), and their reverse recovery characteristics (determining switching losses).

The junction topology used in Schottky diodes produces a lower forward voltage drop, and gives a fairly fast and soft reverse recovery characteristic, however this structure also limits their blocking voltage. Fast, ultrafast, and soft diodes have different reverse recovery characteristics, but SiC diodes exhibit almost no reverse recovery. Switching performance is prioritised in this application so SiC diodes have been selected. The specific diodes selected are the Infineon IDH10G120C5 (1.2 kV, 10 A, 41 nC) SiC Schottky diodes. A summary of some of these key properties is provided in Table 3.7.

3.4.2 Inductor Design

All the inductors used in this application are custom-made. Inductor design is a complex process with several variables and constraints. There are two main components to inductors:

- the magnetic core, which can be further divided into:
  - core material
  - core shape
- the windings, which can be further divided into:
  - type of windings (conductor material, cross-sectional area, number of strands)
  - number of turns

First, the core material must be selected. Some of the key properties that need to be considered when selecting the core material are the switching frequency, the material's saturation point, and the material's permeability. It is desirable to operate the core at a peak flux density that is below the saturation flux density of the core material. For DC line reactor applications like this one, this is a particularly salient point since there is a substantial DC current bias, pushing the core's flux towards saturation, as shown in Figure 3.9. For this reason, in inductor applications (unlike for transformers), low permeability is a desirable characteristic. Thus, though ferrite cores have typically been used in DC line reactor applications [120], nanocrystalline powder cores have an advantage due to their homogeneous low permeability [121]. Nanocrystalline powder cores are formed with distributed and controllable micro air gaps to achieve low permeability (normally from 60 to 120) in order to avoid saturation of flux density caused by the large DC currents, thus one single piece of magnetic core can be used for the

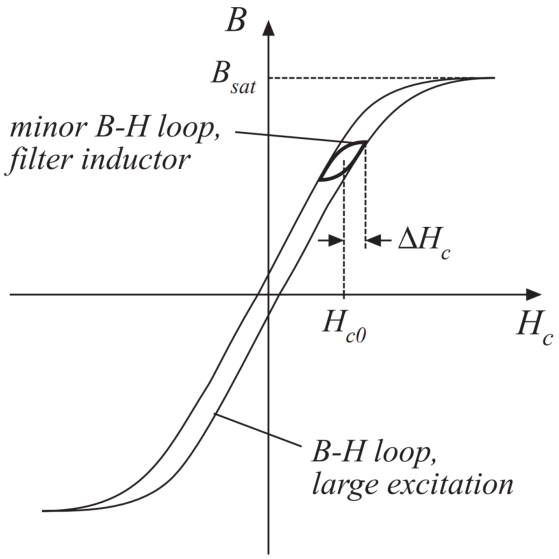


Figure 3.9: B-H curves [14].

inductor. Due to ferrite's naturally high permeability (normally several thousand) and low saturation point, additional air gaps must be inserted between ferrite core pieces when making the inductor in order to avoid saturation. This can lead to complex and difficult designs and inconsistent performance. Additionally, the saturation point of nanocrystalline-based materials is more than twice that of ferrite, which further supports the use of nanocrystalline powder cores in DC line reactors [122]. The core losses depend not only on the material selected (which determines the 'thickness' of the B-H loop), but also on the size of the ripple (which determines the width of the B-H loop). This is shown in Figure 3.9, where the minor B-H loop relates to the current ripple superimposed on the average inductor current, compared with the large B-H excitation loop which would relate to an application where the entire current is alternating (e.g. a transformer).

Next, the core shape and dimensions must be decided. As previously mentioned, nanocrystalline powder cores do not need additional air gaps, so toroidal cores are popular due to their uniform cross-sectional area. For ferrite cores, there are numerous geometries similar to E cores, which will require a specific air gap to dominate the inductor properties and prevent the core from saturating. The overall size of the core depends on the energy stored (given by $\frac{1}{2}LI^2$).

Once the core material, shape, and size have been determined, it is necessary to consider the windings. Typically, copper conductors are used, and a minimum cross-sectional area can be determined based on the current carried and the conductor's current density. The skin effect is the tendency for high frequency currents to be distributed near the surface of conductors. This effect predominantly affects AC inductors and transformers, and is usually not relevant for DC line reactors be-

cause the DC currents distribute evenly through the conductors. The skin depth, δ, where the current density reaches approximately 37% of its surface value can be calculated using:

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_r \mu_0}}$$

where

ρ is the resistivity

f is the signal frequency

μ_r is the relative permeability

μ_0 is the permeability of free space.

In situations where the ripple component of a DC current is significant then the skin effect may still need to be considered by reducing the effective cross-sectional area of the conductors. In these situations, larger gauge conductors may provide a sufficient conducting area, though this is an ineffective utilisation of copper, so smaller, stranded conductors are generally used. If possible, the effective cross-sectional area should be increased to be as large as possible above the minimum requirements in order to reduce the resistance (and hence copper losses), but these conductors should remain sufficiently small in order to fit the required number of turns in the core window. For a 100 kHz current ripple component in copper conductors, the skin depth is calculated to be $206\,\mu m$. Considering all factors, multistrand Litz wire is used for the inductors in this application.

Next, the number of turns required can be calculated using the desired inductance, core size, and core permeability. The 'fill factor' (also known as the 'window utilisation factor'), is a value between 0 and 1 that represents how much of the window area is occupied by conductors. In order for the desired number of windings to fit, the following must hold:

$$window\,area \times fill\,factor \geq number\,turns \times cross-sectional\,area$$

This can be an iterative process, for example if the core selected cannot fit the required number of turns, or if a different trade-off between copper and core losses is desired. The copper losses depend on the rms inductor current, which is close to its DC component when the ripple components are relatively small. Typically, these copper losses dominate the core losses (which can usually be ignored), and so the design is driven largely by the windings.

Table 3.8: Details of the capacitors selected in the CCS converter.

	Target	Part number	Capacitance	Voltage
C_S	1.04 μF	KEMET R71VN41504030K	1.5 μF	520 V
C_C	0.47 μF	Vishay MKP1840 447 104M	0.47 μF	1 kV
C_P	4.25 μF	Vishay MKP1848 550 704K2	5 μF	700 V
C_N	0.39 μF	KEMET R75MI33304030J	0.33 μF	400 V

3.4.3 Capacitor Type Selection

The two main types of DC capacitors used in SMPS applications are the electrolytic capacitor and the film capacitor. Electrolytic capacitors typically have lower voltage ratings and shorter lifespans due to evaporation of their non-solid electrolytes, causing decreases in capacitance and increases in their equivalent series resistance (ESR). By contrast, film capacitors are commonly rated up to 3 kV, however are only available in relatively low capacitance values. In this application, the capacitors experience relatively high voltages (e.g. the Cuk capacitor voltage can exceed 800 V), and only modest capacitances are required due to the high switching frequency. Thus, film capacitors are the most well-suited capacitors for this application. The specific capacitors selected are given in Table 3.8.

3.4.4 Power board

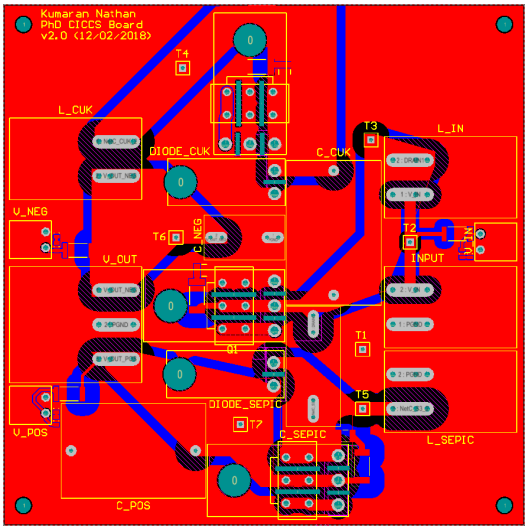
The initial PCB for the CCS converter included both the gate drive circuitry and power devices to minimise the overall converter size, however later revisions separated them to further reduce stray inductance in the power circuit. The final version of the power board prototype is shown in Figure 3.10. In designing a PCB for high power applications, there are three key considerations: current-carrying capacity, voltage ratings, and reduction of the stray inductance in the power circuit.

To ensure that the PCB can support the current requirements of the converter, a sufficient conductor cross-sectional area must be provided. This is achieved by:

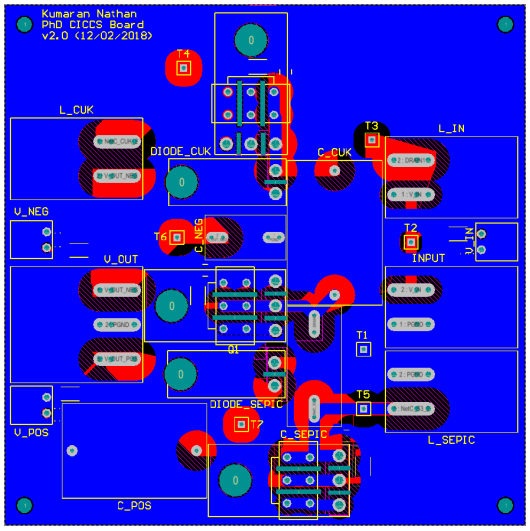
1. Increasing the copper thickness of the traces compared to a 'signal' or 'control' PCB

2. Using wider traces

3. Running traces on multiple PCB layers, though traces on inner PCB layers aren't easily cooled.



(a) Top layer.



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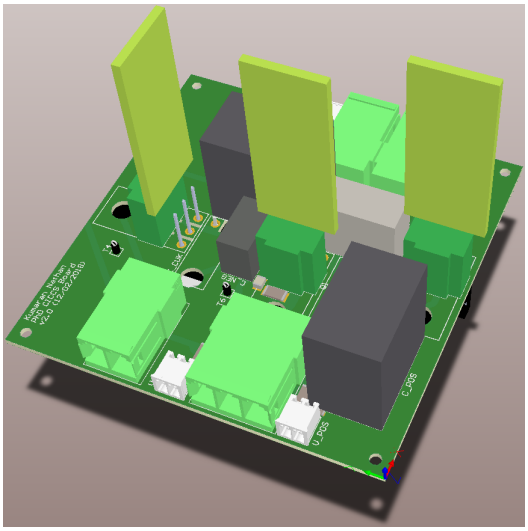
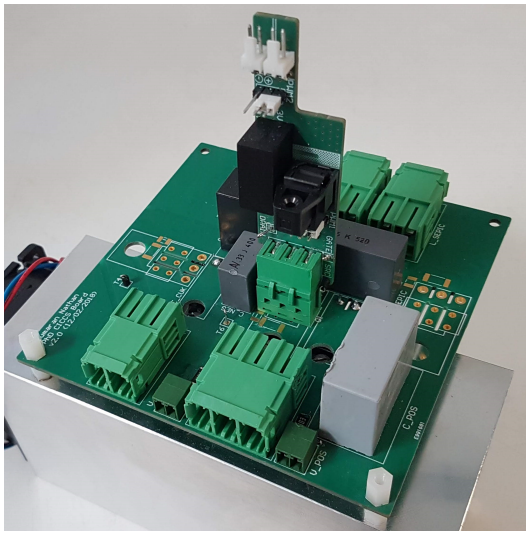


(c) 3D PCB model.



(d) Photo of developed PCB.

Figure 3.10: 4 kW CCS converter's power board PCB.

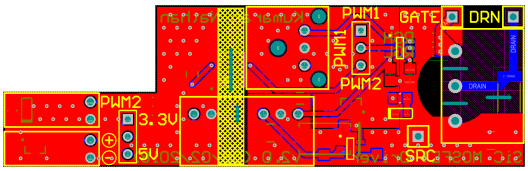
In this application, the PCB copper thickness was 35 μm, as the manufacturing costs go up substantially beyond this point. The PCB was designed with two layers, so traces were run on both layers. With this trace thickness and number of layers, to support a peak current of 26 A (shared over two layers) it was necessary to ensure a minimum trace width of 3.9 mm.

To support the voltages present between various nodes of the converter, it is necessary to ensure sufficient spacing (known as 'creepage' distances) between PCB traces to avoid flashover and tracking. The board itself is made of standard FR-4 glass epoxy which has breakdown voltage of 20 kV/mm. The standard PCB thickness from the selected manufacturer is 1.55 mm, so insulation between PCB layers is not an issue. For clearances on the same layer, the PCB design was guided by IPC-2221B (Generic Standard on Printed Board Design) and IPC-9592 (Performance Parameters for Power Conversion Devices). From Table 3.5, it can be seen that two common peak voltages that occur in this converter are approximately 750 V and 400 V, at the nominal input condition. For 750 V, the clearance should be at least 3.75 mm between exposed copper (e.g. component pads that will be soldered to), and 1.56 mm for coated copper (e.g. traces that have an epoxy-ink solder mask applied). For 400 V, these clearance requirements drop to 2.5 mm and 0.8 mm respectively. Note that for other input voltages within the defined input range, these peak voltages will be higher. Thus, the converter has been designed to the worst case conditions, with substantial extra margin to account for overshoot and ringing.

Beyond ensuring the PCB can support the currents and voltage present in the converter, proper component layout and trace routing is required to minimise the stay inductance of certain critical paths. These critical paths include any traces where large, fast changes in current are expected to occur - including the switch, energy transfer capacitors, and diodes. For these paths, careful planning has been undertaken to minimise the inductance by:

- Placing key components close together to reduce the trace length
- Increasing the trace width
- Using power planes and careful routing traces for the current return paths to minimise loop size.

The PCB designed also includes test points to easily measure the voltages at all nodes. One limitation introduced by optimising for inductance is that current sensing shunt resistors were removed - thus explicit current measurements are only possible for the input, outputs, and inductors. However, through an understand-



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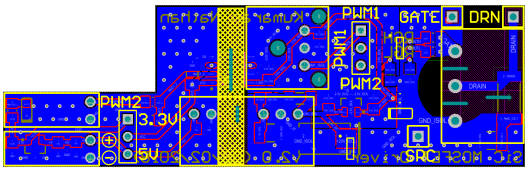

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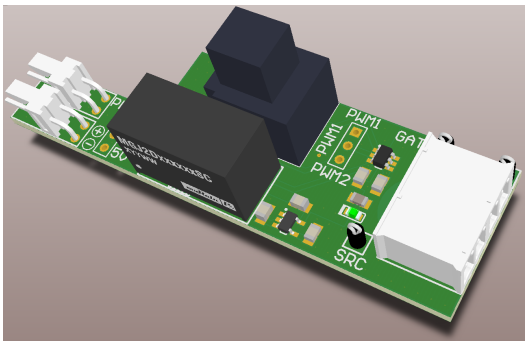
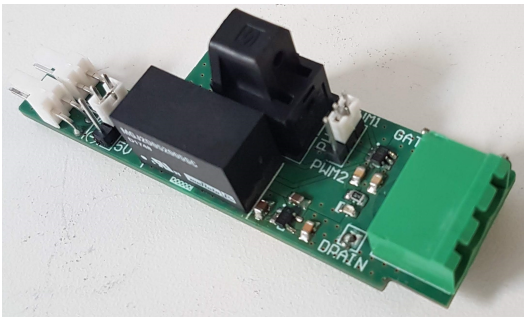


(c) 3D PCB model.



(d) Photo of developed PCB.

Figure 3.11: Isolated gate driving board.

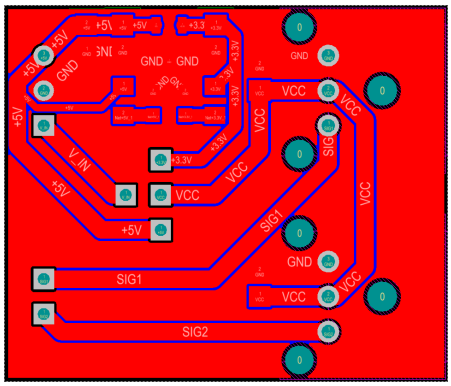
ing of the circuit's operation and applying Kirchhoff's current law, the currents through most other components can be implicitly obtained.

3.4.5 Gate Driving

As discussed in the previous section, a separate PCB was designed for the gate drive circuitry to allow the power board designed to be optimised (shown in Figure 3.11). Though not required for this application (due to the ground-referenced switch), the gate driver was designed with isolation included to maximise compatibility in other applications. The driver is powered with a 5 V supply, and the gate drive signal can be provided in three ways:

- as a 3.3 V electrical signal (directly from most common microcontrollers)
- as a 5 V electrical signal
- via a fibre optic cable

If the PWM signal is provided electrically then it is passed through a digital isolator (Texas Instruments ISO721) to the 'hot' (isolated) side of the gate drive PCB. The gate driver used is the Texas Instrument UCC27531. This chip is capable of sourcing 2.5 A and sinking 5 A through asymmetrical drive (split outputs), and allows separate resistors for turn-on and turn-off. The circuit has been configured to apply a +20 V turn-on signal and a -2.5 V turn-off signal. Applying



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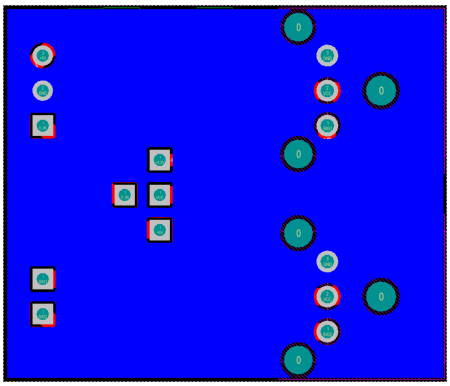

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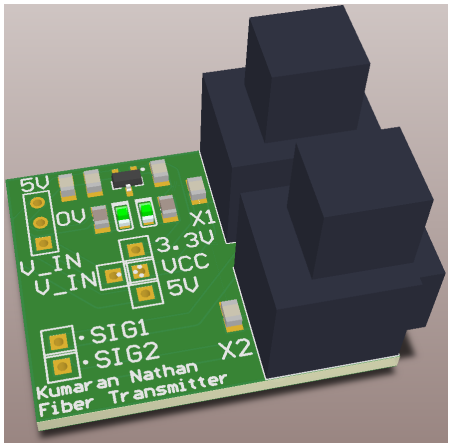
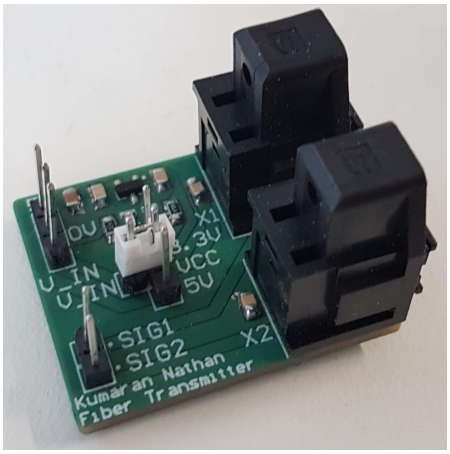


(c) 3D PCB model.

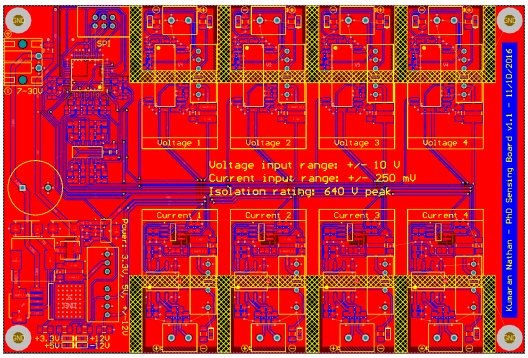


(d) Photo of developed PCB.

Figure 3.12: Optical transmitter board.

a negative voltage for turn-off provides immunity against parasitic turn-on. This parasitic turn-on can occur due to the rapid voltage changes causing a current to flow through the Miller capacitance and the gate resistances, potentially inducing a voltage on the gate in excess of the threshold voltage [123]. Even though SiC MOSFETs have small Miller capacitances compared with silicon IGBTs, they switch much faster and have lower threshold voltages.

In this application, a fibre optic cable has been used to send the PWM signal to the gate drive circuit, so a simple optical transmitter PCB has also been built, as shown in Figure 3.12. This board has two channels, which can be configured with jumpers to be driven from either a 3.3 V or 5 V signal source. In this application, the input has been configured as 3.3 V, driven directly from the microcontroller's PWM output.



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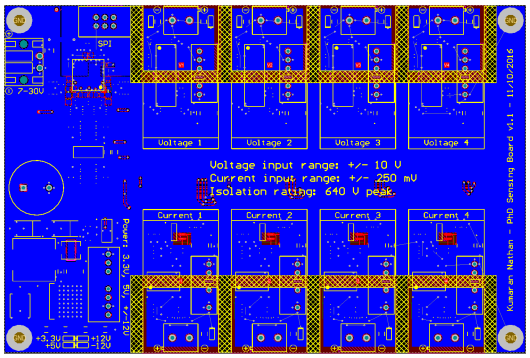

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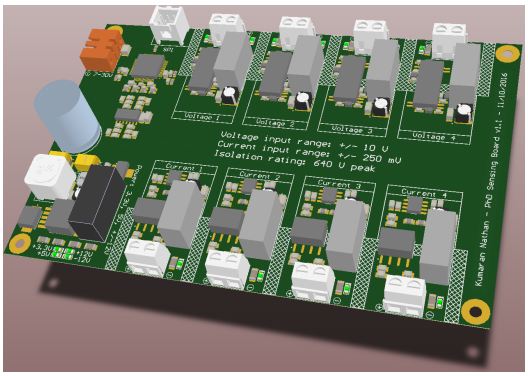
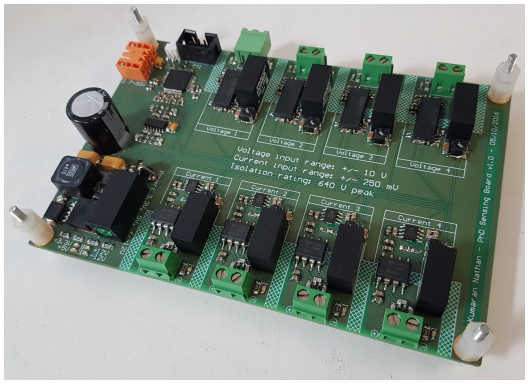


(c) 3D PCB model.



(d) Photo of developed PCB.

Figure 3.13: Isolated voltage and current sensing board.

3.4.6 Sensing

Isolated voltage and current sensing is needed for closed-loop control of the CCS converter. There are several isolated sensing options which are detailed here:

- *Voltage:* The simplest method to measure high voltages is with a large resistive voltage divider, where a large resistor drops the bulk of the voltage and the voltage across the small resistor is measured by an isolated sensor. An alternative is to use an isolated current sensor to measure the current flowing through the large shunt resistor.

- *Current:* The use of a Hall effect current transducer is inherently isolated. It is also possible to add a small series (shunt) resistor, which will have a voltage across it proportional to the current. This voltage can be measured and isolated as described previously.

These isolated waveforms must then be converted to digital form for use within the microcontroller, with analog-to-digital converters (ADCs). Some of the key specifications used to classify ADCs include their resolution, accuracy, and sampling speed. There are many types of ADCs, of which two are commonly used in power

electronics applications:

- *The successive approximation register (SAR) ADC* is one of the oldest and most widely used ADC types, which works by sampling a signal then using an iterative process to converge upon a digital value for each conversion point [124].
- *The Sigma-Delta ADC* is a newer type of ADC which became popular with the development of practical digital signal processing. It is slower than the SAR ADC, but offers a higher resolution and noise mitigation. Sigma-Delta ADCs make use of oversampling signal data and applying digital filters [125].

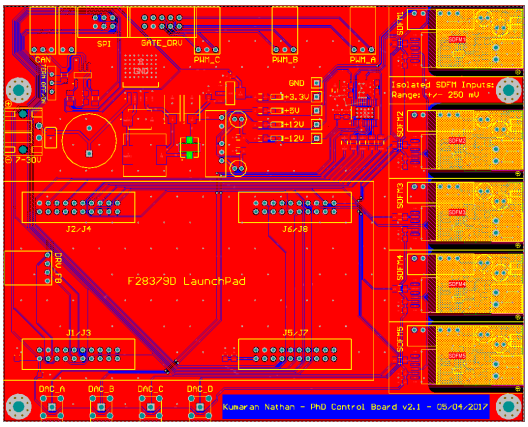
In this application, voltages are measured using the voltage divider technique, feeding isolated voltage sensors which are connected to the controller's SAR ADCs, and currents are measured using Hall effect current sensors, processed with op-amp circuits, and then connected to the controller's SAR ADCs. An isolated sensing board was developed as shown in Figure 3.13. This board can simultaneously sample four voltages and currents, and communicate the measured data to the controller via SPI.

3.4.7 Controller

A Texas Instruments C2000 Delfino microcontroller (MCU) is selected for controlling the converter due to its high resolution PWM modules, built-in ADCs (both SAR and Sigma-Delta), high clock speed, and processing power, allowing it to perform complex control algorithms in the short switching period. The specific model selected is the F28379D, which is a dual-core 200 MHz MCU, specifically designed for closed-loop control applications. One of the cores is allocated the control (high priority) tasks, and the other core is used for interfacing and other non-critical tasks.

The MCU is obtained on a low cost evaluation and development board, known as the LaunchPad (LAUNCHXL-F28379D), which has a subset of the MCU's pins available. This board is used because the limited pins available are more than sufficient for the requirements for the CCS converter, and using an evaluation board reduces development time associated with designing complex PCBs to accommodate MCUs.

The LaunchPad has 4 $\times$ 20-pin headers, so a 'control board' has been designed here to provide extended peripherals. This control board has been designed not



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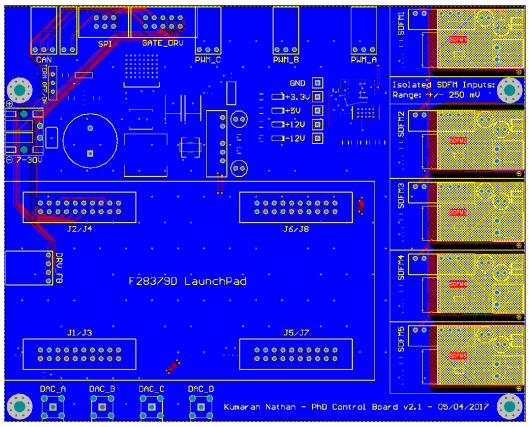

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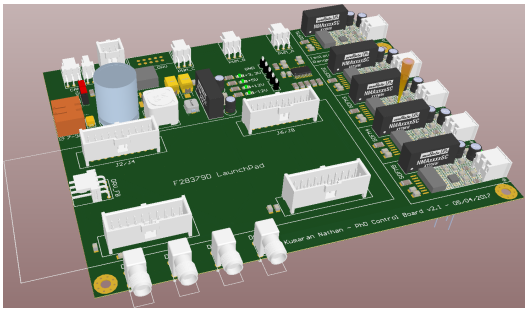
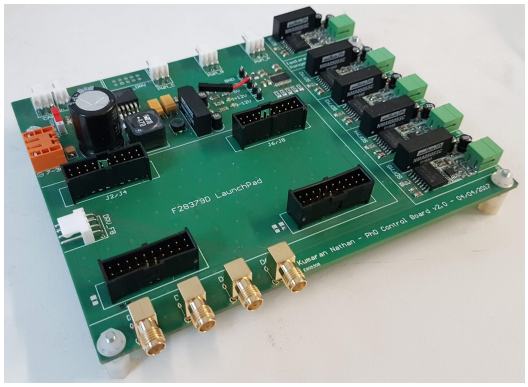


(c) 3D PCB model.



(d) Photo of developed PCB.

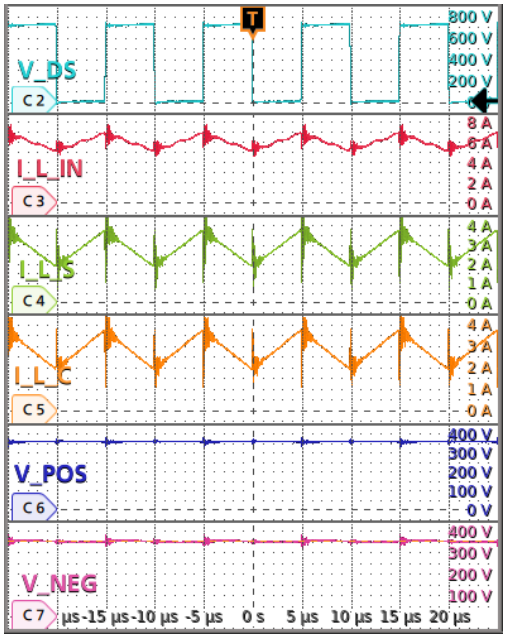
Figure 3.14: Control board for the LaunchPad MCU development board.

Figure 3.15: Load bank consisting of 10 × 120 Ω, 1 kW resistors.

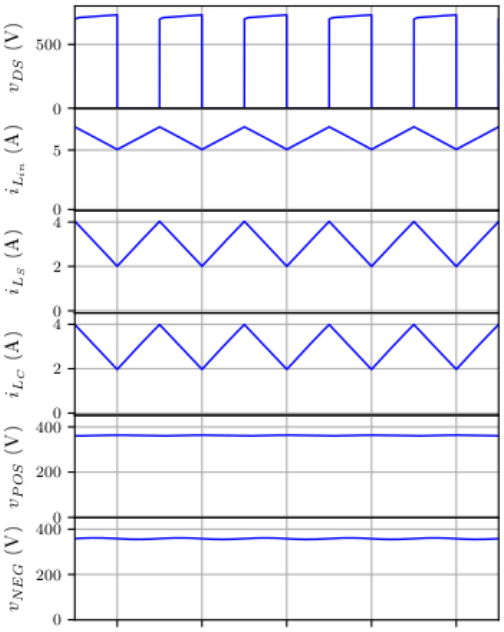
only for this application, but also to provide extended functionality so that it can be used easily in other applications. The board provides:

- a regulated power supply for the LaunchPad, generated from a supply with an input in the range of 7 V - 30 V
- a four channel, bipolar output, 16-bit digital-to-analog converter (DAC) which communicates with the MCU via SPI, and provides coaxial SMA connectors to easily view internal data on an oscilloscope
- five isolated Sigma-Delta ADCs
- six PWM connectors
- a SPI connector for communicating with the sensing board previously discussed
- a Controller Area Network (CAN) driver for communication with other controllers

Figure 3.14 shows this control board.



(a) Experimental results with 120 Ω resistance connected to each output.



(b) Simulation waveforms equivalent to the experimental measurements.

Figure 3.16: Experimental and equivalent simulation waveforms for $V_{in} = V_{POS} = V_{NEG} = 360\,V$: MOSFET voltage ($v_{DS}$), $i_{L_{in}}$, i_{L_S}, i_{L_C}, v_{POS}, v_{NEG}.

3.4.8 Load Bank

A bank of 10 × 120 Ω resistors (TE Connectivity TE1000B120RJ) has been built to serve as the DC load for the CCS converter, as shown in Figure 3.15. The resistors are wired to connectors to allow them to be easily configured into various topologies. This allows numerous effective resistance values to be created, allowing the converter to be tested over a range of output powers. These resistors have been mounted within a box for safety, and are cooled with a large automotive fan.

3.5 Experimental Results

A programmable DC supply, capable of providing 4 kW of power at a voltage range of 294 V to 440V is connected to the input of the CCS converter. The load used consists of 10 × 1 kW resistive loads with flexible configuration options. By varying the series and parallel connections, it is possible to test the CCS converter under several output power conditions. In this section, the converter has been tested at an output power of 2160 W (closest power available with the available resistance configurations to the 2 kW described in Section 3.2.2), though Chapter 5 investigates the converter's operation in other load conditions.

Tektronix THDP0200 high-voltage differential probes (200 MHz bandwidth) and TCP0030A current probes (DC to 120 MHz bandwidth) have been used for all measurements. The experimental results obtained with this prototype are shown in Figure 3.16a. Simulation results similar to those in Section 3.3.1 have been obtained, however the output power and passive component values have been modified to match the experimental configuration. The set of simulation results corresponding to the experimental waveforms has been presented in Figure 3.16b to provide a clear side-by-side comparison. This comparison demonstrates that the simulation and experimental waveforms are highly consistent, validating both the simulation studies and the analytical derivations presented. One notable difference between the experimental and simulation results is the presence of ringing at the switching transients. This ringing is due to parasitics present in the converter, particularly in the inter-turn capacitance of the hand-wound inductor windings, and so it is expected that with better inductor and winding design, this ringing would reduce substantially.

Depending on the application, there are two potential issues with the CCS converter as designed so far:

1. The input current ripple is relatively large with modest inductance values.
2. Having three discrete inductors requires three discrete magnetic structures, increasing the volume and weight, and thus negatively impacting the volumetric and gravimetric power density.

The first issue could be resolved by simply increasing the size of the input inductor, however to achieve small ripples (for example, less than 5%) a very sizeable inductor would be required, exacerbating the second issue. In the next chapter, this converter is modified in such a way that both of these issues are addressed.

Further experimental results and analysis of the CCS converter will be provided in Chapter 5 after the modified CCS converter has been introduced.

3.6 Chapter Conclusion

This chapter introduced the CCS converter and discussed its strengths - a grounded bipolar DC output, a high gain, its flexibility in providing both voltage step-up and step-down, its continuous input current, and its topology which requires only a single ground-referenced MOSFET. The CCM operation of the converter was

examined, with a description of the energy transfer process from the input to the output during each of the switch 'on' and 'off' states.

Following this theoretical analysis of the converter, the process of designing a converter was explained. Equations were derived for sizing each of the passive components based on the required performance specifications. Additional equations were also provided to determine the peak voltage and current ratings for all of the converter's components. With these values, the proposed converter was simulated using the Saber simulation platform to:

- provide insight into the various component waveforms (currents and voltages)
- verify that the performance criteria were satisfied
- validate the component sizing and rating equations.

The development process of a 4 kW experimental prototype was then studied, with an examination into the various design decisions. These decisions included the choice of semiconductor technology, inductor core material, capacitor technology, and voltage and current sensing methods. The various PCBs developed for this prototype were shown, with an explanation of the constraints involved in their design. Finally, data was obtained from this experimental prototype which validated both the theoretical and simulation results. Two issues have been identified (a large input current ripple, and three discrete magnetic structures). These issues will be addressed in the following chapter.

Chapter 4

Inductor Coupling in the CCS Converter

The previous chapter examined the CCS converter and explained its suitability for solar PV applications. This chapter introduces the ripple steering concept, achieved through inductor coupling, and demonstrates the benefits this has for the CCS converter, particularly in PV applications. It provides analytical derivations and simulation results, followed by a discussion of optimisation strategies and objectives. A comprehensive inductor design process is presented, supported by simulation and experimental results which demonstrate the large reductions in input current ripple.

4.1 Ripple Steering in Cuk and SEPIC Converters

Domestic solar PV applications are highly cost sensitive and demand high performance. Costs can be reduced by using converters with lower component count, as well as minimising their size and weight to help reduce logistics and installation costs. It has been established that performance (defined as total energy extracted) can be improved by reducing the solar array's current ripple, allowing it to maintain operation closer to its MPP. In this chapter, it will be shown that both of these metrics can be improved by modifying the CCS converter's magnetics using a technique called 'ripple steering'.

Standard Cuk and SEPIC converters have a major advantage over several other DC-DC converters with their continuous (non-pulsating) input and output currents. The current waveforms are average DC currents with superimposed tri-

angular switching frequency ripple components. Considering the topology of the magnetic connections (i.e. the magnetic circuit) in addition to the electrical circuit can bring enormous benefits. This coupled-inductor concept was first investigated in [126] and termed 'integrated magnetics'. The author stated that "in addition to the original capacitive energy transfer from the input to the output, the coupled inductors bring a simultaneous inductive energy transfer. Thus one may intuitively feel that this coupling will reduce the ripple of both the input and output currents, which is indeed the case" [126].

Magnetically coupling the inductors can lead to large reductions in the triangular ripple current components. This has numerous benefits:

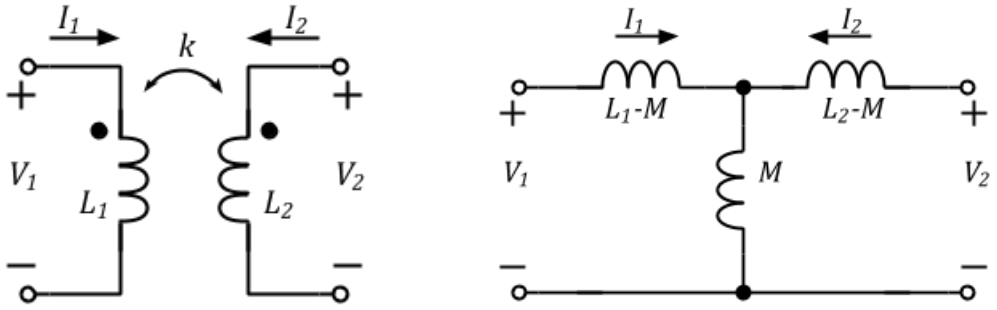
- *Reductions in size and weight:* Reduced inductance requirements meaning fewer turns are required, decreasing the size and weight of the inductors. Lower current ripple can allow for smaller, lower-rated capacitors to be used as there is less stress on the capacitors. In some applications, the reduced input current ripple may even mean the difference between an input decoupling capacitor being required or not. These reductions in size and weight translate directly into increases in volumetric and gravimetric power density.

- *Reduced cost:* Fewer turns requires less copper, reducing the cost of the inductors. The reduced capacitor requirements also means that cheaper capacitors can be used.

- *Reductions in losses:* Fewer turns means the winding resistance can be reduced, lowering the inductor copper losses. The smaller current ripple also reduces the rms current, also contributing to lower copper losses. Smaller current ripples means smaller variations in magnetic field strength, decreasing the size of the B-H curves, reducing the hysteresis losses in the inductor cores, and the smaller capacitor currents decreases the stress on the capacitors and lowers their ESR losses. The reduced losses not only increases the efficiency, but the reduced heat also contributes to prolonged component (and hence converter) lifespan.

These benefits are not limited to the Cuk and SEPIC converters, but are present in any converter employing integrated magnetics, including the CCS converter proposed in the previous chapter.

Ripple steering theory, as originally applied in the Cuk converter, considers a basic system of two coupled inductors as shown in Figure 4.1a (with coupling factor) and Figure 4.1b (with mutual inductance). This system accounts for leakage and



(a) Coupled inductors described using the coupling factor, k.

(b) Coupled inductors described with the mutual inductance, M.

Figure 4.1: Two-port network of two coupled inductors.

mutual inductance, but neglects other non-idealities like winding resistances and inter-turn capacitances. This forms a two-port network, which can be described by Equation 4.1 and Equation 4.2:

$$v_1(t) = L_1 \frac{di_1(t)}{dt} + M \frac{di_2(t)}{dt} \tag{4.1}$$

$$v_2(t) = M \frac{di_1(t)}{dt} + L_2 \frac{di_2(t)}{dt} \tag{4.2}$$

The mutual inductance, M, is defined by $M = k\sqrt{L_1 L_2}$, where the k is the coupling factor. This coupling factor is a measure of the degree of magnetic coupling between the inductors and is commonly defined over the range of $0 \leq k \leq 1$, spanning from no coupling (i.e. completely independent coils) to perfect coupling. In this thesis however, the coupling factor is defined for $-1 \leq k \leq 1$, where negative coupling factors represent polarity inversions of the coil connections and winding directions.

The above equations can be rearranged as follows:

$$di_1(t) = \frac{v_1(t)\,dt - M di_2(t)}{L_1} \tag{4.3}$$

$$di_2(t) = \frac{v_2(t)\,dt - M di_1(t)}{L_2} \tag{4.4}$$

Solving these two equations simultaneously gives the following:

$$di_1(t) = \frac{v_1(t)\,dt - M\left(\frac{v_2(t)dt - Mdi_1}{L_2}\right)}{L_1} \tag{4.5}$$

$$di_1(t)\left(\frac{L_1L_2 - M^2}{L_1L_2}\right) = \left(\frac{v_1(t)}{L_1} - \frac{Mv_2(t)}{L_1L_2}\right)dt \tag{4.6}$$

$$\frac{di_1(t)}{dt} = \left(\frac{L_1L_2}{L_1L_2 - M^2}\right)\left(\frac{v_1(t)}{L_1} - \frac{Mv_2(t)}{L_1L_2}\right) \tag{4.7}$$

$$\frac{di_1(t)}{dt} = \frac{L_2v_1(t) - Mv_2(t)}{L_1L_2 - M^2} \tag{4.8}$$

Writing the magnetising inductance in terms of the coupling factor:

$$\begin{aligned}\frac{di_1(t)}{dt} &= \frac{L_2v_1(t) - k\sqrt{L_1L_2}v_2(t)}{L_1L_2 - k^2L_1L_2}\\ \frac{di_1(t)}{dt} &= \frac{v_1(t) - k\sqrt{\frac{L_1}{L_2}}v_2(t)}{L_1(1-k^2)}\end{aligned} \tag{4.9}$$

If $v_1(t) = v_2(t)$ (which is true on average for both the switch 'on' and switch 'off' states), then:

$$\frac{di_1(t)}{dt} = \frac{v_1(t)\left(1 - k\sqrt{\frac{L_1}{L_2}}\right)}{L_1(1-k^2)} \tag{4.10}$$

$$v_1(t) = \frac{L_1(1-k^2)}{1 - k\sqrt{\frac{L_1}{L_2}}}\frac{di_1}{dt} \tag{4.11}$$

This means the equivalent L_1 inductance can be expressed as:

$$v(t) = L_{1_{equivalent}}\frac{di_1}{dt} \tag{4.12}$$

$$L_{1_{equivalent}} = \frac{L_1(1-k^2)}{1 - k\sqrt{\frac{L_1}{L_2}}} \tag{4.13}$$

In order for the ripple current component of i_1 to be eliminated, $L_{1_{equivalent}}$ must be infinite, so the denominator must be zero:

$$\begin{aligned}1 - k\sqrt{\frac{L_1}{L_2}} &= 0\\ k &= \sqrt{\frac{L_2}{L_1}}\end{aligned} \tag{4.14}$$

If it is instead desired to eliminate the ripple current component of i_2, the result becomes:

$$k = \sqrt{\frac{L_1}{L_2}} \tag{4.15}$$

In practice, it won't be possible to reduce the ripple in a winding to exactly zero and produce perfect ripple steering [127]. The remaining 'residual current ripple' is present for two main reasons:

- *Zero-ripple condition mismatch:* The number of turns in inductor windings is discrete, and the inductance also depends on the permeability of the magnetic circuit (which will vary due to manufacturing tolerances), so in practice Equation 4.14 won't be perfectly met.

- *Impressed voltage mismatch:* The process of deriving Equation 4.14 assumed that $v_1(t) = v_2(t)$, though in practice this won't hold due to internal factors (e.g. the voltage drop across the winding resistance, which was neglected), and external factors (e.g. the other components in the circuit).

It is possible to quantify the residual current ripple, including the contributions from both of these sources, by re-writing Equation 4.9 as:

$$\frac{di_1(t)}{dt} = \frac{v_1(t) - k\sqrt{\frac{L_1}{L_2}}\left[v_1(t) - (v_1(t) - v_2(t))\right]}{L_1(1-k^2)}$$

$$\frac{di_1(t)}{dt} = \frac{1}{L_1(1-k^2)}\left[\underbrace{\left(1 - k\sqrt{\frac{L_1}{L_2}}\right)v_1(t)}_{\text{zero-ripple condition mismatch}} + \underbrace{k\sqrt{\frac{L_1}{L_2}}\left(v_1(t) - v_2(t)\right)}_{\text{impressed voltage mismatch}}\right] \tag{4.16}$$

In perfect conditions the inductance itself is theoretically irrelevant and could almost be zero and still achieve full current ripple cancellation. In practice, Equation 4.16 shows that the inductance is important in determining the residual current ripple resulting from these unavoidable mismatches.

With theory underpinning the ripple steering technique detailed for a system of two coupled inductors, it is possible to expand it for application to the CCS converter.

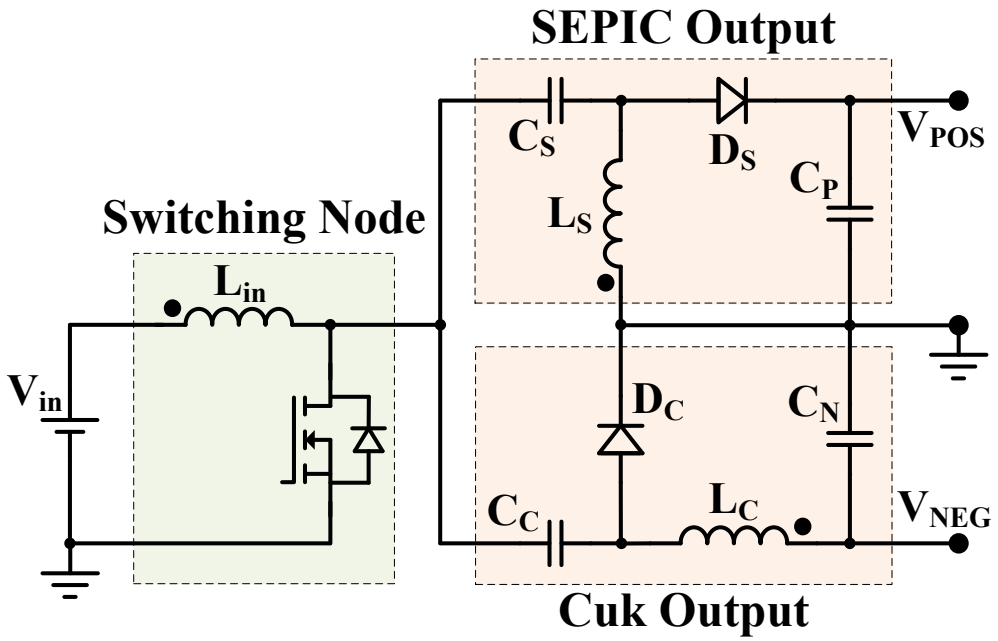


Figure 4.2: Topology of the CI-CCS converter.

4.2 The CI-CCS Converter

By following a similar procedure, but extending it to a system of three coupled inductors, we can begin to apply the principle of ripple steering to the CCS converter. This modified CCS converter with integrated magnetics is known as the Coupled Inductors Combined Cuk-SEPIC (CI-CCS) converter, and is shown in Figure 4.2. The topology diagram is identical to that of the regular CCS converter, with the exception of dots added to the inductors to indicate the polarity of the added magnetic coupling.

4.2.1 Determining Equivalent Input Inductance

With the goal of determining the equivalent input inductance, we start with the generalised inductance matrix for a system of three inductors (Equation 4.17), and apply it to the CI-CCS converter to produce Equation 4.18:

$$L = \begin{bmatrix} L_{11} & L_{12} & L_{13} \\ L_{21} & L_{22} & L_{23} \\ L_{31} & L_{32} & L_{33} \end{bmatrix} \tag{4.17}$$

$$L_{CI-CCS} = \begin{bmatrix} L_{in} & M_S & M_C \\ M_S & L_S & M_{SC} \\ M_C & M_{SC} & L_C \end{bmatrix} \tag{4.18}$$

where:

M_S is the mutual coupling between the input inductor and the SEPIC inductor

M_C is the mutual coupling between the input inductor and the Cuk inductor

M_{SC} is the mutual coupling between the SEPIC inductor and the Cuk inductor

It should be noted that this matrix is symmetric since the mutual inductances between two inductors are equal regardless of which is taken first (i.e. $L_{xy} = L_{yx}$).

Next, the generalised inductor equations (Equations 4.19 - 4.21) are applied to the CI-CCS converter to produce Equation 4.22 (expressed in matrix form):

$$v_1(t) = L_{11}\frac{di_1(t)}{dt} + L_{12}\frac{di_2(t)}{dt} + L_{13}\frac{di_3(t)}{dt} \tag{4.19}$$

$$v_2(t) = L_{21}\frac{di_1(t)}{dt} + L_{22}\frac{di_2(t)}{dt} + L_{23}\frac{di_3(t)}{dt} \tag{4.20}$$

$$v_3(t) = L_{31}\frac{di_1(t)}{dt} + L_{32}\frac{di_2(t)}{dt} + L_{33}\frac{di_3(t)}{dt} \tag{4.21}$$

$$\begin{bmatrix} v_{L_{in}}(t) \\ v_{L_S}(t) \\ v_{L_C}(t) \end{bmatrix} = \begin{bmatrix} L_{in} & M_S & M_C \\ M_S & L_S & M_{SC} \\ M_C & M_{SC} & L_C \end{bmatrix} \begin{bmatrix} \frac{di_{L_{in}}(t)}{dt} \\ \frac{di_{L_S}(t)}{dt} \\ \frac{di_{L_C}(t)}{dt} \end{bmatrix} \tag{4.22}$$

The objective here is to determine an equivalent input inductance, so we need to eliminate i_{L_S} and i_{L_C}. By rearranging Equation 4.22 and performing appropriate substitutions, Equation 4.23 can be obtained:

$$\begin{aligned} v_{L_{in}}(t) = {} & \frac{L_{in}M_{SC}^2 - L_{in}L_SL_C + L_SM_C^2 + L_CM_S^2 - 2M_SM_CM_{SC}}{M_{SC}^2 - L_SL_C}\frac{di_{L_{in}}(t)}{dt} \\ & + \frac{M_CM_{SC} - L_CM_S}{M_{SC}^2 - L_SL_C}v_{L_S}(t) + \frac{M_SM_{SC} - L_SM_C}{M_{SC}^2 - L_SL_C}v_{L_C}(t) \end{aligned} \tag{4.23}$$

Finally, we can apply the approximation $v_{L_{in}}(t) = v_{L_S}(t) = v_{L_C}(t)$, as in the 'on' state these voltages all average to V_{in}, and in the 'off' state these voltages all average to $-V_{out}$. After rearranging this results in Equation 4.24:

$$v_{L_{in}}(t) = \frac{L_{in}L_SL_C + 2M_SM_CM_{SC} - L_SM_C^2 - L_CM_S^2 - L_{in}M_{SC}^2}{L_SL_C + M_SM_{SC} + M_CM_{SC} - L_CM_S - L_SM_C - M_{SC}^2}\frac{di_{L_{in}}(t)}{dt} \tag{4.24}$$

$$v_{L_{in}}(t) = L_{in_{equivalent}}\frac{di_{L_{in}}(t)}{dt}$$

This produces the expression for the equivalent input inductance given in Equa-

tion 4.25:

$$L_{in_{equivalent}} = \frac{L_{in}L_SL_C + 2M_SM_CM_{SC} - L_SM_C^2 - L_CM_S^2 - L_{in}M_{SC}^2}{L_SL_C + M_SM_{SC} + M_CM_{SC} - L_CM_S - L_SM_C - M_{SC}^2} \tag{4.25}$$

The same process carried out for the SEPIC and Cuk inductors gives the equivalent inductance expressions in Equation 4.26 and Equation 4.27:

$$L_{S_{equivalent}} = \frac{L_{in}L_SL_C + 2M_SM_CM_{SC} - L_SM_C^2 - L_CM_S^2 - L_{in}M_{SC}^2}{L_{in}L_C - L_{in}M_{SC} - L_CM_S + M_C\left(M_S - M_C + M_{SC}\right)} \tag{4.26}$$

$$L_{C_{equivalent}} = \frac{L_{in}L_SL_C + 2M_SM_CM_{SC} - L_SM_C^2 - L_CM_S^2 - L_{in}M_{SC}^2}{L_{in}L_S - L_{in}M_{SC} - L_SM_C + M_{SC}\left(M_C - M_S + M_{SC}\right)} \tag{4.27}$$

If we were to replace all three mutual inductance terms (M_S, M_C, M_{SC}) with zero in Equations 4.25 - 4.27, we would simply be left with:

$$L_{in_{equivalent}} = L_{in} \tag{4.28}$$

$$L_{S_{equivalent}} = L_S \tag{4.29}$$

$$L_{C_{equivalent}} = L_C \tag{4.30}$$

This leaves us with the same inductances as the previous CCS (uncoupled) converter, as expected.

In this application, we are primarily focused on minimising the input current ripple so the remainder of this section centres on the maximising the equivalent input inductance, $L_{in_{equivalent}}$. A discussion of the merits of increasing the equivalent output inductance is provided in Section 4.5.

Generally, it is more practical to think in terms of coupling factors rather than mutual inductances, so we apply Equations 4.31 - 4.33:

$$M_S = k_1\sqrt{L_{in}L_S} \tag{4.31}$$

$$M_C = k_2\sqrt{L_{in}L_C} \tag{4.32}$$

$$M_{SC} = k_3\sqrt{L_SL_C} \tag{4.33}$$

With these substitutions, Equation 4.25 becomes Equation 4.34:

$$L_{in_{equivalent}} = \frac{L_{in}\left(1 + 2k_1k_2k_3 - k_1^2 - k_2^2 - k_3^2\right)}{1 - k_3^2 + \sqrt{\frac{L_{in}}{L_S}}\left(k_2k_3 - k_1\right) + \sqrt{\frac{L_{in}}{L_C}}\left(k_1k_3 - k_2\right)} \tag{4.34}$$

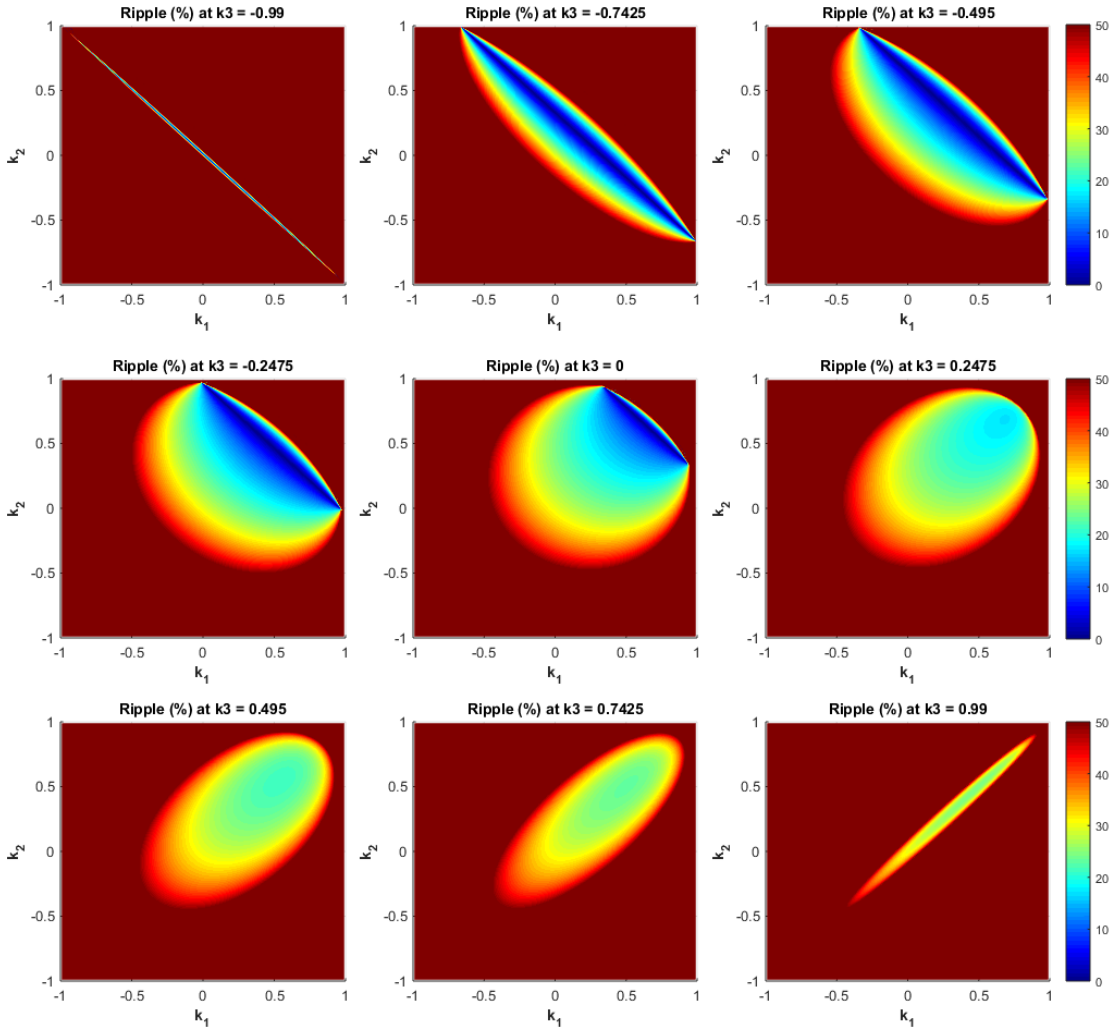


Figure 4.3: Input current ripple as a function of k_1 and k_2, at various values of k_3.

4.2.2 Effects on Input Current Ripple

With this new equivalent input inductance expression, it is desirable to estimate the impact this has on the input current ripple. From $v = L\frac{di}{dt}$, we know that the current ripple varies inversely to the inductance (for the same applied voltage). Thus, for a given equivalent input inductance, we can estimate what the input current ripple would be with Equation 4.35, which scales the uncoupled input current ripple inversely to the equivalent inductance:

$$i_{ripple_{new}} = \frac{L_{in}}{L_{in_{equivalent}}} i_{ripple_{uncoupled}} \tag{4.35}$$

Figure 4.3 shows this theoretical input current ripple as a function of k_1 and k_2, at various values of k_3, using the same inductance values determined in the previous chapter ($L_{in} = 545\,\mu H$, $L_S = L_C = 891\,\mu H$). These graphs are based on the nominal input voltage condition ($V_{in} = 360\,V$), so the input current ripple has

been normalised to 30% (the theoretically expected input current ripple for the uncoupled CCS converter, determined using Equation 3.6). In this figure, the input current ripple has been capped at 80% for the sake of providing sufficient resolution in the 'interesting' sections of the graphs. There are several important observations from these results:

- There are substantial areas which are dark blue, representing reduced input current ripple. There is an even bigger space that is covered by yellow, orange, and red areas, which represent higher input current ripple, and thus the coupling factors should be selected carefully.
- All nine graphs show perfect symmetry along the $k_1 = k_2$ line. The reasons for this, and its implications, will be discussed in the next section.
- In some of the graphs, there is a dark blue line, representing zero input current ripple. The origins of this line will be discussed in Section 4.2.3.
- Negative values of k_3 appear to have larger areas of low input current ripple, but positive values seem to lose this benefit.
- Around the regions of low input current ripple, the ripple appears to be particularly sensitive to changes in coupling factors. This means that care needs to be taken in inductor design to ensure that the benefits are being fully utilised.

4.2.3 Simplifying the Equivalent Input Inductance

The nine input current ripple graphs in Figure 4.3 all display perfect symmetry along the $k_1 = k_2$ line. There are two reasons for this:

- Equal inductances have been used for L_S and L_C, due to the design process outlined in the previous chapter
- The form of Equation 4.34 shows that k_1 and k_2 appear in "equivalent" places, as do L_S and L_C.

This result has important implications. Due to this symmetry, we can apply two constraints to greatly simplify the equivalent input inductance expression:

- Let $L_S = L_C \ (= L_{out})$, since the L_S and L_C sizing expressions (Equation 3.7 and Equation 3.8) yield identical values when the same output current ripple targets are used

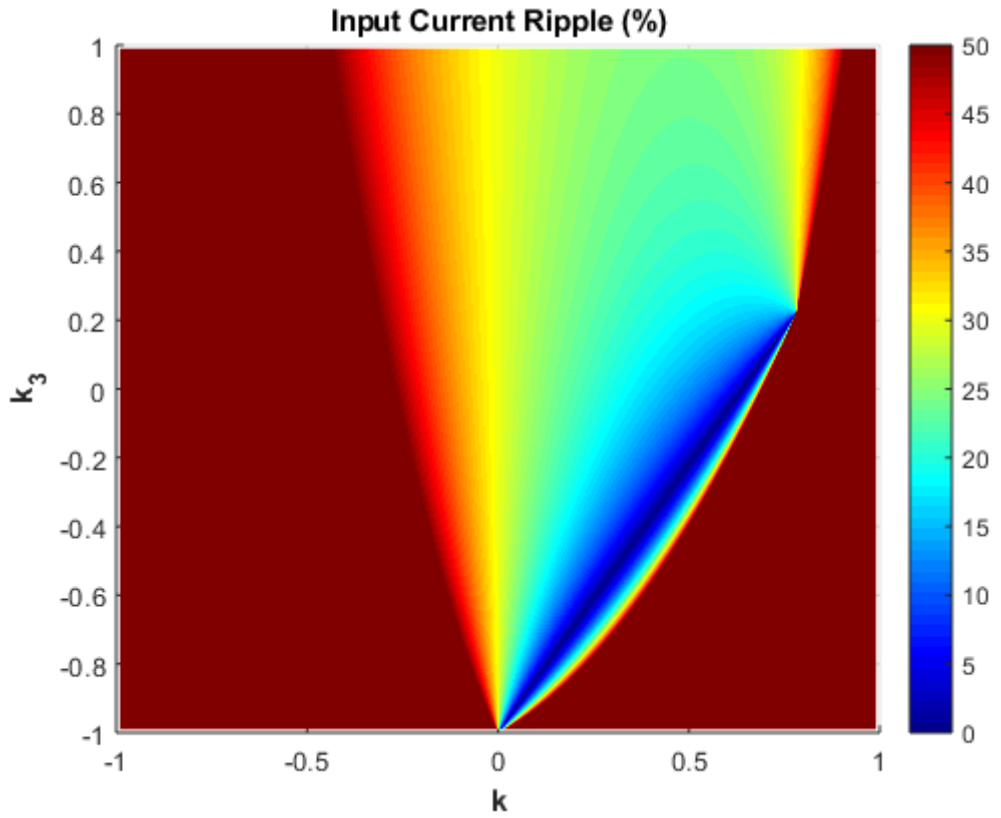


Figure 4.4: Colour map of input current ripple as a function of k and k_3.

- Let $k_1 = k_2$ $(= k)$, since the symmetric results show no advantages to have distinct values for these coupling factors.

With these constraints, the equivalent input inductance expression (Equation 4.34) can be simplified to Equation 4.36:

$$L_{in_{equivalent}} = \frac{L_{in}\left(1 + 2k^2k_3 - k^2 - k^2 - k_3^2\right)}{1 - k_3^2 + \sqrt{\frac{L_{in}}{L_{out}}}\left(kk_3 - k\right) + \sqrt{\frac{L_{in}}{L_{out}}}\left(kk_3 - k\right)}$$

$$L_{in_{equivalent}} = \frac{L_{in}\left(1 + k_3 - 2k^2\right)}{1 + k_3 - 2k\sqrt{\frac{L_{in}}{L_{out}}}} \tag{4.36}$$

In Figure 4.3, only nine values of k_3 were tested, however with the reduced number of variables it is now possible to generate a single graph covering *all* possible values of k_3. This is shown as a colour map in Figure 4.4 (and Figure 4.5 shows this same data as a 3D surface plot), where the estimated input current ripple is plotted as a function of k and k_3, covering all coupling factors between -1 and 1 with the constraints $k_1 = k_2$ and $L_S = L_C$.

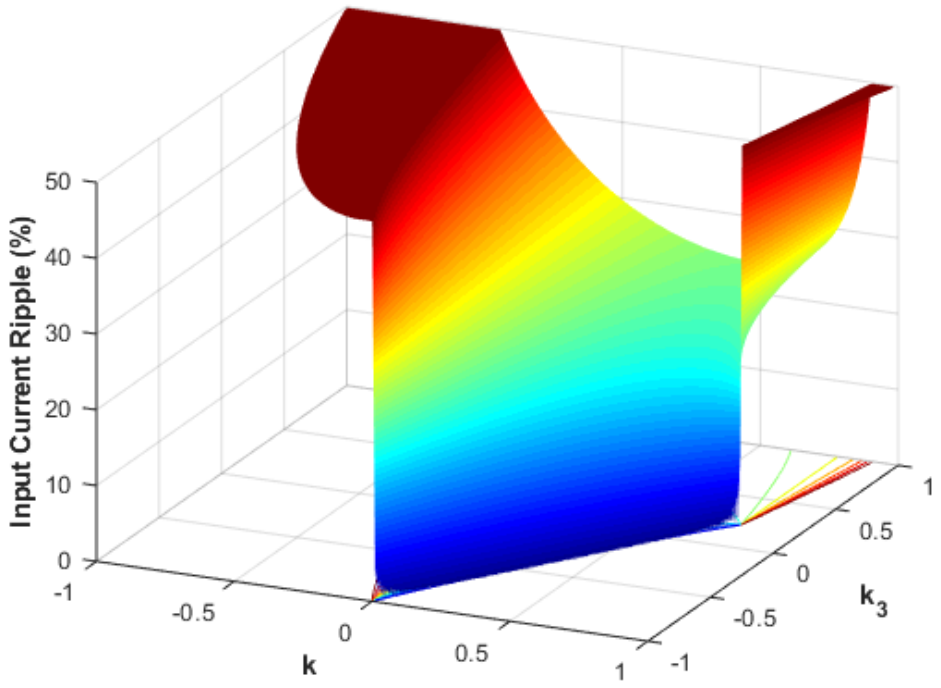


Figure 4.5: Surface plot of input current ripple as a function of k and k_3.

It can be seen that there is a line with zero current ripple originating at ($k = 0$, $k_3 = -1$) and slanted up to the right. The derivation of this line can be obtained by understanding that the input current ripple is eliminated when the equivalent input inductance is infinite. This occurs when the denominator of Equation 4.36 is zero, giving Equation 4.38, which describes the line observed in the graph:

$$1 + k_3 - 2k\sqrt{\frac{L_{in}}{L_{out}}} = 0 \tag{4.37}$$

$$k_3 = 2k\sqrt{\frac{L_{in}}{L_{out}}} - 1 \tag{4.38}$$

It should be noted that the values of L_{in} and L_{out} are fixed here at 545 μH and 891 μH, though it can be seen that the gradient of Equation 4.38 could be varied by altering these inductances.

From the graph, it can also be seen that negative values of k should be discarded as they produce higher input current ripple than the uncoupled scenario. Similarly, k_3 values above approximately 0.2 don't give the lowest input current ripple. Thus, the lowest current ripple area appears to be bounded by $0 \leq k \leq 0.8$ and $-1 \leq k_3 \leq 0.2$. Figure 4.6 shows a colour map zoomed into this area of interest, where a zero input current ripple is theoretically possible.

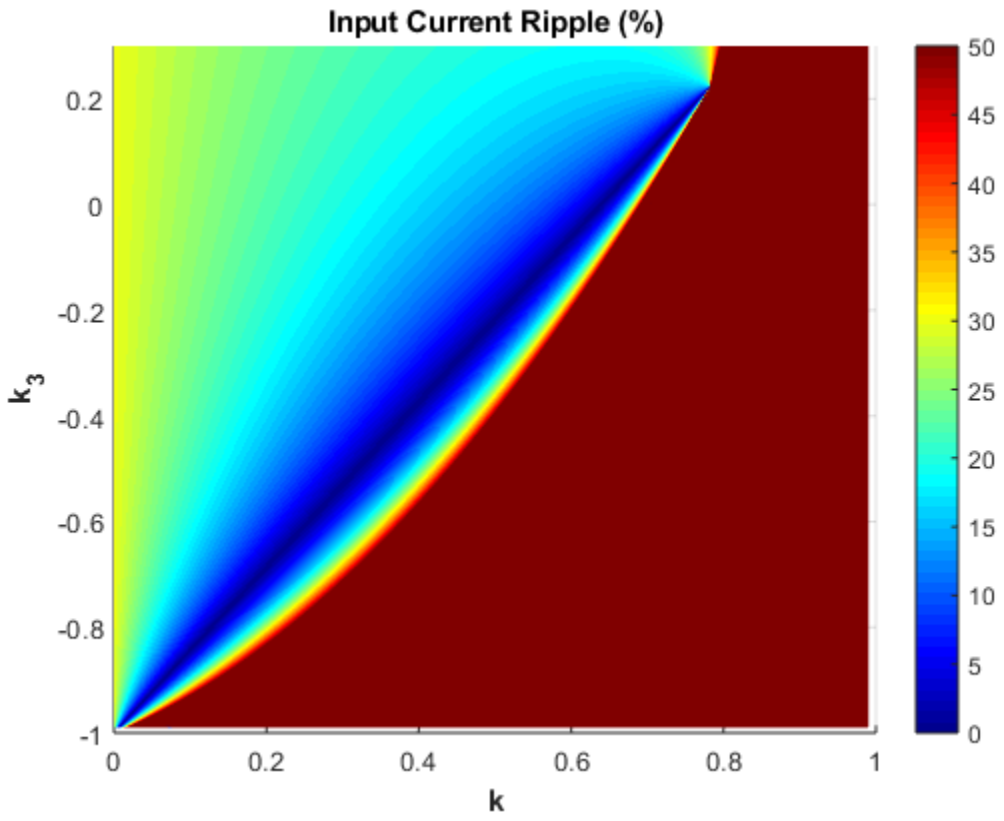


Figure 4.6: Colour map of input current ripple as a function of k and k_3, showing the lowest ripple section.

One limitation of this approach is created when progressing from Equation 4.23 to Equation 4.24, where the time-varying voltage terms were replaced with their average values, effectively creating a first-order approximation. Thus, there will still be a ripple component present in the input current due to the higher order terms.

In order to quantify the impact of this approximation, it is necessary to perform simulation studies of the CI-CCS converter at varied coupling factors.

4.3 Simulation Studies

In order to verify the effects of coupling the CCS converter's inductors and assess the accuracy of the analytical results obtained in Section 4.2.2, it is necessary to undertake simulations of the CI-CCS converter. Here, the MathWorks Simulink environment has been used, and the component values are the same as in the previous section.

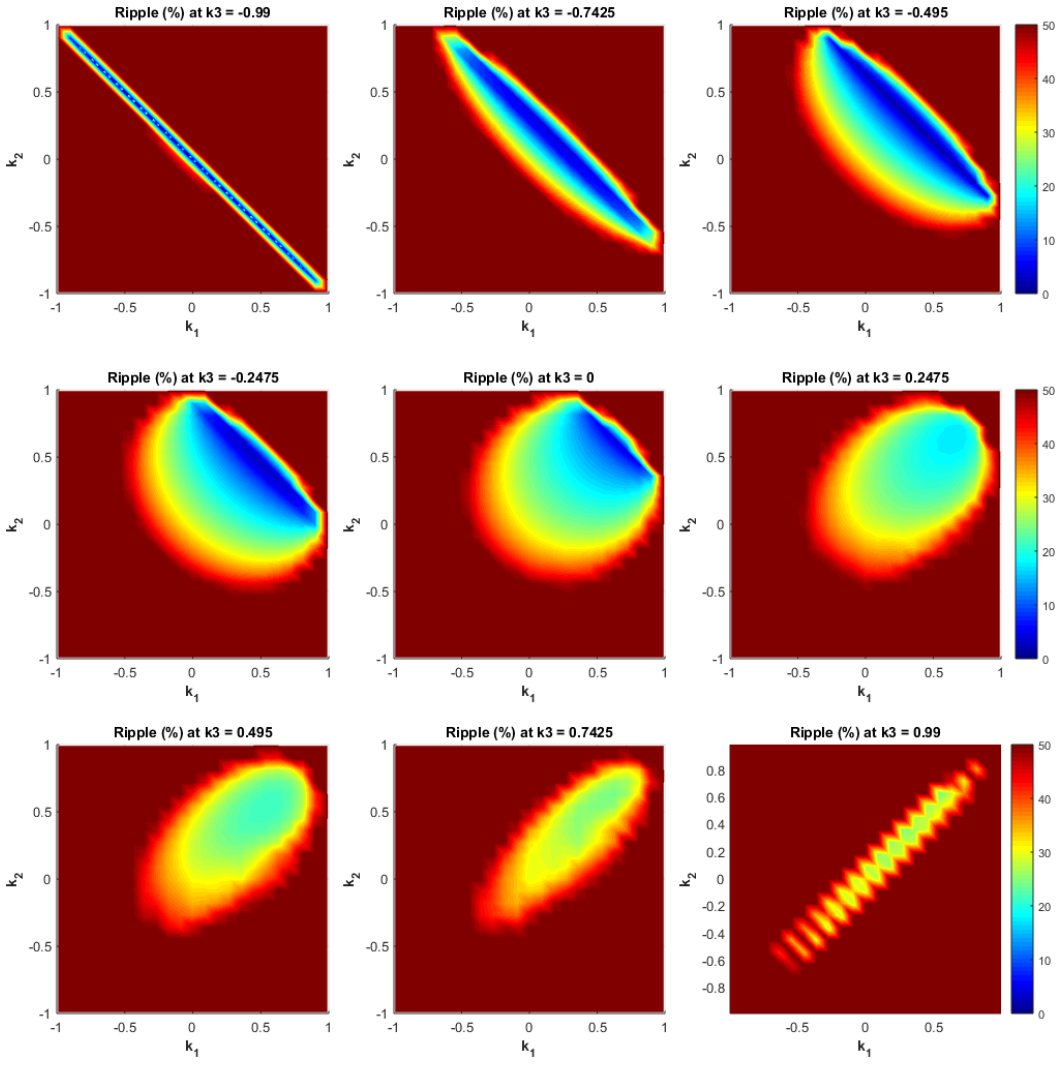


Figure 4.7: Input current ripple as a function of k_1 and k_2, at various values of k_3.

The first set of simulations have been performed relaxing the previous constraint of $k_1 = k_2$ in order to provide a comparison with the analytical results presented in Figure 4.3. These simulations have been performed by sweeping the coupling factors across the same range (-0.99 to 0.99), and at the same values of k_3, and the results are shown in Figure 4.7.

Obtaining such graphs is extremely computationally intensive; in the analytical case (Figure 4.3) the coupling factors were incremented in steps of 0.01, giving hundreds of thousands of data points which, if simulated, would take almost three weeks [1]. Even if the simulations were parallelised across processor cores, the time

[1] Nine graphs, each with k_1 and k_2 varying from -0.99 to 0.99 at 0.01 increments gives $9 \times 199 \times 199 = 356,409$ data points. At 5 seconds per simulation, this would take $(356409 \times 5) \div (60 \times 60 \times 24) = 20.6$ days.

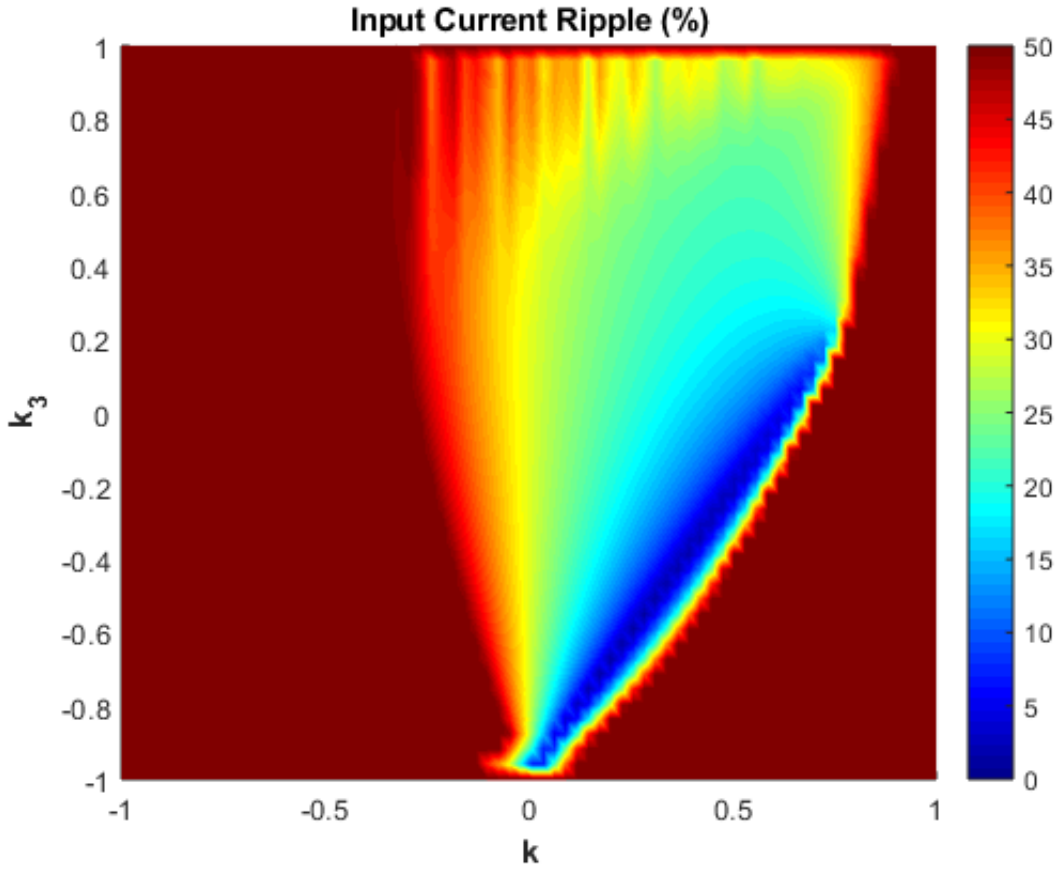


Figure 4.8: Colour map of input current ripple as a function of k and k_3.

taken to obtain a single set of results would still prohibitively long. Thus, the coupling factor increment used for obtaining these results is 0.09, producing in the slightly 'blockier' graphs. This computational time challenge will be addressed in Section 4.4.

Aside from this coarse granularity, these results obtained from simulations match very closely with the corresponding analytical results previously presented in Figure 4.3. The ripple values obtained in simulations are slightly higher than those obtained theoretically, due to the higher order effects which were neglected in the first-order approximations.

As with the theoretical results, there is clear symmetry along $k_1 = k_2$, so we can again apply a simplifying constraint that $k_1 = k_2 \,(= k)$. With this simplification, we can obtain another graph covering all possible values of coupling factors, k and k_3.

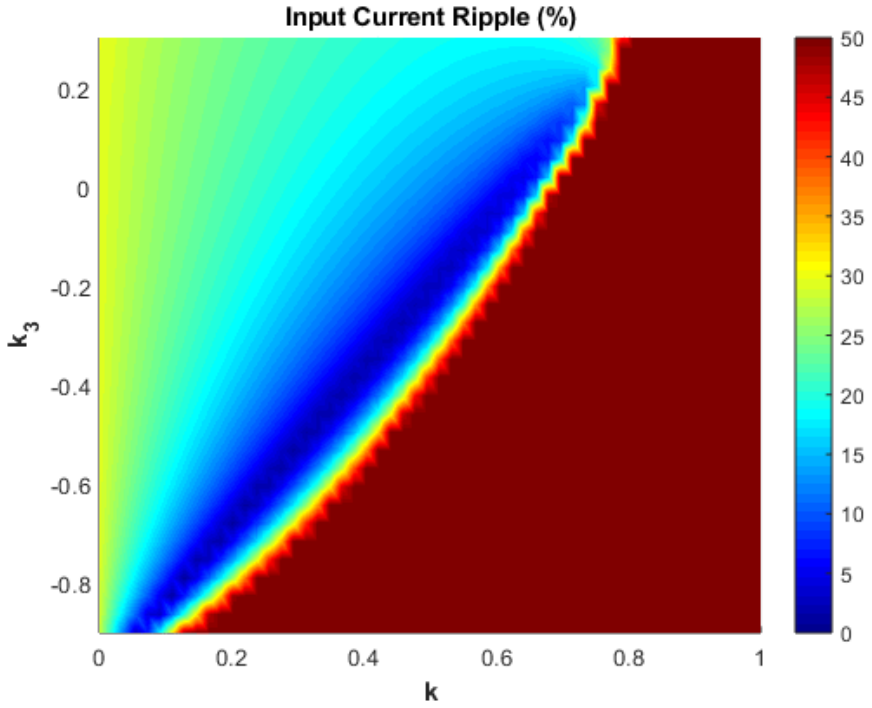


Figure 4.9: Colour map of input current ripple as a function of k and k_3, showing the lowest ripple section.

This graph is shown in Figure 4.8, and shows close resemblance with the theoretical version presented in Figure 4.4. Simulations are performed at a higher resolution in the area of interest and the results are shown in Figure 4.9, which again shows close resemblance to the theoretical version in Figure 4.6. Once again, these graphs are 'blockier' than the theoretical equivalents due to the computational intensity of running these simulations.

In order to accurately determine the minimum input current ripple over this entire space, it would be necessary to increase the resolution of these simulations, but in doing so the computational intensity goes up in polynomial time. It would of course also be possible to start with a large step size to isolate the regions where the lowest input current ripples are located, then iteratively use a finer step size on small regions, until sufficient accuracy has been reached. This method is still time-consuming, requires significant manual intervention, and still won't necessarily guarantee the most optimal result (unless by chance it corresponds to a sample point).

Alternatively, the consistent analytical and simulation results mean that the analytical expressions can be used to greatly reduce the "space" of k and k_3 needing to be simulated (rather than simulating the entire space).

Clearly a better solution is required.

4.4 Optimisation Techniques for Determining Optimal Inductor Coupling

4.4.1 Overview of Optimisation Techniques

In order to find the combination of coupling factors that yields the lowest input current ripple, a method is required that is less-computationally intensive than simply testing a region at a fixed step size. This section introduces a number of popular optimisation techniques and discusses their suitability for this application. These optimisation techniques are often used in machine learning applications (for example, training neural networks), where the variables being tuned are known as 'hyperparameters'. The most popular optimisation techniques are:

- *Grid search:* This is the method used in the previous section, where hyperparameters are swept over a defined space. Grid search optimisation suffers from the 'curse of dimensionality', meaning the number of test points increases drastically with the number of parameters being optimised.

- *Random search:* This method chooses hyperparameter combinations randomly, rather than exhaustively testing all hyperparameter combinations as with the grid search method. This method can outperform the grid search method, especially when the problem has a low dimensionality (i.e. a small number of hyperparameters).

- *Gradient-based optimisation:* This method calculates the gradient with respect to the hyperparameters to guide the optimisation. This can be done with first order algorithms (e.g. gradient descent), or second or higher order algorithms (e.g. Hessian) - though these are not commonly used as they are slower than first order algorithms and the performance improvement is marginal.

- *Evolutionary optimisation:* These methods work by first generating a random initial population of sample points, then evaluating the 'fitness' of these points (i.e. determining the ripple at each point), and finally generating a new population by perturbation of the existing population. This process is repeated until some stopping criteria is met. The differences between evolutionary algorithms lies primarily in the method of producing new populations based on solutions from the previous populations. The most popular types of evolutionary optimisations are the 'particle swarm' and 'genetic algorithm' methods. These methods are useful when the function has discontinuities,

when there many dimensions, and when there are several optimisation objectives.

- *Bayesian optimisation:* This method works by defining a probabilistic 'surrogate function' which approximates the real function, and is easy to evaluate. It then iteratively evaluates promising parameter combinations, based on an 'acquisition function', which estimates the profit for sampling at a point [128]. Bayesian optimisation works best for a low number of dimensions (typically 10 or fewer), and for 'well behaved' functions, making it the most applicable optimisation technique for this application. Thus, it will be explained in more depth in the following section.

4.4.2 Bayesian Optimisation Applied to the CI-CCS Converter

The overview of optimisation techniques presented in the previous section gave a brief introduction to Bayesian optimisation, and this section further explains the technique and how it can be applied to minimise the CI-CCS converter's input current ripple. Bayesian optimisation is an iterative method which repeats the following steps:

1. Pick a random set of hyperparameters and evaluate the function (i.e. perform a simulation with random values of k and k_3 in the range of -0.99 to 0.99, and determine the ripple).

2. Create a 'surrogate function' which approximates the true function, but is easy to evaluate. It is popular to use surrogate models which are non-parametric Gaussian processes (GPs), in order to model complex data and estimate uncertainty [129, 130].

3. Create an 'acquisition function', which estimates the profit for sampling at all possible hyperparameter combinations. It estimates this profit by using the most up-to-date surrogate function. This acquisition function aims to balance exploitation (searching in regions with the best estimated value) against exploration (searching in regions of high uncertainty). There are a variety of acquisition functions (e.g. max probability of improvement, upper confidence bound, expected improvement, etc.) which balance this trade-off differently [131].

4. The maximum of the chosen acquisition function is found, and the real func-

tion is then evaluated at the hyperparameter combination corresponding to this maximum. The resulting ripple is used to re-train the surrogate function and the process is repeated with the updated function.

5. This process is repeated until some stopping criteria are met. These stopping criteria are defined by the designer and could include a set number of evaluations, a fixed time, or a threshold in the rate of improvement [132].

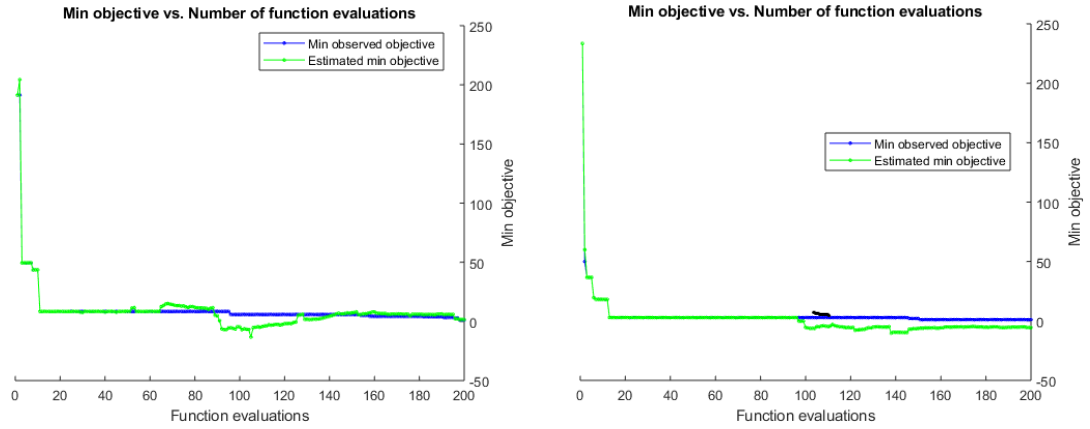
This process makes Bayesian optimisation well suited for applications where:

- The function describing the surfaces are 'well behaved' (loosely meaning that it satisfies some regularity conditions and the function's value at some point can be estimated by looking to neighbouring values). They can be multimodal because Gaussian processes will ensure that the optimisation doesn't get 'stuck' in local minima.
- The function is explicitly unknown
- Evaluations of the function are expensive
- There are a low number of dimensions (typically 10 or fewer).

As can be seen, the Bayesian optimisation technique is well-suited to the coupled inductor design process. The next section details the input current ripple minimisation of the CI-CCS converter, given the inductances from the uncoupled CCS converter.

4.4.3 Minimum Input Current Ripple

A Bayesian optimisation is performed to determine the optimal inductor coupling to minimise the worst case input current ripple (i.e. at $V_{in} = 440\,V$). The inductances are again set to their values from the uncoupled CCS converter design, and the hyperparameters being varied are k_1, k_2, and k_3 - this is referred to as the 'unconstrained' optimisation. This optimisation is run for 200 iterations, and the optimisation results obtained are shown in Figure 4.10a. The coupling factors produced by this unconstrained optimisation are shown in Table 4.1, and the input current ripple is calculated to be just 1.24%. It can be noted that despite the graphs in Figure 4.7 appearing symmetrical (suggesting that there is no advantage to distinct values of k_1 and k_2), the coupling factors produced have $k_1 \neq k_2$. This is because along the 'valleys' of low current ripple, there may be slight variations in the input current ripple.



(a) Unconstrained optimisation (k_1, k_2, k_3 varied).

(b) Constrained optimisation (k, k_3 varied).

Figure 4.10: Optimisation results: minimum input current ripple vs. number of evaluations.

Table 4.1: Coupling factors for the various optimisations.

Optimisation	k_1	k_2	k_3
None	0	0	0
Unconstrained	0.024963	0.23709	-0.79016
Constrained	0.23764		-0.62429

A 'constrained' optimisation is then conducted with $k_1 = k_2 (= k)$. This optimisation is also run for 200 iterations, and the optimisation results obtained are shown in Figure 4.10b. The coupling factors produced by this constrained optimisation are shown in Table 4.1, and the input current ripple is calculated to be 1.38%. Both optimisations in Figure 4.10 show that despite being run for 200 iterations, coupling factor combinations producing input current ripples close to the final results are obtained in less than 20 iterations, demonstrating the power of using the Bayesian optimisation technique in this application.

Table 4.2: Ripple components at the various optimisations.

Optimisation	$\Delta i_{L_{in}}$ (%)	Δi_{L_S} (%)	Δi_{L_C} (%)	Δv_{POS} (%)	Δv_{NEG} (%)
None	40.0	39.9	40.2	1.82	2.00
Unconstrained	1.24	191.8	194.2	1.78	9.67
Constrained	1.38	106.3	107.9	1.81	5.36

Voltage and current waveforms of the converter with these optimised coupling factors are provided in Figure 4.11, and the calculated ripple components are listed in Table 4.2. These results clearly demonstrate the reduction in the input current ripple when these optimisations are performed, compared with the uncoupled inductors scenario. The input current ripple of the CI-CCS converter

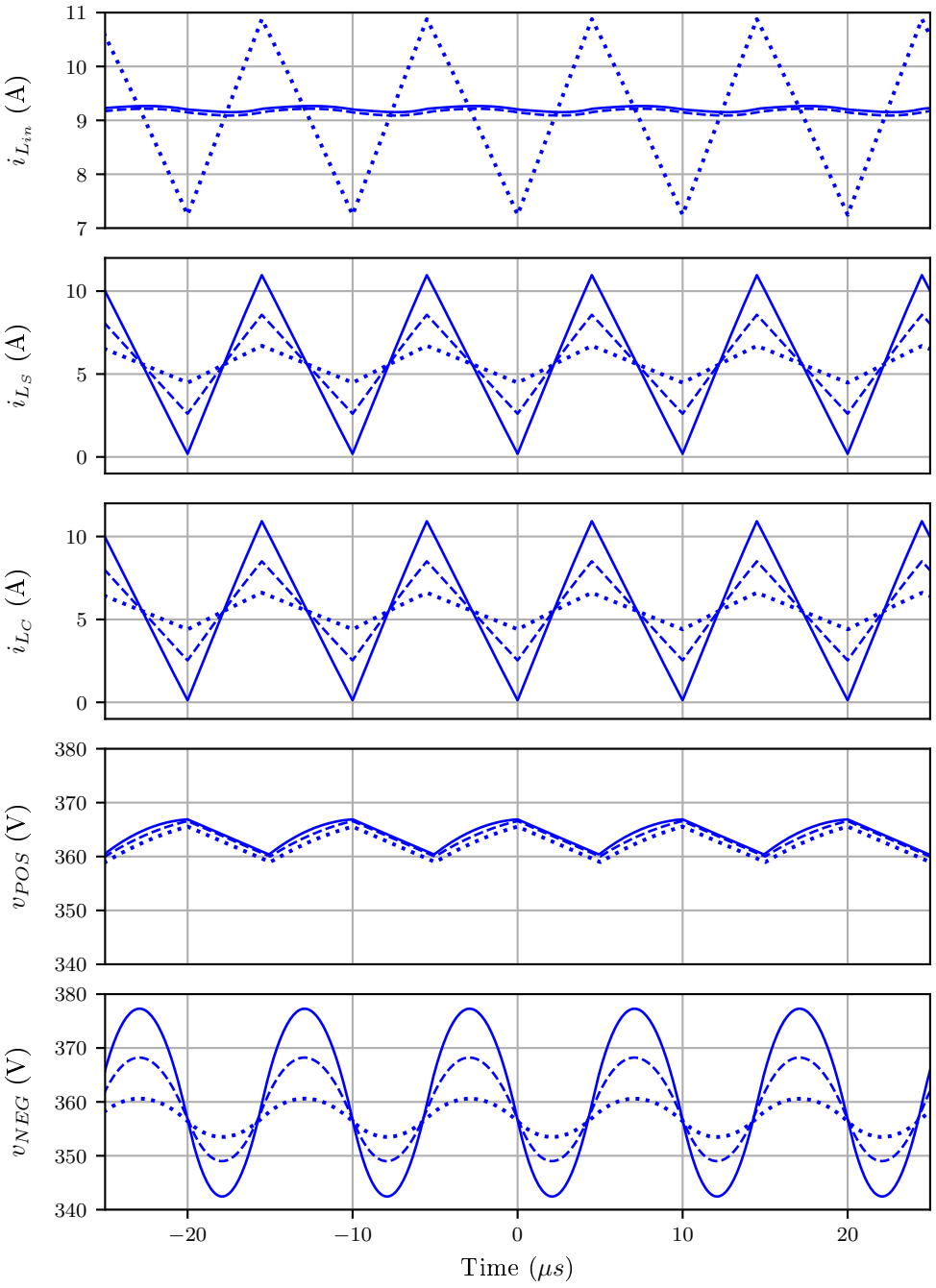


Figure 4.11: Converter waveforms at $V_{in} = 440\,V$ for various optimisations (none - dotted line; unconstrained - solid line; constrained - dashed line).

can be reduced by 96.9% compared to the CCS converter, with the same inductance and capacitance values (a reduction from from 40.0% to 1.24%, as shown in Table 4.2).

It can be seen that despite the massive reduction in input current ripple, there is a substantial increase in current ripple in the two output inductors, impacting the negative output voltage ripple (due to the nature of the LC filter at the Cuk converter's output). This problem can be addressed by leaving the output inductors uncoupled (i.e. constraining $k_3 = 0$), which will be discussed in Section 4.5.3.

Now, we have shown that a substantial reduction in input current ripple is possible, though in practice we are interested in a range of other objectives too. The following section discusses the broader aims of the CI-CCS converter design process, and the optimisation processes used to meet them.

4.5 Broader Optimisation of the CI-CCS Converter

4.5.1 Potential Optimisation Objectives

Designing a switched-mode converter of any type is a multidimensional optimisation process involving several interdependent parameters. Trade-offs exist everywhere, where increases in design parameters like switching frequency have negative impacts on losses, or reducing the size of some passives comes at the cost of having to increase the size of others. Thus, in addition to reduced input current ripple and total inductance, there are other objectives that may be considered when designing the CI-CCS converter. These include:

- *Constraining the inductor design:* Minimising the input current ripple might produce coupling factors that are difficult to obtain practically. We may want to apply other constraints to the coupling factors to simplify the inductor design (e.g. we may want all three inductors wound together so we only have a single magnetic structure; we may have a preference for toroidal cores over E-cores).

- *Constraining the coupling factors:* Depending on the core shape low coupling factors may be hard to achieve so it may be desirable to have tightly wound inductors with a high coupling factor. For example, coupled inductors with a low coupling factor may need complex shapes with precisely controlled air gaps. Conversely, tightly coupled inductors may be achieved with simple

core shapes, such as a toroid.

- *Altering the input current ripple target:* In Section 2.2.3, it was determined that a maximum current ripple of 5% should be enforced to ensure high levels of energy extraction from the PV array. In reality, even this target is flexible and it could be relaxed (to further reduce the inductor requirements) or tightened (to increase the energy extracted).

- *Output inductor current ripple:* Though we are primarily interested in the input current ripple, lower current ripple in the output inductors also has benefits (e.g. lower hysteresis losses and therefore higher efficiency, reduced output inductor size, reduced output capacitor size, option to reduce switching frequency).

- *Switching frequency:* A lower switching frequency may be desired to use a different semiconductor technology, or to reduce heat sinking requirements for the switching device (as the switching losses generally exceed the conduction and blocking losses). A lower switching frequency comes at the cost of increased passive component sizes and losses in other areas.

- *Internal (energy transfer) capacitor voltage ripple:* In Section 3.2.1, a 10% target for the internal capacitor voltage ripple was selected to guide the design and allow linear approximations to be used. In reality, this target can be relaxed. A larger voltage ripple would reduce the capacitances required, though potentially require higher voltage capacitors, and larger inductors. This additional degree of flexibility allows the size, efficiency, and cost of the converter to be optimised.

- *Internal inductor current ripple:* Like above, the 40% internal inductor current ripple target specified in Section 3.2.1 can be relaxed. Larger permissible current ripples reduce the inductances required, though this comes at the cost of increased capacitances.

- *Efficiency:* The different loss sources vary according to different parameters. For example the switching frequency impacts the switching device losses, copper losses (lower peak current but higher effective resistance due to the skin effect), eddy current losses, hysteresis losses, and capacitor ESR losses differently.

- *Volume, weight, and cost:* The design may be optimised to reduce the overall size of all the inductive and capacitive components, in applications where size and weight is a high priority.

4.5.2 Examples of CI-CCS Optimisations

In practice, all of the objectives given in Section 4.5.1 could be used for optimising the CI-CCS converter's design. Here, some examples of potential optimisations are given:

1. *Minimum input current ripple:* This is the optimisation that was carried out in Section 4.4.3, aiming to minimise the input current ripple by varying the coupling factors without any constraints.

2. *Minimum input current ripple with constrained inductor design:* The first optimisation process could produce coupling factors that are difficult to obtain practically, so it is possible to apply constraints to simplify the magnetic design. For example, restricting coupling factors to high values removes the need for precisely controlled air gaps. Also, the choice of core shape restricts coupling factors obtainable. For example, three windings on a single toroidal core can either have three positive coupling factors, or one positive and two negative coupling factors (and reversing the polarity of all three windings does *not* turn this into two positive and one negative coupling factor). With these constraints applied, the coupling factors can be varied to minimise the input current ripple.

3. *Minimum input current ripple with experimental flexibility:* This optimisation is a subset of the second optimisation with the constraint that $k_3 = 0$. This restriction means that the input inductor is coupled with both the SEPIC and Cuk output inductors, but these output inductors themselves are uncoupled. The benefits this has for simplicity and flexibility in the experimental design will be explained in Section 4.6, which details how such coupling factors are obtained. Removing coupling between the output inductors also solves the increase in output current ripple observed in Section 4.4.3 when the optimisation was run with k_3 left unconstrained.

4. *Minimum overall inductance:* In practice, the objective is unlikely to be simply to minimise inductance absolutely, but rather to meet a certain target, such as the 5% target set in Section 2.2.3. The first three optimisations listed here are based on the uncoupled inductances obtained previously, which are arbitrary here. Thus, the three inductances (L_{in}, L_S, L_C) should be considered as hyperparameters in addition to the coupling factors (k_1, k_2, k_3), in order to determine the minimum inductance values that would meet the ripple targets. Lower inductances typically mean smaller, lighter, and cheaper inductors. As previously seen, the worst case input current

ripple occurs at the maximum input voltage, so this optimisation should be performed at this voltage.

5. *Maximum efficiency:* The first four optimisations listed here are focused on the input current ripple, but this optimisation is concerned with improving the CI-CCS converter's efficiency. This would be achieved by defining how the various losses vary depending on other parameters. For example, switching losses decrease with frequency, but lower switching frequencies lead to higher copper losses (either through larger inductors which have higher resistances, or higher ripple components increasing rms inductor currents).

6. *Maximum PV energy extraction:* The previous optimisation focused on maximising the CI-CCS converter's efficiency, however this is not the same as maximising the overall power output of the PV system. This is because the PV array's average output increases as the input current ripple decreases, but the converter's maximum efficiency may not be at this low input ripple current level. Thus, an optimisation could be performed that accounts for the impact of varying input current ripple on both the PV array's average output and the CI-CCS converter's efficiency.

7. *Maximum volumetric or gravimetric power density:* An optimisation could be performed on the physical characteristics of the converter (e.g. size or weight). Once again, by varying parameters like the switching frequency, the size of the passive components can be reduced, though care must be taken include the required heat sink sizes resulting from changes in losses. Trade-offs also exist between inductances and capacitances, so different targets and values can be used to reduce the converter's size and weight.

8. *Hybrid optimisation:* Rather than optimising for a specific objective to the detriment of others, any number of objectives could be concurrently optimised. This requires the converter designer to define an appropriate cost function which includes all of the desired objectives, appropriate weighting factors, and any constraints which must be satisfied.

There are some constraints that should be considered irrespective of the objectives being optimised:

- *CCM operation:* All analyses in this thesis are on the basis of CCM operation of the CI-CCS converter. This operational mode is not essential for the converter's functioning, though it is important to note that below a certain load level the converter will transition into DCM operation, introducing additional switch states as discussed in Section 3.1.2. The previous component

sizing and rating equations provided in Section 3.2.4 and Section 3.2.5 were derived on the basis of the switch 'on' and 'off' states only, so a shift into DCM operation means that these derivations may no longer hold.

- *Converter performance objectives:* Constraints should be applied to ensure that the converter's performance objectives are still met during the optimisation process. For example, reducing the converter's volume through changes in switching frequency and internal ripple targets may result in output voltage ripple targets not being met.

- *Operational range:* Extending on the previous point, it should be ensured that the converter meets its performance requirements not only at the nominal conditions, but also over the entire operational range (for example, at the lower and upper input voltage limits).

In this thesis, the third optimisation (minimising input current ripple with experimental flexibility) is the most appropriate because it allows the benefits of coupling on the CCS converter to be experimentally demonstrated with flexibility and without an overly complicated magnetic design.

4.5.3 Minimising Input Current Ripple with Experimental Flexibility

There are several coupling factors that could demonstrate the reduced input current ripple of the CI-CCS converter, though in this thesis it is beneficial to:

- use the same inductance values as the uncoupled CCS converter to provide an accurate representation of the input current ripple reductions due to coupling factor changes alone

- have a system of coupled inductors that allows coupling factors to be modified relatively easily if required.

Leaving the inductances (L_{in}, L_S, L_C) at their uncoupled values satisfies the first point, and applying the restriction $k_3 = 0$ allows the second point to be achieved, by effectively splitting the input inductance into two, each half of which is coupled separately with the SEPIC and Cuk output inductors, as shown in Figure 4.15.

With this configuration, interdependencies are minimised so that k_1 and k_2 can be varied without affecting k_3. This is explained further in Section 4.6. One drawback with this configuration is that the coupling factors as previously defined

are limited to $k_{new} = \frac{k}{\sqrt{2}}$, because $M = k\sqrt{L_{in}L_{out}}$, so if L_{in} is halved then $M = k\sqrt{\frac{L_{in}}{2}L_{out}} = \frac{k}{\sqrt{2}}\sqrt{L_{in}L_{out}}$. It will be seen that isn't an issue in this case because the optimal coupling factor is lower than this limit.

Letting $k_1 = k_2\,(= k)$ and $k_3 = 0$ is equivalent to taking the diagonal cross-section of the centre graph of Figure 4.3 and Figure 4.7.

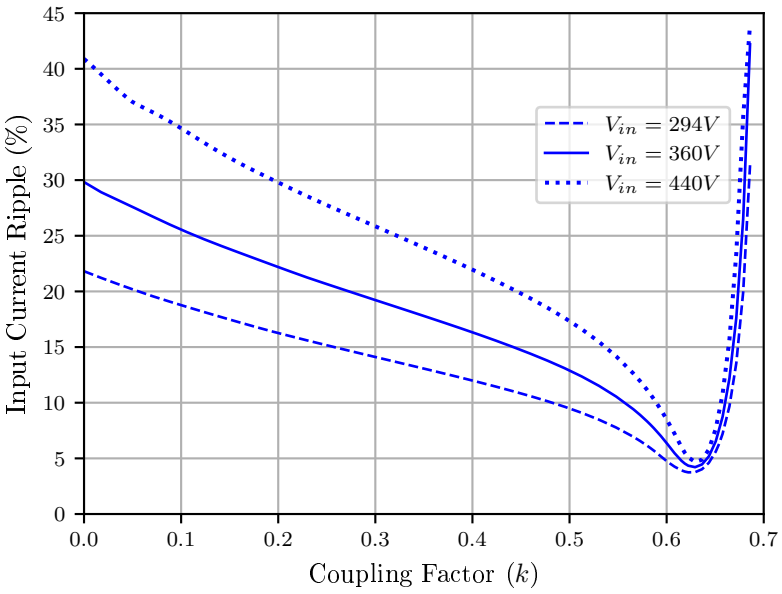
The converter is simulated at rated power using the Saber simulation platform. The resulting input current ripple as a function of coupling factor, k, can be seen in Figure 4.12a, which shows the sensitivity of the input current ripple against the coupling factor, k, at rated power. Using Figure 4.9, the range of k has been limited to exclude the region of high input current ripple. The three lines show the input current ripple (as a percentage of average input current) at the nominal input voltage (360 V), as well as at the limits of the input voltage range (294 V and 440 V). It is observed that the minimum ripple occurs at the same coupling factor, independent of input voltage and voltage conversion ratio.

Using Equation 4.38, the theoretical equivalent input inductances can be calculated for each value of k. With this, an input current ripple can be estimated using Equation 4.35. The results of this are shown in Figure 4.12b, which aligns closely with the simulation results in Figure 4.12a, with the exception of the area near zero ripple due to the approximations made in the analytical derivations neglecting high order harmonics. The theoretically expected optimal coupling factor for this scenario using Equation 4.38, is $k = 0.639$.

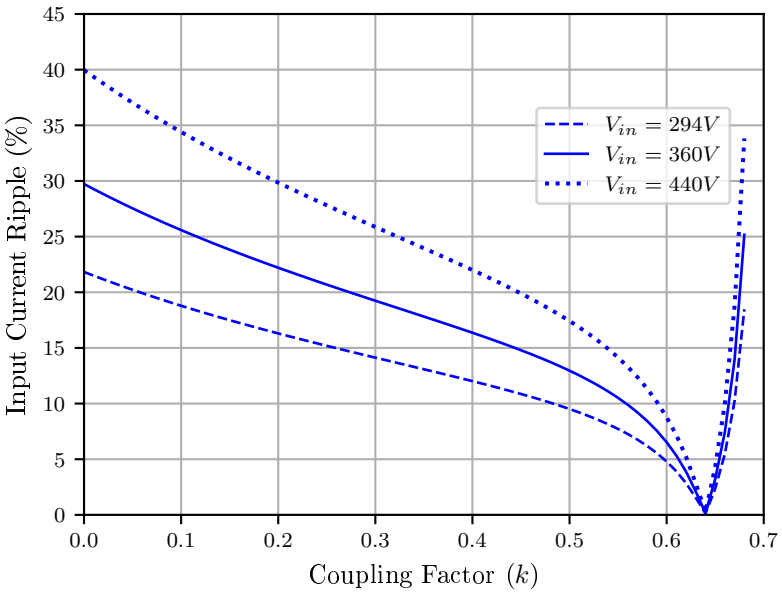
A Bayesian optimisation is performed on k to determine the optimal coupling factor. The results of this optimisation are shown in Figure 4.13, demonstrating that the curve in Figure 4.12a can be recreated with far fewer simulations. The optimal coupling factor determined through this simulation-based optimisation is $k = 0.631$, demonstrating that the theoretical and simulation results are highly consistent. This result shows a significant decrease in input current ripple of more than 80% for all three input voltages.

The most relevant component waveforms of these simulations are shown in Figure 4.14, which also shows the same waveforms for the standard (uncoupled) CCS converter obtained in Section 3.3. The key observation is the significant decrease in the input current ripple in the coupled inductors scenario, without negatively impacting any other component current or voltage waveforms.

The average input current remains the same regardless of coupling factor, however the ripple component is significantly reduced when a 0.631 coupling factor between input and output inductors is used. The input current ripple (peak-to-peak) as a

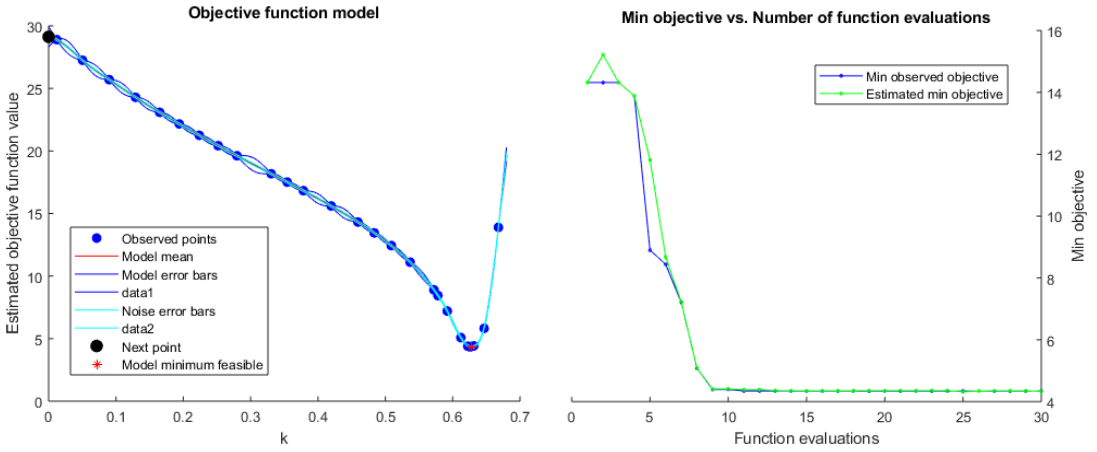


(a) Simulation results.



(b) Analytically obtained.

Figure 4.12: Input current ripple vs. coupling factor at rated power for the limit and nominal input voltages.



(a) Objective function model.

(b) Minimum objective vs. number of evaluations

Figure 4.13: Bayesian optimisation to obtain the optimal coupling factor, k, with $k_3 = 0$.

percentage of average input current at rated power (4 kW) is shown in Table 4.3. These results demonstrate that the optimal coupling factor reduces input current ripple by 82% to 88% compared with the uncoupled scenario.

Table 4.3: Input current ripple at various coupling factors and input voltages.

Coupling	Input current ripple (percentage of average)		
	$V_{in} = 294\,V$	$V_{in} = 360\,V$	$V_{in} = 440\,V$
None ($k = 0$)	21.8%	29.7%	40.0%
Optimal ($k = 0.631$)	3.8%	4.2%	4.7%

The current and voltage ripples in the output inductors and capacitors aren't increased when $k_3 = 0$, addressing the issues created when k_3 was left unconstrained in the optimisation undertaken in Section 4.4.3.

The peak-to-peak output voltage ripple is measured to be 1.8% for the positive DC output and 2% for the negative DC output, fulfilling the design requirements. These values remain largely constant over variations in both input voltage and coupling factor.

4.6 Experimental Design of the Coupled Inductors

The previous sections investigated various optimisations to reduce the input current ripple, with a focus on one which applied the constraint $k_3 = 0$ in order to demonstrate the CI-CCS concept whilst maintaining the flexibility to adjust

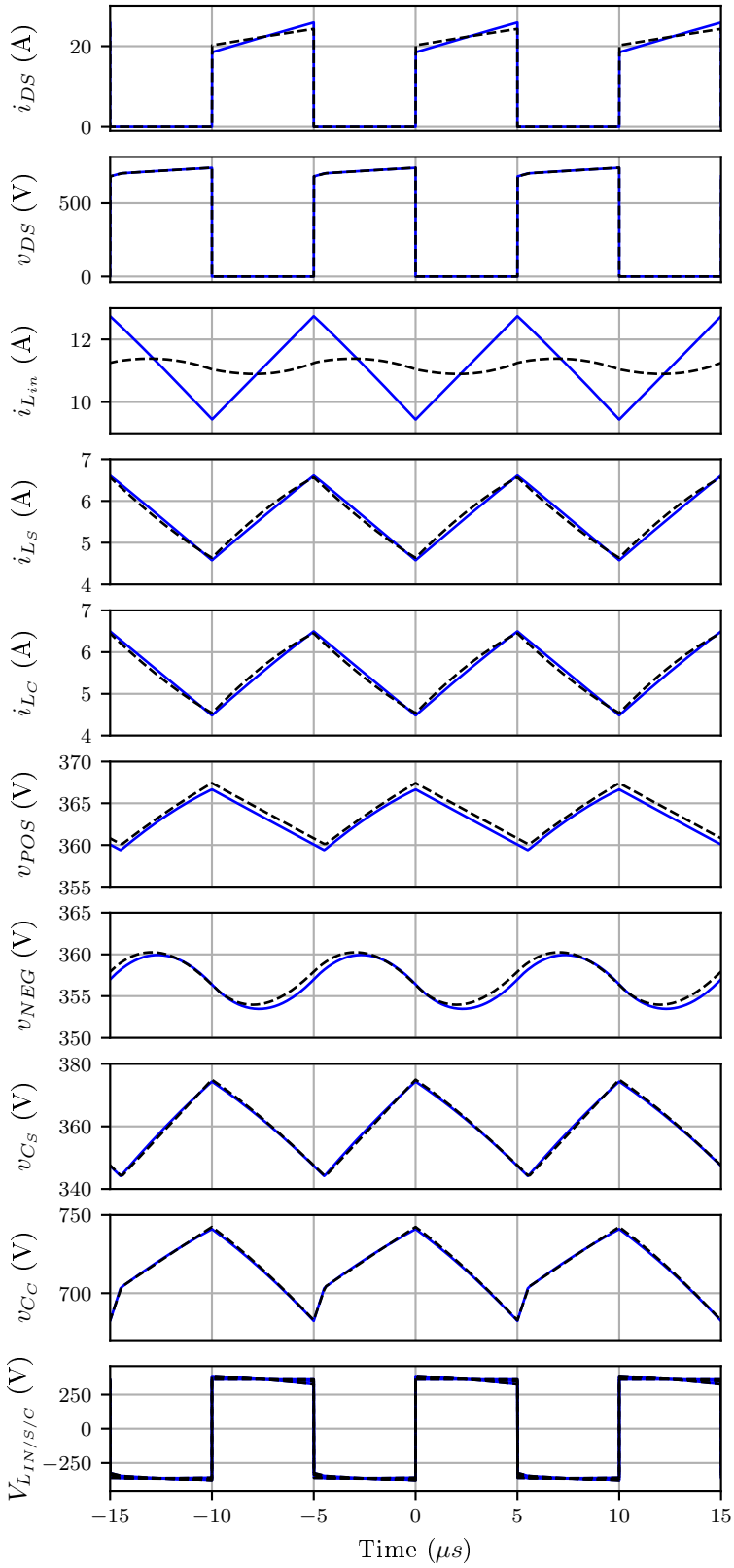
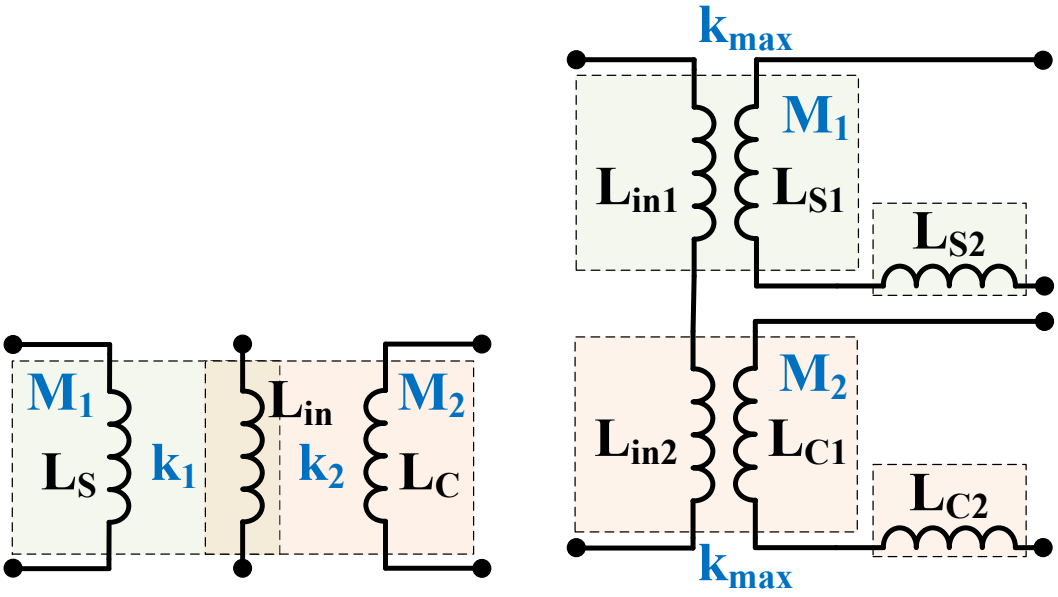


Figure 4.14: Switch current (i_{DS}), switch voltage (v_{DS}), $i_{L_{in}}$, i_{L_S}, i_{L_C}, v_{POS}, v_{NEG}, v_{C_S}, v_{C_C}, $v_{L_{in/S/C}}$ with $V_{in} = 360\,V$.



(a) Specialised design.

(b) Simple equivalent design.

Figure 4.15: Specialised vs. simple equivalent coupled inductors.

coupling factors. This optimisation produces a set of coupling factors, as shown in Figure 4.15a.

This section details the full design process for these custom-made coupled inductors. Different coupling factors can be realised by connecting tightly coupled toroidal inductors ($k = k_{max} \approx 1$) in series with separate uncoupled inductors, as shown in Figure 4.15b.

The self and mutual inductances of the coupled inductors in Figure 4.15a are:

$$L_{in} = L_{in} \tag{4.39}$$

$$L_S = L_S \tag{4.40}$$

$$L_C = L_C \tag{4.41}$$

$$M_1 = k_1 \sqrt{L_{in} \times L_S} \tag{4.42}$$

$$M_2 = k_2 \sqrt{L_{in} \times L_C} \tag{4.43}$$

Similarly, the self and mutual inductances of the tightly coupled inductors in

Figure 4.15b are:

$$L_{in} = L_{in1} + L_{in2} \tag{4.44}$$

$$L_S = L_{S1} + L_{S2} \tag{4.45}$$

$$L_C = L_{C1} + L_{C2} \tag{4.46}$$

$$M_1 = k_{max}\sqrt{L_{in1} \times L_{S1}} \tag{4.47}$$

$$M_2 = k_{max}\sqrt{L_{in2} \times L_{C1}} \tag{4.48}$$

Note that the input inductance has been split into two, where $L_{in1} = L_{in2} = 0.5 \times L_{in}$. If two coils tightly wound on the same toroidal core have a coupling factor of $k_{max} \approx 1$, then L_{S1} and L_{C1} can be calculated by rearranging Equation 4.47 and Equation 4.48, where the values for M_1 and M_2 are obtained from the desired values given in Equation (4.42) and Equation (4.43). This produces the expressions for L_{S1} and L_{C1} given in Equation (4.49) and Equation (4.50):

$$L_{S1} = 2\left(\frac{k_1}{k_{max}}\right)^2 L_S \tag{4.49}$$

$$L_{C1} = 2\left(\frac{k_2}{k_{max}}\right)^2 L_C \tag{4.50}$$

It is then easy to calculate the separate series-connected inductances required, L_{S2} and L_{C2} by using Equation (4.51) and Equation (4.52):

$$L_{S2} = L_S - L_{S1} \tag{4.51}$$

$$L_{C2} = L_C - L_{C1} \tag{4.52}$$

This means that the overall mutual and self inductance (and hence performance) are identical to what would be obtained with a specialised inductor design.

The design requirements from the optimisation process are:

$$L_{in} = 545\,\mu H \tag{4.53}$$

$$L_S = 891\,\mu H \tag{4.54}$$

$$L_C = 891\,\mu H \tag{4.55}$$

$$k_1 = k_2 = 0.631 \tag{4.56}$$

$$k_3 = 0 \tag{4.57}$$

With the equations in this section, the parameters in the 'simple equivalent' in-

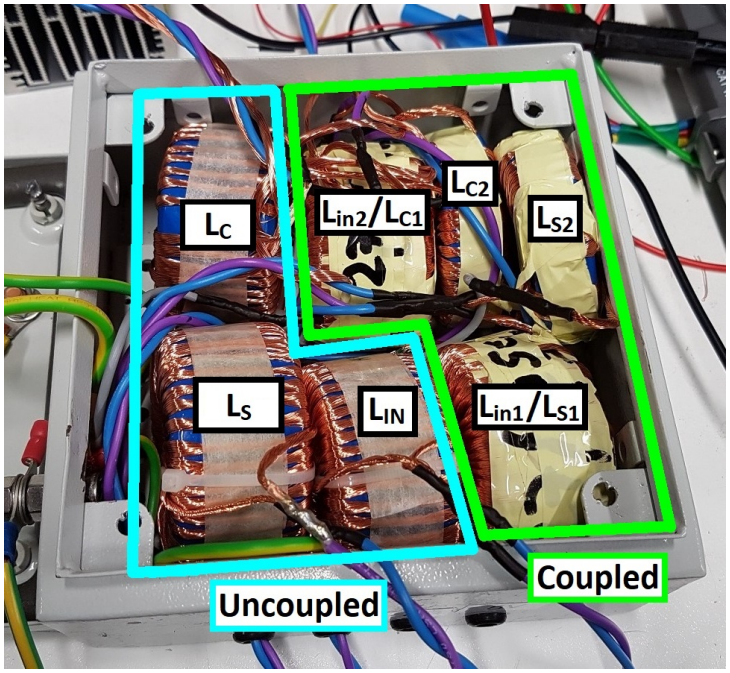


Figure 4.16: Coupled and uncoupled inductors.

ductor design are determined to be:

$$L_{inA} = 272.5\,\mu H \tag{4.58}$$

$$L_{S1} = 710\,\mu H \tag{4.59}$$

$$L_{S2} = 181\,\mu H \tag{4.60}$$

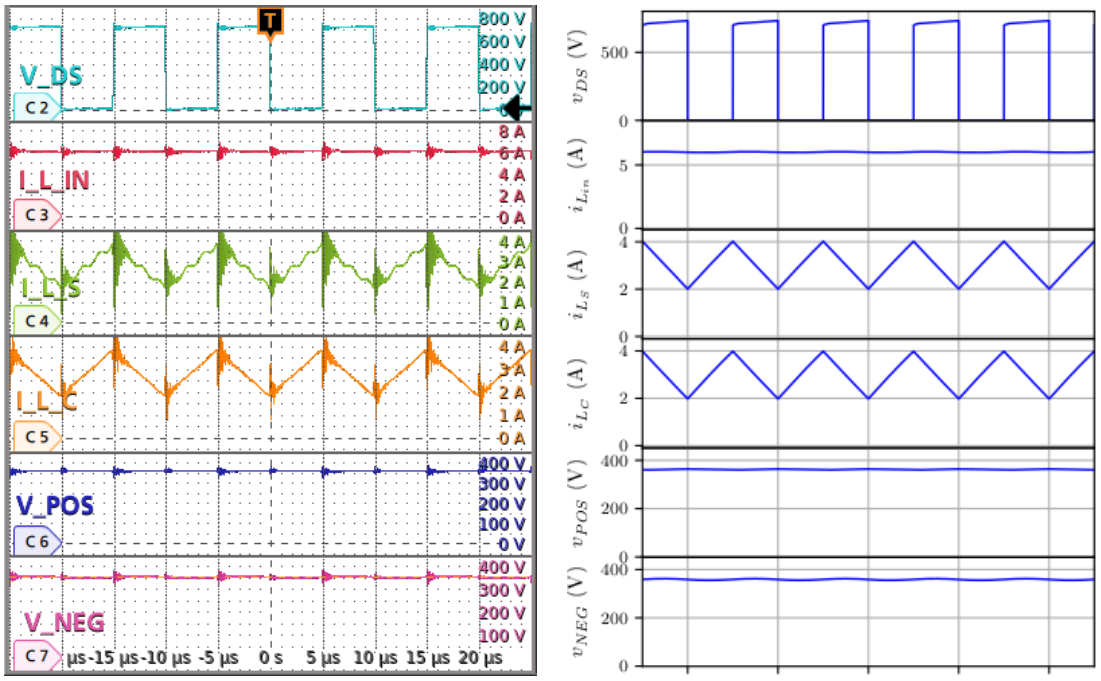
$$L_{inB} = 272.5\,\mu H \tag{4.61}$$

$$L_{C1} = 710\,\mu H \tag{4.62}$$

$$L_{C2} = 181\,\mu H \tag{4.63}$$

$$k_{max} \approx 1 \tag{4.64}$$

With these parameters, the number of turns needed to produce the necessary inductance for each core is calculated, and the inductors are hand-wound with this required number of turns. The final uncoupled and coupled inductors used in the experimental testbed are shown in Figure 4.16.



(a) Coupled inductors: experimental results.

(b) Coupled inductors: simulation results.

Figure 4.17: Comparison of experimental and simulation waveforms for the CI-CCS converter: MOSFET voltage (v_{DS}), $i_{L_{in}}$, i_{L_S}, i_{L_C}, v_{POS}, v_{NEG} (with $V_{in} = V_{POS} = V_{NEG} = 360\,V$).

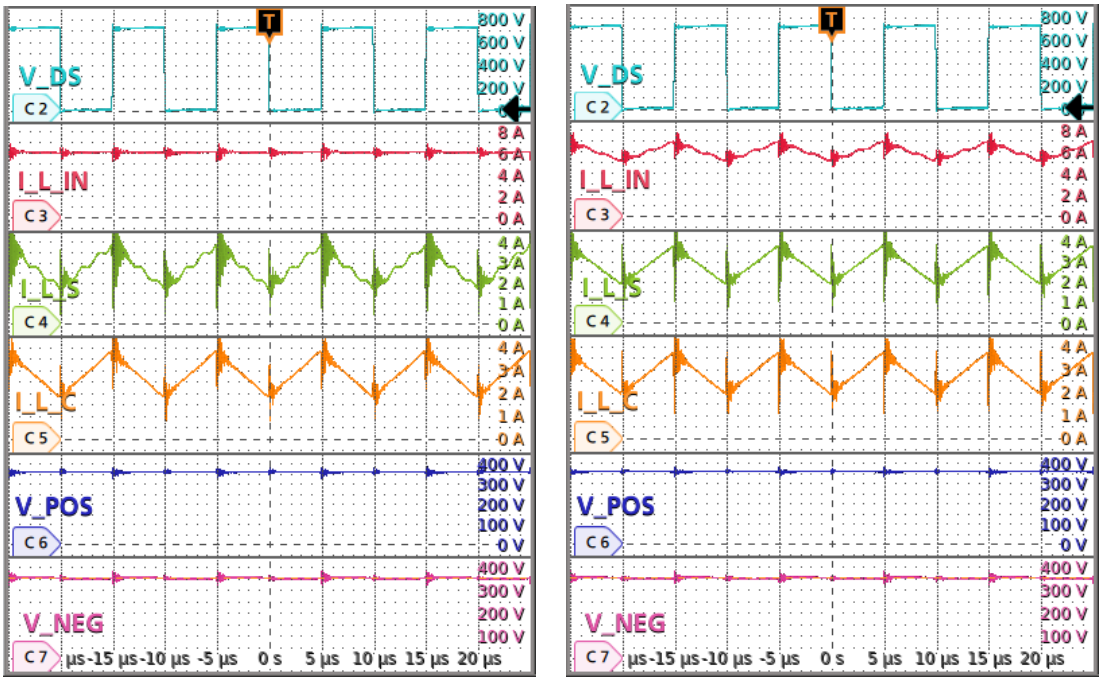
4.7 Experimental Evaluation of the CI-CCS Converter

4.7.1 CI-CCS and CCS Converter Results Comparison

With these coupled inductors, it is possible to experimentally evaluate the CI-CCS converter's performance. The resulting waveforms are presented in Figure 4.17a and Figure 4.18a (duplicated for easier side-by-side comparison), demonstrating the operation and performance of the CI-CCS converter with an output power of 2160 W.

Simulation results similar to those in Section 4.5.3 have been obtained, however the output power and passive component values have been modified to match the experimental configuration. The set of waveforms corresponding to the experimental waveforms has been presented in Figure 4.17b, to provide a clear side-by-side comparison.

This comparison demonstrates that the simulation and experimental waveforms are highly consistent, validating both the simulation studies and the analytical



(a) Coupled inductors: experimental results.

(b) Uncoupled inductors: experimental results.

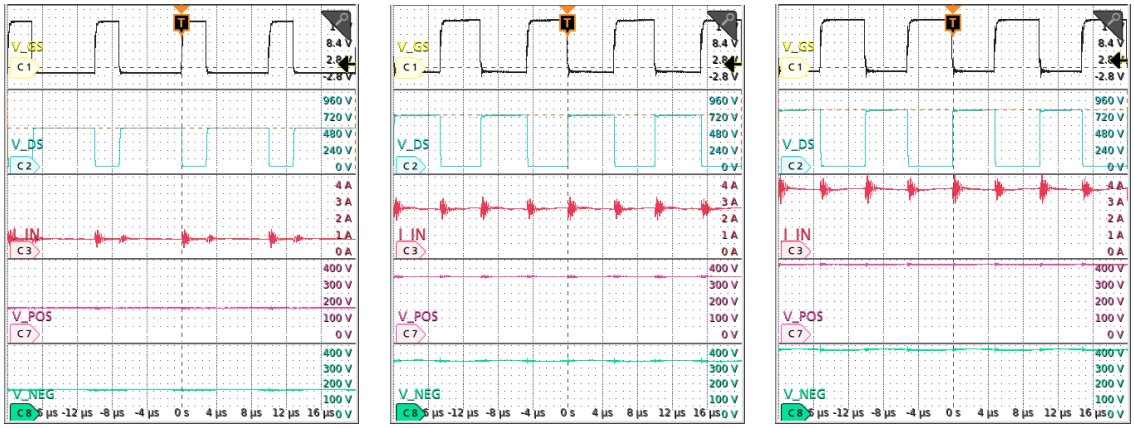
Figure 4.18: Experimental comparison of the CI-CCS converter and the CCS converter: MOSFET voltage (v_{DS}), $i_{L_{in}}$, i_{L_S}, i_{L_C}, v_{POS}, v_{NEG} (with $V_{in} = V_{POS} = V_{NEG} = 360\,V$).

derivations presented. As in the previous chapter, a notable difference between the experimental and simulation results is the presence of ringing at the switching transients. This ringing is due to parasitics present in the converter, particularly in the inter-turn capacitance of the hand-wound inductor windings, and so it is expected that with better inductor and winding design, this ringing would reduce substantially.

The experimental waveforms of the previous (uncoupled) CCS converter from the Chapter 3 have been included again here in Figure 4.18b to give a direct comparison of the CI-CCS converter and the CCS converter. This side-by-side comparison of the experimental results obtained with all parameters, except the coupling factors, being equal, clearly shows the large reduction in input ripple current when coupled inductors are used.

When all inductors are left uncoupled, the peak-to-peak input current ripple is 30.2%. When the integrated magnetics are introduced, the peak-to-peak current ripple drops to just 2.0%, representing a reduction of more than 93%.

It can also be seen that there is a minor imbalance between the positive and negative output voltages due to component non-idealities impacting each converter differently. The peak-to-peak output voltage ripple is measured to be 1.2% for the



(a) Step-down ($I_{in} = 0.6\,A$). (b) Step-down ($I_{in} = 2.8\,A$). (c) Step-up ($I_{in} = 3.5\,A$).

Figure 4.19: Switch signal (v_{GS}), MOSFET voltage (v_{DS}), $i_{L_{in}}$, v_{POS}, v_{NEG} (with $V_{in} = 400\,V$, at different output voltages).

positive DC output and 2.3% for the negative DC output, and these values remain largely constant over variations in both input voltage and coupling factor.

4.7.2 Other Voltage Gain Ratios

In addition to the previous results which show a unity voltage gain for each individual output (360 V input and 360 V on each output), three additional sets of results are presented to demonstrate the wide voltage conversion ratios possible with this converter. These three tests are conducted with the same input voltage (400 V) but with different duty cycles:

- Figure 4.19a shows a step-down in both individual output voltages, as well as the overall positive-to-negative voltage bus.
- Figure 4.19b shows a step-down for each individual output voltage (from an input of 400 V to an output per bus of 360 V), but an overall step-up of the positive-to-negative voltage bus (from an input of 400 V to an combined output of 720 V).
- Figure 4.19c shows a step-up in both individual output voltages, as well as the overall positive-to-negative voltage bus.

It can also be observed that the input current ripple remains small in these scenarios. With the steady-state operation of the CI-CCS converter now studied under balanced conditions, the next chapter aims to undertake a more advanced evalu-

ation of the converter's performance.

4.8 Chapter Conclusion

This chapter introduced a converter which remedies an important issue with the CCS converter: its relatively large input curent ripple. The modified converter, known as the CI-CCS converter, derives its benefits from magnetically coupling the CCS converter's three inductors. Analytical derivations were carried out to demonstrate the theoretical basis of the reduced input current ripple resulting from an increased equivalent input inductance. This analysis involved exploring the impact of all possible coupling factors, before providing some simplifying assumptions that could be made given the results obtained.

Simulation studies were then undertaken to validate the analytical work, with the results being highly consistent with the theoretical expectations. As these simulations are computationally intense, a less costly (time-wise) process was required, so a number of optimisation techniques were reviewed, with Bayesian optimisation deemed the most useful in this application. A Bayesian optimisation was performed to determine a set of coupling factors which minimised the input current ripple. With the same passive component values, the worst-case input ripple current could be reduced from 40% to 1.78%, however this came at the expense of increased ripples in the output inductor currents and negative output voltage. The proposed Bayesian optimisation can also be used for optimising other objectives in addition to the input current ripple.

Next, a discussion was provided about broader potential optimisation objectives beyond minimising input current ripple. One such Bayesian optimisation was undertaken with a constraint on the permissible coupling factors ($k_3 = 0$), and the worst-case input current was reduced from 40% to 4.7%, though this time with no negative impact on other component waveforms (e.g. peak currents or voltages). This produced a system of coupled inductors that provided experimental flexibility and easy of prototyping, in addition to demonstrating the primary objective of reducing the input current ripple.

The hardware design process for these coupled inductors was detailed, followed by experimental results. These results were once again highly consistent with both the simulation results and theoretical expectations, and demonstrate a significant reduction in input current ripple. Additional results were also presented to show the wide voltage conversion range achievable with the CI-CCS converter.

Chapter 5

CI-CCS Converter Control and Performance Analysis

The previous chapters demonstrated the benefits that inductor coupling can bring to the CCS converter, particularly in solar PV applications. This chapter presents an in-depth exploration of the CI-CCS converter in terms of its control and performance. The converter's control strategies are presented, its losses are characterised to ascertain its efficiency, and its performance under non-ideal conditions is examined.

5.1 Controller Design and Performance

For practical use in almost all applications, DC-DC converters must have their input(s) and/or output(s) regulated in some way. This regulation is typically provided in the form of a closed-loop current or voltage controller. For example, applications involving batteries usually employ both constant voltage and constant current modes for charging. For applications where the DC-DC converter is supplying a load, the output voltage is usually regulated (e.g. laptop power supply), and for PV applications the converter's input voltage and current are controlled to ensure operation at the MPP.

In this work, the CI-CCS converter will transfer power from PV panels to an inverter. The overall control structure of the converters will be examined in Section 6.2, though for now it is sufficient to say that the CI-CCS converter must have its innermost control loop regulating the input current for MPPT purposes.

5.1.1 Input Current Controller

Control of the CI-CCS converter's input current is achieved with a closed-loop controller, which senses the input current and adjusts the MOSFET's duty cycle accordingly. A Proportional Integral (PI) controller is chosen due to its simplicity. There are several open-loop and closed-loop methods of tuning the PI controller's two parameters, and the method selected here due to its simplicity is the closed-loop Ziegler-Nichols method, which is a heuristic tuning method that does not require a model of the system [133–136]. The resulting controller parameters obtained using this tuning method tuning are $P = 3$ and $I = 830$, at a control frequency of 100 kHz. The performance of this controller can be demonstrated in two ways:

1. *Apply a step change to the reference current*, with the input voltage held constant. If the reference current is increased then the input power must increase, and so too will the output power. The controller will achieve this by adjusting the duty cycle to raise the output voltage, to increase the power dissipated in the resistors according to $P = \frac{V_{out}^2}{R}$. The converse will happen if the reference current is decreased.

2. *Apply a step change to the input voltage*, with the reference current held constant. This is equivalent to the previous case where the input power, and hence output power, will change in proportion to the change in input voltage.

The second method of demonstrating the controller's performance is limited by the rate of change of the input DC voltage. Most controllable DC voltage sources have quite slow slew rates (relative to the converter and controller bandwidth), so the first method is preferable to highlight the converter's fast dynamic response.

The current controller receives a continuously updated reference value from the MPPT controller. The reference generated by the MPPT would typically vary smoothly, however to demonstrate the performance of the current controller, a step change in the reference current is demanded. A test was conducted with the input current initially regulated to 1 A, with a step change in the reference current to 3 A at 0 ms. As the input voltage is held constant at 200 V, this corresponds to a step increase in the input power changes of 400 W (10% of rated power).

Figure 5.1 shows the converter's response to this step change. These results demonstrate that the converter is capable of tracking a 400 W step change in under 4 ms, meaning that its bandwidth is easily sufficient for optimal MPPT performance

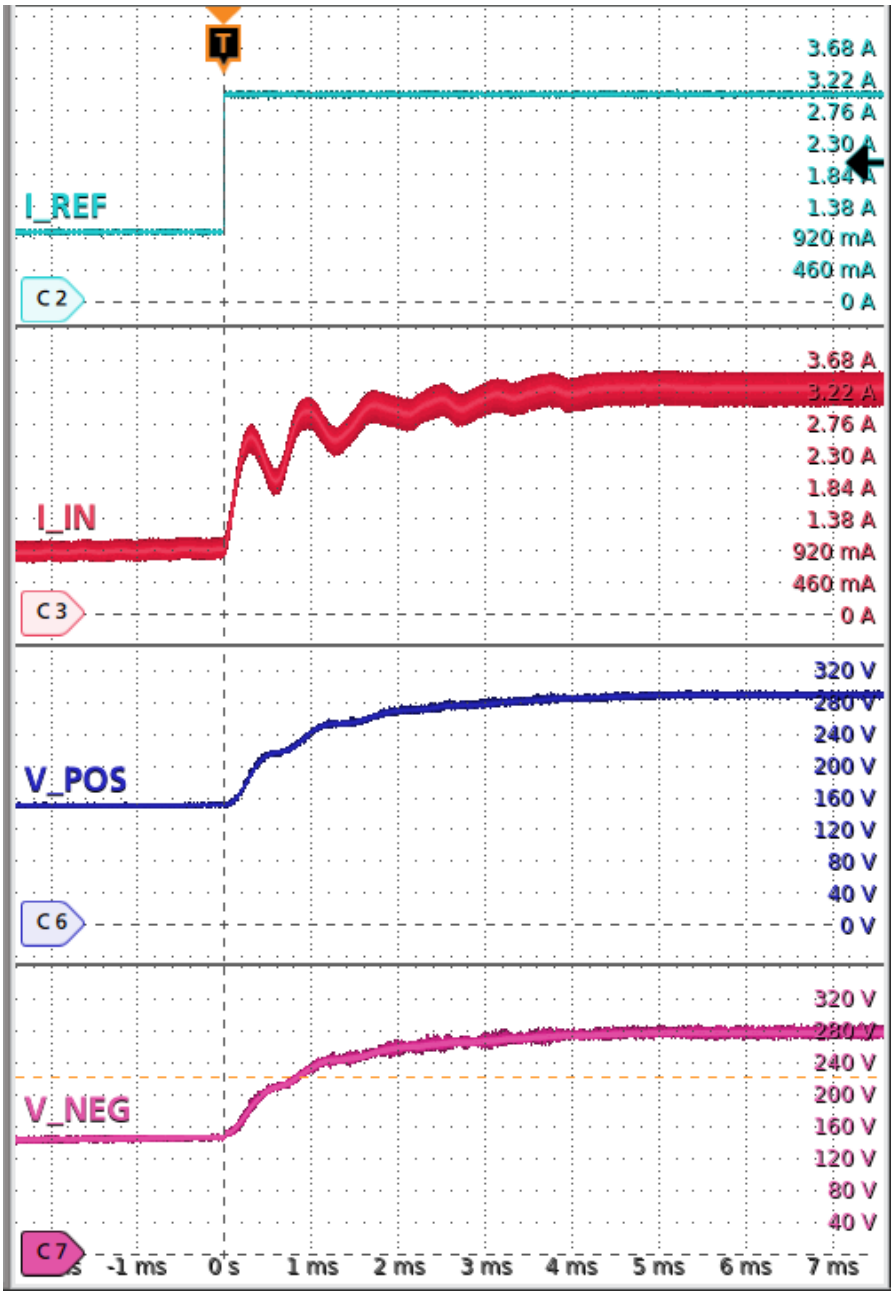


Figure 5.1: Reference input current ($i_{in_{ref}}$), Measured input current (i_{in}), v_{POS}, v_{NEG} (with $V_{in} = 200\,V$).

(as the fastest changes in panel conditions are typically in the order of seconds). The converter achieves this current control by increasing the duty cycle, such that the output voltage (and hence output power) increases. With a constant input voltage, the input current must therefore increase in order to supply the bigger output power. The 'thickness' of the input current waveforms is not from the switching frequency ripple, but rather from the ringing that was observed in previous results.

5.2 Efficiency and Loss Characterisation

An important performance characteristic of any power converter is its efficiency. The overall efficiency is calculated by dividing the measured output power by the measured input power. The converter losses (i.e. the difference in these powers) can be broadly categorised into:

1. *MOSFET switching losses:* These losses can be further separated into turn-on and turn-off losses. They result primarily from the simultaneous voltage across, and current through, the MOSFET during switching transients. Typically, turn-on losses outweigh turn-off losses due to the slower nature of device turn-on.

2. *MOSFET conduction losses:* These I^2R losses stem from the on-state resistance ($R_{DS_{on}}$) of the MOSFET.

3. *Diode conduction losses:* These losses stem from the forward voltage drop across the diodes when they are conducting.

4. *Diode switching losses:* These losses stem from the reverse recovery characteristics of the diodes. When SiC Schottky diodes are used, this reverse recovery is minimal and so these losses may be neglected.

5. *Inductor core losses:* These losses can be further separated into hysteresis losses and eddy current losses.

   (a) *Hysteresis losses:* These losses stem from the energy lost in charging and discharging the magnetic core as its magnetic field strength (and hence field density) vary due to varying inductor currents. The losses depend on the width of the B-H curve (largely dependent on the size of the current ripple), and the height of the B-H curve (largely dependent on the core material).

(b) *Eddy current losses:* These resistive losses stem from the currents induced by the changing magnetic field in the inductors. These losses can be reduced or eliminated when a non-conducting core is used, or when the core is made with insulated laminations to reduce the loop size.

6. *Copper losses:* These I^2R losses stem from the resistance of the conductors used in the windings of the inductors. The rms current is close to the DC average, though as the ripple component increases so too does the rms current.

7. *Capacitor losses:* These losses include the equivalent series resistance (ESR) and dielectric losses, and increase as the rms current through the capacitors increase.

Each of these sources of losses is dependent on a number of parameters, including switching frequency, temperature, voltage, and current In this application, with a fixed (and already decided) switching frequency and a stable temperature (due to good cooling), the main factor impacting the efficiency is the output power. Hence, it is desirable to measure the efficiency over a range of output powers.

When comparing the uncoupled CCS converter with the CI-CCS converter, it is expected that the CI-CCS converter would have slightly lower losses due the following:

- Inductor copper losses are expected to decrease because:
  - As the triangular ripple current components reduce and the current waveforms move closer to their average, the rms values also decrease. This reduction in rms current leads to a reduction in I^2R losses.
  - If the ripple component is kept constant and the inductor size is instead reduced, the I^2R losses will decrease due a lower resistance associated with fewer windings required to produce the smaller inductance.
- Hysteresis losses are dependent on the area inside the hysteresis loop. If the inductor current ripple is reduced, then the ripple in the magnetic field strength will also reduce, causing the area inside the hysteresis loop to decrease. This decreased area will lead to lower hysteresis losses.
- As the current ripple reduces, the current flowing through the capacitors will decrease. For a given ESR value, a smaller capacitor current leads to reduced ESR losses.

Tests are conducted at the nominal input and output voltages (360 V), and the

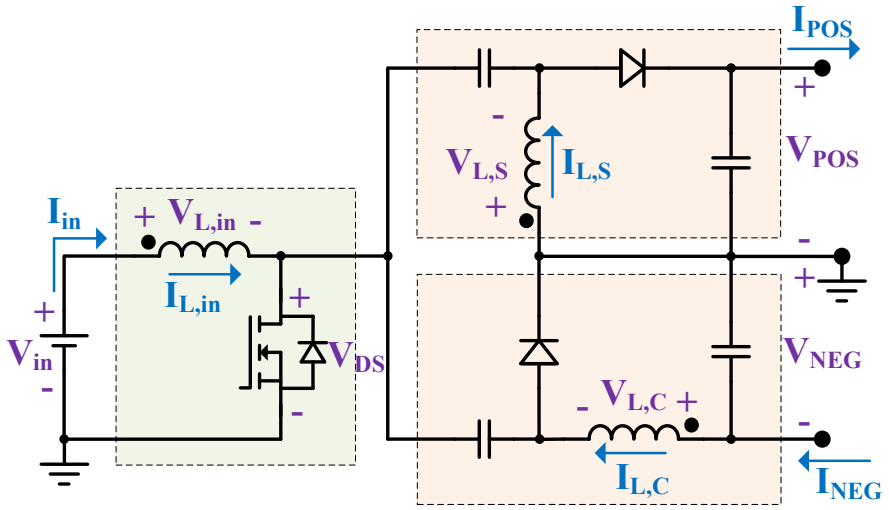


Figure 5.2: CI-CCS topology showing the variables measured for efficiency calculations.

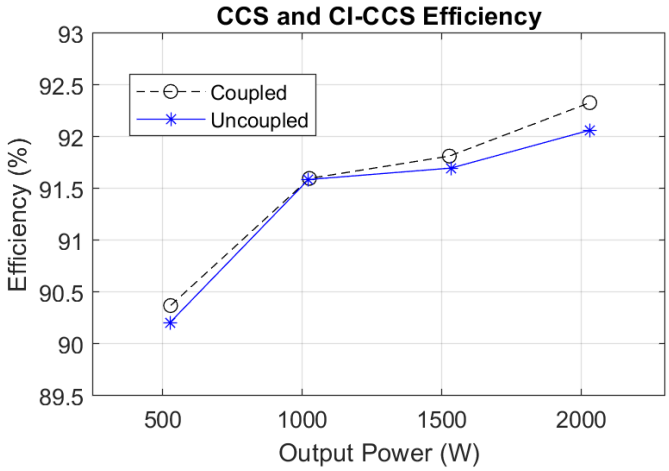


Figure 5.3: Efficiency measurements for the CCS and CI-CCS over a range of output powers at the nominal input voltage condition ($V_{in} = 360\,V$).

load is varied by changing the resistance connected to each output from 480 Ω to 120 Ω, corresponding to a range of combined output powers spanning from 540 W to 2160 W (assuming $V_{OUT} = 360\,V$).

Figure 5.2 shows the variables measured in the converter during the efficiency tests. These variables, in combination with datasheet information, have been used to determine the contribution of some loss sources as later detailed.

Figure 5.3 shows the measured efficiency for both the CCS and CI-CCS converters. The efficiency remains largely constant over the range of powers tested, and is very similar between the CCS and CI-CCS converters, with the CI-CCS converter's efficiency being slightly higher, as expected. The raw data in Table 5.1 shows that the CI-CCS converter is more efficient than the CCS converter at all data points,

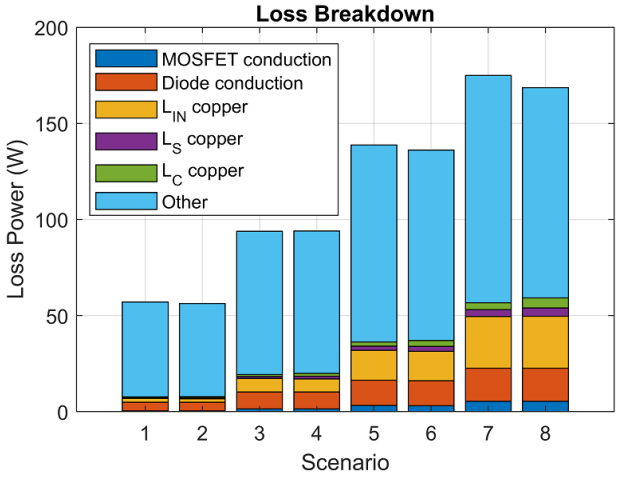


Figure 5.4: Loss breakdown for the CCS and CI-CCS converters at various output powers.

Table 5.1: Efficiency of the CCS and CI-CCS converters at various output powers.

Output Power (W)		Efficiency (%)	
CI-CCS	CCS	CI-CCS	CCS
528	525	90.4	90.2
1025	1022	91.6	91.6
1526	1533	91.8	91.7
2029	2029	92.3	92.1

however this difference is marginal, on average being just 0.15% better. The major advantage in solar PV applications comes from the reduced current ripple which facilitates PV operation closer to the MPP, hence improving the overall system efficiency.

Next, it is desirable to segment these losses into the categories described previously. The losses can be determined as follows:

1. *Inductor copper losses:* Calculated by measuring the inductor currents and resistances

2. *MOSFET conduction losses:* Calculated with the total MOSFET current ($i_{MOSFET} = i_{L_{in}} + i_{L_S} + i_{L_C}$) and the MOSFET's on-state resistance or measured v_{DS}

3. *Diode conduction losses (combined):* Using the combined diode current ($i_{D_S} + i_{D_C} = i_{L_{in}} + i_{L_S} + i_{L_C}$) and the diodes' forward voltages

4. *Other:* The rest of the losses combined (primarily MOSFET switching, but also inductor core and capacitor ESR losses) can be calculated subtracting the calculated losses above from the total power loss ($P_{loss} = P_{in} - P_{out}$).

The loss breakdowns are shown in Figure 5.4, where the eight stacked graphs correspond to the efficiency measurements in Figure 5.3 (scenarios 1 and 2 correspond to the 500 W output, both uncoupled and coupled; scenarios 3 and 4 correspond to the 1000 W output, uncoupled and coupled; scenarios 5 and 6 correspond to the 1.5 kW output, uncoupled and coupled; and scenarios 7 and 8 correspond to the 2 kW output, uncoupled and coupled). The height of these bars are equal to the total loss in each scenario.

The portion of the 'other' segment resulting from the switching losses can be estimated using the ROHM SCT3030KL datasheet. The turn-on and turn-off losses (E_{on} and E_{off}) are listed as $468\,\mu J$ and $204\,\mu J$ respectively. By using the graphs provided, these values can be scaled based on the drain-to-source voltage, drain current, and external gate resistances. The resulting values can then be summed and multiplied by the switching frequency to obtain the switching loss. Following this process, the switching losses are estimated as 30 W in the lowest output power scenario, and 100 W in the highest output scenario. This demonstrates that switching losses are the single largest loss source, suggesting that the converter's efficiency could be improved significantly if a lower switching frequency is used. In this thesis, reducing the input current ripple has been the main objective (with no consideration to the efficiency), and a lower switching frequency would usually require prohibitively large inductors. The results of the last chapter show that it is possible to obtain substantial reductions in input current ripple with the use of coupled inductors, suggesting that the switching frequency could be reduced considerably whilst still meeting current ripple targets with reasonable inductances. Thus, a converter using coupled inductors has the potential for much better efficiencies compared with an equivalent converter without coupled inductors.

Similarly, the large inductor copper losses suggest that the efficiency could be improved if smaller inductances (with fewer turns and hence lower resistance) are used. Once again, this option is made possible due to inductor coupling enabling low input current ripple targets to be met with smaller inductances.

Finally, the diode conduction losses may be reduced by changing to a diode technology with a lower forward voltage drop, though this would come at the cost of increased switching losses (due to the reverse recovery of silicon diodes). This trade-off would need to be evaluated based on the power ratings and switching frequency of the converter being designed.

5.3 Imbalance Analysis

Until now it has been assumed that the load is distributed equally across the positive and negative DC outputs. In this section, the way the CCS and CI-CCS converters respond to load imbalances is examined. This is particularly relevant for grid-connected applications because when the DC-DC converter is feeding a bipolar input inverter, power is drawn separately from each DC output in a time-varying manner. This will be examined further in Section 6.3.

Here, the converter is studied in steady-state with the load varying from only on the positive output terminal, to balanced, to only on the negative output terminal. Three sets of results have been obtained to determine if the converter's performance changes over its duty cycle range: step-down operation (with a 45% duty cycle), unity gain operation (with a 50% duty cycle), and step-up operation (with a 55% duty cycle).

The impact these load imbalances have on the output voltages is shown in Figure 5.5a (step-down operation), Figure 5.5b (unity gain operation), and Figure 5.5c (step-up operation). The voltage imbalance can be calculated as either output voltage relative to the average output voltage. The advantage of defining the imbalance relative to the average output voltage is that the magnitude is the same regardless of which output is considered, whereas defining the imbalance as V_{POS} relative to V_{NEG} would produce a different result to defining it as V_{NEG} relative to V_{POS}. Here positive imbalances have been arbitrarily defined as the positive output voltage being higher:

$$V_{imbalance}\,(\%) = \frac{V_{POS} - V_{AVG}}{V_{AVG}} = \frac{-\left(V_{NEG} - V_{AVG}\right)}{V_{AVG}} \tag{5.1}$$

where $V_{AVG} = \frac{V_{POS}+V_{NEG}}{2}$.

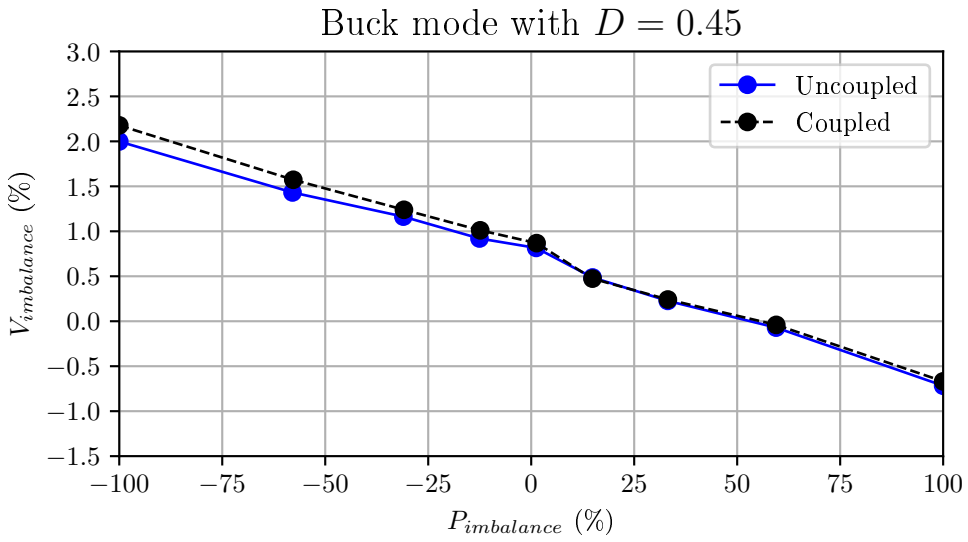
The load power imbalance has been similarly defined as:

$$P_{imbalance}\,(\%) = \frac{P_{POS} - P_{AVG}}{P_{AVG}} = \frac{-\left(P_{NEG} - P_{AVG}\right)}{P_{AVG}} \tag{5.2}$$

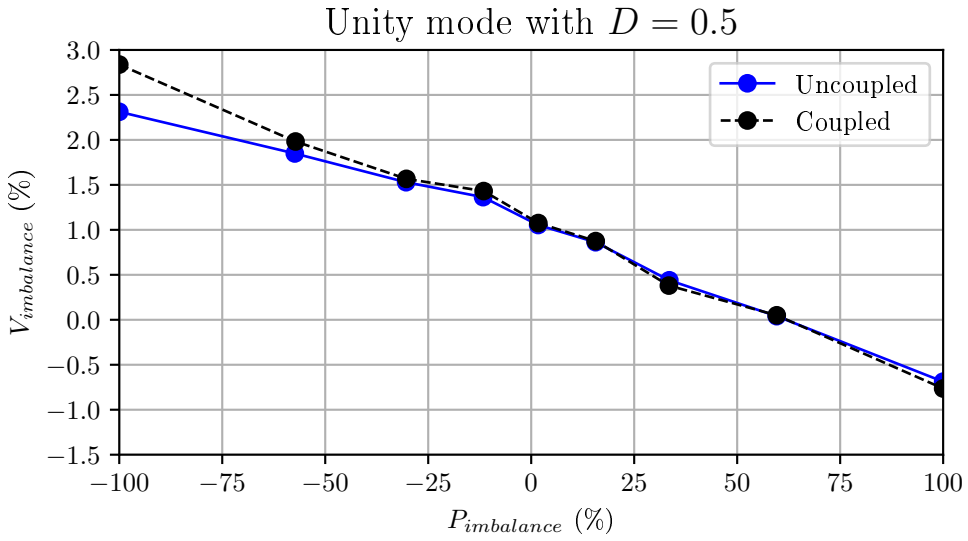
where $P_{AVG} = \frac{P_{POS}+P_{NEG}}{2}$.

There are several notable observations from this data:

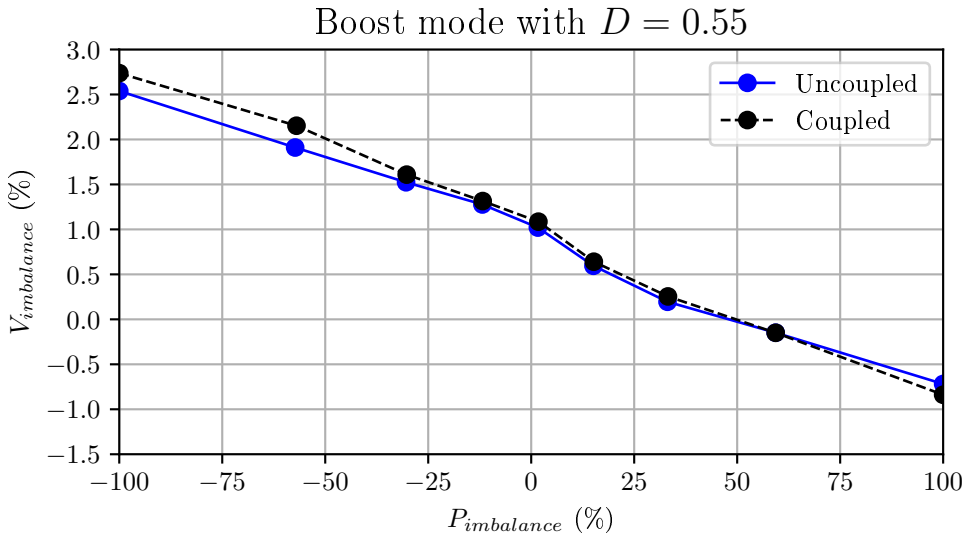
- *Performance:* The overall output voltage balance of the converter is exceptionally good, with the worst case voltage imbalance over all 54 experimental data points calculated to be 2.84%, and the average imbalance being just



(a) Experimental voltage imbalances with step-down operation ($D = 0.45$).

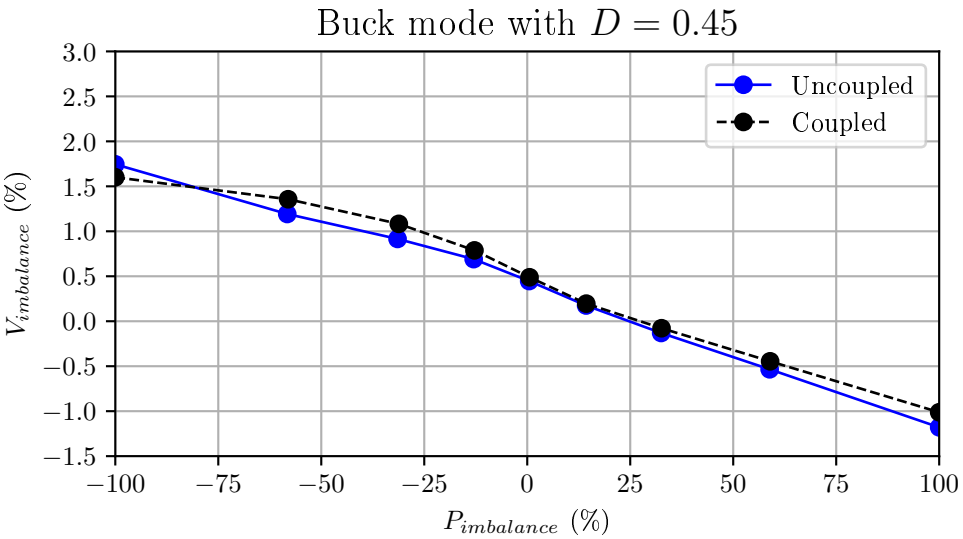


(b) Experimental voltage imbalances with unity gain operation ($D = 0.5$).

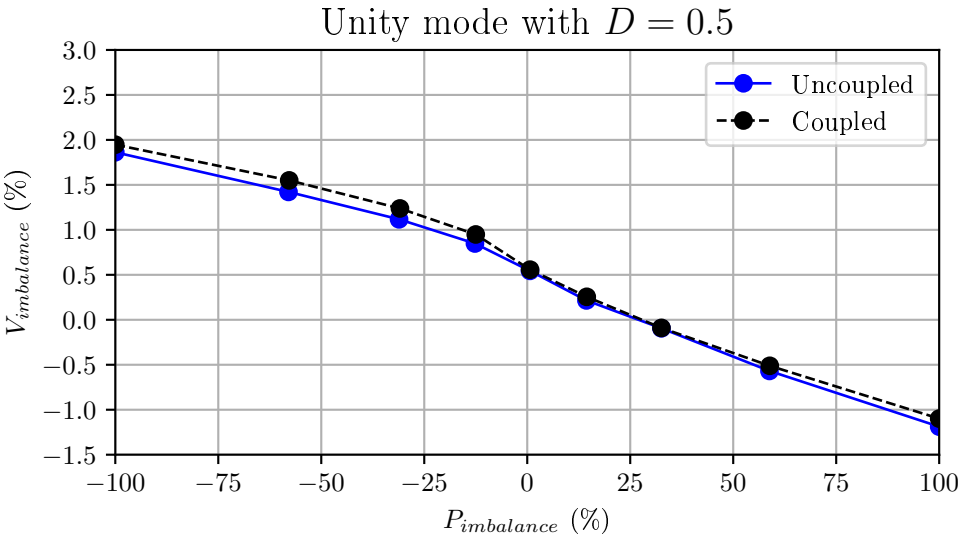


(c) Experimental voltage imbalances with step-up operation ($D = 0.55$).

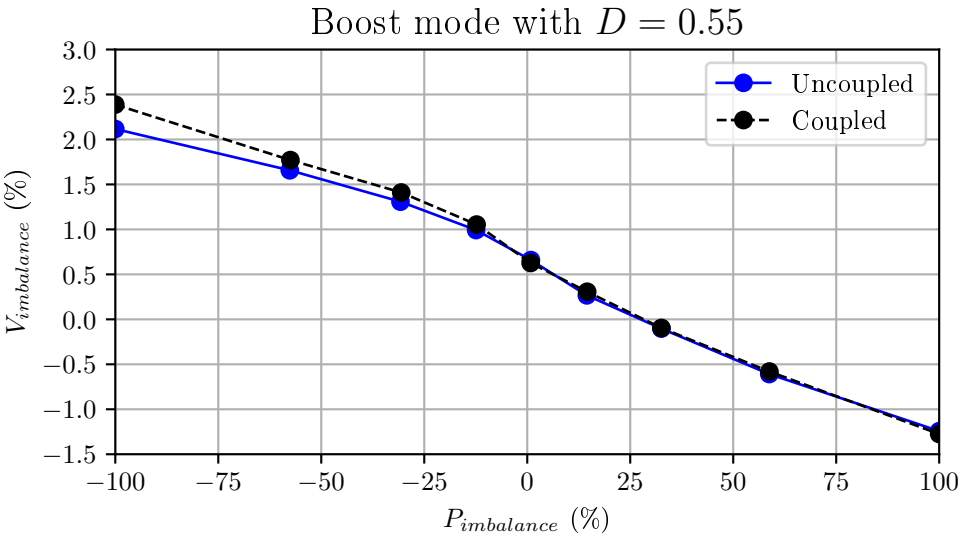
Figure 5.5: Experimental voltage imbalances as a function of power imbalance of the CCS and CI-CCS converters.



(a) Simulated voltage imbalances with step-down operation ($D = 0.45$).



(b) Simulated voltage imbalances with unity gain operation ($D = 0.5$).



(c) Simulated voltage imbalances with step-up operation ($D = 0.55$).

Figure 5.6: Simulated voltage imbalances as a function of power imbalance of the CCS and CI-CCS converters.

0.89%.

- *CCS vs. CI-CCS:* The CCS converter has slightly better voltage balance than the CI-CCS converter for all three voltage conversion ratios. The average output voltage imbalance of the CCS converter is 0.86% compared with 0.93% for the CI-CCS converter.

- *Voltage regulation:* The gradient of all six lines shows that the positive output voltage decreases relative to the negative output voltage as it is progressively loaded, as expected.

- *Unloaded operation:* One of the most interesting observations is that it is possible to operate both converters with either output completely unloaded - something which is not possible with the individual Cuk and SEPIC converters. The reason for this is that in the standard converters, the input inductor is continuously charged in every switch 'on' state, and this energy is forced towards the output in every switch 'off' state. If this energy is not drawn out of the converter, then it continuously builds in the capacitors until a component fails from overvoltage. In the CCS and CI-CCS converters, even if one output is completely unloaded, the energy is still able to flow out of the other output. This is critical for grid-connected applications as each output is completely de-loaded for 10 ms (half the period for a 50 Hz grid).

- *Balanced load:* When equal loads are connected to both the positive and negative outputs, a $\pm 1\%$ voltage imbalance exists for all three gain ratios (with the positive output voltage being higher). This was observed in earlier chapters, in Figure 3.16 and Figure 4.17.

- *Duty cycle variation:* The voltage imbalance is largely independent of the voltage gain ratio, however slightly better performance is obtained with step-down operation.

Simulations results have also been obtained over the same voltage change ratios and load imbalance range, and the results are presented in Figure 5.6a (step-down operation), Figure 5.6b (unity operation), and Figure 5.6c (step-up operation). These results are largely consistent with the results obtained experimentally.

Overall, these observations suggest that the CCS and CI-CCS converters are well-suited to feeding bipolar DC input inverters (such as the half bridge and T-type) in grid-connected applications. The next chapter investigates this pairing in detail to demonstrate the complete power flow from a DC PV input to an AC voltage output.

5.4 Chapter Conclusion

In this chapter, the CI-CCS converter's performance has been examined in several ways. Firstly, a PI-based current controller has been developed using the Ziegler-Nichols tuning method. The bandwidth of the converter and controller has been tested by applying a step change to the input current reference and measuring the converter's response time. Changes in the demanded input current of 2 A (corresponding to power increases of 400 W) have been tracked with no overshoot in under 4 ms.

Next, the efficiency of the CI-CCS converter was measured over a range of load powers. The sources of losses have been segmented into inductor copper losses, MOSFET conduction losses, diode conduction losses, and other losses (combining MOSFET switching losses, inductor core losses, and capacitor ESR losses). A peak efficiency of 92.3% was measured at a load power of 2029 W. The efficiency of the uncoupled CCS converter was also measured under the same range of conditions and the separate losses were again quantified. This comparison showed that the CI-CCS converter was marginally more efficient under all load powers tested.

Finally, the performance of the CCS and CI-CCS converters was analysed under unbalanced load conditions. The results showed that the output voltages were largely constant over variations in load between the outputs, though the positive (SEPIC) output voltage had a tendency to be slightly higher than the negative (Cuk) output voltage, with a voltage imbalance of $\pm 1\%$ when the loads were equally balanced. The average output voltage imbalance was measured to be $\pm 0.89\%$, and the worst output voltage imbalance observed was $\pm 2.84\%$ when the positive output was left completely unloaded. Performance under these conditions is important when the converter is used in a PV system, because bipolar input inverters draw power unequally from each output.

Chapter 6

AC Integration

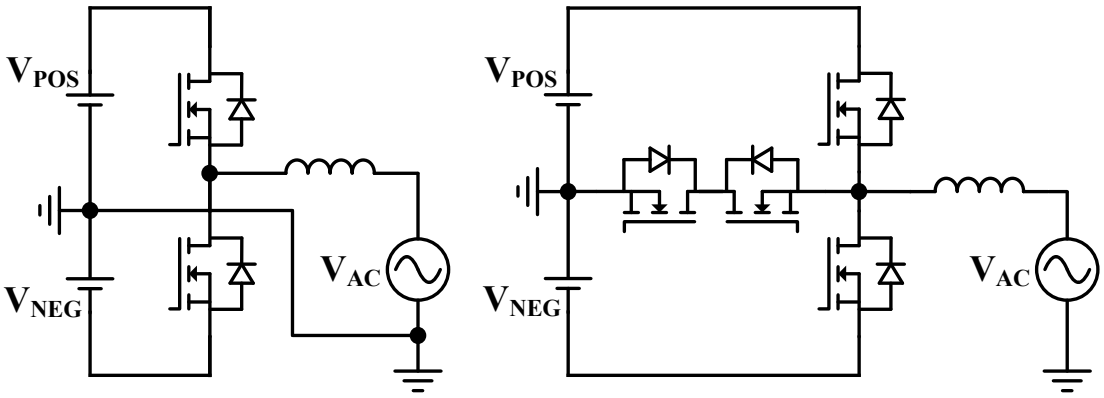
Previous chapters have examined the CI-CCS converter and explained why it is particularly well-suited to solar PV applications. This chapter provides a case study to demonstrate this assertion by implementing the CI-CCS converter in a PV system. Control strategies are discussed for grid-connected and stand-alone operation, and the DC bus and inverter component sizing are investigated. Simulation and experimental results are provided for the system, using an adaptable inverter that can test two topologies.

6.1 Inverter Selection

Inverters are an integral part of most PV domestic PV systems, and are required in grid-connected, power sharing, and stand-alone operational modes, which will be examined in Section 6.2. The application considered here is a standard domestic PV system, which typically feeds a grid with the following properties:

- *Single-phase:* This causes the instantaneous power flow to be time-varying (with the shape $P_{out}(t) = \widehat{v_{AC}}\widehat{i_{AC}}\sin^2(\omega t)$ for unity power factor operation), compared with a balanced three-phase system where the instantaneous power flow is constant. The PV array should produce a constant power, so storage must be present between the PV array and the grid, usually in the form of DC bus capacitors. This will be discussed in Section 6.3.

- *Grounded:* Three different earthing systems are commonly used in UK households: TT, TN-S, and TN-C-S (which is sometimes known as protective multiple earthing (PME)). All these earthing systems share the common characteristic that the low voltage feeder supplying the household is earthed



(a) Half bridge inverter topology. (b) T-type inverter topology.

Figure 6.1: Grounded bipolar DC input inverter topologies.

at the distribution transformer. This means that common mode voltages present in the household can cause leakage currents to flow to ground through parasitic capacitances present in the system.

Both of these properties influence the inverter topology used for a given system. In this thesis, one aim is to design a PV system with no leakage currents. As discussed in Section 2.2.5, leakage currents can be eliminated by introducing galvanic isolation (either high frequency or low frequency), by using DC decoupling inverters (e.g. HERIC, H5, H6), or by using inverters with a grounded DC input, with the latter method having numerous advantages. Examples of grounded DC input inverters include simple half bridge inverters, single-phase T-type inverters, and multilevel inverters (e.g. diode/neutral-point-clamped inverters, flying capacitor/capacitor-clamped inverters). Due to the power and voltage levels associated with domestic PV applications, multilevel converters are surplus to requirements, so the main topologies left to consider are the half bridge inverter and the single-phase T-type inverter. Both of these inverters were introduced in Section 2.4, and a brief comparison of these inverters for this application is provided here, outlining the trade-offs between component count, DC bus capacitance, and output filter size:

- *Number of devices:*
  - *Half bridge inverter:* The half bridge inverter (shown in Figure 6.1a) is one of the simplest of all inverter topologies. It only has two switching devices, each of which must be rated to withstand the combined DC bus voltage, and peak AC output current. The devices operate in a complementary fashion, so each must be capable of operation at the switching frequency.

  - *T-type inverter:* The T-type inverter adds a 'zero state' leg between the output and DC bus midpoint, as shown in Figure 6.1b, bringing the total switch count to four. These extra devices allow the T-type converter to produce a zero output voltage, in addition to the positive and negative output voltages. Two of these devices are needed in order to conduct and block in both directions. The additional switches have the same current rating, but only half the voltage rating. In unity power factor operation, these additional switches only need to be driven at the grid frequency.

- *Operation:*

  - *Half bridge inverter:* The half bridge inverter has two output states: $\pm V_{DC}$, and an average an output is produced by simply switching between these states.

  - *T-type inverter:* The T-type inverter is a three-level inverter, with output states of $-V_{DC}$, 0, $+V_{DC}$. In unity power factor operation, the zero state switches only operate at grid frequency (i.e. one switch remains 'on' in each grid half cycle). For non-unity power factor operation, one of the zero state switches must be driven at PWM frequency during the phase-shifted portions of the voltage/current cycles (i.e. when the AC voltage and current polarities differ) [62, 63, 94].

- *DC bus capacitance:* The half bridge inverter requires bigger DC bus capacitances than the T-type inverter (for the same allowable voltage ripple). This is due to the fact that in the T-type inverter, power flows into one DC input only (within a grid half cycle), whereas the complementary nature of the half bridge inverter's switches means that there is some power flow in the opposite DC bus too. This is discussed further in Section 6.3.

- *AC output filter:* The addition of the 0 V output state reduces the harmonics of the generated PWM output voltage, in turn reducing the size of the required output filter to obtain the same performance as a half bridge inverter (or get better performance for the same output filter size).

Regardless of which inverter is used, the overall control objectives are the same. The next section investigates this control structure for the integrated 'PV $\rightarrow$ DC-DC converter $\rightarrow$ Inverter $\rightarrow$ AC output' system.

6.2 Coordinated Control Structure

These inverters can be controlled to operate in grid-connected, power sharing, and stand-alone operational modes, and this section investigates the similarities and differences between these modes. The changes required are mostly in the control system, though the filter requirements may also change slightly, because stand-alone systems need to generate a sinusoidal voltage waveform whereas grid-connected systems are more concerned with the quality of the current injected into the grid to ensure they meet the necessary standards. The three distinct operation modes can be described as:

1. *Grid-connected:* The PV system is connected to an AC network which can be treated as an infinite bus, and the typical aim is to export excess PV generation to the electrical grid.

2. *Power sharing:* The PV system is one of several generation sources in a smaller AC network (i.e. the connection point cannot be treated as an infinite bus), and communications between the various sources cannot be assumed.

3. *Stand-alone:* The PV system is the sole AC generation source, and the devices using the generated PV power are designed to operate from standard AC mains. These applications could be off-grid homes which are permanently disconnected (e.g. in areas with no electrical infrastructure), or normally grid-connected homes that can maintain islanded operation during grid power outages.

In this thesis, the focus is on the first and third operational modes. Though the hardware proposed here is capable of operating in power sharing mode, this mode faces its own unique control challenges which are largely unrelated to the focus of this thesis. In such a system (for example, a microgrid), the inverter would be typically be operated in droop control mode (real power-frequency and reactive power-voltage) to ensure stable power sharing amongst distributed generation sources without centralised control and communications.

The control structure can be divided into two levels as shown in Figure 6.2, where the higher level controller sets the overall system objectives and the lower level controllers manage the converters to meet these objectives. From the perspective of the higher level controller, there are three sections to be managed - the PV system, the DC link voltages, and the AC output - and the control objectives for each depend on whether the system is operating in grid-connected or stand-alone

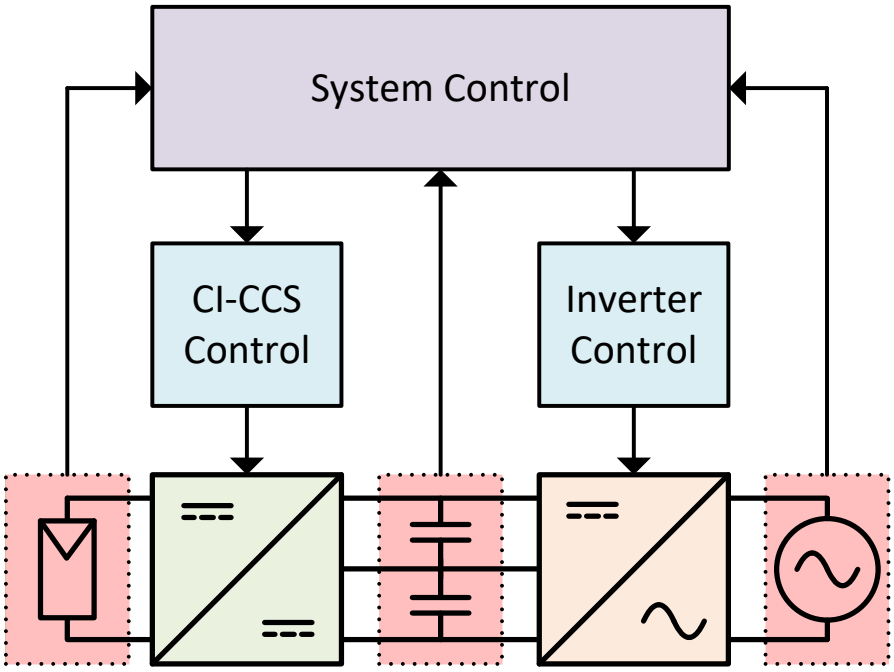


Figure 6.2: Coordinated control structure of the PV system.

mode.

6.2.1 Grid-Connected Mode

- *PV array:* The PV array should be operated at its MPP. The AC grid is treated as an infinite bus, so if the generated PV power is less than the total domestic load then power will be imported from the grid, and if the PV generation exceeds local demand then the difference will be exported to the grid. In both scenarios the PV array is fully utilised. MPPT can be performed by either the DC-DC converter or the inverter.

- *DC bus:* The DC bus needs to be regulated to ensure it stays within its limits. The lower voltage limit is set by the inverter requirements to produce the necessary AC voltage, and the upper voltage limit is set by the ratings of the components used in the converters. MPPT is usually performed by the DC-DC converter to extract as much power from the PV system and "push" it into the DC bus, and this bus is then regulated by the inverter by "pulling" sufficient power out to maintain the setpoint voltage. It is also possible for MPPT to be performed by the inverter, in which case the DC bus regulation is performed by the DC-DC converter. This has an advantage where the infinite bus may turn into a microgrid, since the DC-DC converter's control need not be changed [137].

- *AC output:* The inverter uses a closed-loop controller to act as a sinusoidal current source into the network. A phase-locked loop (PLL) is used to track the grid voltage so that the inverter can maintain the correct frequency and phase. Typically these systems operate with unity power factor (i.e. the current is in phase with the grid voltage), but reactive power control is also possible (for example, to provide voltage regulation, or perform power factor correction of downstream loads) provided the kVA rating of the inverter is sufficient.

6.2.2 Stand-Alone Mode

Often, a stand-alone PV system will be combined with an energy storage system (ESS), typically in the form of lead acid or lithium-ion batteries, to provide better utilisation of the panels and ensure that power can be provided through periods of low, or no, solar insolation. This storage is typically connected via a separated interfacing AC-DC converter, and thus may be treated like any other load in the system. Another connection option is to connect the storage to the main DC bus of the PV system via a DC-DC converter.

- *PV array:* Since there is no infinite bus present it is not possible to export excess PV power production into the grid. Thus, the PV system should be operated at a point that balances its generation with the total demand, and hence cannot be operated with an MPPT controller. There are three distinct scenarios depending on the total generation capacity, load, and presence of an ESS.
  - *PV generation exceeds demand, with ESS:* If an ESS is present (for example, battery banks are commonly used in off-grid applications), then it is treated as a variable load and the PV system may be fully utilised (up to the maximum charge rate of the ESS).
  - *PV generation exceeds demand, without ESS (or ESS fully charged):* The PV system will not be fully utilised, but will generate enough power to perfectly meet the total demand.
  - *Demand exceeds PV generation:* If the demand exceeds PV generation then an ESS is required to produce the difference in power. If the difference exceeds the capacity of the ESS, or no ESS is present, then the system cannot operate (unless loads are shed).
  - Note that the case where PV generation perfectly matches total demand

(excluding the ESS) has been excluded as this is almost impossible to occur due to continuously changes in generation and demand, so the system will be instead shift between the cases described above.

- *DC bus:* The DC bus needs to be regulated to ensure it stays within its limits. As in grid-connected mode, the lower limit is set by the inverter requirements to produce the necessary AC voltage, and the upper limit is set by the ratings of the components used in the converters. The DC bus regulation is performed by the DC-DC converter.

- *AC output:* The inverter has a closed-loop controller to act as a sinusoidal voltage source, and the power supplied depends on the current drawn by loads connected to the inverter. As current is drawn, power is "pulled" from the DC bus, causing the DC bus voltage to decrease. The DC-DC converter performs voltage regulation by moving the PV array's operating point to "push" the required amount of power into the DC bus to maintain its setpoint voltage.

It is also worth noting that grid-connected, power sharing, and stand-alone modes of operation have been considered as distinct, but in reality the same system may operate in different modes at different times (e.g. an upstream network fault turning an infinite bus into a microgrid, or a local grid fault forcing a house into islanded operation). The seamless transition between these operational modes is a challenging and ongoing area of research.

Only stand-alone operation will be considered for the rest of this chapter, as it requires a better filter, and so grid-connected mode can almost be considered as a subset of stand-alone operation, with some relatively simple control changes for grid synchronisation.

With the control system established, the next section continues with an investigation into the hardware - specifically, the bipolar DC bus design.

6.3 Bipolar DC Bus Capacitance

As discussed in Section 6.1, trade-offs exist between the half bridge inverter and the T-type inverter in terms of their component counts, DC bus capacitances, and output filter requirements. This section further investigates the differences between these converters in terms of the DC bus capacitances required, in order to inform the choice between these inverters.

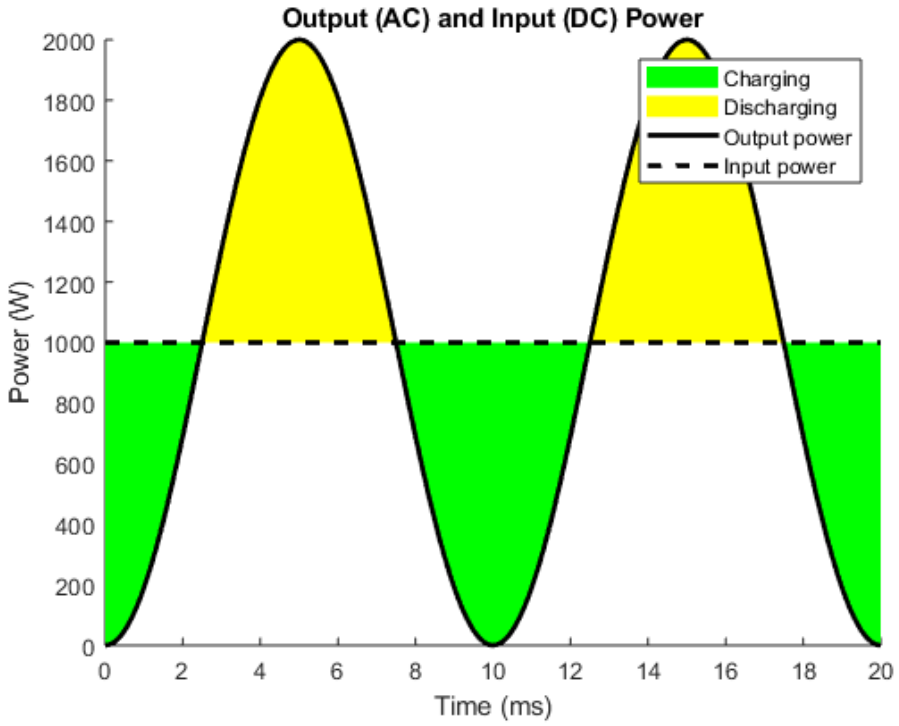


Figure 6.3: Output (AC) and input (DC) power of an ideal 1 kW PV system.

The DC bus capacitance requirements stem from the nature of the single-phase AC instantaneous power output (time-varying) compared with the nature of the PV power generated (constant over small time scales, and equal to the average AC output power). This necessitates some form of energy storage, as shown in Figure 6.3. This challenge cannot be avoided as it is inherent to the basic physics of the system, regardless of DC-DC or inverter topology selection. This energy storage is short-term, with a charge/discharge cycle time of 10 ms for a 50 Hz AC output, and is typically provided by bulk capacitors connected to the DC bus between the DC-DC converter and inverter.

The energy stored in these capacitors and their voltages are related by $Q = \frac{1}{2}CV^2$, so the capacitor voltages will fluctuate as they are charged and discharged. Based on the time-varying power flows, maximum allowable voltage, and the minimum required voltage, it is possible to estimate the DC bus capacitances required [138].

The AC output power for a unity power factor supply is given by:

$$P_{out}(t) = \widehat{v_{AC}}\widehat{i_{AC}}\sin^2(\omega t) \tag{6.1}$$

$$P_{out}(t) = \widehat{P_{out}}\sin^2(\omega t) \tag{6.2}$$

where $\widehat{v_g}$ and $\widehat{i_g}$ are the peak grid voltage and currents respectively, and $\widehat{P_{out}}$ is the product of these terms (i.e. the peak instantaneous AC power output). It should

be noted that this instantaneous AC output power is the same for both the half bridge and T-type inverters, however the way it is drawn from the DC links by each inverter is different, and is discussed later in this section.

The average output power (and hence the input power, assuming lossless converters) is given by:

$$\overline{P_{out}} = P_{in} = \frac{1}{\pi}\int_{\omega t=0}^{\omega t=\pi} \widehat{P_{out}} \sin^2(\omega t)\, dt \tag{6.3}$$

$$P_{in} = \frac{\widehat{P_{out}}}{2} \tag{6.4}$$

In Figure 6.3, the green and yellow areas are the same size, and represent the energy ripple in the storage for charging and discharging respectively. The magnitude of this energy ripple can be determined by calculating the size of the yellow area:

$$\Delta E = \int \left[P_{out}(t) - P_{in}(t)\right] dt \tag{6.5}$$

$$= \int_{\omega t=\frac{\pi}{4}}^{\omega t=\frac{3\pi}{4}} \left[\widehat{P_{out}} \sin^2(\omega t) - \frac{\widehat{P_{out}}}{2}\right] dt \tag{6.6}$$

$$\Delta E = \frac{\widehat{P_{out}}}{2\omega} \tag{6.7}$$

This energy ripple is stored in the capacitor, so using $Q = \frac{1}{2}CV^2$ the capacitance required can be calculated as:

$$\Delta E = \frac{\widehat{P_{out}}}{2\omega} = \frac{1}{2}C\left(V_{C_{max}}^2 - V_{C_{min}}^2\right) \tag{6.8}$$

$$C = \frac{2\overline{P_{out}}}{\omega\left(V_{C_{max}}^2 - V_{C_{min}}^2\right)} \tag{6.9}$$

In order to minimise these voltage fluctuations, a stiff DC bus can be created with very large capacitances, though this comes at a higher cost and size. By picking the smallest capacitance value that satisfies the constraints, the cost and size of the system can be reduced, though this comes at the penalty of larger voltage fluctuations on the DC bus.

These voltage fluctuations do not present a problem if the inverter is controlled to account for them, by measuring the DC bus voltages and adjusting the inverter's modulation accordingly. There are two constraints on the voltage fluctuations:

- *Maximum voltage:* The largest DC bus capacitor voltage needs to be within the voltage ratings of all devices. The DC bus capacitors typically have quite

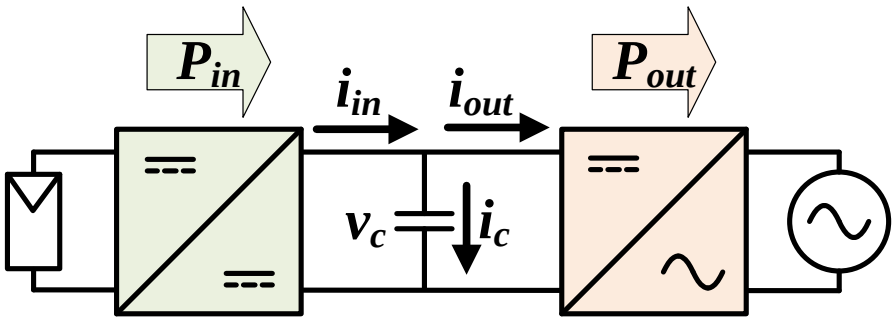


Figure 6.4: Power flows between DC-DC converter and inverter with a single DC bus.

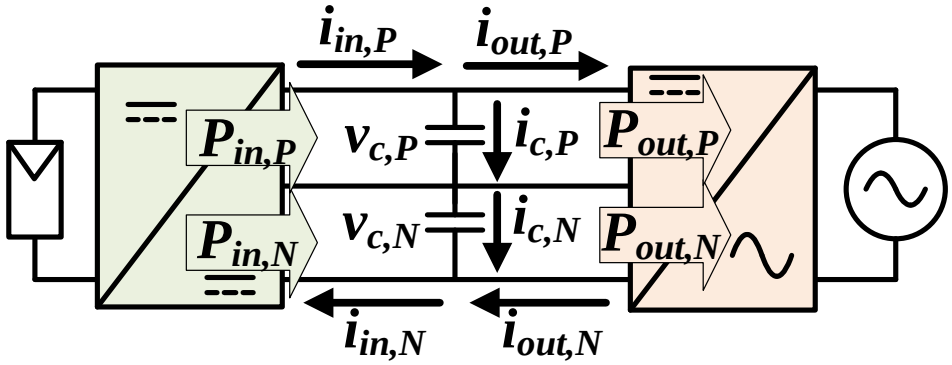


Figure 6.5: Power flows between DC-DC converter and inverter with a bipolar DC bus.

high capacitances and so electrolytic capacitors are usually used. These are commonly rated at 500 V, so the maximum designed voltage should be 450 V (10% below the rated voltage).

- *Minimum voltage:* The DC bus voltage must always exceed the instantaneous grid voltage (plus a margin for the voltage drop across the output filter) in order for the linear modulation of the inverter to function correctly. The maximum required output voltage can be conservatively approximated as $\widehat{v_g} + 10\% = 230\sqrt{2} + 10\% \approx 360\,V$, so the bus voltage should at least match this.

Thus, the approximate required bulk capacitance per kW can be calculated as:

$$C_B = \frac{2 \times 1000}{2\pi \times 50 \times (450^2 - 360^2)} \tag{6.10}$$

$$C_{B_{min}} \approx 87\,\mu F \text{ per kW} \tag{6.11}$$

This is the capacitance that would be required for one capacitor in a single DC bus, as shown in Figure 6.4 (for example, a boost converter feeding a full bridge inverter). Here however, the storage is formed with two capacitors across a bipolar

DC bus connecting the CI-CCS converter to the half bridge/T-type inverter, as shown in Figure 6.5. Thus, this principle of determining power flows into and out of the DC link should be provided for each DC bus.

In fact, the power flows from the bipolar DC bus to a T-type converter are the same as the power flows for a single DC bus to full bridge inverter, however the power is drawn from each of the positive and negative DC links in alternating grid half cycles. Similarly, the power supplied by the CI-CCS inverter can be approximated as flowing into the same DC links in the corresponding grid half cycles. Thus, the capacitance calculated previously for a single DC bus is the same capacitance required in each half of a bipolar DC bus. The shape of the power drawn by the half bridge inverter is slightly different due to the converter's operation, so the DC bus capacitance should be increased slightly.

It is possible to more accurately determine the minimum capacitance required by improving the modelling accuracy of these DC link power flows and the maximum and minimum voltage requirements. This is somewhat tangential to the focus of this thesis so the approximations provided thus far are adequate, and only a summary of this process is provided here. The time-varying DC bus capacitor voltages can be described analytically as a function of $P_{in}(t)$ (the power flowing from the DC-DC converter to each DC bus) and $P_{out}(t)$ (the power flowing from each DC bus to the inverter) - as shown in Figure 6.4 and Figure 6.5 - with Equation 6.17:

$$i_c(t) = C\frac{dv_c(t)}{dt} \tag{6.12}$$

$$i_{in}(t) - i_{out}(t) = C\frac{dv_c(t)}{dt} \tag{6.13}$$

$$\frac{P_{in}(t)}{v_c(t)} - \frac{P_{out}(t)}{v_c(t)} = C\frac{dv_c(t)}{dt} \tag{6.14}$$

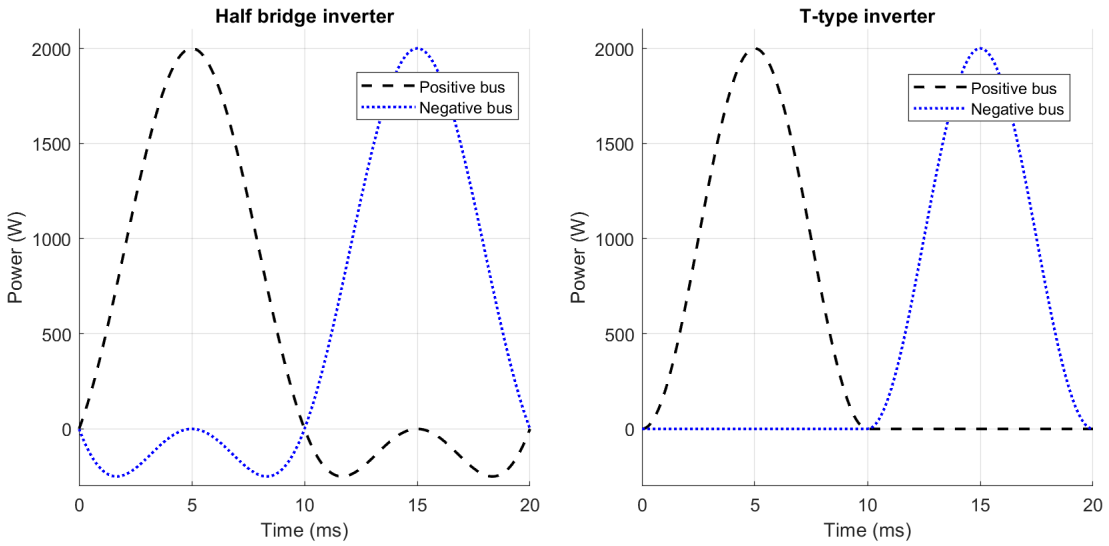
$$\int_0^t v_c(t)\,dv_c = \frac{1}{C}\int_0^t \left(P_{in}(t) - P_{out}(t)\right)dt \tag{6.15}$$

$$\frac{1}{2}\left(v_c^2(t) - v_c^2(0)\right) = \frac{1}{C}\int_0^t \left(P_{in}(t) - P_{out}(t)\right)dt \tag{6.16}$$

$$v_c(t) = \sqrt{\frac{2}{C}\int_0^t \left(P_{in}(t) - P_{out}(t)\right)dt + v_c^2(0)} \tag{6.17}$$

The $\int_0^t P_{out}(t)$ can be determined by understanding the power flowing out of the the bipolar DC bus for the:

- *Half bridge inverter:* $P_{out}(t) = \overline{P_{out}}\left(1 + \sin(\omega t)\right)\sin(\omega t)$, with the sine



(a) Power out of DC links for half bridge inverter. (b) Power out of DC links for T-type inverter.

Figure 6.6: Power out of DC links for T-type and half bridge inverters.

terms replaced with their negative values for the negative DC bus, as shown in Figure 6.6a. The negative portion of the power flows represent power flowing from the inverter to the DC bus, causing a rise in that DC bus capacitor voltage, and hence an increase in the DC bus voltage ripple.

- *T-type inverter:* $P_{out}(t) = 2\overline{P_{out}}\sin^2(\omega t)$ for each of the positive and negative DC links in their respective grid half cycles, as shown in Figure 6.6b. This is the model implied with the approximation made in determining the bulk capacitance previously.

Next, $\int_0^t P_{in}(t)$ can be determined with knowledge of the input power, which can be modelled in steps of increasing accuracy (albeit with increasing complexity):

1. Assume the power output of both CI-CCS converter terminals to be constant over time, each equal to half the PV array's power.

2. Assume the full power output of the CI-CCS converter alternates between each terminal during the grid's positive and negative half cycles. This is the model implied with the approximation made in determining the bulk capacitance previously.

3. Assume the power output of each CI-CCS converter terminal rises at the same rate as the power drawn from the DC bus until it reaches the full PV array's power. It then maintains this limit until the power drawn from the other DC bus starts to increase, at which point it decreases back to zero.

4. Model the CI-CCS converter's power output based on simulation results.

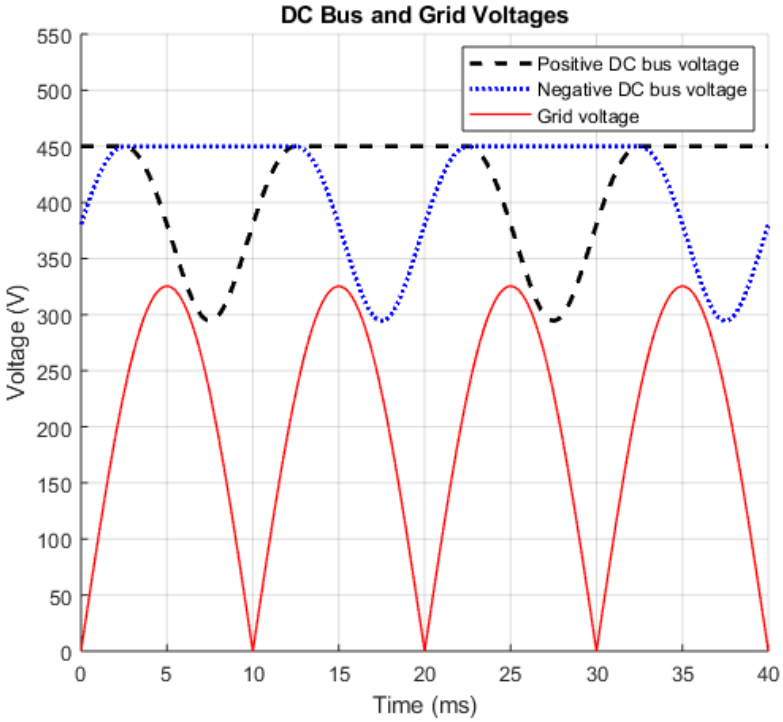


Figure 6.7: Demonstration of how the DC bus voltages can drop below the peak grid voltage.

Using Equation 6.17 and the $P_{in}(t)$ and $P_{out}(t)$ models above, more accurate expressions of the capacitor voltage can be determined. From this, the maximum and minimum values can be calculated, and the limits determined previously can be used to calculate the capacitance required.

In fact, this minimum required capacitance can be further reduced by considering the minimum DC link voltage requirement. Previously, it was stated that the DC link voltage should always be greater than the peak grid voltage (plus the voltage drop across the output filter) if linear modulation is applied. In reality, this requirement is sufficient but not necessary, as the DC link voltage only needs to be greater than the *instantaneous* grid voltage (plus the voltage drop across the output filter) [139]. This is illustrated in Figure 6.7, where the DC bus voltage may in fact drop below the grid's peak. This increase in the DC bus voltage utilisation allows for a reduction in the required capacitance, though care needs to be taken as the relative position of the DC bus voltage valleys and the grid voltage peaks change with power factor. Once again, minimising the size of the DC bus bulk capacitance is not the objective of this thesis, so it is not pursued further here.

Table 6.1: Design specifications for the inverter.

AC output power	1 kW
AC output voltage	110 V_{ac} to 230 V_{ac}
AC output frequency	50 Hz to 60 Hz
Input voltage range	±360 V to ±450 V

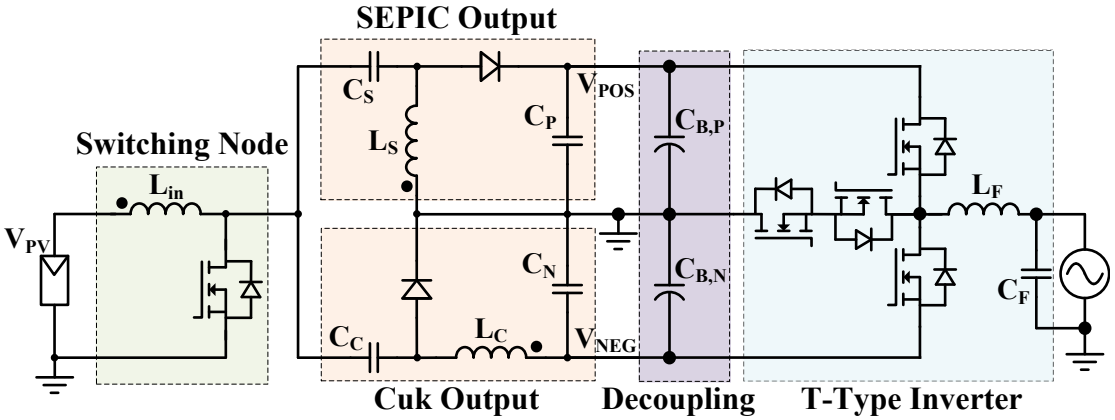


Figure 6.8: Combined CI-CCS and T-type inverter.

6.4 Combined Half Bridge/T-Type Inverter Design

A T-type inverter is designed with the specifications given in Table 6.1. The AC output power rating comes from Section 3.2.2, and the AC output voltage and frequency correspond to distribution network standards commonly used around the world. The minimum input voltage is based on the peak grid voltage with 10% margin, and the maximum input voltage is set to provide a sufficient margin for capacitors rated at 500 V. The full topology (CI-CCS and T-type inverter) is shown in Figure 6.8, and by leaving the 'zero leg' switches of the T-type inverter open and modifying the switching strategy, the same converter can be operated as a half bridge inverter, as shown in Figure 6.9.

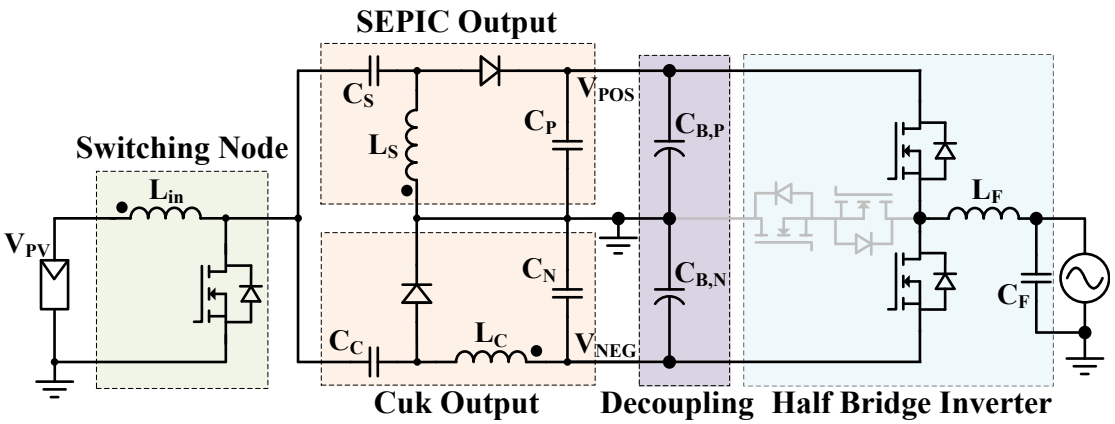


Figure 6.9: Combined CI-CCS and half bridge inverter.

Table 6.2: Passive component values for the inverter.

DC bus bulk capacitance	
C_{B_P}	100 μF
C_{B_N}	100 μF

Output filter	
L_F	330 μH
C_F	1 μF

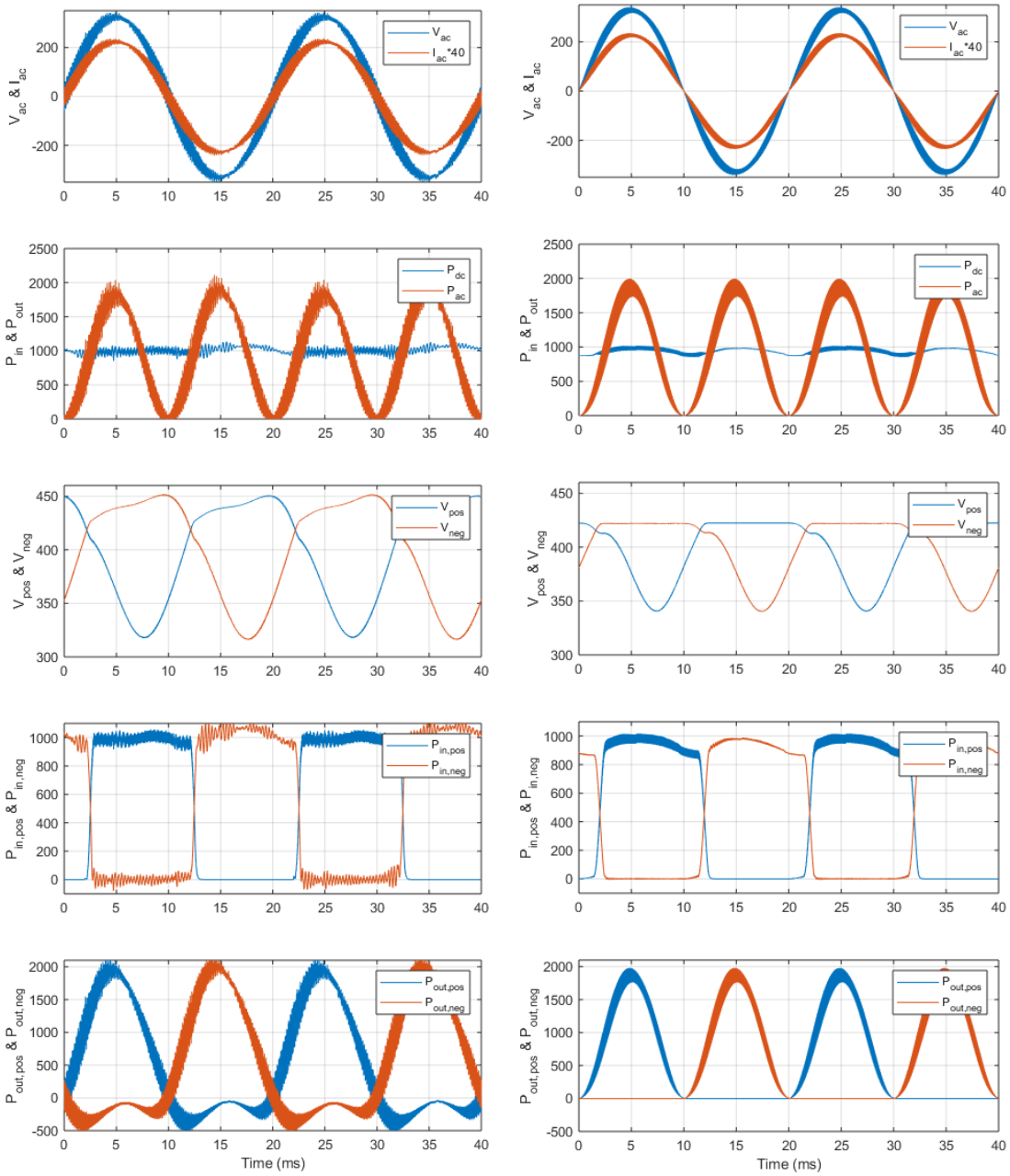
Bulk storage capacitors (C_{B_P} and C_{B_N}) are used on the DC bus between the CI-CCS converter and the inverter. The value of these capacitances listed in Table 6.2 are based on the values derived in Section 6.3, with some margin added.

A purely inductive output filter works well for the output filter in grid-connected applications, but makes closed-loop voltage control challenging in stand-alone applications. An LCL filter provides very good attenuation of the switching frequency ripple, however resonance needs to be managed. Thus, an LC output filter is selected here as it provides a straightforward method of producing a sinusoidal voltage output. Selecting the switching frequency is a trade-off between switching losses and output filter size. Here, a 20 kHz switching frequency has been selected as an appropriate balance between these factors. The grid filter should have a cut-off frequency at approximately half of the switching frequency. A cut-off frequency of 8.7 kHz can be achieved with the standard passive sizes listed in Table 6.2.

6.5 Simulation Results

Simulations results are provided for both the half bridge and T-type inverters, to show the difference in the DC bus voltage fluctuations and the AC output ripple. The results have been provided with a 230 V_{rms} output, and a 52.9 Ω load (1 kW).

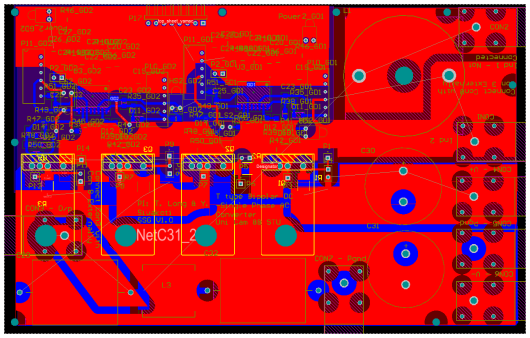
Comparing the DC bus voltage ripple for the half bridge (Figure 6.10a) and T-type (Figure 6.10b) inverters, it can be seen that the DC bus voltage fluctuations are smaller for the T-type than the half bridge inverter. This is due to the portions of negative instantaneous power flow (from the inverter to the DC bus) exhibited in the half bridge inverter. Similarly, the current ripple is smaller for the T-type inverter due to the extra zero voltage output state. The importance placed on the DC bus voltage stability and output current ripple depends on the system designer, though it is unlikely that increased cost and complexity of the T-type inverter (due to the extra switches) justifies the marginal benefits it provides in domestic PV applications.



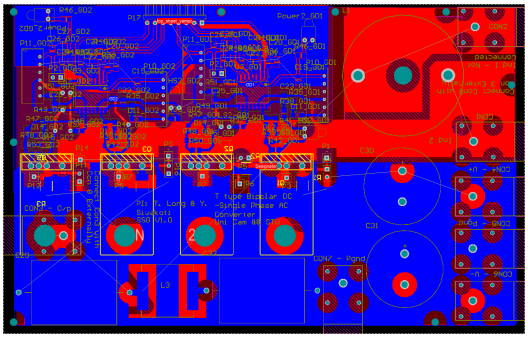
(a) Half bridge inverter waveforms.

(b) T-type inverter waveforms.

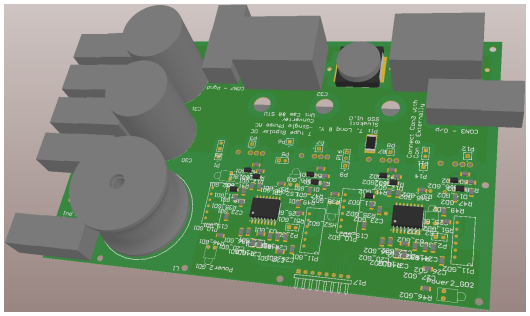
Figure 6.10: Simulated waveforms of the half bridge and T-type inverters.



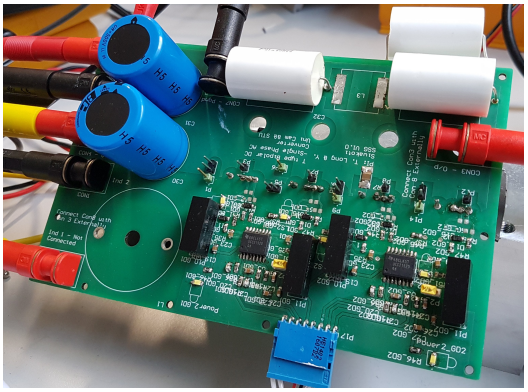
(a) Top layer.



(b) Bottom layer.



(c) 3D PCB model.



(d) Photo of developed PCB.

Figure 6.11: Combined half bridge/T-type inverter.

6.6 Experimental Design and Results

A T-type inverter (which can be used as a half bridge inverter if the 'zero state' switches are left open) is designed with the passive component sizes listed in Table 6.2. SiC MOSFETs have been used for the four switching devices to maintain consistency with the CI-CCS converter to simplify the design process. The developed PCB is shown in Figure 6.11.

With this prototype, experiments have been carried out in stand-alone operation with a DC input voltage of 100 V, an AC output voltage of 110 V_{rms}, and a 60 Ω resistive load connected to the AC output. This reduced voltage was chosen due to a lack of availability of loads with an appropriate resistance and power rating.

Figure 6.12 shows the experimental waveforms obtained with the half bridge inverter and Figure 6.13 shows the same waveforms obtained with the T-type in-

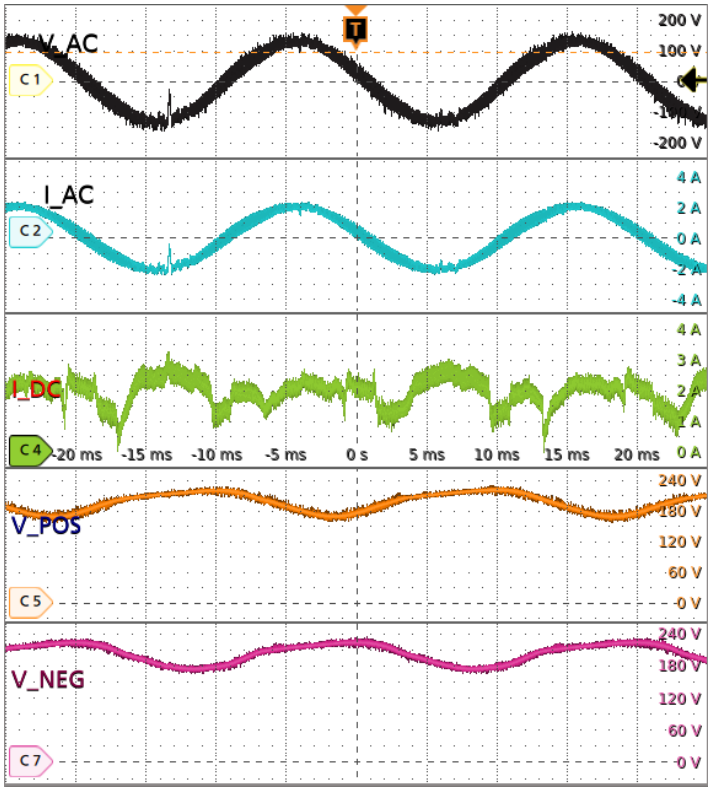


Figure 6.12: Experimental half bridge inverter waveforms (fed from the CI-CCS converter): : v_{AC}, i_{AC}, $i_{L_{in}}$, v_{POS}, v_{NEG}.

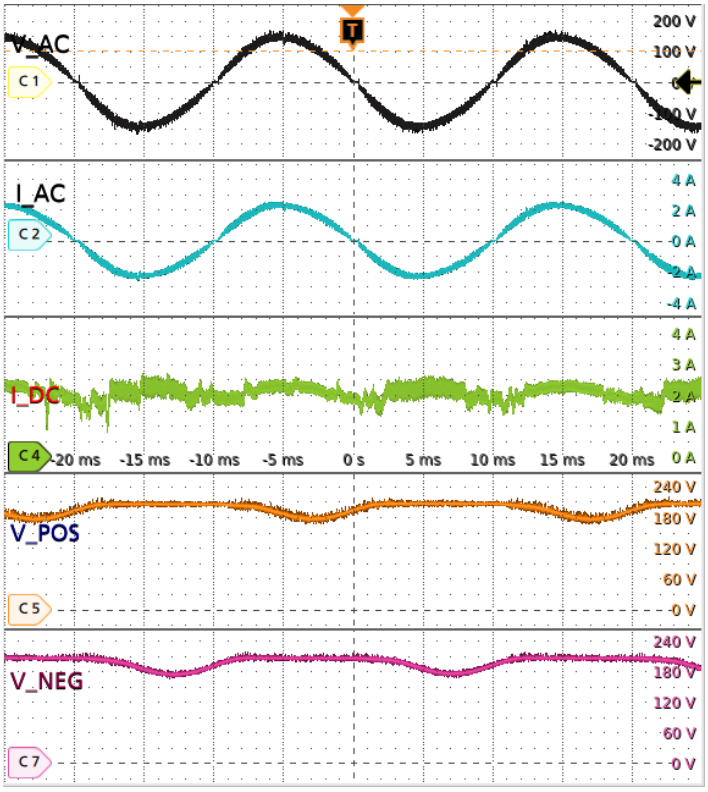


Figure 6.13: Experimental T-type inverter waveforms (fed from the CI-CCS converter): : v_{AC}, i_{AC}, $i_{L_{in}}$, v_{POS}, v_{NEG}.

verter. It can be seen that shape of the DC bus voltages match closely with the simulation results, though the input current is a little noisier. The primary reason for this is additional sensing noise (mainly due to the ringing caused by parasitics within the inductors) which negatively impacts the controller's performance. The output AC voltage and current waveforms are noticeably 'cleaner' for the T-type inverter, due to the reduced harmonics resulting from the extra 0 V output state. It can also be seen that the DC bus voltage ripple is smaller for the T-type inverter due to the lack of reverse power flow shown in Figure 6.6. The importance placed on these different performance characteristics is dependent on the specific application, though it anticipated that for domestic PV applications, the two additional switches required by the T-type inverter would not justify these benefits, and so the half bridge inverter would likely be selected.

6.7 Chapter Conclusion

This chapter provided an examination of the CI-CCS converter's application in a typical PV system. Grounded bipolar DC input inverters were explored because they pair well with the proposed converter for domestic (single-phase) PV applications. Using the CI-CCS converter with the half bridge or T-type inverter allows the leakage current issue to be fundamentally addressed, while providing a galvanic path from the PV array to the grid's earth connection point.

Different control strategies have been provided for both grid-connected and stand-alone applications, outlining the responsibilities of the DC-DC converter and inverter in each mode. The chapter proceeded with a focus on stand-alone applications due to them being largely a superset of grid-connected applications.

The chapter then continued with an investigation into a key point of difference between the half bridge/T-type inverter and other commonly used inverters: the bipolar DC bus structure. The power flows in and out of the DC bus were studied and their impacts on the DC bus voltages quantified. With this information, an expression was derived to size the DC bus bulk capacitances.

Next, an adaptable inverter was designed that can function as either a half bridge inverter or a T-type inverter. Simulation and experimental results were obtained which demonstrate the performance of both inverter topologies. The DC bus voltage fluctuations and AC output ripple were observed to be larger for the half bridge than the T-type inverter, as expected. Even with these disadvantages, it is anticipated that the half bridge inverter would be better suited to most

applications due to the reduced component count and converter complexity.

Chapter 7

Conclusions and Future Work

This final chapter provides a summary of the work done in this thesis, with a particular focus on its key contributions and how they address the problems outlined in the introductory chapter. The most significant results and their implications are discussed, alongside limitations of the work undertaken. The chapter concludes with suggestions for future work to extend this research and address its limitations.

7.1 Summary of Work Done

In this thesis, a new DC-DC converter has been proposed. This converter, known as the CI-CCS converter, is based on the Cuk and SEPIC converter. It has several properties that make it well suited for interfacing with certain types of inverter topologies, particularly in domestic PV applications, which have been the focus of this thesis:

- Its bipolar output structure means that when the CI-CCS converter is used in conjunction with a bipolar DC input inverter, the PV array does not have common mode voltages present on it. This eliminates the leakage currents that flow through parasitic capacitances in most domestic PV systems.
- The wide voltage conversion ratio, and step-up and step-down capabilities mean that the proposed converter can regulate a wide range of PV systems at varying panel conditions.
- The continuous input current with very low ripple ensures that the PV array operates close to its MPP, maximising its utilisation. The negative effects of input current ripple on the average output power of PV systems are shown in

order to demonstrate why a DC-DC converter with low input current ripple is critical to improve PV system utilisation.

In Chapter 3, the operation of the CCS converter was examined in CCM to understand the energy transfer pathways from the input to the output terminals in both the switch 'on' and switch 'off' states.

A range of equations were derived to size the converter's seven passive components based on the desired performance requirements. Additionally, equations were also derived to determine how the ten components (one switch, two diodes, three inductors, four capacitors) should be rated - both in terms of peak currents and peak voltages.

Following this, simulation results were obtained with these parameters to demonstrate the operation of the converter. The accuracy of the 27 component sizing expressions were also validated, with simulation results agreeing closely with the analytical predictions. On average, the passive sizing expressions agree to within $\pm 1.56\%$, the peak voltage expressions agree to within 0.88%, and the peak current expressions agree to within 0.66%. This gives confidence that the analytical expressions can be used to guide component selection in the design process, and the resulting converter will largely satisfy the performance specifications.

A full account of the experimental design process was then presented, explaining the choice of semiconductor power devices, passive device technologies, and the PCB design process for several PCBs used in this prototype, including the power board, the gate driver, the controller and optical fibre transmitter, and isolated sensing boards. A 4 kW converter was built using SiC power devices, nanocrystalline powder core inductors, and film capacitors.

Experimental results obtained with this prototype demonstrate strong consistency with the simulation results. This major result proves that the theoretical equations describe the experimental system with a high degree of accuracy, meaning that the proposed converter is able to be designed quickly and easily based on design specifications alone.

In Chapter 4, coupling between the CCS converter's three inductors was applied with the aim of reducing the switching frequency ripple present in the input current. This modified converter is known as the CI-CCS converter. Starting with a generalised inductance matrix for a system of three inductors, an expression was derived for the equivalent input inductance of the proposed converter as a function of coupling factors. The impacts this has on the input current ripple was shown, initially as a function of all three coupling factors. Given these results,

simplifications were applied to produce an expression for the coupling factors as a function of the inductances, which yields a theoretically infinite input inductance.

Once again, these analytical derivations were tested in simulations, and once again, the results obtained are highly consistent. The differences are explained by the approximations made in the theoretical derivations, but are sufficiently small that the theoretical expressions can be confidently relied upon.

Several optimisation techniques were reviewed, and Bayesian optimisation was selected as the most applicable technique here. Potential objectives were explained, and example optimisations were provided. Three of these optimisations were undertaken:

1. Minimising the input current ripple with no constraints on coupling factors, with simulation results showing input current ripple reductions of 96.9%
2. Minimising the input current ripple with $k_1 = k_2$, and k_3 unconstrained, with simulation results showing input current ripple reductions of 96.6%
3. Minimising the input current ripple with $k_1 = k_2$, and $k_3 = 0$, with simulation results showing input current ripple reductions of 88.3%.

Following these simulations, a method of developing these inductors using only toroidal cores was presented. This allows the merits of the ripple steering concept to be proven experimentally with relatively simple inductor designs. These experimental results demonstrated a reduction the input current ripple of 93%. The waveforms measured closely match the simulation waveforms, and again demonstrate the reliability of the analytically derived expressions. With their validity confirmed, the designer can be confident in using these expressions as a basis for further design and optimisation.

In Chapter 5, a closed-loop current controller was implemented to regulate the input current. This was achieved with a PI controller, whose parameters are determined using the Ziegler-Nichols tuning method. The performance of this controller was examined, and it was shown to track a 400 W step-change in current demand (from 1 A to 3 A at 200 V) in under 4 ms. This bandwidth is far higher than what is required by the MPPT controller, which would typically have dynamics in the order of seconds.

Following this, the converter's efficiency was measured over a range of power outputs, with a peak efficiency of 92.33% achieved at an output power of 2029 W (51% of the converter's rated power). Voltage and current measurements taken throughout the circuit were used to quantify several of the loss sources, with the

biggest contributor being the MOSFET's switching loss.

Next, the impact of load imbalance on the converter's bipolar outputs was examined, showing that it still provides tight regulation of both outputs (maximum imbalance of $\pm 2.84\%$) even under large imbalances (up to 100%). Due to the unique connection of its output structures, the proposed converter is able to have either of its terminals completely unloaded, something that would cause component failure due to overvoltage in a standard Cuk or SEPIC converter. Imbalance analysis is critical for systems with a bipolar input inverter (such as the half bridge and T-type) because the loads placed on each output are inherently unbalanced and time-varying.

In Chapter 6, the proposed converter was implemented in a wider system to show how its unique characteristics make it particularly useful in solar PV applications. Two grid-interface inverters were introduced, both of which are suitable for domestic single-phase applications. These inverters both have a grounded bipolar DC input, which eliminates common mode voltages, and hence leakage currents, when paired with the CI-CCS converter. A comparison of these converters was made, showing that the half bridge inverter requires larger DC bus capacitances and output filter compared with the T-type inverter, though has half the number of switching devices. With this trade-off, it is expected that the half bridge inverter would generally be better suited to domestic solar PV applications than the T-type inverter.

The coordinated control structure of both the CI-CCS converter and inverter was presented for both grid-connected and stand-alone modes of operation. It was shown that each converter's responsibilities differ in these modes, from managing the PV array (with MPPT or otherwise), regulating the DC bus, and providing a current-controlled or voltage-controlled AC output.

Next, the system's passive components were sized, beginning with an analytical exploration of the power flows through the bipolar DC bus in order to determine appropriate capacitance requirements. An inverter control strategy was implemented which permits weak DC bus voltages (with small capacitances) to be used, by measuring the voltages and adjusting the modulation appropriately. The inverter's switching frequency and output filter sizes were also determined, followed by simulation results of the designed converter. A hardware prototype was developed which allows both half bridge and T-type inverters to be tested.

These final results demonstrated that a complete PV system - from the solar PV panels to the AC output - can be constructed with just three switching devices,

and this system has no common mode voltages or leakage currents, a wide input regulation range, and gives high PV utilisation due to low PV current ripple.

7.2 Key Contributions and Implications

A novel DC-DC converter, known as the CI-CCS has been proposed, which has the following properties:

- It has a bipolar output structure with a grounded midpoint
- It is able to perform both voltage step-up and step-down
- It has a high gain
- It has a continuous input current
- It has extremely low input current ripple
- It operates with only one MOSFET, which has its source terminal grounded, allowing for a relatively simple gate driver to be used.

The converter has been analysed in several ways, and consistent results have been obtained:

- *Analytically:* With several expressions derived theoretically to understand and design the converter.
- *Simulations:* The operation and performance of the CCS and CI-CCS converter have been studied in two simulation platforms.
- *Experimentally:* Prototypes have been developed of both the CCS and CI-CCS converter to demonstrate the performance of the converters.

It has been observed that the results attained through all three of these methods have little deviation between them. The closeness of these outcomes means that costly simulation and experimental development time can be saved, and the quality can be improved, because the analytical expressions produce accurate component requirements. For more involved designs, simulations may still be required, however the analytical expressions can guide optimisation processes by considerably reducing the 'space' of all parameters that need to be considered.

The converter designed has the following performance metrics:

- *Input current ripple reduction:* 40% for the CCS converter and less than 5% for the CI-CCS converter
- *Voltage gain range with limited duty cycle range:* A wide gain range (per output) of 0.82 to 1.22 obtained with a narrow duty cycle range of 0.45 to 0.55
- *Efficiency:* The measured efficiency ranges from 90.2% to 92.3% over an output power range of 525 W to 2029 W
- *Current control:* The converter can track changes in power at rate of 100 W per ms
- *Voltage balance:* Power imbalances (even up to 100%) at the converter's outputs result in voltage imbalances of less than 3%.

The unique properties of the converter, the consistency of results obtained, and the performance metrics all demonstrate that the converter has a promising future in a range of applications and merits further research.

7.3 Limitations of Work Undertaken

This work focused on the development of a new type of DC-DC converter, which has a combination of properties that make it unique compared to existing DC-DC converter topologies. The limitations of the work undertaken can be broadly considered in three categories:

- *Application:* In this thesis, the proposed converter is only considered for one application: domestic solar PV. It is anticipated that the CI-CCS converter would also be well suited to a range of other applications.
- *Design:* As this thesis is focused on exploring the novelties of the proposed converter, the design process had a somewhat narrow focus on highlighting its points of differentiation (in particular, its low input current ripple). In other designs, it is anticipated that considering other important objectives would significantly improve the converter's efficiency, reduce its size, and reduce its cost.
- *Analysis:* The proposed converter has been analysed in steady-state CCM operation, its efficiency has been measured, and its performance under unbalanced conditions has been studied. In addition, its transient performance has been investigated with a closed-loop current controller. For any DC-DC

converter, there are other ways the performance could be characterised, including thermal studies and a stability analysis.

With these limitations in mind, the next section suggests a range of paths that could be taken to extend the work undertaken.

7.4 Future Work

There are several ways to build upon the work presented in this thesis. This final section offers a range of suggestions that address the limitations previously outlined, as well as suggests new ideas for how the proposed converter could be further developed.

7.4.1 Bidirectional Operation

If the two diodes are replaced with MOSFETs, then the converter is able to operate with bidirectional power flow. This enables the proposed converter to be used in energy storage applications, and drives applications (with regenerative braking). Further, the converter could be designed to operate with power flowing the opposite direction, where two power sources are connected to the bipolar DC bus and the output is combined to a single unipolar DC bus.

7.4.2 Loss Characterisation and Efficiency Optimisation

If a PCB is designed with increased sensing, then the losses could be characterised with higher accuracy and into more segments (including MOSFET switching losses, individual diode conduction losses, inductor core losses, and capacitor ESR losses). These loss analyses could be performed over a range of switching frequencies. A better understanding of the converter's losses would help to guide a design concerned with maximising efficiency.

7.4.3 Thermal Analysis and Design

With a better understanding of the losses involved in each component, a proper thermal analysis of the converter could be undertaken. The results of this analysis would help to determine the required heat sink size, and better understand the

trade-offs between switching frequency, heat sink size, and passive component sizes. These results could inform the design of a converter concerned with improved volumetric and/or gravimetric power densities.

7.4.4 Discontinuous Conduction Mode (DCM) Operation

Due to the PV application studied, only CCM operation has been considered. It may be worth investigating the converter's operation under DCM operation. In this thesis, there is just one switch 'off' state to be considered. If this constraint is lifted, there are actually eight possible switch 'off' states. Since there are three inductors we have:

- One state where all three inductors are conducting
- Three different states where two inductors are conducting, depending on which inductor stops conducting first
- Three different states where one inductor is conducting, depending on which two inductors stop conducting first
- One state where none of the inductors are conducting.

7.4.5 Soft Switching

Soft switching, where transitions occur under favourable conditions (zero voltage or current) has been studied in other converters to reduce switching losses. The application of these techniques to the proposed converter has the potential to improve its efficiency.

7.4.6 Small Signal Model

The small signal models of both the CCS and CI-CCS converters could be determined. These small signal models could be used to better design controllers, and understand the stability, transient performance, and dynamic behaviour of the converter.

7.4.7 Energy Storage Integration on DC bus

Energy storage using batteries (commonly lithium-ion or lead acid) could be added to the bipolar DC bus, between the CI-CCS converter and the inverter. These batteries could either be directly connected (charged/discharged by controlling the DC bus voltages), or connected via a DC-DC converter to allow the batteries to be controlled independently of the DC bus voltage.

7.4.8 Wider Optimisation of Other Parameters

An optimisation (Bayesian or other) could be conducted not only on the coupling factors, but on other converter parameters too, including the inductances, capacitances, and switching frequency. Potential optimisation objectives include minimising the overall size (volume and weight), or maximising efficiency. This efficiency could be the converter's efficiency, the overall system's peak efficiency, or the overall system's weighted efficiency.

The weighted efficiency is calculated by considering the system's efficiency at various power outputs and using statistical data to describe how much time the system spends at various irradiance levels. The California Energy Commission (CEC) and European weighted efficiencies can be calculated with Equation 7.1 and Equation 7.2 respectively:

$$\eta_{CEC} = 0.04\eta_{10\%} + 0.05\eta_{20\%} + 0.12\eta_{30\%} + 0.21\eta_{50\%} + 0.53\eta_{75\%} + 0.05\eta_{100\%} \quad (7.1)$$

$$\eta_{Euro} = 0.03\eta_{10\%} + 0.06\eta_{20\%} + 0.13\eta_{30\%} + 0.10\eta_{50\%} + 0.48\eta_{75\%} + 0.20\eta_{100\%} \quad (7.2)$$

where $\eta_{X\%}$ is the efficiency at X% of rated capacity.

7.4.9 Advanced MPPT Control Techniques

Improved MPPT controllers (beyond simple P&O MPPT) could be implemented into the system controller to account for both local and global peaks, and improve tracking speed during insolation transients.

7.4.10 Extend the Control for Microgrid Applications

Research into the transition between grid-connected, power sharing, and standalone operational modes could be incorporated into the system controller. This

seamless transition could allow the proposed system to be used in microgrid applications.

7.4.11 Smaller Converter for Module-Level Integration

Smaller versions of the CI-CCS converter (rated at 100 W to 200 W) could be designed for use at the module-level, in the 'power optimiser' type systems described in Section 2.2.4. CI-CCS converters could be well suited in these applications due to the large step-up voltage (when considering the two outputs as a single non-grounded output). Alternatively, the converters could all grounded and have their outputs connected in parallel, though another boost stage would likely be required for connection to a grid-connected inverter.

7.4.12 Other CI-CCS Applications

In this thesis, the CI-CCS converter has only been considered for domestic PV applications. This converter also has applications for EVs, battery charging, and more.

Bibliography

[1] G. Carr, "Sunny uplands," tech. rep., The Economist, 2012.

[2] J. Trube, "International Technology Roadmap for Photovoltaic Results 2017," tech. rep., International Technology Roadmap for Photovoltaic (ITRPV), 2017.

[3] G. Masson, S. Orlandi, and M. Rekinger, "Global Market Outlook for Solar Power 2014 - 2018," tech. rep., European Photovoltaic Industry Associatio, 2014.

[4] G. Masson and M. Brunisholz, "A snapshot of global PV (1992-2014)," tech. rep., International Energy Agency - Photovoltaic Power Systems Programme, 2014.

[5] G. Masson and M. Brunisholz, "A snapshot of global PV (1992-2015)," tech. rep., International Energy Agency - Photovoltaic Power Systems Programme, 2015.

[6] G. Masson and M. Brunisholz, "A snapshot of global PV (1992-2016)," tech. rep., International Energy Agency - Photovoltaic Power Systems Programme, 2016.

[7] M. Rekinger and F. Thie, "Global Market Outlook for Solar Power 2015 - 2019," tech. rep., SolarPower Europe, 2015.

[8] M. Schmela, "Global Market Outlook for Solar Power 2016 - 2020," tech. rep., SolarPower Europe, 2016.

[9] J. Rogers and L. Wisland, "Solar Power on the Rise: The Technologies and Policies behind a Booming Energy Sector," tech. rep., Union of Concerned Scientists, 2014.

[10] U.S. Energy Information Administration, "Short-term energy outlook," tech. rep., U.S. Energy Information Administration, 2017.

[11] M. Boyd and C. Hansen, "Single diode equivalent circuit models," tech. rep., Sandia National Laboratories, 2012.

[12] N. Mohammad, M. Quamruzzaman, M. R. T. Hossain, and M. R. Alam, "Parasitic Effects on the Performance of DC-DC SEPIC in Photovoltaic Maximum Power Point Tracking Applications," *Smart Grid and Renewable Energy*, vol. 04, pp. 113–121, Jan. 2013.

[13] A. H. E. Khateb, N. A. Rahim, J. Selvaraj, and B. W. Williams, "DC-to-DC Converter With Low Input Current Ripple for Maximum Photovoltaic Power Extraction," *IEEE Transactions on Industrial Electronics*, vol. 62, pp. 2246–2256, April 2015.

[14] B. Erickson, "Power electronics and photovoltaic power systems laboratory: Filter inductor design," 2018.

[15] T. Esram and P. Chapman, "Comparison of Photovoltaic Array Maximum Power Point Tracking Techniques," *Energy Conversion, IEEE Transactions on*, vol. 22, pp. 439–449, June 2007.

[16] P. Stott, "How climate change affects extreme weather events," *Science*, vol. 352, no. 6293, pp. 1517–1518, 2016.

[17] R. A. Pielke Jr, "The British Climate Change Act: a critical evaluation and proposed alternative approach," *Environmental Research Letters*, vol. 4, no. 2, p. 024010, 2009.

[18] S. Droge, *The Paris Agreement 2015: turning point for the international climate regime*, vol. 4/2016. Social Science Open Access Repository (SSOAR), 2016.

[19] Sandbag, "Coal To Clean: How the UK phased out coal without a dash for gas," tech. rep., WWF, 2018.

[20] WWF, "Electric avenues: Driving home the case for electric vehicles in the UK," tech. rep., WWF, 2011.

[21] M. Yilmaz and P. Krein, "Review of Battery Charger Topologies, Charging Power Levels, and Infrastructure for Plug-In Electric and Hybrid Vehicles," *Power Electronics, IEEE Transactions on*, vol. 28, pp. 2151–2169, May 2013.

[22] P. Gadd, "Can your business or innovation help save the UK truckloads of CO2?," tech. rep., Innovate UK, 2016.

[23] ACEA, "Overview on tax incentives for electric vehicles in the EU," tech. rep., European Automobile Manufacturers Association, 2016.

[24] B. Tuttle, "So About That Goal of 1 Million Electric Cars by 2015," tech. rep., Time Inc., 2015.

[25] United Nations, "World population projected to reach 9.8 billion in 2050, and 11.2 billion in 2100," tech. rep., United Nations Department of Economic and Social Affairs, 2017.

[26] J. Cai, Z. Huang, J. Hauer, and K. E. Martin, "Current Status and Experience of WAMS Implementation in North America," tech. rep., Doubletree Systems, Inc., 02 2005.

[27] M. Riordan and L. Hoddeson, "The origins of the PN junction," *IEEE Spectrum*, vol. 34, pp. 46–51, June 1997.

[28] E. F. Kingsbury and R. S. Ohl, "Photoelectric properties of ionically bombarded silicon," *The Bell System Technical Journal*, vol. 31, pp. 802–815, July 1952.

[29] R. S. Ohl, "Properties of ionic bombarded silicon," *The Bell System Technical Journal*, vol. 31, pp. 104–121, Jan 1952.

[30] P. V. Kamat, "Solar Energy - Beyond the Hype," tech. rep., Department of Chemical and Biomolecular Engineering, University of Notre Dame, 2008.

[31] D. Feldman, J. Hoskins, and R. Margolis, "Q4 2017/Q1 2018 solar industry update," tech. rep., National Renewable Energy Laboratory, 2018.

[32] C. Roselund, "BNEF expects 34% fall in PV module prices in 2018," tech. rep., pv magazine, 2018.

[33] International Energy Agency, "Renewable electricity generation climbs to second place after coal," tech. rep., International Energy Agency, 2016.

[34] U.S. Energy Information Administration, "Short-term energy outlook," tech. rep., U.S. Energy Information Administration, 2018.

[35] Crown Agents Limited, "The Solar Revolution," tech. rep., Crown Agents Limited, 2017.

[36] S. Philipps and W. Warmuth, "Photovoltaics Report," tech. rep., Fraunhofer ISE, 2018.

[37] M. C. D. Piazza, M. Luna, G. Petrone, and G. Spagnuolo, "Translation of the single-diode PV model parameters identified by using explicit formulas," *IEEE Journal of Photovoltaics*, vol. 7, pp. 1009–1016, July 2017.

[38] J. Aller, J. Viola, F. Quizhpi, J. Restrepo, A. Ginart, and A. Salazar, "Explicit model of PV cells considering variations in temperature and solar irradiance," in *2016 IEEE ANDESCON*, pp. 1–4, Oct 2016.

[39] V. Nanjannavar, P. Gandhi, and N. Patel, "LabVIEW based PV cell characterization and MPPT under varying temperature and irradiance conditions," in *2013 Nirma University International Conference on Engineering (NUiCONE)*, pp. 1–6, Nov 2013.

[40] A. Kane and V. Verma, "Characterization of PV cell-environmental factors consideration," in *2013 International Conference on Power, Energy and Control (ICPEC)*, pp. 26–29, Feb 2013.

[41] E. Koutroulis, K. Kalaitzakis, and N. C. Voulgaris, "Development of a microcontroller-based, photovoltaic maximum power point tracking control system," *IEEE Transactions on Power Electronics*, vol. 16, pp. 46–54, Jan 2001.

[42] F. Liu, Y. Kang, Y. Zhang, and S. Duan, "Comparison of P&O and hill climbing MPPT methods for grid-connected PV converter," in *2008 3rd IEEE Conference on Industrial Electronics and Applications*, pp. 804–807, June 2008.

[43] Ying-Tung Hsiao and China-Hong Chen, "Maximum Power Tracking for Photovoltaic Power System," in *Industry Applications Conference, 2002. 37th IAS Annual Meeting. Conference Record of the*, vol. 2, pp. 1035–1040 vol.2, Oct 2002.

[44] A. Barchowsky, J. Parvin, G. Reed, M. Korytowski, and B. Grainger, "A Comparative Study of MPPT Methods for Distributed Photovoltaic Generation," in *Innovative Smart Grid Technologies (ISGT), 2012 IEEE PES*, pp. 1–7, Jan 2012.

[45] M. Masoum, H. Dehbonei, and E. Fuchs, "Theoretical and Experimental Analyses of Photovoltaic Systems With Voltage- and Current-Based Maximum Power-Point Tracking," *Energy Conversion, IEEE Transactions on*, vol. 17, pp. 514–522, Dec 2002.

[46] M. Bodur and M. Ermis, "Maximum Power Point Tracking for Low Power Photovoltaic Solar Panels," in *Electrotechnical Conference, 1994. Proceedings., 7th Mediterranean*, pp. 758–761 vol.2, Apr 1994.

[47] A. E. Khateb, N. A. Rahim, J. Selvaraj, and B. W. Williams, "The effect of input current ripple on the photovoltaic panel efficiency," in *2013 IEEE Conference on Clean Energy and Technology (CEAT)*, pp. 478–481, Nov 2013.

[48] A. E. Khateb, M. N. Uddin, N. A. Rahim, and B. W. Williams, "A comparative study on D converter based on control schemes of maximum extracted power," in *2016 IEEE Industry Applications Society Annual Meeting*, pp. 1–7, Oct 2016.

[49] A. H. E. Khateb, N. A. Rahim, and B. W. Williams, "Impact of fill factor on input current ripple of photovoltaic system," in *2015 International Conference on Renewable Energy Research and Applications (ICRERA)*, pp. 120–123, Nov 2015.

[50] J. Bing, "Advances in Commercial Applications of Photovoltaic Technology in North America: 2009 Update," in *Power and Energy Society General Meeting, 2010 IEEE*, pp. 1–5, July 2010.

[51] Y. Levron, D. Clement, Beomseok Choi, C. Olalla, and D. Maksimovic, "Control of Submodule Integrated Converters in the Isolated-Port Differential Power-Processing Photovoltaic Architecture," *Emerging and Selected Topics in Power Electronics, IEEE Journal of*, vol. 2, pp. 821–832, Dec 2014.

[52] Shibin Qin, A. Morrison, and R. Pilawa Podgurski, "Enhancing Microinverter Energy Capture with Sub-module Differential Power Processing," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, pp. 621–628, March 2014.

[53] D. Gautam, F. Musavi, M. Edington, W. Eberle, and W. Dunford, "An Automotive Onboard 3.3-kW Battery Charger for PHEV Application," *Vehicular Technology, IEEE Transactions on*, vol. 61, pp. 3466–3474, Oct 2012.

[54] S.-M. Chen, T.-J. Liang, and K.-R. Hu, "Design, Analysis, and Implementation of Solar Power Optimizer for DC Distribution System," *Power Electronics, IEEE Transactions on*, vol. 28, pp. 1764–1772, April 2013.

[55] SolarEdge, "8 Ways Power Optimizers are Better by Design: Microinverters & Power Optimizers - a Technical Comparison," tech. rep., SolarEdge, 2014.

[56] G. Walker, "Photovoltaic DC-DC Module Integrated Converter for Novel Cascaded and Bypass Grid Connection Topologies - Design and Optimisation," in *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, pp. 1–7, June 2006.

[57] H. Bergveld, D. Buthker, C. Castello, T. Doorn, A. de Jong, R. Van Otten, and K. de Waal, "Module-Level DC/DC Conversion for Photovoltaic Systems: The Delta-Conversion Concept," *Power Electronics, IEEE Transactions on*, vol. 28, pp. 2005–2013, April 2013.

[58] EnergySage, "String inverters vs. microinverters vs. power optimizers," tech. rep., EnergySage, 2014.

[59] SMA Solar Technology AG, "Technical Information: Capacitive Leakage Currents," tech. rep., SMA Solar Technology AG, 2018.

[60] L. Ma, F. Tang, F. Zhou, X. Jin, and Y. Tong, "Leakage current analysis of a single-phase transformer-less PV inverter connected to the grid," in *2008 IEEE International Conference on Sustainable Energy Technologies*, pp. 285–289, Nov 2008.

[61] W. Chen, X. Yang, W. Zhang, and X. Song, "Leakage current calculation for PV inverter system based on a parasitic capacitor model," *IEEE Transactions on Power Electronics*, vol. 31, pp. 8205–8217, Dec 2016.

[62] L. Wang, Y. Shi, Y. Shi, R. Xie, and H. Li, "Ground leakage current suppression in a 50 kW 5-level T-type transformerless PV inverter," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 1–6, Sept 2016.

[63] L. Wang, Y. Shi, Y. Shi, R. Xie, and H. Li, "Ground Leakage Current Analysis and Suppression in a 60-kW 5-Level T-Type Transformerless SiC PV Inverter," *IEEE Transactions on Power Electronics*, vol. 33, pp. 1271–1283, Feb 2018.

[64] A. Borgaonkar, "Solid state transformers: A review of technology and applications," tech. rep., Department of Electrical Engineering, Indian Institute of Technology, Delhi, 2015.

[65] B. Haug, "72 V Hybrid DC-to-DC Converter Reduces Intermediate Bus Converter Size by up to 50

[66] D. Dong, I. Cvetkovic, D. Boroyevich, W. Zhang, R. Wang, and P. Mattavelli, "Grid-Interface Bidirectional Converter for Residential DC Distribution

Systems - Part One: High-Density Two-Stage Topology," *Power Electronics, IEEE Transactions on*, vol. 28, pp. 1655–1666, April 2013.

[67] W. Li, Y. Gu, H. Luo, W. Cui, X. He, and C. Xia, "Topology Review and Derivation Methodology of Single-Phase Transformerless Photovoltaic Inverters for Leakage Current Suppression," *IEEE Transactions on Industrial Electronics*, vol. 62, pp. 4537–4551, July 2015.

[68] S. Goranti and G. TamizhMani, "Potential induced degradation (PID) study on accelerated stress tested PV modules," in *2012 38th IEEE Photovoltaic Specialists Conference*, pp. 002438–002441, June 2012.

[69] S. Pingel, O. Frank, M. Winkler, S. Daryan, T. Geipel, H. Hoehne, and J. Berghold, "Potential induced degradation of solar cells and panels," in *2010 35th IEEE Photovoltaic Specialists Conference*, pp. 002817–002822, June 2010.

[70] R. Redl, L. Balogh, and N. O. Sokal, "A new family of single-stage isolated power-factor correctors with fast regulation of the output voltage," in *Proceedings of 1994 Power Electronics Specialist Conference - PESC'94*, vol. 2, pp. 1137–1144 vol.2, June 1994.

[71] M. Nymand and M. A. E. Andersen, "High-Efficiency Isolated Boost DC-DC Converter for High-Power Low-Voltage Fuel-Cell Application," *IEEE Transactions on Industrial Electronics*, vol. 57, pp. 505–514, Feb. 2010.

[72] R. Erickson, M. Madigan, and S. Singer, "Design of a simple high-power-factor rectifier based on the flyback converter," in *Fifth Annual Proceedings on Applied Power Electronics Conference and Exposition*, pp. 792–801, March 1990.

[73] Y. Yang, "Analysis and design of a current-fed push-pull parallel-resonant converter for cooker magnetrons," in *2016 IEEE International Conference on Sustainable Energy Technologies (ICSET)*, pp. 300–305, Nov 2016.

[74] S. Devikala and P. Nirmalkumar, "Relative investigation between push-pull converter and non-isolated converter of low to high voltage gain," in *2012 International Conference on Emerging Trends in Electrical Engineering and Energy Management (ICETEEEM)*, pp. 366–370, Dec 2012.

[75] E. Hiraki, K. Hirao, T. Tanaka, and T. Mishima, "A push-pull converter based bidirectional DC-DC interface for energy storage systems," in *2009 13th European Conference on Power Electronics and Applications*, pp. 1–10, Sept 2009.

[76] C. Qiao and K. M. Smedley, "A topology survey of single-stage power factor corrector with a boost type input-current-shaper," *IEEE Transactions on Power Electronics*, vol. 16, pp. 360–368, May 2001.

[77] N. Kasa, T. Iida, and L. Chen, "Flyback inverter controlled by sensorless current MPPT for photovoltaic power system," *IEEE Transactions on Industrial Electronics*, vol. 52, pp. 1145–1152, Aug 2005.

[78] K. C. Tseng and T. J. Liang, "Novel high-efficiency step-up converter," *IEE Proceedings - Electric Power Applications*, vol. 151, pp. 182–190, March 2004.

[79] R. Watson, F. C. Lee, and G. C. Hua, "Utilization of an active-clamp circuit to achieve soft switching in flyback converters," *IEEE Transactions on Power Electronics*, vol. 11, pp. 162–169, Jan 1996.

[80] K. . Liu and F. C. Y. Lee, "Zero-voltage switching technique in DC/DC converters," *IEEE Transactions on Power Electronics*, vol. 5, pp. 293–304, July 1990.

[81] D. Habumugisha, S. Chowdhury, and S. P. Chowdhury, "A DC-DC interleaved forward converter to step - up DC voltage for DC Microgrid applications," in *2013 IEEE Power Energy Society General Meeting*, pp. 1–5, July 2013.

[82] H. Wu and Y. Xing, "A Family of Forward Converters With Inherent Demagnetizing Features Based on Basic Forward Cells," *IEEE Transactions on Power Electronics*, vol. 25, pp. 2828–2834, Nov 2010.

[83] B. Singh and G. D. Chaturvedi, "Comparative Performance of Isolated Forward and Flyback AC-DC Converters for Low Power Applications," in *2008 Joint International Conference on Power System Technology and IEEE Power India Conference*, pp. 1–6, Oct 2008.

[84] Y. Lu, T. Liang, C. Lin, and K. Chen, "Design and implementation of a bidirectional DC-DC forward/flyback converter with leakage energy recycled," in *2017 Asian Conference on Energy, Power and Transportation Electrification (ACEPT)*, pp. 1–6, Oct 2017.

[85] M. Taheri, J. Milimonfared, H. Bayat, H. Riazmontazer, and A. Noroozi, "Analysis and design of a new choke less interleaved ZVS forward-flyback converter," in *2011 2nd Power Electronics, Drive Systems and Technologies Conference*, pp. 81–86, Feb 2011.

[86] K. Gopinathan and M. I, "Pre-regulated push pull converter for hybrid energy systems," in *2015 International Conference on Technological Advancements in Power and Energy (TAP Energy)*, pp. 121–126, June 2015.

[87] Y. Yuan, L. Chang, and P. Song, "A New LCL- Resonant Push-Pull DC-DC Converter for Inverter Applications," in *2007 Large Engineering Systems Conference on Power Engineering*, pp. 261–264, Oct 2007.

[88] A. J. Sabzali, E. H. Ismail, M. A. Al-Saffar, and A. A. Fardoun, "New Bridgeless DCM Sepic and Cuk PFC Rectifiers With Low Conduction and Switching Losses," *IEEE Transactions on Industry Applications*, vol. 47, pp. 873–881, March 2011.

[89] China Energy Storage Network, "Ningxia built the country's largest desert photovoltaic integrated zone on the southern edge of the Tengger Desert," tech. rep., China Energy Storage Network, 2016.

[90] J.-S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," *IEEE Transactions on Industry Applications*, vol. 32, pp. 509–517, May 1996.

[91] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, pp. 724–738, Aug 2002.

[92] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, pp. 2219–2230, July 2010.

[93] J. Rekola and H. Tuusa, "Comparison of Line and Load Converter Topologies in a Bipolar LVDC Distribution," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, pp. 1–10, Aug 2011.

[94] E. Gurpinar and A. Castellazzi, "Single-Phase T-Type Inverter Performance Benchmark Using Si IGBTs, SiC MOSFETs, and GaN HEMTs," *IEEE Transactions on Power Electronics*, vol. 31, pp. 7148–7160, Oct 2016.

[95] P. Q. Dzung, D. N. Dat, N. B. Anh, L. C. Hiep, and H. Lee, "Design of HERIC inverter for PV systems by using hardware in the loop (HIL) concept," in *2014 9th IEEE Conference on Industrial Electronics and Applications*, pp. 2035–2040, June 2014.

[96] S. Hu, C. Li, W. Li, X. He, and F. Cao, "Enhanced HERIC based transformerless inverter with hybrid clamping cell for leakage current elimination," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 5337–5341, Sept. 2015.

[97] L. Zhang, K. Sun, Y. Xing, and M. Xing, "H6 transformerless full-bridge PV grid-tied inverters," *IEEE Transactions on Power Electronics*, vol. 29, pp. 1229–1238, March 2014.

[98] S. V. Araujo, P. Zacharias, and R. Mallwitz, "Highly Efficient Single-Phase Transformerless Inverters for Grid-Connected Photovoltaic Systems," *IEEE Transactions on Industrial Electronics*, vol. 57, pp. 3118–3128, Sept 2010.

[99] P. Somani and D. J. Vaghela, "Design of HERIC configuration based grid connected single phase transformer less photovoltaic inverter," in *2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT)*, pp. 892–896, March 2016.

[100] H. F. Xiao, L. Zhang, and Y. Li, "A Zero-Voltage-Transition HERIC-Type Transformerless Photovoltaic Grid-Connected Inverter," *IEEE Transactions on Industrial Electronics*, vol. 64, pp. 1222–1232, Feb 2017.

[101] Y. Yang, F. Blaabjerg, and H. Wang, "Low-Voltage Ride-Through of Single-Phase Transformerless Photovoltaic Inverters," *IEEE Transactions on Industry Applications*, vol. 50, pp. 1942–1952, May 2014.

[102] M. Victor, F. Greizer, S. Bremicker, and U. Hubler, "Method of converting a direct current voltage from a source of direct current voltage, more specifically from a photovoltaic source of direct current voltage, into a alternating current voltage," Aug. 2008.

[103] S. Saridakis, E. Koutroulis, and F. Blaabjerg, "Optimization of SiC-Based H5 and Conergy-NPC Transformerless PV Inverters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, pp. 555–567, June 2015.

[104] W. Cha, K. Kim, Y. Cho, S. Lee, and B. Kwon, "Evaluation and analysis of transformerless photovoltaic inverter topology for efficiency improvement and reduction of leakage current," *IET Power Electronics*, vol. 8, no. 2, pp. 255–267, 2015.

[105] G. Vazquez, T. Kerekes, A. Rolan, D. Aguilar, A. Luna, G. Azevedo, and G. Azevedo, "Losses and CMV evaluation in transformerless grid-connected

PV topologies," in *2009 IEEE International Symposium on Industrial Electronics*, pp. 544–548, July 2009.

[106] B. Ji, J. Wang, and J. Zhao, "High-Efficiency Single-Phase Transformerless PV H6 Inverter With Hybrid Modulation Method," *IEEE Transactions on Industrial Electronics*, vol. 60, pp. 2104–2115, May 2013.

[107] G. Rizzoli, M. Mengoni, L. Zarri, A. Tani, G. Serra, and D. Casadei, "Comparison of single-phase H4, H5, H6 inverters for transformerless photovoltaic applications," in *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, pp. 3038–3045, Oct 2016.

[108] W. Yu, J. S. Lai, H. Qian, C. Hutchens, J. Zhang, G. Lisi, A. Djabbari, G. Smith, and T. Hegarty, "High-efficiency inverter with H6-type configuration for photovoltaic non-isolated ac module applications," in *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1056–1061, Feb 2010.

[109] W. Yu, J. S. J. Lai, H. Qian, and C. Hutchens, "High-Efficiency MOSFET Inverter with H6-Type Configuration for Photovoltaic Nonisolated AC-Module Applications," *IEEE Transactions on Power Electronics*, vol. 26, pp. 1253–1260, April 2011.

[110] M. Xu, L. Zhang, Y. Xing, and L. Feng, "A novel H6-type transformerless inverter for grid-connected photovoltaic application," in *2012 7th IEEE Conference on Industrial Electronics and Applications (ICIEA)*, pp. 58–63, July 2012.

[111] T. S. Sangeetha and C. M. Noufal, "H6 inverter integrated with boost converter for PV application," in *2015 Online International Conference on Green Engineering and Technologies (IC-GET)*, pp. 1–6, Nov 2015.

[112] A. Das and G. Sheeja, "Photovoltaic H6-type transformerless inverter topology," in *2016 IEEE Annual India Conference (INDICON)*, pp. 1–6, Dec 2016.

[113] A. Reznik, M. Simoes, A. Al Durra, and S. Muyeen, "LCL Filter Design and Performance Analysis for Grid-Interconnected Systems," *Industry Applications, IEEE Transactions on*, vol. 50, pp. 1225–1232, March 2014.

[114] A. Anand and B. Singh, "Power Factor Correction in Cuk-SEPIC Based Dual Output Converter fed SRM Drive," *IEEE Transactions on Industrial Electronics*, pp. 1–1, 2017.

[115] M. B. Ferrera, S. P. Litran, E. Duran, and J. M. Andujar, "A SEPIC-Cuk converter combination for bipolar DC microgrid applications," in *2015 IEEE International Conference on Industrial Technology (ICIT)*, pp. 884–889, IEEE, mar 2015.

[116] M. B. Ferrera, S. P. Litran, E. Duran Aranda, and J. M. Andujar Marquez, "A Converter for Bipolar DC Link Based on SEPIC-Cuk Combination," *IEEE Transactions on Power Electronics*, vol. 30, pp. 6483–6487, dec 2015.

[117] G. Ranganathan and L. Umanand, "Power factor improvement using DCM Cuk converter with coupled inductor," *IEE Proceedings - Electric Power Applications*, vol. 146, pp. 231–236, March 1999.

[118] E. Wang, "Current Ripple Factor of a Buck Converter," tech. rep., Richtek, Apr. 2014.

[119] C. Yen, H. Hung, C. Hung, L. Lee, C. Lee, Y. Huang, F. Hsu, and T. Chen, "Negative bias temperature instability on subthreshold swing of SiC MOSFET," in *2016 European Conference on Silicon Carbide Related Materials (ECSCRM)*, pp. 1–1, Sept 2016.

[120] M. S. Rylko, B. J. Lyons, J. G. Hayes, and M. G. Egan, "Revised Magnetics Performance Factors and Experimental Comparison of High-Flux Materials for High-Current DC-DC Inductors," *IEEE Transactions on Power Electronics*, vol. 26, pp. 2112–2126, Aug 2011.

[121] Feng Wang, Xinke Wu, F. Lee, and Fang Zhuo, "Analysis of Unified Output MPPT Control in Sub-Panel PV Converter System," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, pp. 1–8, Sept 2013.

[122] G. T. Nikolov and V. C. Valchev, "Nanocrystalline magnetic materials versus ferrites in power electronics," *Procedia Earth and Planetary Science*, vol. 1, pp. 1357–1361, sep 2009.

[123] S. Jahdi, O. Alatise, J. Ortiz-Gonzalez, P. Gammon, L. Ran, and P. Mawby, "Investigation of parasitic turn-ON in silicon IGBT and Silicon Carbide MOSFET devices: A technology evaluation," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, pp. 1–8, Sept 2015.

[124] C. Liu, S. Chang, G. Huang, and Y. Lin, "A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 731–740, April 2010.

[125] R. Gray, "Oversampled Sigma-Delta Modulation," *IEEE Transactions on Communications*, vol. 35, pp. 481–489, May 1987.

[126] S. Cuk, "A new zero-ripple switching DC-to-DC converter and integrated magnetics," *IEEE Transactions on Magnetics*, vol. 19, pp. 57–75, Mar 1983.

[127] C. Adragna, "Minimizing filtering with ripple steering," tech. rep., STMicroelectronics, 2004.

[128] m. Jiang and Y. Chen, "Research on Bayesian optimization algorithm selection strategy," in *The 2010 IEEE International Conference on Information and Automation*, pp. 2424–2427, June 2010.

[129] W. Lyu, P. Xue, F. Yang, C. Yan, Z. Hong, X. Zeng, and D. Zhou, "An Efficient Bayesian Optimization Approach for Automated Optimization of Analog Circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, pp. 1954–1967, June 2018.

[130] Z. Shi, H. Liu, and Y. Zhu, "Study on the Performance of Decision Graph Bayesian Optimization Algorithm," in *2009 International Conference on Artificial Intelligence and Computational Intelligence*, vol. 1, pp. 573–576, Nov 2009.

[131] L. Shimin, T. Fengzhan, and L. Yuchang, "Global optimization using Bayesian heuristic approach," in *Proceedings of the 3rd World Congress on Intelligent Control and Automation (Cat. No.00EX393)*, vol. 5, pp. 3470–3473 vol.5, June 2000.

[132] H. Wang, B. van Stein, M. Emmerich, and T. Back, "A new acquisition function for Bayesian optimization based on the moment-generating function," in *2017 IEEE International Conference on Systems, Man, and Cybernetics (SMC)*, pp. 507–512, Oct 2017.

[133] D. Gomez, J. Becares, J. R. Janeiro, L. Gorostiaga, E. Baeyens, and E. J. Moya, "Assessment of Ziegler-Nichols tuned loops using control performance monitoring indices," in *ETFA2011*, pp. 1–4, Sept 2011.

[134] J. J. Gude and E. Kahoraho, "Modified Ziegler-Nichols method for fractional PI controllers," in *2010 IEEE 15th Conference on Emerging Technologies Factory Automation (ETFA 2010)*, pp. 1–5, Sept 2010.

[135] C. C. Hang, K. J. Astrom, and W. K. Ho, "Refinements of the Ziegler-Nichols tuning formula," *IEE Proceedings D - Control Theory and Applications*, vol. 138, pp. 111–118, March 1991.

[136] P. M. Meshram and R. G. Kanojiya, "Tuning of PID controller using Ziegler-Nichols method for speed control of DC motor," in *IEEE-International Conference On Advances In Engineering, Science And Management (ICAESM -2012)*, pp. 117–122, March 2012.

[137] C. T. Rodriguez, D. V. de la Fuente, G. Garcera, E. Figueres, and J. A. G. Moreno, "Reconfigurable control scheme for a PV microinverter working in both grid-connected and island modes," *IEEE Transactions on Industrial Electronics*, vol. 60, pp. 1582–1595, April 2013.

[138] R. Du and P. Robertson, "Cost-effective grid-connected inverter for a micro combined heat and power system," *IEEE Transactions on Industrial Electronics*, vol. 64, pp. 5360–5367, July 2017.

[139] Y. Xia, J. Roy, and R. Ayyanar, "A Capacitance-Minimized, Doubly Grounded Transformer less Photovoltaic Inverter With Inherent Active-Power Decoupling," *IEEE Transactions on Power Electronics*, vol. 32, pp. 5188–5201, July 2017.