

Video Article

Scalable Quantum Integrated Circuits on Superconducting Two-Dimensional Electron Gas Platform

Kaveh Delfanazari^{1,2}, Pengcheng Ma², Reuben Puddy², Teng Yi², Moda Cao², Yilmaz Gul³, Carly L. Richardson⁴, Ian Farrer^{2,5}, David Ritchie², Hannah J. Joyce¹, Michael J. Kelly^{1,2}, Charles G. Smith²

¹Centre for Advanced Photonics and Electronics, Engineering Department, University of Cambridge

²Department of Physics, Cavendish Laboratory, University of Cambridge

³Department of Electronic and Electrical Engineering, University College London

⁴Department of Materials Science and Metallurgy, University of Cambridge

⁵Department of Electronic and Electrical Engineering, University of Sheffield

Correspondence to: Kaveh Delfanazari at kd398@cam.ac.uk

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Abstract

To form a coherent quantum transport in hybrid superconductor-semiconductor (S-Sm) junctions, the formation of a homogeneous and barrier-free interface between two different materials is necessary. The S-Sm junction with high interface transparency will then facilitate the observation of the induced hard superconducting gap, which is the key requirement to access the topological phases (TPs) and observation of exotic quasiparticles such as Majorana zero modes (MZM) in hybrid systems. A material platform that can support observation of TPs and allows the realization of complex and branched geometries is therefore highly demanding in quantum processing and computing science and technology. Here, we introduce a two-dimensional material system and study the proximity induced superconductivity in semiconducting two-dimensional electron gas (2DEG) that is the basis of a hybrid quantum integrated circuit (QIC). The 2DEG is a 30 nm thick $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}$ quantum well that is buried between two $\text{In}_{0.75}\text{Al}_{0.25}\text{As}$ barriers in a heterostructure. Niobium (Nb) films are used as the superconducting electrodes to form Nb- $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}$ -Nb Josephson junctions (JJs) that are symmetric, planar and ballistic. Two different approaches were used to form the JJs and QICs. The long junctions were fabricated photolithographically, but e-beam lithography was used for short junctions' fabrication. The coherent quantum transport measurements as a function of temperature in the presence/absence of magnetic field B are discussed. In both device fabrication approaches, the proximity induced superconducting properties were observed in the $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}$ 2DEG. It was found that e-beam lithographically patterned JJs of shorter lengths result in observation of induced superconducting gap at much higher temperature ranges. The results that are reproducible and clean suggesting that the hybrid 2D JJs and QICs based on $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}$ quantum wells could be a promising material platform to realize the real complex and scalable electronic and photonic quantum circuitry and devices.

Video Link

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Introduction

A Josephson junction (JJ) is formed by sandwiching a thin layer of a non-superconducting (normal) material between two superconductors¹. Various novel quantum electronic and photonic circuits and devices can be built based on JJs^{2,3,4,5,6,7,8,9,10,11,12,13,14,15,16}. Among them, the JJs with semiconductor as their non-superconducting (normal) part, or superconductor-semiconductor-superconductor (S-Sm-S) JJs, have received much attention in recent years after the purported detection of exotic Majorana particles with zero electrical charges at the interface of a superconductor and a semiconducting one-dimensional (1D) nanowire^{17,18,19,20,21,22}. Nanowire-based hybrid devices are limited to the 1D geometry of the nanowire and fabrication of Y and/or T-structures out of them - a necessary requirement for Majorana braiding- is challenging²². The fine tuning of nanowire's chemical potential, for accessing topological phases, requires JJs with several electrostatically gates which causes quite a lot of issues in complex device fabrication out of nanowires. To overcome the scalability issues of 1D wires, two-dimensional (2D) material platforms are highly desirable^{19,22}.

Among 2D materials, the two-dimensional electron gas (2DEG) platform -forms when electrons are confined to an interface between two different materials in a semiconductor heterostructure- is the most promising candidate²². The combination of 2DEG with superconductors and forming hybrid 2D JJs opens a new avenue towards the development of next-generation scalable quantum systems such as topological quantum processing and computing. They can support phase coherent quantum transport, and proximity induced superconductivity with high transmission probability, which are fundamental requirement for topological phase observation. In this regard, we demonstrate a QIC on a chip which consists of array of ballistic 2D JJs that can be controlled by 20 wires. Each junction has two Nb electrodes as the superconducting part

and $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}$ quantum wells in a semiconducting heterojunction as the normal part. The wafer can be easily patterned to form complex structures and networked QICs.

The advantages of $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}$ 2DEG include: (i) relatively large g -factor, (ii) strong Rashba spin-orbit coupling, (iii) the low electron effective mass, and (iv) that the indium composition can be tuned allowing the formation of JJs with high interface transparency^{23,24,25}. The wafer can be grown as a disk of up to 10 cm diameter, allowing fabrication of thousands of hybrid 2D JJs and complex QICs networks so overcoming the scalability challenges of these quantum devices.

We discuss two different approaches for device fabrications: For device 1, a circuit which includes eight identical and symmetric JJs of 850 nm length and 4 μm widths are patterned by photolithography^{23,24}. The device 2 includes eight junctions with different lengths. They all have the same width of 3 μm . The JJs are patterned by e-bam lithography²⁵. The transport measurements at sub-Kelvin temperature ranges in absence/presence of magnetic field will be presented. The on-chip QICs consists of array of 2D Nb- $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}$ -Nb JJs. The long and short junctions are measured in a dilution fridge with a base temperature of 40 mK and liquid ^3He cooled cryostat with a base temperature of 300 mK, respectively. Devices are biased with an ac -signal of 5 μV at 70 Hz which is superimposed to the junction dc voltage bias. A two-terminal standard lock-in technique is used to measure the device output ac -current^{23,24,25}.

Protocol

NOTE: Semiconductor heterostructure and hybrid S-Sm Josephson junction fabrication are presented.

1. Semiconducting heterostructure fabrication

NOTE: The molecular beam epitaxy (MBE) grown $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}$ quantum wells are used in this study^{23,24,25,26}. **Figure 1** depicts the sequence of distinct layers:

1. Clean a 500 μm thick, 3-inch semi-insulating (001) GaAs substrate and remove the oxide layer in high temperature (above 200 $^{\circ}\text{C}$)²⁶.
2. Adjust the growth temperature at 580 $^{\circ}\text{C}$ and grow the buffer layer of GaAs/AlAs/GaAs films with thicknesses of 50/75/250 nm²⁶.
3. Ramp down the substrate temperature for 20 min and then grow a step-graded buffer layer of InAlAs with a 1300 nm thickness at starting substrate temperatures of $T = 416, 390, 360, 341, 331$ and 337 $^{\circ}\text{C}$ ²⁶.
4. Grow a 30 nm thick $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}$ quantum well 2DEG at slightly higher substrate temperature²⁶.
5. Cover the 2DEG quantum well with a 60 nm $\text{In}_{0.75}\text{Al}_{0.25}\text{As}$ spacer, and then modulation dope the wafer by a 15 nm thick of a n -type $\text{In}_{0.75}\text{Al}_{0.25}\text{As}$. This will assure the conductance in the dark²⁶.
6. Grow a 45 nm $\text{In}_{0.75}\text{Al}_{0.25}\text{As}$ layer followed by a cap layer of InGaAs with thickness of 2 nm²⁶.
7. Perform the measurement of the Shubnikov-de Haas oscillations and Hall effect to find the electron density (n_s) and mobility (μ_e) at temperature $T = 1.5 \text{ K}$ ²⁶. From the transport measurements, it was inferred that the $n_s = 2.24 \times 10^{11} \text{ (cm}^{-2}\text{)}$ and $\mu_e = 2.5 \times 10^5 \text{ (cm}^2\text{/Vs)}$ in the dark but $n_s = 2.28 \times 10^{11} \text{ (cm}^{-2}\text{)}$ and $\mu_e = 2.58 \times 10^5 \text{ (cm}^2\text{/Vs)}$ after illumination.

2. Two-dimensional Josephson junction fabrication

NOTE: Here, the fabrication process of the hybrid QICs with two different approaches are discussed^{23,24,25}. Device 1 with eight identical long Josephson junctions was fabricated only with a few steps of photolithography processing. The second device fabrication procedure was similar to device 1 up to formation of JJs which step the e-beam- lithography was used.

1. Sketch the JJs and QIC device layout, including mesa and ohmic patterns by using AutoCad software²⁵. Start the drawing by selecting appropriate layers to form the layer selector menu. Create a new layer from **Format | Layer** in the AutoCad software.
2. Design and fabricate the photolithography mask. Choose desired shapes and geometries from the panel menu in the software. Click on the desired shape of JJs (i.e., rectangles, squares) and push the drawing window to initiate the shape (click in the Autocad software help menu for more details).
3. Pattern the JJs and QICs designs, after developing the photoresist on the wafer, and fabricate the mesa structures to act as the active region (the raised area in **Figure 1**) by wet-etch in acid solutions of H_2SO_4 : H_2O_2 : (1:8:1000)^{23,24,25}. Rinse the device in DI water for 30 s and then dry with nitrogen gas.
4. Ensure an etch depth of $\sim 150 \text{ nm}$ by the DEKTA surface profiler^{23,24,25}.
5. Form ohmic contacts, to make electrical contact between the metal and 2DEG, by spinning photoresist on top of the wafer and then exposure to UV light through a photo-mask. Develop the resist in MF-319 for 1 min. Deposit a thin layer, between 50 nm and 100 nm of gold/germanium/nickel (AuGeNi) alloy over the resist-patterned sample^{23,24,25}.
6. Etch a # 140 nm deep trench on top of the active region to form 2D JJs by either photolithographically (device 1) or e- beam lithographically (device 2) patterning and wet-etching in acid described above (the JJs should be formed far from the ohmic contacts, a distance of $> 100 \mu\text{m}$, to ensure that the normal electrons from this part do not influence to the junction's interfaces)^{23,24,25}.
7. Sputter a #130 nm superconducting Nb film to form Nb- $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}$ -Nb JJs (by DC magnetron sputtering in Ar plasma),
8. Deposit 10/50 nm thick Ti/Au films for electrical contacts and transport measurement purposes.
9. Transfer and load the device on the standard leadless chip carrier (LCC) by using GE varnish, and make the electrical contacts between the device and LCC pads by using gold wires.
10. Load the devices into a ^3He cryostat or dilution refrigerator for transport measurements.

Representative Results

Figure 2a shows the scanning electron microscope (SEM) image of the device 1. A quantum circuit with 20 electrical wires can be seen. The design allows the measurement of one or series of JJs on a chip in one fridge cool-down. The SEM image of one junction on the circuit of Device

2, that was fabricated by e-beam lithography, is shown in **Figure 2b**. The distance between two Nb films in each side of the Nb-In_{0.75}Ga_{0.25}As-Nb junction is $L = 550$ nm at the shortest path. **Figure 2c** shows the SEM image of one junction of Device 1- which is photolithographically fabricated. Here, the two Nb electrodes are separated by a distance of $L = 850$ nm.

The Blonder–Tinkham–Klapwijk (BTK) theory is an acceptable model to describe the quantum transport in hybrid S-Sm junctions²⁷. The influence of the superconductor order parameters in semiconducting 2DEG results in a nonlinear differential conductance. At low temperatures, there are two possible reflection mechanisms at the Nb-In_{0.75}Ga_{0.25}As interfaces: normal reflection which causes no charge transmission through the interface and the Andreev reflections, which transmits two charge quanta $2e$, with the retroreflection of a hole^{23,24,25}. As the superconducting condensate consists of spin singlet Cooper pairs, the reflected hole has the opposite spin as the incoming electron. The cartoon diagram of these two processes is shown in **Figure 3a,b**, respectively²⁸.

If the interface between the Nb and In_{0.75}Ga_{0.25}As contact is not transparent, there is coexistence of both normal and Andreev reflected electrons. Thus, the resistance increases and a zero-bias peak within the gap is formed. Such an in-gap peak in the dV/dI (V_{SD}) is not observed in our junctions. However, for a homogeneous and barrier free ($Z=0$) interface between the Nb film and In_{0.75}Ga_{0.25}As contact, all incident electrons undergo Andreev reflection. In such condition, an excess current I_{exc} is formed in the junction due to correlations of electron- and hole-like quasiparticles. Therefore, the differential resistance within the gap is reduced and a flat U-shape dip in dV/dI (V_{SD}) is observed. According to BTK model, it can be inferred that no tunneling barrier formed at the Nb-In_{0.75}Ga_{0.25}As interfaces of both devices. Therefore, the barrier strength is estimated to be $Z < 0.2$ in our junctions^{23,24,25}.

Because of the proximity effect, induced gap of approximately $\Delta_{ind} \approx 100$ μ eV, and 650 μ eV are measured in the devices 1 and 2, respectively. The temperature dependence induced superconducting gap with pronounced subharmonic energy gap structures (SGS) peaks and dips for device 1 are shown in **Figure 4a**. The multiple Andreev reflections (MAR) at the interfaces of the Nb-In_{0.75}Ga_{0.25}As junction result in the observation of SGS in the differential conductance. At the lowest measured temperature $T = 50$ mK (red curve), the SGS appears with three peaks (named as P1, P2 and P3) and three dips (named as d1, d2 and d3). The temperature evolution of the peaks and dips due to the suppression of the induced superconductivity with temperature increase are shown in **Figure 4b**. The SGS peak positions obey the expression $V = 2\Delta/ne$ (Δ is the Nb gap energy, $n = 1, 2, 3, \dots$ is an integer, and e is the electron charge): P1, P2, P3 and P4 positions approximately correspond to $2\Delta/3e$, $2\Delta/4e$, $2\Delta/6e$ and the induced gap edge but the dip positions do not follow the expression. All features are significantly temperature dependent, and the strongest (weakest) SGS peaks (dips) are observed at $T = 50$ mK (800 mK). It is worth mentioning that even at temperatures above $T = 500$ mK where the supercurrent can no longer be seen, the SGS is observed but it disappears at $T > 800$ mK- when induced superconductivity is washed out.

For this device with array of eight 2D JJs, in 4 out of 7 junctions, a hard-induced superconducting gap in In_{0.75}Ga_{0.25}As 2DEG was found^{23,24}. However, three junctions showed a soft gap signature and neither a hard- nor a soft-gap structure was observed for the last junction because of a wire contact failure between the device and pad.

The superconducting gap as a function of applied V_{SD} voltage and temperature of device 2 is shown in **Figure 5a**. This device was measured at a ³He cryostat with base temperature of $T = 280$ mK. The temperature and magnetic field dependences transport measurements of device 2 do not show any sign of in-gap or sub-gap oscillations which are observed for device 1 (see **Figure 5a, b**). This could be due to the arrow-shaped geometry of the junction which may cause destructive interference of the MAR. Such features might appear in the differential conductance if the device is measured at much lower temperatures (dilution fridge base temperature). The induced gap is suppressed and moved toward zero voltage bias and their amplitudes diminish with further increasing of the applied temperature and magnetic field.

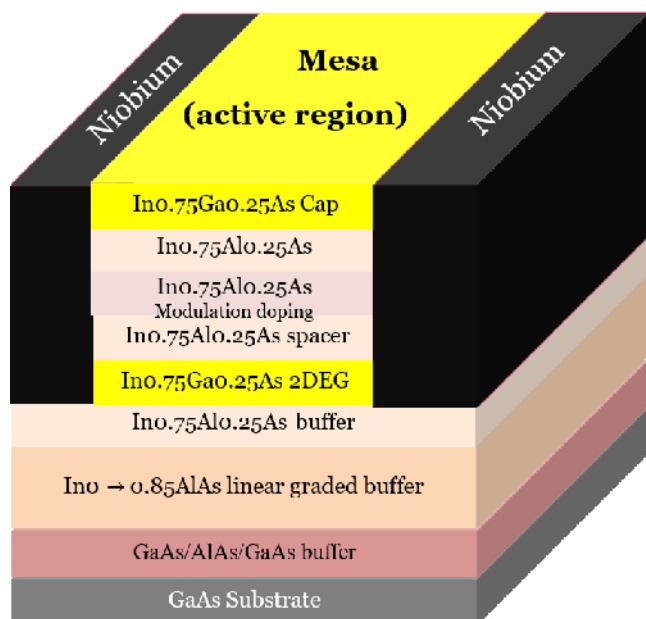


Figure 1. In_{0.75}Ga_{0.25}As/In_{0.75}Al_{0.25}As/GaAs heterostructure. The schematic view of the heterojunction where an In_{0.75}Ga_{0.25}As quantum well with 30 nm thickness is formed #120 nm below the wafer surface. Nb was used as the superconducting contacts (shown in black) to form a hybrid and ballistic Nb-In_{0.75}Ga_{0.25}As 2DEG–Nb Josephson junction. [Please click here to view a larger version of this figure.](#)

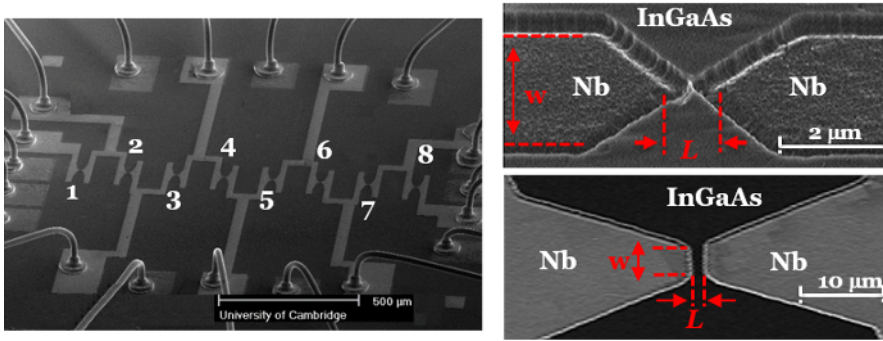


Figure 2: On-chip hybrid superconducting-semiconducting quantum circuits. (a) SEM image of the QICs device showing a top view of a quantum circuit with 20 control wires, and 8 planar and symmetric JJs on a chip. The SEM image of Nb-In_{0.75}Ga_{0.25}As-Nb JJs with an In_{0.75}Ga_{0.25}As 2DEG gap of length $L = 550$ nm and 850 nm for e-beam lithographically (b) and photolithographically (c) fabricated junctions. [Please click here to view a larger version of this figure.](#)

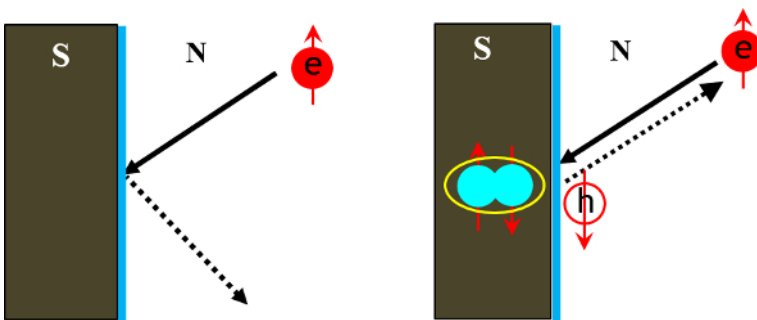


Figure 3: Normal and Andreev Reflections in hybrid superconducting-semiconducting junctions. (a) Specular quasiparticle reflection with no charge transmission through the interface. (b) Andreev reflection whereas the incoming electron is reflected as a hole in the opposite spin sub-band and transfer $2e$ charge into superconducting electrode. [Please click here to view a larger version of this figure.](#)

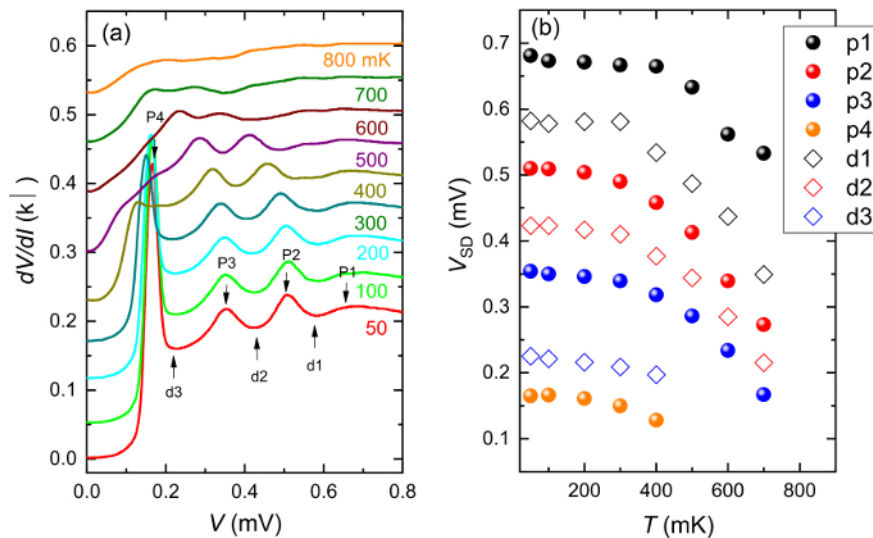


Figure 4: Induced superconductivity and SGS in In_{0.75}Ga_{0.25}As quantum wells in photolithographically fabricated junction. (a) Temperature dependence induced superconducting gap with pronounced SGS peaks due to multiple Andreev reflections. The SGS and the induced gap edge peaks, are marked by P1 to P4 while the SGS dips are marked by d1 to d3. (b) The SGS peaks and dips shown in (a) as a function of temperature. SGS are suppressed significantly at $T > 400$ mK leading to a shift toward zero bias. [Please click here to view a larger version of this figure.](#)

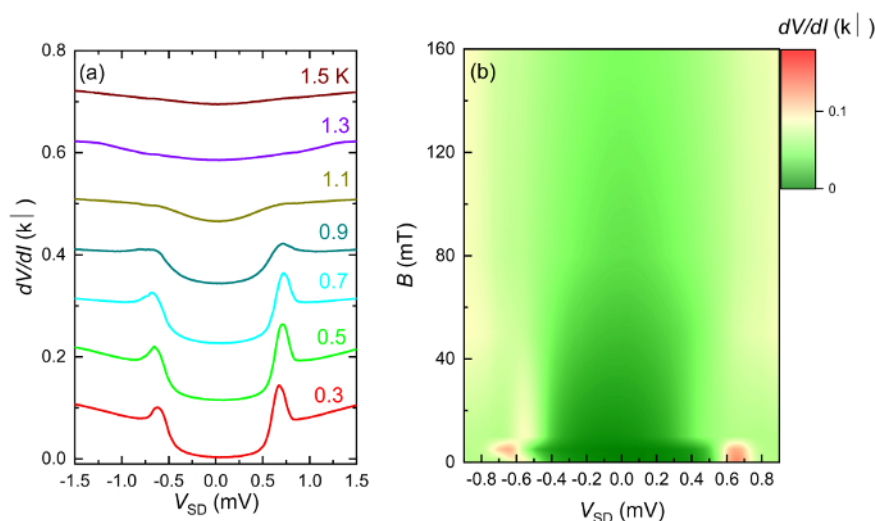


Figure 5. The temperature and magnetic field dependence of induced superconductivity in e-beam lithographically fabricated junctions. (a) Induced superconducting gap vs. applied source-drain voltage V_{SD} at temperatures between 300 mK and 1.5 K. The curves are vertically offset for clarity. (b) Color-coded differential resistance as a function of V_{SD} and perpendicular magnetic field at $T = 300$ mK. [Please click here to view a larger version of this figure.](#)

Discussion

On-chip QICs comprising an array of JJs based on superconducting indium gallium arsenide ($\text{In}_{0.75}\text{Ga}_{0.25}\text{As}$) quantum wells were demonstrated. Two important challenges of hybrid S-Sm material systems such as the scalability and interface transparency were addressed. Two critical steps within the protocol including the growth of high quality and high mobility $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}$ two-dimensional electron gas in semiconducting heterostructures and proximity induced superconductivity into 2DEG were discussed^{23,24,25}.

Growth of $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}$ with step-graded buffer layers in GaAs substrate and also the formation of homogeneous and barrier-free interfaces between the superconductor and semiconductor is a crucial step in such hybrid 2D quantum circuit development. It was demonstrated that with careful etching the sputtered superconducting film can make highly transparent contacts to $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}$ quantum wells resulting in detection of induced superconducting gap in semiconductors^{23,24,25}.

The significance with respect to existing methods is that the presented technique for 2D hybrid JJs and circuit realization does not require the in situ deposition of superconductor on semiconductors in an MBE chamber after the semiconductor growth has been completed^{23,24,25}. The other significance is that the heterostructure wafer can be grown as a disk of up to 10 cm diameter, allowing the fabrication of thousands of hybrid 2D junctions and circuits, so overcoming the scalability challenges of the hybrid S-Sm quantum circuits and devices^{22,23,24,25}.

The induced superconductivity in quantum wells, SGS on differential conductance of the 2D junctions, and the phase coherent ballistic quantum transport measured in our junctions strongly suggest that hybrid 2D junctions and circuits based on superconducting $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}$ 2DEG afford promising material system for scalable quantum processing and computing technologies. Our approach may open a new road toward quantum technology and helps pave the way for the development of on-chip topological quantum circuits for realizing the next generation of quantum processors^{23,24,25}.

Disclosures

The authors have nothing to disclose.

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