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Operation and performance of the 4H-SiC junctionless FinFET

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Abstract

This work presents a comprehensive study on the behaviour and operation of a vertical 1.2 kV 4H-SiC junctionless power FinFET. The increased bulk conduction in the channel of this topology may bring reductions in the channel resistance compared to trench MOSFETs, whose performance is limited by the high interface state density. For this purpose, finite element (FE) simulations are used to examine the operation of this device. It is hence demonstrated that the junctionless FinFET can attain a high average channel drift mobility well above 100 $cm^2/(Vs)$, leaving the resistance to be determined by the drift and substrate regions. This allows the FinFET to turn on and reach its steady state current using a much ($>$ 3x) smaller gate overdrive than standard designs. On the other hand, however, the overly high field in the gate oxide, the lack of an efficient mechanism for hole extraction, and the low threshold voltage can cause significant reliability issues. Furthermore, it is shown that the high input capacitance of the FinFET can limit its switching speed to slower levels than in standard trench MOSFETs, which raises the need for further development of the original design proposed for vertical GaN devices. In this context, it is demonstrated that the addition of a p-shield below the trenches can alleviate the off-state reliability issues and increase the speed, while still maintaining a competitive $R_{on} \sim 2 m\Omega\ cm^2$ even without the use of n-JFET enhancement doping.

1. Introduction

In recent years 4H-SiC has found wide-ranging applications in power electronics, thanks to its attractive electro-thermal properties and the continuous advances in its processing technology [1]. Nevertheless, the performance of conventional vertical planar MOSFETs grown on the Si-face is still limited by the high density of states D_{it} at the semiconductor-oxide interface [2]. The trapping of mobile carriers by these states during device operation leads to the well-known problems of a low channel drift mobility μ_{ch} [3, 4] and a dynamic instability of the threshold voltage V_{th} [5].

At the same time, vertical trench 4H-SiC MOSFETs have also been introduced as a competitive topology [6]. Due to the lower D_{it} of the oxide interface, which now forms on a non-basal crystal face, these devices can attain a much higher channel mobility. Indeed, very high field-effect mobilities $\sim$ 100 $cm^2/(Vs)$ have been commonly measured on nitrided MOS structures grown on $(1\bar{1}00)$ or $(11\bar{2}0)$ substrates [7]. However, the overall μ_{ch} will still be limited by the high transverse electric field $E_{\perp}$ at the interface, which promotes surface roughness and phonon scattering [8].

In this context, there has been an increased interest in applying solutions from digital electronics to the design of power devices. A noteworthy example is a junctionless double-gate MOSFET structure recently proposed for vertical GaN devices [9]. This design dispenses with the difficulties of acceptor implantation in GaN and has been reported to attain a low specific on-state resistance R^*_{on} ($\sim$1.8 $m\Omega\ cm^2$), along with a competitive efficiency even at MHz switching frequencies [10]. However, the enlarged bulk conduction of this FinFET structure may also prove to be beneficial to 4H-SiC technology through potentially increasing the switching speed and the channel mobility. In fact, SiC MOSFETs with sub-100 nm fin pitches have already been demonstrated through state-of-the-art processing techniques [11]. That is why this work looks into the likely

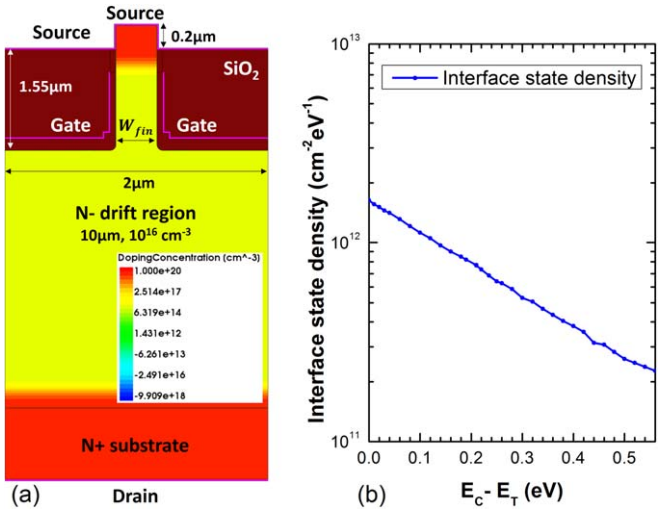

Figure 1. Structure of the examined FinFET (a) and assumed energy distribution of states at the gate oxide/semiconductor interface (b).

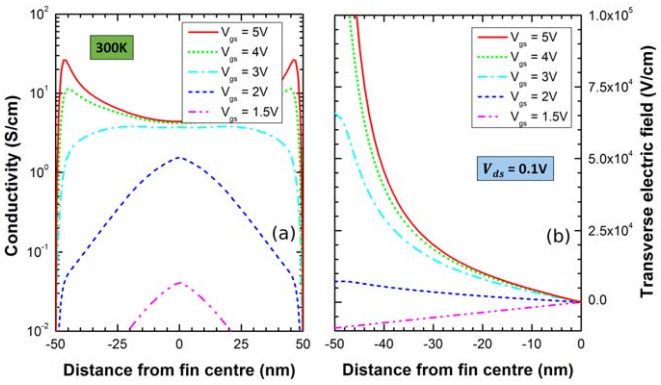

Figure 2. Profiles of the conductivity (a) and the transverse electric field (b) across the fin. The channel forms initially at the fin's centre. At V_{gs} above V_{fb} the current starts to increasingly shift toward the MOS interface.

performance of this device, using finite element simulations. The spatial distribution of the carriers and the channel mobility in the on-state are examined in section 2. In turn, the blocking capability is investigated in section 3 for a range of fin widths. Finally, section 4 looks into the FinFET's performance during clamped inductive switching and provides a comparison for a number of design variants (including a reference conventional trench structure). In this way, the key capabilities and limitations of this device can be identified, which makes it possible to identify some of the necessary changes that need to be made to the original design proposed for GaN.

2. On-state performance

The examined power FinFET is a 1.2 kV structure, whose specifications are presented in figure 1(a). The drift region is 10 μm thick and is doped n-type at 10^{16} cm^{-3} (the same doping is used for the fin). Conversely, the substrate is modelled as a lumped resistor of 0.7 mΩ cm^2 at 300 K, which varies by 6 $\mu\Omega$ cm^2 K^{-1}. The gate oxide thickness is set to 50 and 100 nm along the sidewalls and the bottom of the trench, respectively. A cell pitch of 2 μm is assumed, while the fin width W_{fin} is left as a variable. As discussed in [9], the threshold of this device is to be adjusted through the work function difference between the gate electrode and the semiconductor fin. Thus, for the purpose of illustration, the gate metal is assumed to have a work function ϕ_M of 5.05 eV (same as Ni, which is commonly used in 4H-SiC Schottky diodes [3]). Although this value may be modified through the use of an alternative gate metal or doped polysilicon, here it allows to beneficially increase the threshold voltage V_{th}.

Similarly to trench MOSFETs, the gate oxide interface here forms on one of the non-basal planes of the semiconductor. Since the D_{it} profiles on the $(1\bar{1}00)$ and $(11\bar{2}0)$ faces are comparable and remain linear (on a log

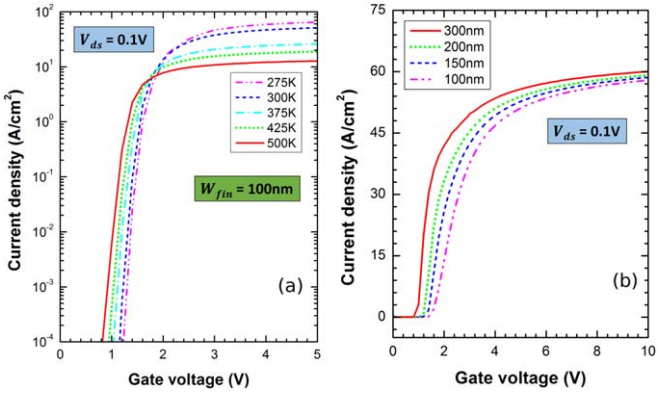

Figure 3. FinFET transfer characteristic for various temperatures (a) and fin widths (b). Conduction in the fin's bulk leads to rapid (for < 3 V overdrive) modulation and 'saturation' of the channel resistance.

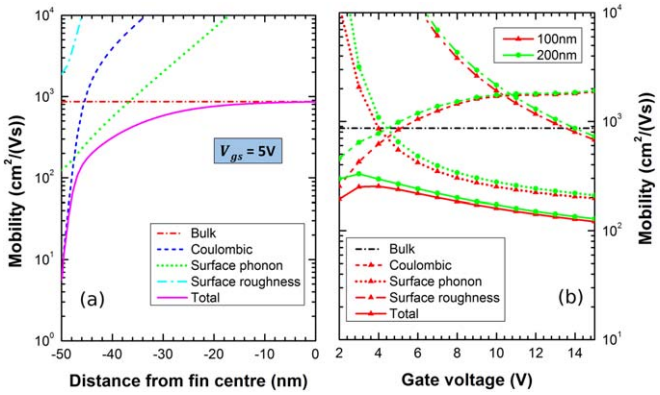

Figure 4. Evolution of the drift mobility's components with the semiconductor depth (a) and of their net value with V_{gs} for two fin widths (b). At a low overdrive (< 3 V) Coulomb scattering dominates, yet, unlike in the trench MOSFET [3], it gets fully replaced by phonon scattering at higher V_{gs} due to the stronger screening. The increased role of bulk conduction makes the net mobility larger for the wider fin. Still, in both cases $\mu^*_{ch} > 100$ cm^2/(Vs).

scale) even close to the bottom of the conduction band E_C [7], the interface here is freely described with the D_{it} for the $(1\bar{1}00)$ plane in [7] (figure 1(b)). This distribution is extrapolated to estimate the interface state density near E_C. Despite the use of nitridation (and the consequent generation of donor states [12]), all traps are (for simplicity) assumed to be acceptor. Conversely, trap levels in the conduction band (and fixed charges) are not considered due to lack of data.

The turn-on mechanism of the FinFET is now examined in figure 2 (for a fin width W_{fin} of 100 nm).

The gradual increase of V_{gs} counteracts the intrinsic band bending at the oxide-semiconductor interface, causing the depletion region in the fin to contract and shift toward the sides. As a result, unlike a more conventional FinFET with a p-doped fin [11], here the conductive channel forms firstly at the centre (figure 2(a)). This decreases the impact of the interface states on the turn-on process and hence allows the subthreshold leakage current J_l to increase with nearly the 'ideal' theoretical slope of 60 mV/dec (figure 3(a)).

At a higher gate bias the on-state current gets shifted toward the MOS channel. Firstly, at $V_{gs} \approx 1.9$ V the carrier density n reaches the doping concentration N_D. Since from Poisson's law $\frac{\partial E_\perp}{\partial z} \approx q(N_D - n)/\epsilon_{SiC}$ (where ϵ_{SiC} is the dielectric permittivity, z is the depth into the semiconductor relative to the interface, and q is the elementary charge), the transverse electric field $E_\perp$ falls to zero throughout the entire fin (figure 2(b)). Thus, here the MOS channel turns on already at the flatband voltage $V_{fb} \approx 1.9$ V, which can also be (approximately) estimated from the intrinsic band bending via (1), where χ_{SiC}, N_C, and N_{it} are the electron affinity, the effective conduction band density of states, and the steady state density of active interface charges (at a given V_{gs}), while C_{ox} is the gate oxide capacitance per unit area [9]. The low $E_\perp$ and the (still significant) conduction at the fin's centre make the net channel mobility comparable to the bulk mobility (figure 4). As a result, the current reaches 75% of its 'saturated' value within just $\sim$2 V variation in V_{gs} (figure 3(b)).

$$V_{fb} = \frac{\phi_M - \chi_{SiC} - k_B T \ln(N_C/N_D)}{q} + \frac{qN_{it}(V_{fb})}{C_{ox}} \quad (1)$$

After the MOS channel gets activated, the on-state current exhibits a well-defined hard saturation (figure 3(b)). Indeed, by means of measuring the drop of the electron quasi-Fermi level across the vertical length of the fin, it is found that the resulting R^*_{on} of ≈ 1.65 mΩ cm^2 (at 15 V V_{gs}) is dominated by the combined resistance of the substrate, drift, and current spreading regions ($\approx$89% of the total). The reduced significance of the channel can also be inferred from the temperature coefficient of R^*_{on}, which increases monotonically with temperature T due to the enhanced lattice vibrations (figure 3(a)). Here it must be noted that, in practice, the contact resistance at the source will become important (at sufficiently small W_{fin}), unless an interdigitated design is used for the structure, so that the contacting (with the n+ source) is done in a region with a larger cross-sectional area. Nevertheless, it can be seen that here the structures with a wider fin do already attain a smaller R^*_{on}. While this is partially due to the greater overdrive (and hence larger electron density per gate area N_{inv} for a given V_{gs}) for larger W_{fin}, the average channel mobility also increases with the fin width. This trend is mirror opposite to what has been reported for another SiC FinFET device, which, however, incorporates a p-type doped channel [11].

In order to examine this difference more concretely, the individual components (μ_i) of μ_{ch} are computed using Matthiessen's rule [13] and are then averaged with respect to the conductivity σ (across the width of the fin) using (2) (figure 4(b)). Due to the lack of experimental data on the drift mobility in a non-Si-face channel, surface phonon and roughness scattering are estimated using the fittings in [14] for the (0001) plane. Conversely, Coulombic scattering is described through the well-known semi-empirical relation $\mu_C \sim N_s^\gamma(z)/N_{it}$, where $N_s(z)$ is the sheet carrier density at a depth z [8]. For this purpose, a dedicated model, which can compute the integral expression for $N_s(z)$ exactly (in the TCAD), has been built and fitted to the results for the aforementioned p-channel FinFET

$$\frac{1}{\mu_i^*} = \frac{\int_0^\infty (\sigma(z)/\mu_i(z))\,dz}{\int_0^\infty \sigma(z)\,dz} \quad (2)$$

in [15]. Finally, the bulk mobility μ_B is estimated using Uhnevionak's improvement on Arora's model [16].

The resulting composition of μ_{ch} can be observed in figure 4. At a low gate bias Coulombic scattering by the interface charges is the dominant process. In practice, the presence of fixed charges ($\sim 10^{12}$ cm^{-2}) will enhance this effect further through increasing N_{it} (which here reaches only $\sim 3.5 \times 10^{11}$ cm^{-2}). For the currently examined device, however, Coulombic scattering becomes negligible at larger V_{gs} due to the greatly increased screening by the electron carriers. Thus, at higher V_{gs} phonon (and eventually roughness) scattering becomes the dominant component. From figure 4(b) it can now clearly be seen that the role of surface scattering increases when the fin width is reduced, simply due to the smaller distance between the interface and the fin's centre. Indeed, in the junctionless FinFET, carrier flow through the centre is more strongly pronounced at larger W_{fin} due to the weaker depletion, which is why μ^*_{ch} is closer to the bulk mobility in this case. Conversely, the mobility improvement in the ultra-narrow-body MOSFET in [11] is obtained through the bulk inversion of the p-type fin, which arises only at sufficiently small W_{fin}. Thus, the channels in these two devices form by different mechanisms. Regardless of this, the mobility in the junctionless FinFET remains well above 100 cm^2/(Vs) for both values of W_{fin}. In fact, the small contribution of the channel to the total on-state resistance R^*_{on} can make this structure particularly attractive for blocking voltage ratings below 1.2 kV, where it can compete with Si Superjunction and GaN power devices.

On the other hand, despite its good current carrying capability, the examined device possesses important reliability issues. As seen from figure 3(a), the FinFET is characterised by a fairly low threshold voltage V_{th} already at 300 K. At 425 K this value falls down even below 1 V. This problem may be further aggravated by the presence of positive fixed charges, which already for a density of 10^{12} cm^{-2} reduce V_{th} below 0 V. Parasitic turn-on can hence also arise during switching (due to the extensive gate/drain coupling). The threshold can be increased by reducing W_{fin} further, yet this is not a flexible approach. An alternative may be to dope the channel p-type as in [11], albeit at the cost of reducing the improvement in the channel mobility. Regardless of the exact method, the original junctionless FinFET design (proposed for GaN) requires further development to increase V_{th}.

3. Off-state performance

One of the primary problems of junctionless devices is well known to be their current blocking capability. That is why the off-state behaviour of the FinFET is now to be considered. For this purpose, the impact ionisation coefficients $\alpha_{n,p}$ are computed by means of Okuto-Crowell's model, using Niwa's parameters for 4H-SiC [17].

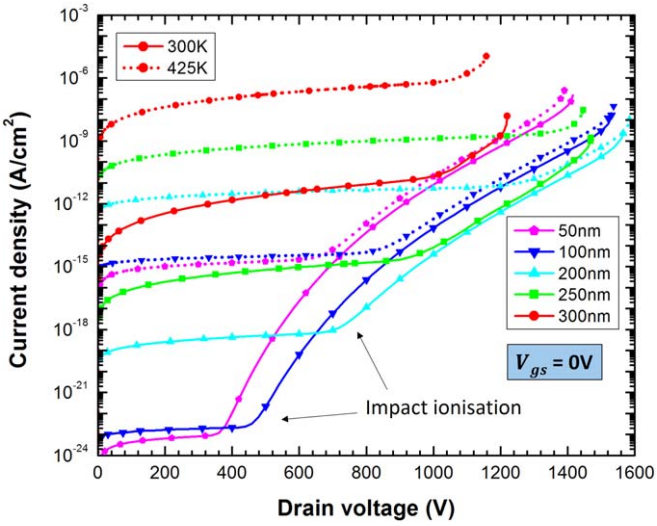

Figure 5. Quasistationary breakdown characteristic for various fin widths. Breakdown for fin widths above ~200 nm is dominated by punch-through. Conversely, for small $W_{fin} \sim 50$ nm premature impact ionisation at the bottom of the fin causes a reduction of V_{br}.

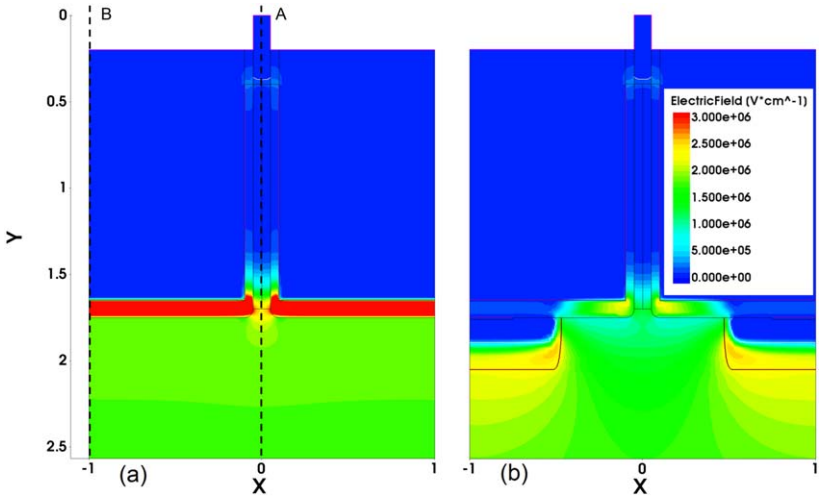

Figure 6. Electric field profile (at 1000 V V_{ds}) for the structure from figure 1(a) and a different, modified design (from figure 10(a)) with a grounded p-shield (b).

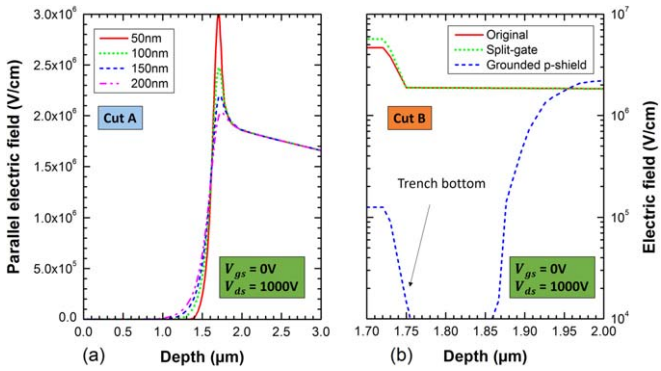

Figure 7. Electric field profiles through the centre of the fin (along cutline A in figure 6(a)) for various fin widths (a) and across the gate oxide (cutline B for a W_{fin} of 100 nm) (b) at 1000 V V_{ds} for the topologies in figure 10.

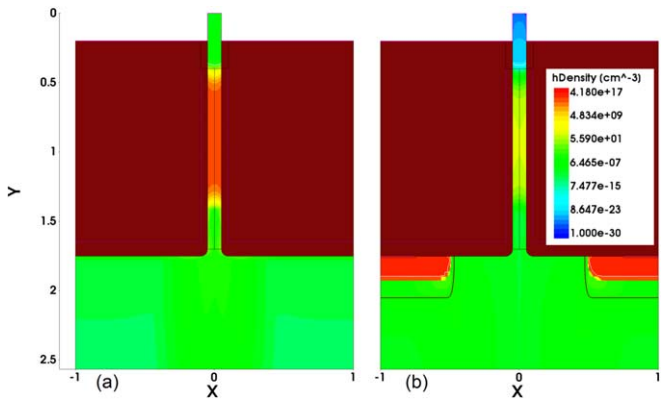

Figure 8. Profile of the hole density in the fin for the structures from figures 1(a) and 10(a) at 1000 V V_{ds}.

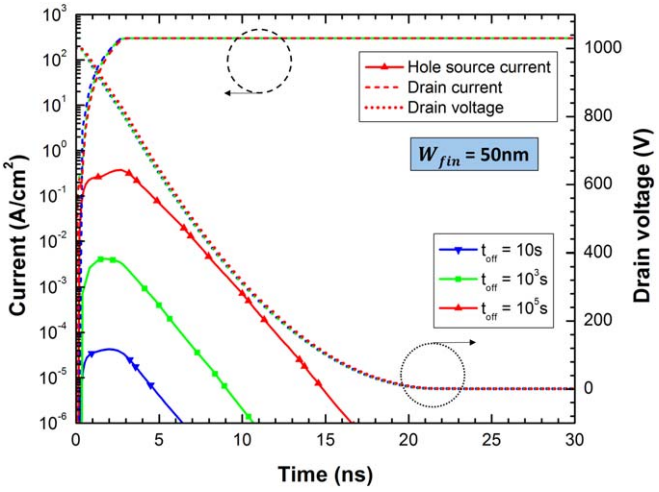

Figure 9. Turn-on characteristic of the original FinFET (W_{fin} = 50 nm and active area of 1 cm^2) after an initial blocking period (with a DC supply of 1 kV) t_{off} of 10, 10^3, and 10^5 s. The holes, which accumulate in the fin during the off-state, increase R^*_{on} and induce a source hole current at turn-on. This effect, however, becomes negligible for kHz switching applications.

In turn, the SRH lifetimes are modelled using Scharfetter's relation [18], with a peak lifetime $\tau_{n,p}$ of 150 ns for both types of carriers.

The quasistationary breakdown I_{ds}/V_{ds} characteristic (at $V_{gs} = 0$ V) can be observed in figure 5 for a range of fin widths. Initially, at low V_{ds}, the leakage current J_l increases monotonically with W_{fin}, as a result of the weaker depletion of the carriers at the centre of the fin. This implies the presence of punch through-assisted breakdown (at a higher V_{ds}), which can be recognised from the negative temperature coefficient of the breakdown voltage V_{br} that is observed for fin widths W_{fin} above $\sim$200 nm. For improved device reliability, it is clearly preferable to design the fin so that breakdown occurs through avalanche. In practice, the onset of punch through breakdown will occur at a smaller W_{fin} if a lower gate work function is assumed. For this design, however, a peak fin width W_{fin} limit of 200 nm is sufficient.

At higher V_{ds} a knee point appears in the response of the structures with a narrow fin. This steeper rise of J_l turns out to be caused by premature impact ionisation at the bottom of the fin (figures 6–7). Indeed, at high V_{ds} a sizeable potential drop ($\sim$ tens of V) develops across the bottom of the gate oxide (due to the gate contact deposited on top). Thus, this same potential difference needs to be supported by the fin (for the electron quasi-Fermi potential (relative to the source) in the drift region is nearly constant ($\pm$5% variation) in the lateral direction). As seen from figure 7(a), however, the gate oxide pushes the potential field lines down toward the drift region more effectively for narrower fin widths. This leads to an accumulation of the field lines at the bottom of the fin (in order for the same voltage drop to develop across it), thereby creating a spike in the vertical component of the electric field. This does not result in immediate device failure, since impact ionisation remains localised due to the small ($\ll W_{cell}$) width of the fin. In fact, the limited degree of this process (which, nonetheless, is now the dominant mechanism for carrier generation) allows the leakage currents at both temperatures to become comparable (without the device failing). At a sufficiently high V_{ds}, however, this effect

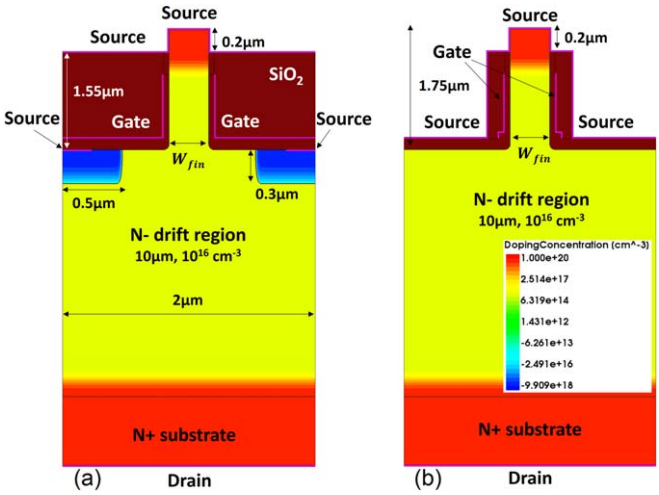

Figure 10. Schematic of an alternative FinFET design with a grounded p-shield (peak doping of 10^{19} cm^{-3}) (a) and the split-gate topology (b) proposed in [10].

aids the formation of a premature avalanche current. That is why, if the fin width is reduced below ~100 nm, the breakdown voltage V_{br} now starts to decrease (figure 5). As a result, the peak blocking capability is attained at an intermediate fin width in the range 100–200 nm.

The effect described above also creates a reliability problem at turn-on. Indeed, although the generated holes get extracted by the fin, they cannot continue further, due to the potential barrier that the highly doped n-source region presents. Thus, the holes instead accumulate inside the fin, where they can reach a high steady state concentration ~10^{17} cm^{-3} (figure 8). On the one hand, the presence of this virtual p-region contains weakly the punch-through current, allowing satisfactory blocking up to ~200 nm W_{fin} (which is why this limiting value for the fin width falls to ~175 nm, if $\tau_{n,p}$ is increased to 1 μs). Nevertheless, these holes can also slow down the turn-on process due to recombination with the electron majority carriers. To examine this, the FinFET is inserted in a single phase voltage clamp circuit (with a PSPICE diode) and is kept in blocking mode for a period of t_{off}, after which the gate is ramped to 15 V for 1 ns. In order to strengthen the above effect of hole generation (and hence attempt to consider a worst-case scenario), here W_{fin} is decreased to 50 nm, while the positive supply rail is set to 1 kV. The load inductor L_1 is also replaced by a constant current source of 48 A (≡ 300 A cm^{-2}) to make the comparison feasible. From the subsequent results in figure 9 it can hence be seen that, for t_{off} above 10^3 s, a measurable spike of hole current flows to the source contact, as soon as the device turns on. At the same time the presence of holes in the fin does slow down the rate at which V_{ds} falls and J_{ds} increases (due to the larger R^*_{on}), yet the effect is quite negligible, since the holes get cleared from the channel by the electron current well before V_{ds} reaches its on-state value. Thus, these differences will be more pronounced at lower current levels. Nonetheless, the hole current decreases by orders of magnitude, as the blocking period t_{off} is reduced, which is why this effect will become negligible during kHz switching.

On the other hand, the lack of protection for the gate oxide can cause important reliability issues. Indeed, since the applied voltage is supported solely through the semiconductor/oxide junction, the electric field in the oxide rises above 4 MV cm^{-1} well below the rated V_{br} (figure 7(b)). In practice, this will clearly increase the gate leakage current and eventually cause TDDB of the oxide. That is why the original design from [9] has to be modified to address this issue. A well known technique, which can be applied to this structure, is to insert a p-shield just below the gate trenches (figure 10(a)) [19, 20]. Here the p-layer is specified to cover only a portion of the area below the gate trench (which can be performed as an intermediate implantation in a multi-step epitaxial growth process) to contain the adverse effect on R^*_{on}. This problem is especially important for the FinFET, due to the small (~ nm) width of the fin (and hence larger current spreading resistance). In addition, the p-shield here is electrically connected to the source, so as to prevent its gradual depletion of holes during switching (and hence avoid the concomitant increase of R^*_{on} and the electric field at the p–n junction) [21].

The resulting improvement of the off-state performance can be clearly seen from figures 6, 8(b). The newly added p-layer shifts the peak of the electric field away from the corner of the trench to the newly formed p–n junction, thereby protecting the oxide. Furthermore, the p-shield can now collect the holes generated due to impact ionisation, thanks to the fact that it is grounded. As a result, the holes no longer accumulate in the fin but flow to the source through the p-shield instead (figure 8(b)), thereby resolving the reliability issue discussed in figure 9. Similarly to conventional trench structures, a more complicated layout may need to be developed in order to facilitate the grounding of the p-shield [22, 23]. However, thanks to the increase of the channel mobility

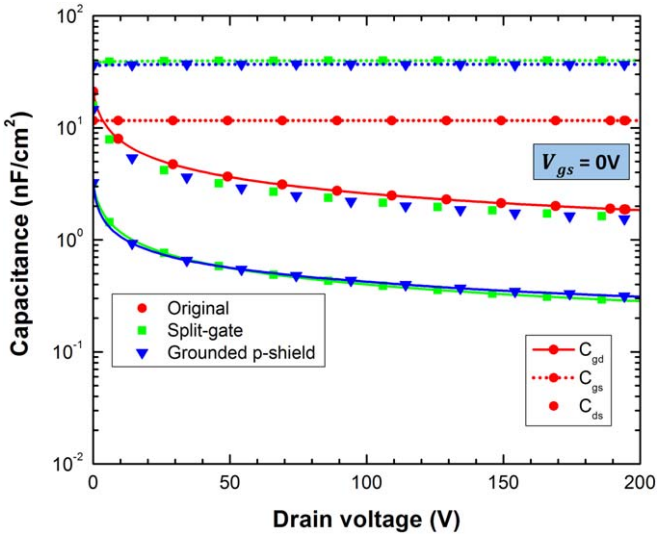

Figure 11. Capacitance/voltage profile of the examined FinFET structures during the off-state. The designs in figure 10 decrease C_{gd}, thereby reducing switching losses and the susceptibility to parasitic gate turn-on.

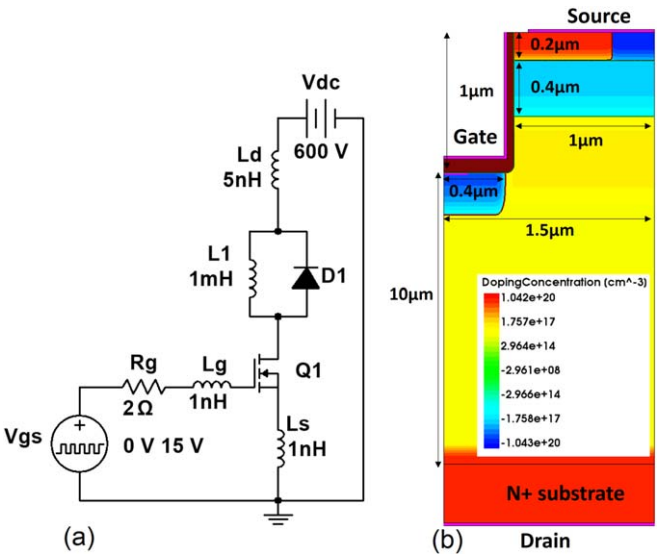

Figure 12. Inductive circuit used for the switching simulations (a) and schematic of the reference trench structure (b) used for the comparison.

provided by the junctionless FinFET, a smaller channel density can be tolerated to a greater degree than in other SiC trench structures, thereby allowing for a looser layout design.

4. Switching performance

Thanks to the improved modulation of the channel by the gate, the current has been observed to rise sharply with V_{gs} (figure 3(b)). Clearly, however, the switching speed of the device will be determined by the internal coupling between the contacts of the structure, as well as by the external impedance seen by the device at each terminal. These terms will depend on the layout and the packaging of the die, yet the individual cell itself will also impose a fundamental limitation on the achievable speed. That is why the capacitances of the unit cell in figure 1(a) are now examined (for $W_{fin} = 100$ nm). These are computed by means of a linearised small signal analysis, using a 1 MHz perturbation signal superimposed on the DC bias of each contact [18].

The resulting C/V waveforms can be seen in figure 11. Due to the small ($\ll W_{cell}$) width of the fin, the drain-to-source capacitance C_{ds} is negligible. Conversely, the transfer capacitance C_{rss} clearly forms the largest component (at 0 V V_{ds}) in the original design. This results in a large C_{gd}/C_{ds} ratio, which is undesirable due to the

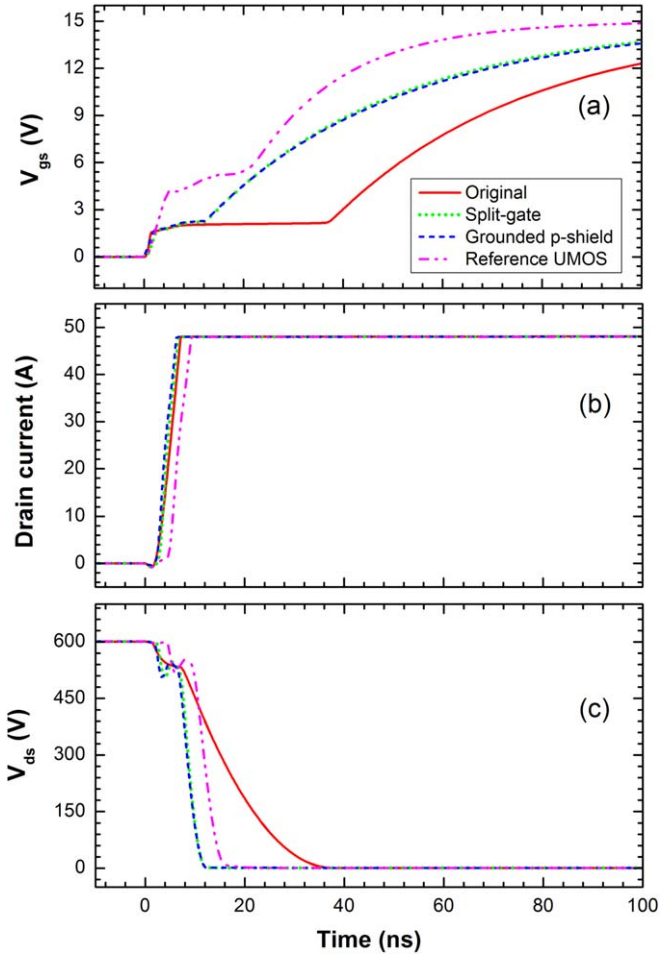

Figure 13. Turn-on characteristic of the examined FinFETs and the reference for an active area of 16 mm^2.

disproportionately increased gate-drain charge Q_{gd} (and hence larger switching losses). An alternative approach, which has been proposed as a development of the GaN FinFET [10], is to use a split-gate topology for the trench (figure 10(b)). Here the oxide layer is etched selectively, so as to be able to deposit the source metal at the bottom of the trench. As a result, the device's main blocking junction is now regulated fully by the potential drop between the drain and source (rather than the gate). This modification reduces C_{gd} by an order of magnitude and at the same time increases C_{gs}, thereby providing improved resistance to parasitic turn-on due to high dV_{ds}/dt during switching. Nevertheless, similarly to the original structure (figure 1(a)), this topology will also suffer from the above problems of a high off-state field in the oxide and accumulation of holes in the fin, as a result of the lack of protection to the oxide.

An alternative design, which can resolve these issues, can be obtained from the previous FinFET designs by implanting a protective p-shield below each trench and connecting it to the source's potential. As discussed in section 3, the peak electric field of this design is now shifted to the p–n junction (away from the oxide), thereby alleviating the reliability problems during the off-state. At the same time, this design maintains the lower C_{gd} of the split-gate thanks to the fact that the p-shield is grounded (figure 11). Nonetheless, an implementation of this topology will pose greater requirements on the design of the layout, so as to connect the p-shield to the source. In order to properly bias the p-shield in each region of the active area (and also reduce the source contact resistance), it may be needed to employ an interdigitated design [24]. The reduction of the channel density, which would result from such a design, however, will have a limited effect on the on-state losses, since, as discussed in section 2, the channel resistance becomes less important in the (stripe) junctionless FinFET.

In order to compare the devices examined above, they are now connected in the clamped inductive switching circuit in figure 12(a). Here the diode is assumed to be ideal (from the PSPICE library), while the active area of the FinFET is set to 16 mm^2. The device is controlled via an RTZ gate drive of 15 V amplitude and 1 ns risetime through a 2 Ω gate resistor. A comparison with the switching response of a more conventional trench MOSFET (figure 12(b)) is also attempted. Here the same oxide thickness and doping profiles are used, with the sole differences being the larger cell pitch and 'fin width' (of 2 μm), the presence of a p-well (peak acceptor

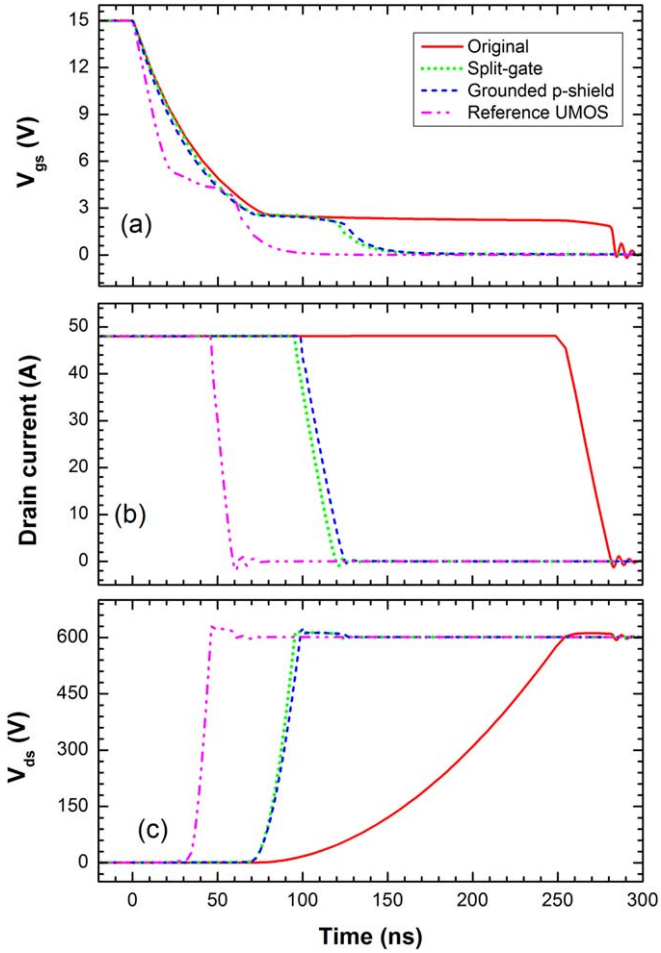

Figure 14. Turn-off characteristic of all examined structures (for an active area of 16 mm^2 and the circuit from figure 12). The split-gate and grounded p-shield FinFETs reduce the turn-off time by nearly 50% relative to the original.

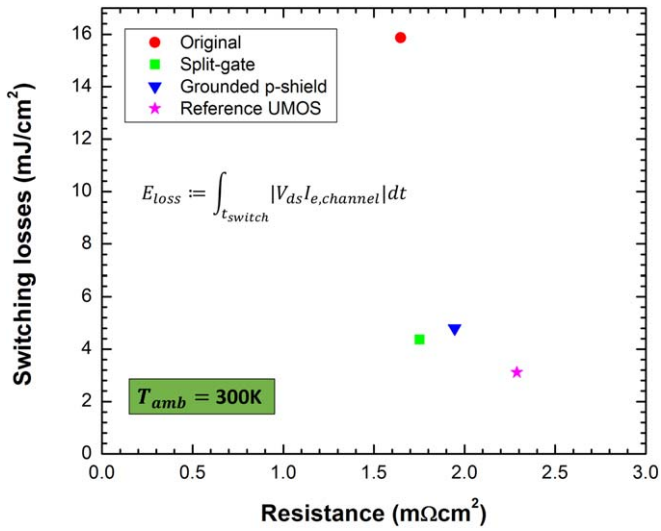

Figure 15. Total switching losses (per cycle) and R^*_{on} (at 15 V V_{gs} and 0.1 V V_{ds}) of the examined designs (t_{on} and t_{off} measure the first 95% of the risetime of V_{gs}). The more advanced FinFET structures reduce the switching losses by ~75% relative to the original design.

doping of 5×10^{17} cm^{-3}) and an n-JFET enhancement epi layer (5×10^{16} cm^{-3}), and the shallower trench depth (1 μm). A p-shield with the profile from figure 10(a) is also used to protect the bottom oxide and guarantee avalanche breakdown above 1.2 kV. Clearly, this structure is very different from the FinFETs, which is why this comparison on the switching performance is to be purely qualitative.

The resulting turn-on response of the examined structures can be seen in figure 13. During the first phase the FinFETs exhibit a comparable charging characteristic of the gate due to their similar values of the input capacitance C_{iss}. Here it should be noted that, in practice, the input RC time constant may be increased additionally by the low conductivity of the metal used for the gate contact. Nonetheless, if this issue can be neglected, the split-gate and the grounded p-shield FinFETs reach their steady on-state $V_{ds} \sim 0.5$ V earlier than the reference trench (figures 13(a)–(c)). This occurs not only due to the smaller V_{th} of the FinFETs, but also thanks to the steeper rise of the current with V_{gs}, which allows for full activation of the channel already at $V_{gs} \sim 5$ V (figure 3(b)) and hence compensates for the larger C_{gs} of the fin devices. This can also be inferred from the waveform of V_{gs} during the Miller plateau, in which time period the slope of V_{gs} is an order of magnitude smaller in the FinFETs than in the reference UMOSFET. Thus, unlike the FinFET, the conventional MOSFET requires an increasingly larger V_{gs} to further reduce the channel resistance and hence be able to carry the inductor current also at lower I_{ds} values ~ 300 A cm^{-2}. Therefore, the FinFETs may hypothetically be operated from a gate drive with a more unconventional amplitude that is less than 15 V, which can further increase the switching speed without affecting R^*_{on}. On the other hand, the original FinFET design displays by far the slowest turn-on response due to its excessively long Miller plateau. This agrees with the waveforms in figure 11, where this structure suffers from a transfer capacitance C_{rss} that is an order of magnitude larger than in the other devices.

A similar comparison can also be made at turn-off (figure 14). In this case, the reference MOSFET shows a faster (albeit still comparable) switching response than all the other FinFET structures. This occurs partially due to the higher V_{th} and the lower C_{gs} of the reference design. In addition, from the risetime of V_{ds} it is also seen that in this case the FinFETs exhibit a longer Miller plateau at turn-off than the UMOSFET. This increased C_{rss} arises from the weaker depletion of carriers at the bottom of the fin (compared to the trench MOSFET), since the protective p-shields below the trenches need to be maintained sufficiently far from the fin so as to maintain a competitive on-state resistance. Thus, in spite of the improved channel mobility, the FinFET can easily become slower than a conventional trench MOSFET (when considered as individual cells) due to the weaker depletion of free carriers and the larger C_{gs}. Nevertheless, the split-gate and the grounded p-shield topologies still achieve a competitive turn-off speed, which is $\approx 50\%$ larger than in the original FinFET design. This improvement agrees qualitatively with the results for the GaN split-gate reported in [10] and can (similarly to turn-on) be directly explained with the smaller C_{rss}.

The total losses incurred during switching (in the transistor) are now compared in figure 15. Here E_{loss} is computed using the electron current through the channel (rather than the drain current from figures 13–14), hence neglecting power dissipation due to the capacitive currents. The faster transient response (t_{switch}) of the p-shield and split-gate FinFETs reduces the losses by 75% compared to the original design, albeit at the cost of an increase in R^*_{on} of $\sim 15\%$ (in the case of the grounded p-shield FinFET). In fact, practically no current flows (at $V_{ds} = 0.1$ V), if the p-shield's half-width is increased to 0.7 μm. Thus, in this case it becomes necessary to use n-JFET enhancement doping (which, for brevity and clarity, has not been considered in this work), so as to contain the parasitic JFET effect. Despite this degradation, the grounded p-shield design still remains more attractive than the other SiC FinFETs because it does not suffer from their off-state reliability issues. On the other hand, all considered FinFET cell designs incur larger switching losses than the reference UMOSFET due to the increased C_{rss}. The performance of the split-gate and the p-shield FinFETs, however, still remains comparable to that of the trench MOSFET. At the same time, all FinFETs achieve a lower on-state resistance than the reference, thanks to the increased channel mobility. This difference will become even more significant (as a proportion of R^*_{on}) at lower V_{br} ratings. Thus, despite its intrinsically higher C_{rss}, the lower static losses of the SiC FinFET can still keep it competitive in this voltage range.

5. Conclusion

In this work the operation of the 4H-SiC junctionless FinFET has been examined for a range of cell topologies. Thanks to the use of the bulk of the fin for conduction, this device features a high channel mobility well above 100 cm^2/Vs, which reduces R^*_{on} nearly to the limit imposed by the drift and substrate regions. On the other hand, the original FinFET design proposed for GaN suffers from major reliability problems when applied to SiC, such as a low $V_{th} \sim 2$ V and a high electric field in the gate oxide, as well as a lack of a mechanism for the extraction of holes. In this context, it has been shown that the latter two issues can be resolved by means of a p-shield implanted below a portion of the trench and connected to the source. This technique can also provide for a $\sim 50\%$ increase in the turn-off speed and $\sim 75\%$ reduction of the switching losses of the device compared to the original FinFET design, at the cost of an increase of the combined drift/spreading resistance of $\approx$ 0.25 mΩ cm^2 (for a V_{br} of 1.2 kV). Thus, with further improvements that address the low threshold of this device, the junctionless FinFET can become particularly attractive for lower voltage applications.

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Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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