Turn-Off Voltage Sharing of Field-Stop IGBTs in Series Connection under Inductive Load Conditions

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Abstract – Operating Silicon (Si) Insulated Gate Bipolar Transistors (IGBTs) in series connection is attractive to many power electronic applications, including converters, hybrid circuit breakers, etc. To operate IGBTs in series connection, regulating the voltage sharing between the IGBTs during the IGBT turn-off is essential.

The objective of this thesis is to explore practical and efficient methods at IGBT device level for regulating the voltage sharing of IGBTs in series connection during the IGBT turn-off under inductive load condition. The discussions in this thesis are regarding modern Field-Stop (FS) Si IGBTs which are widely adopted. The key mechanisms at IGBT device level are discussed regarding the turn-off voltage sharing of series-connected IGBTs under typical inductive load conditions. A Finite Element Method IGBT model of a 1700 V FS Si IGBT is developed, and simulations of two-in-series IGBT turn-off using this IGBT model in an inductive current commutation loop are conducted to study the effects of a few selective IGBT internal parameter variations and control errors on the turn-off voltage sharing.

Following these studies, three types of approaches from different perspectives are attempted to mitigate the turn-off voltage divergence of series-connected IGBTs. For a passive approach, a few selective adjustments to IGBT internal parameters are reviewed in simulation regarding their effects on the turn-off voltage divergence. Some of these parameter adjustments are useful for improving the basis of the turn-off voltage sharing, and appropriate application of them in combination is attractive.

Active voltage sharing regulation is essential for achieving closely matched turn-off voltage sharing of series-connected IGBTs. Regarding the direct control of IGBT gate for the voltage sharing regulation, a redesigned direct regulation method based on an Active Voltage Control (AVC) scheme is presented. This direct regulation method is based on differential regulation designed to regulate the voltage sharing as it tends to diverge. The design concept and the mechanism of this direct method is discussed, and the experimental demonstration is shown. Compared with previous relevant researches, the direct regulation method here avoids significant additional losses caused by the voltage sharing regulation process.

In addition, an external regulation method using auxiliary Silicon Carbide (SiC) Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) controlled by the AVC scheme is presented. This external regulation method is also based on differential regulation designed to regulate the voltage sharing as it tends to diverge. The design concept and the mechanism of this external method is discussed, and the experimental demonstration is shown. The response of the voltage sharing regulation is improved with the auxiliary SiC MOSFETs. Both the direct and the external regulation methods here are effective in the experiments.

The conclusions are drawn regarding the work presented in this thesis on the turn-off voltage sharing of series-connected IGBTs and its improvement and regulation. The limits in the experimental implementations here of the two voltage sharing regulation methods are discussed. Future work is suggested regarding modelling and advanced optimisation in simulation and advancing the voltage sharing regulation methods.

To my family.

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Chapter 1 Introduction

Electricity as a form of energy is essential for today's technology evolution. Electric energy is widely adopted as a practical energy medium in the conversion of different energy forms. The processing of electric power is evolving constantly. The development of power electronic technologies enables the use of switch-mode power processing on high power applications. Switch-mode power processing provides higher conversion efficiency and enhanced control flexibility and precision for high power applications at lower costs, weights, and dimensions. Advanced power electronic technologies are widely adopted in energy conversion systems of a wide power range from milliwatts to megawatts. In switch-mode power processing, power flows are directed by active switches to achieve required power delivery between power sources, energy storage components, and loads.

In actual switching mode circuits, the active switches are implemented by solid-state power semiconductor devices with actively controllable switching capabilities to control the power flows. These power semiconductor devices are normally in either the on-state or the off-state during most of a switching cycle. The characteristics of these power devices in the on-state and the off-state have strong influences on the power processing capabilities. The switching behaviours of these power devices between the on-state and the off-state are a determining aspect in the reliability, the stability, and the performance of a power electronic system. Depending on the requirements, a power electronic system may use power semiconductor devices in various combinations, e.g. IGBTs in series connection switched simultaneously.

1.1 An Introduction to Power Semiconductor Devices

In recent decades, a variety of power semiconductor devices have been developed. From Bipolar Junction Transistors (BJTs) in the late 1940s [1], [2] to Wide BandGap (WBG) power semiconductor devices [3], [4], the power ratings and the optimal switching frequencies of power semiconductor devices are improving constantly. Limited by the properties and the processing technologies of semiconductors over the years only a few types of practical power semiconductor devices have been widely adopted in power electronics.

Modern active power semiconductor devices originate from the Bipolar Junction Transistor (BJT) first introduced by J. Bardeen and W.H. Brattain in 1948 [1]. Later in 1952 the first power semiconductor rectifiers and transistors were reported by R.N. Hall [2]. Today there are two major types of commercial power semiconductor devices on the basis of active turn-off capability. The original thyristors, also known as Silicon-Controlled Rectifiers (SCRs) represent the type of switching devices without active turn-off capability. Introduced in 1956 by J.L. Moll [5], thyristors have dominated the power device market until late 1980s. They are widely adopted in high power applications of up to megawatts. To turn off the original symmetric thyristors, the thyristor current needs to be reduced below a holding current, normally by applying a reverse-biased anode-cathode voltage. Power diodes as passive devices also belong to this category. They are as important as other switching devices in power electronic systems, and modern power diode structures are highly optimised.

In power electronic systems that require both device turn-on and turn-off to be actively controllable, sometimes referred to as fully controllable, power BJTs and Gate Turn-Off (GTO) thyristors and their variants have been used since the 1980s in high power range. The first power BJT with substantial power processing capability was achieved in the 1960s [6]. Also invented in the same decade is the GTO thyristor [7]. Compared with power BJTs, GTO thyristors can easily achieve high conducting current densities with high blocking voltages. A GTO thyristor only requires a pulse of gate driving current for turn-on or turn-off, whereas a power BJT requires a continuous gate driving current in its on-state. Consequently, Si high power BJTs have been largely replaced by GTO thyristors in many power applications.

At the same current and voltage ratings, in general the on-state voltage and the gate driving current of a GTO thyristor are both higher than those of an original thyristor. Si GTO thyristors are fully controllable devices that possess the highest switchable current densities today among all the existing commercial Si power semiconductor devices with active turn-off capabilities. Improvements on the structure, the gate drive, the packaging, and the reverse conducting diode of the GTO thyristor device led to the Integrated Gate-Commutated Thyristor (IGCT). Compared with the original GTO thyristors, IGCTs have improved switching characteristics, allowing operation without dV/dt snubber at high current densities. Also, IGCTs provide reduced switching losses and external driving requirements. Featuring integrated low inductance gate drives, IGCTs are popular in MVA high voltage power applications [8].

Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) are another type of fully controllable devices introduced in 1963 [9] that first made an impact on low voltage electrical signal processing in the 1970s [10]. In 1978, devices based on the same basic principles with a significant increase in the scale, namely power MOSFETs, made a similar impact on power electronic applications. Power MOSFETs feature high static gate impedance which results in low driving power consumption for gate drives. Another advantage of power MOSFETs is rapid switching. The typical operating frequencies of power MOSFETs can be up to two orders of magnitude higher than that of GTO thyristors. The large Safe Operating Area (SOA) and the capability to withstand high dV/dt rates make power MOSFETs a desirable choice in high frequency power electronic circuits. However, as power MOSFETs are based on unipolar carrier transport, the on-state resistance increases greatly as the maximum blocking voltage increases, which limits the use of Si power MOSFETs at high voltage ratings. In general, the voltage ratings of Si power MOSFETs are below 1000 V, but commercial Silicon Carbide (SiC) power MOSFETs rated 1700 V and 225 A have appeared, e.g. Wolfspeed/Cree CAS300M17BM2.

Until early 1980s there had been two major concepts in power semiconductor devices: bipolar devices, e.g. power BJTs and GTO thyristors, and unipolar devices, e.g. power MOSFETs. These two device concepts each possess unique advantages while are subject to different drawbacks. After power MOSFETs were reported, it was realised that a proper integration of a MOSFET and a BJT will lead to a breakthrough in power semiconductor devices. The combination of the reduced on-state driving requirements and the rapid switching of power MOSFETs and the low on-state losses of BJTs was considered a great step towards the standards of ideal power semiconductor devices.

In 1983, the breakthrough was achieved with the Insulated Gate Bipolar Transistor (IGBT) reported by Baliga, the name of which was Insulated Gate Transistor at first [11]–[14]. In the same year a similar device named Conductivity-Modulated Field Effect Transistor (COMFET) was reported by Russell [15]. Since then, the ratings and the performance of IGBTs have been improved significantly. Successfully combining the advantages of power MOSFETs and power BJTs, IGBTs are now preferable in numerous high voltages, low switching frequencies and high output power electronic systems [16]–[18].

Due to the superior performance, IGBTs replaced power BJTs and are competitive with power MOSFETs, as commercial IGBTs with operating frequencies of up to 150 kHz have appeared [19]. After years of research and development, commercial IGBT modules of 6500 V and 750 A, e.g. Infineon FZ750R65KE3, 3300 V and 1500 A, e.g. Infineon FZ1500R33HE3, and 1700 V and 3600 A, e.g. Infineon FZ3600R17HE4, have appeared. Modern IGBTs are capable of challenging GTO thyristors in high power applications with their rapid switching, large Reverse Bias Safety Operating Area (RBSOA) and low driving requirements. In recent years, with the latest advancements in power semiconductor technologies, such as trench gate and Field-Stop (FS) design concepts, IGBTs have dominated medium to high voltage, medium power electronic systems, and is competitive in high voltage, high power electronic systems.

The innovations in WBG semiconductor technologies also contribute to the development of power semiconductor devices. Commercial SiC power devices are gaining popularity in 650 V to 1700 V classes, which overlap with the popular voltage classes of Si IGBTs. Compared with Si IGBTs, due to the high critical electric field of SiC, the same blocking voltage can be supported by a SiC drift region of a low thickness and a high doping concentration, which enables the use of unipolar current conduction for the on-state. As a result, SiC MOSFETs feature reduced switching losses at the same specific on-state performance due to the absence of excess carriers in the on-state. When SiC device technologies mature, SiC power devices will lead to a breakthrough in power electronics, although this is anticipated to extend over some years as in the case of Si IGBTs.

1.1.1 An Introduction to Operations of IGBTs

One of the basics in power electronics is converting electric power between various forms. Power electronic converters are versatile due to their adaptability to the changes in input conditions and output requirements. The maximum efficiency of modern power electronic converters can exceed 90% depending on the application and the operating conditions. Power electronic converters are designed to reduce internal energy losses, e.g. the operations of IGBTs in the gate voltage controlled active region of operation, where at a certain gate voltage the device current is considered to be saturated with increases in the device voltage. For a low-loss on-state, the IGBTs are in the linear region of operation, where the relation between the increases in the device voltage and the increases in the device current is near linear.

Due to diffusion, drift, and recombination of the carriers in semiconductor devices, IGBT switching does not complete instantly. Typical IGBT switching creates an overlap between high device current and high device voltage that causes significant losses, especially under inductive

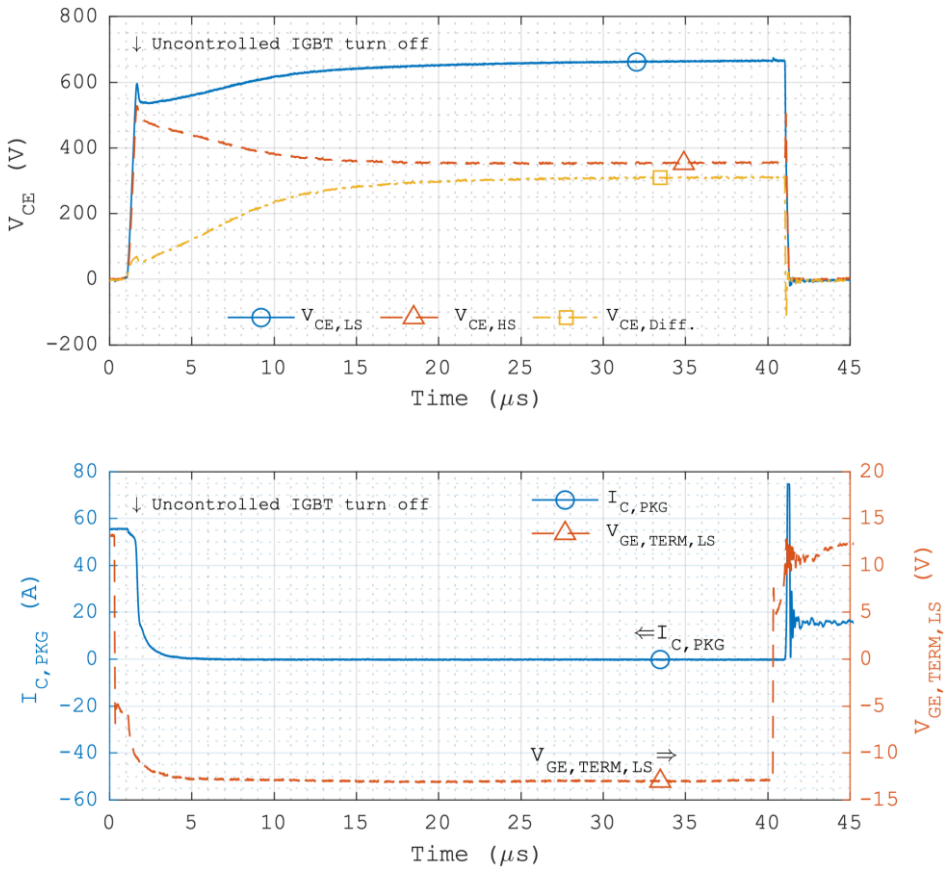


Figure 1.1: An experiment example of the uncontrolled switching of two series-connected IGBTs under inductive load condition.

load conditions which are common in power electronic converters. In inductive IGBT turn-on, the device voltage will remain at near the DC level until the device current reaches the load current. Often, a current overshoot is observed as the FreeWheeling Diode (FWD) requires reverse recovery. Similarly, in inductive IGBT turn-off, the device current will remain at near the load level until the device voltage reaches the DC level. Often, a voltage overshoot is observed due to the stray inductance in the Current Commutation Loop (CCL). An example of uncontrolled switching of two FS IGBTs in series connection under inductive load condition is shown in Figure 1.1 with diverged voltage sharing during the turn-off, the off-state, and the turn-on. Due to the internal gate resistance inside the IGBT module, the gate-emitter voltage measured is different from that of the IGBT chip. Normally operation of IGBTs in the gate voltage controlled active region is only expected in switching events.

1.1.2 General Limits in Commercial Si IGBTs

Until 2016, commercial IGBTs are Si based and are subject to compromises between fabrication cost and multiple performance aspects arising from the limits in Si properties. For Si IGBTs, a higher voltage rating will result in a higher on-state voltage at a given current density. Reducing the on-state voltage at a certain voltage rating can be achieved by increasing the on-state excess carrier concentration, which will reduce the turn-off speed and increase the turn-off losses.

For Si IGBTs, to achieve a forward-blocking voltage of 5 kV, the theoretical maximum operating frequency will be limited to 500 Hz, and to achieve a forward-blocking voltage of 10 kV, the theoretical maximum operating frequency will be further limited to 230 Hz [17]. An

alternative approach for reducing the on-state voltage is increasing the IGBT active chip area. As the current density is reduced, the on-state voltage at a given load current decreases. But with the increased active chip area the fabrication cost to achieve a given current rating increases.

The pursuit for the ideal power semiconductor device has inspired many innovations in power semiconductor technologies. Still, modern commercial power semiconductor devices are subject to compromises between performance, fabrication, and cost. To fulfil the requirements of high-power converters, semiconductor chips and devices are often operated together. Multiple chips are often connected in parallel in a package to provide a high current rating. Several devices are operated in parallel for a load current beyond the highest current rating provided in a product line. Most modern IGBTs have positive temperature coefficient of resistance that is favourable for parallel on-state current sharing. Still, current sharing between chips and devices needs careful attention, especially in switching events.

Similarly, to support a high DC link voltage, IGBTs are often operated in series connection, although the form of the series connection varies. The uncontrolled switching of IGBTs in series connection with evenly distributed voltage sharing between the IGBTs is challenging under practical conditions. The inevitable variations in device parameters and control errors can cause large divergence in the voltage sharing. Snubbers can limit the voltage divergence at the cost of additional switching losses. Nonetheless, large numbers of series-connected thyristors have been in use for many years with the assistance of snubbers.

Appropriate active feedback control on IGBTs can also regulate the turn-off voltage sharing of IGBTs in series connection. Although offering an improved trade-off between voltage regulation effects and additional losses, the implementation of such active feedback control can be sophisticated.

1.2 An Introduction to the Relevant Basics of Si IGBT Physics

An introduction to the relevant basics of Si IGBT physics is essential to establish an understanding of the turn-off voltage sharing between Si IGBTs in series connection. Here for Si IGBTs with large cell dimensions, magnetic effects, differences between carrier temperature and lattice temperature, and ultra-short distance effects are not considered. Also, IGBT physics that are irrelevant to the concerned topics of this thesis are not included.

It is also reasonable to assume that IGBTs of the same model are operated in series connection, where differences between the IGBT devices accumulated in the manufacturing processes that affect the turn-off V_{CE} sharing are of small degrees. The following IGBT physics are intended for a general understanding rather than detailed modelling.

1.2.1 Intrinsic Carrier Concentration

Intrinsic carriers exist in silicon semiconductor material due to thermal generation. The concentration of the intrinsic carriers is determined by the energy bandgap E_G and the density of states in the conduction band N_C and the valence band N_V [20]–[22]:

$$n_i = \sqrt{np} = \sqrt{N_C N_V} \exp\left(-\frac{E_G}{2kT}\right) \qquad \text{Equation 1.1}$$

where k is the Boltzmann's constant 1.38×10^{-23} J/K, T is the absolute temperature. In silicon, an expression of the n_i of Si with good agreement near 300 K is [21], [23]:

$$n_i = 9.15\times10^{19}(T/300)^2\exp\left(-\frac{6880}{T}\right)\ cm^{-3} \qquad \text{Equation 1.2}$$

1.2.2 Impact Ionisation Coefficients

Impact ionisation is related to the carrier generation by high electric fields in semiconductors, e.g. in the depletion region of an IGBT with a high V_{CE}. The impact ionisation coefficient for electrons (α_n) or holes (α_p) is defined as the number of electron-hole pairs created by an electron or a hole traversing 1 cm in the depletion region along the direction of the electric field. In Si the impact ionisation coefficients satisfy Chynoweth's Law [24]:

$$\alpha = a_\infty \mathrm{e}^{-b/E} \qquad \text{Equation 1.3}$$

where E is the electric field component in the direction of current flow, with separate parameters for electrons and holes around the room temperature [25]:

	a_∞ (cm^{-1})	b (V/cm)	Condition
Electrons	7.03×10^5	1.231×10^6	1.75×10^5 V·cm^{-1} ≤ E ≤ 6.0×10^5 V·cm^{-1}
Holes	1.582×10^6	2.036×10^6	1.75×10^5 V·cm^{-1} ≤ E ≤ 4.0×10^5 V·cm^{-1}
	6.71×10^5	1.693×10^6	4.0×10^5 V·cm^{-1} ≤ E ≤ 6.0×10^5 V·cm^{-1}

a_∞ is relatively constant with temperature [26], [27]. For electrons $\mathrm{d}b_n/\mathrm{d}T \approx 1.3\times10^3$ cm/V°K, and for holes $\mathrm{d}b_p/\mathrm{d}T \approx 1.1\times10^3$ cm/V°K [26].

1.2.3 Carrier Mobility

Here, only conductivity carrier mobility is considered for the scope of Si power devices. In general, carrier drift velocity is related to electric field and scattering. Carrier drift velocity increases until scattering occurs, which is between carriers and lattices, ionised dopants, or other free carriers [22], [28], [29]. Carrier mobility μ is defined as the coefficient that relates the electric field E to the average carrier drift velocity v_d [22], [30]:

$$v_d = \mu E \qquad \text{Equation 1.4}$$

The average carrier drift velocity saturates at high electric fields in silicon, often expressed as [22], [30], [31]:

$$v_d = v_m \frac{E/E_c}{[1+(E/E_c)^\beta]^{1/\beta}} \qquad \text{Equation 1.5}$$

with separate parameters including temperature dependences for electrons and holes [31], [32], for $T \geq 250$ K:

	v_m (cm/s)	E_c (V/cm)	β
Electrons	$1.43\times10^9\times T^{-0.87}$	$1.01\times T^{1.55}$	$2.57\times10^{-2}\times T^{0.66}$
Holes	$1.62\times10^8\times T^{-0.52}$	$1.24\times T^{1.68}$	$0.46\times T^{0.17}$

The saturation drift velocity is virtually independent of doping concentration [22], [33]. The electric field dependence of carrier mobility can be derived from Equation 1.5 [30]:

$$\mu = \frac{v_m/E_c}{[1+(E/E_c)^\beta]^{1/\beta}} = \frac{\mu_0}{[1+(E/E_c)^\beta]^{1/\beta}} \qquad \text{Equation 1.6}$$

where μ_0 is the low field carrier mobility.

In typical operating temperatures of Si IGBTs, e.g. -40 to 175 °C, the low-field carrier mobility μ_0 in silicon decreases with temperature [22], [28], [29], [31]. The temperature dependence of the low-field carrier mobility is expressed in [31] as:

$$\mu = AT^{-\gamma} \qquad \text{Equation 1.7}$$

with separate parameters for electrons and holes:

	A (cm^2K^{γ}/Vs)	γ
Electrons	1.43×10^{9}	2.42
Holes	1.35×10^{8}	2.20

which agrees with the temperature dependence in Equation 1.5.

Low-field carrier mobility is related to doping concentration [28], [30], [31], [34]. The doping dependence of low-field carrier mobility at 300 K is expressed in [28], [34] as:

$$\mu = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + (N/C_r)^{\alpha}} - \frac{\mu_1}{1 + (C_s/N)^{\beta}} \qquad \text{Equation 1.8}$$

where N is the doping concentration, with separate parameters for electrons and holes:

	μ_{min} ($cm^2V^{-1}s^{-1}$)	μ_{max} ($cm^2V^{-1}s^{-1}$)	μ_1 ($cm^2V^{-1}s^{-1}$)	C_r (cm^{-3})	C_s (cm^{-3})	α	β
Electrons	68.5	1414	56.1	9.20×10^{16}	3.41×10^{20}	0.711	1.98
Holes	44.9	470.5	29.0	2.23×10^{17}	6.10×10^{20}	0.719	2.00

The dependence of carrier mobility on carrier-carrier scattering becomes significant at high carrier concentrations, e.g. in an IGBT N-drift region under high-level injection where the minority carrier concentration exceeds the doping concentration. The carrier concentration dependence of low-field carrier mobility is expressed in [35]–[37] as:

$$\mu = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + (N/C_r)^{\alpha}} - \frac{\mu_1}{1 + (C_s/N)^{\beta}} \qquad \text{Equation 1.9}$$

The carrier mobility in an inversion layer close to the oxide-semiconductor interface, e.g. a MOS channel, in Si IGBTs and MOSFETs is related to surface scattering, including phonon scattering, Coulomb scattering, and surface roughness scattering [38], [39]. As will be discussed later, here the use of a small gate resistance is assumed for the concerned IGBT turn-off in this thesis, which results in an IGBT MOS channel cut-off very early in the fast V_{CE} rising. And since an IGBT MOS channel in a typical on-state is in the linear region of operation, the surface scattering related to an IGBT MOS channel is less relevant to the topics in this thesis and hence will not be discussed in further detail here.

1.2.4 Carrier Recombination and Recombination Lifetime

In the bulk of a semiconductor under non-equilibrium condition, i.e. $pn \neq n_i^2$ where p and n are the hole and the electron concentrations, respectively, recombination where $pn > n_i^2$ and thermal generation where $pn < n_i^2$ tend to restore the carrier state back to equilibrium. Si IGBTs are designed to achieve high-level injection in the N base, where in typical operation excess carriers exist in the on-state before turn-off. Hence, in inductive IGBT turn-off, carrier recombination is a major process to consider. Since Si is an indirect-bandgap semiconductor, the carrier recombination processes to consider for Si IGBT turn-off are Shockley-Read-Hall (SRH)

recombination and Auger recombination [29], [40]–[42]. Here, the effective recombination lifetime τ_{eff} as a combination of the SRH recombination lifetime τ_{SRH} and the Auger recombination lifetime τ_{Auger} is given by [42], [43]:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{Auger}} \quad \text{Equation 1.10}$$

1.2.4.1 Shockley-Read-Hall Recombination

In Si as an indirect-bandgap semiconductor, indirect carrier recombination and generation via bulk traps are important carrier transition processes. The single-level recombination involves electron capture and hole capture, and was first described by Shockley and Read [44], and by Hall [45] (SRH), usually referred to as SRH recombination. The net SRH recombination rate U in steady state is described in the general form of [44]–[46]:

$$U = \frac{pn - n_i^2}{\tau_p\left(n + n_i \exp\left(\frac{E_t - E_i}{kT}\right)\right) + \tau_n\left(p + n_i \exp\left(\frac{E_i - E_t}{kT}\right)\right)} \quad \text{Equation 1.11}$$

where p is the hole concentration, n is the electron concentration, τ_p is the low-level hole lifetime in heavily doped N-type silicon, τ_n is the low-level electron lifetime in heavily doped P-type silicon, E_t is the trap energy level, and E_i is the intrinsic Fermi level. The τ_n and τ_p are dependent on the doping concentration N [47]–[49], described in [49] as:

$$\tau_n = \frac{\tau_{n0}}{1 + \frac{N}{N_{ref}}} \quad \text{Equation 1.12}$$

$$\tau_p = \frac{\tau_{p0}}{1 + \frac{N}{N_{ref}}} \quad \text{Equation 1.13}$$

where $\tau_{n0} = 30$ µs is the low-concentration electron lifetime, $\tau_{p0} = 10$ µs is the low-concentration hole lifetime, and $N_{ref} = 10^{17}$ cm^{-3} is the reference roll-off concentration.

The N$^-$ drift region and the N buffer region in a modern FS IGBT in a typical on-state are under high-level injection, where the excess electron and hole concentrations δn and δp, respectively, satisfy $\delta n \approx \delta p > N_D > n_i$, where N_D is the N-type doping concentration. As $n = n_0 + \delta n$ and $p = p_0 + \delta p$ where n_0 and p_0 are the equilibrium electron and hole concentrations, respectively, the SRH lifetime under high-level injection becomes [43], [44]:

$$\tau_{SRH} = \frac{\delta n}{U} \approx \frac{\tau_p\left(n_0 + \delta n + n_i \exp\left(\frac{E_t - E_i}{kT}\right)\right) + \tau_n\left(p_0 + \delta p + n_i \exp\left(\frac{E_i - E_t}{kT}\right)\right)}{n_0 + p_0 + \delta n} \quad \text{Equation 1.14}$$

Assuming E_t is near E_i, the high-level SRH lifetime $\tau_{SRH,HL}$ approximates [43]:

$$\tau_{SRH,HL} \approx \tau_n + \tau_p \quad \text{Equation 1.15}$$

1.2.4.2 Auger Recombination

In Si regions where the carrier concentration is high, a three-particle carrier transition process, Auger recombination, is important in addition to the SRH recombination. Auger recombination is a band-to-band process that transfers the excess energy from the recombination process to a third free electron, the e-e-h process, or hole, the e-h-h process [50]–[55]. Traditional modelling of the Auger recombination rate is $R_{eeh} = C_n n^2 p$ for the e-e-h process and $R_{ehh} = C_p n p^2$ for the e-

h-h process, where C_n and C_p are the respective Auger recombination coefficients [51], [54], [55]. Therefore, the total Auger recombination rate R_{Auger} in [51], [54], [55] is given by:

$$R_{Auger} = R_{eeh} + R_{ehh} = C_n n^2 p + C_p n p^2 \quad \text{Equation 1.16}$$

Under low-level injection, the Auger recombination lifetimes in [54], [55] are given by, for N-type silicon:

$$\tau_{Auger,n,LL} = \frac{1}{C_{n,LL} N_D^2} \quad \text{Equation 1.17}$$

and for P-type silicon:

$$\tau_{Auger,p,LL} = \frac{1}{C_{p,LL} N_A^2} \quad \text{Equation 1.18}$$

where $C_{n,LL}$ and $C_{p,LL}$ are the low-level Auger recombination coefficients for electrons and holes, respectively, N_D and N_A are the doping concentrations of N-type and P-type silicon, respectively. For doping concentrations higher than 2×10^{18} cm^{-3}, at T = 300 K, $C_{n,LL} = 2.8\times10^{-31}$ cm^{6}s^{-1} and $C_{p,LL} = 9.9\times10^{-32}$ cm^{6}s^{-1} as in [51]. $C_{n,LL}$ and $C_{p,LL}$ have weak dependences on temperature [51], and vary as $T^{0.6}$ between 195 and 372 K as in [56]. Under high-level injection, the Auger recombination lifetime in [54], [55] is given by, assuming $\delta n \approx \delta p$:

$$\tau_{Auger,HL} = \frac{1}{C_a \delta n^2} \quad \text{Equation 1.19}$$

where C_a is the ambipolar Auger recombination coefficient. For δn between 1×10^{15} to 2×10^{17} cm^{-3}, $C_a = 1.66\times10^{-30}$ cm^{6}s^{-1} as in [57].

From Equation 1.16, $C_a \equiv C_n + C_p$, however, the measurement of C_a reveals that C_a is generally higher than ($C_{n,LL} + C_{p,LL}$) [54], [55]. The transition of the Auger recombination coefficients in Equation 1.16 from low-level to high-level is approximated in [54] by:

$$C_{n,eff} = C_{n,LL}\left(\frac{N_D}{N_D + p}\right) + \frac{C_a}{2}\left(\frac{p}{N_D + p}\right) \quad \text{Equation 1.20}$$

$$C_{p,eff} = C_{p,LL}\left(\frac{N_A}{N_A + n}\right) + \frac{C_a}{2}\left(\frac{n}{N_A + n}\right) \quad \text{Equation 1.21}$$

where $C_{n,eff}$ and $C_{p,eff}$ are the effective Auger recombination coefficients to replace the respective C_n and C_p in Equation 1.16.

1.2.5 Basic Equations for Si Power Devices

The equations included here for Si power devices describes the basics of the internal physics relevant to the low-loss turn-off of modern IGBTs under typical operating conditions.

In Maxwell's equations, the differential form of Gauss's law, Poisson's equation, is useful for describing the electric field distribution:

$$\nabla \cdot \vec{E} = \frac{\rho}{\varepsilon_s} \quad \text{Equation 1.22}$$

where E is the electric field, ρ is the total charge density, ε_s is the permittivity of a semiconductor. In some high voltage vertical Si power devices, such as Si IGBTs, the bulk regions feature uniform horizontal doping profiles and a total thickness considerably greater than the scale of

the cell pitch, for which some analyses can be simplified to One-Dimensional (1D) problems. In these cases, Equation 1.22 can be reduced to:

$$\nabla \cdot \vec{E} = \frac{\partial \vec{E}}{\partial x} = \frac{\rho}{\varepsilon_s} = \frac{q(p - n + N_D - N_A)}{\varepsilon_s} \quad \text{Equation 1.23}$$

where x is the distance, q is the elementary charge, p and n are the hole and electron concentrations, respectively, N_D and N_A are the donor and acceptor doping concentrations, respectively.

The steady state conducting current can be approximated by a combination of the drift current due to the electric field and the diffusion current due to the carrier concentration gradient, for electrons and holes [22], [31], [58]:

$$\overrightarrow{J_n} = qn(\mu_n \vec{E}) + qD_n \nabla n \quad \text{Equation 1.24}$$

$$\overrightarrow{J_p} = qp(\mu_p \vec{E}) - qD_p \nabla p \quad \text{Equation 1.25}$$

where $\overrightarrow{J_n}$ and $\overrightarrow{J_p}$ are the electron and hole current densities, respectively, $D_n = (kT/q)\mu_n$ and $D_p = (kT/q)\mu_p$ are the electron and hole diffusion coefficients, respectively, both given by Einstein relation. $\mu_n \vec{E}$ and $\mu_p \vec{E}$ yield the respective electron and hole drift velocities, which saturate at high electric fields with quantitative reductions in μ_n and μ_p. For 1D problems, Equation 1.24 and Equation 1.25 can be reduced respectively to:

$$\overrightarrow{J_n} = qn(\mu_n \vec{E}) + qD_n \frac{\partial n}{\partial x} = qn(\mu_n \vec{E}) + q\left(\frac{kT}{q}\mu_n\right)\frac{\partial n}{\partial x} \quad \text{Equation 1.26}$$

$$\overrightarrow{J_p} = qp(\mu_p \vec{E}) - qD_p \frac{\partial p}{\partial x} = qp(\mu_p \vec{E}) - q\left(\frac{kT}{q}\mu_p\right)\frac{\partial p}{\partial x} \quad \text{Equation 1.27}$$

Due to charge conservation, the net changes in the carrier concentrations are related to the carrier generation and recombination and the current densities, expressed by the continuity equations for electrons and holes [22], [58]:

$$\frac{\partial n}{\partial t} = (G_n - U_n) + \frac{1}{q}\nabla \cdot \overrightarrow{J_n} \quad \text{Equation 1.28}$$

$$\frac{\partial p}{\partial t} = (G_p - U_p) - \frac{1}{q}\nabla \cdot \overrightarrow{J_p} \quad \text{Equation 1.29}$$

where G_n and G_p are the respective electron and hole generation rates, U_n and U_p are the respective electron and hole recombination rates. For 1D problems, Equation 1.28 and Equation 1.29 can be reduced respectively to:

$$\frac{\partial n}{\partial t} = (G_n - U_n) + \frac{1}{q}\frac{\partial \overrightarrow{J_n}}{\partial x} \quad \text{Equation 1.30}$$

$$\frac{\partial p}{\partial t} = (G_p - U_p) - \frac{1}{q}\frac{\partial \overrightarrow{J_p}}{\partial x} \quad \text{Equation 1.31}$$

1.3 Introduction to IGBT Structural Components

High voltage Si IGBTs are normally vertical n-channel devices. Such an IGBT can be considered as an integration of a PNP BJT and a n-channel MOSFET that characterises the typical IGBT performance [59]. The semiconductor relevant contents in this thesis are limited to the scope of modern Field-Stop (FS) n-channel vertical Si IGBTs. The schematic diagrams shown in this thesis are not to scale.

Historically, the naming "collector" and "emitter" of the current conducting terminals of an IGBT was for the compatibility of IGBTs with power BJT circuits when IGBTs were first introduced [16]. The collector and the emitter of the equivalent BJT in an IGBT do not refer respectively to the "collector" and the "emitter" terminals of the IGBT.

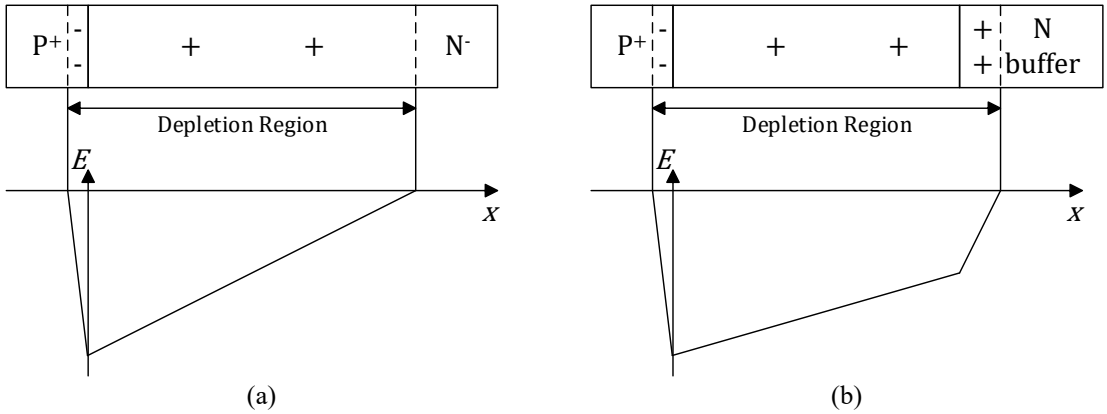
1.3.1 PN Junction and Depletion Region

A basic PN junction consists of a P-type region and a N-type region adjacent to each other. In Si IGBTs, reverse biased PN junctions are used to block high voltages. High voltage n-channel IGBTs feature lightly doped N^- drift regions. In such an IGBT, this N^- drift region forms a P^+/N^- junction with the heavily doped P base region, also referred to as the P body region. When this P^+/N^- junction is reverse biased, the depletion region is distributed mostly in the lightly doped N^- drift region according to Equation 1.23, as illustrated by the 1D schematic diagram in Figure 1.2 (a). Therefore, in an IGBT a forward-blocking C-E voltage V_{CE} is supported mostly in the N^- drift region, in which case the P^+/N^- junction can be considered as an abrupt PN junction. For the depletion region in the N^- drift region, the 1D Poisson's equation can be reduced to:

$$-\frac{\partial^2 v}{\partial x^2} = \frac{\partial \vec{E}}{\partial x} = \frac{\rho}{\varepsilon_s} = \frac{q(p - n + N_D)}{\varepsilon_s} \qquad \text{Equation 1.32}$$

where for a n-channel IGBT in a forward-blocking state, p is related to the hole current in the depletion region and n is related to the electron current in the depletion region.

Field-Stop (FS) IGBT design and similar design concepts such as Soft Punch-Through and Light Punch-Through are widely adopted in modern IGBTs [59]–[62]. In general, these IGBT design concepts feature a N buffer of a doping concentration higher than that of the N^- drift region that only stops the electric field in the depletion region from reaching the vicinity of the backside P emitter. The schematic diagram in Figure 1.2 (b) illustrates a such reverse biased P^+/N junction with a N buffer where the electric field in the depletion region is stopped by the N buffer. Equation 1.32 also applies to the depletion region in the N-type region here. FS IGBTs achieve reduced device thicknesses and conducting losses while achieving reduced switching losses due to the reduced on-state excess carriers in the N bulk regions [59].



(a) (b)

Figure 1.2: Schematic diagrams of (a) a reverse biased P^+/N^- junction and (b) a reverse biased P^+/N^- junction with the electric field "stopped" by a N buffer.

1.3.2 Power BJT

A basic n-channel IGBT includes a PNPN structure, in which the PNP component forms an equivalent BJT with the base current provided by the MOS channel in the IGBT. In normal operation, a BJT is fully controllable by the base current I_B. Regarding the general doping profile, a basic BJT consists of a NPN or PNP structure. Schematic diagrams of a NPN BJT and a PNP BJT are shown in Figure 1.3 (a) and (b), respectively.

Regarding the basic operations of power BJTs, the following discussion considers a basic PNP power BJT, the same basic type as the equivalent PNP BJT in a n-channel IGBT, and only major carrier transport mechanisms. Complementary conclusions are applicable to NPN power BJTs. Under normal forward voltage blocking, the collector-base junction is reverse-biased, and the depletion region is distributed mostly in the wide/thick and lightly doped collector region. In a basic PNP power BJT, when the P^+ emitter to N base junction is forward-biased, electrons diffuse from the N base into the P^+ emitter and holes are injected from the P^+ emitter into the N base. Referring to the directions in Figure 1.3 (b), in a typical PNP power BJT the N base is narrow/thin so that the majority of the injected holes diffuse through the N base and are collected by the P collector, while only a small proportion of the injected holes recombine in the N base.

Referring to the directions in Figure 1.3, in a typical power BJT the collector region is normally wide/thick while the base region is narrow/thin. However, in a n-channel IGBT the equivalent PNP BJT has a narrow/thin P^+ collector region and a wide/thick N^- base region. This difference is shown in the respective schematic diagrams in Figure 1.4.

Power BJTs normally function as power switches in dedicated power BJT circuits. The design and the operation of power BJTs are for reducing operating losses while providing high voltage and current ratings, which are significantly different from those of signal BJTs. To reduce on-state losses, conductivity modulation by high-level injection is applied to the lightly

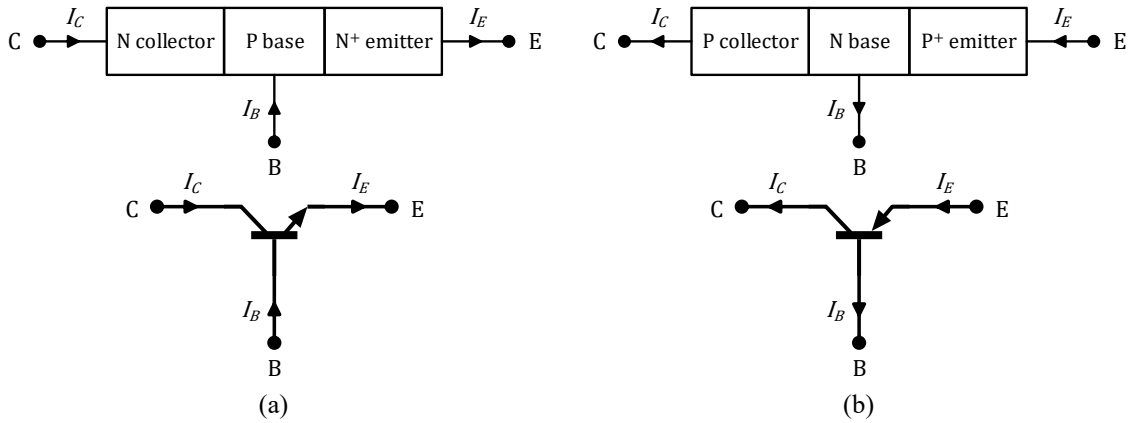


Figure 1.3: Schematic diagrams of (a) a basic NPN BJT and (b) a basic PNP BJT.

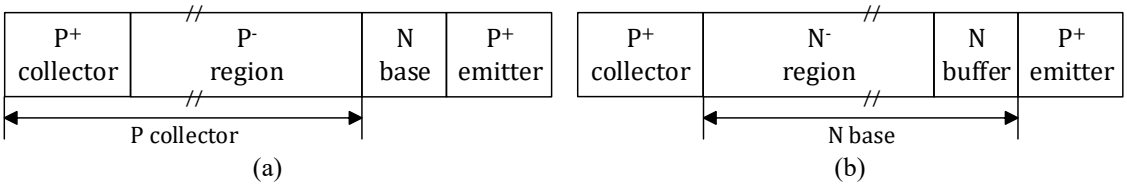


Figure 1.4: Schematic diagrams of (a) a basic PNP power BJT and (b) the equivalent PNP BJT in a n-channel IGBT.

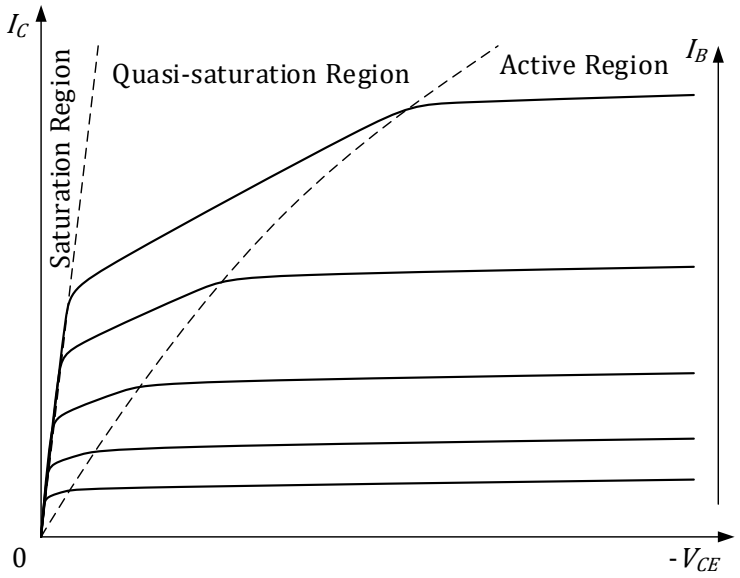


Figure 1.5: Schematic diagram of basic DC *I-V* characteristics of a NPN power BJT.

doped regions of a power BJT. For a forward conducting power BJT, its operation modes include active mode, quasi-saturation mode, and saturation mode, as indicated in the schematic diagram of the basic DC *I-V* characteristics of a PNP power BJT shown in Figure 1.5. Breakdown characteristics are not included in Figure 1.5.

In the active mode, the emitter-base junction is forward-biased while the collector-base junction is reverse-biased. A depletion region is formed across the reverse-biased collector-base junction. In static or quasi-static situation, at a certain collector-emitter voltage V_{CE}, the collector current I_C increases with the base current I_B.

In the quasi-saturation mode, the emitter-base and the collector-base junctions are both forward-biased. Part of the lightly doped collector region near the collector-base junction, i.e. part of the P^- region near the P^-/N-base junction in Figure 1.4 (a), is under high-level injection and is conductivity-modulated as the conductivity is increased. Depending on the doping profile, the base region may not be entirely under high-level injection. At a given V_{CE}, the I_C increases with the I_B, and at a given I_B, the I_C increases with the V_{CE}.

In the saturation mode, both the emitter-base and the collector-base junctions are forward-biased. The entire lightly doped collector region, i.e. the P^- region in Figure 1.4 (a), is under high-level injection and is conductivity-modulated. Often, the base region is also under high-level injection. The I_C increases with the V_{CE} at a higher rate compare with that in the quasi-saturation mode at the same I_B.

For a typical power BJT in forward conducting state considering only major current components, the I_C is related to the I_B by the common-emitter current gain h_{FE}:

$$h_{FE} = \frac{I_C}{I_B} \qquad \text{Equation 1.33}$$

In normal DC situations, the h_{FE} is dependent on the I_C. At a very low I_C where the emitter-base recombination current is comparable to the effective emitter diffusion current through the base, the h_{FE} is relatively low and increases with the I_C. However, at a higher I_B where the base

becomes under high-level injection, e.g. in the quasi-saturation and saturation modes, the h_{FE} decreases with the I_C due to the increase in the effective base doping level and the extension of the electrical base caused by the injected high-level excess carriers. Also, in general, h_{FE} decreases with the effective base width/thickness [22], [63]–[68].

For the equivalent PNP BJT in a n-channel IGBT, in forward conducting state its wide/thick N base under high-level injection results in a low h_{FE}. Due to the significant differences in device geometry between a typical PNP power BJT and a n-channel IGBT, the on-state carrier distribution of the equivalent PNP BJT in a n-channel IGBT will be discussed separately.

1.3.3 Power MOSFET

A basic n-channel IGBT includes a n-channel MOSFET structure. Since modern high voltage IGBTs are mostly n-channel devices, the following discussions considers a basic n-channel power MOSFET and only major carrier transport mechanisms. Complementary conclusions are applicable to p-channel devices. Schematic diagrams of basic 2D vertical n-channel planar-gate and trench-gate power MOSFETs are shown in Figure 1.6 (a) and (b), respectively, in the form of half-cell vertical cross-sections. Normally, under forward voltage blocking, the N-drift region to P base junction is reverse-biased, and the depletion region is distributed mostly in the thick and lightly doped N-drift region.

MOSFETs are unipolar devices without conductivity modulation by high-level injection in the on-state. In normal operation, MOSFETs are fully controllable by the gate-source voltage V_{GS}. The current conduction in a MOSFET is controlled by a MOS channel formed by an inversion layer. The n-type MOS channels, n-channels, in power MOSFETs or IGBTs are mostly surface inversion channels formed by electrons. The basic principles of MOS channels are the same for planar-gate and trench-gate devices.

In a n-channel MOSFET, when the gate-source voltage V_{GS} exceeds the threshold voltage V_{TH}, electrons from the semiconductor regions are attracted towards the interface between the

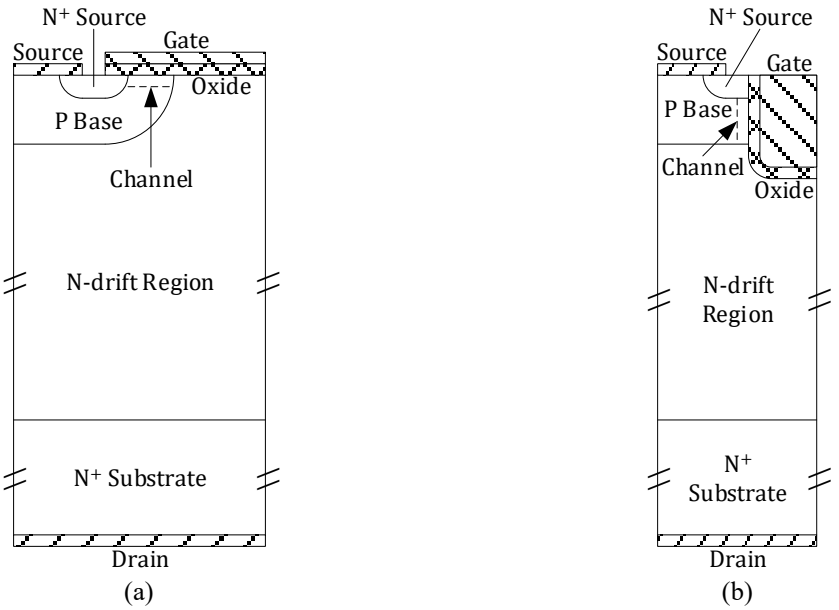


Figure 1.6: Schematic diagrams of (a) a basic vertical n-channel planar power MOSFET and (b) a basic vertical n-channel trench power MOSFET.

gate oxide and the semiconductor region, and an inversion layer of electrons is formed in the P base adjacent to the gate oxide. With positive drain-source voltage V_{DS}, electrons from the N^+ source flow through a MOS channel in the P base formed by that inversion layer and into the N-drift region. The electrons through the MOS channel spread across the width of the N-drift region and flow towards the drain terminal.

In the general scope of vertical power MOSFETs and IGBTs, a trench MOS gate provides direct access to the bulk regions for the electrons through the vertical MOS channel, compared with a planar MOS gate. This avoids the depletion region formed by the reverse-biased N-drift region to P base junction under a forward V_{DS}. Consequently, the reduced crowding and path length of the electrons out of the MOS channel in the MOS gate area improve the MOS channel density and the on-state resistance.

Regarding DC *I-V* characteristics, long-channel and low-field carrier mobilities are assumed for the MOS channels in n-channel power MOSFETs and IGBTs. The Shockley MOSFET model [69] is widely used in this situation [22], [70], [71]. For a n-channel power MOSFET, when the $(V_{GS} - V_{TH}) > 0$ and the $V_{DS} \ll V_{DS,sat}$, the MOS channel is nearly resistive for the MOS channel current, Figure 1.7 (a), where $V_{DS,sat}$ is the drain saturation voltage at which the drain current I_D starts to saturate to $I_{D,sat}$. This nearly resistive regime is referred to as the linear region of operation, indicated in the schematic diagram shown in Figure 1.8. The $V_{DS,sat}$ and the $I_{D,sat}$ will be discussed later.

As the V_{DS} increases and is reaching the $V_{DS,sat}$, due to the MOS channel resistance the voltage along the MOS channel increases and starts to reduce the effect of the $(V_{GS} - V_{TH})$ on inducing the inversion charges near the drain end of the MOS channel. Consequently, the inversion charges near the drain end of the MOS channel are reduced, and the I_D starts to increase sublinearly with the V_{DS}. This sublinear regime is referred to as the nonlinear region of operation, indicated in the schematic diagram shown in Figure 1.8.

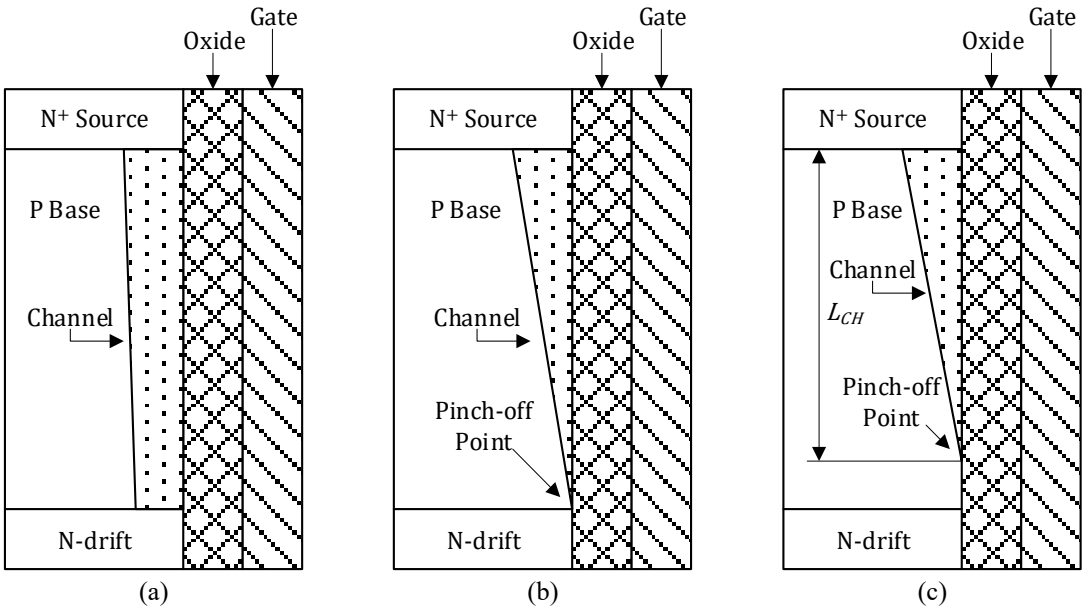


Figure 1.7: Schematic diagrams of a basic MOS channel: (a) in the linear region, (b) when $V_{DS} = V_{DS,sat}$, and (c) in the saturation region.

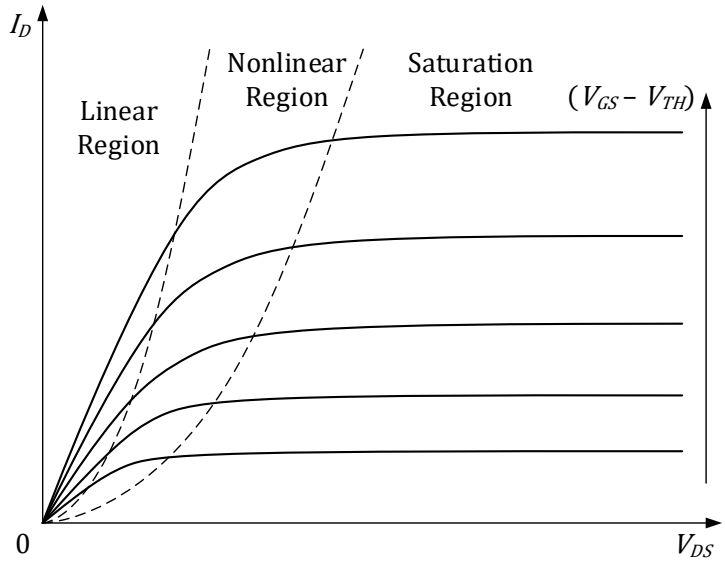


Figure 1.8: Schematic diagram of DC *I-V* characteristics of a n-channel power MOSFET.

As the V_{DS} increases to the $V_{DS,sat}$, the inversion charges are eventually reduced to near zero at the drain end of the MOS channel, where the MOS channel starts to pinch off, Figure 1.7 (b). As the V_{DS} exceeds the $V_{DS,sat}$, the pinch-off point shifts towards the source end of the MOS channel, and the effective channel length L_{CH} is reduced slightly, Figure 1.7 (c). The voltage at the pinch-off point with respect to the source remains unchanged. The additional voltage is supported by a depletion region from the pinch-off point along the MOS channel into the N-drift region, formed by the reverse-biased N-drift region to P base junction. The I_D essentially saturates with the V_{DS} to the $I_{D,sat}$, although a minor increase in the I_D may be observed due to the slightly reduced L_{CH}. This saturation regime is referred to as the saturation region of operation, indicated in the schematic diagram shown in Figure 1.8.

In the Shockley MOSFET model, the $V_{DS,sat}$ is described as:

$$V_{DS,sat} = (V_{GS} - V_{TH}) \qquad \text{Equation 1.34}$$

For a n-channel power MOSFET, Equation 1.34 is applicable to the MOS channel area. The resistance and the voltage across the bulk regions, e.g. the N-drift region and the N^+ substrate, need to be considered in determining the actual $V_{DS,sat}$.

In the saturation region where $V_{DS} \geq V_{DS,sat}$, the $I_{D,sat}$ is described as:

$$I_{D,sat} = \frac{Z}{2L_{CH}} \mu_{n,CH} C_{ox} (V_{GS} - V_{TH})^2 \qquad \text{Equation 1.35}$$

where Z is the channel width orthogonal to the cross-sections shown in Figure 1.7, $\mu_{n,CH}$ is the electron mobility in the MOS channel, and $C_{ox} = (\varepsilon_{ox}/t_{ox})$ is the gate oxide capacitance per unit area, where ε_{ox} and t_{ox} are the permittivity and the thickness of the oxide, respectively.

In the linear and the nonlinear regions where $V_{DS} < V_{DS,sat}$, the I_D is described as:

$$I_D = \frac{Z}{L_{CH}} \mu_{n,CH} C_{ox} \left\{ (V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right\} \qquad \text{Equation 1.36}$$

For a n-channel MOSFET, the V_{TH} is described as:

$$V_{TH} = \phi_{MS} - \frac{Q_{ox}}{C_{ox}} + \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) + \frac{\sqrt{4\varepsilon_S N_A kT\ln(N_A/n_i)}}{C_{ox}} \qquad \text{Equation 1.37}$$

where ϕ_{MS} is the work function difference between the gate and the semiconductor, Q_{ox} is the fixed oxide charges per unit area, N_A is the P-type doping concentration in the n-channel, and ε_s is the permittivity of the semiconductor. For Equation 1.37, $dV_{TH}/dT < 0$ for n channels [72].

1.4 An Introduction to Relevant IGBT Basics

1.4.1 High Voltage IGBT Structures

High voltage IGBTs are mostly vertical n-channel devices. Schematic diagrams of a few representative 2D vertical n-channel IGBT structures are shown in Figure 1.9. A n-channel IGBT is an integration of a n-channel MOSFET and a PNP BJT, where the MOS channel current functions as the base current of the PNP BJT structure, Figure 1.10. Compared with a vertical n-channel MOSFET, a n-channel IGBT has a P emitter layer or a P^+ substrate as the P emitter on the backside. This integration forms a PNPN structure.

Unlike the PNPN structure in a thyristor, in an IGBT to avoid the latch-up of the PNP and NPN BJTs in the PNPN structure, the NPN BJT is suppressed first by shorting its P-base and N-emitter with the "emitter" metallisation of the IGBT. Also, that P-base is small and heavily doped to avoid an excessive voltage across it that would activate the P-base/N-emitter junction of the NPN BJT in normal operation. These methods ensure that an IGBT is fully controllable by its MOS gate in normal operation.

In this thesis when referring to IGBTs, the term "P emitter" and its variants refer to the P emitter of the PNP BJT structure in a n-channel IGBT on the backside. Also, the term "N base" and its variants refer to the thick N base of the PNP BJT structure, which for an FS IGBT includes the N-drift region and the N FS buffer.

Some early n-channel IGBTs were fabricated on thick and heavily doped P^+ substrates. This P^+ substrate as the P emitter has very high injection efficiency which requires a heavily

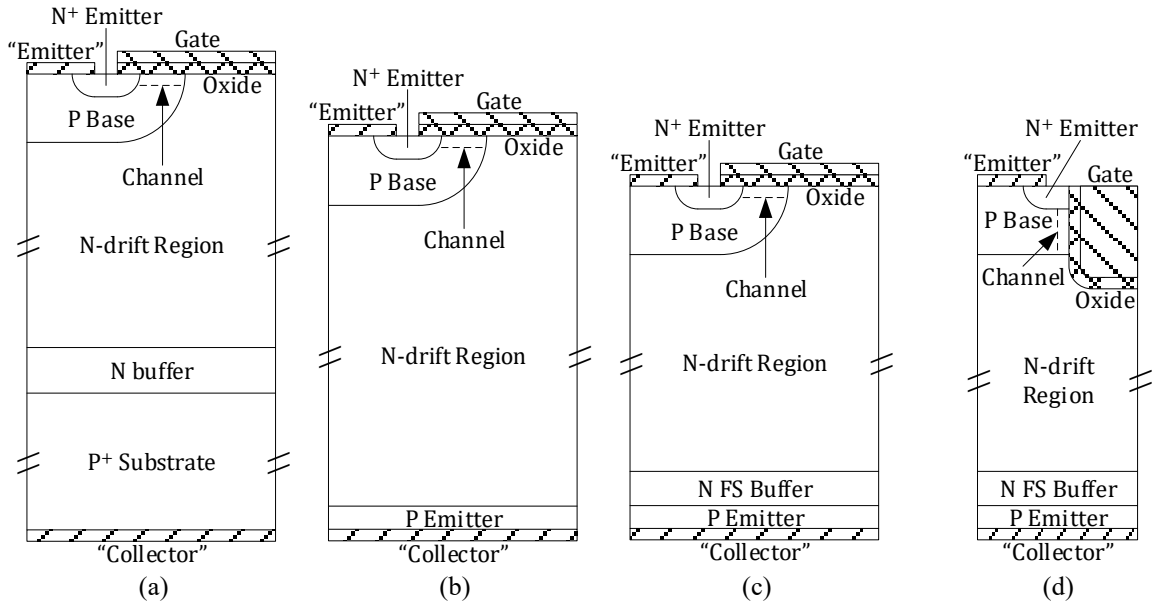


Figure 1.9: Schematic diagrams of basic vertical n-channel IGBTs: (a) a planar PT IGBT, (b) a planar NPT IGBT, (c) a planar FS IGBT, and (d) a trench FS IGBT.

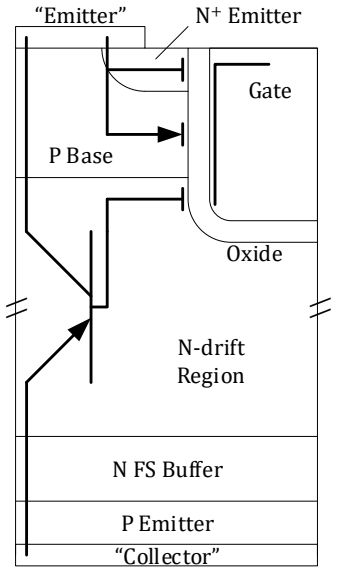


Figure 1.10: Schematic diagrams of a basic vertical n-channel trench FS IGBT.

doped N^+ buffer layer, Figure 1.9 (a), and carrier lifetime control to achieve usable switching speeds. In a forward-blocking off-state at high collector terminal to emitter terminal voltage V_{CE}, the N-drift region to P base junction is reverse-biased, and the electric field in the depletion region can punch through the N-drift region and is stopped in the N^+ buffer, resulting in a quadrilateral (1D, vertical) distribution of the electric field in the N base. IGBTs of this type are commonly referred to as Punch-Through (PT) IGBTs.

Later, the maturing of thin wafer technologies enabled the fabrication of n-channel IGBTs without P^+ substrates. The resulting IGBT has a thin P emitter with low injection efficiency, which no longer requires a N^+ buffer, Figure 1.9 (b), or carrier lifetime control for practical use. In a forward-blocking off-state, the N-drift region to P base junction is reverse-biased, and the electric field in the depletion region is designed to not punch through the N-drift region and reach the vicinity of the P emitter. IGBTs of this type are commonly referred to as Non-Punch-Through (NPT) IGBTs.

Advancing from NPT IGBTs, to reduce the thickness of the N-drift region, a lightly doped N buffer layer is implemented, Figure 1.9 (c), to achieve a quadrilateral (1D, vertical) distribution of the electric field in the depletion region in the N base at high forward-blocking V_{CE} in an off-state. This N buffer layer is designed to stop the electric field from reaching the vicinity of the P emitter without significantly reducing the injection efficiency of the P emitter [59], [60]. This lightly doped N buffer layer is often referred to as a Field-Stop (FS) layer, and IGBTs of this type are often referred to as Field-Stop (FS) IGBTs.

A comparison of the key features of the three aforementioned mainstream IGBT design concepts is shown in Table 1.1 [59]. Other commercial IGBTs that are based on essentially the same key design concept of Field-Stop IGBTs, e.g. Soft Punch-Through and Light Punch-Through IGBTs, will not be discussed separately.

Table 1.1: Comparison of key features of mainstream IGBT design concepts. © 2017 IEEE

	P emitter	N drift	N buffer	Carrier lifetimes
PT IGBT	Thick P^+ substrate, very high injection efficiency	Thin	Heavily doped, to stop the electric field and reduce the P emitter injection efficiency	Low, by carrier lifetime control
NPT IGBT	Thin, low injection efficiency	Medium	No N buffer	High, no global carrier lifetime control
FS IGBT	Thin, low injection efficiency	Thin	Lightly doped, only to stop the electric field	High, no global carrier lifetime control

In a modern FS IGBT, the doping concentration of the N FS buffer is often about one to two orders of magnitude lower than that of the P emitter [73]–[75]. As a result, the N FS buffer is also under high-level injection in a typical on-state, where the N FS buffer can be considered as part of the N base of the PNP BJT structure alongside the N-drift region.

Regarding the MOS gate structure of FS IGBTs, a trench MOS gate, Figure 1.9 (d), provides direct access to the N base for the electrons through the vertical MOS channel, compared with a planar MOS gate. This avoids the depletion region formed by the reverse-biased N-drift region to P base junction under a forward V_{CE}. Consequently, the reduced crowding and path length of the electrons out of the MOS channel in the MOS gate area improve the MOS channel density and the on-state performance.

1.4.2 Basic IGBT Operations

A basic FS IGBT only has practical forwarding blocking capability due to the N FS buffer and is normally operated with a Free-Wheeling Diode (FWD) in anti-parallel, which enables reverse current conducting and prevents excessive reverse voltage for the IGBT. At a high forward V_{CE}, the N-drift region to P base junction is reverse-biased. As previously discussed and illustrated in Figure 1.2 (b), a high forward V_{CE} is supported by a depletion region distributed mostly in the N-drift region.

Some early FS IGBTs were designed with a N-drift region of a very low doping concentration to reduce the thickness of the N-drift region and the operating losses. Such a design results in a low static punch-through voltage V_{PT}, where the V_{PT} refers to the forward static off-state V_{CE} when the depletion edge in the N base just reaches the N buffer. However, a major issue of such a low V_{PT} design is that the FS IGBT is more likely to be subject to oscillation at fast turn-off due to lack of high-level excess carriers after the depletion region reaches the N buffer [73]–[75]. Later generations of FS IGBTs greatly mitigated this issue by increasing the thickness and the doping concentration of the N-drift region to raise the V_{PT} above the typical utilisation of the V_{CE} rating in practice. This situation is assumed in this thesis.

The typical DC *I-V* characteristics of a n-channel IGBT resemble those of a n-channel power MOSFET, with the differences resulting from the P emitter of the PNP BJT structure in the IGBT. In a n-channel IGBT, when the gate-emitter voltage V_{GE} exceeds the threshold voltage V_{TH}, an inversion layer of electrons is formed in the P base adjacent to the gate oxide. With a positive V_{CE} and the P emitter to N FS buffer junction forward-biased, electrons from the N^+ emitter flow through a MOS channel in the P base formed by that inversion layer and into the N-drift region.

In a typical IGBT on-state, this electron current functions as the base current of the PNP BJT structure and induces a hole injection current from the P emitter through the N FS buffer and into the N-drift region. With a sufficient ($V_{GE} - V_{TH}$) for the voltage across the MOS channel, the MOS channel is in its linear region, and the resulting ambipolar current components in the N-drift region lead to high-level injection and conductivity modulation in it. As $p \approx n$ under high-level injection and due to the higher mobility of the electrons, the electron current via the MOS channel accounts for a higher proportion of the ambipolar current in the N-drift region.

The hole current in the N-drift region flows into the P base at the frontside and to the "emitter" terminal. Meanwhile, the electrons in the N-drift region flows into the P emitter, where the electrons diffuse into the P emitter with the electron concentration decreasing due to recombination. This operation region of an IGBT, often referred to as the saturation region in Figure 1.11, resembles the linear region of operation of a power MOSFET.

In static or quasi-static situations, when the ($V_{GE} - V_{TH}$) is inadequate for the voltage across the MOS channel, the MOS channel pinches off and the MOS channel current saturates with the V_{CE}. Since this MOS channel current functions as the base current of the equivalent PNP BJT with a very thick N base typically under high-level injection, the induced hole injection current from the P emitter also tends to saturate with the V_{CE}. Hence, the IGBT collector terminal current I_C exhibits saturation characteristics against the V_{CE}. Determined by the MOS gate structure, the I_C under channel pinch-off conditions is related to $(V_{GE} - V_{TH})^2$. With a sufficient I_C that results in high-level injection in the undepleted part of the N base, the saturated IGBT I_C can be approximated by [76]:

$$I_{C,sat} \approx \frac{I_{MOS}}{1 - \alpha_{PNP}} \propto \{C_{ox}(V_{GE} - V_{TH})^2\} \qquad \text{Equation 1.38}$$

where I_{MOS} is the MOS channel current, α_{PNP} is the common-base current gain of the PNP BJT structure, and C_{ox} is the gate oxide capacitance per unit area. This operation regime is often referred to as the V_{GE} controlled active region in Figure 1.11, and the transition region between this active region and the saturation region is often referred to as the quasi-saturation region.

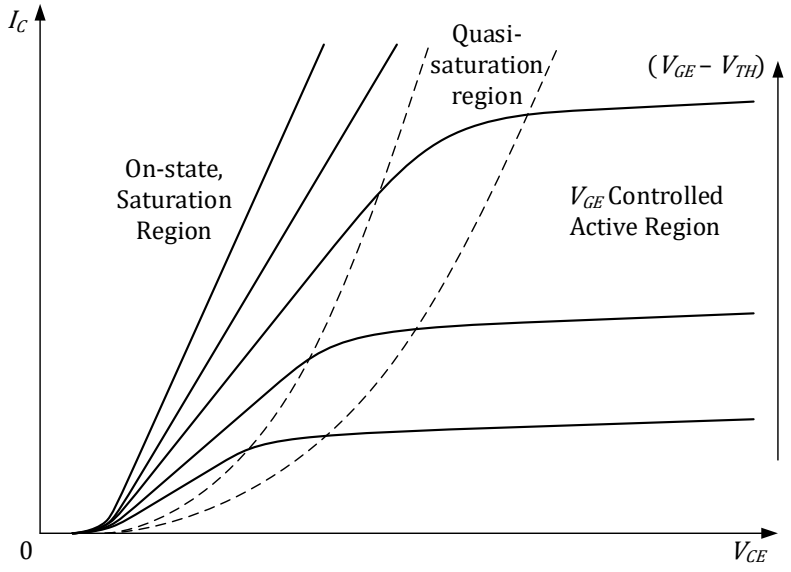


Figure 1.11: Schematic diagram of DC *I-V* characteristics of a n-channel IGBT.

The carrier transport in the IGBT N base in the transient of a fast turn-off from a typical on-state has an additional degree of freedom contributed by the high-level excess carriers. Detailed IGBT turn-off process will be discussed later.

1.4.3 High-level Injection and Ambipolar Carrier Transport

IGBTs are designed to achieve high-level injection in the N base from low current densities [76]. Under high-level injection, the concentrations of both types of carriers exceed the doping concentration. Carriers of each type attract carriers of the complementary type. The drift of electrons and holes is coupled by the same electric field [76]. As a result, the electron concentration is approximately equal to the hole concentration. In the regions under high-level injection, the electric field is referred to as the ambipolar electric field E_A and is responsible for the carrier transport and the quasi-neutrality of the net charges, $p \approx n$ [77]–[81]. The carrier transport under high-level injection is often referred to as ambipolar carrier transport, which is significantly different from the carrier transport in signal BJTs.

For the N base in a high voltage IGBT, the discussion of the carrier transport under high-level injection can be reduced to 1D situations [76]. From Equation 1.26 and Equation 1.27, the electron current I_n and the hole current I_p are described as:

$$I_n = qnA(\mu_n E) + qAD_n\frac{\partial n}{\partial x} = qnA(\mu_n E) + qA\left(\frac{kT}{q}\mu_n\right)\frac{\partial n}{\partial x} \quad \text{Equation 1.39}$$

$$I_p = qpA(\mu_p E) - qAD_p\frac{\partial p}{\partial x} = qpA(\mu_p E) - qA\left(\frac{kT}{q}\mu_p\right)\frac{\partial p}{\partial x} \quad \text{Equation 1.40}$$

where A is the IGBT active area. With $I_C = I_n + I_p$ and $n \approx p$, the I_n and I_p can be described without the electric field term [76], [77]:

$$I_n = \frac{\mu_n}{\mu_n+\mu_p}I_C + qA\left\{\left(\frac{kT}{q}\right)\left(\frac{2\mu_n\mu_p}{\mu_n+\mu_p}\right)\right\}\frac{\partial n}{\partial x} = \frac{b}{b+1}I_C + qAD_a\frac{\partial n}{\partial x} \quad \text{Equation 1.41}$$

$$I_p = \frac{\mu_p}{\mu_n+\mu_p}I_C - qA\left\{\left(\frac{kT}{q}\right)\left(\frac{2\mu_n\mu_p}{\mu_n+\mu_p}\right)\right\}\frac{\partial p}{\partial x} = \frac{1}{b+1}I_C - qAD_a\frac{\partial p}{\partial x} \quad \text{Equation 1.42}$$

where $b = \mu_n/\mu_p$ is the ambipolar mobility ratio, and $D_a = (n + p)/(n/D_p + p/D_n)$ is the ambipolar diffusion coefficient, which can be reduced to $2D_nD_p/(D_n + D_p)$ under high-level injection due to $n \approx p$. From Equation 1.30 and Equation 1.31, for the IGBT N base under high-level injection, the 1D continuity equations for electrons and holes are:

$$\frac{\partial n}{\partial t} = -U_n + \frac{1}{q}\frac{\partial J_n}{\partial x} = -\frac{\delta n}{\tau_{HL}} + \frac{1}{q}\frac{\partial J_n}{\partial x} \quad \text{Equation 1.43}$$

$$\frac{\partial p}{\partial t} = -U_p - \frac{1}{q}\frac{\partial J_p}{\partial x} = -\frac{\delta p}{\tau_{HL}} - \frac{1}{q}\frac{\partial J_p}{\partial x} \quad \text{Equation 1.44}$$

Substituting Equation 1.41 into Equation 1.43 and Equation 1.42 into Equation 1.44, as the I_C is independent of position in the IGBT N base under high-level injection [76]:

$$\frac{\partial n}{\partial t} = -\frac{\delta n}{\tau_{HL}} + D_a\frac{\partial^2 n}{\partial x^2} \quad \text{Equation 1.45}$$

$$\frac{\partial p}{\partial t} = -\frac{\delta p}{\tau_{HL}} + D_a\frac{\partial^2 p}{\partial x^2} \quad \text{Equation 1.46}$$

In the case of n-channel IGBTs, often Equation 1.46 for holes is used and regarded as the Ambipolar Diffusion Equation (ADE). Since holes are minority carriers in N-type regions, under high-level injection $\delta p \approx p$. Equation 1.46 can also be expressed as:

$$\frac{\partial^2 p}{\partial x^2} = \frac{\delta p}{D_a \tau_{HL}} + \frac{1}{D_a}\frac{\partial p}{\partial t} = \frac{\delta p}{L_a^2} + \frac{1}{D_a}\frac{\partial p}{\partial t} \qquad \text{Equation 1.47}$$

where $L_a = \sqrt{D_a \tau_{HL}}$ is the ambipolar diffusion length. In most practical IGBTs, the typical τ_{HL} produces a L_a that is similar to or larger than the thickness of the N base, which results in a near linear on-state excess carrier profile [82]. This is assumed for the discussions in this thesis. The linear approximation of the on-state excess carrier profile under different front-end structures are shown in Figure 1.12 [82], where $x = 0$ is defined as the vertical position of the P emitter to N base junction and $x = W_B$ is defined as the vertical position of the N base to P well junction.

For the N base region under high-level injection, the generalised on-state carrier profile can be described using a linear approximation [82], as shown in Figure 1.12:

$$p(x) = p_0\left(1 - (1-\alpha)\frac{x}{W_B}\right) \qquad \text{Equation 1.48}$$

where p_0 is the hole concentration at $x = 0$ and α, between 0 and 1 depending on the frontside structure, is used to fit the $p(x)$ at $x = W_B$. In the two extreme cases shown in Figure 1.12, α approximates 1 for the ideal trench gate profile and 0 for the ideal planar gate profile. In [82], p_0 is found by solving for $\partial p/\partial x$ at the P emitter to N base junction:

$$p_0 \approx \sqrt{\frac{bI_C}{qAh_p(b+1)}} \qquad \text{Equation 1.49}$$

where h_p is the P emitter recombination parameter, defined for an abrupt junction as:

$$h_p = \frac{1}{N_{A,P}}\coth\left(\frac{W_P}{L_{n,P}}\right)\frac{D_{n,P}}{L_{n,P}} = \frac{1}{N_{A,P}}\coth\left(\frac{W_P}{L_{n,P}}\right)\sqrt{\frac{D_{n,P}}{\tau_{n,P}}} \qquad \text{Equation 1.50}$$

where $N_{A,P}$ is the P emitter doping concentration, W_P is the vertical thickness of the P emitter, and $L_{n,P} = \sqrt{D_{n,P}\tau_{n,P}}$, $D_{n,P}$, and $\tau_{n,P}$ are the diffusion length, diffusion coefficient, and lifetime, respectively, of the minority electrons in the P emitter.

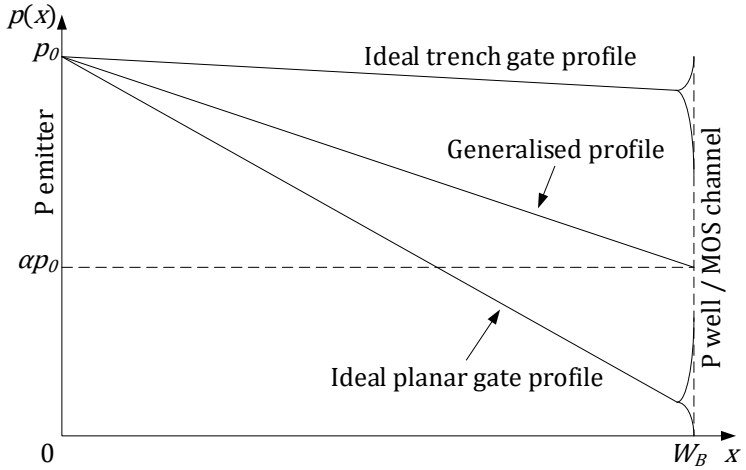


Figure 1.12: Linear approximations of the on-state excess carrier profiles in the IGBT N base under different front-end structures [82].

1.5 Internal Mechanisms of FS IGBTs in Typical Inductive Turn-off

The FS IGBTs referred to in this thesis are modern high voltage vertical n-channel Si commercial devices. The thesis focuses on the major mechanisms and factors that affect the V_{CE} sharing in the simultaneous turn-off of IGBTs in direct series connection. The effects of oscillation of the V_{CE} and the I_C at the turn-off in a poorly optimised Current Commutation Loop (CCL) are intended for the future work. The temperature range considered is the temperature range of commercial modern IGBTs in normal operation of 300 K to 450 K, in which complete ionisation of dopants can be assumed.

IGBT modules are often packaged with multiple IGBT chips in parallel. The IGBT characteristics in this thesis refer to the collective characteristics of the active IGBT cells in those IGBT chips. Typical operation of IGBTs within the Reverse Bias Safe Operating Area (RBSOA) is assumed. Further research regarding the variations between the IGBT cells/chips in parallel and abnormal operating states of the IGBTs is intended for the future work.

In this thesis, the term “voltage” in “voltage sharing”, “voltage divergence” and similar phrases relevant to IGBTs refers to the IGBT V_{CE}. The term “series” in “series turn-off”, “series voltage sharing”, “series voltage divergence” and similar phrases relevant to IGBTs refers to the series connection of IGBTs in electrical terms.

1.5.1 1D Approximations for the IGBT N Base

The FS IGBTs considered in this thesis are modern high voltage vertical Si devices. The 1700 V IGBTs used in the later experiments and simulations in this thesis have a semiconductor thickness, referred to as the vertical and the y direction in 2D, in the range of 170-190 µm. The MOS gate side of an IGBT has a 2D or 3D structure, which results in non-uniform lateral distributions of the carriers, the electric field, and the current near the MOS gate. The collector terminal side of an IGBT may also have a 2D or 3D structure, e.g. Reverse Conducting IGBTs, that results in similar non-uniform effects in the lateral/x direction.

Following the discussion of 1D approximations in [76], normally in the part of an IGBT bulk region beyond 15 µm in vertical depth from a semiconductor surface, the carrier and the electric field distributions can be considered to have approximated uniform lateral distributions. These have been observed in the Silvaco simulations to be shown later. In typical IGBT turn-off, e.g. at 50% utilisation of the rated maximum V_{CE}, the majority of the depletion region develops deeply into the thick IGBT N base to support the high V_{CE} with a vertical depth that greatly exceeds 15 µm, which supports the use of 1D approximations.

At the backside of a non-reverse-conducting IGBT, the doping profile is uniform along the lateral/x direction, which supports the use of 1D approximations. Regarding reverse conducting IGBTs, in typical use, e.g. at 50% utilisation of the rated maximum V_{CE}, the depletion region in the turn-off and the off-state also has a margin from the backside semiconductor surface that normally exceeds 15 µm. Hence, 1D approximations are acceptable in the generalised analysis of the turn-off and voltage sharing mechanisms of the high voltage vertical Si IGBTs and is therefore used in this thesis.

1.5.2 The IGBT Initial State Prior to Turn-off

The output characteristics of an IGBT in inductive turn-off depend on the carrier profile under high-level injection in the on-state prior to the turn-off. As previously discussed in section 1.4, the N FS buffer in a modern FS IGBT is designed to be also under high-level injection in a typical on-state, where the N FS buffer can be considered as part of the N base of the PNP BJT structure of the FS IGBT alongside the N-drift region.

Hence, considering the semiconductor structure of an FS IGBT, the most influencing factors on the on-state carrier distribution include the P emitter doping profile, the MOS channel conductivity, the N base thickness, and the effective carrier lifetimes. The N FS buffer in a modern FS IGBT only has a minor influence on the carrier profile in a typical on-state. In this thesis, both the N-drift region and the N FS buffer are assumed to be under high-level injection in a typical IGBT on-state.

1.5.3 Low IGBT Gate Resistance and Fast IGBT Turn-off

The current commutation in the IGBT turn-off in an inductive CCL requires the total V_{CE} to first exceed the DC link voltage V_{DC} so that the FWD in the CCL becomes forward-biased to receive the load current. This process results in an overlap between the high V_{CE} and the high I_C that generates high losses. Switching an IGBT off using a low gate resistance can shorten this overlap period and reduce the IGBT turn-off losses. By using a low gate resistance, the MOS channel that provides the electron base current for the PNP BJT structure is cut off early in the fast V_{CE} rising. This prevents IGBT turn-off from passing through much of the V_{GE} controlled active region of operation and increases the use of the I_C in the transport of the excess carriers in the IGBT N base that expands the depletion region. Using this turn-off method, an IGBT can quickly establish its V_{CE} to reduce the overlap period of the high V_{CE} and the high I_C in which high losses are produced. To reduce the turn-off losses, it is preferable to use gate resistors of low values, although this approach tends to produce high V_{CE} overshoots.

Another consideration of using a small gate resistance for IGBT turn-off is the possibility of dynamic avalanche. In the depletion region, when the peak electric field reaches the critical electric field due to the overlap between the high V_{CE} and the high I_C, dynamic avalanche occurs as the impact ionisation reaches avalanche multiplication. Modern IGBT chips are able to achieve a larger RBSOA up to the rated maximum V_{CE} and twice the rated maximum I_C simultaneously due to the improvements in the capability to withstand dynamic avalanche and in latch-up immunity, even with a low gate resistance for turn-off [83]–[85]. In power electronic systems, the utilisation of IGBT ratings is usually conservative [86], e.g. not exceeding 50%. At such utilisation, it can be assumed that even if using a low gate resistance, dynamic avalanche is avoided in the fast V_{CE}-I_C transient, which includes the fast V_{CE} rising and the rapid I_C falling as the V_{CE} overshoots. Using a low gate resistance assists to prevent current crowding near the MOS channel in IGBT turn-off, and as the MOS channel is cut off at a low V_{CE} before the dynamic avalanche conditions are reached, and the maximum current turn-off capability is enhanced [83], [87].

In Chapter 1-4, uncontrolled and hard-switched IGBT turn-off is assumed, without any feedback control or snubber circuit applied. The IGBT gate drive output is assumed to switch abruptly from the on-state driving voltage to the off-state driving voltage. The IGBT gate drive output and the IGBT gate terminal are connected using only one gate resistor of a low value to facilitate the IGBT turn-off without extensive use of the V_{GE} controlled active region of operation in the turn-off.

1.5.4 Initial Behaviour of the MOS Channel Region

In an IGBT on-state, the electrons through the MOS channel provide the base current for the PNP BJT structure. Initially in IGBT turn-off, the behaviour of the MOS channel region affects the later behaviour of the IGBT.

At the beginning of IGBT turn-off, the gate drive output switches abruptly from the on-state driving voltage to the off-state driving voltage. Initially, the gate-emitter capacitance C_{GE} discharges through the gate resistor, and the IGBT V_{GE} falls. In this stage, the gate current I_G is negative, referred to as flowing out from the IGBT gate. The MOS channel is still under inversion conditions while the V_{GE} remains above the V_{TH}. Due to the reduction in the V_{GE}, the voltage across the MOS channel increases slightly. This initial discharging continues until the V_{GE} reaches the minimum level of ($V_{GE} - V_{TH}$) required to support the on-state MOS channel current without channel pinch-off, after which the IGBT turn-off enters the gate plateau period where the V_{GE} only decreases slightly.

In the gate plateau period, the negative I_G reduces the charges across the gate oxide. The electron concentration in the MOS channel decreases and the inversion layer thickness is reduced. Meanwhile, the accumulation layer in the part of the N-drift region adjacent to the gate oxide is also weakened as the electron concentration in that area decreases. A large number of charges is removed from this thin layer in this manner and must be removed before the depletion region can form. The excess carrier concentration in the N-drift region adjacent to the MOS gate decreases and the V_{CE} increases slightly. In this period, as the total V_{CE} is below the V_{DC} and the FWD in the CCL is not conducting, the I_C remains at the load level.

As this gate discharging by the negative I_G continues, the depletion region across the P base to N-drift region junction expands and the depletion region under the gate oxide in the N-drift region starts to form. These two depletion regions are temporarily separated due to the electron current from the MOS channel which directs the total current into a narrow path between them towards the MOS channel. The expansion of the depletion regions and the narrowing of the current path increase the V_{CE} slightly.

In the gate plateau period, as the inversion layer that forms the MOS channel is weakened, the MOS channel resistance increases. While the V_{GE} remains at nearly the same level, the MOS channel current remains virtually unchanged, and the voltage across the MOS channel increases. As the gate discharging continues, the pinch-off conditions of the MOS channel are eventually reached, similar to the MOS channel pinch-off in a power MOSFET.

1.5.5 Ambipolar Carrier Transport in the CSR in the Fast V_{CE}-I_C Transient

Further discharging the MOS gate beyond the initial MOS channel pinch-off forces the MOS channel into saturation, and the MOS channel current starts to reduce. In typical IGBT turn-off, due to the high-level excess carriers and the ambipolar carrier transport in the N base, the load current in the N base can be supported independently of the MOS channel current in this turn-off stage. Consequently, when using a low gate resistance for turn-off, the V_{CE} in the turn-off is not strongly dependent on the I_G, which is significantly different from the current conducting mechanism in power MOSFET turn-off after the initial MOS channel pinch-off. With a low gate resistance, the MOS channel current can be reduced quickly to zero while the V_{CE} is still low. This cuts off the supply of electrons from the MOS channel to the Carrier Storage Region (CSR), which changes the carrier transport mechanism at the MOS gate side boundary of the CSR. It is assumed for the IGBT turn-off referred to in this thesis that the MOS channel is cut off very early in the fast V_{CE} rising.

As the IGBT V_{CE} rises, the blocking voltage of the FWD in the CCL is reduced, which results in a discharging current through the FWD. Due to the nearly constant load current under inductive load conditions, this FWD discharging current results in a small reduction in the IGBT I_C before the rapid I_C falling. However, due to the absence of high-level excess carriers in the reverse-biased FWD, the FWD discharging current is normally insignificant compared with the load current and is not considered in the discussions here. The IGBT I_C is considered to remain unchanged in the fast V_{CE} rising until the following V_{CE} overshoot where the I_C falls rapidly.

After the MOS channel is cut off, in the inner section of the CSR the same current composition still remains, predominantly in the form of ambipolar current until the tail time. In the inner section of the CSR, the ambipolar current is still formed by the drift currents of the high-level excess carriers under the ambipolar electric field, for which free electrons are still required to be supplied to the inner section of the CSR from the MOS gate side CSR boundary. However, since the electrons from the MOS channel is no longer available, the free electrons at the MOS gate side CSR boundary, including the excess electrons and the free electrons from the ionised N-type dopants, are transported towards the inner section of the CSR.

At the MOS gate side CSR boundary, this electron transport simultaneously exposes the excess holes and produces N-type dopants that lose electrons which both exhibit positive charges. These exposed excess holes and N-type dopants without electrons of the same electric polarity produce an electric field that propels those free excess holes into the depletion region towards the MOS gate side. The simultaneous electron and hole transport at the MOS gate side CSR boundary results in the CSR shrinking from the MOS gate side and the simultaneous depletion region expanding, which is related to the fast V_{CE} rising and the following V_{CE} overshoot. Hence, in typical IGBT turn-off after the MOS channel is cut off, the expansion of the depletion region in the fast V_{CE}-I_C transient is a result of the CSR shrinking from the MOS gate side due to supporting the ambipolar current in the inner section of the CSR without the electrons supplied from the MOS channel.

1.5.6 Carrier Recombination in the CSR in the Fast V_{CE}-I_C Transient

As discussed previously, the continuity equations for the CSR can be reduced to 1D situations, in which the divergence math operators become gradient math operators. In the inner section of the CSR, the current and the excess carrier profile are considered to remain unchanged during the fast V_{CE} rising before the rapid I_C falling. For the inner section of the CSR, the continuity equations suggest that the same total current in the CSR is composed of an electron current and a hole current of complementary gradients over distance, which are related to the dynamic losses of electrons and holes due to recombination. The complementary current gradients are due to the effective carrier lifetimes of both electrons and holes reach the same high-level lifetime under high-level injection. As the I_C falls during the V_{CE} overshoot, the excess carrier profile in the remaining CSR falls accordingly. Consequently, the recombination rate in the remaining CSR decreases, and the complementary current gradients become lower in rates.

If taking a non-ideal FWD in the CCL into consideration, as discussed in section 1.5.5, under inductive load conditions the I_C will fall slightly before the V_{CE} overshoot, which will cause the excess carrier profile in the remaining CSR to fall slightly. But since a typical fast V_{CE}-I_C transient is considerably shorter compared with the high-level carrier lifetime, that slight reduction in the excess carrier profile in the remaining CSR before the V_{CE} overshoot is usually negligible and therefore is not considered here.

1.5.7 Carrier Transport at the MOS Gate Side CSR Boundary in the Fast V_{CE}-I_C Transient

Following the discussion in section 1.5.5, regarding the carrier transport at the MOS gate side CSR boundary, the free electrons are transported towards the inner section of the CSR while the excess holes are transported into the depletion region towards the MOS gate side. In the fast V_{CE}-I_C transient, the inner section of the CSR experiences the same type of ambipolar current that equals the I_C, despite that the electron source for this ambipolar current is switched from the electrons via the MOS channel to the free electrons from the MOS gate side CSR boundary. This continuing ambipolar current in the CSR consumes the free electrons in the CSR itself from the MOS gate side CSR boundary, where the excess holes are exposed to a high electric field and are transported into the depletion region. This process causes the shrinking of the CSR and the expansion of the depletion region.

Regarding the ambipolar current in the CSR, the high-level excess carriers propelled by the ambipolar electric field form the major current components, which predominate over the small diffusion current components by the non-uniform excess carrier profile. As the high-level excess electrons and holes are under the same ambipolar electric field and their concentrations are considered the same, within the ambipolar current that equals the I_C the ratio of the electron drift current to the hole drift current is determined by the ratio of the electron mobility to the hole mobility. Since $I = \mathrm{d}Q/\mathrm{d}t$, the number of free electrons transported from the MOS gate side CSR boundary, mainly the high-level excess electrons without the electron supply via the MOS channel, is related to the I_C. Similarly, the number of excess holes that are exposed to a high

electric field and transported into the depletion region is also related to the I_C. Therefore, the expansion of the depletion region is related to the I_C.

Hence, in IGBT turn-off at the same load current, a higher on-state excess carrier profile results in a slower depletion process and a lower dV_{CE}/dt rate, and therefore a lower V_{CE} sharing in the fast V_{CE}-I_C transient. Relevant discussions will follow.

1.5.8 Hole Current and Electric Field in the Depletion Region in the Fast V_{CE}-I_C Transient

In typical IGBT turn-off, after the MOS channel is cut off, in the fast V_{CE}-I_C transient the current in the depletion region consists of basically a hole current composed of the holes transported from the MOS gate side CSR boundary. These holes in the depletion region increase the electric field gradient in the depletion region. Following the discussion in section 1.5.3, here it can be assumed that in the depletion region during the fast V_{CE}-I_C transient, dynamic avalanche is avoided, and impact ionisation only results in insignificant changes to the current composition.

After the MOS channel is cut off, the depletion region soon becomes large enough that the electric field in it becomes high enough to allow free holes to reach saturated drift velocities, which soon becomes valid in the majority of the depletion region. Hence, the hole concentration in the majority of the depletion region has a near linear relation to the IGBT I_C. According to the Gauss's law, in 1D the electric field gradient at a certain location is related to the net charge density. Here in the depletion region, the net charges are predominantly determined by the positive charges contributed by the N-type dopants as they lose electrons in the depletion region and the holes in the depletion region related to the I_C. As the doping profile in the N-drift region is considered uniform, a higher I_C will result in a higher hole concentration in the depletion region which leads to a higher electric field gradient in the depletion region.

After the MOS channel is cut off, in 1D the electric field in the depletion region is first in a near triangle distribution. The electric field gradient in the depletion region in the N-drift region first remains basically unchanged as the I_C remains at the load level until the later V_{CE} overshoot where the I_C falls rapidly. In the fast V_{CE}-I_C transient, the 1D expression for the electric field gradient can be approximated by:

$$\frac{dE}{dx} = \frac{q(N_D + p_{SC})}{\varepsilon_S} \qquad \text{Equation 1.51}$$

$$p_{SC} \propto \frac{I_C}{qAv_{sat,p}} \qquad \text{Equation 1.52}$$

where q is the elementary charge, N_D is the doping concentration in the N-type depletion region, p_{SC} is the hole concentration in the depletion region, ε_S is the permittivity of the semiconductor, and $v_{sat,p}$ is the saturation drift velocity of the holes in the depletion region.

Here, the stray inductances in the CCL of the IGBTs are considered, in the form of a lumped stray inductance L_S connected between the IGBT branch and the FWD branch in the CCL. The inductive load is connected to the node between the L_S and the FWD branch. In the IGBT turn-off, after the total V_{CE}, $V_{CE,tot}$, reaches the V_{DC}, due to the continuing I_C the $V_{CE,tot}$ first continues to increase and exposes the L_S to the ($V_{CE,tot} - V_{DC}$). This causes the current of the L_S, $I_{Ls} = I_C$

due to the series connection, to fall which enables the load current commutation from the IGBT branch to the FWD branch in the CCL. In an IGBT in series, despite the falling I_C, the depletion region continues to expand towards the N FS buffer. As the I_C falls, the hole concentration and the electric field gradient in the depletion region decrease, and the carrier transport at the MOS gate side CSR boundary is reduced. Consequently, the $\mathrm{d}V_{CE}/\mathrm{d}t$ rate will decrease from positive to negative and return to near zero, which completes the V_{CE} overshoot and the main load current commutation due to the related changes in the $(V_{CE,tot} - V_{DC})$.

In IGBT turn-off under abnormal conditions, the V_{CE} may become high enough to force the depletion region to punch through the N-drift region and reach the N buffer. Due to the higher doping concentration in the N buffer, the part of the N buffer in the depletion region exhibits a higher positive charge density, which produces an increased electric field gradient. Despite the thin depletion region in the N buffer, the electric field at the N-drift region to N buffer boundary is significantly increased, which elevates the electric field in the N-drift region. Therefore, the $\mathrm{d}V_{CE}/\mathrm{d}t$ rate increases, and if the depletion region reaches the N buffer while the V_{CE} falls in the V_{CE} overshoot, a second V_{CE} overshoot may appear. The I_C falling rate increases which is likely to cause V_{CE}-I_C oscillation.

1.5.9 Current Commutation in Inductive Turn-Off with Stray Inductance

Inductive load conditions for IGBTs are common in power electronic systems such as DC-DC converters. The basic CCL of such inductive switching circuits is usually composed of an active switch branch by IGBTs, an FWD branch by power diodes, and an inductive load branch connected to the IGBT to FWD connection node. The discussions in this thesis assume such an inductive CCL for the IGBT turn-off. In addition, load conditions in zero-voltage switching and zero-current switching of IGBTs are to be considered in the future work.

For the IGBTs, stray inductances exist in the device packages and the CCL and can be considered as a lumped stray inductance L_S. The L_S is normally considered to be a self-inductance and is inductively uncoupled without magnetic saturation effects, represented by an uncoupled air-core coil inductor. A change in its flux that is directly related to the current through the L_S, I_{Ls}, induces a back ElectroMotive Force (EMF) in the form of a voltage across the L_S, V_{Ls}, with the *I-V* characteristics of $V_{Ls} = L_S(\mathrm{d}I_{Ls}/\mathrm{d}t)$. The V_{Ls} and the I_{Ls} of the stray inductance as a magnetically uncoupled self-inductance are passively determined by the interaction between itself and the external circuit. When the stray inductance is exposed to a voltage across it, the I_{Ls} changes at a rate that induces a V_{Ls} to counter that voltage to which the L_S is exposed. The I_{Ls} changes passively to induce a V_{Ls} that satisfies both the KVL and the KCL.

Following the relevant discussion in section 1.5.8, during the V_{CE} overshoot, the $V_{CE,tot}$ first exceeds the V_{DC} due to the continuous I_C, and the positive $(V_{CE,tot} - V_{DC})$ is the voltage across the L_S against the direction of the I_{Ls}, which causes the I_{Ls} to fall rapidly. As $I_C = I_{Ls}$, the I_C also falls rapidly. Hence, as coupled by the CCL, the I_C falling during the V_{CE} overshoot is in response to exposing the L_S to the $(V_{CE,tot} - V_{DC})$ across it. In an IGBT in series, the I_C is related to the electric field of the depletion region and therefore the $V_{CE,tot}$. As the I_C falls, the electric

field gradient in the depletion region and the carrier transport at the MOS gate side CSR boundary are reduced. Thus, the V_{CE} overshoot and the main load current commutation are completed.

1.5.10 Carrier Transport and Recombination in the Tail Time

As discussed in section 1.5.9, the I_C falling during the V_{CE} overshoot follows the I_{Ls} falling passively as coupled by the CCL. In this stage, the ambipolar carrier transport is still predominant inside the CSR. Later as the I_C falls, the I_C becomes comparable to the hole diffusion current in the remaining CSR towards the depletion region. This marks the transition of the IGBT turn-off from the fast V_{CE}-I_C transient to the tail time.

In the tail time, the carrier recombination and diffusion in the undepleted part of the N base become important. The remaining excess carriers recombine and diffuse, especially for the transport of the excess holes that is related to the tail current. In the tail time as the I_C continues to fall, in part of the N base near the P emitter, the electron concentration starts to reach the doping level. For the holes as minority carriers in the same region, the hole concentration continues to fall below the N-type doping level, and the hole diffusion current decreases. In addition to carrier recombination and diffusion, carrier drift provides another degree of freedom in the carrier transport to enable the same net current in the undepleted part of the N base. The IGBT output characteristics in the tail time are affected by the combined effects of carrier drift and carrier diffusion under the influence of carrier recombination.

At the beginning of the tail time, in the case of an IGBT having an extended remaining CSR, e.g. due to a thinner depletion region, the holes from the remaining CSR produce an enhanced diffusion current due to the additional supply of holes from the broader inner section of the remaining hole distribution. Similarly, in the case of an IGBT having a higher carrier profile in the remaining CSR, e.g. due to a higher P emitter doping profile, the holes from the remaining CSR also produce an enhanced diffusion current due to the additional supply of holes from the inner section of the remaining hole distribution of a higher concentration. In the case of higher carrier lifetimes, in the tail time the reduction in the hole concentration in the remaining CSR due to recombination is slower, the effect of which is similar to the previous case of a higher hole concentration producing an enhanced diffusion current.

As the transport and recombination of the remaining holes continue, the hole concentration falls and gradually becomes stable. Meanwhile, the I_C falls to the leakage level while the $V_{CE,tot}$ falls to the V_{DC}, and the IGBT turn-off is completed.

Chapter 2 Application and Research Motivation for Operating IGBTs in Series Connection

2.1 Applications of IGBTs in Series Connection

By the time this research was completed, commercial IGBTs were Silicon (Si) based with voltage classes up to 6.5 kV [59], [88]–[93], although Silicon Carbide (SiC) based IGBTs of voltage ratings exceeding 10 kV have been reported [94]–[102]. In many IGBT based power electronic systems that are related to HVDC technologies, the DC link voltage for the IGBT branch exceeds the maximum V_{CE} rating of a single IGBT device to a great extent [103]–[109]. In such cases, IGBTs are operated in series connection in different forms. In converters, two common forms include IGBT devices in series connection and IGBT based submodules in series connection. The latter are often in a half-bridge configuration with a DC capacitor. The series connection of IGBT devices is often used in two-level or three-level converters, and the series connection of IGBT based submodules is often used in multi-level converters such as Modular Multi-level Converters (MMCs).

2.1.1 VSC using IGBTs in Series Connection

In late 1990s, some HVDC related VSCs used the series connection of IGBT devices to gain high voltage handling capabilities. A representative implementation is the early HVDC Light technologies developed by ABB, first in 1997 for evaluation and in 1999 for commercial use [110]–[117]. The generations 1-3 of the ABB HVDC Light were based on IGBT devices in series connection, using two-level and three-level configurations [118]. The series connection of IGBT devices is a direct approach to support high DC link voltages. It enables the use of simple converter circuits and less complicated control at converter circuit level.

However, two-level and three-level VSCs require PWM schemes to achieve sinusoidal output, in which all the IGBT devices in series connection in a half-leg are switched simultaneously as a single switch. This produces high switching losses and high dV/dt rates that cause harmonic and ElectroMagnetic Compatibility (EMC) issues. Filters are required as a result, which increases the total cost and the operating losses of the converter.

The voltage sharing between the series-connected IGBT devices needs to be controlled in the turn-off, the off-state, and the turn-on. This is to prevent over-voltage breakdown and to achieve similar thermal stresses on each IGBT device. However, achieving evenly distributed voltage sharing between the series-connected IGBT devices in real time with low switching losses presents various challenges.

2.1.2 Hybrid Circuit Breaker for MMCs

In 2003, the MMC concept was first introduced [119], [120]. The first commercial implementation of the MMC for HVDC was by Siemens in 2010 [117], [121]–[123]. An MMC consists of several IGBT based submodules in series connection. A typical submodule uses a half-bridge configuration rather than an H-bridge configuration. By the time this research was completed, all commercial MMC installations for HVDC were based on half-bridge submodules [117].

This is to reduce the number of IGBTs for saving both conduction losses and costs. A typical submodule consists of two switches by IGBTs with anti-parallel FWDs and one capacitor.

The MMC improves upon the VSC using series-connected IGBT devices in several key aspects. With the assistance from the capacitors in the MMC submodules, the real-time voltage sharing issues between the series-connected IGBT devices in the VSCs are significantly mitigated. In nature, an MMC converts the regulation of the V_{CE} sharing between series-connected IGBTs into the regulation of the voltage sharing between the capacitors in the submodules. The scaling of the MMC for higher DC voltages is easier due to the modularised design.

In a typical MMC, only one submodule is switched at a time. At the same DC voltage, the total number of switching events of the IGBTs can be reduced compared with VSCs using IGBT devices in series connection. The switching losses and the harmonics are also reduced. For an MMC at a certain DC voltage, as the number of submodules increases, the harmonics and the requirements for filters are reduced, which reduces the operating losses [124]. A representative implementation of the MMC for HVDC is the HVDC PLUS by Siemens [105], [123].

However, MMCs are also subject to challenges in operation. The half-bridge submodule configuration only has partial active control of its capacitor voltage. A typical MMC based HVDC system requires 300-400 two-level submodules to support grid level DC voltages. Regulating the voltage sharing between such a large number of submodule capacitors in real-time operation is complicated and imposes significant challenges to the central controller, the measurement system, and the communication system [124], [125]. The absence of filters would require a large and bulky capacitor in each submodule [124], [126].

Also, the half-bridge submodule configuration is unable to produce a negative output voltage. In the event of a DC side short circuit fault, the anti-parallel FWDs of the IGBTs in the submodules will form a current path for the DC fault current. Due to the passive nature of diodes, this DC fault current path is uncontrollable by the half-bridge submodules. Due to the response delay, preferably the DC fault current needs to be limited using a DC side circuit breaker rather than an AC side circuit breaker [124], [126]–[129].

Conventional mechanical circuit breakers are not ideal for the use in modern HVDC systems, especially under inductive load conditions, due to arcing and response time issues [130]. In such a situation, the use of power semiconductor devices in DC circuit breakers is attractive, specifically, the use of power semiconductor devices alongside mechanical circuit breakers. The resulting circuit breakers are referred to as Hybrid Circuit Breakers (HCBs) [130], [131], in which fully controllable power semiconductor devices are connected in series to provide high blocking voltages. IGBTs are favourable for HCBs [130], [132]–[138]. The use of IGBTs as voltage-controlled devices enables easier implementation of control schemes for regulating the voltage sharing. A schematic circuit diagram of an HCB for HVDC using IGBTs in series connection for the main breaker and the Load Commutation Switch (LCS) is shown in Figure 2.1 [135]. An HCB cell for HVDC with four HCB stacks is illustrated in Figure 2.2 [139].

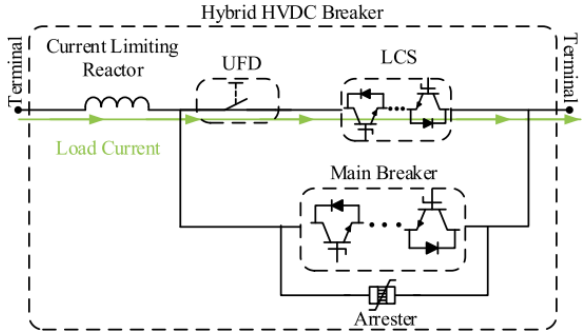


Figure 2.1: Schematic diagram of an HCB circuit for HVDC using IGBTs in series connection [135].

Schematic diagram of an HCB cell removed for copyright reasons. Copyright holder is ABB.

Figure 2.2: An HCB cell for HVDC with four HCB stacks [139].

The voltage sharing between the series-connected IGBTs is important for an IGBT based HCB [138]–[140]. Although not directly applied to MMCs, the use of IGBTs in series connection is still involved in the protection of MMCs.

2.1.3 Director Switch in Alternate Arm Converters

The half-bridge submodules in MMCs are vulnerable against DC side short circuit faults. New converter topologies are developed to solve this issue [141]–[143]. One of the approaches is the

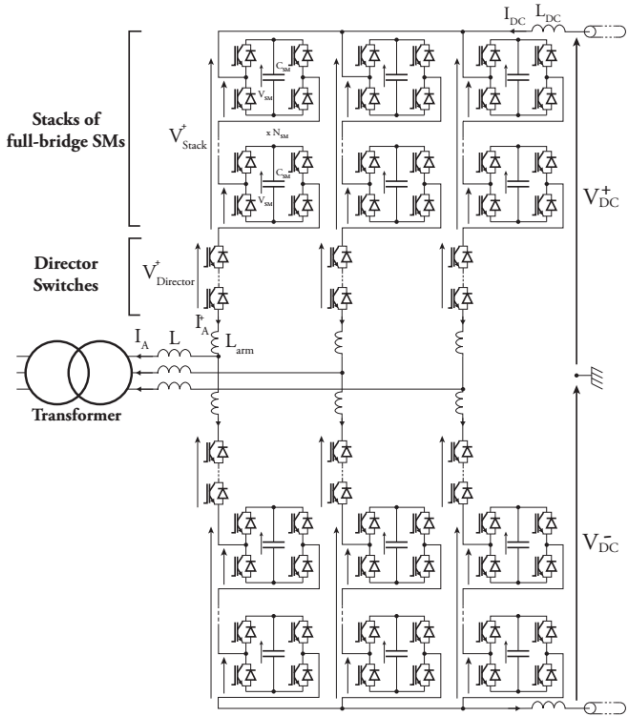


Figure 2.3: Schematic diagram of the circuit topology of the AAC [145].

Alternate Arm Converter (AAC) developed by Alstom Grid in conjunction with Imperial College, with the commercial name of HVDC MaxSine [124], [142], [144].

The AAC is an integration of the key concepts of MMCs and two-level VSCs [124], [142]. The schematic diagram of the AAC circuit topology is shown in Figure 2.3 [145]. Each phase of the AAC has two arms, and each arm is composed of a stack of series-connected H-bridge cells, which resembles the concept of MMCs. In series with those H-bridge cells is a director switch, which resembles the concept of two-level VSCs, and a small arm inductor [124]. The director switch controls the conducting period of the arm. Such an integration of series-connected H-bridge cells and a director switch is capable of controlling the current in the event of a DC side short circuit fault and supporting the AC side using a STATCOM mode [124].

The director switch is composed of a large number of series-connected IGBTs to provide a high voltage rating, e.g. $2V_{DC}/\pi$ [124]. Evenly distributed voltage sharing between the series-connected IGBTs in the director switches is preferable for reliable operation of the AAC.

2.1.4 Cascaded Two-Level Converter

ABB uses a hybrid variant of the MMC concept named Cascaded Two-Level (CTL) converter in the generation 4 of its HVDC Light [117], [118], [146], which is the most recently published by the time this research was completed. The circuit topology of the CTL converter resembles that of the original MMC by cascading submodules in series, but each active switch in the submodule consists of IGBTs in series connection, 8 IGBTs in series as reported in [117], [146]. The schematic diagram of the layout of the ABB Troll A 3 & 4 HVDC Light project is shown in Figure 2.4. The schematic diagram of the circuit topology for one phase of the CTL converter is shown in Figure 2.5. A double IGBT cell and a module of IGBTs in series connection as indicated in Figure 2.5 are shown in Figure 2.6 (a) and (b), respectively [118].

In the CTL converter, the use of series-connected IGBTs as a single switch in a submodule significantly increases the voltage rating of a submodules compared with the use of a single IGBT as a single switch in the original MMC. The increase in the voltage rating of a single submodule significantly reduces the number of submodules required to support a certain DC bus voltage. For example, using a CTL converter to support a ±320 kV DC bus voltage, typically only 38 submodules are required in each arm [146], whereas using the original MMC concept

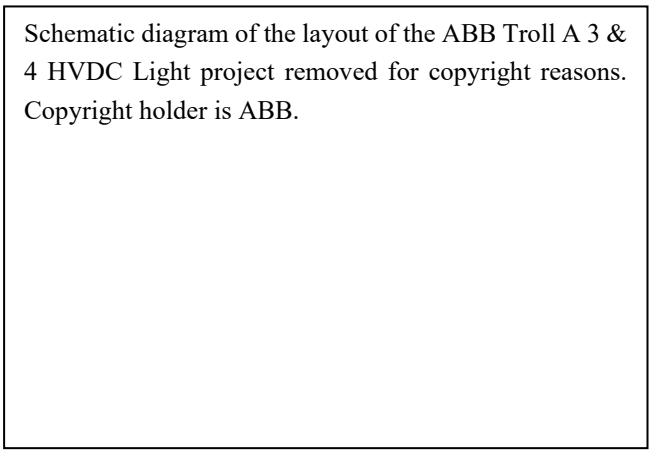


Figure 2.4: Schematic diagram of the layout of the ABB Troll A 3 & 4 HVDC Light project [118].

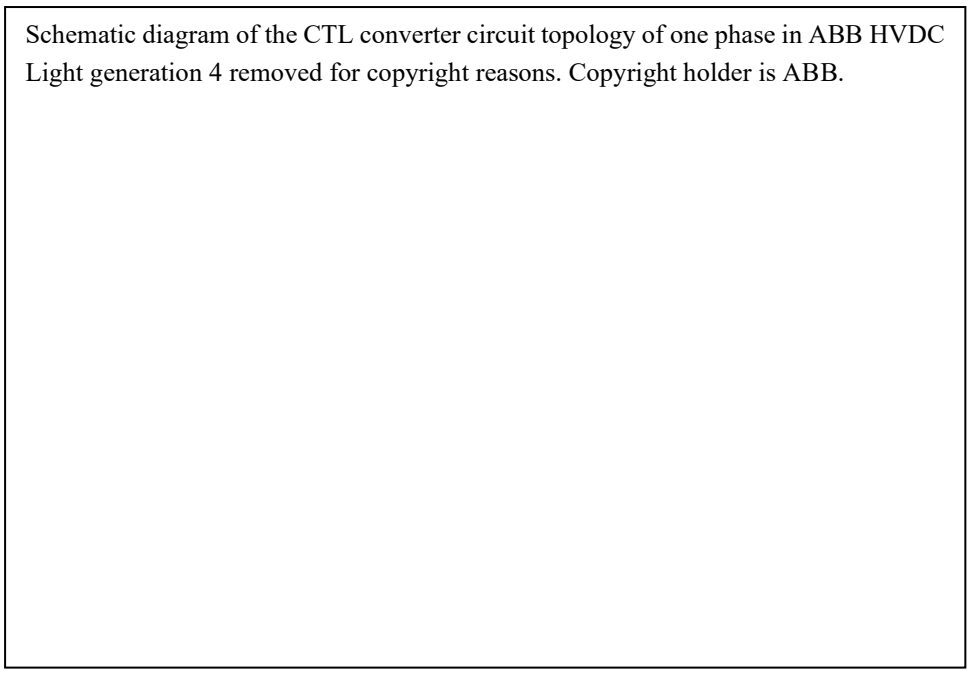


Figure 2.5: Schematic diagram of the CTL converter circuit topology of one phase in ABB HVDC Light generation 4 [118].

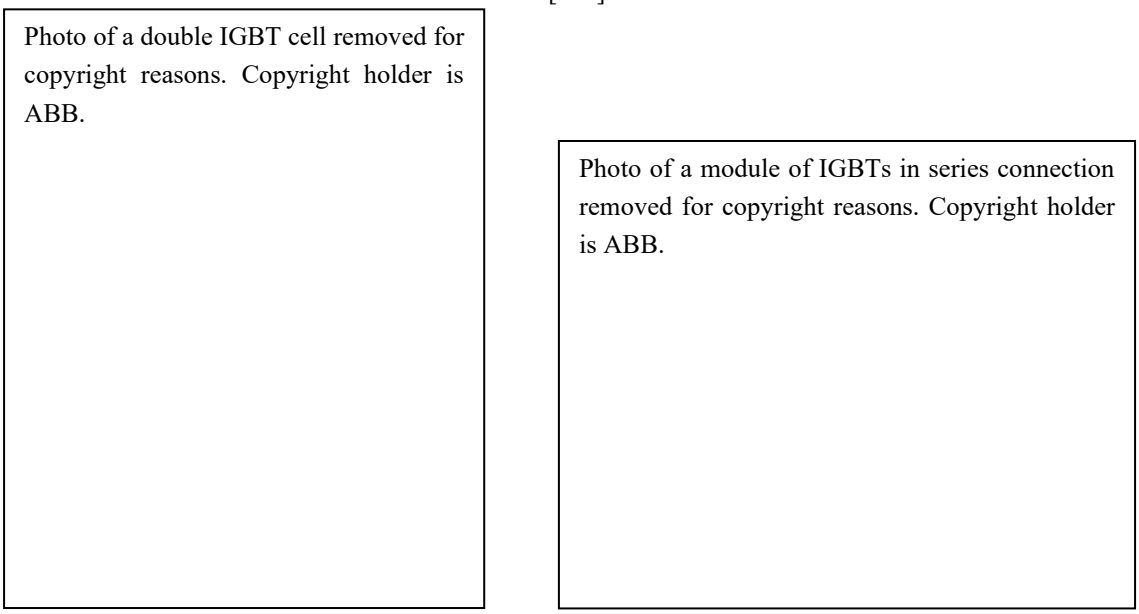


Figure 2.6: (a) a double IGBT cell, and (b) a module of IGBTs in series connection in the CTL converter as indicated in Figure 2.5 [118].

the number of submodules required is 304 because of the 1:8 IGBT device ratio in a single switch due to the use of series connection.

The control complexity of the CTL converter is distributed to an upper level control, referring to the circuit level control, and a lower level control, referring to the submodule level control. In the CTL converter, the considerable reduction in the number of submodule capacitors to be controlled can significantly reduce the complexity of the circuit level control [117], including the control algorithm, the required computing resources, and the measurement and the communication systems for the submodules.

As the number of submodules is reduced, the number of output voltage levels is reduced. As a result, the harmonic performance of the CTL converter is inferior to that of the original

MMC at the same DC bus voltage, but the CTL converter still remains satisfactory to operate without AC filters [146].

In the CTL converter, the operation of IGBTs in series connection in the submodules is of critical importance. The performance, the reliability, and the efficiency of the CTL converter all depend on the operation of IGBTs in series connection.

2.2 Review of Methods for Improving the V_{CE} Sharing

Achieving evenly distributed voltage sharing between IGBTs in series connection without applying additional control would require identical IGBT devices and their individual operating conditions, such as gate drives, parasitic and stray parameters, and snubbers if used. However, in practice, these conditions can hardly be fulfilled. IGBT devices of the same model are usually subject to variations in the physical parameters of the IGBT chips and packages which cause differences in the switching characteristics. And so are IGBT gate drives and other circuit parameters for the IGBTs in series that also affect the switching behaviours of the IGBTs. These variations and differences combined cause different switching behaviours between the IGBTs and result in divergence in the voltage sharing between the IGBTs in series during turn-off.

Many methods have been developed to improve the turn-off voltage sharing of IGBTs in series connection. These methods include load side control methods and active gate control methods, depending on whether the intervention for the voltage sharing is applied via IGBT gate control. A few representative methods are summarised here.

2.2.1 Load Side Control Methods

The load side control methods here refer to the voltage sharing control methods that apply intervention without using the IGBT gate. This type of methods usually involves the use of snubber circuits and may be assisted by feedback control. The IGBT gate drives perform uncontrolled switching regardless of the V_{CE}.

Many load side control methods have been developed [147]–[151], and a few representative load side control methods are summarised here. Most of the load side control methods are based on Resistor-Capacitor-Diode (RCD) configurations that in nature use capacitors to reduce the relative differences in the IGBT switching characteristics, so that their influence on the voltage sharing can be reduced.

2.2.1.1 Basic RCD Snubber

Resistor-Capacitor-Diode (RCD) snubbers connected in parallel to the IGBTs in series is a simple method to mitigate the voltage divergence between the IGBTs in series, [147]. As shown in Figure 2.7, a basic RCD snubber for this purpose usually consists of a resistor of a high value, R_{SVR}, for the voltage sharing in an IGBT off-state and an RCD circuit, by R_{DVR}, C_{VR} and D_{VR}, for the voltage sharing during IGBT switching.

The choice of the R_{SVR} value is related to the off-state C-E resistance of the IGBT in series connection, $R_{CE,off}$, by $R_{SVR} \approx 0.1R_{CE,off}$ as suggested in [147]. For an IGBT, with a R_{SVR} in parallel, the influence of the $R_{CE,off}$ on the overall off-state resistance of the IGBT and the RCD

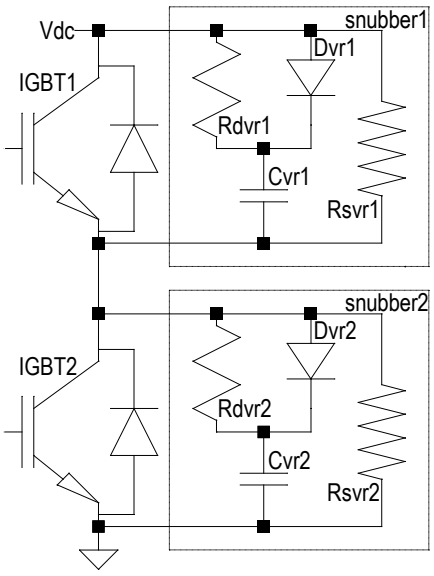


Figure 2.7: A voltage sharing control method using basic RCD snubbers [147].

snubber is reduced. Therefore, using R_{SVR} of high precision, the influence of the differences in the $R_{CE,off}$ of the IGBT in series connection on the off-state V_{CE} sharing is reduced.

The capacitor C_{VR} is designed to be comparable with the average output capacitance of the IGBT in series during switching. Therefore, the influence of the dynamic differences in the output capacitance of the IGBT in series on the V_{CE} sharing during switching is reduced.

During IGBT turn-off, the C_{VR} is charged mainly through the diode D_{VR} as the V_{CE} rises. The D_{VR} is designed to enable fast charging of the C_{VR} by providing a low resistance path for the charging current. The low resistance charging for the C_{VR} provides a voltage sharing control effect as the V_{CE} increases rapidly during IGBT turn-off, where voltage sharing control is required for the IGBTs in series.

During IGBT turn-on, the C_{VR} is discharged through the resistor R_{DVR} as the V_{CE} falls. The R_{DVR} needs to be carefully chosen to prevent an excessive discharging current flowing from the C_{VR} to the IGBT, while allowing adequate discharging of the C_{VR} during IGBT turn-on to maintain some voltage sharing control effect for the IGBT turn-on [147].

The choice of the C_{VR} needs to consider the trade-off between the voltage sharing control effects and reducing the extra switching losses. Compared with the output capacitance of the IGBT during switching, the C_{VR} should be adequate to significantly reduce the dynamic differences in the output capacitance of the IGBT in series. However, if the C_{VR} is too high, the $\mathrm{d}V_{CE}/\mathrm{d}t$ rate will be excessively reduced, which leads to high switching losses. Hence, the choice of the C_{VR} depends on the characteristics of the IGBTs in series, the load conditions, and the limits on the switching losses.

The basic RCD snubber method only requires the use of passive components and is simple to implement. However, the extra losses caused by the RCD snubbers need to be considered. In an IGBT switching cycle, the C_{VR} that is comparable to the IGBT output capacitance is charged to the IGBT off-state V_{CE} during turn-off and is discharged during turn-on. During IGBT turn-off, as the C_{VR} uses a part of the load current of the IGBT branch as its charging current, the

IGBT turn-off dV_{CE}/dt rate is reduced, which increases the total turn-off losses of the IGBT branch. During IGBT turn-on, as the discharging of the C_{VR} is through the R_{DVR} which is lossy in nature, the RCD snubber itself causes extra losses. Preferably, the extra losses caused by the RCD snubbers should be reduced or recycled.

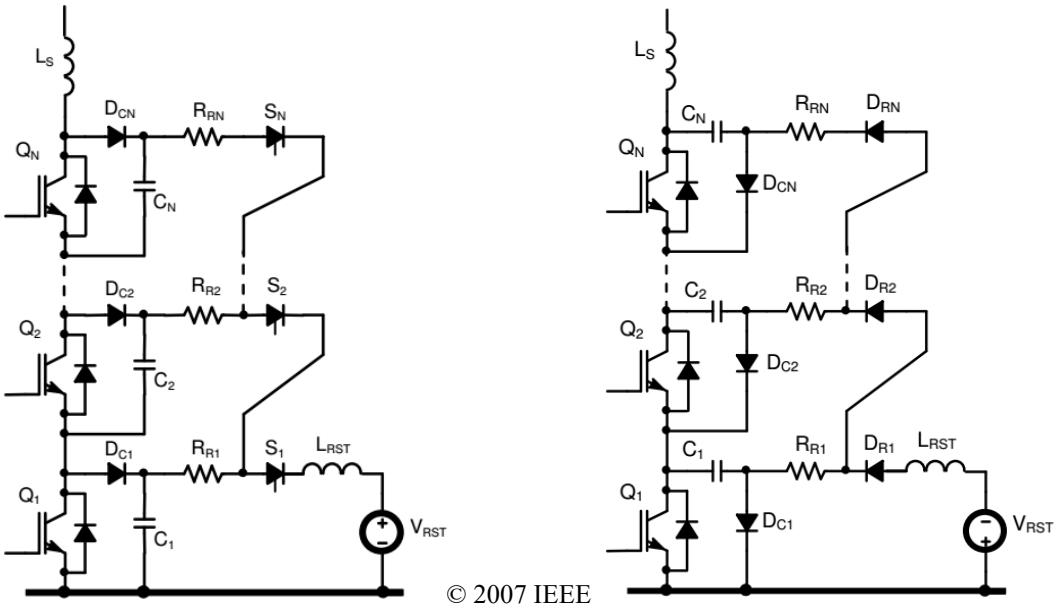
2.2.1.2 Biased RCD Snubber

In the use of the basic RCD snubber, part of the extra losses is due to the energy exchange of the C_{VR} via a lossy path, as the C_{VR} is charged to the IGBT off-state V_{CE} and fully discharged via the R_{DVR} during an IGBT switching cycle. A method that mitigates this issue is biased RCD snubbers, which reduce the use of the C_{VR} to partial charging and discharging to reduce the extra losses [150]. Figure 2.8 shows two original implementations with static voltage sharing resistors omitted from the work reported in [150].

In both cases shown in Figure 2.8, during an IGBT on-state, the capacitors C_1 to C_N are effectively connected to the V_{RST} through the respective R_{R1} to R_{RN}, L_{RST}, and either the respective reset switches S_1 to S_N when turned on in Figure 2.8 (a) or the respective reset diodes D_{R1} to D_{RN} in Figure 2.8 (b). During IGBT turn-on and the following on-state, any of the C_1 to C_N that has a voltage higher than the V_{RST} will be discharge to the V_{RST}.

In Figure 2.8 (a) the reset switches are implemented by thyristors. They can be replaced by other active power devices such as IGBTs. The R_{R1} to R_{RN} and the L_{RST} affect the reset current. The R_{R1} to R_{RN} and the L_{RST} of smaller values can shorten the reset period but increase the peak reset current. The R_{R1} to R_{RN} and the L_{RST} should maintain the reset switches or diodes within their respective SOAs, especially for the S_1 or the D_{R1} where the reset currents converge.

At IGBT turn-off assuming successful reset, after the V_{CE} of an IGBT Q_i reaches the V_{RST}, the D_{Ci} is on and the C_i is effectively connected in parallel to the IGBT Q_i. The C_i is charged with the IGBT Q_i and provides voltage sharing control effects for the IGBT Q_i, similar to the C_{VR} in the basic RCD snubber.



(a) (b)

Figure 2.8: A voltage sharing control method using biased RCD snubbers by (a) reset switches and (b) reset diodes with static voltage sharing resistors omitted [150].

The biased RCD snubber method causes reduced extra switching losses compared with the basic RCD snubber method, due to the limited lossy discharging of the snubber capacitors to the V_{RST}. The extra switching losses are lower at a higher V_{RST}. The demonstration in [150] set the V_{RST} to V_{DC}/N, referring to Figure 2.8, the average off-state IGBT V_{CE}. In this case, fast dV_{CE}/dt rates are preserved in the majority of the V_{CE} rising.

Nevertheless, for IGBT turn-off the V_{CE} range in which the voltage sharing control is effective is limited, as the snubber capacitors can only be charged after the V_{CE} reaches the V_{RST}. Also, this method has limited voltage sharing control effects for IGBT turn-on, as the capacitor voltage can only be discharged to the V_{RST}. Although the changes in the snubber capacitor voltage are reduced, the discharging of the snubber capacitors is still through the lossy reset resistors. The trade-off between the voltage sharing control effects and reducing the extra switching losses remains similar to that of the basic RCD method.

2.2.1.3 Snubber with An Energy Recovery Circuit

A common drawback of the prior RCD based methods is the extra switching losses related to the voltage sharing control effects. Strong voltage sharing control effects require a high value and substantial use of the snubber capacitor. In addition to the extra switching losses related to the reduction in the IGBT dV_{CE}/dt rates during switching, other extra losses are caused due to the lack of energy recovery for the discharging of the snubber capacitor during IGBT turn-on. A representative solution for this issue is an active snubber energy recovery circuit that is effective at both IGBT turn-off and turn-on [151].

The active snubber energy recovery circuit in [151] consists of a capacitor *C1* for IGBT turn-off and *L1* for IGBT turn-on as snubber components, Figure 2.9 [151]. The prior lossy

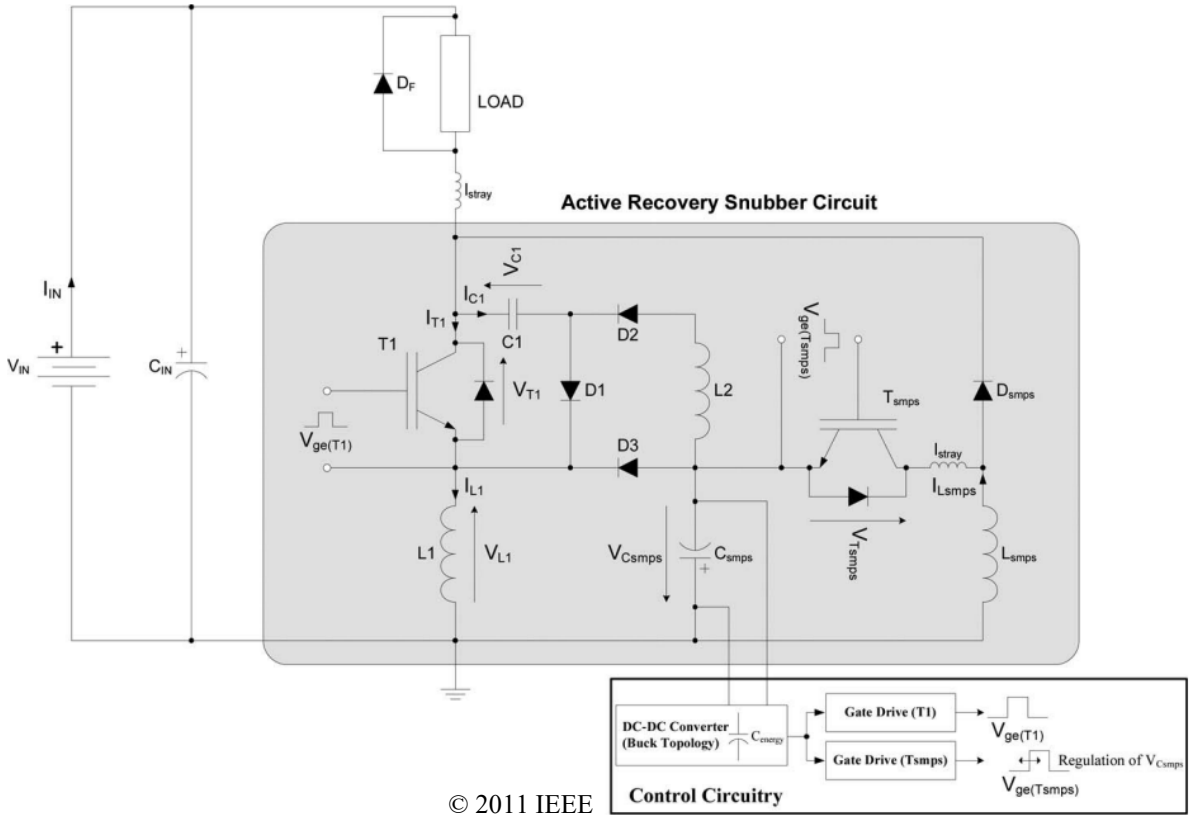


Figure 2.9: A voltage sharing control method using an active snubber energy recovery circuit [151].

discharging resistor in an RCD snubber is replaced with a boost circuit, which is capable of recycling the stored energy in the *L1* and the *C1* using the capacitor C_{smps}.

Referring to Figure 2.9, at IGBT turn-off, the *C1* is first charged through the current path of *C1-D1-L1* and provides voltage sharing control effects for the IGBT *T1*. After the V_{CE} of the IGBT *T1* reaches (V_{IN} + V_{Csmps}), the *D3* turns on, diverting the current path through *L1* to *L1-*C_{smps}*-D3*. The energy stored in the *L1* from the IGBT on-state is then transferred to the C_{smps} until the I_{L1} reaches zero and the energy recycling for the *L1* is completed.

At IGBT turn-on, the *C1* is first discharged through the current path of *C1-T1-L1-*C_{smps}*-L2-D2*, and the *L1* is charged and reduces the current overshoot of the IGBT *T1*. In this process, the stored energy in the *C1* from the IGBT off-state is transferred to the C_{smps}, while the I_{L1} remains above the load current level. This indicates that compared with the on-state values, excess energy exists in both the *L1* and the *L2*. When the *C1* is fully discharged, the excess energy in the *L1* and the *L2* is transferred to the C_{smps} through the current path of *L1-*C_{smps}*-L2-D2-D1*. When the I_{L1} returns to the load level and the I_{L2} returns to zero, the energy recycling for the *C1* is completed.

The recycled energy stored in the C_{smps} is recovered to the load side during an IGBT off-state, using the boost circuit with the L_{smps}, T_{smps} and D_{smps} in discontinuous mode. The T_{smps} is first turned on, discharging the C_{smps} to the L_{smps} through the path of C_{smps}-L_{smps}-T_{smps}, which transfers the recycled energy from the C_{smps} to the L_{smps}. When the C_{smps} is discharged to a preset level, the T_{smps} is turned off, discharging the L_{smps} to the load side through the path of L_{smps}-D_{smps}. In this process, the stored energy in the L_{smps} is transferred to the load side. When the L_{smps} is fully discharged, the energy recovery process is completed.

This energy recovery circuit significantly reduces the extra switching losses caused by the snubber circuit, which is a major improvement on a basic RCD based snubber circuit. This advantage enables the use of large snubber capacitors that are capable of providing strong voltage sharing control effects without causing excessive losses in the snubber. The stored energy in the C_{smps} in the energy recovery circuit is also capable of providing self-powering for the gate drives and supporting the DC link voltage in certain cases [151].

However, the energy recovery circuit is unable to solve the reduction in the IGBT switching speed due to the energy storage components in the snubber circuit. For the IGBT, the reduced $\mathrm{d}V_{CE}/\mathrm{d}t$ rate and $\mathrm{d}I_C/\mathrm{d}t$ rate increase the switching losses.

RCD snubbers are useful in many ways, especially for reducing the V_{CE} overshoot in a CCL with a high stray inductance. For the control of the V_{CE} sharing between IGBTs in series connection, the RCD snubber is effective but not preferable considering that the snubber capacitor would reduce the IGBT switching speed and increase the switching losses of the IGBTs. Hence, other V_{CE} sharing control methods via IGBT gate control are attractive.

2.2.2 Active Gate Control Methods

Most active gate control methods, also referred to as gate side methods, use feedback control that responds to the divergence in the V_{CE} sharing of IGBTs in series connection. Voltage

regulation effects are achieved by controlling the IGBT V_{GE}. The V_{CE} divergence is measured, processed, and converted into intervention applied via IGBT gate control in various forms.

Compared with load side control methods, active gate control methods cause less reduction in IGBT switching speed and less extra switching losses. Many active gate control methods are developed, [152]–[186]. A few representative active gate control methods are summarised here.

2.2.2.1 Miller Effect Methods

The consistency of the V_{GE} timings in each IGBT switching stage between IGBTs in series connection is important for achieving evenly distributed V_{CE} sharing. However, in practice it is challenging to achieve that consistency of a high level due to the differences in IGBT parameters and gate drives. Adjustments during the Miller effect stage in IGBT turn-off can improve the V_{CE} sharing caused by poor timing consistency in the IGBT V_{GE}. The methods in [152], [153] use different approaches to apply interventions during the Miller effect stage in IGBT turn-off. It is noteworthy that the methods in [152], [153] refer to an early stage in IGBT development in which IGBTs are turned off in a manner related to charging the Miller capacitance. This is similar to power MOSFET turn-off and is different from the later fast IGBT turn-off with low gate resistance.

The method in [152] is an implementation of the Miller effect method using snubber capacitors, Figure 2.10 [152]. The MOSFETs S1 and S2 are on in an IGBT on-state and are turned off immediately before the following IGBT turn-off. Capacitive snubber effects are applied to the IGBT gate-collector terminals during the Miller effect stage and is removed by turning on the S1 and S2 when all the IGBTs in series reach the fast V_{CE} rising stage. By increasing the equivalent C_{GC} (Miller capacitance) of any IGBT that reaches the fast V_{CE} rising stage early, the difference in the turn-off timing at the start of the fast V_{CE} rising is reduced. With the improved consistency of the start of the fast V_{CE} rising between the IGBTs, the voltage divergence during the turn-off can be reduced.

The method in [152] enables the use of smaller snubber capacitances that reduces snubber losses compared with those of basic RCD methods. However, this method is less effective when using low IGBT gate resistance for fast IGBT turn-off when the MOS channel is cut off early in the fast V_{CE} rising. The snubber capacitor in a basic RCD configuration still affects the dV_{CE}/dt rates and the IGBT switching losses.

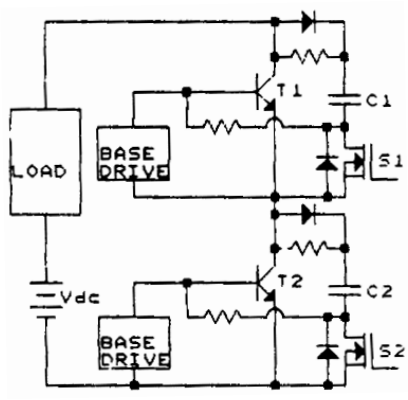


Figure 2.10: A voltage regulation method based on the Miller effect by snubber capacitors [152].

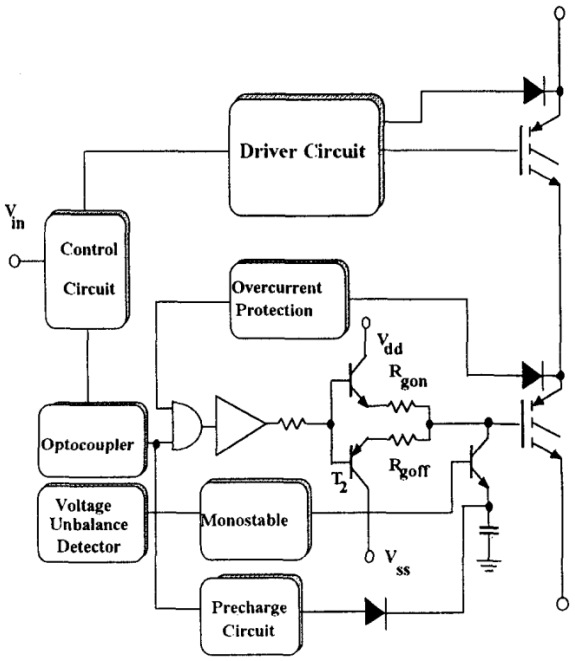


Figure 2.11: A voltage regulation method based on the Miller effect by gate current injection [153].

The method in [153] injects a current pulse to the gate terminal of a faster IGBT in terms of entering the Miller effect stage, Figure 2.11 [153]. This is to extend the Miller effect stage in the faster IGBT to improve the timing consistency of the fast V_{CE} rising. Once the voltage divergence is detected, a pre-charged capacitor is connected to the gate terminal of the faster IGBT which injects a current pulse to extend the Miller effect stage.

This method does not have a significant influence on the $\mathrm{d}V_{CE}/\mathrm{d}t$ or the $\mathrm{d}I_C/\mathrm{d}t$ during IGBT turn-off, and therefore does not have an obvious influence on IGBT switching losses. However, this method is also less effective when using low IGBT gate resistance for fast IGBT turn-off when the MOS channel is cut off early in the fast V_{CE} rising. Also, as the number of IGBTs in series increases, the control of the pre-charged capacitors for injecting the current pulse becomes more complicated in terms of determining the required profile of the individual current pulses for the IGBTs to achieve an evenly distributed V_{CE} sharing.

2.2.2.2 Gate Signal Timing Methods

IGBTs and gate drives are usually subject to parameter variations and control errors that lead to poor consistency of switching behaviours which results in divergence in the voltage sharing. Static and quasi-static differences between IGBTs and gate drives can be compensated for by adjusting the relative delays between IGBT driving signals using feedback control. The researches in [154], [161], [167], [168] presents a few representative gate signal timing methods.

The method in [154] uses separate delay times for turn-on and turn-off gate signals set by a transient balancing controller to control the V_{CE} sharing during IGBT switching, Figure 2.12 (a) [154]. In [154], the transient balancing controller is designed to be a time-discrete controller that is synchronised to central control signals. It compares the average V_{CE} to the individual V_{CE} of each IGBT to determine the delay times to be applied in the upcoming IGBT switching event.

This method is effective to compensate for the imbalance in the V_{CE} sharing caused by static and quasi-static differences in the IGBT and their gate drives, regardless of the specific

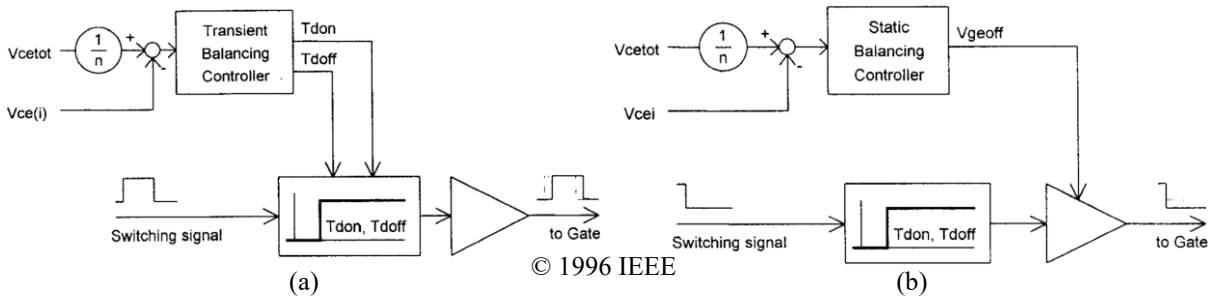


Figure 2.12: A voltage regulation method using (a) a transient balancing controller and (b) a static balancing controller [154].

types of differences. However, as it uses the measurements in the previous switching event to determine the upcoming delay settings, this method is less effective against the real-time differences that are less predictable in each switching cycle.

In practice, the turn-off delay settings required to achieve evenly distributed V_{CE} sharing in the turn-off are likely to compromise the V_{CE} sharing in the following off-state, and vice versa. In this case, adjustments to the turn-off delay settings are unable to regulate the V_{CE} sharing during both the turn-off and the following off-state. In [154], another static balancing controller for the off-state V_{CE} sharing is used to apply the V_{CE} sharing regulation by adjusting the gate driving voltage, Figure 2.12 (b) [154]. Similar to the previous Miller effect methods, the calculation of the turn-off delay and the gate driving voltage settings becomes more increasingly complicated as the number of IGBTs in series rises.

The delays from the central switching instruction signal to the outputs of gate drives are difficult to match closely between the IGBTs in series. This is partially due to the timing variations in the signal acquisition in the gate drive, and partially due to the parameter variations in the gate driving stage in the gate drive. These variations affect the consistency of the switching behaviours between the IGBTs in series, which can cause divergence in the V_{CE} sharing.

The timing variation is balanced in [161] by magnetically coupling all the IGBT gate wires with 1:1 ratio cores, Figure 2.13 [161]. Even with poor timing consistency between different gate drives, the coupling cores are capable of providing closely matched gate currents for the IGBTs. Therefore, the consistency of the IGBT gate currents is improved. This method does not require measurement or comparison of all the IGBT V_{CE} for the calculation of control settings. Hence, this method has an advantage in scaling up in terms of the number of IGBTs in series. Also, this method does not cause significant increases in IGBT switching losses.

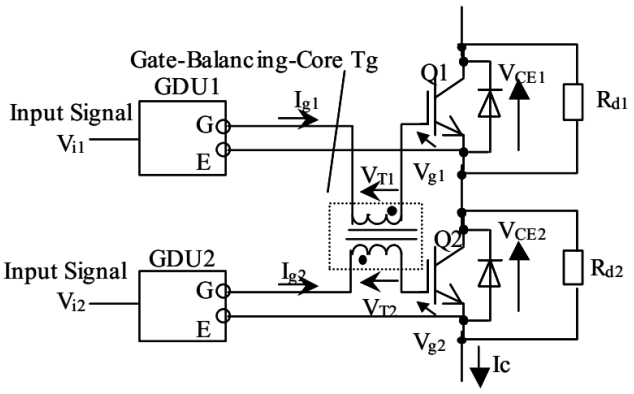


Figure 2.13: A voltage regulation method based on gate current synchronisation using magnetic coupling [161].

This method enforces synchronisation of all the IGBT gate currents. The V_{CE} sharing during IGBT switching can be improved when the dynamic IGBT characteristics during switching are closely matched. However, this can be challenging in practice, especially when using low gate resistance for fast IGBT turn-off. IGBTs are usually subject to parameter variations, which require different gate current profiles to achieve evenly distributed V_{CE} sharing. This is difficult with enforced synchronisation of the IGBT gate currents.

The method in [167] uses status feedback to adjust the switching signal timings for IGBT gate drives, Figure 2.14 [167]. The status feedback circuit responses to the V_{CE} difference in the off-state between the IGBTs in series, Figure 2.14 (a), and the microcontroller generates appropriate switching signal timings for the IGBT gate drives to regulate the voltage sharing in the following off-state, Figure 2.14 (b). In [168], an universal control scheme is used to extend the use of the method in [167] to multiple IGBTs in series, Figure 2.15 [168]. This extended control scheme is enabled by the use of a high-speed FPGA processor to compute appropriate switching signal timings for all the IGBT gate drives.

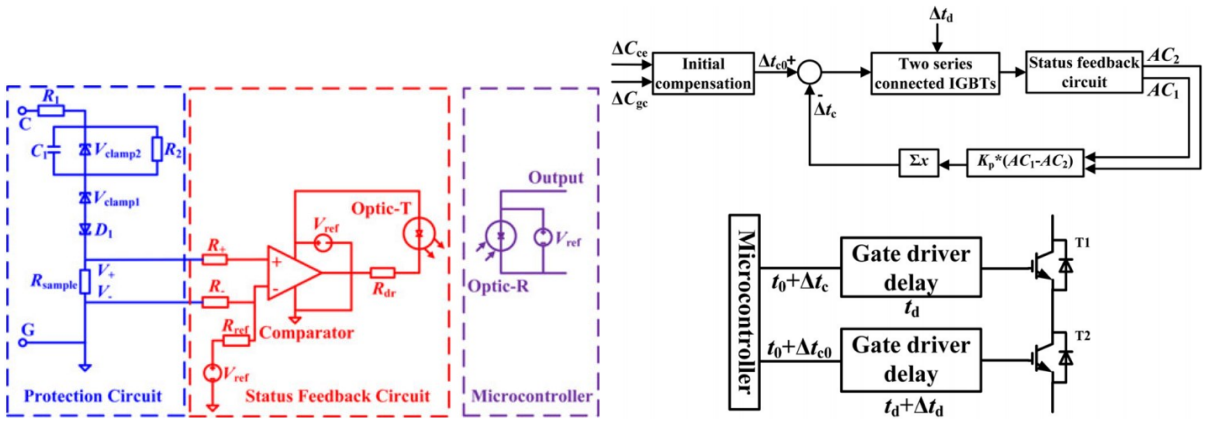


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Figure 2.14: A voltage regulation method based on gate timing control using status feedback: (a) the status feedback circuit, and (b) the feedback control loop [167].

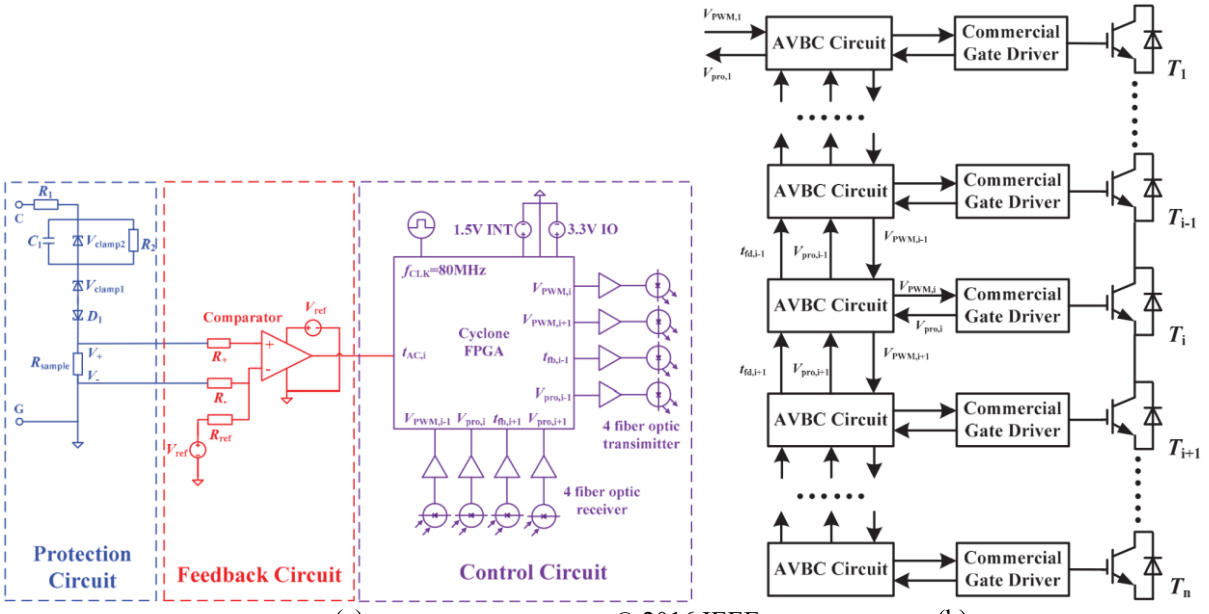

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Figure 2.15: A voltage regulation method based on gate timing control using status feedback: (a) the status feedback circuit and the control circuit, (b) the control loop for multiple IGBTs [168].

The method in [167] and its extended universal control scheme in [168] are practical and useful for scaling up the number of IGBTs in series due to the feedback control loop and the control algorithm that provide robust computing of switching signal timings for multiple IGBT gate drives. However, the regulation of the off-state V_{CE} sharing is likely to cause divergence in the voltage sharing in the turn-off transient prior to the off-state, which leads to differences in the turn-off losses. This is a general dilemma of the gate signal timing methods. Voltage sharing regulation at IGBT device level are attractive for the voltage sharing in the IGBT turn-off and the following off-state and turn-on in one IGBT switching cycle.

2.2.2.3 Gate Compensation and Active Zener Clamping

Gate compensation using a RC network [157] and V_{CE} clamping using Zener diodes [158] are methods to apply active IGBT V_{GE} control for V_{CE} sharing regulation. The method in [157] uses a RC network to regulate the V_{CE} sharing, Figure 2.16 [157]. In this method, the R_1 and R_2 are designed for static voltage sharing. The C_a is designed to be considerably higher than the C_b, about 10 times in [157], and is assumed to be relatively stable at approximately the average off-state IGBT V_{CE}. Due to the high C_a/C_b ratio, at IGBT turn-on a small discharging of the C_a discharges the C_b to the opposite voltage of the C_a.

During IGBT turn-off, the voltage of the C_b rises with the IGBT V_{CE}. In series connection if the IGBT V_{CE} exceeds the voltage of the C_a, the voltage of the C_b becomes positive and charges the IGBT V_{GE} through the diode D to reduce the IGBT V_{CE}. This mechanism is also applicable to the IGBT turn-on.

In terms of V_{CE} regulation for IGBTs in series, this method is effective for clamping the overvoltage of the V_{CE} and is simple to implement. However, the dynamic voltage regulation for IGBT switching is not included in this method.

The method in [158] uses multi-stage V_{CE} regulation that combines Zener diode clamping with gate $\mathrm{d}V_{CE}/\mathrm{d}t$ regulation by an external C_{GC}, Figure 2.17 [158]. In IGBT turn-off, before the IGBT V_{CE} reaches the Zener clamping voltage of the Z_1, the clamping circuit is essentially inactive despite a negligible charging current for the parasitic capacitance of the Z_1. This enables a high $\mathrm{d}V_{CE}/\mathrm{d}t$ rate for low turn-off losses.

In the turn-off, an IGBT with a higher V_{CE} reaches Zener clamping of the Z_1 earlier. After the Z_1 reaches Zener clamping as the V_{CE} increases, the C_1 effectively increases the total C_{GC} of the IGBT, which is designed to reduce the $\mathrm{d}V_{CE}/\mathrm{d}t$ rate. The reduced $\mathrm{d}V_{CE}/\mathrm{d}t$ rate of this IGBT mitigates the divergence in the V_{CE} sharing as an IGBT with a lower V_{CE} still has a higher $\mathrm{d}V_{CE}/\mathrm{d}t$ rate before reaching Zener clamping of the Z_1 at a later time. If the V_{CE} continues to

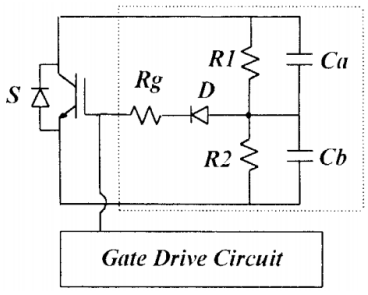


Figure 2.16: A voltage regulation method based on gate compensation using a RC network [157].

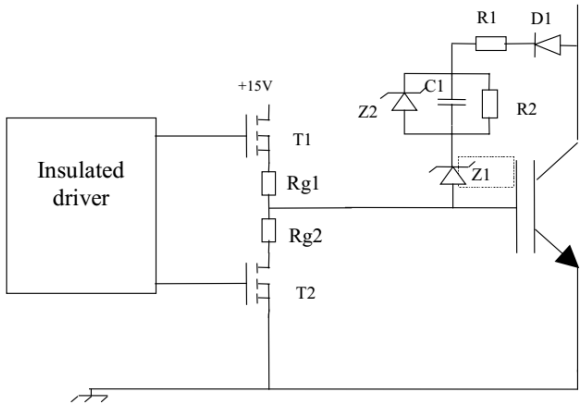


Figure 2.17: A voltage regulation method based on Zener clamping and gate compensation [158].

increase and both the Z_1 and the Z_2 reach Zener clamping, the IGBT gate will be charged and give rise to active V_{CE} clamping. The V_{CE} will be limited to a preset level determined by the combined Zener clamping voltages of the Z_1 and the Z_2. Therefore, the V_{CE} sharing in the turn-off is improved. In the IGBT off-state, the Z_1 is still under Zener clamping. The circuit of D_1-R_1-R_2-Z_1-R_{G2}-T_2 functions as a resistive potential divider in parallel to the IGBT to improve the V_{CE} sharing in the IGBT off-state.

This method combines partial V_{CE} regulation in IGBT turn-off with active V_{CE} clamping. In IGBT turn-on, the active V_{CE} clamping can limits the overvoltage. Besides some extra turn-off losses due to the partially reduced $\mathrm{d}V_{CE}/\mathrm{d}t$ in IGBT turn-off, this active clamping circuit also lacks adequate voltage regulation for IGBT turn-on.

The method in [166] integrates the key concepts of the multi-stage V_{CE} regulation and the active V_{CE} clamping in [158] with additional $\mathrm{d}V_{CE}/\mathrm{d}t$ regulation, Figure 2.18 [166]. Except for the R_1-C_1, the mechanisms of essentially the same V_{CE} regulation and active V_{CE} clamping circuity in Figure 2.18 will not be repeated here. In [166], the R_1-C_1 functions as a RC snubber for the Zener clamping circuit, and is designed to effectively increase the total C_{GC} of the IGBT for additional $\mathrm{d}V_{CE}/\mathrm{d}t$ regulation. This additional $\mathrm{d}V_{CE}/\mathrm{d}t$ regulation without limited by Zener clamping is effective for both IGBT turn-off and turn-on.

Zener diodes based active V_{CE} clamping and external C_{GC} based $\mathrm{d}V_{CE}/\mathrm{d}t$ regulation are simple to implement but require the assistance of static V_{CE} sharing resistors. Such a

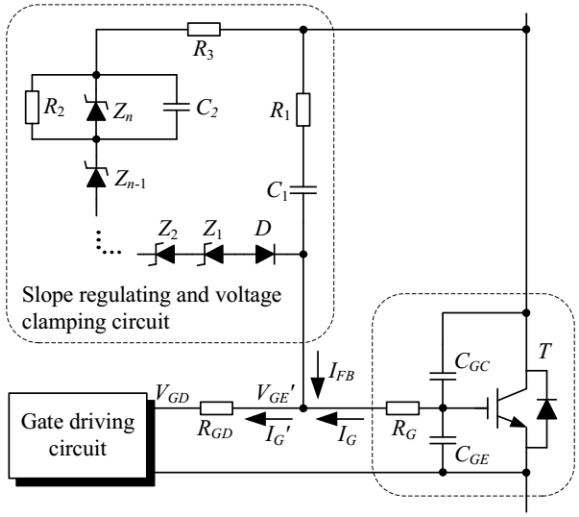


Figure 2.18: A voltage regulation method based on Zener clamping and $\mathrm{d}V_{CE}/\mathrm{d}t$ regulation [166].

combination as in [166] reduces the dynamic V_{CE} divergence but cannot eliminate it. The Zener clamping is preset at a fixed voltage level and is less adaptive. The dV_{CE}/dt regulation by an external C_{GC} can reduce the dV_{CE}/dt rates during IGBT switching and cause additional switching losses. It can also be difficult to apply this C_{GC} based dV_{CE}/dt regulation to fast IGBT turn-off using low gate resistance, in which the MOS channel is cut off early, as the V_{CE} may oscillate.

2.2.2.4 Active Gate Control – V_{CE} Clamping

Active gate control using operational amplifier (op-amp) based V_{CE} feedback control loop is capable of various control functions. The researches in [155], [156], [162] uses such active gate control to clamp the maximum V_{CE} during IGBT switching. The measured and scaled V_{CE} as a V_{CE} feedback signal is compared with a V_{CE} reference signal. When the V_{CE} feedback signal exceeds the V_{CE} reference signal, the V_{CE} feedback control loop raises the gate driving voltage and charges the IGBT gate to mitigate the rising of the V_{CE} and clamp the V_{CE}. With a well-designed V_{CE} feedback controller, the maximum V_{CE} can be clamped to a preset value.

The implementations of active gate control for V_{CE} clamping are different in [155], [156], [162]. In [155], an overvoltage control is applied at the gate driving stage to clamp the maximum IGBT V_{CE}, Figure 2.19 [155]. When the V_{CE} feedback signal exceeds the V_{CE} reference signal, the error signal is processed to raise the gate driving voltage and charge the IGBT gate to clamp the maximum V_{CE}.

In [156], a separate gate driving circuit is used for V_{CE} feedback control, Figure 2.20 [156]. The V_{CE} feedback signal, $V_{CE,fb}$, is compared with the V_{CE} reference signal V_{ref}. In the normal mode where the V_{CE} is below the clamping level, the TR3 and the TR4 are off while the TR5 is on. The TR1 and the TR2 are used to drive the IGBT gate normally. In the clamping mode where the V_{CE} exceeds the clamping level, the TR5 is turned off which turns off the TR2, and the TR4 is turned on which turns on the TR3. Thus, the TR4 charges the IGBT gate through RG2 to clamp the overvoltage.

In [162], the IGBT V_{CE} is converted into a V_{GE} reference for V_{CE} clamping, which is compared with another V_{GE} reference for switching by a selector circuit, and the higher one is selected and fed into a V_{GE} control circuit, Figure 2.21 (a) [162]. The selected V_{GE} reference is compared with the measured V_{GE} and the error signal is processed to drive two current sources to charge or discharge the IGBT gate, Figure 2.21 (b) [162]. In addition, a dV_{CE}/dt feedback loop is applied via the current source for charging the IGBT gate to adjust the dV_{CE}/dt rate.

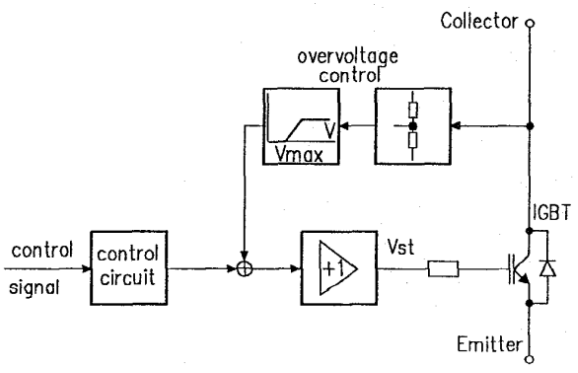


Figure 2.19: A voltage regulation method based on active gate control for over V_{CE} clamping [155].

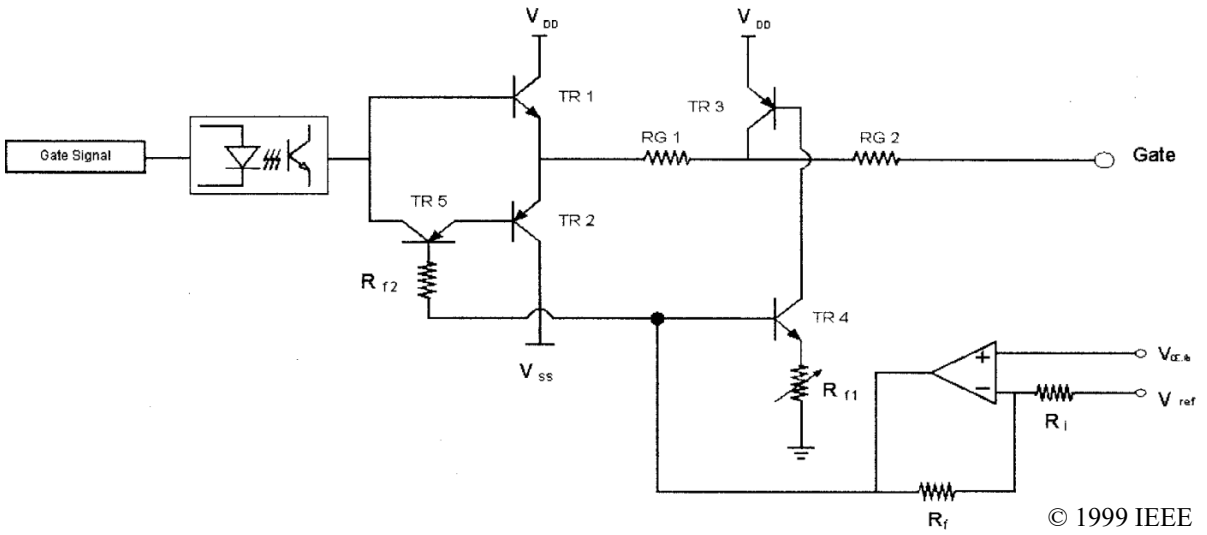
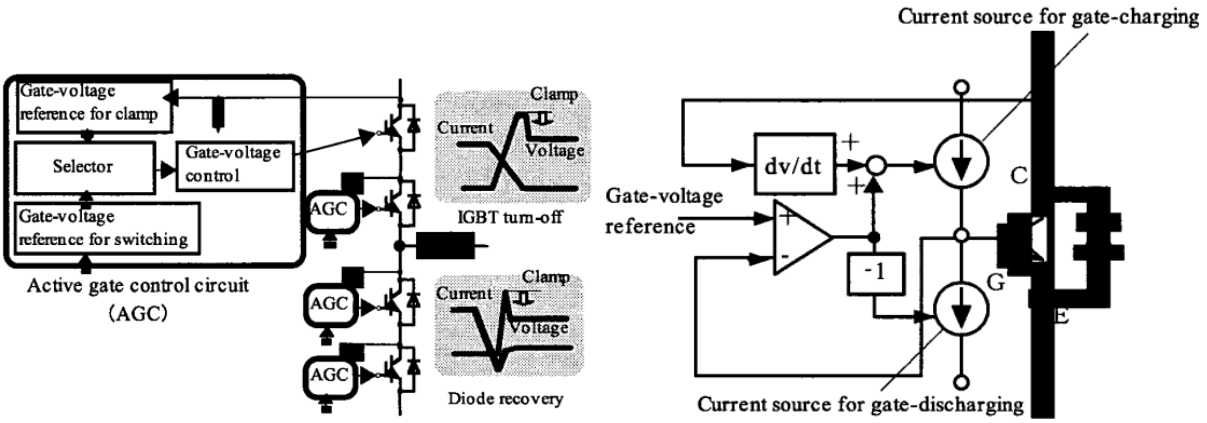


Figure 2.20: A voltage regulation method based on active gate control for V_{CE} clamping using a separate gate driving circuit [156].



(a) (b)

Figure 2.21: A voltage regulation method based on active gate control for V_{CE} clamping using (a) V_{GE} reference selection and (b) feedback control for V_{GE} [162].

The V_{CE} clamping using active gate control can be more adaptive compared with the aforementioned active Zener clamping. In terms of the V_{CE} sharing regulation, the simple V_{CE} clamping is a basic use of the active gate control. A well-designed V_{CE} reference signal for the active gate control can extend the V_{CE} sharing regulation to IGBT switching.

2.2.2.5 Active Gate Control – Primary-Replica Method

The method in [160] uses primary-replica control capable of adaptive V_{CE} sharing regulation for IGBT switching, Figure 2.22 [160]. It uses feedback control to drive "replica" IGBTs to follow the V_{CE} trajectory of a "primary" IGBT that performs uncontrolled switching. The V_{CE} of the "primary" IGBT is measured, scaled, and fed into the controller for a "replica" IGBT, in which the processed "primary" V_{CE} as the V_{CE} reference signal is compared with the measured and scaled V_{CE} of the "replica" IGBT as the V_{CE} feedback signal. The error signal is processed through the control circuit to control an auxiliary current source gate drive circuit in the "replica" IGBT controller to adjust the IGBT gate current so as to mitigate the V_{CE} divergence. Using feedback control with a processed V_{CE} trajectory as the V_{CE} reference signal enables the IGBTs in series to achieve closely matched V_{CE} trajectories.

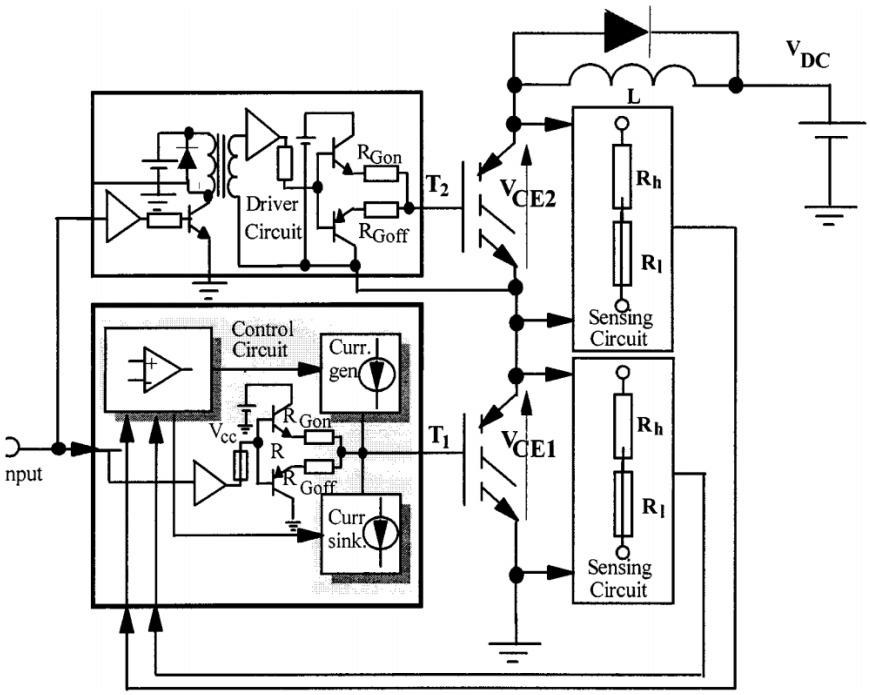


Figure 2.22: A voltage regulation method based on active primary-replica gate control [160].

This primary-replica method essentially uses a differential V_{CE} sharing regulation strategy, which is adaptive to changes in the $\mathrm{d}V_{CE}/\mathrm{d}t$ rate during switching. The auxiliary current source gate drive circuit is adaptive to the changes in the V_{GE} during switching due to changes in the I_C or parameter variations in the IGBT gate oxide. This method is more effective when the IGBTs are switched through the V_{GE} controlled active region where the V_{CE} can be controlled by charging or discharging the C_{GC}.

Propagation delays exist in the feedback control circuit and the gate driving stage, which are subject to variations caused by differences in the circuit and component parameters. The variations in the propagation delays and the variations in the IGBT parameters can cause an initial divergence in the V_{CE} sharing in a switching event, which is more difficult to mitigate in fast IGBT switching of high $\mathrm{d}V_{CE}/\mathrm{d}t$ rates where the propagation delays are no longer negligible. The "primary" IGBT needs to be carefully chosen to reduce this type of V_{CE} divergence due to lack of a preconditioning stage in the primary-replica method here. An actively generated V_{CE} reference signal can include a preconditioning stage capable of mitigating the respective initial differences between the IGBTs and the control circuits to reduce that type of initial V_{CE} divergence and improve the V_{CE} sharing later in a switching event.

2.2.2.6 Active Voltage Control

V_{CE} feedback control based on actively generated V_{CE} reference signal s is capable of more control functions, such as preconditioning IGBTs and control circuits before a switching event. Many researches have focused on the use of V_{CE} feedback control based on actively generated V_{CE} reference signals, often referred to as Active Voltage Control (AVC), on regulating the V_{CE} sharing, [169]–[186].

The basic V_{CE} feedback control loop in the AVC based methods, Figure 2.23 [172], is similar in the general form to those in the aforementioned active gate control methods. As shown

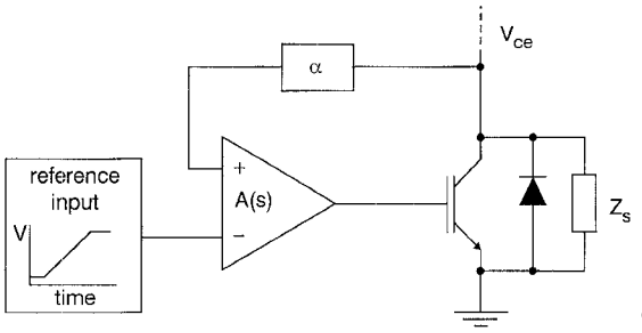


Figure 2.23: A voltage regulation method based on basic AVC [172].

in Figure 2.23, the V_{CE} is measured and scaled down to signal processing level by a potential divider network α. The scaled V_{CE} as the V_{CE} feedback signal and the actively generated V_{CE} reference input signal are compared and the error signal is processed in the controller A(s). The output of the A(s) drives the IGBT gate, often via a driving stage. The V_{CE} reference signal, which often consists of a few stages based on the IGBT characteristics and the circuit conditions, can be generated actively by a signal generator, e.g. an FPGA processor.

In [169]–[172], ramp signals are used in the V_{CE} reference signals to regulate the dV_{CE}/dt rates in the entire ([169], [171]) or the majority ([170], [172]) of the main V_{CE} rising in IGBT turn-off. This controlled V_{CE} rising is designed to use the V_{GE} controlled active mode, so that the dV_{CE}/dt rates can be regulated to the same profile to reduce the V_{CE} divergence.

To improve the consistency of the initial V_{CE} response, preconditioning stages are used in the V_{CE} reference signals for IGBT turn-off ([170], [172]) and turn-on, ([174], [175], [177]), Figure 2.24 [177]. For IGBT turn-off, the preconditioning stage here is a voltage step slightly higher than the scaled value of the on-state V_{CE}, the t_{RISE} stage in Figure 2.24. For IGBT turn-on, the preconditioning stage is a slow ramp that extends to slightly below the scaled value of the average off-state V_{CE}, the t_{FALL} stage in Figure 2.24. The preconditioning stages are expected to avoid excessive extra losses, [177].

The consistency of the initial V_{CE} response is affected by the respective initial differences between the IGBTs and the control circuits including the driving stages. The duration of the preconditioning stage is set to minimise those initial differences prior to the main V_{CE} rising or falling. Also, to ensure a secure IGBT on-state and a secure IGBT off-state against ElectroMagnetic Interference (EMI), the V_{CE} reference signal is designed to saturate the control circuit in the IGBT on-state and off-state, respectively, which leads to poor operating conditions for the

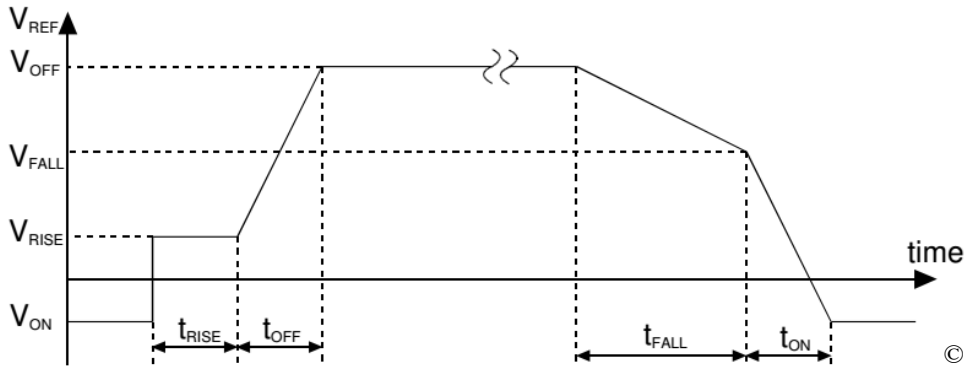


Figure 2.24: The V_{CE} reference signal of an AVC based voltage regulation method with preconditioning stages [177].

op-amps and the transistors in the control circuit in terms of control response. Another function of the preconditioning stage is to desaturate the control circuit to improve the response of the op-amps and the transistors in the control circuit.

The V_{CE} reference signal in [177] and those in other related early researches use a fixed clamping voltage throughout an IGBT off-state. This fixed off-state clamping voltage is set above the average off-state V_{CE} to accommodate the V_{CE} overshoot during IGBT turn-off with stray inductances in the CCL to enable load current commutation. However, such a fixed off-state clamping voltage above the average off-state V_{CE} is unable to actively regulate diverged V_{CE} sharing in the off-state.

To regulate the V_{CE} sharing in the off-state while accommodating the V_{CE} overshoot, a method using a V_{CE} reference signal with a lowered temporary clamp in the off-state is developed and tested in [180] and analysed in [186], Figure 2.25 [180]. In [180], the temporary clamp is applied a few microseconds after the fast V_{CE}-I_C transient in turn-off when the V_{CE} is expected to reach the original off-state clamping voltage due to V_{CE} divergence. The temporary clamping voltage is calibrated to be slightly above the average off-state V_{CE} for shoot-through protection.

In the temporary clamping stage, for an IGBT with a V_{CE} higher than the average off-state V_{CE}, the temporary clamp charges the IGBT gate via the V_{CE} feedback control and introduces a small electron current via the MOS channel to recover part of the depletion region for reducing the V_{CE} to the temporary clamping voltage. The current through this clamped IGBT charges the C_{OES} of the IGBT that is not clamped and increases its V_{CE}. Thus, the voltage sharing is regulated. The temporary clamp is removed when the V_{CE} sharing stabilises and is expected to remain stable if the temporary clamp is removed.

Specially designed sections in the V_{CE} reference signal and the feedback circuit for AVC based methods can provide additional control functions. A control scheme for IGBT dI_C/dt is discussed in [174]. A separate feedback loop for dV_{CE}/dt control is discussed in [175]. The control of the peak reverse recovery current of the FWD in the CCL during IGBT turn-on is

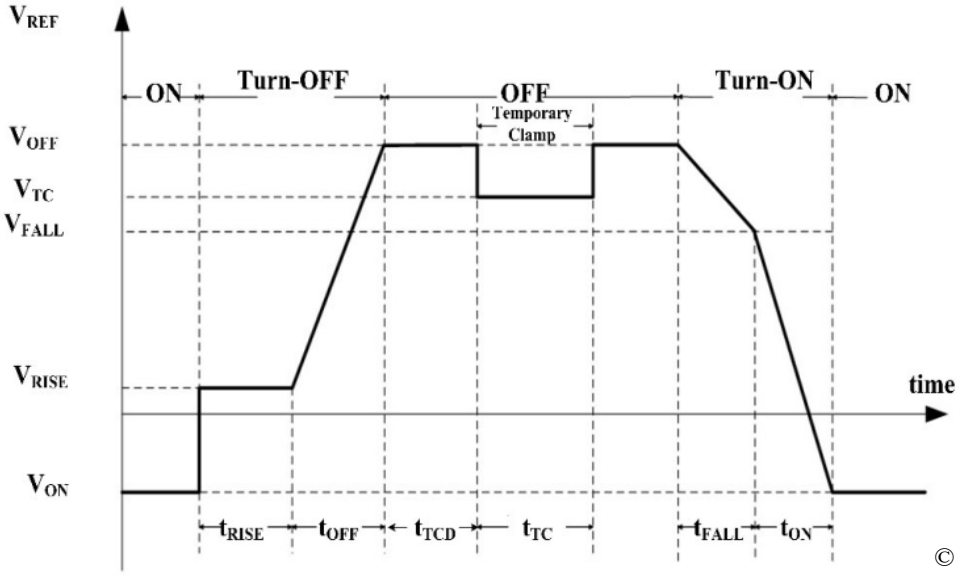


Figure 2.25: The V_{CE} reference signal of an AVC based voltage regulation method with temporary clamp [180].

discussed in [178]. An AVC based method is used for regulating the V_{DS} sharing of SiC MOSFETs in series connection, [184].

The extra switching losses caused by the preconditioning stage and the dV_{CE}/dt control, the stability concerns for the temporary clamp, and a few practical issues of the previous use of AVC for the V_{CE} sharing regulation are discussed in [185]. These concerns and issues can be improved to achieve more efficient V_{CE} sharing regulation.

2.3 Research Motivations

Operating IGBTs in series connection is required in different forms in high voltage converters and their related systems. The research on the operation of IGBTs in series connection facilitates the development of modern high power and HVDC related technologies.

The two-level and three-level VSCs depend on the operation of IGBTs in series connection to achieve high output voltages. The performance of the IGBTs in series connection determines the performance of those high voltage VSCs to a great extent.

The MMC uses submodule-based switching without using IGBTs in series connection in the MMC submodules. In the MMC, the control of the IGBT V_{CE} is converted into the control of the submodule capacitor voltages. The commonly used half-bridge MMC submodules require HCBs for the protection against DC side short circuit faults. The use of IGBTs in series connection is a popular solution for the semiconductor branch in HCBs. The operation of IGBTs in series connection is involved in the operation of the MMC, although indirectly.

The AAC uses submodule level switching that resembles the MMC concept. As key components in the AAC, the director switches which control the conduction period of each arm are composed of IGBTs in series connection.

The CTL converter uses an integration of modularised multi-level switching and the operation of IGBTs in series connection within its submodules. The operation of IGBTs in series connection is of critical importance in the CTL converter and determines various performance aspects of the CTL converter.

The operation of IGBTs in series connection is involved in the aforementioned mainstream technical tracks of high voltage converters, either directly in the switching events, or indirectly in the protection aspect. The research on the use of IGBTs in series connection can improve the reliability and the performance of modern high voltage converters. High performance methods for improving the voltage sharing of IGBTs in series connection can reduce the switching losses and the differences in the thermal stress of the IGBTs. These benefits become significant in HVDC related power electronic systems, where the DC bus voltage is high and IGBTs in large numbers are to be operated in series. With low-loss V_{CE} sharing regulation methods, the use of IGBTs of a lower voltage class in series can provide the same total voltage and power handling capabilities at reduced total operating losses compared with the use of IGBTs of a higher voltage class in series, especially at high switching frequencies [178].

2.3.1 Negative Effects of Uncontrolled V_{CE} Divergence

In the operation of IGBTs in series connection, the V_{CE} sharing between the IGBTs is a major challenge, especially in the turn-off and the off-state. Uncontrolled divergence in the turn-off V_{CE} sharing is risky, especially in a situation of multiple IGBTs in series where the total DC link voltage is significantly higher than the maximum rated V_{CE} of one IGBT in series.

In uncontrolled turn-off of series-connected IGBTs, an IGBT in series may start to turn off and establish its V_{CE} earlier or experience a higher $\mathrm{d}V_{CE}/\mathrm{d}t$ rate compared with the other IGBTs in series. Either case can lead to a higher V_{CE} sharing of an IGBT compared with the other IGBTs. In IGBT turn-off under inductive load conditions, the coexistence of high voltage and high current during the turn-off imposes thermal stress on the IGBTs, especially for the IGBTs leading in V_{CE} sharing. The IGBTs with higher thermal stress caused by higher V_{CE} sharing are more likely to experience a negative influence on the lifespan.

Regarding overvoltage faults, the higher V_{CE} sharing of an IGBT in series reduces the voltage safety margin and the voltage redundancy of the IGBT branch. Under short circuit fault conditions, the IGBTs leading in V_{CE} sharing are more vulnerable to thermal breakdown or overvoltage breakdown when turning off the short circuit current. If any of those IGBTs leading in V_{CE} sharing fails, it is likely that another IGBT with a high V_{CE} sharing prior to the first breakdown event will rapidly reach its maximum V_{CE} limit and break down subsequently. Without adequate protection or redundancies, the remaining IGBTs in the series string will be subject to a chain reaction of breakdowns.

2.3.2 Approaches at IGBT Device Level for Improving V_{CE} Sharing

The FS IGBT concept and similar variants are widely adopted in modern Si IGBTs. However, in terms of the V_{CE} sharing, some FS IGBTs are more sensitive to the internal parameter variations and the gate driving errors, depending on the N base design of the IGBT, e.g. the N-drift region and the N buffer profiles. Different N base designs for the same voltage class can lead to different degrees of V_{CE} divergence caused by the same degree of parameter variations or gate driving errors. These parameter variations or gate driving errors cannot be fully avoided in practice, and the resulting V_{CE} divergence is commonly seen in uncontrolled switching of IGBTs in series connection.

The research here aims to, at IGBT device level, study the basic mechanisms of the V_{CE} divergence in hard-switched fast turn-off of modern FS IGBTs in series connection in typical use, and explore solutions to the concerned V_{CE} divergence from different approaches. To better mitigate the V_{CE} divergence, it is necessary to first establish an understanding of the basic mechanisms of the V_{CE} divergence between the IGBTs during such turn-off. This provides guidance on the approaches to the mitigation and the regulation of the V_{CE} divergence. The resulting mitigation and regulation methods here aim to reduce the drawbacks of the V_{CE} sharing control methods reported in previous researches where possible, especially the extra turn-off losses.

After an introduction to the relevant basics of IGBT physics, hard-switched fast turn-off of two series-connected FS IGBTs is discussed. This discussion includes a few basic turn-off processes of FS IGBTs in typical use and the V_{CE} diverging effects of a few IGBT parameter

variations and gate driving errors. To gain a further understanding of the V_{CE} divergence, a 2D Finite Element Method (FEM) model of an FS IGBT is developed in Silvaco ATLAS. Two-in-series turn-off simulations using this FS IGBT model in an inductive CCL are conducted in Silvaco ATLAS MixedMode to study the effects of the IGBT parameter variations and the gate driving errors on the turn-off processes related to the V_{CE} divergence in a controlled environment.

Based on the understanding of the basic mechanisms of the turn-off V_{CE} divergence, three types of approaches to the mitigation and the regulation of the turn-off V_{CE} divergence are discussed. Regarding the IGBTs themselves, a few adjustments to IGBT operating conditions and IGBT internal parameters that are expected to mitigate the V_{CE} divergence are discussed and tested in Silvaco simulations. These adjustments are within the existing technical tracks in the IGBT industry.

As discussed earlier, in addition to the V_{CE} sharing regulation capabilities in a full IGBT switching cycle, the AVC with an appropriate V_{CE} reference signal is also capable of preconditioning the IGBTs and the control circuits to improve the initial V_{CE} response and the initial V_{CE} sharing. Hence, the AVC is used as the basis of the active V_{CE} sharing regulation methods here. Two active V_{CE} sharing regulation methods using AVC gate drives are discussed and tested in experiments, including a direct method via IGBT gate control and an external method via additional SiC MOSFETs.

Compared with prior researches on this topic, the direct V_{CE} sharing regulation method here focuses on mitigating the V_{CE} divergence as it tends to emerge in both the fast V_{CE}-I_C transient and the following tail time. A differential V_{CE} sharing regulation strategy is used, which reduces the extra losses. This avoids considerable V_{CE} divergence to be reached between the IGBTs and reduces the differences in the turn-off losses while enables a high $\mathrm{d}V_{CE}/\mathrm{d}t$ rate in the fast V_{CE} rising. The preconditioning strategy is redesigned to reduce the extra losses. This method is experimentally tested using commercial FS IGBTs of a recent generation.

The new external V_{CE} sharing regulation method incorporates the use of a SiC MOSFET controlled by an AVC gate drive in parallel to each of the IGBTs in series, allowing the load-carrying IGBTs to operate uncontrolled and hard-switched turn-off. This external V_{CE} sharing regulation method also mitigates the V_{CE} divergence as it tends to emerge and uses the same differential V_{CE} sharing regulation strategy. This method provides low-loss V_{CE} sharing regulation effects similar to those of the direct V_{CE} sharing regulation method without extra stress imposed on the IGBT MOS gate. This method is also experimentally tested using the same test setup for the direct V_{CE} sharing regulation method with a few modifications in circuit parameters.

Chapter 3 Internal Mechanisms and Simulations of the Turn-off V_{CE} Divergence

3.1 Practical Conditions for the Turn-off V_{CE} Sharing

In normal practice, IGBTs and gate drives of respectively the same models are used to reduce the control requirements for achieving evenly distributed V_{CE} sharing in the turn-off of IGBTs in series connection. Physical differences introduced in semiconductor processing and packaging usually exist between IGBT chips of the same model and specifications and normally lead to parameter differences between IGBTs of the same model. These parameter differences cause differences in turn-off characteristics between the IGBTs of the same model. In uncontrolled turn-off of IGBTs in series, those differences in IGBT turn-off characteristics cause divergence in the turn-off V_{CE} sharing.

Differences in IGBT gate driving can also cause divergence in the turn-off V_{CE} sharing. The switching signal acquisition and the response of the gate drives are subject to various differences in practice. Similarly, in uncontrolled IGBT turn-off, these gate driving differences can cause variations in the timing when the MOS channel conduction in an IGBT is constrained and the continuing ambipolar current in the CSR starts to expand the depletion region in the IGBT N base. These gate timing variations can cause V_{CE} divergence in the IGBT turn-off.

To focus on the basic mechanisms at device level of the V_{CE} divergence in the IGBT turn-off, a two-in-series situation is considered under inductive load conditions with a lumped stray inductance in the CCL. The stray inductance in the CCL cannot be reduced easily in high voltage power electronic systems that can benefit from the operation of IGBTs in series connection due to insulation requirements. Other external factors that may affect the turn-off voltage sharing also exist, e.g. unevenly distributed parasitic capacitances between the IGBTs to ground. These external factors are not part of the focus of this thesis and are intended for future research.

3.2 Experiment Examples of the Turn-off V_{CE} Divergence

For an impression of the turn-off V_{CE} divergence in practice, Figure 3.1 and Figure 3.2 show two experiment examples of uncontrolled turn-off of two FS IGBTs of a recent generation in series connection, sampled at different times in a continuous test period with unchanged circuit control. The two IGBTs are connected directly in series inside a half-bridge IGBT module, Fuji Electric 2MBI650VXA-170E-50 rated 1700 V and 650 A for each IGBT, without any snubber circuit attached except for the internal anti-parallel FWDs. The two IGBTs in series are operated as the main switch in a basic boost converter circuit using the double pulse test method in [172], which enables testing power devices without high throughput power. The related basic mechanisms at device level of the V_{CE} divergence will be discussed later.

In the experiment figures, $V_{CE,LS}$ refers to the V_{CE} of the Lower Side (LS) IGBT in terms of electric potential, similarly $V_{CE,HS}$ refers to the V_{CE} of the Higher Side (HS) IGBT, $V_{CE,Mean}$ refers to $(V_{CE,LS} + V_{CE,HS})/2$, and $V_{CE,Diff.}$ refers to $(V_{CE,LS} - V_{CE,HS})$. $V_{GE,TERM,LS}$ refers to the terminal V_{GE} of the lower side IGBT measured at the G-E terminals of the IGBT package, which is different from the chip V_{GE} of the lower side IGBT chips due to the internal gate resistance.

$I_{C,PKG}$ refers to the package current measured at the higher side "C" terminal of the IGBT package, which includes the small current through the internal anti-parallel FWDs in the IGBT off-state under the test conditions here. The same annotations are also used in other figures presenting experiment results.

The results shown in Figure 3.1 and Figure 3.2 are sampled during a continuous test period with unchanged circuit control including the input voltage and the double pulse switching signal. Due to device availability and input power limitations and for safety considerations, the DC link voltage and the inductive load current are set to 1000 V and 55 A, respectively, for the two IGBTs in series.

During the test, the V_{CE} divergence observed was changing constantly and apparently randomly. In the nominal off-state the $V_{CE,LS}$ was often found to be above the $V_{CE,HS}$, such as shown in Figure 3.1. In Figure 3.1, the V_{CE} divergence reaches a quasi-static state approx. 30 µs after the fast V_{CE}-I_C transient as the I_C reaches the leakage level. When the $V_{CE,LS}$ is above the $V_{CE,HS}$, in the following turn-on an overshoot in the $V_{CE,HS}$ can sometimes be observed, such as shown in Figure 3.1. This is due to a timing lead in the MOS channel cut-off in the lower side IGBT mainly caused by early triggering of the digital gate drive, which will be discussed later. Due to the insulation limits of the voltage probes, only the terminal V_{GE} of the lower side IGBT can be measured at the IGBT package terminals. Because of the internal gate resistance inside the IGBT package, the measured terminal V_{GE} is different from the chip V_{GE}, but the terminal V_{GE} can still indicate the key timings of the chip V_{GE}.

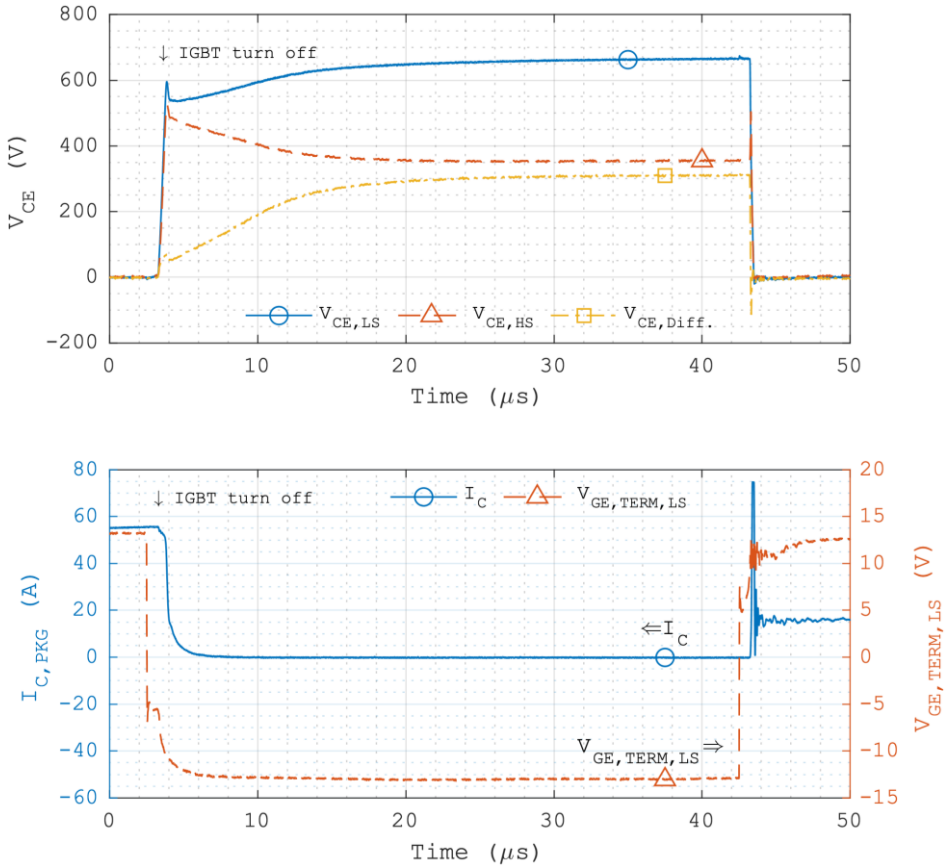


Figure 3.1: Uncontrolled turn-off of two IGBTs in series with large V_{CE} divergence.

Occasionally, in the off-state the $V_{CE,LS}$ was slightly below the $V_{CE,HS}$, such as shown in Figure 3.2. In such cases, sometimes an evenly distributed V_{CE} sharing can be observed late in the off-state, and in the following turn-on overshoot is not observed in the $V_{CE,LS}$ or the $V_{CE,HS}$.

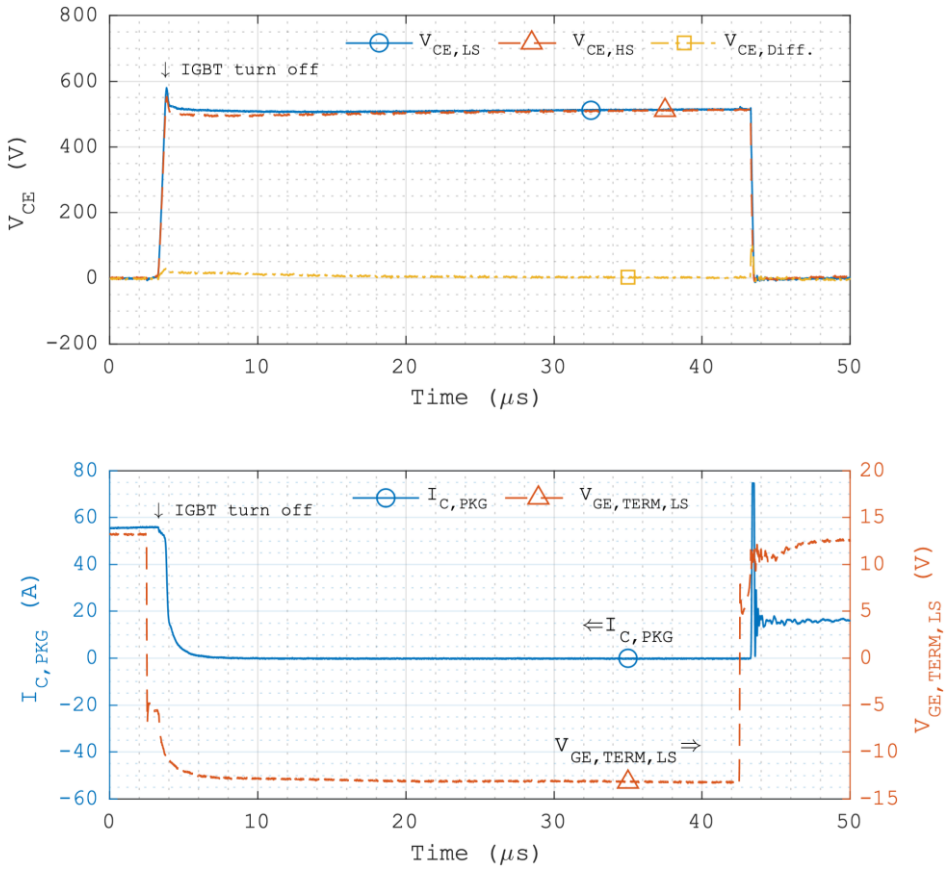


Figure 3.2: Uncontrolled turn-off of two IGBTs in series with small V_{CE} divergence.

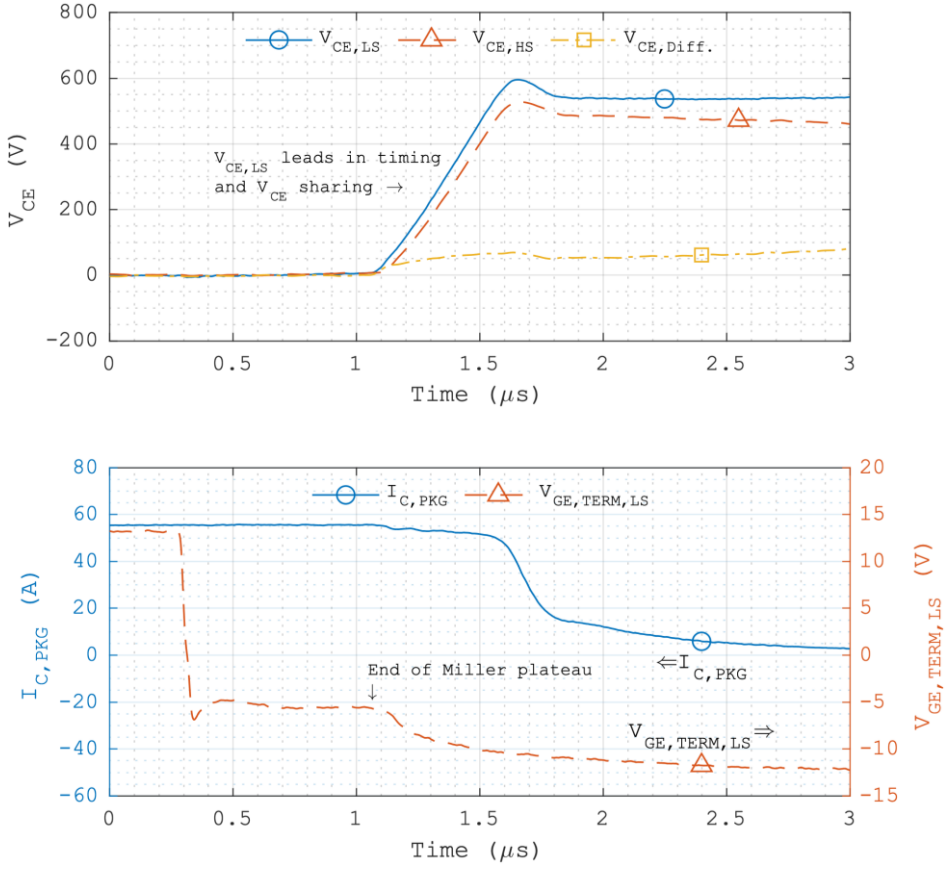


Figure 3.3: Detailed turn-off of two IGBTs in series with large V_{CE} divergence.

Figure 3.3 shows a detailed view of the IGBT turn-off event shown in Figure 3.1. In Figure 3.3, the largest V_{CE} divergence in the fast V_{CE}-I_C transient is considerably lower compared with that in the following off-state as shown in Figure 3.1. Because of the stray inductance in the CCL, the IGBT I_C starts to fall rapidly after the total V_{CE} exceeds the V_{DC}. As the I_C falls rapidly, the V_{CE} divergence decreases slightly until the V_{CE} overshoot completes and the turn-off process enters the tail time, where the V_{CE} divergence starts to increase again. In Figure 3.3, the $V_{CE,LS}$ remains above the $V_{CE,HS}$ from the first point of significant divergence. It is also noteworthy that in terms of timing, the end of the V_{GE} Miller plateau is closely related to the start of the fast V_{CE} rising at a high dV_{CE}/dt rate, which reflects the discussion in section 1.5 regarding the cut-off of the MOS channel conduction early in the fast V_{CE} rising enabled by the degree of freedom provided by the ambipolar transport of the high-level excess carriers in the N base.

3.3 Basic Diverging Mechanisms of the Turn-Off V_{CE} Sharing

This section concerns the turn-off V_{CE} sharing of two n-channel FS IGBTs in direct series connection without any snubber applied. The discussion first considers an IGBT-only situation as the anti-parallel FWD in an IGBT module is reverse-biased when the IGBT V_{CE} is positive, e.g. in the IGBT on-state and switching under inductive load conditions. The influence of the anti-parallel FWDs on the V_{CE} sharing will be discussed later. It is reasonable to assume typical use of modern high voltage vertical Si FS IGBTs of the same active chip area, the same uniform doping profile of the N-drift region, and diverging factors of small degrees as in practical situations. Hence, it can also be assumed that in the IGBT turn-off and nominal off-state, the depletion region will not punch through the N-drift region and reach the N buffer. The discussions related to the turn-off V_{CE} diverging mechanisms in this thesis consider only the predominant factors.

3.3.1 IGBT Internal Parameter Variations and Gate Driving Errors

Following the discussions in section 1.5, at IGBT device level, the V_{CE} divergence between the series-connected IGBTs in turn-off is due to the interaction between the IGBTs caused by differences in the internal carrier transport in the turn-off. A few IGBT parameter variations and gate driving errors that can cause significant turn-off V_{CE} divergence are more likely to be encountered. Including the factors considered in [183], seven IGBT parameter variations and gate driving errors are discussed and simulated here:

1) Output delay between the IGBT gate drives, 10 ns relative delay to be simulated.
2) Variation in the doping profile of the backside P emitter, 5% relative variation in concentration to be simulated.
3) Variation in the total IGBT gate resistance, 1% relative variation to be simulated.
4) Variation in the IGBT gate oxide thickness, 1% relative variation to be simulated.
5) Variation in the doping concentration of the FS N buffer, 5% relative variation to be simulated.

6) Variation in the carrier lifetimes, 5% relative variations in both the low-level τ_{n0} and τ_{p0} in the SRH and the Auger recombination models to be simulated.

7) Variation in the IGBT lattice temperature, 5 K relative difference in the thermal boundary temperature to be simulated.

3.3.2 Basic Scenarios of the Turn-Off V_{CE} Divergence in the Fast V_{CE}-I_C Transient

Following the discussions in section 1.5, the turn-off V_{CE} divergence develops differently in the fast V_{CE}-I_C transient and in the tail time, due to the changes in the predominant carrier transport mechanisms in the IGBTs.

In the fast V_{CE}-I_C transient, the differences in the timing of the MOS channel cut-off and the initial excess carrier profile affect the following depletion progress in the N base. Following the discussions in section 1.5, due to the same I_C and the same doping profile of the N-drift region, a delay in the timing of the MOS channel cut-off postpones the depletion progress in the N base, causing a delay in the fast V_{CE} rising. Also, a higher initial excess carrier profile reduces the shrinking of the CSR and the related expansion of the depletion region in the N base, causing reduced $\mathrm{d}V_{CE}/\mathrm{d}t$ rates in the fast V_{CE} rising. These two basic scenarios both lead to lower V_{CE} sharing in the fast V_{CE}-I_C transient and are applicable to all the IGBT parameter variations and gate driving errors considered in this thesis. The excess carrier profiles of the IGBTs at the end of the fast V_{CE}-I_C transient affect the V_{CE} divergence in the tail time.

In the fast V_{CE}-I_C transient, in the depletion region the main current component is the hole current, the holes of which increase the electric field gradient. Impact ionisation exists in the depletion region, and the generated electrons are propelled towards the N buffer, while simultaneously the generated holes are propelled towards the P base. This carrier transport reduces the shrinking of the CSR and the related expansion of the depletion region. In the IGBT with a higher V_{CE}, the impact ionisation in the depletion region is stronger, which leads to further reduction in the expansion of the depletion region compared with the situation in the IGBT with lower V_{CE}. Hence, the impact ionisation here in the depletion region tends to reduce the increase in the V_{CE} and mitigate the V_{CE} divergence.

Dynamic avalanche, although unlikely in the typical use of modern IGBTs, has an effect on the V_{CE} divergence similar to that of impact ionisation considering the electron-hole pairs generated in the depletion region. In a typical situation where the V_{CE} divergence is caused by small parameter variations, the IGBT with a higher V_{CE} has a higher peak electric field in the depletion region. Often, dynamic avalanche is first triggered in a small area of a high electric field and causes concentrated current flow in that area, where the peak electric field is saturated at the critical electric field. When dynamic avalanche is reached, in the IGBT with a higher V_{CE}, the generated electron-hole pairs result in further reduction in the expansion of the depletion region, which tends to mitigate the V_{CE} divergence.

3.3.3 Basic Scenarios of the Turn-off V_{CE} Divergence in the Tail Time

The turn-off V_{CE} divergence in the tail time is affected by the combined effects of carrier drift and carrier diffusion in the undepleted part of the N base under the same I_C and the influence of

carrier recombination. Following section 1.5, due to the same I_C and the same doping profile of the N-drift region, the types of the differences in the initial excess carrier profile in the tail time include: (1) one IGBT has an extended initial remaining CSR, and (2) one IGBT has an initial remaining CSR of a higher excess carrier profile. These two basic scenarios are applicable to all the IGBT parameter variations and gate driving errors considered in this thesis.

In the tail time, the I_C becomes comparable to the hole diffusion current in the undepleted part of the N base towards the depletion region, and the electrons from the CSR can only be propelled away from the depletion region. Therefore, this hole diffusion current is important in the V_{CE} diverging process. With the same I_C and the same doping profile in the N-drift region, the position of the depletion edge determines the V_{CE} sharing. Hence, the focus is first on the hole diffusion current in the undepleted part of the N base towards the depletion region, considering the two basic scenarios here.

In the first scenario where one IGBT has an extended initial remaining CSR, in the undepleted part of the N base the holes will produce an enhanced diffusion current towards the depletion region due to additional supply of holes from the broader inner section of the remaining hole distribution. In the second scenario where one IGBT has an initial remaining CSR of a higher excess carrier profile, the holes in the undepleted part of the N base will also produce an enhanced diffusion current towards the depletion region due to additional supply of holes from the inner section of the remaining hole distribution of a higher profile.

In the two basic scenarios here, in the undepleted part of the N base the diffusion-drift relation of the holes is biased differently between the two IGBTs in series under the same I_C. In general, the diffusion-drift relation of those holes is biased towards diffusion in the IGBT with an enhanced hole diffusion current in the undepleted part of the N base towards the depletion region. At the depletion edge, the resulting electric field also biases the diffusion-drift relation of the electrons towards diffusion. These effects combined recover some N-type depletion region from the depletion edge in the N base and expand the hole distribution to match the recovery. As a result, the depletion region shrinks and the V_{CE} of this IGBT decreases. The shrinking of the depletion region reduces the generation current in it, while in the undepleted part of the N base the hole concentration decreases due to recombination, reducing the hole diffusion current towards the depletion region. In the tail time, these two effects reduce the differences in the output current characteristics between the two IGBTs, which assists in reaching a quasi-static state of the V_{CE} sharing.

Meanwhile, in the other IGBT, the relatively inadequate hole diffusion current towards the depletion region in the undepleted part of the N base requires enhanced drift of holes in it towards the depletion region under the same I_C, and the drift of electrons related to the same electric field is also enhanced. This results in expansion of the depletion region that leads to an increase in the V_{CE}. The generation current in the expanding depletion region becomes higher, while in the undepleted part of the N base the hole concentration also decreases due to recombination, reducing the hole diffusion current towards the depletion region. These two effects also reduce the differences in the output current characteristics between the two IGBTs, which assists in reaching a quasi-static state of the V_{CE} sharing.

Hence, regarding the two basic scenarios here, in the tail time the V_{CE} sharing will be lower for the IGBT with an extended initial remaining CSR and/or an initial remaining CSR of a higher excess carrier profile. Individual cases will be discussed later.

3.3.4 Combinations of the Basic V_{CE} diverging Scenarios

Following the discussion in section 3.3.2, in the IGBT turn-off, a V_{CE} diverging factor which results in a lower initial excess carrier profile and/or a relative timing lead in the MOS channel cut-off would also lead to higher V_{CE} sharing of the IGBT in the fast V_{CE}-I_C transient. Following the discussion in section 3.3.3, these two cases both lead to higher V_{CE} sharing in the tail time, which is consistent with the V_{CE} diverging feature in the fast V_{CE}-I_C transient. In this sense, regarding the basic V_{CE} diverging scenarios discussed in sections 3.3.2 and 3.3.3, their respective V_{CE} diverging features in the fast V_{CE}-I_C transient and the following tail time are consistent.

An individual V_{CE} diverging factor concerned in this thesis can be resolved into a combination of the basic V_{CE} diverging scenarios in the fast V_{CE}-I_C transient and the tail time discussed in sections 3.3.2 and 3.3.3. The seven cases included in section 3.3.1 will be discussed in this manner. Three aspects will be discussed regarding the V_{CE} divergence: a) the on-state excess carrier profile prior to the turn-off, b) the V_{CE} diverging mechanisms in the fast V_{CE}-I_C transient and c) in the tail time, respectively. One diverging factor is discussed at a time with the following assumptions: a two-in-series IGBT-only situation, the same active chip area, and a steady on-state prior to the turn-off. The following individual discussions apply to the IGBT with a specified V_{CE} diverging factor relative to the other IGBT.

1) An output delay in an IGBT gate drive:
   a) The same on-state excess carrier profile.
   b) In the fast V_{CE}-I_C transient, the gate drive output delay causes late MOS channel cut-off, which delays the depletion progress and causes a lower V_{CE} sharing.
   c) In the tail time, the delayed depletion progress causes an extended initial remaining CSR from the fast V_{CE}-I_C transient, which leads to a lower V_{CE} sharing and further enlarges the V_{CE} divergence.
2) An IGBT with a higher P emitter doping profile:
   a) In the on-state, the higher P emitter doping profile causes enhanced hole diffusion from the P emitter and a higher excess carrier profile.
   b) In the fast V_{CE}-I_C transient, the higher excess carrier profile causes a slower depletion progress, leading to a lower V_{CE} sharing.
   c) In the tail time, the slower depletion progress causes an extended initial remaining CSR with a higher excess carrier profile from the fast V_{CE}-I_C transient, which leads to a lower V_{CE} sharing and further enlarges the V_{CE} divergence.
3) An IGBT with a higher gate resistance R_G:
   a) The same on-state carrier profile due to the same on-state V_{GE} despite a higher R_G.

b) In the fast V_{CE}-I_C transient, the higher R_G causes slower gate discharging, leading to late MOS channel cut-off, which delays the depletion progress and causes a lower V_{CE} sharing.

c) In the tail time, the delayed depletion progress causes an extended initial remaining CSR from the fast V_{CE}-I_C transient, which leads to a lower V_{CE} sharing and further enlarges the V_{CE} divergence.

4) An IGBT with a higher gate oxide thickness:

a) In the on-state, the higher gate oxide thickness causes a weaker inversion layer at the same on-sate V_{GE}, which leads to a slightly lower excess carrier profile.

b) In the fast V_{CE}-I_C transient, during the initial gate discharging, the higher gate oxide thickness results in lower gate capacitances and lower gate charges at the same V_{GE}, and a higher gate plateau voltage at the same $I_{C,sat}$. Therefore, the initial discharging voltage across the gate resistance is higher at the same off-state gate driving voltage, which leads to a higher gate discharging current. These effects all lead to early MOS channel cut-off, and the lower excess carrier profile leads to a faster depletion progress. These two situations both lead to a higher V_{CE} sharing.

c) In the tail time, both the early MOS channel cut-off and the lower excess carrier profile result in a contracted initial remaining CSR with a lower excess carrier profile from the fast V_{CE}-I_C transient, which leads to a higher V_{CE} sharing and further enlarges the V_{CE} divergence.

5) An IGBT with a higher N buffer doping profile:

a) In the on-state, reduced hole diffusion from the P emitter through the N buffer of a higher doping profile causes a lower excess carrier profile. However, this reduction in the on-state excess carrier profile is often very limited as normally the N buffer is designed to be under high-level injection in typical use.

b) In the fast V_{CE}-I_C transient, the lower excess carrier profile causes a faster depletion progress, which leads to a higher V_{CE} sharing.

c) In the tail time, the faster depletion progress results in a contracted initial remaining CSR with a lower excess carrier profile from the fast V_{CE}-I_C transient, which leads to a higher V_{CE} sharing assisted by enhanced carrier recombination in the N buffer of a higher doping profile and further enlarges the V_{CE} divergence.

6) An IGBT with longer carrier lifetimes:

a) In the on-state, the longer carrier lifetimes result in an enhanced ambipolar diffusion length, which leads to a higher excess carrier profile.

b) In the fast V_{CE}-I_C transient, the higher excess carrier profile results in a slower depletion progress, which leads to a lower V_{CE} sharing.

c) In the tail time, the slower depletion progress results in an extended initial remaining CSR with a higher excess carrier profile from the fast V_{CE}-I_C transient, which leads to a lower V_{CE} sharing and further enlarges the V_{CE} divergence.

7) An IGBT with a higher temperature:

A difference in IGBT temperature gives rise to a variety of differences in IGBT characteristics that have mixed effects on the turn-off V_{CE} sharing. The discussions regarding a temperature difference are limited to the normal operating temperatures of high voltage Si IGBTs. Since high voltage Si IGBTs have semiconductor thicknesses that far exceed micron-scale, e.g. about 170-190 µm for 1700 V devices, the discussions here regarding temperature differences only consider lattice temperature differences.

a) In the on-state, electron and hole diffusion lengths increase with temperature in the semiconductor regions where the doping concentration is below 1.5×10^{18} cm^{-3}, despite decreases in carrier mobilities [28], [29], [187]. Since the peak doping concentration in the N base of a modern Si FS IGBT is below 1.5×10^{18} cm^{-3}, here the IGBT with a higher temperature has a higher excess carrier profile in the N base.

b) In the initial gate discharging period, the gate plateau voltage for the same $I_{C,sat}$ decreases at a higher temperature. In uncontrolled hard-switching, normally IGBT gate drives use fixed on-state and off-state gate driving voltages. Therefore, during the turn-off gate plateau period as the gate plateau voltage decreases, the discharging voltage across the gate resistance decreases, and the gate discharging current decreases. Despite the decrease in the inversion layer capacitance [188], the initial gate discharging period increases [82]. Here, a longer initial turn-off delay tends to cause a lower V_{CE} sharing.

In the fast V_{CE}-I_C transient, depending on the temperature range and the V_{DC}, the effects of a higher temperature on the turn-off V_{CE} sharing may not be consistent. As demonstrated by the experiments shown in the Fig. 13 of [82], the 50 A and 300 V group from 25 °C to 50 °C shows an increase in the dV_{CE}/dt rate as the temperature increases, whereas decreases in the dV_{CE}/dt rate are observed elsewhere at 50 A.

Carrier mobilities and saturation drift velocities decrease with temperature [32], which results in increased carrier transport under the same I_C in the remaining CSR. This leads to a higher hole concentration and a higher electric field as a result in the depletion region. Under certain conditions, e.g. from 25 °C to 50 °C at 50 A and 300 V in the Fig. 13 of [82], these changes can prevail over the opposite effects of the higher excess carrier profile of the CSR and result in a higher dV_{CE}/dt rate in the fast V_{CE}-I_C transient. However, more often the dV_{CE}/dt rate is reduced with the temperature.

It is possible that the longer initial turn-off delay causes a lower V_{CE} at first, but under certain conditions a higher dV_{CE}/dt rate in the fast V_{CE}-I_C transient can compensate for the initial lower V_{CE} and lead to a higher V_{CE} during the fast V_{CE}-I_C transient. After the total V_{CE} exceeds the V_{DC}, as the I_C decreases the mechanism that results in the higher dV_{CE}/dt rate weakens and the dV_{CE}/dt rate decreases, which may reduce the V_{CE} sharing.

More often, at a higher temperature, the slower depletion progress due to the higher excess carrier profile of the CSR prevails over the increased electric field in the depletion region and results in a lower dV_{CE}/dt rate [82] and lower V_{CE} sharing.

Overall, the V_{CE} divergence in the fast V_{CE}-I_C transient due to a temperature difference depends on the temperature range and the other operating conditions of the IGBTs and needs to be investigated on a case-by-case basis.

c) In the tail time, at a higher temperature, more often the slower depletion progress prevails and results in an extended remaining CSR with a higher carrier profile from the fast V_{CE}-I_C transient, which leads to a lower V_{CE} sharing and further enlarges the V_{CE} divergence.

Under certain conditions as discussed earlier, at a higher temperature the dV_{CE}/dt rate can be higher in the fast V_{CE}-I_C transient, but the excess carrier profile in the remaining CSR still remains higher. Because of the initial turn-off delay at a higher temperature that causes a lower V_{CE} sharing at first, it is likely that despite the following higher dV_{CE}/dt rate, the depletion process in the N base is inadequate to offset the higher carrier profile in the CSR and result in a larger depletion region. Hence, it is likely that as the remaining CSR is larger with a higher excess carrier profile, the V_{CE} sharing in the following tail time is still lower.

Overall, the V_{CE} sharing in the tail time due to a temperature difference also depends on the temperature range and the other operating conditions of the IGBTs and needs to be examined on a case-by-case basis.

Multiple V_{CE} diverging factors may coexist under practical conditions, and the turn-off V_{CE} divergence will result from the mixed effects of the involved diverging factors. Between IGBTs in direct series connection, the turn-off V_{CE} divergence is related to the differences in the carrier transport under the same I_C in the CSR during the fast V_{CE}-I_C transient and the undepleted part of the N base during the following tail time as discussed in the basic V_{CE} diverging scenarios.

3.3.5 The Influence of the Anti-Parallel FWDs on the Turn-Off V_{CE} Sharing

Anti-parallel FWDs are usually required for modern FS IGBTs, where one FWD is in anti-parallel to each IGBT. The effects of the anti-parallel FWDs on the turn-off V_{CE} sharing of series-connected IGBTs needs to be considered in the fast V_{CE}-I_C transient and the tail time following the previous discussions of the turn-off V_{CE} diverging mechanisms.

3.3.5.1 The Influence of the Anti-Parallel FWDs in the Fast V_{CE}-I_C Transient

The anti-parallel FWDs in an IGBT module are reverse-biased in both a typical IGBT on-state and the following turn-off here. Therefore, during typical IGBT turn-off, such an anti-parallel FWD does not possess high-level excess carriers in its N-drift region. The high-level excess carrier profile in the IGBT N base in a typical on-state usually exceeds the N-drift doping profile in concentration by an average of 2-3 orders of magnitude. Hence, in the fast V_{CE}-I_C transient of the IGBT turn-off, the internal anti-parallel FWDs function primarily as small variable capacitances, one in parallel to each IGBT.

In the IGBT turn-off as the IGBT V_{CE} increases rapidly in the fast V_{CE}-I_C transient, part of the load current of the IGBT module flows through the anti-parallel FWD as a charging current so that its reverse-blocking voltage ($-V_{AK}$) can increase with the IGBT V_{CE}. This FWD reverse charging current, due to the high $\mathrm{d}V_{CE}/\mathrm{d}t$ rate, far exceeds the generation current in the depletion region of the FWD. Therefore, the difference in the reverse charging of the FWD output capacitance is the predominant mechanism to consider regarding the influence of the anti-parallel FWDs in the fast V_{CE}-I_C transient.

In the fast V_{CE}-I_C transient, the high-level excess carrier concentration in the CSR in the IGBT N-drift region far exceeds the doping concentration of the N-drift region, and the depletion process in the IGBT N-drift region is related to the ambipolar transport of those high-level excess carriers which shrinks the CSR. Hence, the FWD reverse charging current is much smaller compared with the I_C through the IGBT in the fast V_{CE}-I_C transient. With the high-level excess carriers in the IGBT, in the fast V_{CE}-I_C transient the output capacitance of the IGBT far exceeds that of the anti-parallel FWD.

In the fast V_{CE}-I_C transient, the output capacitance of the anti-parallel FWD follows the basic principle of $C = \varepsilon A/d$, where ε is the permittivity of the FWD semiconductor material, A is the effective chip area of the FWD, and d is the depletion region thickness in 2D along the Anode-Cathode (AK) direction of the FWD. Regarding the IGBTs of the same model in series, it is reasonable to assume that the A and the ε here remain unchanged between the anti-parallel FWDs. Also, for Si PiN anti-parallel FWDs that have N-drift regions with the $N_D \leq 1\mathrm{e}16/\mathrm{cm}^3$, the ε of the FWD N-drift region regarding the output capacitance can be considered the same [189]. Therefore, the output capacitances of the anti-parallel FWDs are assumed to have closely matched basic characteristics.

The output capacitance of an anti-parallel FWD decreases as its reverse-blocking voltage ($-V_{AK}$) increases, which is related to the expansion of the depletion region. Therefore, the effects of the anti-parallel FWDs on the IGBT turn-off V_{CE} sharing are not consistent compared with those of fixed snubber capacitors in parallel to the IGBTs.

Summarising from sections 3.3.2 and 3.3.4, in the fast V_{CE}-I_C transient there are two basic V_{CE} diverging scenarios: (1) a delay in the fast V_{CE} rising due to a delay in the MOS channel cut-off, and (2) a difference in the $\mathrm{d}V_{CE}/\mathrm{d}t$ rate due to a difference in the excess carrier profile in the N base of the IGBT. In the case of a delay in the fast V_{CE} rising, during the delay period the output capacitance of the anti-parallel FWD results in a reduced $\mathrm{d}V_{CE}/\mathrm{d}t$ rate of the leading IGBT and the V_{CE} divergence accumulated. In the fast V_{CE}-I_C transient after the initial delay period, the anti-parallel FWD in the IGBT-FWD pair with a higher V_{CE} exhibits a lower output capacitance which requires a lower reverse charging current at a certain $\mathrm{d}V/\mathrm{d}t$ rate. However, in order to mitigate the V_{CE} divergence in the turn-off, the ambipolar carrier transport in the CSR and the related I_C of the IGBT with a higher V_{CE} needs to be reduced, so that the $\mathrm{d}V_{CE}/\mathrm{d}t$ rate can be reduced. As the total current is the same for the IGBT-FWD pairs in direct series, for the IGBT-FWD pair with a higher V_{CE}, a reduction in the IGBT I_C requires an increase in the reverse charging current of the anti-parallel FWD, which cannot be achieved here as the output capacitance of the anti-parallel FWD decreases with the IGBT V_{CE}. Consequently, in the

fast V_{CE}-I_C transient the anti-parallel FWDs cannot mitigate the V_{CE} divergence. This conclusion is also applicable to the use of SiC Schottky Barrier Diodes (SBDs) as the anti-parallel FWDs.

3.3.5.2 The Influence of Anti-Parallel FWDs during the IGBT Tail Time

In the IGBT tail time, the IGBT I_C gradually reaches its leakage level, which is comparable with the reverse leakage current of the Si anti-parallel FWD. Since the V_{DC} can be considered quasi-static in the IGBT tail time, the difference in the FWD leakage current becomes a key factor to consider regarding the influence of the anti-parallel FWDs during the IGBT tail time.

Summarising from sections 3.3.2 and 3.3.4, in the IGBT tail time there are two basic V_{CE} diverging scenarios: initially from the fast V_{CE}-I_C transient, (1) an extended remaining CSR, and (2) a remaining CSR of a higher excess carrier profile, which both result in an enhanced hole diffusion current in the undepleted part of the N base towards the depletion region.

With the anti-parallel FWDs, the difference in the hole diffusion current towards the depletion region in the undepleted part of the N base between the IGBTs is also absorbed by the anti-parallel FWDs. The reverse leakage current of the anti-parallel FWD increases with the reverse-blocking voltage ($-V_{AK}$) due to the increase in the carrier generation in the expanded depletion region. As the initial IGBT tail current is much higher than the later IGBT leakage current, the IGBT with a relatively inadequate hole diffusion current towards the depletion region in the undepleted part of the N base is still subject to increases in its depletion region and V_{CE}, which reduces the differences in the output current characteristics between the IGBTs. The increasing V_{CE} gives rise to a reverse charging current through the anti-parallel FWD in this IGBT-FWD pair, which leads to the expansion of the FWD depletion region and an increase in the generation current in it. Hence, for this IGBT the I_C is lower, and the expansion of the IGBT depletion region and the increase in the V_{CE} become smaller.

Meanwhile, the IGBT with a relatively enhanced hole diffusion current towards the depletion region in the undepleted part of the N base experiences shrinking of its depletion region, which results in decreases in its V_{CE} and the generation current in its depletion region. The anti-parallel FWD to this IGBT experiences a reverse discharging current, which leads to shrinking of its depletion region and a decrease in the generation current in it. These changes in this FWD are the opposite of those changes in the other FWD that has an increase in its reverse-blocking voltage. Those changes in the two FWDs assist in absorbing the differences in the output current characteristics between the IGBTs that cause the turn-off V_{CE} divergence. Hence, the anti-parallel FWDs reduce the turn-off V_{CE} divergence in the tail time.

Theoretically the conclusion here is also applicable to the use of SiC SBDs as anti-parallel FWDs. However, due to the WBG features of SiC SBDs, the leakage current of a SiC SBD is considerably lower compared with that of a Si diode of the same ratings. Hence, the influence of SiC SBDs as anti-parallel FWDs on the turn-off V_{CE} sharing is very limited.

3.3.5.3 The Scale of the Influence of Anti-Parallel FWDs

In the fast V_{CE}-I_C transient, the charging of the output capacitances of the IGBT and the anti-parallel FWD is an important mechanism to consider. Due to the significant difference in the

output capacitance between the IGBT and the anti-parallel FWD, the difference in the FWD output capacitance due to its dependence on the reverse-blocking voltage can only has very limited negative influence on the turn-off V_{CE} sharing in the fast V_{CE}-I_C transient.

However, in the tail time the IGBT I_C approaches its leakage level which is comparable with the leakage current of the anti-parallel FWD, and the changes in the leakage currents become another important mechanism to consider. The anti-parallel FWDs assist in absorbing the difference in the output current characteristics between the IGBTs. Therefore, the influence of the anti-parallel FWDs on the IGBT turn-off V_{CE} sharing becomes positive and important in the IGBT tail time.

Here, the influence of the anti-parallel FWDs on the turn-off V_{CE} sharing is negative but very limited in the fast V_{CE}-I_C transient, whereas it is positive and important in the IGBT tail time. This leads to an overall positive influence of the anti-parallel FWDs on the IGBT turn-off V_{CE} sharing. The conclusion here is also applicable to the use of SiC SBDs as anti-parallel FWDs for the IGBTs, although the influence in the IGBT tail time is very limited. Hence, also because the anti-parallel FWDs are not an initiating factor that causes the V_{CE} divergence, the anti-parallel FWDs for the IGBTs in series will not be discussed further.

3.3.6 Long-Term Stability of the V_{CE} Sharing in the IGBT Off-State

The long-term stability of the turn-off V_{CE} sharing in the IGBT off-state, whether the V_{CE} sharing is self-stabilising, is important in the turn-off of IGBTs in series. In the IGBT off-state, due to the PNP BJT structure in the IGBT, the IGBT intrinsic leakage current is affected by the carrier generation rate in the depletion region, the position of the depletion edge in the N base, and the doping profiles of the P emitter, the N buffer, and the N-drift region. For an IGBT in a static off-state, a larger depletion region related to a higher V_{CE} gives rise to a higher generation current in the depletion region and a higher common-emitter current gain, which results in a higher intrinsic leakage current.

In a two-in-series situation, to match the same I_C in direct series connection, for the IGBT with a lower intrinsic leakage current, additional carriers are required to compensate for the difference in the intrinsic leakage current and can only be supplied using electrons from the undepleted part of the N base via depletion. Consequently, the depletion region in this IGBT expands, which increases the V_{CE} and the intrinsic leakage current.

Meanwhile, in the other IGBT with a higher intrinsic leakage current, the opposite process occurs. Part of the electrons generated in the depletion region recover the depletion region from the depletion edge in the N base. Consequently, the depletion region in this IGBT shrinks, which reduces the V_{CE} and the intrinsic leakage current. Thus, the intrinsic leakage currents of the IGBTs gradually converge and will eventually match where a stable V_{CE} sharing is reached if the IGBT off-state is sufficiently long. Hence, the long-term V_{CE} sharing in the IGBT off-state is self-stabilising.

However, depending on the V_{CE} diverging factors, matching intrinsic leakage currents of the IGBTs do not necessarily lead to evenly distributed V_{CE} sharing or reduced V_{CE} divergence.

The self-stabilising of the V_{CE} sharing in the IGBT off-state is slow compared with the V_{CE} divergence in the IGBT turn-off as the intrinsic leakage current and the difference in it are low.

3.3.7 Temperature Differences Arising from the Turn-Off Voltage Divergence

Besides differences in thermal boundary conditions which can directly cause IGBT temperature differences, other IGBT parameter variations and gate driving errors can also result in differences in turn-off losses which lead to IGBT temperature differences. Here, the discussion refers to the feedback effects of the temperature differences on the V_{CE} divergence in the turn-off arising from IGBT parameter variations and gate driving errors.

As discussed in section 3.3.4, the V_{CE} diverging effects of a V_{CE} diverging factor in general are consistent in the fast V_{CE}-I_C transient and the following tail time. The turn-off losses are distributed mainly in the fast V_{CE}-I_C transient, where the temperature differences develop between the IGBTs. Hence, a V_{CE} diverging factor that causes higher voltage sharing of an IGBT also causes higher losses in the fast V_{CE}-I_C transient and a higher temperature rise of this IGBT.

In the fast V_{CE}-I_C transient, as discussed in section 3.3.4, in general a higher temperature has the effect of reducing the V_{CE} sharing, except for certain limited operating conditions. Hence, in general the higher temperature of an IGBT caused by higher V_{CE} sharing has the effect of mitigating the V_{CE} divergence.

In the tail time, the hole diffusion current in the undepleted part of the N base towards the depletion region is affected by carrier recombination. A carrier lifetime model with temperature dependence of explicit expressions is given by [29]:

$$\tau^{-1} = (\tau_0^{-1} + C_{SRH}N_t)\left(\frac{300}{T}\right)^{\gamma} + (C_{Aug}n^2)\left(\frac{T}{300}\right)^{\delta} \qquad \text{Equation 3.1}$$

where T is the temperature, N_t is the total doping concentration, and n is the carrier concentration of either electrons or holes, with separate parameters for electrons and holes:

	τ_0 (10^{-3}s)	C_{SRH} (10^{-13}cm^{3}s^{-1})	C_{Aug} (10^{-31}cm^{6}s^{-1})	γ	δ
Electrons	2.50	3.00	1.83	1.77	1.18
Holes	2.50	11.76	2.78	0.57	0.72

For the IGBT N base in the tail time, in Equation 3.1 the first term representing SRH recombination is predominant, which leads to a higher carrier lifetime at a higher temperature. Therefore, at a higher temperature the recombination in the N base is reduced, which enhances the hole diffusion current in the undepleted part of the N base towards the depletion region. Following the discussion in section 3.3.3, such an enhanced hole diffusion current has an effect of reducing the V_{CE} sharing. Hence, a higher temperature of an IGBT caused by higher V_{CE} sharing has an effect of mitigating the V_{CE} divergence. Therefore, the qualitative V_{CE} diverging effect of a V_{CE} diverging factor remains consistent under isothermal conditions.

Regarding the long-term off-state V_{CE} sharing, the discussions in section 3.3.6 is applicable to IGBT temperature differences, under which the long-term off-state V_{CE} sharing is self-stabilising, although evenly distributed V_{CE} sharing or reduced V_{CE} divergence may not be achieved.

3.4 FEM Simulation Setup for the Turn-Off V_{CE} Divergence

To test one V_{CE} diverging factor at a time in a controlled and cost-efficient manner, Finite Element Method (FEM) simulation in Silvaco ATLAS MixedMode is used to study the turn-off V_{CE} divergence of IGBTs in series connection under inductive load conditions.

The simulation uses a basic trench gate Si FS IGBT model of 1700 V class and 1 cm^2 active chip area as the base IGBT model. This IGBT model uses a narrow cell pitch and a high static punch-through voltage V_{PT} of approx. 1200 V, where the depletion edge in the N base just reaches the N buffer in a static forward-blocking off-state. This IGBT model is a 2D vertical half-cell model without edge terminations.

In the simulations of the turn-off, two IGBTs are connected in direct series as the main switch in a basic buck converter circuit, which enables direct control of the load conditions for the IGBT turn-off. In the test circuit, the IGBT with a higher electric potential is referred to as the Higher Side IGBT (IGBT-HS), and the other IGBT with a lower electric potential is referred to as the Lower Side IGBT (IGBT-LS). As discussed in section 3.3.5, anti-parallel FWDs for the IGBTs are not included in the simulation unless specified otherwise. The simulation includes lattice heating and heat flow, which in terms of thermal effects is adequate for the Si high voltage IGBTs far exceeding micron-scale in cell dimensions.

3.4.1 Estimation of IGBT Active Chip Area

The IGBT model and the test circuit in the simulation are configured to achieve reasonably close approximations to the actual IGBT module and the Current Commutation Loop (CCL) in the IGBT turn-off experiments to be presented later. The IGBT module in the experiments is a Fuji Electric V series 2MBI650VXA-170E-50 2-in-1 packaged module in the low switching loss line of 1700 V and 650 A for each IGBT, featuring trench gate and field-stop designs, first released in 2011 [190], [191].

The base active chip area of the IGBT model in the simulation is set to 1 cm^2 to provide a direct conversion of the IGBT I_C into the 1 cm^2 IGBT collector current density J_C, for which some of the simulation circuit parameters are scaled. The scaling depends on the active chip area of the Fuji Electric IGBT, which can be obtained using its rated J_C. However, as only the J_C-V_{CE} curves of the 1200 V IGBTs are provided in the application note of the Fuji Electric V series IGBTs [191], the J_C rating of the 1700 V IGBTs in the experiments has to be estimated from a few commercial 1700 V IGBT bare dies with necessary details provided that feature design concepts similar to those of the Fuji Electric IGBTs, Table 3.1.

The Infineon IGBT bare dies used here are the TRENCHSTOP IGBT3 series, featuring trench gate and field stop designs. The ABB IGBT bare dies used here are the SPT^{++} series, featuring a soft punch through design, an alternative to the field stop concept, and an enhanced planar gate design, an alternative to the trench gate concept. Since the Fuji Electric IGBTs are in the low switching loss product line, similar product lines from Infineon and ABB are used. As the base IGBT model in the simulation does not include edge terminations, the frontside metal areas of the IGBT bare dies are used to estimate the J_C, and the bare dies with large active

chip areas are selected to reduce errors in the estimation caused by edge terminations. The technical details of the IGBT bare dies used are presented in Table 3.1 from their respective datasheets, and the rated J_C values are estimated.

Table 3.1: Estimation of the rated J_C of a few 1700 V IGBT bare dies

IGBT bare die: manufacturer, technology, model	Semiconductor thickness (μm)	Rated I_C with V_{CE}, V_{GE} = 15 V	Frontside metal area (mm^2)	Estimated Rated J_C (A/cm^2)
Infineon, TRENCHSTOP IGBT3, SIGC186T170R3E	190	I_C = 150 A, V_{CE} = 2 V at 25 °C	11.407 × 11.407 = 130.1196	115.2785
Infineon, TRENCHSTOP IGBT3, SIGC158T170R3E	190	I_C = 125 A, V_{CE} = 2 V at 25 °C, 2.4 V at 125 °C	10.354 × 10.354 = 107.2053	116.5987
Infineon, TRENCHSTOP IGBT3, SIGC128T170R3E	190	I_C = 100 A, V_{CE} = 2 V at 25 °C	9.113 × 9.113 = 83.0468	120.4141
ABB, SPT^{++}, 5SMY 12P1730	190	I_C = 225 A, V_{CE} = 2.25 V at 25 °C, 2.55 V at 125 °C, 2.75 V at 175 °C	14.84 × 13.91 = 206.4244	108.9987
ABB, SPT^{++}, 5SMY 12M1731	190	I_C = 160 A, V_{CE} = 2.25 V at 25 °C, 2.55 V at 125 °C, 2.75 V at 175 °C	11.90 × 11.93 = 141.9670	112.7022
ABB, SPT^{++}, 5SMY 12M1730	190	I_C = 150 A, V_{CE} = 2.25 V at 25 °C, 2.55 V at 125 °C, 2.75 V at 175 °C	11.52 × 11.53 = 132.8256	112.9300

As shown in Table 3.1, the estimated rated J_C of the Infineon IGBT bare dies is between 115-121 A/cm^2, and the estimated rated J_C of the ABB IGBT bare dies is between 108-113 A/cm^2. It is noteworthy that the Infineon samples were released a few years ahead of the Fuji Electric IGBTs, and the on-state performance of the enhanced planar gate in the ABB samples may not be as good as that of a typical trench gate. Hence, it is reasonable to presume a rated J_C of 130 A/cm^2 for the Fuji Electric IGBTs, which is the mid-range of the estimated rated J_C of the Infineon samples, 118 A/cm^2, plus a 10% increase that is often gained in a few years of development in that era. Therefore, the rated I_C of 650 A of the Fuji Electric IGBTs is estimated to have an active chip area of 5 cm^2.

3.4.2 Simulation Circuit Parameters and Scaling

The simulation circuit is shown in Figure 3.4. As the IGBTs in the experiments and the simulations are of 1700 V class, the default value of the input DC voltage source V_{in} is set to 1700 V to provide an average off-state V_{CE} of approx. 850 V, 50% of the 1700 V V_{CE} rating of the two

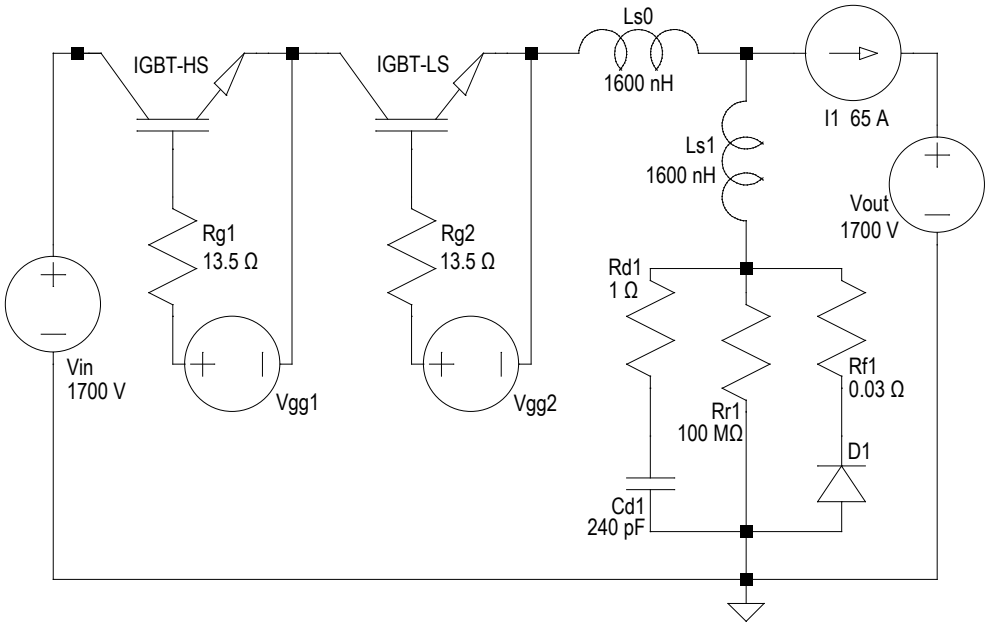


Figure 3.4: Schematic diagram of the basic test circuit in the simulations.

IGBTs in series, which is the mid-range of the typical use of IGBTs in practice. In the simulation circuit, the main inductor in the bulk converter circuit is replaced by the DC current source I_1 to provide a consistent load current for the IGBTs in the on-state and the turn-off. The default area of the IGBT model is 1 cm^2. Hence, the default value of the I_1 is set to 65 A, 50% of the 130 A I_C rating of the IGBT chips, which is the mid-range of the typical use of IGBTs in practice. The output stage of the bulk converter circuit is connected to a second DC voltage source V_{out} with its default value matched to that of the V_{in}. The DC current source I_1 provides a degree of freedom in voltage that enables the use of such a circuit configuration to provide consistent and controlled load conditions. An initial IGBT on-state of 9.9 ms is used simultaneously for all the IGBTs to obtain a quasi-static IGBT on-state for the following turn-off event.

The FWD D_1 in the IGBT CCL uses a built-in idealised diode model in Silvaco ATLAS to improve the numerical convergence and the speed of the simulation. A power diode equivalent circuit is built around the D_1 to approximate the average output capacitance in the expected blocking voltage range of the FWD in the IGBT CCL in the IGBT turn-off. The default parameters of the FWD circuit for two IGBTs in series are shown in Figure 3.4.

At the IGBT turn-off, the two open-loop IGBT gate drives, V_{gg1} and V_{gg2}, switch from their on-state driving voltage to off-state driving voltage linearly in 20 ns. The default driving voltages of the V_{gg1} and the V_{gg2} are both 15 V for an on-state and -15 V for an off-state, the same as those of typical IGBT gate drives. The default values of the gate resistances, R_{g1} and R_{g2}, are 13.5 Ω for both IGBT turn-on and turn-off and for the IGBT active chip area of 1 cm^2, which is calibrated to fit the initial turn-off delay observed in the experiments. When scaled to the estimated 5 cm^2 IGBT active chip area in the experiments, the scaled R_g becomes 2.7 Ω, which is close to the total gate resistance of 2.75 Ω in the experiments that consists of an internal gate resistance of 1.75 Ω and an external gate resistance of 1 Ω.

The stray inductance in the IGBT CCL is included in the simulation circuit in the form of two lumped stray inductances of the same default value in series to the IGBT branch and the FWD branch, L_{S0} and L_{S1} in Figure 3.4, respectively. The stray inductance in the IGBT CCL in the experiments is estimated at approx. 640 nH for two IGBTs in series with the estimated 5 cm^2 active chip area. In the simulations, this value is scaled to a total of 3200 nH, and the default values of the L_{S0} and the L_{S1} are set to 1600 nH as shown in Figure 3.4 for the two IGBTs of the 1 cm^2 active chip area in series.

The default initial temperature values of the test circuit, the IGBT models and the IGBT thermal contacts are set to 300 K. The thermal aspect of the simulation will be introduced later.

3.4.3 FS IGBT Model in the Simulations

The IGBT model in the simulations is a basic 2D vertical half-cell model without edge terminations, featuring trench gate and FS designs, Figure 3.5, noting the 1.5 µm offset on the x-axis. This model is a general-purpose model for studying the turn-off V_{CE} divergence rather than a reverse engineering model. The state-of-the-art IGBTs feature innovative designs, e.g. 3D structures, superjunctions, carrier storage layers (not the CSR), and nanoscale structures [59], [192].

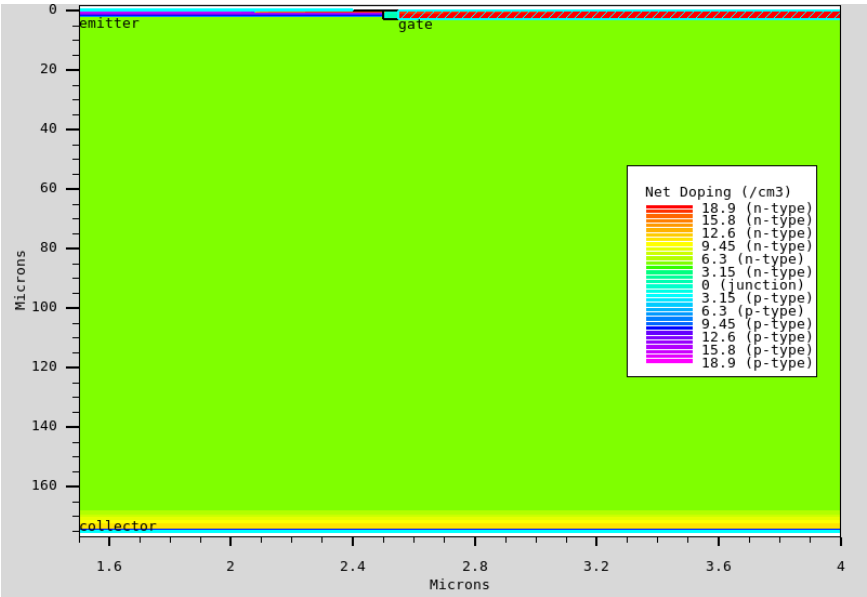


Figure 3.5: The base IGBT model in Silvaco ATLAS.

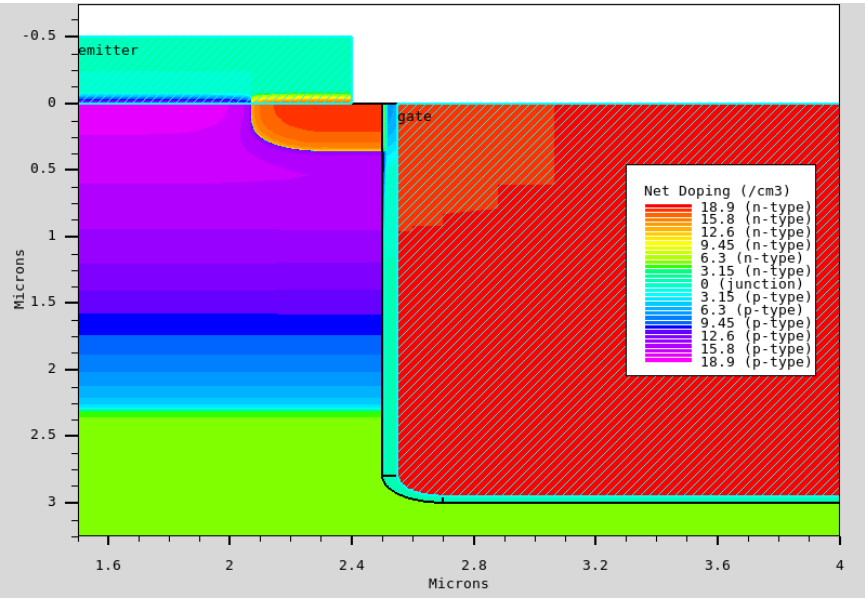
Nevertheless, the basic carrier transport mechanisms of IGBTs are the same, and to better focus on these basics, the doping profiles of the IGBT model use a conventional configuration.

As the Fuji Electric IGBTs in the experiments were released a few years later than the bare die samples in Table 3.1, to reflect the development trend of that era, the semiconductor thickness of the base IGBT model is reduced to 175 µm, which also provides a close approximation to the turn-off characteristics observed in the experiments. The IGBT model is calibrated to the ratings of 1700 V forward-blocking V_{CE} with a static punch-through voltage V_{PT} of approx. 1200 V and 130 A/cm^2 on-state current density. In general, FS IGBTs do not require local carrier lifetime control [193], therefore, local carrier lifetime control is not used in this FS IGBT model.

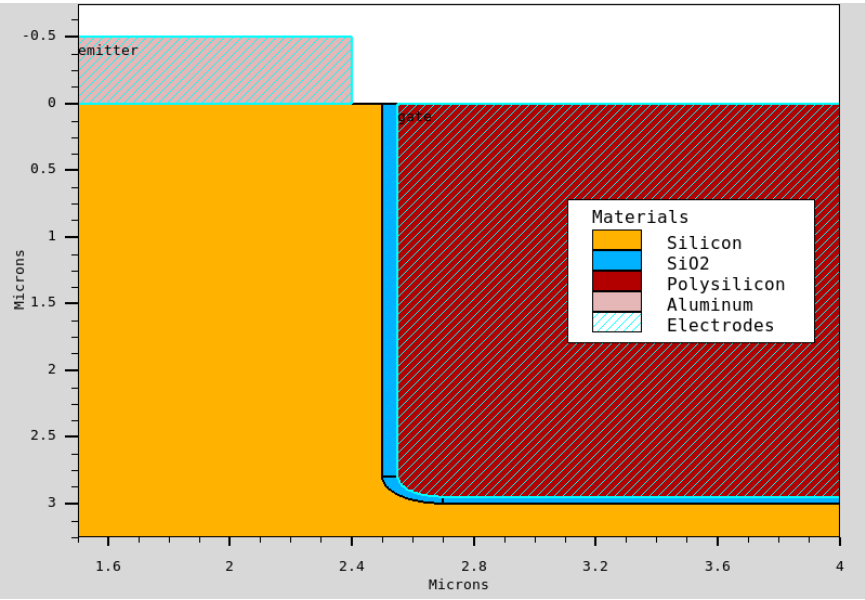
Of the complete IGBT model shown in Figure 3.5, the frontside is shown in Figure 3.6, and the backside is shown in Figure 3.7, with net doping and materials indicated. The P type doping uses boron, and the N-type doping uses phosphorus. The half-cell width as shown in Figure 3.5 is 2.5 µm, from 1.5 µm to 4 µm along the lateral x-axis, and the semiconductor thickness is 175 µm, from 0 µm to 175 µm along the vertical y-axis.

The frontside of the IGBT model is shown in Figure 3.6 with the “gate” and “emitter” electrodes indicated, noting the change of scale on the axes. The doping and material profiles are indicated in Figure 3.6 (a) and (b), respectively. The thickness of the oxide layer of SiO_2 is 500 Å, and the full MOS channel length in the P base is 1.95 µm. The backside of the IGBT model is shown in Figure 3.7 with the “collector” electrode indicated. The doping and material profiles are indicated in Figure 3.7 (a) and (b), respectively. The thicknesses of the P emitter and the FS N buffer are 1 µm and 5 µm, respectively.

The key parameters of the base IGBT model are summarised in Table 3.2. The doping profile is explicitly defined rather than generated by simulations or measurements of IGBT fabrication processes. The doping profiles in the semiconductor region are based on surface diffusion with Gaussian roll off distribution on both x-axis and y-axis where applicable.



(a)

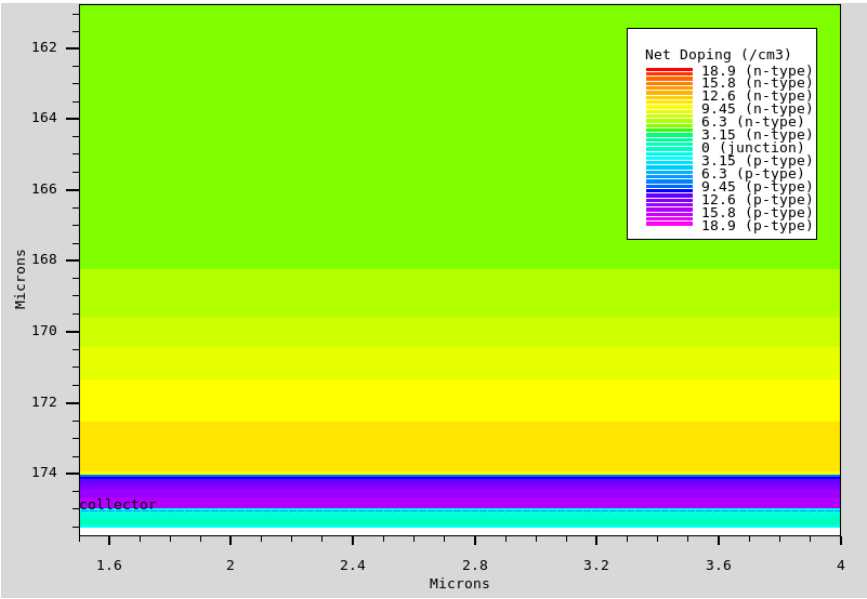


(b)

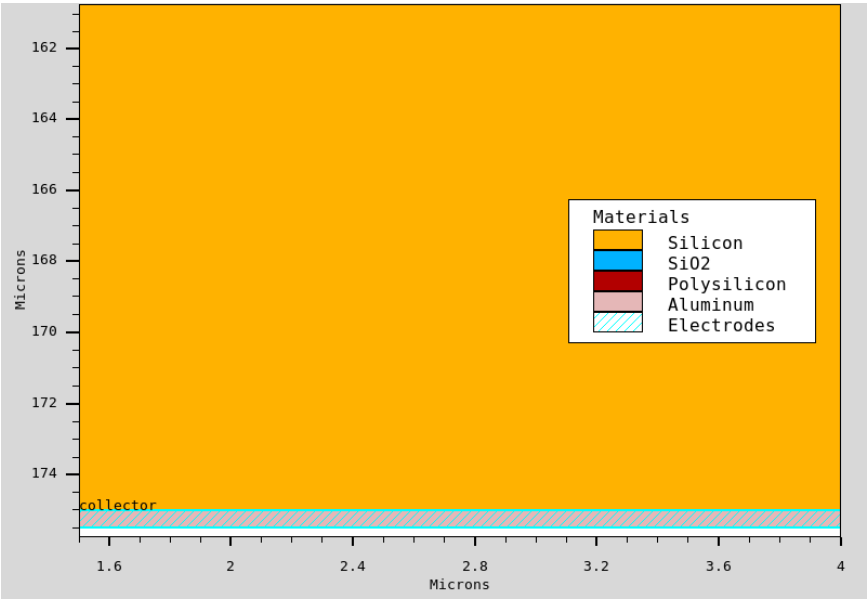
Figure 3.6: The front side of the IGBT model: (a) the doping profile, and (b) the materials.

Table 3.2: Key parameters of the base IGBT model.

Region	Dimension (μm)		Surface doping conc. (cm^{-3})
Semiconductor region	Depth (y-axis): 175	Width (x-axis): 2.5	N/A
Trench gate	Depth (y-axis): 3	Width (x-axis): 1.5	N/A
SiO_2 oxide layer	Thickness: 0.05 (500 Å)		N/A
Full MOS channel length	In the P base: 1.95		N/A
N^+ region, frontside	Depth (y-axis): 0.35	Width (x-axis): 0.43	8×10^{18}
Shallow P^+ region, frontside	Depth (y-axis): 0.35	Width (x-axis): 0.57	4×10^{18}
Deep P well, frontside	Depth (y-axis): 2.3	Width (x-axis): 1	2×10^{18}
N^- drift region	Depth (y-axis): 166.7	Width (x-axis): 2.5	5.6×10^{13}
N FS buffer, backside	Depth (y-axis): 6	Width (x-axis): 2.5	1.15×10^{16}
P^+ emitter region, backside	Depth (y-axis): 1	Width (x-axis): 2.5	6×10^{17}
“Emitter” electrode, frontside	Thickness (y-axis): 0.5	Width (x-axis): 0.9	N/A
“Collector” electrode, backside	Thickness (y-axis): 0.5	Width (x-axis): 2.5	N/A



(a)

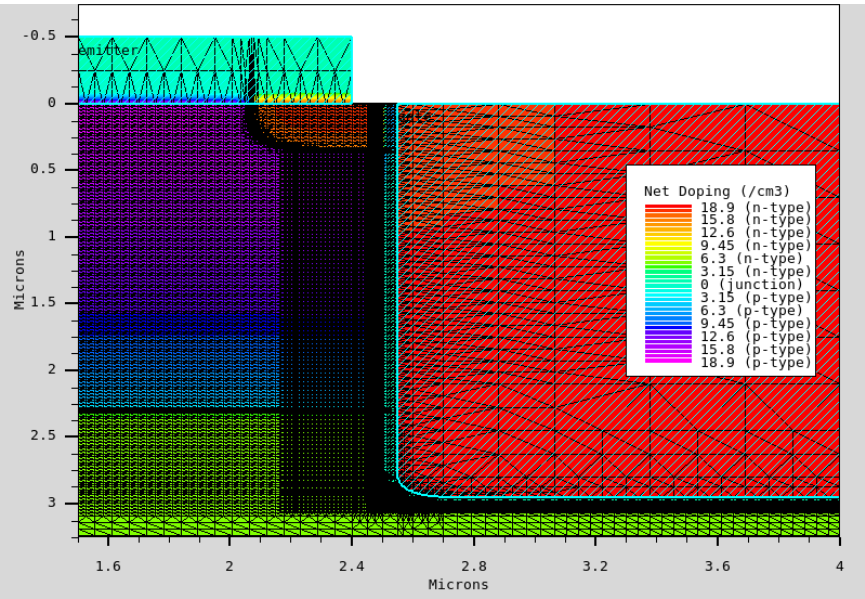


(b)

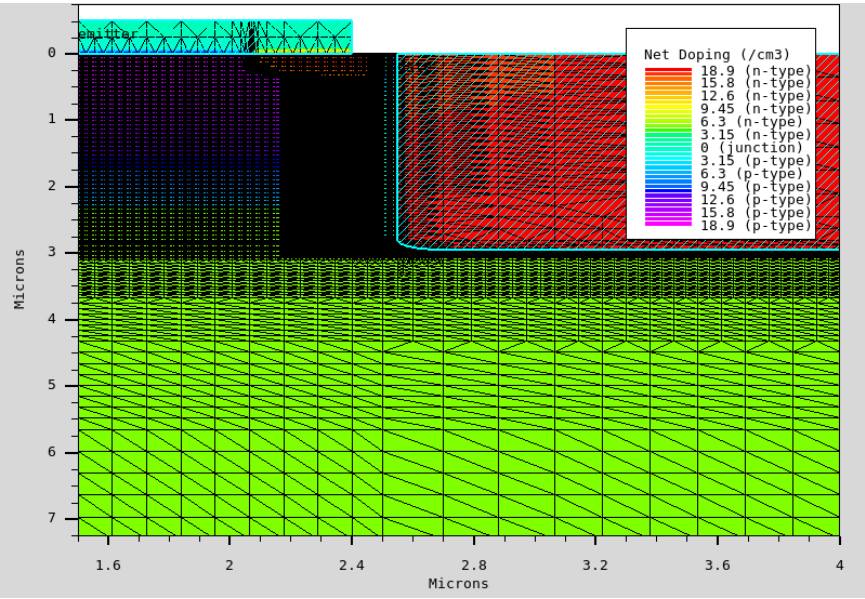
Figure 3.7: The back side of the IGBT model: (a) the doping profile, and (b) the materials.

Figure 3.8 and Figure 3.9 show the mesh grids indicated by triangles at the frontside and the backside of the base IGBT model, respectively, noting the change of scale on the axes. Following the discussions in section 3.3, at IGBT device level the turn-off V_{CE} sharing of series-connected IGBTs has strong dependence on the interaction between the IGBTs caused by their differences in the internal carrier transport. Hence, the mesh grids in the key areas that have strong influences on the simulation accuracy of the related characteristics shall have adequate densities to avoid excessive simulation errors.

Therefore, in the IGBT model here, the grid densities in the following regions are enhanced: (1) the inversion layer and the accumulation layer adjacent to the SiO_2 layer for MOS gate behaviours, including the maximum perpendicular grid spacing for the MOS channel being limited to 0.001 μm, Figure 3.8 (a); (2) the area adjacent to the MOS channel under the N^+ region for current and electric field distributions, Figure 3.8 (a); (3) the lateral semiconductor region beside the trench gate for electric field and carrier distributions, Figure 3.8 (a); (4) the



(a)



(b)

Figure 3.8: Mesh grids at the front side of the IGBT model: (a) the MOS gate region, and (b) the grid density transition towards the deep N-drift region.

semiconductor region across the entire half-cell underneath the trench gate and the P base for current and electric field distributions, Figure 3.8 (b); (5) the N buffer and the P emitter at the backside for carrier and electric field distributions, Figure 3.9.

Regarding the general mesh parameters in the semiconductor region, along the vertical (y-axis) direction, the maximum grid height is limited to 0.4 µm. As dynamic mesh is not supported in Silvaco ATLAS MixedMode, this small mesh spacing limit throughout the N base is required to obtain adequate vertical resolution of the carrier distribution at the moving depletion edge during the turn-off, which affects the simulation accuracy of the V_{CE} sharing. Along the lateral (x-axis) direction, the maximum grid width is limited to 0.2 µm. This is to obtain adequate lateral resolution of the distribution of the current that converges to the trench gate or the P base during the turn-off.

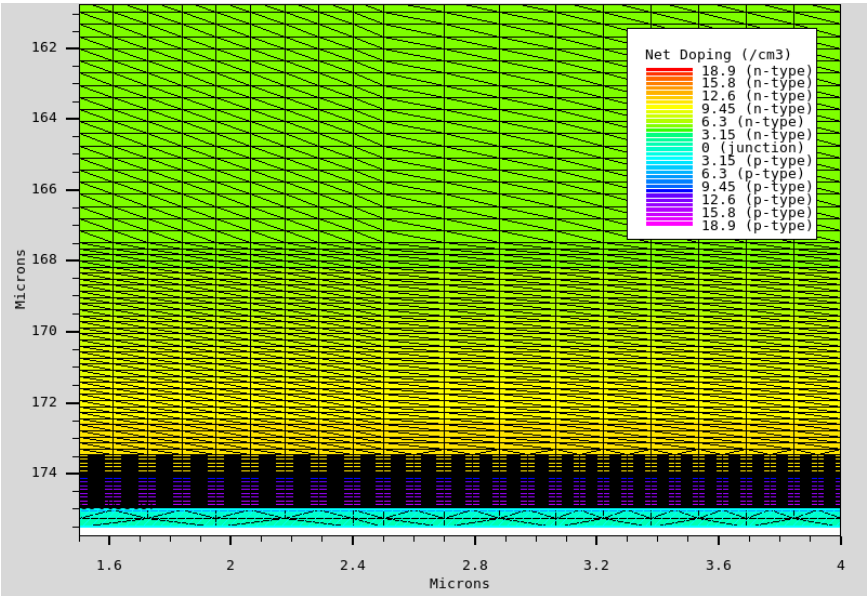


Figure 3.9: Mesh grids at the back side of the IGBT model.

3.4.4 Selection of the Physics Model in Silvaco ATLAS

The selection of the built-in physics models in Silvaco ATLAS for the simulations is based on the semiconductor components in the IGBT model and their operating conditions during the turn-off as discussed in section 3.3. More specifically, the selected built-in physics models and the numerical parameters should be appropriate for the physical characteristics in silicon of: (1) the inversion layer of the MOS channel, (2) the high-level injection and the excess carrier profile of the PNP BJT structure, and (3) the carrier transport and the impact ionisation in the depletion region under a high electric field, including the effects of carrier velocity saturation. The following built-in physics models are set in the simulations:

Mobility Models – The mobility models need to account for the dependence of the carrier mobilities on both parallel and perpendicular electric fields, doping concentration, and temperature. Hence, the built-in Lombardi CVT model and Darwish CVT model are activated by setting the flag `CVT` in the `MODELS` statement and the flag `NEWCVT.N` and `NEWCVT.P` in the `MOBILITY` statement, respectively [39], [194], [195]. The `CVT` model, by default, employs the built-in parallel electric field dependent mobility model, the flag `FLDMOB` in the `MODELS` statement, where the low-field mobility from the `CVT` model is supplied to the `FLDMOB` model to account for carrier velocity saturation effects [39], [195]. The Darwish CVT model is an improved version of the Lombardi CVT model, which incorporates the mobility model by Klaassen [28], [29] for bulk mobility and a new expression for surface roughness [194], [195]. In Silvaco ATLAS, the Darwish CVT model needs to be set concurrently with the Lombardi CVT model to be effective.

Recombination Models – The recombination models need to account for both SRH recombination and Auger recombination. For SRH recombination, the built-in SRH lifetime model with additional doping concentration dependence is activated by setting the flag `CONSRH` in the `MODELS` statement [47]–[49], [195]. A built-in set of parameters for this model suggested by Law [49] is activated by setting the flag `CONSRH.LAW` in the `MODELS` statement. The `CONSRH`

model, by default, employs the built-in standard SRH recombination model, the flag SRH in the MODELS statement [44], [45]. For Auger recombination, the built-in Auger recombination model with temperature and concentration dependent coefficients is activated by setting the flag HNSAUG in the MODELS statement, [56], [196], which, by default, employs the built-in standard Auger recombination model, the flag AUGER in the MODELS statement [51], [195].

Bandgap Narrowing Model – Bandgap narrowing effects start to occur when the doping concentration exceeds 10^{17} cm^{-3} [20], [187], [197], [198]. As part of the doping profiles in the IGBT model exceeds that level, a built-in bandgap narrowing model is activated by setting the flag BGN in the MODELS statement [20], [187], [195].

Impact Ionisation Model – In typical use, the high electric field in an IGBT in the turn-off and the off-state excites impact ionisation, which affects the carrier and the current distributions. Hence, the built-in impact ionisation model by Selberherr is activated by setting the flag SELB in the IMPACT statement [24], [25], [58], [195], [199].

Lattice Heat Flow Models – The simulation of lattice heat flow uses the self-heating simulator GIGA in Silvaco, which implements the thermodynamically rigorous model of lattice heating by Wachutka [195], [200]. This built-in lattice heat flow model is activated by setting the flag LAT.TEMP in the MODELS statement [195]. Regarding the thermal conductivity, the built-in compositionally dependent thermal conductivity model is activated by setting the flag TCON.COMP in the MATERIAL statement [195], [201]. Regarding the heat capacity, the built-in compositionally dependent heat capacity model is activated by setting the flag HC.COMP in the MATERIAL statement, [195], [201]. The thermal boundary is specified as the outside surface of the backside "collector" electrode of the IGBT model in the THERMCONTACT statement, with a default external temperature value of 300 K and a default thermal conductance value of 10 $W/(cm^2 \cdot K)$. This method is compatible with the internal merging of multiple ATLAS devices into one for simulation in ATLAS MixedMode, e.g. the two IGBTs in series.

Contact Characteristics – The "gate" electrode of the IGBT model is N^+ polysilicon. The work function of the "gate" electrode is set to 4.17 eV by setting the flag N.POLYSILICON in the CONTACT statement for the "gate" electrode [195]. The "collector" and the "emitter" electrodes are aluminium on heavily doped silicon which forms ohmic contact. Therefore, the work functions for these two aluminium electrodes are not specified.

Numerical Parameters – The simulations employ the Fermi-Dirac statistics rather than the Boltzmann statistics due to the heavily doped regions in the IGBT model [195]. The quasi-static approximation for transient simulation in the ATLAS solver is disabled for the fast IGBT turn-off. The simulations involve depletion regions at high blocking voltages, in which the low carrier concentrations require a reduction in the minimal concentration to be resolved by the solver to prevent "false" solutions [195], adjusted by the parameter CLIMIT in the METHOD statement. The ATLAS manual recommends an order of magnitude of 1×10^8 cm^{-3} for that minimal concentration for Si diode breakdown simulation [195]. In the simulations here, the CLIMIT is reduced from 1×10^4 to 2×10^{-4}, which reduces that minimal concentration from approx. 4.5×10^{13}

cm^{-3} to approx. 9×10^5 cm^{-3}. However, within a limited arithmetic precision level, e.g. 80 nominal precision bits with 64 significant bits, reducing the `CLIMIT` may cause rounding errors that prevent a resolution to be obtained when a high numerical contrast in an ATLAS device exists, e.g. in the carrier concentration in the turn-off. In the simulations here, the arithmetic precision level is increased from the default 64 bit nominal precision with 53 significant bits to the 80 bits nominal precision with 64 significant bits [195].

3.4.5 Simulation Examples

To validate that the IGBT model here is capable of providing reasonable approximations to an actual IGBT, a simulation result of the IGBT model is compared with the experiment result of the uncontrolled IGBT turn-off shown previously in Figure 3.2. The experiment V_{CE} sharing result is affected by a mixture of gate control errors and parameter variations between the IGBT devices. To obtain the average characteristics of those IGBTs in series, 50% of the total V_{CE} of the two IGBTs in series in the experiment is used as the V_{CE} of a single IGBT for a single-device comparison with the simulation result.

The simulation circuit for this comparison, Figure 3.10, uses the basic circuit shown in Figure 3.4 with a few modifications to account for the parameter scaling for the single-device situation and the anti-parallel FWDs of the IGBT module in the experiment. The FWD circuit D_1 that accounts for another IGBT module of the same model used as the FWDs in the CCL in the experiment is converted into a single-device form. The FWD circuit D_0 is attached in anti-parallel to the IGBT model with the parameters scaled to account for an anti-parallel FWD in the switching IGBT module in the experiment. The stray inductances are halved for a single-

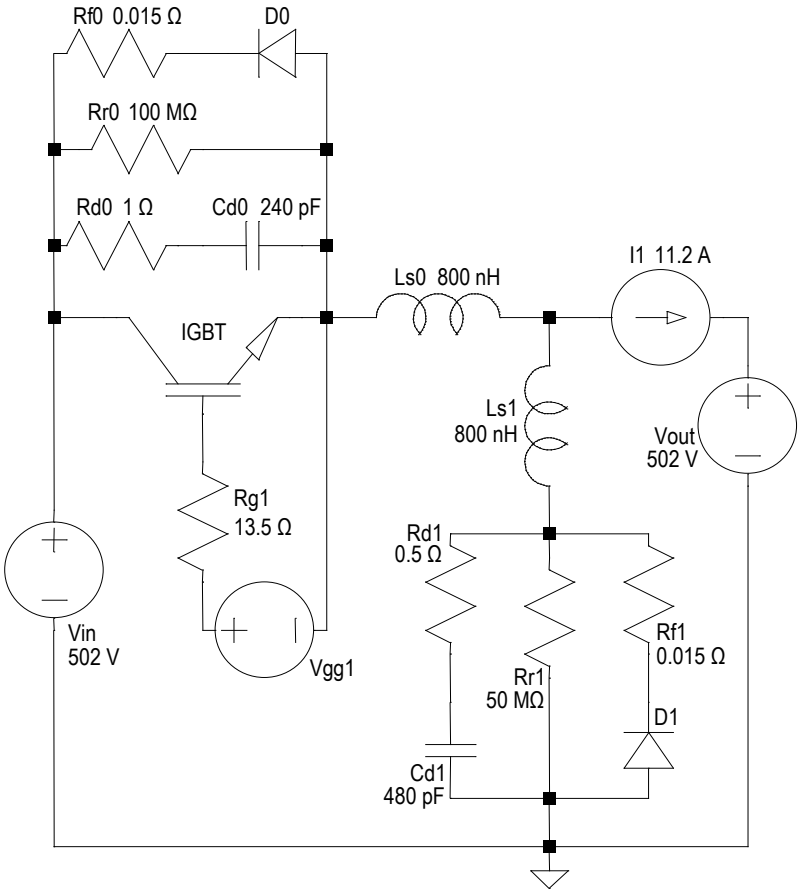


Figure 3.10: The simulation circuit for IGBT model validation.

device situation. To approximate the measured circuit conditions in the experiment, the V_{in} and the V_{out} are set to 502 V and the I_1 is set to 11.2 A for the 1 cm^2 active chip area. The on-state and the off-state IGBT gate driving voltages are set to 13.2 V and -13.2 V, respectively, to approximate the measured driving voltages of the IGBT gate drive in the experiment.

The comparison of a turn-off event is shown in Figure 3.11, where the solid lines represent the simulation results and the dashed lines represent the experiment results. In this simulation, the IGBT model parameters listed in Table 3.2 with the physics models selected and proportionally reduced low-level electron and hole lifetimes of 7.5 µs and 2.5 µs, respectively, are found to provide a close approximation to the experiment results. Regarding the V_{CE}, in the fast V_{CE}-I_C transient, initially at lower voltages the average experiment $V_{CE,ExpAvg}$ has a slight timing lead and a lower dV_{CE}/dt rate compared with the simulation $V_{CE,Sim}$. The $V_{CE,Sim}$ and the $V_{CE,ExpAvg}$ reach close agreement after they exceed 180 V. In the following tail time, the $V_{CE,Sim}$ is subject to a small undershoot, after which the $V_{CE,Sim}$ and the $V_{CE,ExpAvg}$ regain close agreement.

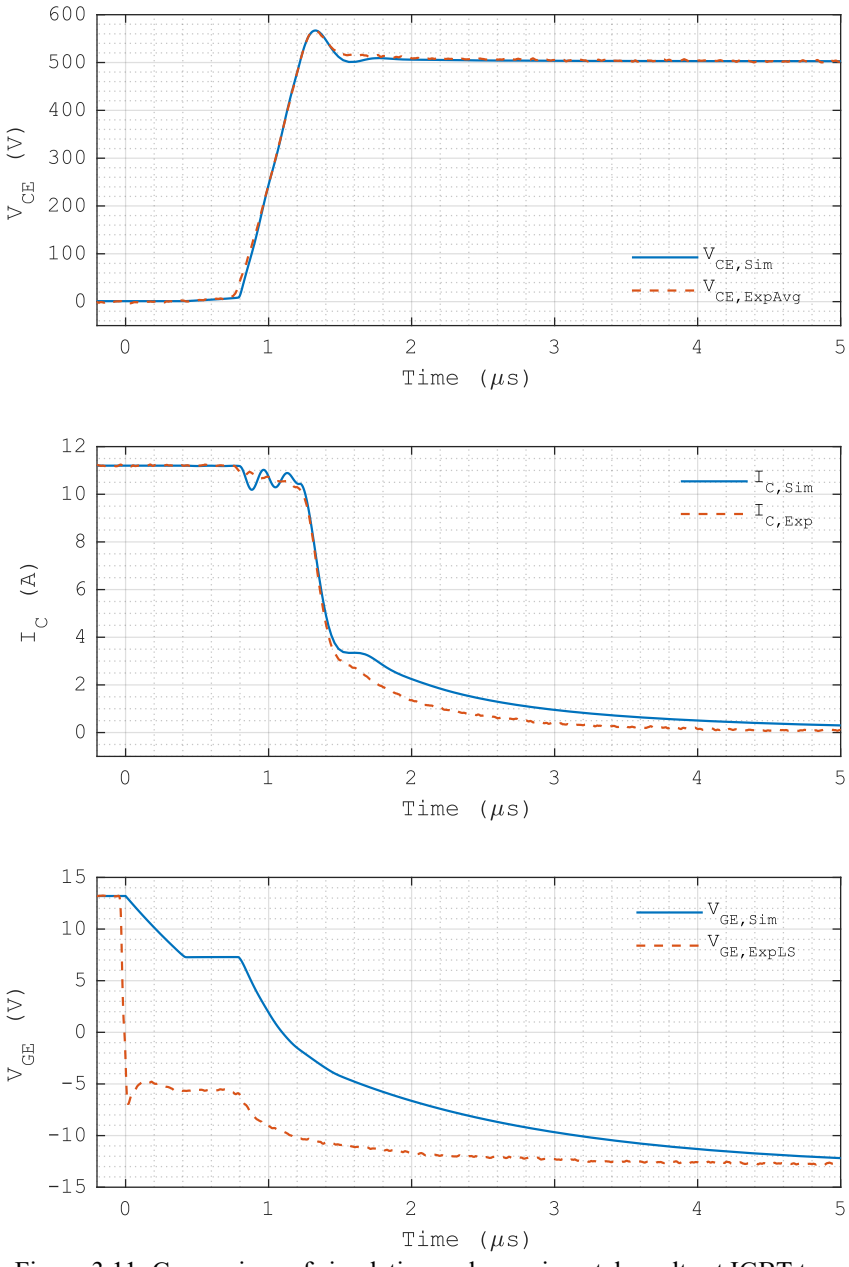


Figure 3.11: Comparison of simulation and experimental results at IGBT turn-off.

Regarding the I_C, the simulation $I_{C,Sim}$ shown in Figure 3.11 includes the current of the anti-parallel FWD circuit D_0 to match the experiment $I_{C,Exp}$ measured at the "C" terminal of the IGBT module which includes the current of the internal anti-parallel FWD. During the fast V_{CE} rising, the $I_{C,Sim}$ is subject to ringing compared with the $I_{C,Exp}$. During the V_{CE} overshoot, the $I_{C,Sim}$ and the $I_{C,Exp}$ reach close agreement as they both fall rapidly. During the transition to the tail time, the $I_{C,Sim}$ is subject to a short holding period compared with the smooth transition of the $I_{C,Exp}$. In the tail time, the decay of the $I_{C,Sim}$ and the decay of the $I_{C,Exp}$ are similar, with slightly faster decay observed in the $I_{C,Exp}$.

Regarding the V_{GE}, in the experiments the low-side IGBT $V_{GE,ExpLS}$ is measured between the 'G'-'E' package terminals of the IGBT module, which is affected by the internal gate resistance. Therefore, the $V_{GE,Sim}$ and the $V_{GE,ExpLS}$ are not comparable as in the simulation the $V_{GE,Sim}$ is measured directly between the 'G'-'E' electrodes of the IGBT chip. Nevertheless, the timings of the key turning points in the V_{GE} at approx. 0.4 µs and 0.8 µs show close agreement between the $V_{GE,Sim}$ and the $V_{GE,ExpLS}$.

The differences between the simulation and the experiment results are contributed by the modelling of the switching circuit and the IGBT device. Regarding the switching circuit, the simulation circuit uses independent voltage sources to provide input and output voltages and an independent current source to provide an inductive load current to obtain directly controlled and consistent load conditions for the IGBTs. A major difference arising from this circuit configuration is in the circuit impedance, where an independent current source is converted into an open circuit and an independent voltage source is converted into a short circuit. Therefore, compared with the experiment circuit, regarding the RLC resonant frequency of the CCL, the simulation circuit lacks the large output capacitors and a set of large input capacitors used in the experiment circuit. As a result, the RLC resonant frequency, proportional to $(LC)^{-0.5}$, of the CCL in the simulation circuit is higher compared with that in the experiment circuit. Also, the RLC damping factor, proportional to $(C/L)^{0.5}$, of the CCL in the simulation circuit is smaller compared with that in the experiment circuit. Hence, obvious oscillations in the $I_{C,Sim}$ and the $V_{CE,Sim}$ are observed in the fast V_{CE}-I_C transient, which affects the agreement between the simulation and the experiment results. The lack of modelling of parasitic capacitances in the simulation circuit also contributes to the disagreements between the results.

Another major difference arising from the circuit modelling is in the output capacitances of the FWDs, where the voltage dependent off-state output capacitance of an FWD is implemented by a fixed capacitance at an estimated average value. This method improves the numerical convergence in the simulation but introduces circuit errors in the fast V_{CE}-I_C transient, although would not qualitatively alter the turn-off V_{CE} divergence. These errors are larger at a lower load current where the IGBT on-state excess carrier profile is lower.

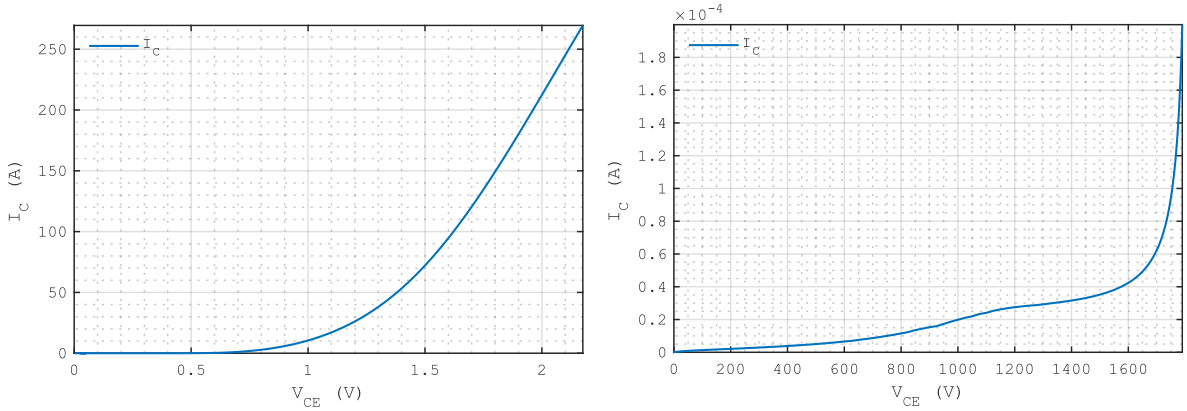
It is also noteworthy that the two IGBTs in series in the experiment are likely to be affected by a relative timing jitter in the gate driving, which causes a delay in the fast V_{CE} rising between the two IGBTs. As the V_{CE} in the experiment result in the comparison is 50% of the total V_{CE} of the two IGBTs, this delay in the fast V_{CE} rising reduces the average dV_{CE}/dt rate at the beginning of the fast V_{CE} rising, where a disagreement between the results is observed.

Regarding the IGBT structure, a factor that affects the agreement of the results is the likely use of a more advanced IGBT design for the Fuji Electric IGBTs used in the experiment. A 1700 V trench-FS IGBT featuring a 3D structure with micro P-base regions from Fuji Electric was reported in 2011 [74] shortly after the release of their V series IGBTs of 1700 V used in the experiment. Considering that it is unusual for power semiconductor manufacturers to reveal a device design before the related product release, although not explicitly specified, it is likely that such a 3D IGBT design has been used in the IGBTs in the experiment. The improved trade-off between the on-state and the switching performance gained from the 3D IGBT design [74] can enable the faster decay of the tail current in the experiment. In the simulation, the low-level carrier lifetimes in the recombination models used have to be reduced to achieve comparable decay of the tail current. Further reduction in the low-level carrier lifetimes would be a deviation.

Overall, the IGBT model and the switching circuit for the simulation are capable of reproducing the key turn-off characteristics of an actual FS IGBT. The modelling objective here is not for reverse engineering, but for IGBT and circuit models that can reproduce the typical turn-off characteristics of modern FS IGBTs to a reasonable extent. Simulation using a 3D IGBT model and an FEM FWD model is possible at the cost of significant increase in computing resource consumption. Hence, such a trade-off has to be considered. The 2D IGBT model, the FWD equivalent circuit, and the rest of the simulation setup here do not qualitatively alter the basics of modern FS IGBTs or the turn-off V_{CE} divergence while providing acceptable simulation speed with reasonable accuracy, which is suitable for the intended research objectives here.

Figure 3.12 shows the static I-V characteristics of the base IGBT model of 1 cm^2 at the external temperature of 300 K. In the static on-state at V_{GE} = 15 V, Figure 3.12 (a), significant increase in the I_C emerges after the V_{CE} exceeds 0.7 V with rapid growth after the V_{CE} exceeds 1.5 V, where I_C = 130 A is achieved at V_{CE} = 1.734 V. In the static forward-blocking off-state at V_{GE} = 0 V, Figure 3.12 (b), the I_C starts to increase rapidly after the V_{CE} exceeds 1700 V.

Figure 3.13 shows the vertical cutlines, along y = 0-175 µm at x = 1.5 µm in Figure 3.5, of the electric field and the doping profile of the base IGBT model at static V_{CE} = 1200 V. At approx. 169 µm where the N buffer joins the N-drift region, the electric field reaches a low level near zero, suggesting a static punch-through voltage $V_{PT} \approx$ 1200 V. In Figure 3.12 (b), at V_{CE} near 1200 V, a decrease in the dI_C/dV_{CE} rate is observed, which also suggests that the depletion



(a) (b)

Figure 3.12: Static I-V characteristics of the base IGBT model at 300 K external temperature: (a) on-state at V_{GE} = 15 V, and (b) off-state at V_{GE} = 0 V.

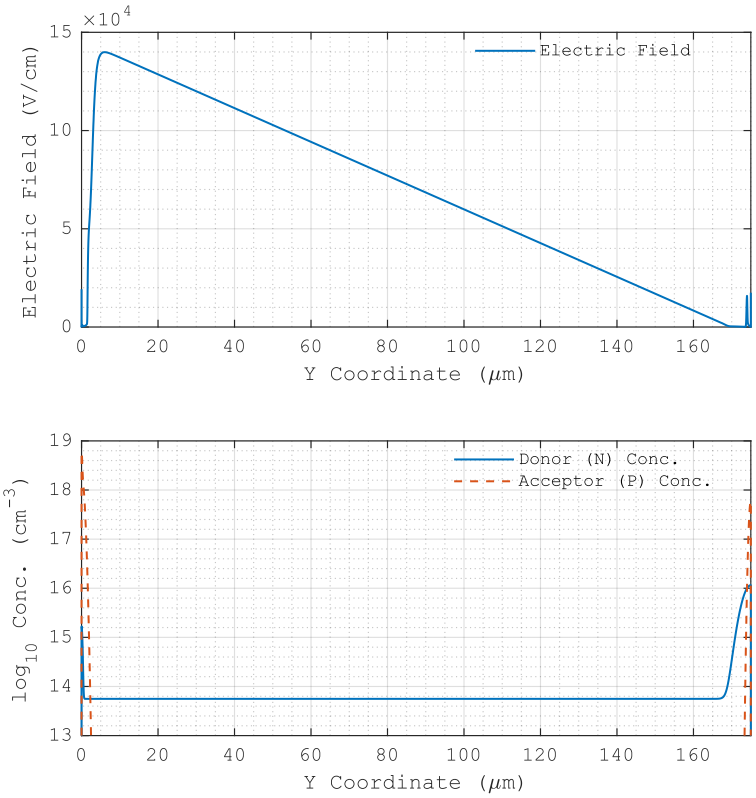


Figure 3.13: The vertical cutlines, along y = 0-175 µm at x = 1.5 µm in Figure 3.5, of the electric field and the doping profile of the base IGBT model at V_{CE} = 1200 V.

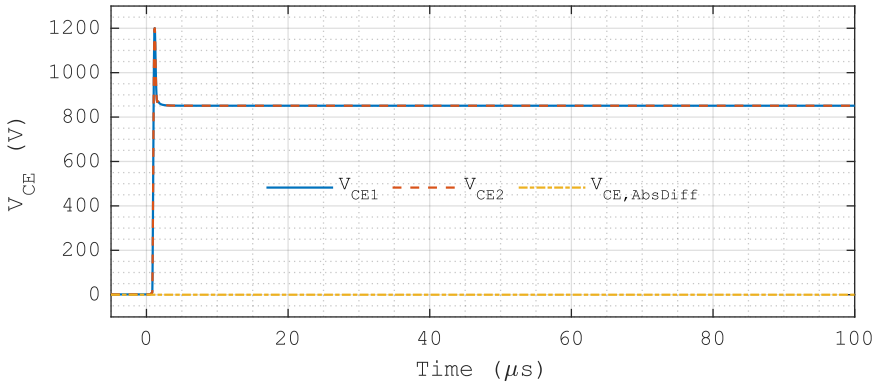


Figure 3.14: Turn-off of two IGBTs in series with identical IGBT model and control.

region punches through the N-drift region and reaches the N buffer, Figure 3.13. As the electric field is "stopped" in the N buffer, the expansion of the depletion region with the V_{CE} is reduced and so is the growth of the generation current in it, and thus the reduction in the dI_C/dV_{CE} rate.

Figure 3.14 shows the turn-off simulation of two IGBTs using identical IGBT model and gate driving parameters. This is to demonstrate that the mesh of the IGBT model, the physics model selection, and the numerical settings would not introduce any significant V_{CE} divergence. In Figure 3.14 the V_{CE1} and the V_{CE2} overlap and the absolute V_{CE} difference $V_{CE,AbsDiff}$ remains at zero level in the entire simulation, including a 100 µs nominal off-state, approx. 10 times of the high-level carrier lifetime in the IGBT N base. Due to the stray inductance in the CCL, for one IGBT the V_{CE} overshoot peaks at approx. 350 V above the 850 V average off-state V_{CE}.

3.5 Simulations of Individual V_{CE} Diverging Factors

The simulations of the individual V_{CE} diverging factors included in section 3.3.1 are presented in this section, following the discussions of their V_{CE} diverging effects in section 3.3.4.

3.5.1 An Output Delay in the IGBT$_1$ Gate Drive

Figure 3.15 shows the turn-off simulation of two IGBTs in series with a 10 ns gate drive output delay applied to the IGBT$_1$. The V_{CE} divergence produced by the IGBT gate drive output delay represents one of the two basic V_{CE} diverging scenarios discussed in section 3.3.4 that features a delay in the depletion progress in the CSR of the same on-state excess carrier profile. In this case, the absolute V_{CE} difference $V_{CE,AbsDiff}$ is defined as ($V_{CE2} - V_{CE1}$) and reaches its maximum of 438.06 V at 11.659 µs before starts to decrease slowly. To reveal more V_{CE} diverging details, the first 15 µs of this turn-off is shown in Figure 3.15. The difference in V_{GE} is very small on this time scale. No significant difference in I_C is observed.

After the initial gate discharging period from 0 µs to approx. 0.8 µs, the V_{CE2} starts to increase rapidly ahead of the V_{CE1}, causing a rapid but small increase in the $V_{CE,AbsDiff}$ at first. The $V_{CE,AbsDiff}$ remains small while the total V_{CE} rises to the V_{DC}. During the V_{CE} overshoot, the V_{CE2} remains higher than the V_{CE1}, but the $V_{CE,AbsDiff}$ starts to decrease as the I_C falls rapidly.

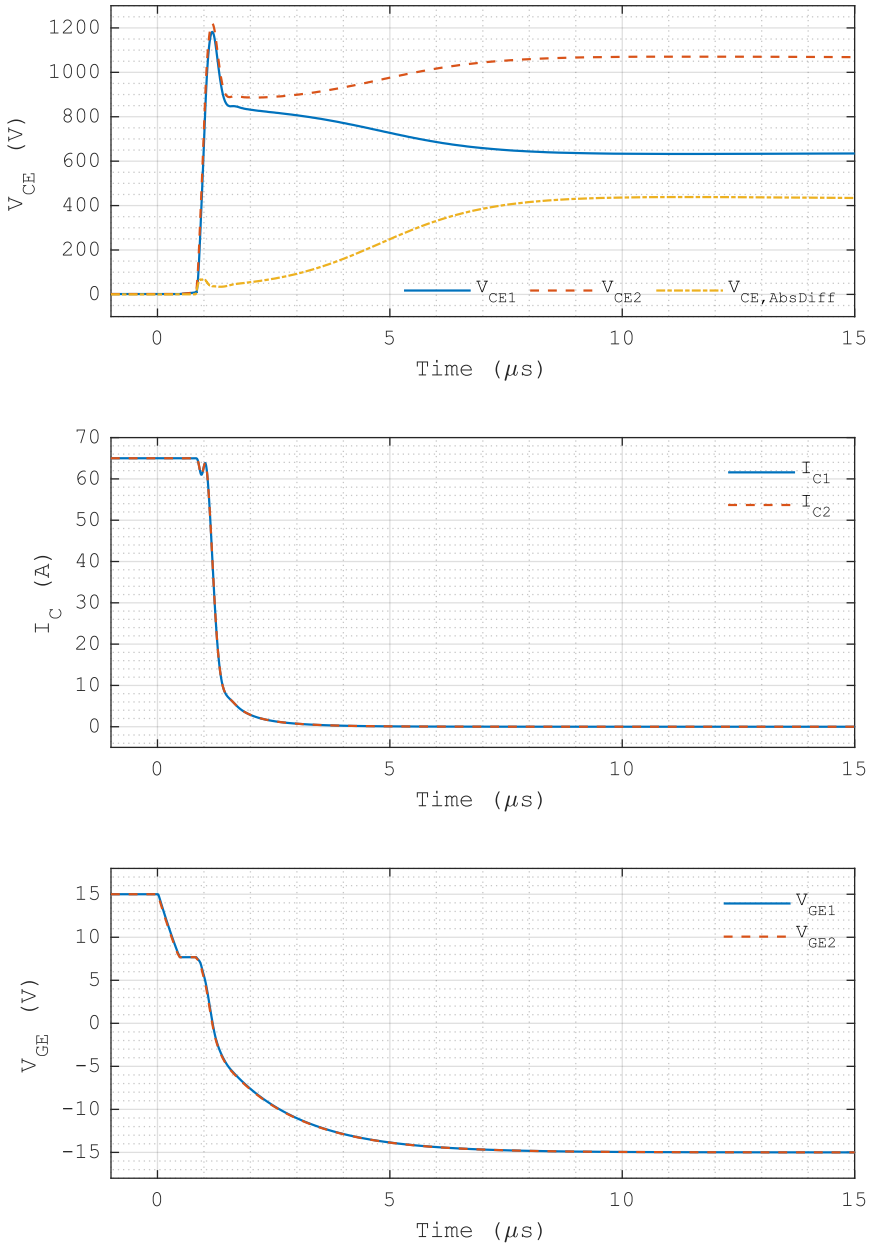


Figure 3.15: Turn-off of two IGBTs in series with a 10 ns gate driving delay applied to the IGBT$_1$.

Similar diverging characteristics are observed in the experiment result shown in Figure 3.3. As the I_C falls, the electric field gradient in the depletion region decreases due to the decrease in the hole carrier profile under the high electric field in the depletion region which is related to the I_C. This reduces the difference in the integral of the electric field over the depletion region, and hence the reduction in the $V_{CE,AbsDiff}$.

In the tail time, the $V_{CE,AbsDiff}$ starts to increase again as the lead of the V_{CE2} over the V_{CE1} increases. In terms of magnitude, the main V_{CE} divergence arises in the tail time over a long period, in which the maximum V_{CE} divergence of 438.06 V is reached at 11.659 µs. At such a point the intrinsic leakage current based on the carrier generation in the depletion region prevails over the hole diffusion current in the undepleted part of the N base towards the depletion region.

Figure 3.16 shows the V_{CE} in the full 100 µs of the turn-off and the off-state. After peaks at 11.659 µs, the $V_{CE,AbsDiff}$ starts to decrease gradually. This V_{CE} converging process is considerably slower than the V_{CE} diverging process in the tail time. The V_{CE2} remains above the V_{CE1} in the entire IGBT turn-off and off-state in this simulation.

Figure 3.17 to Figure 3.19 show respective comparisons of the electric field and the hole carrier profiles, along y = 0-175 µm at x = 1.5 µm in Figure 3.5, between the $IGBT_1$ and the $IGBT_2$ at different times during the turn-off shown in Figure 3.15. The traces sampled at the same time are grouped and indicated, and the timestamps refer to the time axis in Figure 3.15.

The traces in Figure 3.17 are sampled at different times from 0.81 µs to 1.02 µs during the rising of the total V_{CE} from the MOS channel cut-off to the V_{DC} in Figure 3.15. At 0.81 µs when the MOS channel is just cut off, only minor differences in the electric field and the hole carrier profiles caused by the delay in the IGBT gate drive output can be observed. At 0.93 µs, the total V_{CE} rises to approx. 50% of the V_{DC}. Clear gaps between the electric field and the hole carrier profiles, respectively, are observed, which are related to the V_{CE} divergence. The $IGBT_2$ leads in the depletion progress, which is related to its lead in the V_{CE} sharing. At 1.02 µs, the total V_{CE} rises to approx. 100% of the V_{DC}. The respective gaps in the electric field and the hole carrier profiles narrow as the excess carrier concentrations at the MOS gate side CSR boundary increase with the expansion of the depletion regions and hence the expansion is reduced.

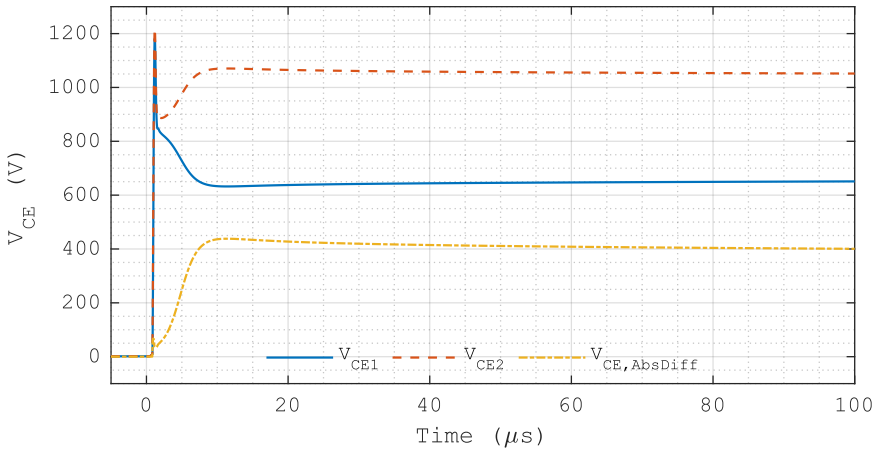


Figure 3.16: Turn-off of two IGBTs in series with a 10 ns gate driving delay applied to the $IGBT_1$.

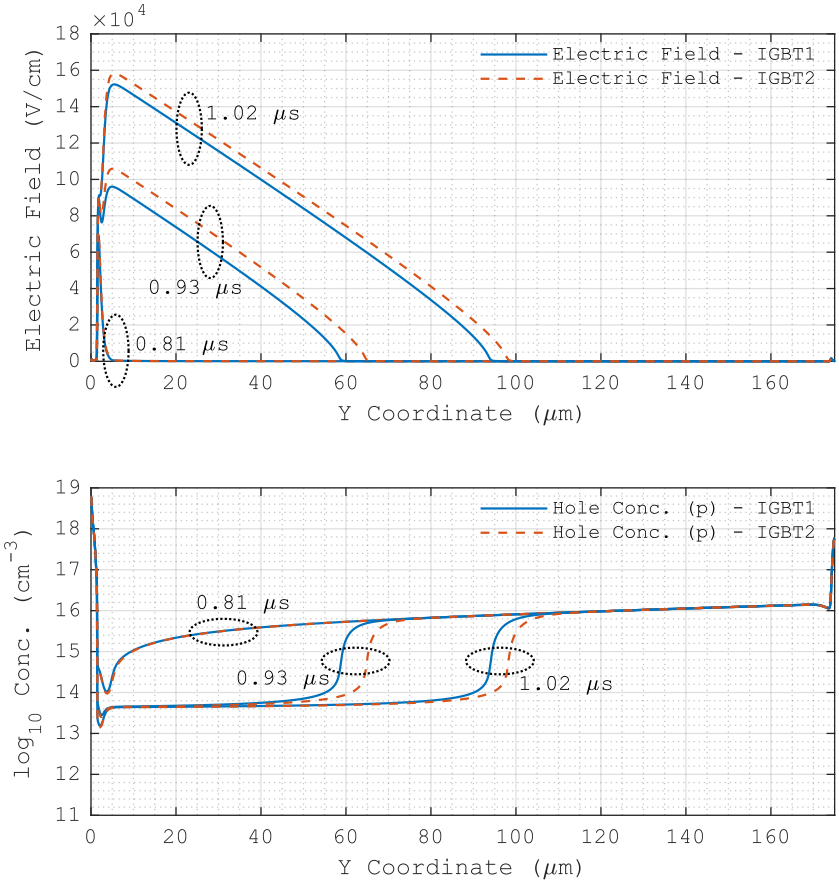


Figure 3.17: Comparisons of the electric field and the hole carrier profiles, along y = 0-175 µm at x = 1.5 µm in Figure 3.5. A 10 ns gate driving delay is applied to the $IGBT_1$.

The electric field gradients at 0.93 µs and 1.02 µs are similar as the IGBT I_C only decreases slightly while the total V_{CE} rises to the V_{DC}. In the part of the depletion region with a high electric field, the hole carrier profiles at 0.93 µs and 1.02 µs are also similar. This is due to the holes that reach the saturation velocity under a high electric field of the hole currents related to the same I_C that remains virtually at the load level. The respective hole carrier profiles in the remaining CSR in the IGBTs also remain virtually unchanged throughout the period covered in Figure 3.17. This is due to the ambipolar current in the remaining CSR is related to the same I_C that remains virtually at the load level.

The traces in Figure 3.18 are sampled following the trace set of 1.02 µs in Figure 3.17 at different times from 1.02 µs to 1.57 µs as the I_C falls from the load level to the initial tail current during the V_{CE} overshoot. At 1.21 µs, the I_C falls to approx. 50% of the load current, which results in decreases in the electric field gradients. Despite this, the expansion of the depletion regions from 1.02 µs still results in higher electric field profiles related to the V_{CE} overshoot. As the I_C falls, the hole carrier profiles in the depletion regions under high electric fields decrease accordingly. Also, small decreases are observed in the hole carrier profiles in the undepleted parts of the N bases due to the decrease in the I_C. At 1.57 µs, the I_C falls to the initial tail current while the total V_{CE} falls to near the V_{DC} level. The electric field gradients continue to decrease, and with limited depletion from 1.21 µs, the electric field profiles decrease and the V_{CE} overshoot completes. The hole carrier profiles in the depletion regions continue to decrease as the I_C falls. At 1.57 µs, the decreases in the hole carrier profiles in the undepleted parts of the

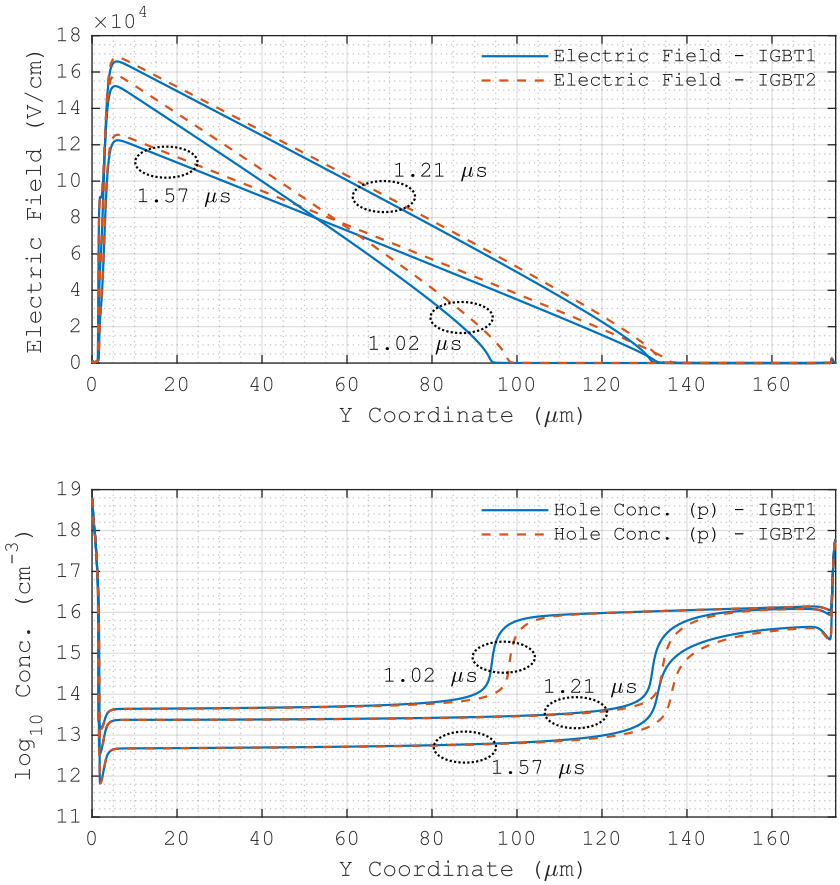


Figure 3.18: Comparisons of the electric field and the hole carrier profiles, along y = 0-175 μm at x = 1.5 μm in Figure 3.5. A 10 ns gate driving delay is applied to the $IGBT_1$.

N bases become significant. Until this point, the V_{CE} divergence caused by the delayed IGBT gate drive output is still small.

The traces in Figure 3.19 are sampled following the trace set of 1.57 μs in Figure 3.18 at different times from 1.57 μs to 11.25 μs in the tail time, where in terms of magnitude the main V_{CE} divergence develops. At 5.35 μs, the I_C falls to approx. 0.065 A, 1% of the initial tail current of approx. 6.5 A. As the I_C falls, the hole carrier profiles and the electric field gradients continue to decrease. Compared with the trace sets at 1.57 μs, in the $IGBT_1$ the depletion edge near 135 μm remains virtually unchanged while the peak electric field in the depletion region decreases. In contrast, in the $IGBT_2$ the peak electric field in the depletion region remains virtually unchanged while the depletion region has an obvious expansion. The gap between the electric field profiles has a significant increase which is related to the increase in the V_{CE} divergence in this period. In the depletion regions, the hole carrier profiles continue to decrease while the difference in concentration between them remains small. However, in the undepleted parts of the N bases, the difference between the hole carrier profiles becomes significant as the hole carrier profile in the $IGBT_2$ decreases faster and becomes narrower.

The respective trends in the electric field and the hole carrier profiles from 1.57 μs to 5.35 μs continue to 11.25 μs. In the $IGBT_1$ the depletion region contracts and the peak electric field decreases, while in the $IGBT_2$ the depletion region expands and the peak electric field increases. This is related to the continuous increase in the V_{CE} divergence from 5.35 μs to 11.25 μs. From 5.35 μs to 11.25 μs, in the depletion regions with high electric fields, the hole carrier profiles

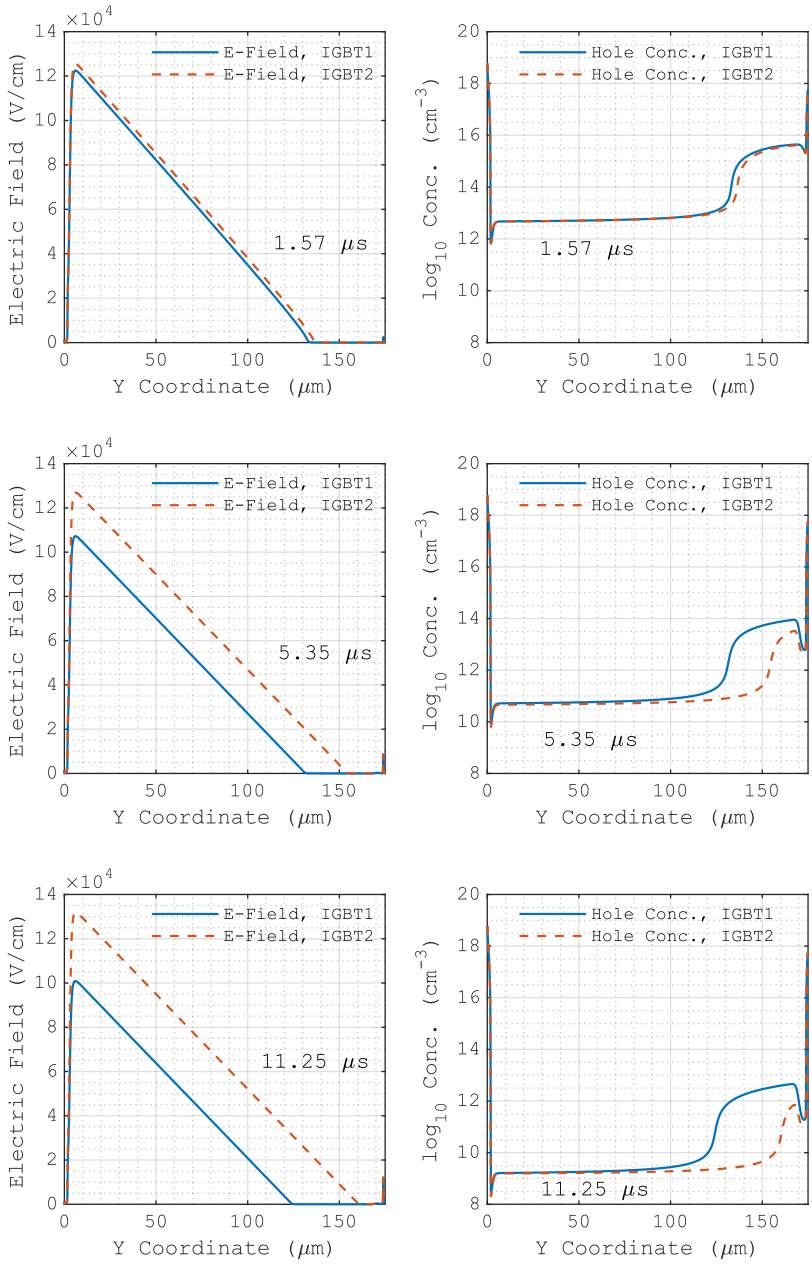


Figure 3.19: Comparisons of the electric field and the hole carrier profiles, along y = 0-175 μm at x = 1.5 μm in Figure 3.5. A 10 ns gate driving delay is applied to the $IGBT_1$.

continue to decrease and the difference in concentration between them remains small. However, in the undepleted parts of the N bases, the difference between the hole carrier profiles continues to increase with the same trend from 1.57 μs to 5.35 μs. At this point, in the undepleted parts of the N bases, the hole carrier profiles have decreased below the N-type doping profiles (not shown) in both the $IGBT_1$ and the $IGBT_2$.

In both the fast V_{CE}-I_C transient and the tail time in this IGBT turn-off simulation, the simulation results agree with the theoretical results of the V_{CE} divergence caused by a gate driving delay in an IGBT discussed in the case 1) in section 3.3.4.

3.5.2 $IGBT_1$ with a Higher P Emitter Doping Profile

Figure 3.20 shows the turn-off simulation of two IGBTs in series with the doping profile of the backside P emitter in the $IGBT_1$ increased by 5% in concentration. The V_{CE} divergence caused by a higher P emitter doping profile in an IGBT represents the other basic V_{CE} diverging

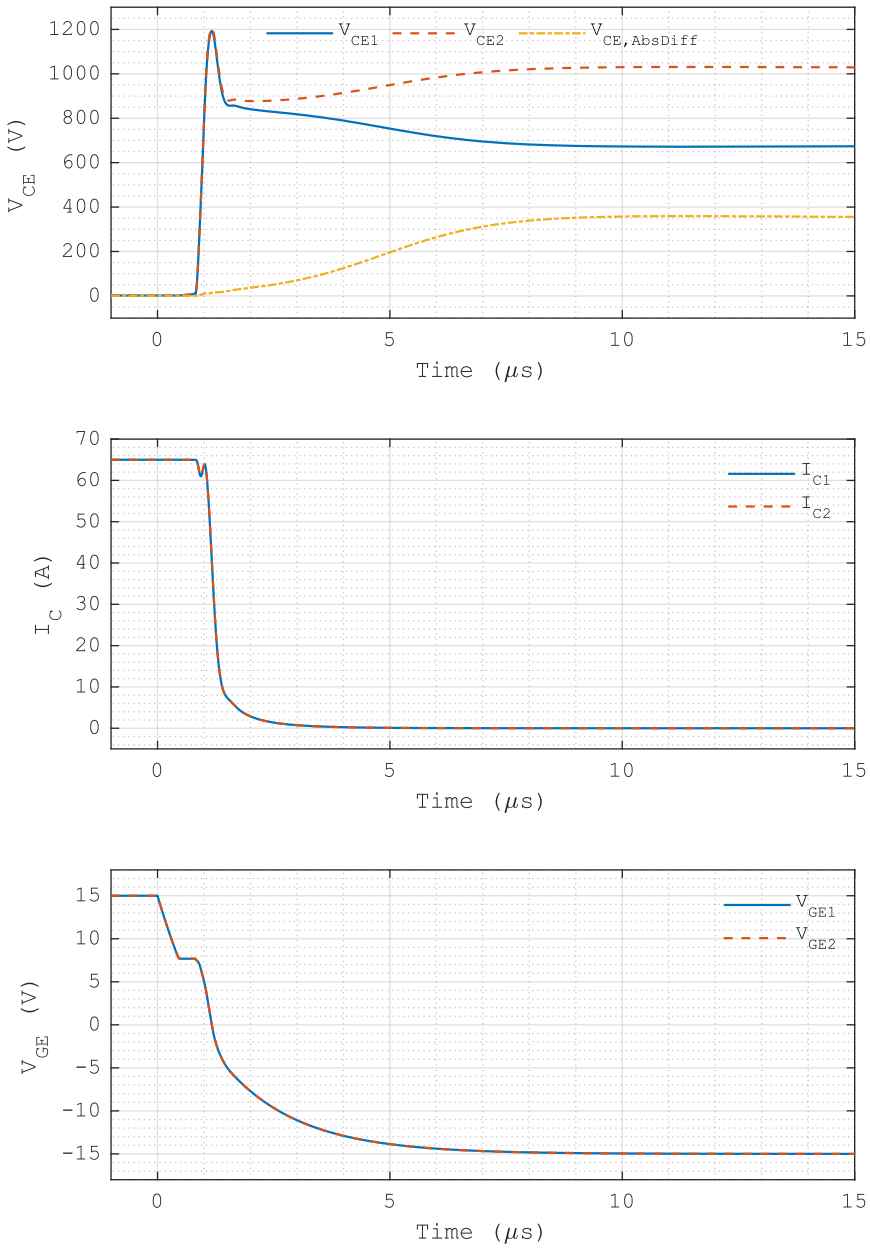


Figure 3.20: Turn-off of two IGBTs in series with the P emitter doping profile in the $IGBT_1$ increased by 5% in concentration.

scenario discussed in section 3.3.4 that features reduced expansion of the depletion region in the N base due to a higher excess carrier profile. Here, the $V_{CE,AbsDiff}$ is defined as ($V_{CE2} - V_{CE1}$) and reaches its maximum of 359.00 V at 11.25 µs before starts to decrease slowly. To reveal more V_{CE} diverging details, the first 15 µs of this turn-off is shown in Figure 3.20. No significant difference in the I_C or the V_{GE} is observed.

After the initial gate discharging period from 0 µs to approx. 0.8 µs, the V_{CE1} and the V_{CE2} both start to increase rapidly. During the fast V_{CE}-I_C transient, the V_{CE2} has a slight lead over the V_{CE1} due to the higher excess carrier profile in the $IGBT_1$ caused by its higher P emitter doping profile. Unlike the previous case of a 10 ns gate driving delay, here the $V_{CE,AbsDiff}$ first increases slowly, and during the V_{CE} overshoot the increase in the $V_{CE,AbsDiff}$ moderates as the I_C falls rapidly. In the tail time, as the lead of the V_{CE2} over the V_{CE1} increases, the $V_{CE,AbsDiff}$ continues to increase and reaches its maximum of 359.00 V at 11.250 µs. In terms of magnitude, the main V_{CE} divergence also arises in the tail time over a long period.

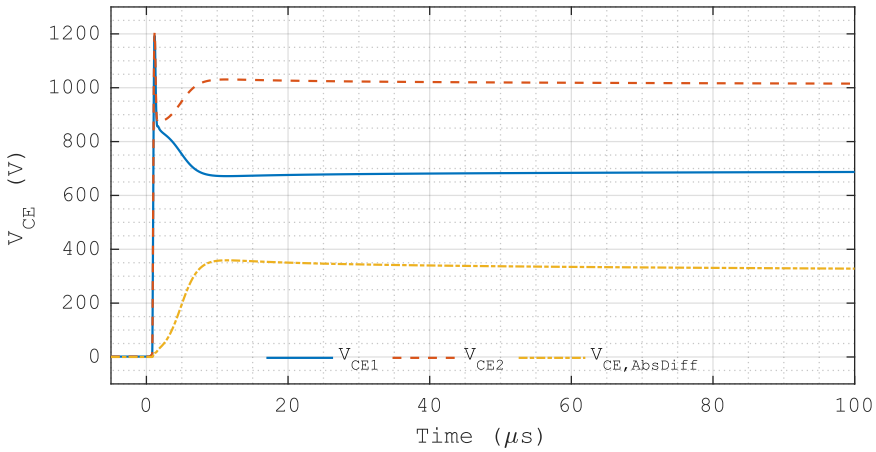


Figure 3.21: Turn-off of two IGBTs in series with the P emitter doping profile in the $IGBT_1$ increased by 5% in concentration.

Figure 3.21 shows the V_{CE} in the full 100 µs of the turn-off and the off-state. After peaks at 11.250 µs, the $V_{CE,AbsDiff}$ also starts to decreases gradually. This V_{CE} converging process is also considerably slower than the V_{CE} diverging process in the tail time. The V_{CE2} remains above the V_{CE1} in the entire turn-off and off-state in this simulation.

Figure 3.22 to Figure 3.24 show respective comparisons of the electric field and the hole carrier profiles, along y = 0-175 µm at x = 1.5 µm in Figure 3.5, between the $IGBT_1$ and the $IGBT_2$ at different times during the turn-off shown in Figure 3.20. The traces sampled at the same time are grouped and indicated, and the timestamps refer to the time axis in Figure 3.20.

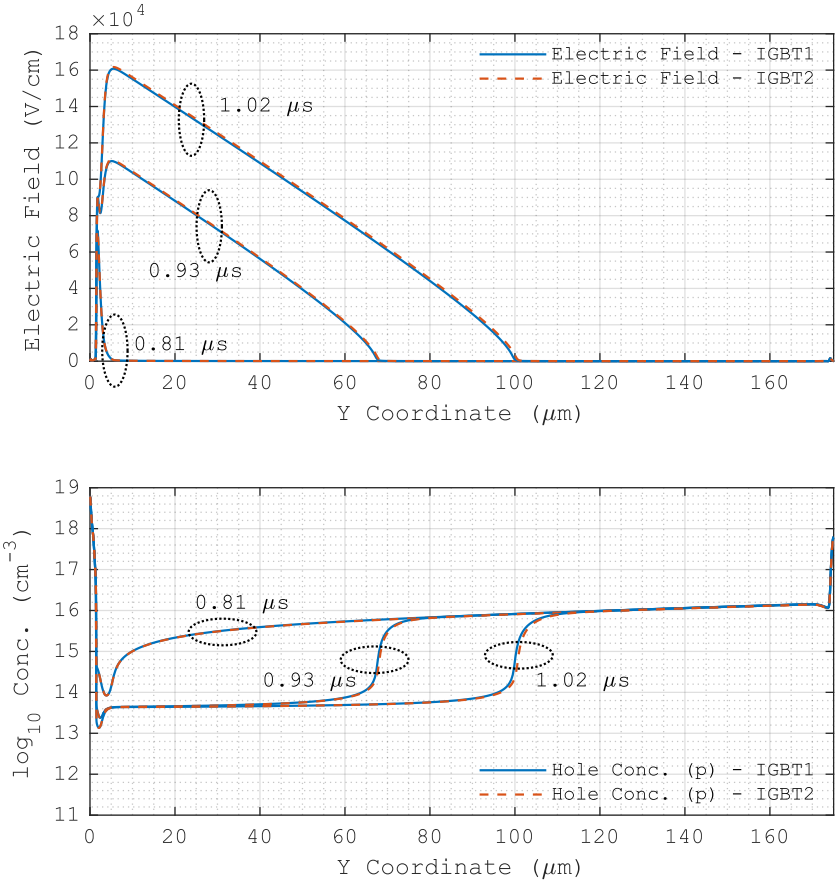


Figure 3.22: Comparisons of the electric field and the hole carrier profiles, along y = 0-175 µm at x = 1.5 µm in Figure 3.5. The P emitter doping concentration in the $IGBT_1$ is increased by 5%.

The traces in Figure 3.22 are sampled at different times from 0.81 µs to 1.02 µs during the rising of the total V_{CE} from the MOS channel cut-off to the V_{DC} in Figure 3.20. At 0.81 µs when the MOS channel is just cut off, no obvious difference in the electric field or the hole carrier profiles between the $IGBT_1$ and the $IGBT_2$ can be observed. Due to the higher P emitter doping profile, the hole carrier profile in the $IGBT_1$ is slightly higher than that in the $IGBT_2$, however, on the scale presented such a small difference is not visually obvious. At 0.93 µs, the total V_{CE} reaches approx. 50% of the V_{DC}. Slight differences in the electric field and the hole carrier profiles can be observed. The $IGBT_2$ with a lower hole carrier profile in the N base leads in the depletion progress, which results in a higher electric field profile in the depletion region and a narrower and lower hole carrier profile in the remaining CSR. At 1.02 µs, the total V_{CE} rises to approx. 100% of the V_{DC}. The electric field gradients at 1.02 µs are similar to those at 0.93 µs as the IGBT I_C remains virtually at the load level before the current commutation during the V_{CE} overshoot. The respective gaps between the electric field and the hole carrier profiles widen slightly compared with those at 0.93 µs. Those gaps during the fast V_{CE}-I_C transient are much smaller compared with those in the previous case of an IGBT gate driving delay. The respective hole carrier profiles in the remaining CSRs in the IGBTs remain virtually unchanged throughout the period covered in Figure 3.22 as the IGBT I_C remains virtually at the load level.

The traces in Figure 3.23 are sampled following the trace set of 1.02 µs in Figure 3.22 at different times from 1.02 µs to 1.57 µs as the I_C falls from the load level to the initial tail current during the V_{CE} overshoot. At 1.21 µs, the I_C falls to approx. 50% of the load current, which reduces the electric field gradients. Still, the expansion of the depletion regions since 1.02 µs

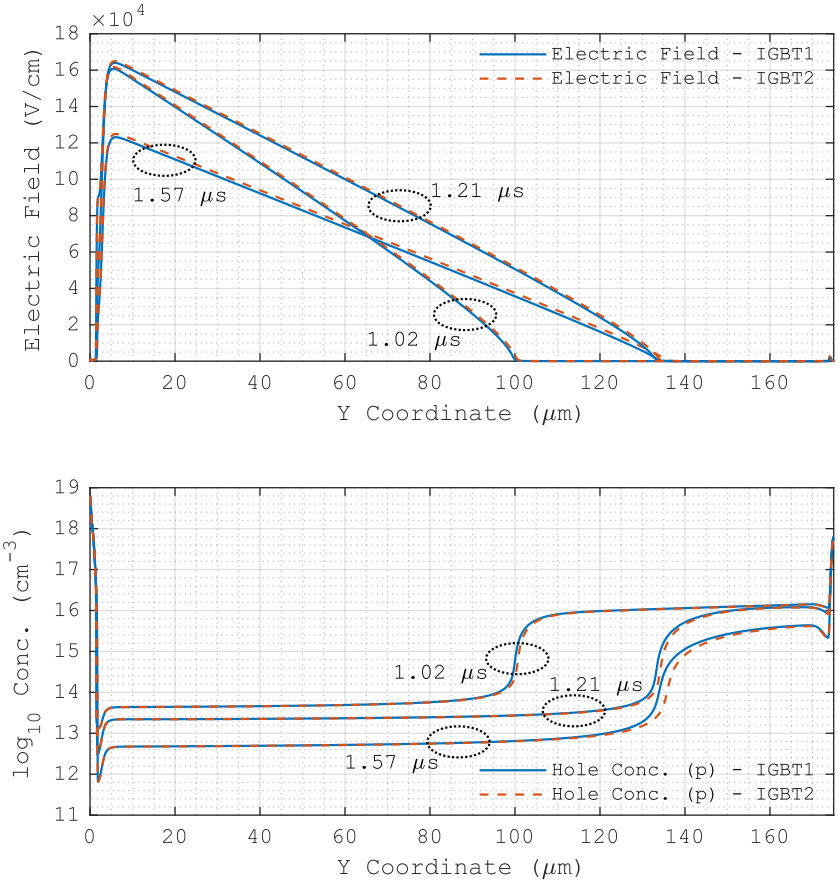


Figure 3.23: Comparisons of the electric field and the hole carrier profiles, along y = 0-175 µm at x = 1.5 µm in Figure 3.5. The P emitter doping concentration in the $IGBT_1$ is increased by 5%.

results in higher electric field profiles related to the V_{CE} overshoot with slight increases in the peak electric field. As the I_C falls, the hole carrier profiles in the undepleted parts of the N bases decrease. In the depletion regions, the hole carrier profiles under high electric fields also decrease. The respective gaps between the electric field and the hole carrier profiles increase slightly but are still small compared with those in the previous case of an IGBT gate driving delay. At 1.57 µs, the I_C falls to the initial tail current while the total V_{CE} falls to near the V_{DC} level. The depletion regions only expand slightly while the electric field gradients continue to decrease, which results in the total V_{CE} falling back to the V_{DC} level and completes the V_{CE} overshoot. The hole carrier profiles in the depletion regions continue to decrease. The hole carrier profiles in the undepleted parts of the N bases show significant decreases as the I_C falls to the initial tail current. The respective gaps between the electric field and the hole carrier profiles continue to widen compared with those at 1.21 µs but are still smaller than those in the previous case of an IGBT gate driving delay.

The traces in Figure 3.24 are sampled following the trace set of 1.57 µs in Figure 3.23 at different times from 1.57 µs to 11.25 µs in the tail time, where in terms of magnitude the main V_{CE} divergence develops. The respective trends in the electric field and the hole carrier profiles in the tail time here are similar to those in the previous case of an IGBT gate driving delay. At 5.35 µs, the I_C falls to approx. 0.065 A, 1% of the initial tail current of approx. 6.5 A. As the I_C falls, the hole carrier profiles and the electric field gradients continue to decrease. Compared with the trace sets at 1.57 µs, in the $IGBT_1$ the depletion edge near 135 µm remains virtually unchanged while the peak electric field in the depletion region decreases. In contrast, in the $IGBT_2$ the peak electric field in the depletion region remains virtually unchanged while the depletion region expands. The gap between the electric field profiles has a significant increase which is related to the increase in the V_{CE} divergence in this period. In the depletion regions, the hole carrier profiles continue to decrease while the difference in concentration between them remains small. However, in the undepleted parts of the N bases, the difference between the hole carrier profiles becomes significant as the hole carrier profile in the $IGBT_2$ decreases faster and becomes narrower.

The respective trends in the electric field and the hole carrier profiles from 1.57 µs to 5.35 µs continue to 11.25 µs. At 11.25 µs, the $V_{CE,AbsDiff}$ reaches its maximum. In the $IGBT_1$ the depletion region contracts and the peak electric field decreases, while in the $IGBT_2$ the depletion region expands and the peak electric field increases. This is related to the continuous increase in the V_{CE} divergence from 5.35 µs to 11.25 µs. From 5.35 µs to 11.25 µs, in the depletion regions with high electric fields, the hole carrier profiles continue to decrease and the difference in concentration between them remains small. However, in the undepleted parts of the N bases, the difference between the hole carrier profiles continues to increase with the same trend from 1.57 µs to 5.35 µs. At this point, in the undepleted parts of the N bases, the hole carrier profiles have decreased below the N-type doping profiles (not shown) in both the $IGBT_1$ and the $IGBT_2$.

In both the fast V_{CE}-I_C transient and the tail time in this IGBT turn-off simulation, the simulation results agree with the theoretical results of the V_{CE} divergence caused by a higher P emitter doping profile in an IGBT discussed in the case 2) in section 3.3.4.

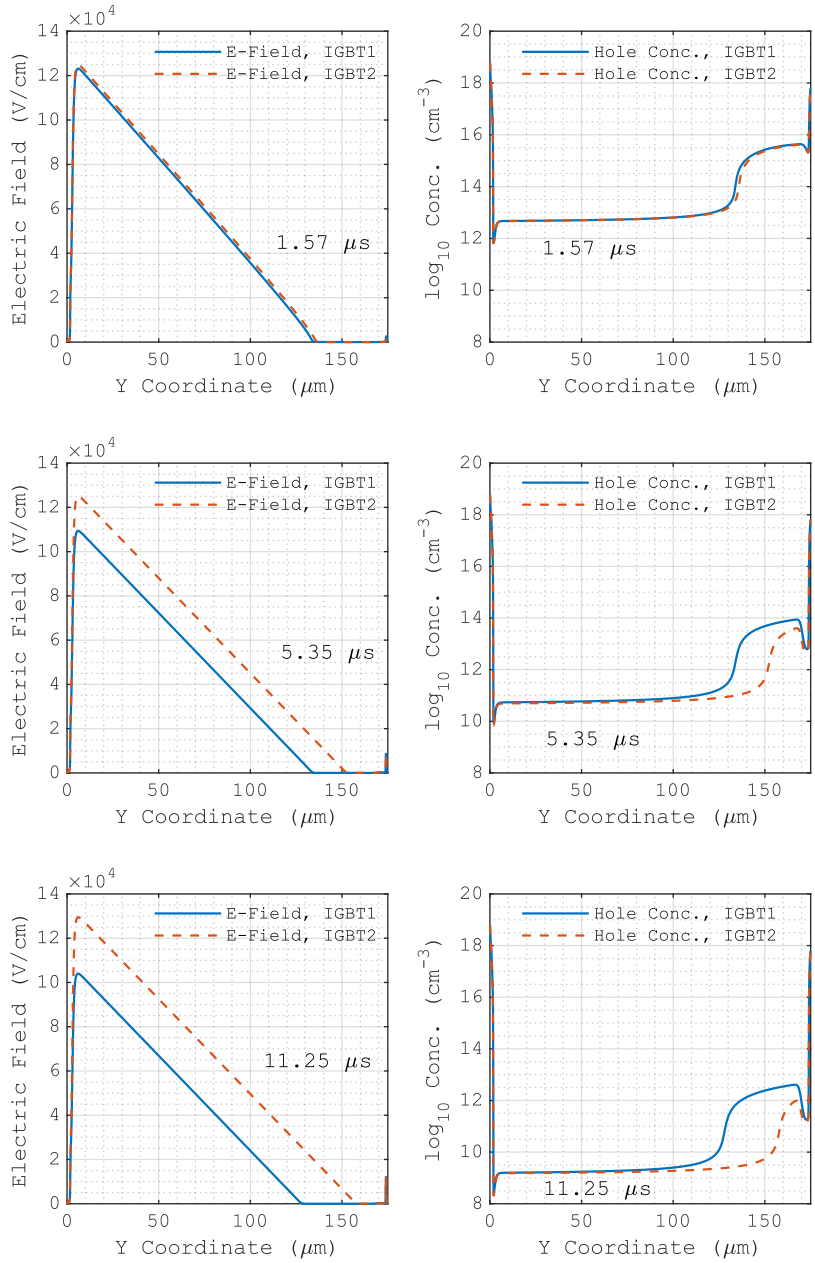


Figure 3.24: Comparisons of the electric field and the hole carrier profiles, along y = 0-175 µm at x = 1.5 µm in Figure 3.5. The P emitter doping concentration in the $IGBT_1$ is increased by 5%.

This scenario with a higher P emitter doping profile and the previous scenario with an IGBT gate driving delay are the two basic V_{CE} diverging scenarios here. Their respective V_{CE} diverging mechanisms in different turn-off phases can be used in combinations to account for the V_{CE} diverging effects of the other V_{CE} diverging factors included in this thesis. Hence, the internal IGBT states in the turn-off simulations of the other V_{CE} diverging factors will not be shown.

3.5.3 $IGBT_1$ with a Higher Gate Resistance

Figure 3.25 shows the turn-off simulation of two IGBTs in series with the gate resistance for the $IGBT_1$ increased by 1%. The higher gate resistance reduces the gate discharging current during the IGBT turn-off, which delays the MOS channel cut-off. Therefore, according to section 3.3.4, the V_{CE} divergence caused by a higher gate resistance in an IGBT can be considered as a variant of the basic scenario of an IGBT gate driving delay discussed in section 3.5.1, where the $IGBT_1$ is delayed by its higher gate resistance. Here, the $V_{CE,AbsDiff}$ is defined as ($V_{CE2} - V_{CE1}$)

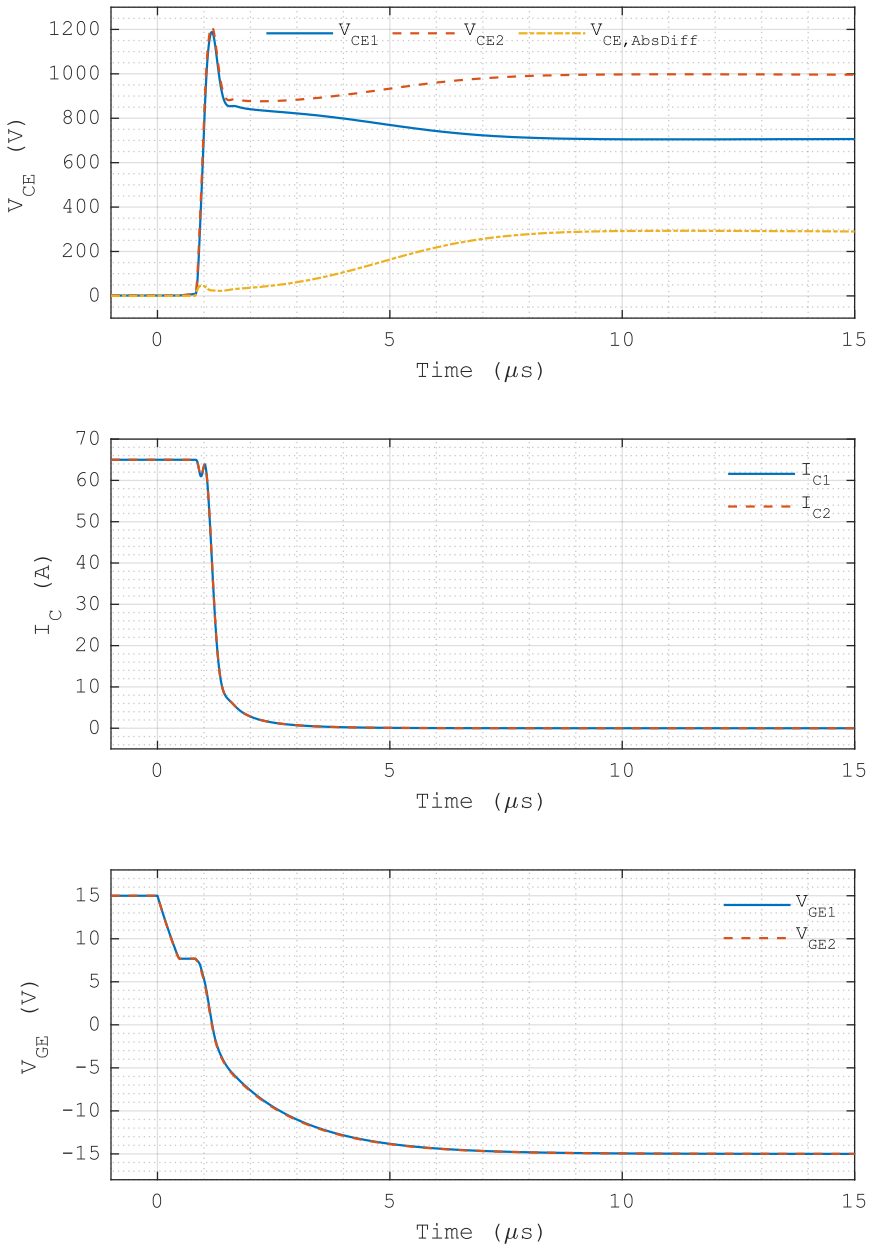


Figure 3.25: Turn-off of two IGBTs in series with the gate resistance for the $IGBT_1$ increased by 1%.

and reaches its maximum of 293.09 V at 11.138 µs before starts to decrease slowly. To reveal more V_{CE} diverging details, the first 15 µs of this turn-off is shown in Figure 3.25. The difference in V_{GE} is very small on this time scale. No significant difference in I_C is observed.

After the initial gate discharging period from 0 µs to approx. 0.8 µs, the V_{CE2} starts to increase ahead of the V_{CE1}. Due to the delay in the MOS channel cut-off in the $IGBT_1$, the $V_{CE,AbsDiff}$ has a rapid increase at first but remains small while the total V_{CE} rises to the V_{DC}. During the V_{CE} overshoot, the V_{CE2} remains higher than the V_{CE1}, but the $V_{CE,AbsDiff}$ starts to decrease as the I_C falls rapidly. A similar V_{CE} diverging feature is observed in the same stage in the simulation of an IGBT gate driving delay shown in Figure 3.15. As the I_C falls, the electric field gradient in the depletion region decreases due to the decrease in the hole carrier profile under the high electric field in the depletion region which is related to the I_C. This reduces the difference in the integral of the electric field over the depletion region, and hence the reduction in the $V_{CE,AbsDiff}$.

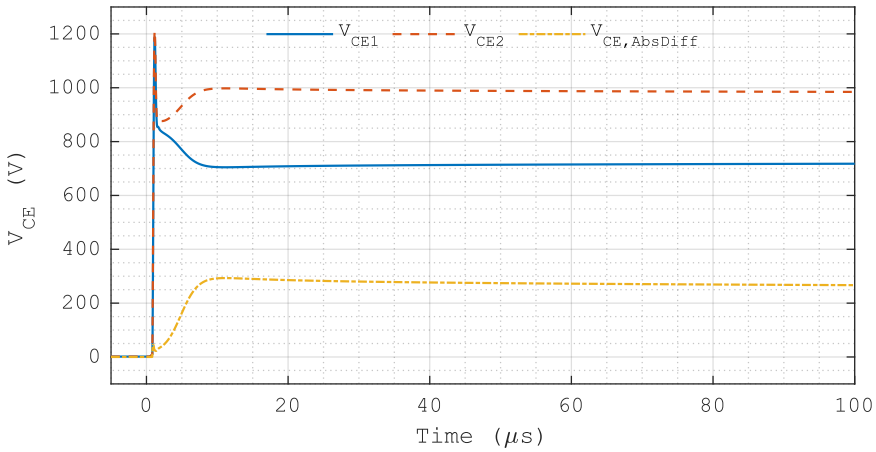


Figure 3.26: Turn-off of two IGBTs in series with the gate resistance for the $IGBT_1$ increased by 1%.

In the tail time, the $V_{CE,AbsDiff}$ starts to increase again as the lead of the V_{CE2} over the V_{CE1} increases. In terms of magnitude, the main V_{CE} divergence arises in the tail time over a long period. The maximum V_{CE} divergence of 293.09 V is reached at 11.138 µs, where the intrinsic leakage current based on the carrier generation in the depletion region prevails over the hole diffusion current in the undepleted part of the N bulk towards the depletion region.

Figure 3.26 shows the V_{CE} in the full 100 µs of the turn-off and the off-state. After peaks at 11.138 µs, the $V_{CE,AbsDiff}$ starts to decrease gradually. This V_{CE} converging process is considerably slower than the V_{CE} diverging process in the tail time. The V_{CE2} remains above the V_{CE1} in the entire turn-off and off-state in this simulation.

In both the fast V_{CE}-I_C transient and the tail time in this IGBT turn-off simulation, the simulation results agree with the theoretical results of the V_{CE} divergence caused by a higher gate resistance for an IGBT discussed in the case 3) in section 3.3.4.

3.5.4 $IGBT_1$ with a Higher Gate Oxide Thickness

Figure 3.27 shows the turn-off simulation of two IGBTs in series with the gate oxide thickness of the $IGBT_1$ increased by 1%. The higher gate oxide thickness leads to a weaker MOS inversion layer and a slightly lower excess carrier profile in the on-state, as well as early MOS channel cut-off in the turn-off. Therefore, according to section 3.3.4, the V_{CE} divergence caused by a higher gate oxide thickness of an IGBT can be considered as a combination of the scenario of a lower P emitter doping profile, the opposite of the situation in section 3.5.2, and the scenario of a timing lead in gate driving, the opposite of the situation in section 3.5.1. Both these scenarios result in higher V_{CE} sharing in the fast V_{CE}-I_C transient and the following tail time. In this case, the $V_{CE,AbsDiff}$ is defined as ($V_{CE1} - V_{CE2}$) and reaches its maximum of 400.12 V at 11.250 µs before starts to decrease slowly. To reveal more V_{CE} diverging details, the first 15 µs of the turn-off is shown in Figure 3.27. The difference in V_{GE} is very small on this time scale. No significant difference in I_C is observed.

After the initial gate discharging period from 0 µs to approx. 0.8 µs, the V_{CE1} starts to increase ahead of the V_{CE2}. Due to the timing lead of the $IGBT_1$ in MOS channel cut-off, the $V_{CE,AbsDiff}$ has a rapid increase at first but remains small while the total V_{CE} rises to the V_{DC}. During the V_{CE} overshoot, the V_{CE1} remains higher than the V_{CE2}, but the $V_{CE,AbsDiff}$ starts to

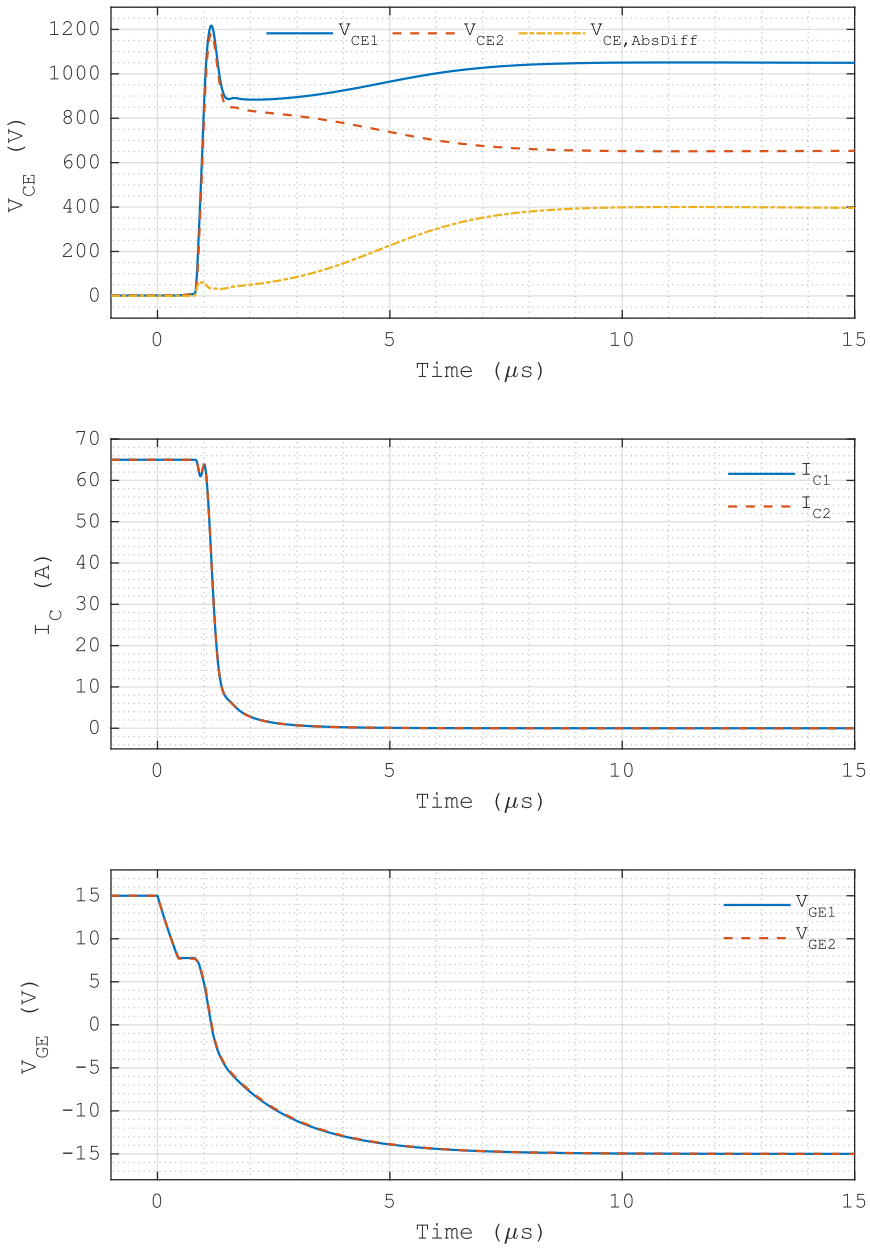


Figure 3.27: Turn-off of two IGBTs in series with the gate oxide thickness of the $IGBT_1$ increased by 1%.

decrease as the I_C falls rapidly. A similar V_{CE} diverging feature is observed in the simulation of an IGBT gate driving delay shown in Figure 3.15. As the I_C falls, the electric field gradient in the depletion region decreases due to the decrease in the hole carrier profile under the high electric field in the depletion region which is related to the I_C. This reduces the difference in the integral of the electric field over the depletion region, and hence the reduction in the $V_{CE,AbsDiff}$.

In the tail time, the $V_{CE,AbsDiff}$ starts to increase again as the lead of the V_{CE1} over the V_{CE2} increases. In terms of magnitude, the main V_{CE} divergence arises in the tail time over a long period. The maximum V_{CE} divergence of 400.12 V is reached at 11.250 µs, where the intrinsic leakage current based on the carrier generation in the depletion region prevails over the hole diffusion current in the undepleted part of the N bulk towards the depletion region.

Figure 3.28 shows the V_{CE} in the full 100 µs of the turn-off and the off-state. After peaks at 11.250 µs, the $V_{CE,AbsDiff}$ starts to decrease gradually. This V_{CE} converging process is

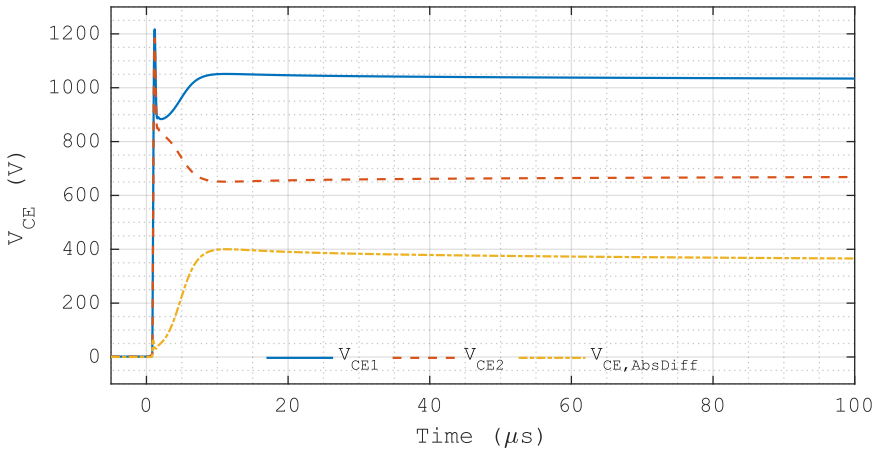


Figure 3.28: Turn-off of two IGBTs in series with the gate oxide thickness of the $IGBT_1$ increased by 1%.

considerably slower than the V_{CE} diverging process in the tail time. The V_{CE1} remains above the V_{CE2} in the entire turn-off and off-state in this simulation.

In both the fast V_{CE}-I_C transient and the tail time in this IGBT turn-off simulation, the simulation results agree with the theoretical results of the V_{CE} divergence caused by a higher gate oxide thickness of an IGBT discussed in case 4) in section 3.3.4.

3.5.5 $IGBT_1$ with a Higher N buffer Doping Profile

Figure 3.29 shows the turn-off simulation of two IGBTs in series with the N buffer doping profile of the $IGBT_1$ increased by 5% in concentration. The higher N buffer doping profile leads to a lower excess carrier profile in the on-state, although the reduction is very limited as the N buffer in a modern FS IGBT is normally designed to be under high-level injection in a typical on-state. Therefore, according to section 3.3.4, the V_{CE} divergence caused by a higher N buffer doping profile of an IGBT can be considered as a variant of the scenario of a lower P emitter doping profile, the opposite of the situation in section 3.5.2, with higher carrier recombination in the N buffer of a higher doping profile in the tail time. This scenario results in higher V_{CE} sharing in the fast V_{CE}-I_C transient and the following tail time. In this case, the $V_{CE,AbsDiff}$ is defined as ($V_{CE1} - V_{CE2}$) and reaches its maximum of 101.54 V at 11.250 µs before starts to decrease slowly. To reveal more V_{CE} diverging details, the first 15 µs of the turn-off is shown in Figure 3.29. No significant difference in the I_C or the V_{GE} is observed.

After the initial gate discharging period from 0 µs to approx. 0.8 µs, the V_{CE1} and the V_{CE2} both start to increase rapidly. During the fast V_{CE}-I_C transient, the V_{CE1} only has a slight lead over the V_{CE2} due to the slightly lower excess carrier profile in the $IGBT_1$ caused by its higher N buffer doping profile. The $V_{CE,AbsDiff}$ first increases slowly, and during the V_{CE} overshoot the increase in the $V_{CE,AbsDiff}$ moderates as the I_C falls rapidly. The $V_{CE,AbsDiff}$ remains very small during the fast V_{CE}-I_C transient. In the tail time, as the lead of the V_{CE1} over the V_{CE2} increases, the $V_{CE,AbsDiff}$ continues to increase and reaches its maximum of 101.54 V at 11.250 µs.

Figure 3.30 shows the V_{CE} in the full 100 µs of the turn-off and the off-state. After peaks at 11.250 µs, the $V_{CE,AbsDiff}$ starts to decreases gradually. This V_{CE} converging process is considerably slower than the V_{CE} diverging process in the tail time. The V_{CE1} remains above the V_{CE2} in the entire turn-off and off-state in this simulation.

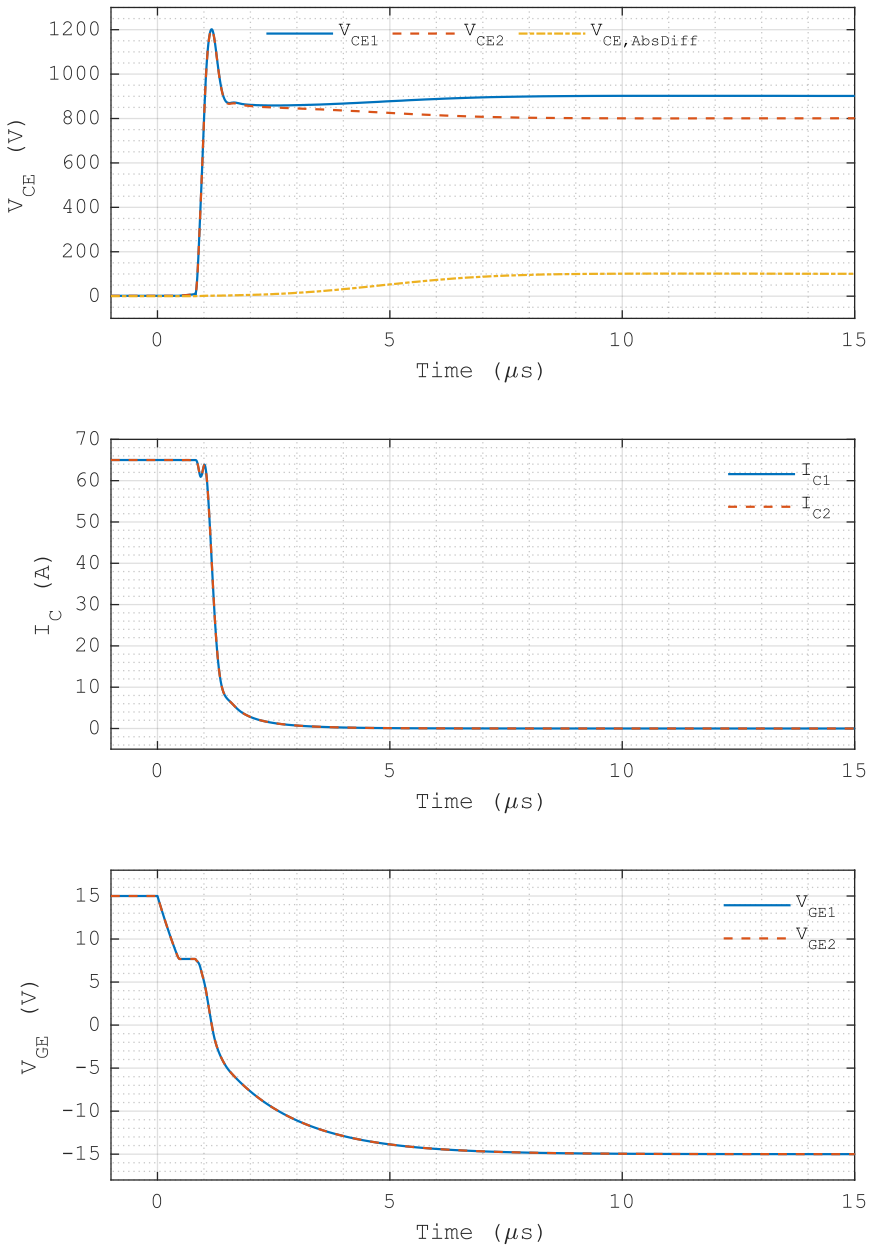


Figure 3.29: Turn-off of two IGBTs in series with the N-buffer doping conc. in the $IGBT_1$ increased by 5%.

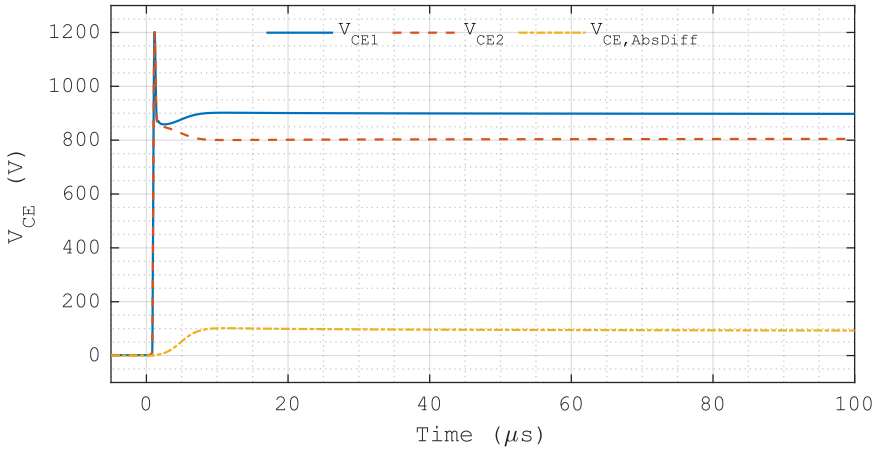


Figure 3.30: Turn-off of two IGBTs in series with the N-buffer doping conc. in the $IGBT_1$ increased by 5%.

In both the fast V_{CE}-I_C transient and the tail time in this IGBT turn-off simulation, the simulation results agree with the theoretical results of the V_{CE} divergence caused by a higher N buffer doping profile of an IGBT discussed in the case 5) in section 3.3.4.

3.5.6 IGBT$_1$ with Longer Carrier Lifetimes

Figure 3.31 shows the turn-off simulation of two IGBTs in series with the low-level carrier lifetimes of both electrons and holes in the IGBT$_1$ increased by 5%. The longer carrier lifetimes lead to a higher excess carrier profile in the on-state. Therefore, according to section 3.3.4, the V_{CE} divergence caused by longer carrier lifetimes of an IGBT can be considered as a variant of the scenario of a higher P emitter doping profile in section 3.5.2, with reduced carrier recombination in the tail time. This scenario results in lower V_{CE} sharing in the fast V_{CE}-I_C transient and the following tail time. In this case, the $V_{CE,AbsDiff}$ is defined as ($V_{CE2} - V_{CE1}$) and reaches its maximum of 127.83 V at 11.250 µs before starts to decrease slowly. To reveal more V_{CE} diverging details, the first 15 µs of the turn-off is shown in Figure 3.29. No significant difference in the I_C or the V_{GE} is observed.

After the initial gate discharging period from 0 µs to approx. 0.8 µs, the V_{CE1} and the V_{CE2} both start to increase rapidly. During the fast V_{CE}-I_C transient, the V_{CE2} only has a slight lead

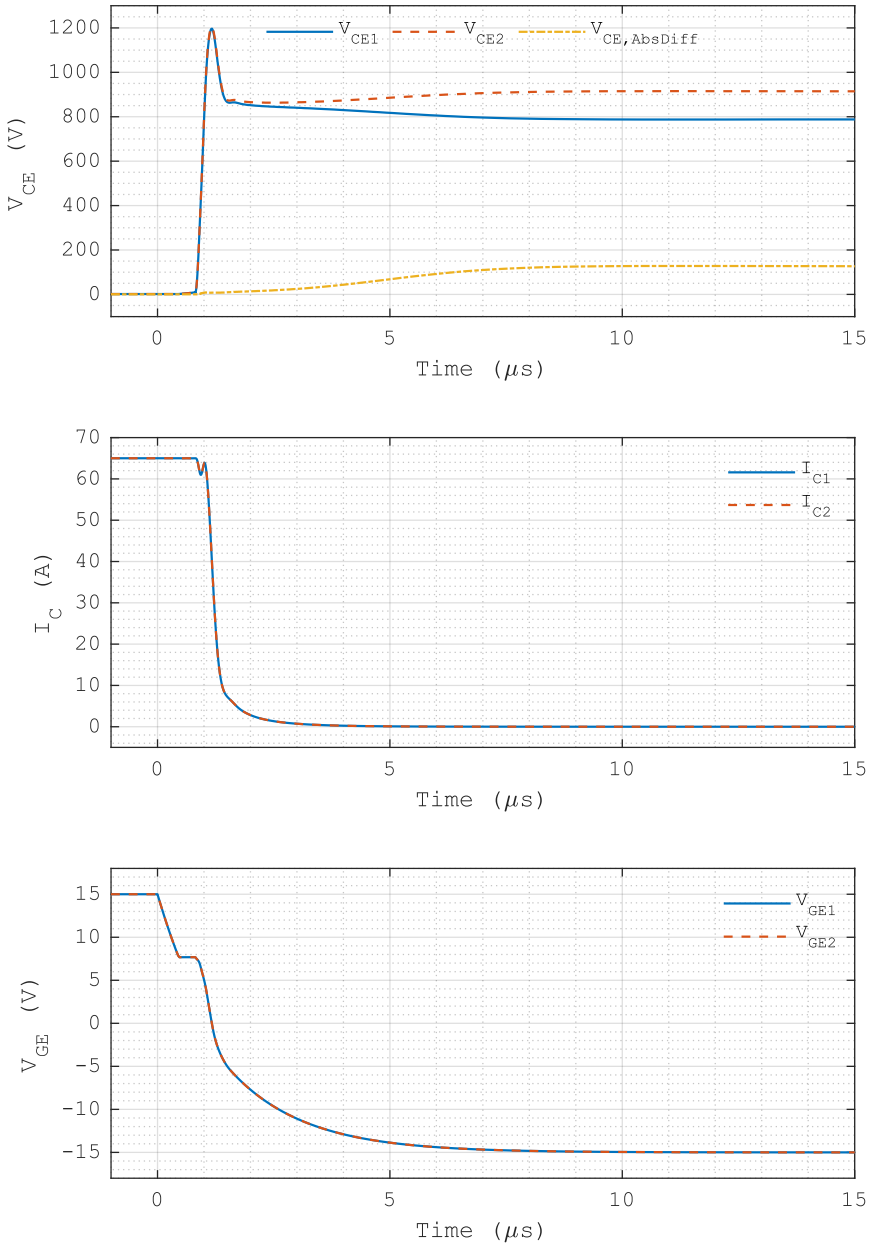


Figure 3.31: Turn-off of two IGBTs in series with the carrier lifetimes in the IGBT$_1$ increased by 5%.

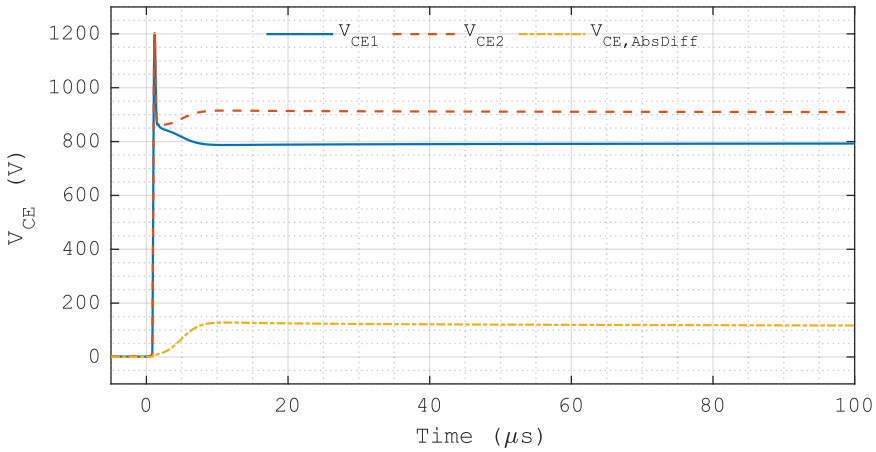


Figure 3.32: Turn-off of two IGBTs in series with the carrier lifetimes in the $IGBT_1$ increased by 5%.

over the V_{CE1} due to the higher excess carrier profile in the $IGBT_1$ caused by its longer carrier lifetimes. The $V_{CE,AbsDiff}$ first increases slowly, and during the V_{CE} overshoot the increase in the $V_{CE,AbsDiff}$ moderates as the I_C falls rapidly. The $V_{CE,AbsDiff}$ remains very small during the fast V_{CE}-I_C transient. In the tail time, as the lead of the V_{CE2} over the V_{CE1} increases, the $V_{CE,AbsDiff}$ continues to increase and reaches its maximum of 127.83 V at 11.250 µs.

Figure 3.32 shows the V_{CE} in the full 100 µs of the turn-off and the off-state. After peaks at 11.250 µs, the $V_{CE,AbsDiff}$ starts to decreases gradually. This V_{CE} converging process is considerably slower than the V_{CE} diverging process in the tail time. The V_{CE2} remains above the V_{CE1} in the entire turn-off and off-state in this simulation.

In both the fast V_{CE}-I_C transient and the tail time in this IGBT turn-off simulation, the simulation results agree with the theoretical results of the V_{CE} divergence caused by longer carrier lifetimes of an IGBT discussed in the case 6) in section 3.3.4.

3.5.7 $IGBT_1$ with a Higher Temperature

Figure 3.33 shows the turn-off simulation of two IGBTs in series with the thermal boundary temperature for the $IGBT_1$ increased by 5 K from that for the $IGBT_2$. The Silvaco ATLAS MixedMode used for the simulations merges all the input ATLAS devices, e.g. the IGBTs in series here, into a large ATLAS device internally for simulation. This mechanism does not support using the `MODELS` statement to apply different temperatures to individual input ATLAS devices. The only method found to apply such different temperatures is via assigning different values to the thermal boundary temperature `EXT.TEMPER` in the `THERMCONTACT` statement. Here a thermal boundary temperature of 305 K is applied to the $IGBT_1$ while the thermal boundary temperature for the $IGBT_2$ is kept at 300 K. Such a simulation setup is also more realistic. To reveal more V_{CE} diverging details, the first 15 µs of the turn-off is shown in Figure 3.33. The difference in V_{GE} is very small on this time scale. No significant difference in I_C is observed.

As discussed in section 3.3.4, a temperature difference can have mixed effects on the turn-off V_{CE} sharing. The simulation result shown in Figure 3.33 presents such a case. After the initial gate discharging period from 0 µs to approx. 0.8 µs, the V_{CE1} and the V_{CE2} both start to increase rapidly. The higher temperature of the $IGBT_1$ leads to a higher excess carrier profile in the on-state and a longer initial turn-off delay, causing the V_{CE1} to be lower at first. In this case, the

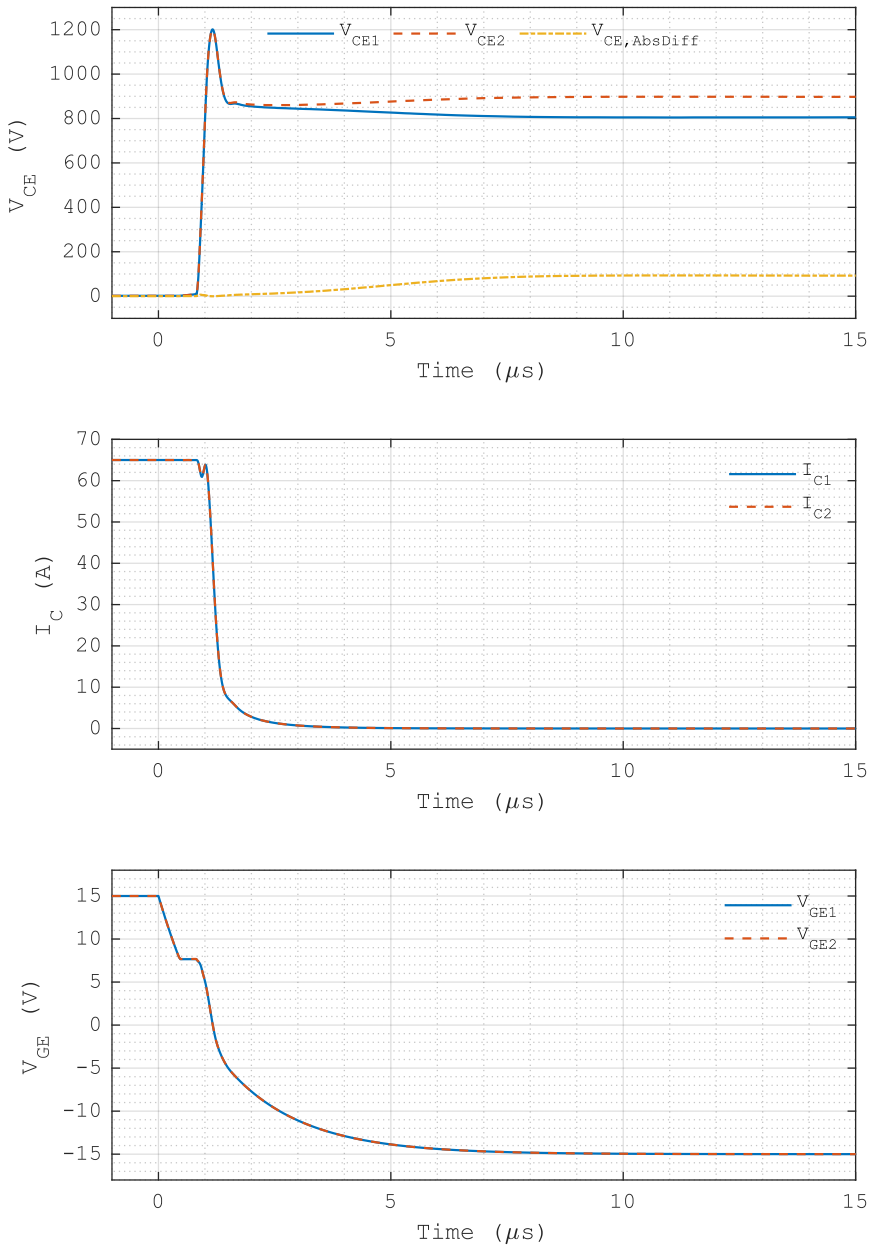


Figure 3.33: Turn-off of two IGBTs in series with the thermal boundary temperature for the $IGBT_1$ increased by 5 K.

$V_{CE,AbsDiff}$ is defined as ($V_{CE2} - V_{CE1}$) and a small increase in the $V_{CE,AbsDiff}$ is first observed at the beginning of the fast V_{CE}-I_C transient.

As discussed in section 3.3.4, at a higher temperature, due to reduced carrier mobilities and saturation drift velocities, the transport of holes from the MOS gate side CSR boundary into the depletion region as well as the hole carrier profile and the electric field gradient in the depletion region all increase. In the $IGBT_1$, as the V_{CE} rises and the saturation velocity of holes in the depletion region is reached, in this temperature range and under the operating conditions here, these related changes start to offset the opposite effects of the higher excess carrier profile at the higher temperature and give rise to a higher dV_{CE}/dt rate. In Figure 3.33, as discussed in the minority case with mixed V_{CE} diverging features in the fast V_{CE}-I_C transient in section 3.3.4, the $V_{CE,AbsDiff}$ decreases to near zero as the V_{CE} rises into the overshoot. When the I_C falls to approx. 40 A during the V_{CE} overshoot, the mechanism related to the higher dV_{CE}/dt rate is reduced to an extent that the $V_{CE,AbsDiff}$ starts to increase during the rest of the V_{CE} overshoot.

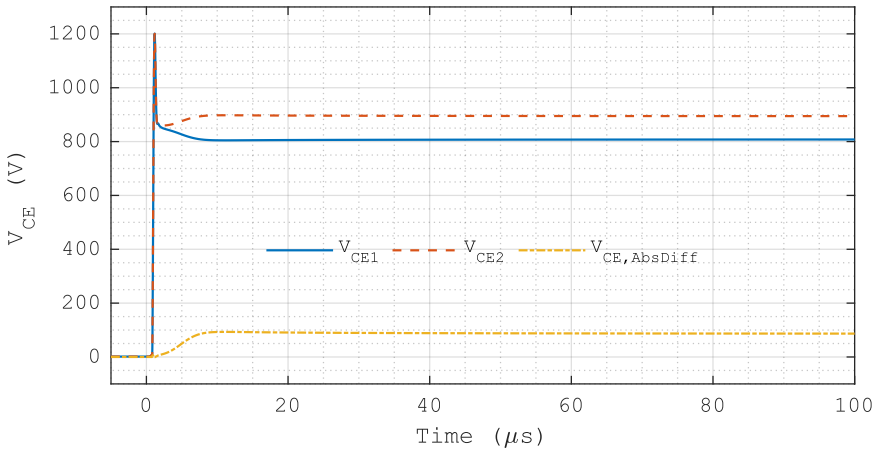


Figure 3.34: Turn-off of two IGBTs in series with the thermal boundary temperature for the $IGBT_1$ increased by 5 K.

In the tail time, the $V_{CE,AbsDiff}$ continues to increase, where the higher hole carrier profile in the undepleted part of the N base of the $IGBT_1$ has a strong influence on the V_{CE} divergence. In the tail time, the V_{CE} divergence caused by a higher temperature in an IGBT can be considered as a variant of the scenario of a higher P emitter doping profile discussed in section 3.5.2. This scenario results in higher V_{CE} sharing in the tail time. In terms of magnitude, the main V_{CE} divergence arises in the tail time over a long period. The maximum V_{CE} divergence of 93.161 V is reached at 11.025 µs, where the intrinsic leakage current based on the carrier generation in the depletion region prevails over the hole diffusion current in the undepleted part of the N base towards the depletion region.

Figure 3.34 shows the V_{CE} in the full 100 µs of the turn-off and the off-state. After peaks at 11.025 µs, the $V_{CE,AbsDiff}$ starts to decrease gradually. This V_{CE} converging process is considerably slower than the V_{CE} diverging process in the tail time. The V_{CE2} remains above the V_{CE1} during the entire tail time and off-state in this simulation.

The V_{CE} divergence caused by a higher temperature in an IGBT depends on the temperature range and the other operating conditions of the IGBTs in series and needs to be examined on a case-by-case basis. The simulation results here agree with the theoretical results of the minority case with mixed V_{CE} diverging features in the fast V_{CE}-I_C transient regarding the V_{CE} divergence caused by a temperature difference discussed in the case 7) in section 3.3.4. Still, in the tail time, the higher hole carrier profile in the undepleted part of the N base of the IGBT with the higher temperature has a strong influence on the V_{CE} divergence, which results in lower V_{CE} sharing.

3.5.8 Summary of the V_{CE} Divergence Results and Sensitivity Analysis

The IGBT turn-off simulations of the individual V_{CE} diverging factors are at V_{DC} = 1700 V and I_{Load} = 65 A for two IGBTs in direct series under an average utilisation of 50% of their V_{CE} and I_C ratings. A summary of the simulation results of the individual V_{CE} diverging factors is presented in Table 3.3. The largest magnitude of ($V_{CE1} - V_{CE2}$) and its relative value to the V_{DC}, ($V_{CE1} - V_{CE2}$)/V_{DC}, are included, as well as the difference in the turn-off losses ($E_{off1} - E_{off2}$) and its relative value to the turn-off losses of the $IGBT_2$, ($E_{off1} - E_{off2}$)/E_{off2}.

Table 3.3: Summary of V_{CE} divergence simulations at V_{DC} = 1700 V and I_C = 65 A.

Diverging factor applied to $IGBT_1$	Largest mag. of (V_{CE1}-V_{CE2}) (V)	Largest mag. of (V_{CE1}-V_{CE2})/V_{DC}	Losses diff. (E_{off1}-E_{off2}) (mJ)	Rel. losses diff. (E_{off1}-E_{off2})/E_{off2}
+10 ns gate driving delay	-438.06	-25.768%	-1.6360	-6.6354%
+5% P emitter doping conc.	-359.00	-21.118%	-0.47832	-1.9723%
+1% gate resistance	-293.09	-17.241%	-1.0820	-4.4383%
+1% gate oxide thickness	+400.12	+23.537%	+1.4858	+6.4348%
+5% N buffer doping conc.	+101.54	+5.9729%	+0.079961	+0.33659%
+5% low-level carrier lifetimes	-127.83	-7.5195%	-0.23953	-0.99714%
+5 K thermal boundary temp.	-93.161	-5.4801%	-0.11994	-0.50173%

Regarding the V_{CE} divergence, in terms of magnitude the main V_{CE} divergence arises in the tail time in all the simulations of the individual V_{CE} diverging factors here, among which the 10 ns IGBT gate driving delay, the +5% higher P emitter doping profile, the +1% gate resistance, and the +1% gate oxide thickness result in considerably higher V_{CE} divergence. Regarding the IGBT parameter variations, the turn-off V_{CE} divergence is more sensitive to a variation in the gate resistance or the gate oxide thickness. The individually V_{CE} divergence caused by the other V_{CE} diverging factors is smaller, but the concurrent V_{CE} diverging effects of certain combinations of those V_{CE} diverging factors can still cause high V_{CE} divergence.

Regarding the difference in turn-off losses, those four cases with considerably higher V_{CE} divergence also result in higher differences in turn-off losses. However, large V_{CE} divergence is not always related to a large difference in turn-off losses. The cases of the 10 ns gate driving delay, the +1% gate resistance, and the +1% gate oxide thickness that feature a significant delay in the MOS channel cut-off have considerably higher differences in the turn-off losses compared with that in the case of the +5% higher P emitter doping profile with comparable V_{CE} divergence. This is because turn-off losses are produced mainly in the fast V_{CE}-I_C transient, where a significant delay in the MOS channel cut-off causes V_{CE} divergence which directly gives rise to a large difference in turn-off losses.

Regarding the sensitivity of the V_{CE} divergence to the basic V_{CE} diverging factors, Figure 3.35 shows the simulations of IGBT gate driving delays applied to the $IGBT_1$ of 20% (2 ns), 50% (5 ns), and 80% (8 ns) of the original 10 ns delay as the reference indicated by "Ref". The basic V_{CE} diverging features are similar at the scaled IGBT gate driving delays and therefore will not be repeated here. Figure 3.36 shows the largest V_{CE} divergences and the relative turn-off loss differences at the scaled IGBT gate driving delays. The largest V_{CE} divergences in the range of the scaled IGBT gate driving delays shown in Figure 3.36 (a) can be fitted as:

$$V_{CE,MaxDiv} = 677.8\{\exp(0.04972 t_{GD}) - 1\} \qquad \text{Equation 3.2}$$

where $V_{CE,MaxDiv}$ is the largest V_{CE} divergence and t_{GD} is the IGBT gate driving delay. This fit achieves a R^2 of 0.9999 and an adjusted R^2 of 0.9998. As the t_{GD} increases, the resulting difference in the remaining CSR at the beginning of the tail time increases. With such a smaller remaining CSR, in the tail time the recombination of holes in the N buffer has a higher influence on the decreases in the hole carrier profile in the undepleted part of the N base and the hole diffusion current in it towards the depletion region. Consequently, the largest V_{CE} divergence increases superlinearly with the IGBT gate driving delay. As the relative turn-off loss difference is strongly related to the V_{CE} divergence during the fast V_{CE}-I_C transient and therefore the IGBT

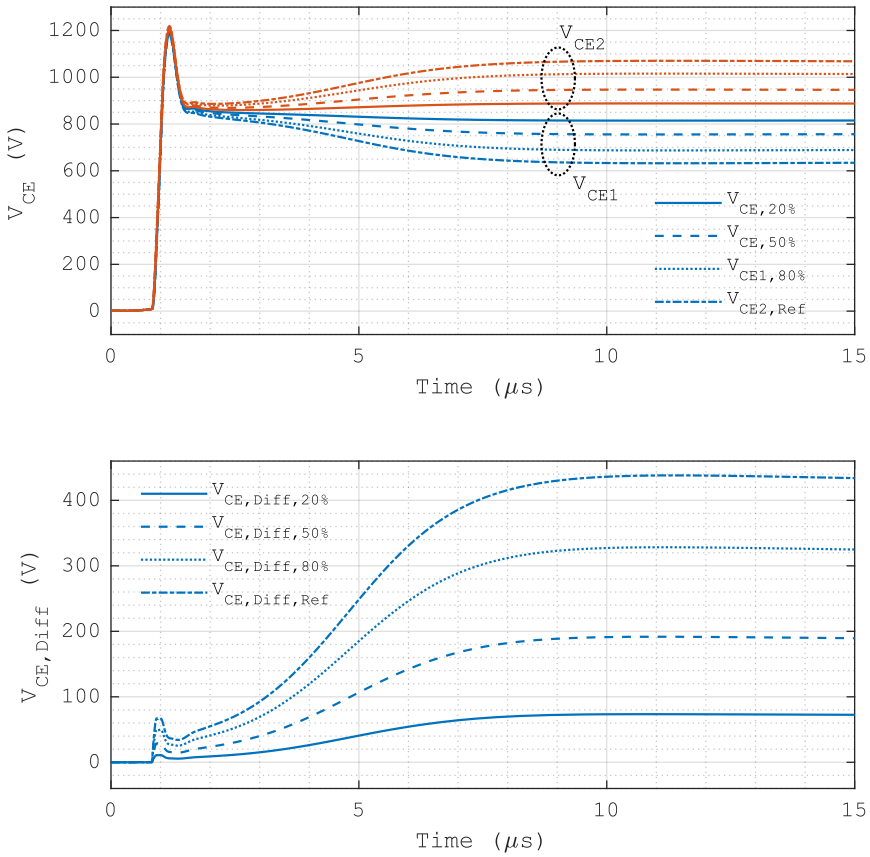


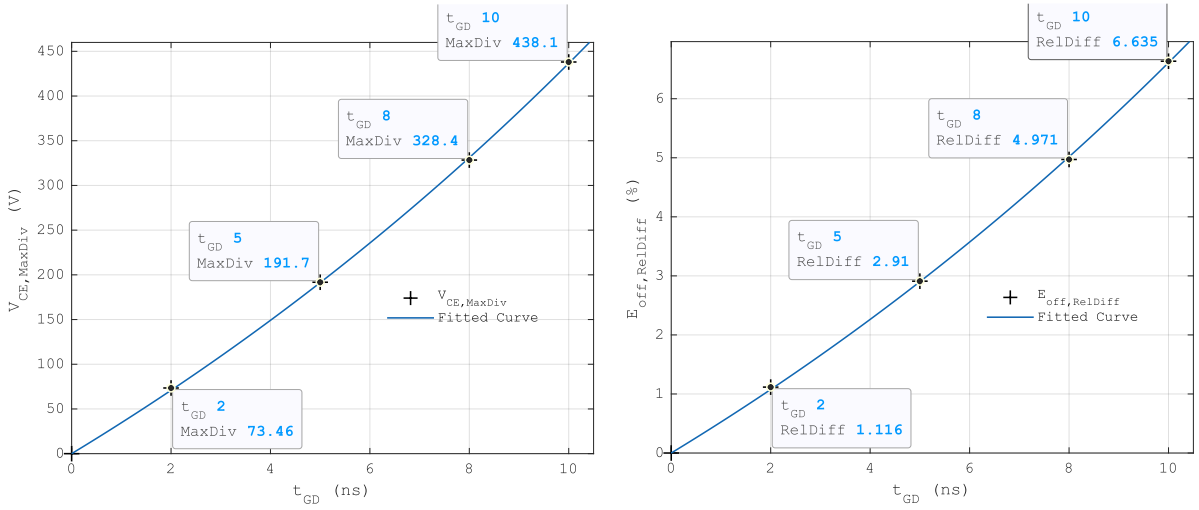
Figure 3.35: Simulations of IGBT gate driving delays of 20%, 50%, and 80% of the original 10 ns delay.

gate driving delay, the relative turn-off loss differences in the range of the scaled IGBT gate driving delays shown in Figure 3.36 (b) can be fitted in the same form of Equation 3.2:

$$E_{off,RelDiff} = 10.41\{\exp(0.04915 t_{GD}) - 1\} \qquad \text{Equation 3.3}$$

where $E_{off,RelDiff}$ is the relative turn-off loss difference. This fit achieves a R^2 of 0.9999 and an adjusted R^2 of 0.9998. The relative turn-off loss difference also increases superlinearly with the IGBT gate driving delay.

Figure 3.37 shows the simulations of increases in the P emitter doping concentration of the $IGBT_1$ of 20% (1%), 50% (2.5%), and 80% (4%) of the original 5% increase as the reference



(a) (b)

Figure 3.36: (a) The largest V_{CE} divergences and (b) the relative turn-off loss differences of the scaled IGBT gate driving delays.

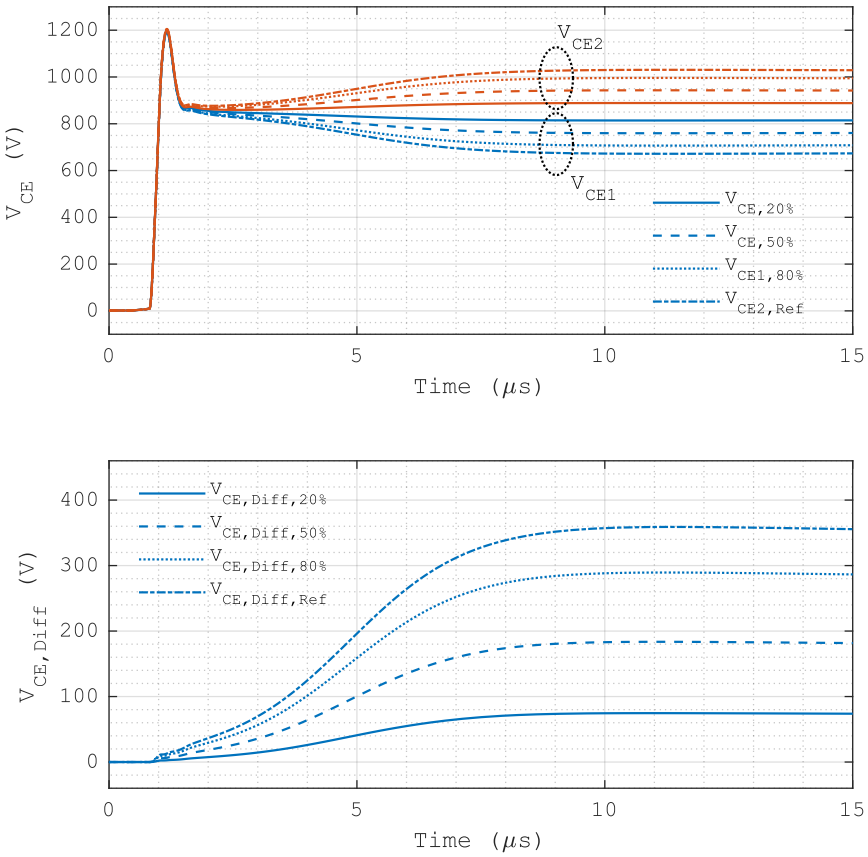
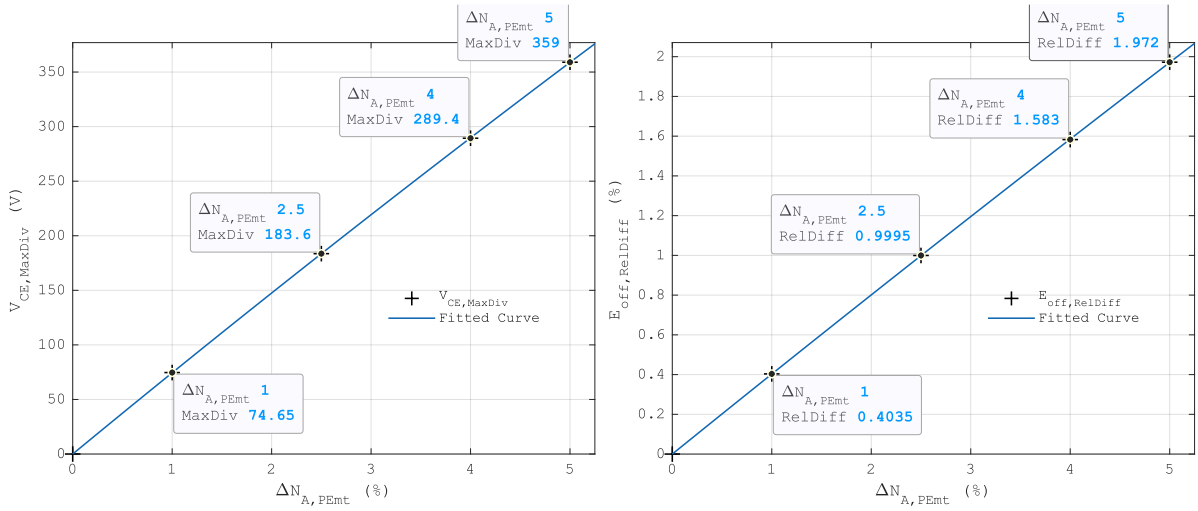


Figure 3.37: Simulations of increases in the P emitter doping concentration of 20%, 50%, and 80% of the original 5% increase.

indicated by "Ref". The basic V_{CE} diverging features are similar at the scaled increases in the P emitter doping concentration and therefore will not be repeated here. Figure 3.38 shows the largest V_{CE} divergences and the relative turn-off loss differences at the scaled increases in the P emitter doping concentration. The largest V_{CE} divergences in the range of the scaled increases in the P emitter doping concentration shown in Figure 3.38 (a) can be fitted as:

$$V_{CE,MaxDiv} = 4081\{1 - \exp(-0.0184\Delta N_{A,PEmt})\} \qquad \text{Equation 3.4}$$

where $\Delta N_{A,PEmt}$ is the increase in the P emitter doping concentration. This fit achieves a R^2 of 0.9999 and an adjusted R^2 of 0.9999. According to the approximations by Equation 1.48 to



(a) (b)

Figure 3.38: (a) The largest V_{CE} divergences and (b) the relative turn-off loss differences of the scaled increases in the P emitter doping concentration.

Equation 1.50 in Chapter 1, as the $\Delta N_{A,PEmt}$ increases, the resulting increase in the on-state excess carrier concentration moderates. Consequently, the largest V_{CE} divergence increases sublinearly with the increase in the P emitter doping concentration. As the relative turn-off loss difference is strongly related to the V_{CE} divergence during the fast V_{CE}-I_C transient, the relative turn-off loss differences in the range of the scaled increases in the P emitter doping concentration shown in Figure 3.38 (b) can be fitted in the same form of Equation 3.4:

$$E_{off,RelDiff} = 38.13\{1 - \exp(-0.01061\Delta N_{A,PEmt})\}. \quad \text{Equation 3.5}$$

This fit achieves a R^2 of 0.9999 and an adjusted R^2 of 0.9999. The relative turn-off loss difference also increases sublinearly with the increase in the P emitter doping concentration. Equation 3.2 to Equation 3.5 are only applicable to the respective basic V_{CE} diverging factors of such small degrees. The effects of V_{CE} diverging factors of large degrees are intended for future research.

The IGBT parameter variations and gate driving errors simulated are of small degrees, yet considerable V_{CE} divergences are produced in some of the cases. It is apparent from the above summary that V_{CE} divergences in both the fast V_{CE}-I_C transient and the tail time need to be mitigated. Approaches to mitigating the V_{CE} divergence can be explored from adjustments to IGBT operating conditions and internal parameters, direct feedback control via IGBT gate control, and external feedback control via additional power devices. These approaches will be discussed in the following three chapters.

Chapter 4 Passive Mitigation Methods at IGBT Device Level under Direct Series Connection

4.1 V_{CE} Diverging Features and Passive Mitigation Methods

The focus of this chapter is on passive mitigation methods for the turn-off V_{CE} divergence under direct series connection at IGBT device level via adjustments to operating conditions and internal parameters of the IGBTs. The objective here is to improve the basis of the turn-off V_{CE} sharing rather than the regulation of the V_{CE} sharing. In Chapter 3, seven V_{CE} diverging factors are discussed regarding their effects on the turn-off V_{CE} divergence. The largest magnitude of the V_{CE} divergence relative to the V_{DC}, the difference in turn-off losses relative to that of the $IGBT_2$, and the key features of those V_{CE} diverging factors are summarised in Table 4.1.

Table 4.1: Summary of V_{CE} diverging features from simulations at V_{DC} = 1700 V and I_C = 65 A.

Diverging factor applied to $IGBT_1$	Largest mag. of $(V_{CE1}-V_{CE2})/V_{DC}$	Rel. losses diff. $(E_{off1}-E_{off2})/E_{off2}$	Initial CSR carrier conc.	MOS channel cut-off timing	CSR carrier profile when the turn-off enters the tail time
+10 ns gate driving delay	-25.768%	-6.6354%	Same	Lag	Extended dist. w/ same local conc.
+5% P emitter doping conc.	-21.118%	-1.9723%	Higher	Virtually same	Extended dist. w/ higher local conc.
+1% gate resistance	-17.241%	-4.4383%	Same	Lag	Extended dist. w/ same local conc.
+1% gate oxide thickness	+23.537%	+6.4348%	Lower	Lead	Narrowed dist. w/ lower local conc.
+5% N buffer doping conc.	+5.9729%	+0.33659%	Lower	Virtually same	Narrowed dist. w/ lower local conc.
+5% low-level carrier lifetimes	-7.5195%	-0.99714%	Higher	Virtually same	Extended dist. w/ higher local conc.
+5 K thermal boundary temp.	-5.4801%	-0.50173%	Higher	Lag	Extended dist. w/ higher local conc.

The passive mitigation methods here consider the first four V_{CE} diverging factors summarised in Table 4.1 that cause considerably higher V_{CE} divergence and relative loss differences than those of the other V_{CE} diverging factors. Considering the general V_{CE} diverging processes, the passive mitigation approaches here aim to mitigate, with regard to the IGBTs in series, (1) a few key differences in initial IGBT conditions, (2) the conversion of these differences in the initial IGBT conditions into the V_{CE} divergence and differences in the carrier profile of the remaining CSR in the fast V_{CE}-I_C transient, and (3) the conversion of the latter differences in the CSR carrier profile into V_{CE} divergence in the tail time.

First, the dependence of the on-state excess carrier concentration on the P emitter doping concentration and the gate oxide thickness is considered. According to the approximations by Equation 1.48 to Equation 1.50 in Chapter 1, the sensitivity of the on-state excess carrier concentration to a variation in the P emitter doping concentration can be moderated by reducing the on-state current density, reducing the carrier lifetimes, or increasing the P emitter doping concentration. Regarding variation in the gate oxide thickness, since in a typical IGBT on-state the MOS channel operates in its linear region, its influence on the on-state carrier concentration is minor and will not be discussed further.

A timing difference in the MOS channel cut-off causes a difference in the depletion progress during the fast V_{CE}-I_C transient, which leads to V_{CE} divergence in the fast V_{CE}-I_C transient

and the tail time. This difference in the depletion progress can be moderated by reducing the J_C according to the approximations by Equation 1.48 to Equation 1.50 in Chapter 1, or by increasing the P emitter doping concentration. However, increasing carrier lifetimes, although can increase the on-state excess carrier concentration, has a stronger opposite effect of enhancing the hole diffusion in the undepleted part of the N base towards the depletion region in the tail time. In typical use, this amplifies the V_{CE} divergence, and hence the opposite approach of reducing carrier lifetimes is useful. Another method to reduce the influence of a difference in the depletion progress on the V_{CE} divergence is increasing the thickness of the N-drift region, which in general reduces the proportion of the depletion difference to the remaining CSR. An additional method based on this principle is reducing the average off-state V_{CE} utilisation of the IGBTs in series, which in general results in a reduced depletion region and an extended remaining CSR. Therefore, the proportion of the depletion difference to the remaining CSR is reduced.

Regarding a timing difference itself in the MOS channel cut-off, if the timing difference is produced in the initial gate discharging process, e.g. in the scenarios of a gate resistance variation or a gate oxide thickness variation, it is useful to reduce the gate resistance to accelerate the initial gate discharging, so that the absolute timing difference in the MOS channel cut-off is reduced. Hence, the V_{CE} divergence in that type of diverging scenarios is reduced. However, that effect of reducing the gate resistance is insignificant in the case of a direct delay in the gate drive output, e.g. caused by a jitter in the control signal acquisition, which results in essentially a shift in time of the same gate discharging process.

Differences in the hole carrier profile in the undepleted part of the N base when the turn-off enters the tail time cause a difference in the hole diffusion current in the undepleted part of the N base towards the depletion region in the tail time which leads to V_{CE} divergence. To reduce the influence of a difference in that hole diffusion current on the V_{CE} divergence, an approach is to accelerate the recombination of the holes in the undepleted part of the N base by reducing carrier lifetimes. Hence, the difference in the hole carrier profile and its influence on the V_{CE} divergence is reduced by a shortened tail time. Another method is to reduce the J_C. Hence, the hole concentration in the undepleted part of the N base and the concerned hole diffusion current in the tail time are reduced, so are their difference and its influence on the V_{CE} divergence.

An additional method is to increase the thickness of the N-drift region, which in general results in an extended remaining CSR when the turn-off enters the tail time. Such an extended initial remaining CSR can reduce the difference in the hole diffusion current towards the depletion region in the undepleted part of the N base as the difference in the undepleted part of the N base increases in the tail time. This is due to the additional supply of holes from the extended inner section of the undepleted part of the N base. This method moderates the conversion of differences in the hole carrier profile in the undepleted part of the N base into V_{CE} divergence, where Figure 3.19 and Figure 3.24 can be considered as opposite examples. Another method based on the same principle is to reduce the off-state V_{CE} utilisation of the IGBTs in series, which in general reduces the depletion region and results in an extended initial remaining CSR when the turn-off enters the tail time.

These passive mitigation methods affect the trade-offs between the V_{CE} sharing and multiple performance and cost aspects. Nevertheless, these passive mitigation methods and their combinations that are useful for improving the basis of the V_{CE} sharing are worth exploring.

4.2 Simulation Test of the Passive Mitigation Methods

The passive mitigation methods at IGBT device level discussed in section 4.1 are summarised as follows: (1) reducing the collector current density, (2) reducing the carrier lifetimes, (3) increasing the P emitter doping concentration, (4) increasing the N-drift region thickness, (5) reducing the off-state V_{CE} utilisation, and (6) reducing the gate resistance.

These methods are tested in the two basic V_{CE} diverging scenarios summarised in section 3.5: (1) an output delay between the IGBT gate drives, and (2) a variation in the P emitter doping concentration, except for the method of reducing the gate resistance which is designed for and tested in the V_{CE} diverging scenarios of a variation in the gate resistance and a variation in the gate oxide thickness. The implementation of these methods is discussed in their individual subsections. To focus the presentation of the test results on the mitigation of the V_{CE} divergence, in section 4.2 the V_{CE1}, the V_{CE2}, and the $V_{CE,AbsDiff}$ are shown and compared with those in the original results indicated by dashed lines and the subscript "Ref". The results are aligned at the first gate drive turn-off action on the time axis, unless specified otherwise.

4.2.1 Reducing the IGBT Collector Current Density

In this simulation test, the IGBT J_C is reduced by 20%, which is implemented by increasing the IGBT active chip area by 25% for both the IGBTs. The on-state J_C is reduced to 52 A/cm^2 from the original value of 65 A/cm^2. This implementation is related to the use of IGBT modules of a higher total current rating for the same load current. To match the increase in the IGBT active chip area, the gate resistances for both IGBTs are scaled down by 20%, and the capacitance in the FWD circuit in the CCL is scaled up by 25%. The rest of the IGBT parameters and the circuit parameters remain unchanged.

Figure 4.1 shows the turn-off simulation with the 20% reduced J_C of two IGBTs in series and a 10 ns delay applied to the gate drive output for the IGBT$_1$. Note that the voltage scale of the $V_{CE,Diff}$ axis is different from that of the V_{CE} axis. With the 20% reduced J_C, during the fast V_{CE} rising, a reduction is observed in the dV_{CE}/dt rate and the $V_{CE,AbsDiff}$ is reduced compared with the original result. The V_{CE} diverging feature during the fast V_{CE}-I_C transient remains similar to that in the original result. The $V_{CE,AbsDiff}$ and the original $V_{CE,RefDiff}$ are similar when the turn-off enters the tail time. The $V_{CE,AbsDiff}$ remains below the original $V_{CE,RefDiff}$ during the tail time and the following off-state in the simulation.

In this simulation, the largest V_{CE} divergence is reduced to 406.40 V at 11.038 µs from the original value of 438.06 V at 11.659 µs, a relative reduction of 7.2286% in the largest V_{CE} divergence. The time of the largest V_{CE} divergence becomes earlier with the reduced J_C due to the reduced hole carrier profile and the reduced hole diffusion current towards the depletion region in the undepleted part of the N base. The difference in the turn-off losses relative to the E_{off2} is reduced to 6.2451% from the original value of 6.6354%, a relative reduction of 5.8817%.

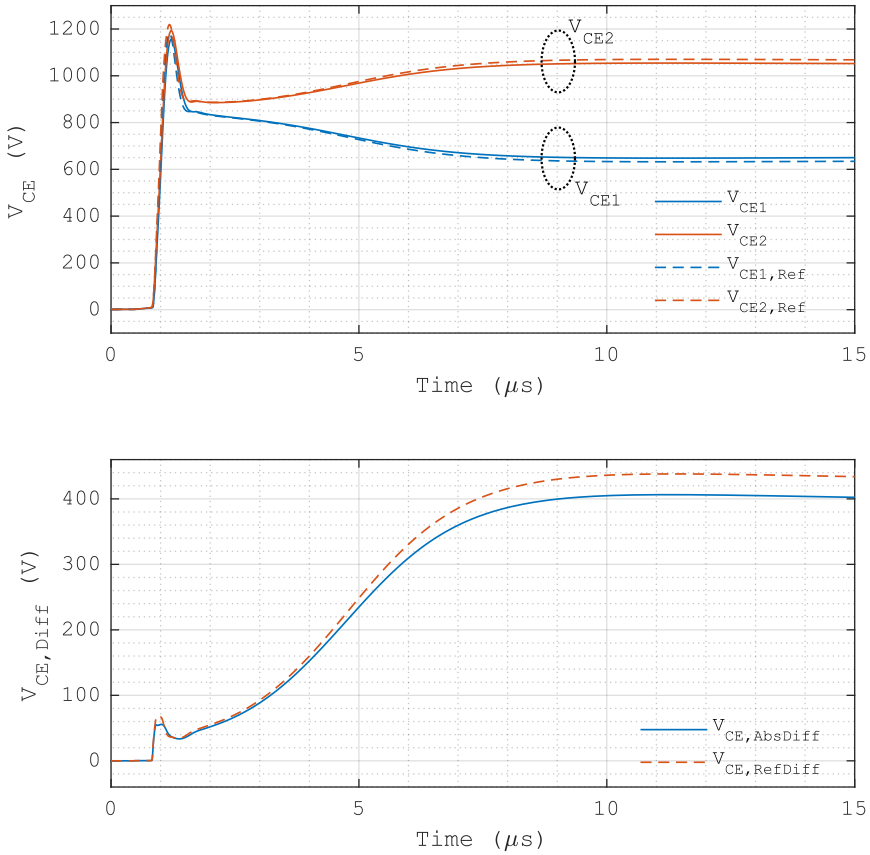


Figure 4.1: Turn-off of two IGBTs in series with the 20% reduced J_C with the gate drive output for the $IGBT_1$ delayed by 10 ns.

Figure 4.2 shows the turn-off simulation with the 20% reduced J_C of two IGBTs in series and a 5% increase in the P emitter doping concentration of the $IGBT_1$. With the 20% reduced J_C, during the fast V_{CE}-I_C transient, a reduction is observed in the dV_{CE}/dt rate and the $V_{CE,AbsDiff}$ is similar compared with the original result. The V_{CE} diverging feature during the fast V_{CE}-I_C transient remains similar to that of the original result. Early in the tail time until approx. 5.8 µs, the $V_{CE,AbsDiff}$ is slightly above the original $V_{CE,RefDiff}$ but the difference is very small. After approx. 5.8 µs, the $V_{CE,AbsDiff}$ becomes lower than the original $V_{CE,RefDiff}$ due to the reduced hole carrier profile and the reduced hole diffusion current towards the depletion region in the undepleted part of the N base.

In this simulation, the largest V_{CE} divergence is reduced to 353.16 V at 10.978 µs from the original value of 359.00 V at 11.250 µs, a relative reduction of 1.6269% in the largest V_{CE} divergence. The time when the largest V_{CE} divergence is reached also becomes earlier with the reduced J_C due to the reduced hole carrier profile and the reduced hole diffusion current towards the depletion region in the undepleted part of the N base. However, due to the reduction in the dV_{CE}/dt rate during the fast V_{CE} rising, the difference in the turn-off losses relative to the E_{off2} is increased to 2.1602% from the original value of 1.9723%, a relative increase of 9.5292%.

At a given load current, reducing the J_C by increasing the total IGBT active chip area is straightforward. The mitigation effect of reducing the J_C on the V_{CE} divergence caused by a delay in the MOS channel cut-off is significant with a reduction in the turn-off losses. However, the mitigation effect of reducing the J_C on the V_{CE} divergence caused by a variation in the on-state excess carrier profile is not ideal, as the relative difference in the turn-off losses increases.

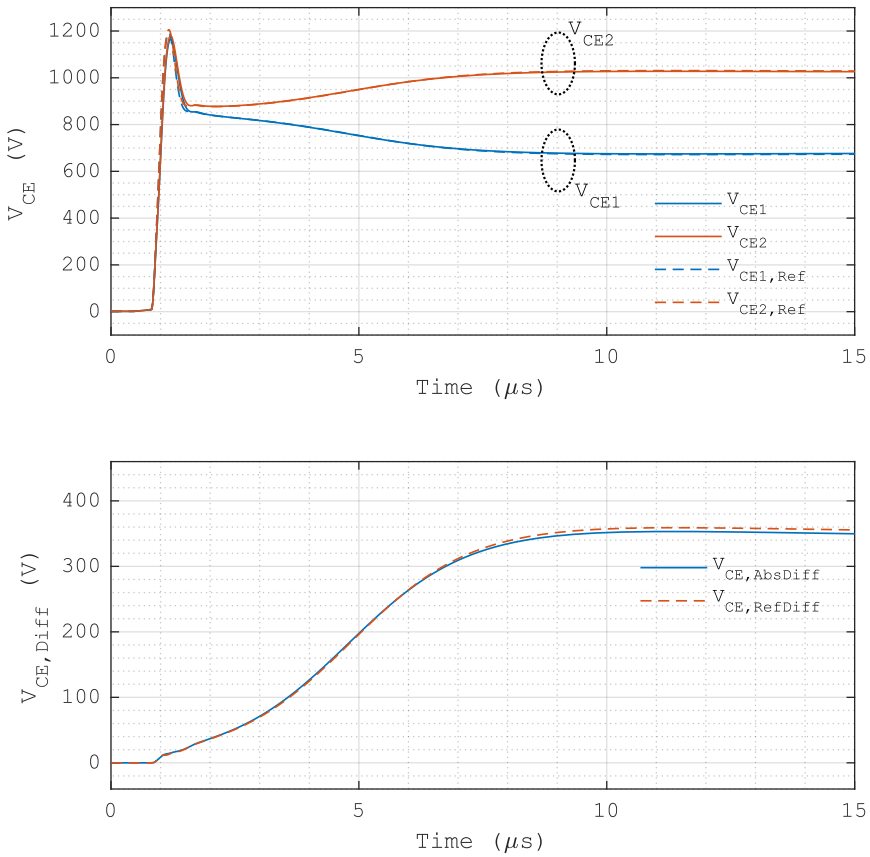


Figure 4.2: Turn-off of two IGBTs in series with the 20% reduced J_C with the P emitter doping concentration of the $IGBT_1$ increased by 5%.

Also, the lower J_C reduces the dV_{CE}/dt rate during the fast V_{CE} rising which causes higher turn-off losses as a side effect.

4.2.2 Reducing the IGBT Carrier Lifetimes

In this simulation test, reducing the carrier lifetimes is implemented by reducing the basic low-level carrier lifetimes of electrons and holes, τ_{n0} and τ_{p0}, respectively, in the SRH and the Auger recombination models for both the IGBTs. The τ_{n0} and the τ_{p0} are both reduced by 20% to 6.0 µs and 2.0 µs from the original values of 7.5 µs and 2.5 µs, respectively. The rest of the IGBT parameters and the circuit parameters remain unchanged.

Figure 4.3 shows the turn-off simulation with the 20% reduced τ_{n0} and τ_{p0} of two IGBTs in series and a 10 ns delay applied to the gate drive output for the $IGBT_1$. With the 20% reduced τ_{n0} and τ_{p0}, the V_{CE} diverging feature during the fast V_{CE}-I_C transient remains similar to that of the original result. During the fast V_{CE} rising, slight increases are observed in the dV_{CE}/dt rate and the $V_{CE,AbsDiff}$ due to the reductions in the carrier lifetimes leading to a reduced excess carrier concentration and a shorter V_{CE} rising time. The $V_{CE,AbsDiff}$ and the $V_{CE,RefDiff}$ are similar when the turn-off enters the tail time. In the tail time, from approx. 4 µs, the $V_{CE,AbsDiff}$ starts to diverge from the original $V_{CE,RefDiff}$ and remains below the $V_{CE,RefDiff}$ during the rest of the tail time and the following off-state in the simulation.

In this simulation, the largest V_{CE} divergence is reduced to 397.75 V at 10.157 µs from the original value of 438.06 V at 11.659 µs, a relative reduction of 9.2027% in the largest V_{CE} divergence, and the time when the largest V_{CE} divergence is reached becomes earlier. These

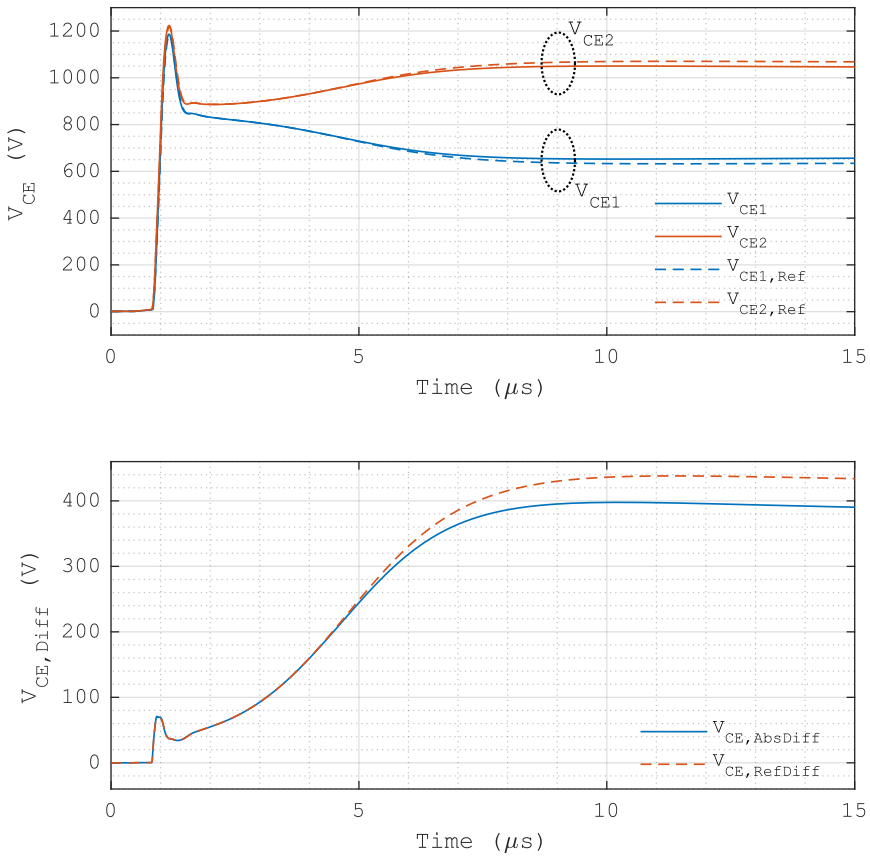


Figure 4.3: Turn-off of two IGBTs in series with the 20% reduced τ_{n0} and τ_{p0}, with the gate drive output for the $IGBT_1$ delayed by 10 ns.

changes are due to the enhanced carrier recombination by the reduced τ_{n0} and τ_{p0} shortening the tail time and reducing the hole diffusion current in the undepleted part of the N base towards the depletion region. The difference in the turn-off losses relative to the E_{off2} is increased slightly to 6.6988% from the original value of 6.6354%, a small relative increase of 0.95558%. This is due to the slightly increased $V_{CE,AbsDiff}$ and the slightly shorter V_{CE} rising time during the fast V_{CE} rising.

Figure 4.4 shows the turn-off simulation with the 20% reduced τ_{n0} and τ_{p0} of two IGBTs in series and a 5% increase in the P emitter doping concentration of the $IGBT_1$. With the 20% reduced τ_{n0} and τ_{p0}, the V_{CE} diverging feature during the fast V_{CE}-I_C transient remains similar to that of the original result. The results are similar during the fast V_{CE} rising, with a slight increase in the dV_{CE}/dt rate due to the reductions in the carrier lifetimes leading to a reduced excess carrier concentration. During the fast V_{CE}-I_C transient, the $V_{CE,AbsDiff}$ and the original $V_{CE,RefDiff}$ are very similar. In the tail time, the $V_{CE,AbsDiff}$ gradually diverges from the original $V_{CE,RefDiff}$ and remains below the $V_{CE,RefDiff}$ during the tail time and the following off-state in the simulation.

In this simulation, the largest V_{CE} divergence is reduced to 319.17 V at 10.073 µs from the original value of 359.00 V at 11.250 µs, a relative reduction of 11.095% in the largest V_{CE} divergence, and the time when the largest V_{CE} divergence is reached becomes earlier. These changes are also due to the enhanced carrier recombination by the reduced τ_{n0} and τ_{p0} shortening the tail time and reducing the hole diffusion current in the undepleted part of the N base towards the depletion region. As the difference in the excess carrier concentration caused by the variation in the P emitter doping concentration decreases due to the reduced τ_{n0} and τ_{p0}, the difference

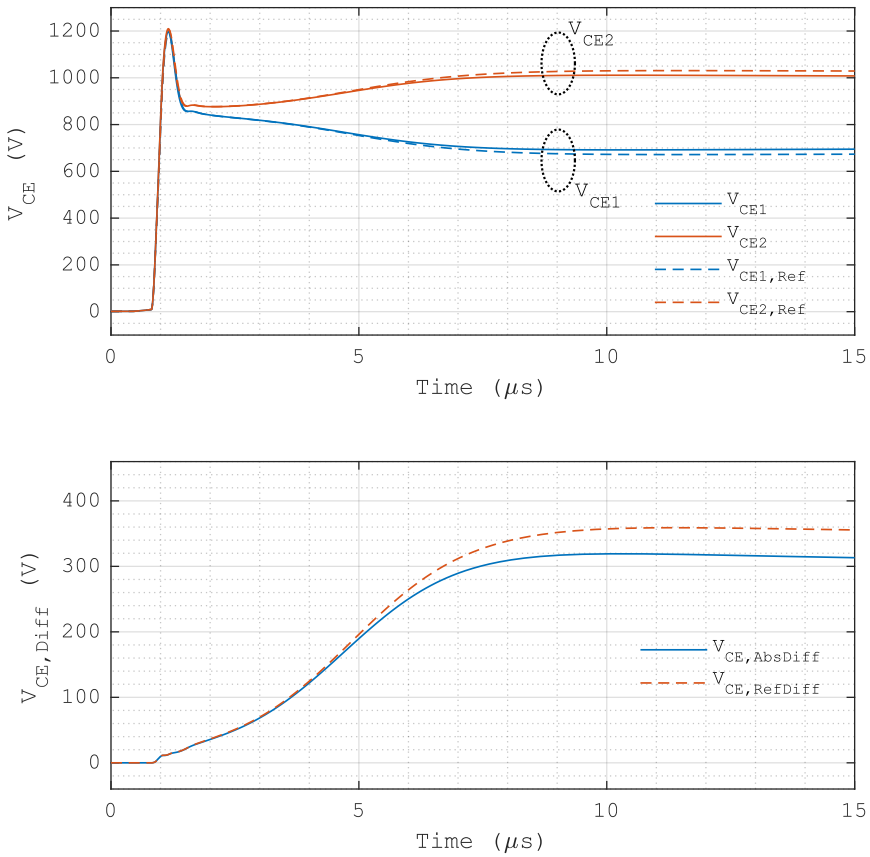


Figure 4.4: Turn-off of two IGBTs in series with the 20% reduced τ_{n0} and τ_{p0}, with the P emitter doping concentration of the $IGBT_1$ increased by 5%.

in the turn-off losses relative to the E_{off2} is reduced to 1.8819% from the original value of 1.9723%, a relative reduction of 4.5813%.

In the two basic V_{CE} diverging scenarios, reducing the carrier lifetimes is effective for mitigating the V_{CE} divergence. Reducing the carrier lifetimes requires additional processing in IGBT fabrication, where local carrier lifetime control in the N buffer is attractive.

4.2.3 Increasing the IGBT P Emitter Doping Concentration

In this simulation test, increasing the P emitter doping concentration is implemented by increasing the basic surface doping concentration of the P emitter at the backside semiconductor surface by 20% to 7.2×10^{17} cm^{-3} from the original value of 6×10^{17} cm^{-3}. The rest of the IGBT parameters and the circuit parameters remain unchanged.

Figure 4.5 shows the turn-off simulation with the 20% increased P emitter doping concentration of two IGBTs in series and a 10 ns delay applied to the gate drive output for the $IGBT_1$. With the 20% increased P emitter doping concentration, the V_{CE} diverging feature during the fast V_{CE}-I_C transient remains similar to that of the original result. Due to the higher excess carrier concentration, during the fast V_{CE} rising, slight reductions are observed in the dV_{CE}/dt rate and the $V_{CE,AbsDiff}$. The $V_{CE,AbsDiff}$ remains below the original $V_{CE,RefDiff}$ during the V_{CE} overshoot but the difference is small. In the tail time, the $V_{CE,AbsDiff}$ diverges from the original $V_{CE,RefDiff}$ and remains below the $V_{CE,RefDiff}$ during the tail time and the following off-state in the simulation.

In this simulation, the largest V_{CE} divergence is reduced to 393.75 V at 11.567 µs from the original value of 438.06 V at 11.659 µs, a relative reduction of 10.115% in the largest V_{CE}

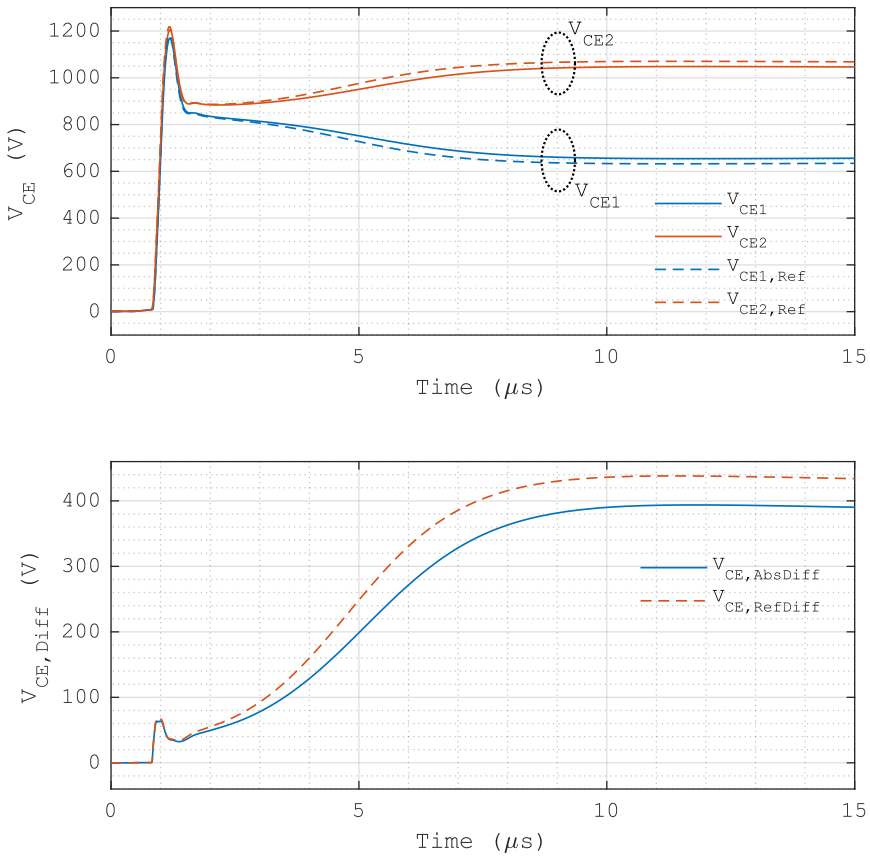


Figure 4.5: Turn-off of two IGBTs in series with the 20% increased basic P emitter doping concentration, with the gate drive output for the $IGBT_1$ delayed by 10 ns.

divergence. These changes are due to the reduced difference in the depletion progress by the increased excess carrier concentration resulting from the 20% increased P emitter doping concentration. The difference in the turn-off losses relative to the E_{off2} is reduced to 6.3326% from the original value of 6.6354%, a relative reduction of 4.5632%. This is due to the relative reduction in the $V_{CE,AbsDiff}$ during the fast V_{CE} rising despite the reduced dV_{CE}/dt rate.

Figure 4.6 shows the turn-off simulation with the 20% increased basic P emitter doping concentration of two IGBTs in series and a 5% further increase in the P emitter doping concentration of the $IGBT_1$. With the 20% increased basic P emitter doping concentration, the V_{CE} diverging feature during the fast V_{CE}-I_C transient remains similar to that of the original result. The results are similar during the fast V_{CE} rising, with a small reduction in the dV_{CE}/dt rate due to the increased excess carrier concentration resulting from the 20% increased basic P emitter doping concentration. During the fast V_{CE}-I_C transient, the $V_{CE,AbsDiff}$ and the original $V_{CE,RefDiff}$ are similar. In the tail time, the $V_{CE,AbsDiff}$ diverges from the original $V_{CE,RefDiff}$ and remains below the $V_{CE,RefDiff}$ during the tail time and the following off-state in the simulation.

In this simulation, the largest V_{CE} divergence is reduced to 342.67 V at 11.594 µs from the original value of 359.00 V at 11.250 µs, a relative reduction of 4.5495% in the largest V_{CE} divergence. These changes are due to the reduced sensitivity of the on-state excess carrier concentration to the P emitter doping concentration at the 20% increased basic P emitter doping concentration. Due to the extended period of the fast V_{CE}-I_C transient resulting from the increased excess carrier concentration, the difference in the turn-off losses relative to the E_{off2} is increased to 1.9976% from the original value of 1.9723%, a relative increase of 1.2828%.

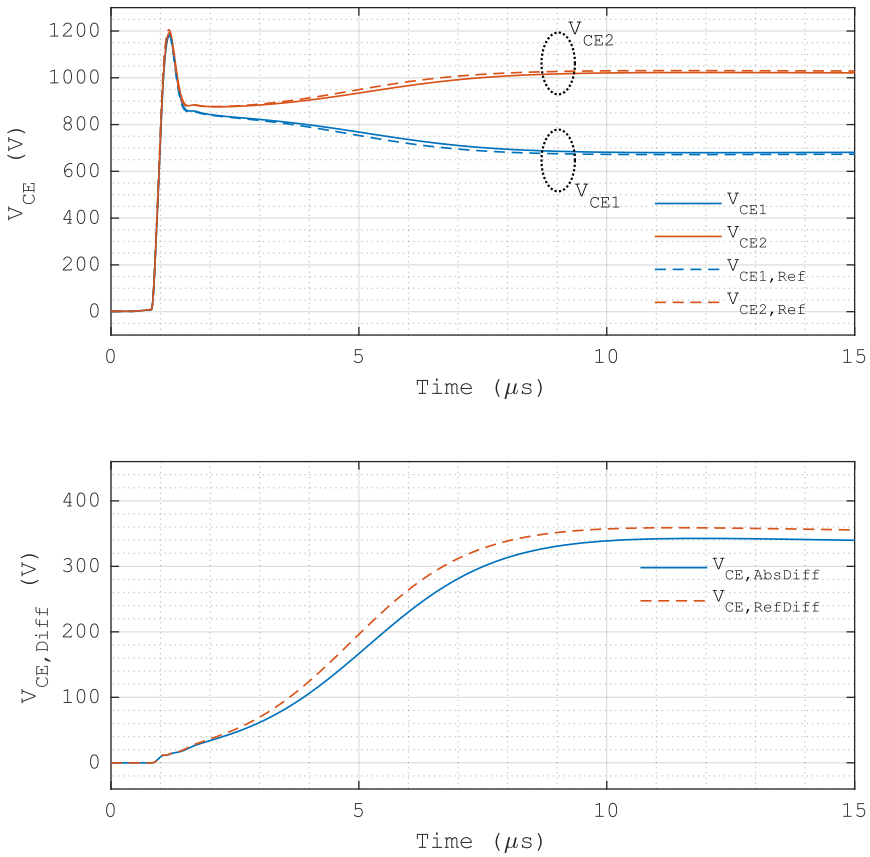


Figure 4.6: Turn-off of two IGBTs in series with the 20% increased basic P emitter doping concentration, with the P emitter doping concentration of the $IGBT_1$ further increased by 5%.

In the two basic V_{CE} diverging scenarios, increasing the P emitter doping concentration is effective for mitigating the turn-off V_{CE} divergence. Increasing the P emitter doping concentration can be implemented by adjusting IGBT fabrication processes. However, the mitigation here of the V_{CE} divergence caused by a variation in the P emitter doping concentration is not ideal, as the relative difference in turn-off losses increases. The increased excess carrier concentration reduces the dV_{CE}/dt rate during the fast V_{CE} rising and causes higher turn-off losses as a side effect. Increasing the P emitter doping concentration results in an increased excess carrier concentration, but it does not conflict with reducing the carrier lifetimes as these two methods are from different approaches.

4.2.4 Increasing the IGBT N-drift Region Thickness

In this simulation test, increasing the IGBT N-drift region thickness is implemented by extending the N-drift region thickness by 15 µm, which increases the semiconductor thickness of the IGBT model to 190 µm from the original value of 175 µm. To obtain comparable results, the 190 µm IGBT model is calibrated to achieve a similar 1700 V class forward-blocking voltage, Figure 4.7, and a dV_{CE}/dt rate similar to that of the 175 µm IGBT model during the fast V_{CE} rising in single-IGBT turn-off at 850 V V_{DC} and 65 A load current, the average circuit conditions for each IGBT in the two-in-series IGBT turn-off. This is achieved by increasing the surface doping concentration of the backside P emitter to 8.5×10^{17} cm^{-3} for the 190 µm IGBT model from the original value of 6×10^{17} cm^{-3} for the 175 µm IGBT model. The rest of the IGBT parameters and the circuit parameters remain unchanged.

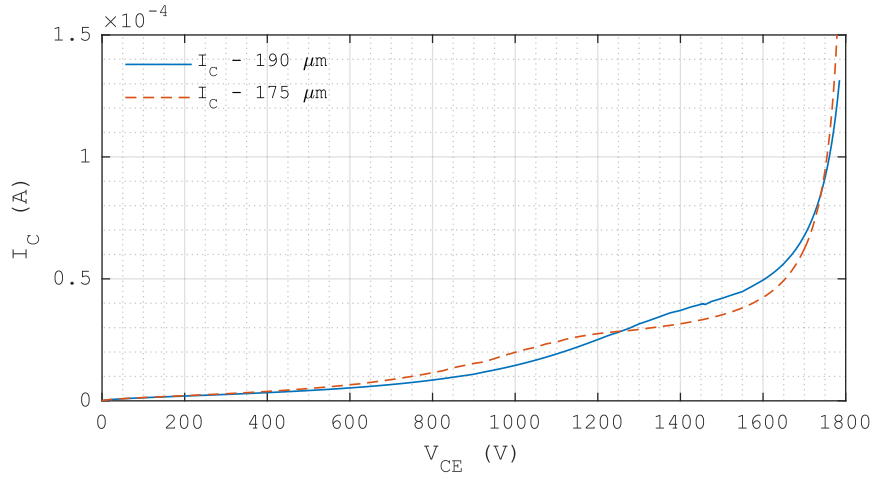


Figure 4.7: Forward-blocking of the IGBT model adjusted to the 190 µm semiconductor thickness.

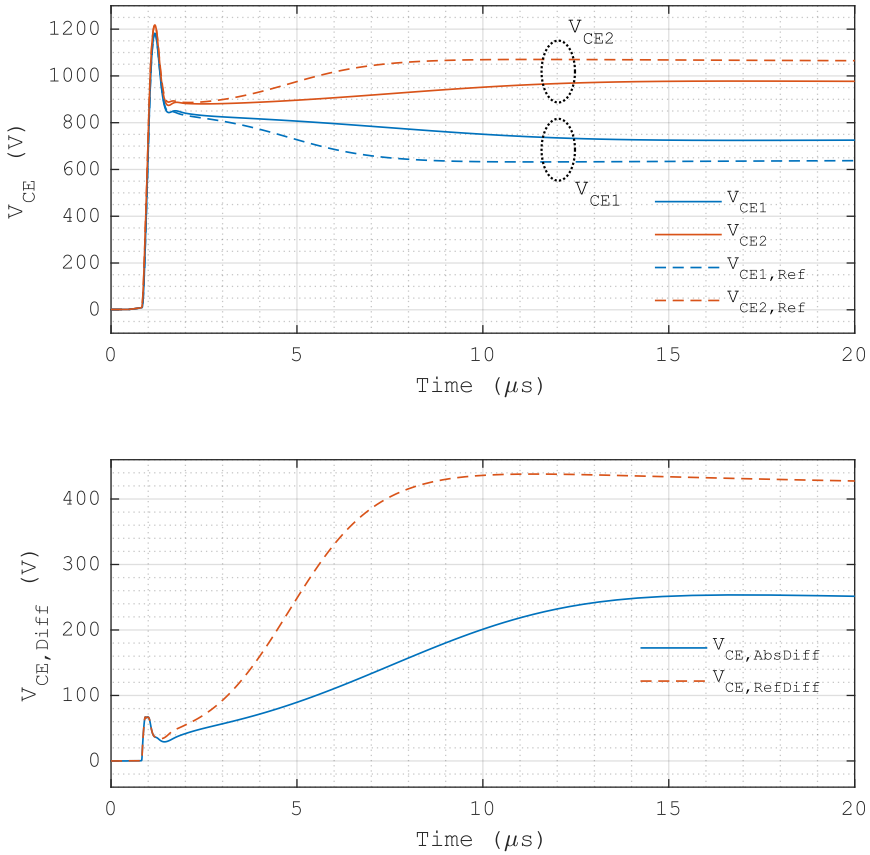


Figure 4.8: Turn-off of two IGBTs in series with the adjusted 190 µm semiconductor thickness, with the gate drive output for the $IGBT_1$ delayed by 10 ns.

Figure 4.8 shows the turn-off simulation with the adjusted 190 µm semiconductor thickness of two IGBTs in series and a 10 ns delay applied to the gate drive output for the $IGBT_1$. Note that the time scale is extended to 20 µs as the expanded CSR here extends the tail time. Despite the adjusted 190 µm semiconductor thickness, in the fast V_{CE}-I_C transient the V_{CE1}, the V_{CE2}, and the $V_{CE,AbsDiff}$ are similar to those in the original result until late in the V_{CE} overshoot at approx. 1.2 µs. From approx. 1.2 µs, the $V_{CE,AbsDiff}$ diverges from and remains below the original $V_{CE,RefDiff}$ in the rest of the turn-off and off-state simulated. In the tail time, the $V_{CE,AbsDiff}$ rises considerably slower than the original $V_{CE,RefDiff}$. This is due to the accumulated effects over time of the larger undepleted part of the N base and the relatively reduced differences in the hole carrier profile and the hole diffusion current towards the depletion region in it.

In this simulation, the largest V_{CE} divergence is reduced to 253.51 V at 16.585 µs from the original value of 438.06 V at 11.659 µs, a relative reduction of 42.129% in the largest V_{CE} divergence despite the extended tail time. These changes are due to the accumulated effects over time of the expanded remaining CSR by the increased N-drift region thickness reducing the difference in the hole diffusion current in the undepleted part of the N base towards the depletion region. The difference in the turn-off losses relative to the E_{off2} is reduced to 6.2057% from the original value of 6.6354%, a relative reduction of 6.4767%. This is due to the relative reduction in the $V_{CE,AbsDiff}$ from late in the V_{CE} overshoot.

Figure 4.9 shows the turn-off simulation with the adjusted 190 µm semiconductor thickness of two IGBTs in series and a 5% increase in the P emitter doping concentration of the $IGBT_1$. The time scale here is also extended to 20 µs as the expanded CSR extends the tail time. In the fast V_{CE}-I_C transient the V_{CE1}, the V_{CE2}, and the $V_{CE,AbsDiff}$ of the 190 µm IGBT model are also similar to those in the original result until late in the V_{CE} overshoot at approx. 1.2 µs. From approx. 1.2 µs, the $V_{CE,AbsDiff}$ diverges from and remains below the original $V_{CE,RefDiff}$ in the rest of the turn-off and off-state simulated. In the tail time, the $V_{CE,AbsDiff}$ also rises considerably slower than the original $V_{CE,RefDiff}$. This is also due to the accumulated effects over time of the larger undepleted part of the N base and the relatively reduced differences in the hole carrier profile and the hole diffusion current towards the depletion region in it.

Similarly, in this simulation, the largest V_{CE} divergence is reduced to 252.61 V at 17.050 µs from the original value of 359.00 V at 11.250 µs, a relative reduction of 29.635% in the largest V_{CE} divergence despite the extended tail time. These changes are also due to the

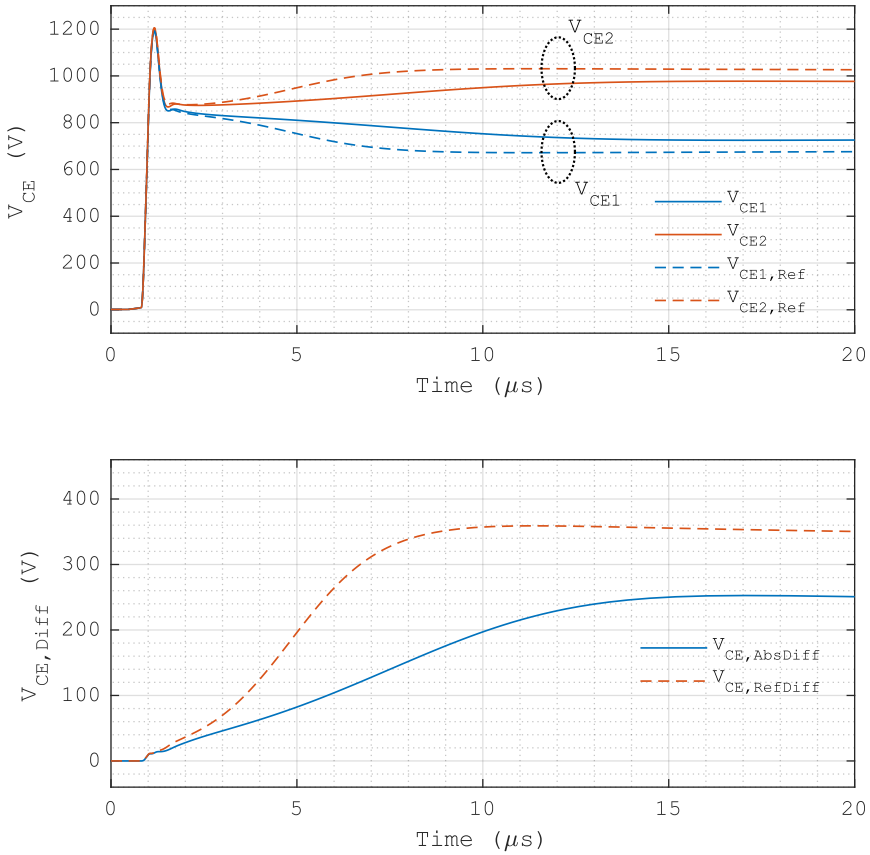


Figure 4.9: Turn-off of two IGBTs in series with the adjusted 190 µm semiconductor thickness, with the P emitter doping concentration of the $IGBT_1$ increased by 5%.

accumulated effects over time of the expanded remaining CSR by the increased N-drift region thickness reducing the difference in the hole diffusion current in the undepleted part of the N base towards the depletion region. However, due to the extended tail time with a higher tail current, the difference in the turn-off losses relative to the E_{off2} is increased to 2.0670% from the original value of 1.9723%, a relative increase of 4.8041%, which is small considering the substantial reduction in the largest V_{CE} divergence.

In the two basic V_{CE} diverging scenarios, increasing the N drift region thickness shows considerable mitigation effects on the turn-off V_{CE} divergence. However, increasing the N drift region thickness alters the trade-off between on-state losses and switching losses which increases overall losses.

4.2.5 Reducing the Off-State V_{CE} Utilisation

In this simulation test, reducing the off-state V_{CE} utilisation is implemented by reducing the DC link voltage V_{DC} via the input and the output stages of the test circuit, the V_{in} and the V_{out} in Figure 3.4, respectively, by 20% to 1360 V from the original value of 1700 V. Thus, the average off-state V_{CE} utilisation of the two IGBTs in series is reduced by 20%. This implementation is related to the use of more IGBTs in series for the same DC link voltage. Hence, the two lumped stray inductances for the IGBT branch and the FWD branch in the CCL, the L_{S0} and the L_{S1} in Figure 3.4, respectively, are both reduced by 20%. The rest of the circuit parameters and the IGBT parameters remain unchanged.

Figure 4.10 shows the turn-off simulation with the 20% reduced off-state V_{CE} utilisation of two IGBTs in series and a 10 ns delay applied to the gate drive output for the $IGBT_1$. Note that the time scale is extended to 20 µs as the expanded CSR here extends the tail time. In the fast V_{CE}-I_C transient, the V_{CE1}, the V_{CE2}, and the $V_{CE,AbsDiff}$ are similar to those in the original result until the early V_{CE} overshoot from approx. 1 µs. During the V_{CE} overshoot, as the I_C falls the $V_{CE,AbsDiff}$ decreases but not as fast as the original $V_{CE,RefDiff}$. This is because the depletion region is smaller at the reduced V_{CE} utilisation, and therefore the decrease in the electric field gradient in it related to the I_C falling has a reduced influence on the voltage across the depletion region. Still, when the turn-off enters the tail time, the $V_{CE,AbsDiff}$ is similar to the original $V_{CE,RefDiff}$. In the tail time, from approx. 1.5 µs, the $V_{CE,AbsDiff}$ diverges from and remains below the original $V_{CE,RefDiff}$ in the rest of the turn-off and off-state simulated. In the tail time, the $V_{CE,AbsDiff}$ rises considerably slower than the original $V_{CE,RefDiff}$. This is due to the accumulated effects over time of the larger undepleted part of the N base and the relatively reduced differences in the hole carrier profile and the hole diffusion current towards the depletion region in it, which is similar to the situation in the previous case of increasing the N drift region thickness.

In this simulation, the largest V_{CE} divergence is reduced to 338.71 V at 16.047 µs from the original value of 438.06 V at 11.659 µs, a relative reduction of 22.679% in the largest V_{CE} divergence despite the extended tail time. These changes are due to the accumulated effects over time of the extended remaining CSR by the lower V_{CE} utilisation reducing the difference in the hole diffusion current in the undepleted part of the N base towards the depletion region. However, the difference in the turn-off losses relative to the E_{off2} is increased to 8.4648% from

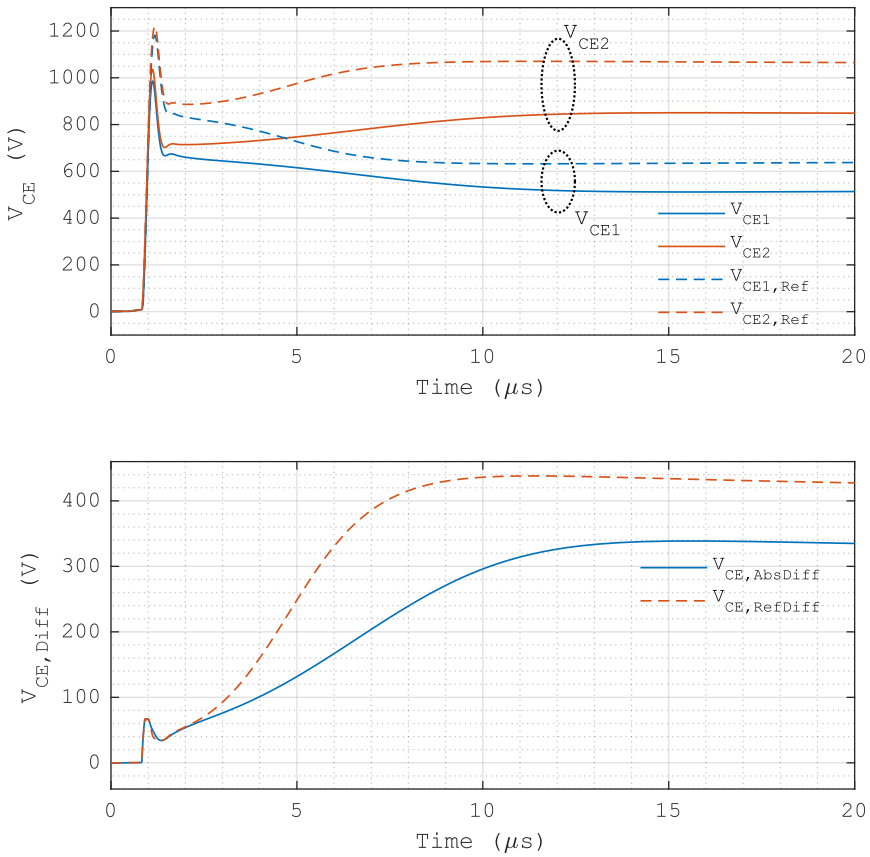


Figure 4.10: Turn-off of two IGBTs in series with the 20% reduced V_{DC}, with the gate drive output for the $IGBT_1$ delayed by 10 ns.

the original value of 6.6354%, a relative increase of 27.570%. This is due to the same load current and the similar V_{CE} divergence during the fast V_{CE}-I_C transient produce a similar turn-off loss difference, but because of the 20% reduction in the V_{DC}, the total turn-off losses here decrease and hence the relative difference in the turn-off losses increases.

Figure 4.11 shows the turn-off simulation with the 20% reduced off-state V_{CE} utilisation of two IGBTs in series and a 5% increase in the P emitter doping concentration of the $IGBT_1$. The time scale here is also extended to 20 µs as the expanded remaining CSR extends the tail time. In the fast V_{CE}-I_C transient, the V_{CE1}, the V_{CE2}, and the $V_{CE,AbsDiff}$ are also similar to those in the original result until the early V_{CE} overshoot from approx. 1 µs. During the V_{CE} overshoot, the $V_{CE,AbsDiff}$ remains close to the original $V_{CE,RefDiff}$. In the tail time, from approx. 1.2 µs, the $V_{CE,AbsDiff}$ diverges from and remains below the original $V_{CE,RefDiff}$ in the rest of the turn-off and off-state simulated. In the tail time, the $V_{CE,AbsDiff}$ rises considerably slower than the original $V_{CE,RefDiff}$. This is also due to the accumulated effects over time of the larger undepleted part of the N base and the relatively reduced differences in the hole carrier profile and the hole diffusion current towards the depletion region in it, which is also similar to the situation in the previous case of increasing the N drift region thickness.

In this simulation, the largest V_{CE} divergence is reduced to 254.10 V at 15.723 µs from the original value of 359.00 V at 11.250 µs, a relative reduction of 29.220% in the largest V_{CE} divergence despite the extended tail time. These changes are also due to the accumulated effects over time of the extended remaining CSR by the lower V_{CE} utilisation reducing the difference in the hole diffusion current in the undepleted part of the N base towards the depletion region.

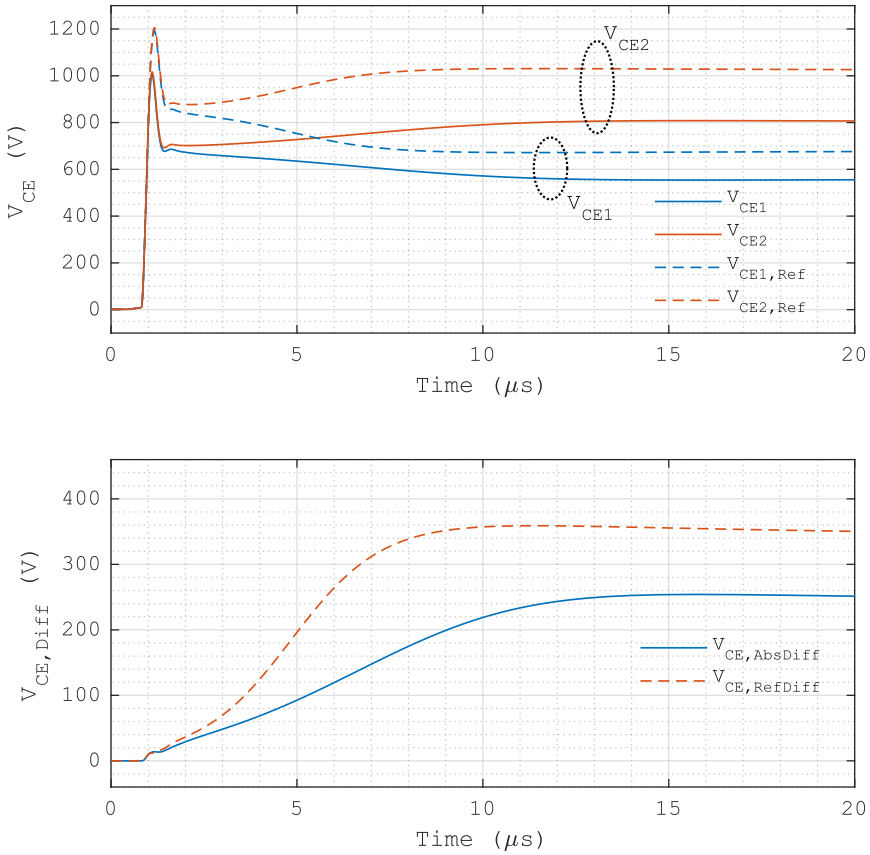


Figure 4.11: Turn-off of two IGBTs in series with the 20% reduced V_{DC}, with the P emitter doping concentration of the $IGBT_1$ increased by 5%.

However, the difference in the turn-off losses relative to the E_{off2} is increased to 2.3910% from the original value of 1.9723%, a relative increase of 21.229%. This is also due to the same load current and the similar V_{CE} divergence during the fast V_{CE}-I_C transient produce a similar turn-off loss difference, but because of the 20% reduction in the V_{DC}, the total turn-off losses here decrease and hence the relative difference in the turn-off losses increases.

In the two basic V_{CE} diverging scenarios, reducing the off-state V_{CE} utilisation shows considerable mitigation effects on the turn-off V_{CE} divergence. However, due to the similar differences in the turn-off losses and the decreases in the total turn-off losses, the relative differences in the turn-off losses are increased.

4.2.6 Reducing the IGBT Gate Resistance

In this simulation test, reducing the IGBT gate resistance is implemented by reducing the basic IGBT gate resistances, the R_{g1} and the R_{g2} in Figure 3.4, by 20% to 10.8 Ω from the original value of 13.5 Ω. The rest of the circuit parameters and the IGBT parameters remain unchanged. According to the discussion in section 1.5.4, an IGBT gate resistance of such a low value completes the MOS channel cut-off early in the fast V_{CE} rising, which only has a minor influence on the dV_{CE}/dt rate in the fast V_{CE} rising. Hence, reducing the IGBT gate resistance only has minor mitigation effects in the two basic V_{CE} diverging scenarios with only minor differences in the individual initial gate discharging between the IGBTs in series. Therefore, reducing the IGBT gate resistance will be tested in the V_{CE} diverging scenarios of a variation in the IGBT gate resistance and a variation in the IGBT gate oxide thickness. The method of reducing the

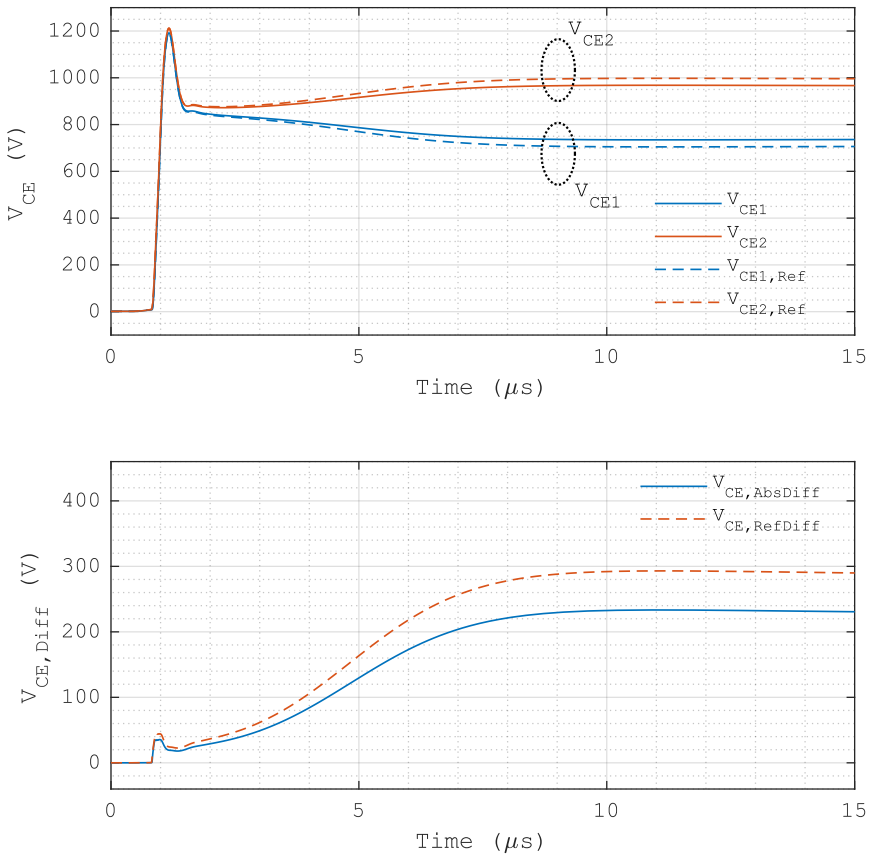


Figure 4.12: Turn-off of two IGBTs in series with the 20% reduced basic IGBT gate resistance, with the R_{g1} for $IGBT_1$ increased relatively by 1%.

IGBT gate resistance is intended for these two scenarios with significant differences in the individual initial gate discharging between the IGBTs in series.

Figure 4.12 shows the turn-off simulation with the 20% reduced basic gate resistance and the R_{g1} for the $IGBT_1$ increased relatively by 1%. Due to the reduced basic gate resistance, the initial gate discharging period is shortened. For a clear comparison, here the test results are shifted along the time axis to align the V_{CE} traces in the fast V_{CE} rising. With the 20% reduced basic gate resistance, the V_{CE} diverging feature remains similar to that in the original result. During the fast V_{CE} rising, a decrease in the $V_{CE,AbsDiff}$ from the original $V_{CE,RefDiff}$ is observed. This is due to the reduced basic gate resistance accelerating the initial gate discharging which reduces the timing difference in the MOS channel cut-off caused by the same relative difference between the gate resistances. During the V_{CE} overshoot, the $V_{CE,AbsDiff}$ remains below the original $V_{CE,RefDiff}$, which suggests that the difference in the depletion progress is reduced. Consequently, in the tail time from approx. 1.5 µs, the $V_{CE,AbsDiff}$ further diverges from and remains below the original $V_{CE,RefDiff}$ in the rest of the turn-off and off-state simulated.

In this simulation, the largest V_{CE} divergence is reduced to 233.42 V at 10.912 µs in Figure 4.12 from the original value of 293.09 V at 11.138 µs, a relative reduction of 20.361% in the largest V_{CE} divergence. The difference in the turn-off losses relative to the E_{off2} is reduced to 3.5550% from the original value of 4.4383%, a relative reduction of 19.901%.

Figure 4.13 shows the turn-off simulation with the 20% reduced basic gate resistance and the gate oxide thickness of the $IGBT_1$ increased by 1%. Due to the reduced basic gate resistance, the initial gate discharging period is shortened. For a clear comparison, here the test results are

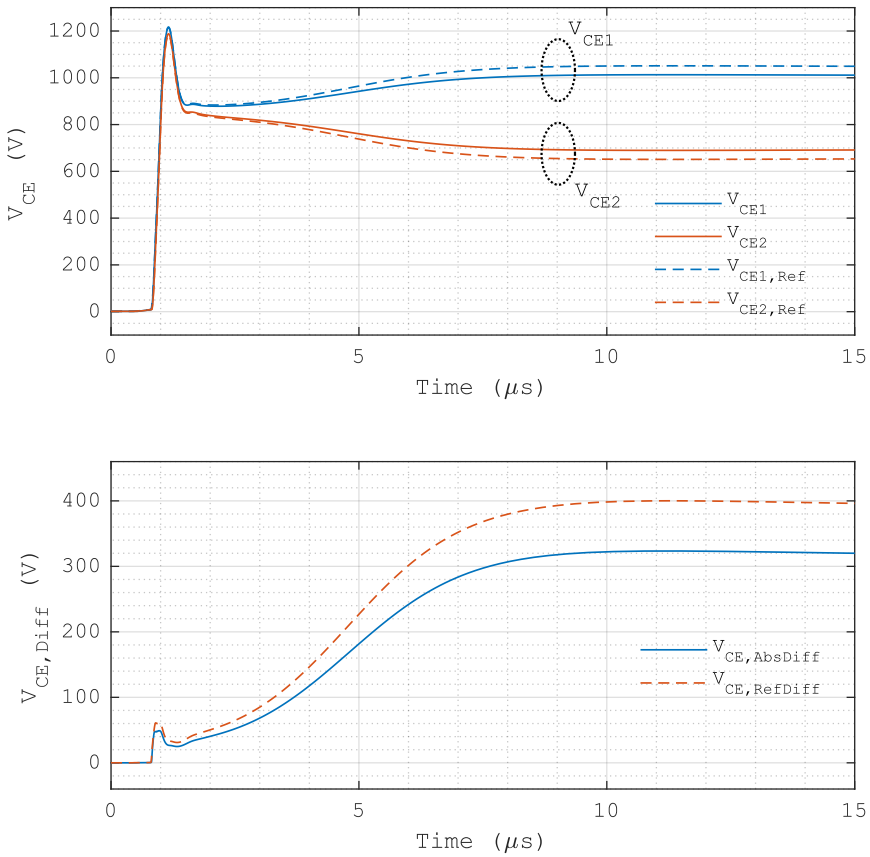


Figure 4.13: Turn-off of two IGBTs in series with the 20% reduced basic gate resistance, with the gate oxide thickness of the $IGBT_1$ increased by 1%.

also shifted along the time axis to align the V_{CE} traces in the fast V_{CE} rising. Note that unlike the previous simulation tests shown in section 4.2, the V_{CE1} in Figure 4.13 is higher than the V_{CE2} due to the increase in the gate oxide thickness applied to the $IGBT_1$. With the 20% reduced basic gate resistance, the V_{CE} diverging feature remains similar to that in the original result. During the fast V_{CE} rising, a decrease in the $V_{CE,AbsDiff}$ from the original $V_{CE,RefDiff}$ is observed. This is due to the reduced basic gate resistance accelerating the initial gate discharging which reduces the timing difference in the MOS channel cut-off caused by the same relative difference in the gate oxide thickness. During the V_{CE} overshoot, the $V_{CE,AbsDiff}$ remains below the original $V_{CE,RefDiff}$, which suggests that the difference in the depletion progress is reduced. Consequently, in the tail time from approx. 1.5 µs, the $V_{CE,AbsDiff}$ further diverges from and remains below the original $V_{CE,RefDiff}$ in the rest of the turn-off and off-state simulated.

In this simulation, the largest V_{CE} divergence is reduced to 323.43 V at 11.509 µs in Figure 4.13 from the original value of 400.12 V at 11.250 µs, a relative reduction of 19.166% in the largest V_{CE} divergence. The difference in the turn-off losses relative to the E_{off2} is reduced to 5.1491% from the original value of 6.4348%, a relative reduction of 19.981%.

Reducing the IGBT gate resistance shows significant mitigation effects on the turn-off V_{CE} divergence caused by a variation in the IGBT gate resistance or the IGBT gate oxide thickness. The relative reductions in the relative turn-off loss differences are close to the relative reductions in the largest V_{CE} divergence, both of which are also close to the relative reduction of 20% in the basic IGBT gate resistance.

4.3 The Use of the Passive Mitigation Methods in Combination

The relative changes in the largest V_{CE} divergence and the relative turn-off loss differences of the test results presented in section 4.2 are summarised in Table 4.2. Note that the results in the last entry of the -20% R_G are tested in different V_{CE} diverging scenarios.

Table 4.2: Summary of the simulation test results of the passive mitigation methods.

Passive mitigation method	+10 ns gate drive output delay		+5% P emitter doping conc.	
	Rel. change in largest V_{CE} divergence	Rel. change in rel. turn-off loss diff.	Rel. change in largest V_{CE} divergence	Rel. change in rel. turn-off loss diff.
-20% J_C (+25% A_{IGBT})	-7.2286%	-5.8817%	-1.6269%	+9.5292%
-20% τ_{n0} and τ_{p0}	-9.2027%	+0.95558%	-11.095%	-4.5813%
+20% P emitter doping conc.	-10.115%	-4.5632%	-4.5495%	+1.2828%
+15 µm N drift region thickness	-42.129%	-6.4767%	-29.635%	+4.8041%
-20% V_{DC}	-22.679%	+27.570%	-29.220%	+21.229%
-20% R_G	-20.361% *	-19.901% *	-19.166% **	-19.981% **
	* tested under +1% gate resistance		** tested under +1% gate oxide thickness	

All the passive mitigation methods in section 4.1 are capable of providing effective mitigation of the V_{CE} divergence. However, individual increases in the relative difference in the turn-off losses are found except for the method of reducing the IGBT gate resistance which is tested in different V_{CE} diverging scenarios. Nevertheless, it is possible to use some of those passive methods in combination to compensate for their individual disadvantages.

Regarding IGBT parameters, the methods of the -20% τ_{n0} and τ_{p0} and the +20% P emitter doping concentration only have small relative increases in the relative loss difference in different basic diverging scenarios. The former has a small relative increase in the basic scenario of a gate driving delay, while the latter has a small relative increase in the basic scenario of a variation in the P emitter doping concentration. Therefore, the use of these two methods in combination can compensate for their individual relative increases in the relative loss difference and their individual influences on the on-state losses. Appropriate application of these two methods in combination can also improve the trade-off between the on-state losses and the turn-off losses. To achieve the same on-state excess carrier profile, a higher P emitter doping concentration with local carrier lifetime control in the N buffer can reduce the tail current in turn-off and improve the basis of the turn-off V_{CE} sharing, although adjustments in IGBT fabrication processes will be required.

Similarly, the method of the +15 µm N drift region thickness provides considerable mitigation effects with only a moderate relative increase in the relative loss difference in the basic scenario of a variation in the P emitter doping concentration. This moderate relative increase can be compensated for by the method of reducing the carrier lifetimes. Therefore, these two methods can be another useful combination.

Regarding IGBT operating conditions, as shown in the last result entry in Table 4.2, the method of the -20% R_G provides consistent mitigation effects on the V_{CE} divergence in the two scenarios for which the method is designed, with comparable and consistent relative reductions

in the relative loss differences. The rest of the methods here, although can provide mitigation effects on the V_{CE} divergence, have disadvantages in the relative loss difference. These methods can be used in combination with the method of reducing the carrier lifetimes to offset their disadvantages in the relative loss difference.

Figure 4.14 and Figure 4.15 show the simulation tests of the use of those four methods in combination in the two basic V_{CE} diverging scenarios with a 10 ns gate driving delay applied to the $IGBT_1$ and a 5% increase of the P emitter doping concentration applied to the $IGBT_1$, respectively. These tests are based on the 190 µm IGBT model used in section 4.2.4, with the other three methods applied in the same manner as in their individual tests. As discussed previously, the method of reducing the IGBT gate resistance is not expected to provide significant mitigation effects in the two basic V_{CE} diverging scenarios. To compare with the original results, the test results here are shifted along the time axis to align the V_{CE} traces. The V_{CE} diverging features shown in Figure 4.14 and Figure 4.15 are similar to those in the respective tests of increasing the IGBT N-drift region thickness using the 190 µm IGBT model and therefore will not be repeated here.

In the simulation of the 10 ns gate driving delay, Figure 4.14, the largest V_{CE} divergence is reduced to 200.36 V at 15.419 µs from the original value of 438.06 V at 11.659 µs, a relative reduction of 54.261% in the largest V_{CE} divergence. The difference in the turn-off losses relative to the E_{off2} is reduced to 6.0402% from the original value of 6.6354%, a relative reduction of 8.9702%.

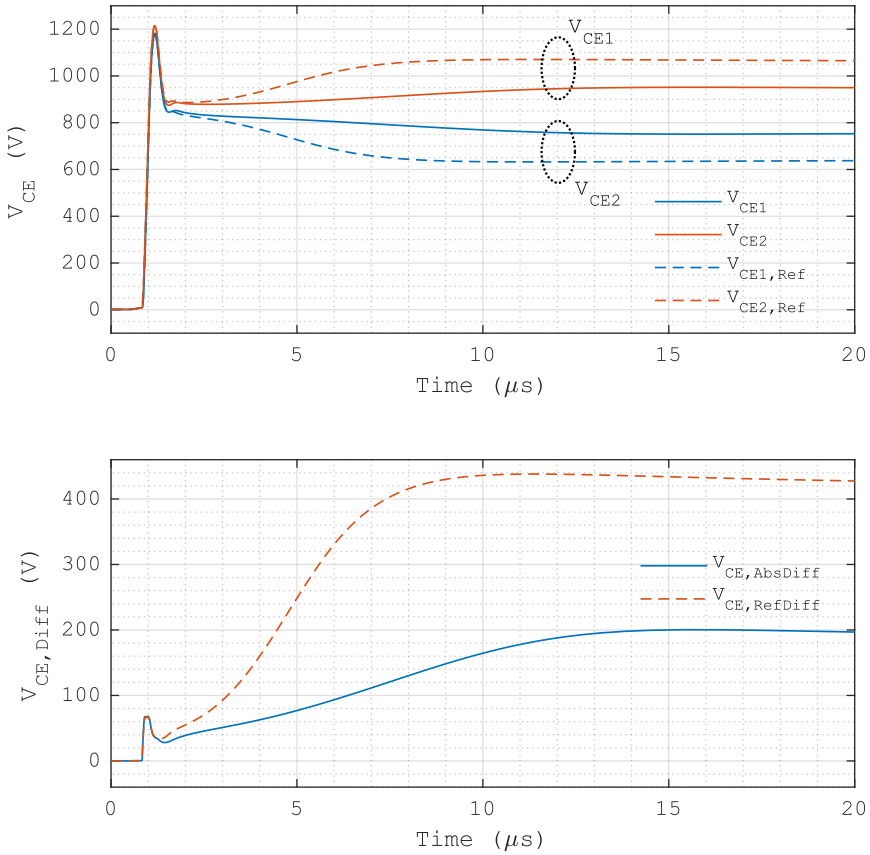


Figure 4.14: Turn-off of two IGBTs in series with the use of three passive mitigation methods in combination. A gate driving delay of 10 ns is applied to the $IGBT_1$.

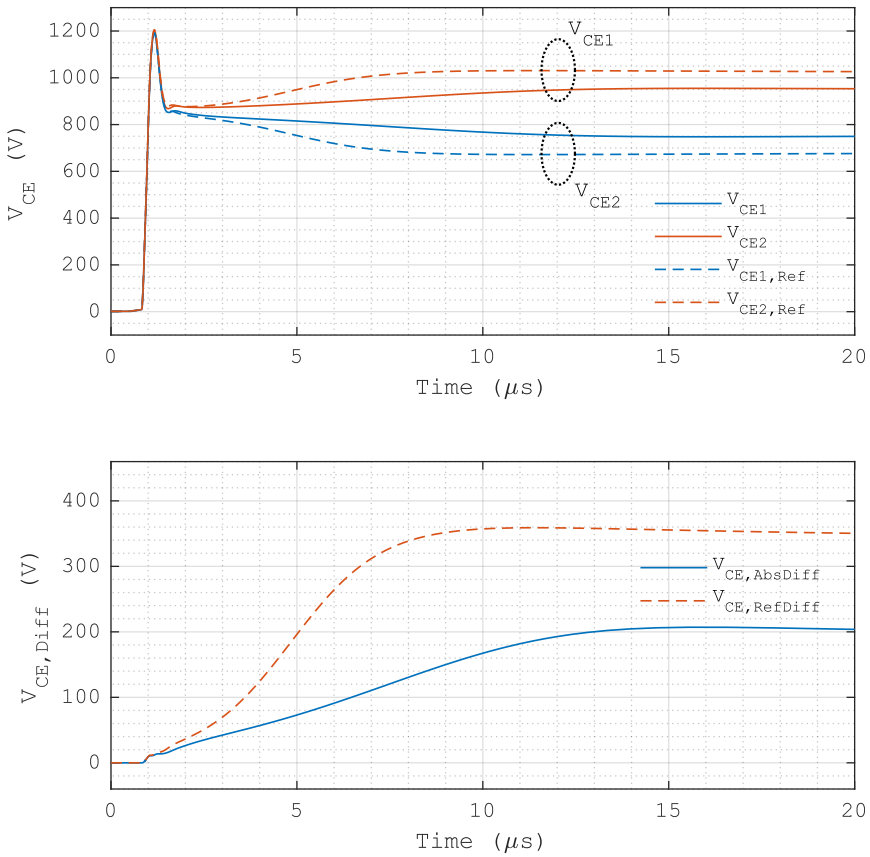


Figure 4.15: Turn-off of two IGBTs in series with the use of three passive mitigation methods in combination. A 5% increase in the P emitter doping concentration is applied to the $IGBT_1$.

In the simulation test of the 5% increase in the P emitter doping concentration, Figure 4.15, the largest V_{CE} divergence is reduced to 207.05 V at 15.545 µs from the original value of 359.00 V at 11.250 µs, a relative reduction of 42.327% in the largest V_{CE} divergence. The difference in the turn-off losses relative to the E_{off2} increases slightly to 2.0028% from the original value of 1.9723%, a small relative increase of 1.5486%.

In these two simulation tests, the relative reductions in the largest V_{CE} divergence and the relative changes in the relative turn-off loss difference are close to the respective products of those of the three methods related to IGBT parameters, Table 4.3. Considering the change of the base IGBT model, the mitigation effects of the tested passive mitigation methods in combination are as expected.

Table 4.3: Comparison of the combined mitigation effects of a few passive mitigation methods.

Method	+10 ns gate drive output delay		+5% P emitter doping conc.	
	Rel. change in largest V_{CE} divergence	Rel. change in rel. turn-off loss diff.	Rel. change in largest V_{CE} divergence	Rel. change in rel. turn-off loss diff.
-20% τ_{n0} and τ_{p0}	-9.2027% (90.797%)	+0.95558% (100.96%)	-11.095% (88.905%)	-4.5813% (95.419%)
+20% P emitter doping conc.	-10.115% (89.885%)	-4.5632% (95.437%)	-4.5495% (95.451%)	+1.2828% (101.28%)
+15 µm N drift region thickness	-42.129% (57.871%)	-6.4767% (93.523%)	-29.635% (70.365%)	+4.8041% (104.80%)
Products of relative changes	-52.770% (47.230%)	-9.8914% (90.109%)	-40.288% (59.712%)	+1.2855% (101.29%)
The use of methods in combination	-54.261%	-8.9702%	-42.327%	+1.5486%

The passive mitigation methods discussed in this chapter are effective in the simulation tests. Appropriate application of some of these methods in combination is attractive as the individual drawbacks of these methods can be compensated for while maintaining or even improving the trade-off between the on-state losses and the turn-off losses. The passive approaches here are focused on improving the basis of the turn-off V_{CE} sharing rather than regulating the V_{CE} sharing. Due to the nature of passive approaches, these passive mitigation methods cannot regulate the V_{CE} sharing or considerably mitigate the V_{CE} divergence without significantly degrading IGBT performance. These challenges can be addressed by the use of active voltage regulation methods via feedback control, which will be discussed in the following two chapters.

Chapter 5 Direct Active Voltage Control for Regulating the Voltage Sharing

5.1 Direct Active IGBT Gate Control for Regulating the V_{CE} Sharing

At IGBT device level, the basic V_{CE} diverging mechanisms and seven V_{CE} diverging factors concerning IGBT internal parameter variations and gate control errors are discussed in Chapter 3. Following Chapter 3, six passive mitigation methods at IGBT device level regarding IGBT parameters and operating conditions are designed and tested in simulation in Chapter 4. Some of these passive mitigation methods and appropriate application of them in combination are practical, but passive mitigation methods cannot regulate the V_{CE} sharing or considerably mitigate the V_{CE} divergence without significantly degrading IGBT performance. Although outside the scope of this thesis, beyond device level, the geometry of the power circuit often results in different parasitic capacitances between the individual IGBT modules in series to ground which affect the turn-off V_{CE} sharing [202]. Hence, active control methods using feedback control are required to regulate the turn-off V_{CE} sharing for the operation of IGBTs in series.

Evenly distributed V_{CE} sharing in uncontrolled IGBT turn-off is rarely achieved in practice due to the differences between the IGBTs, the gate drives, and the circuit parameters for individual IGBTs. The mechanisms of the V_{CE} divergence in IGBT turn-off are discussed in Chapter 3. Ideally, with identical parameters for individual IGBTs, the individual turn-off trajectories of the IGBTs in series will be the same as that of a single IGBT turned off with scaled circuit parameters for one IGBT.

5.1.1 AVC Scheme and Its Implementation for Regulating the V_{CE} Sharing

Among the active control methods summarised in section 2.2, the Active Voltage Control (AVC) is the most versatile control scheme in terms of the control of the V_{CE}. The AVC scheme applies closed-loop feedback control via IGBT gate control to control the V_{CE} of an IGBT. Where controllable, the AVC scheme can control the V_{CE} to follow a preset trajectory using a calibrated V_{CE} reference signal [174], [203], [204], which can be designed for various control targets, e.g. regulating the V_{CE} sharing. Hence, in this thesis the AVC scheme is employed for the active regulation of the V_{CE} sharing.

The use of the AVC scheme in this thesis adopts the basic control structure of the Cascade Active Voltage Control (CAVC) in [204], Figure 5.1. The original CAVC in [204] uses three feedback loops for V_{CE} feedback, $\mathrm{d}V_{CE}/\mathrm{d}t$ feedback, and V_{GE} feedback, Figure 5.1. The stability of the CAVC has been analysed with experiments in [204]. The active V_{CE} sharing regulation method here aims to achieve a high turn-off $\mathrm{d}V_{CE}/\mathrm{d}t$ rate using the strategy of differential regulation with a low gate resistance. Hence, the V_{GE} feedback is not applicable due to the internal gate resistance which is comparable to the external gate resistance preventing usable feedback of the V_{GE} of the IGBT chips. Also, the $\mathrm{d}V_{CE}/\mathrm{d}t$ feedback is not applicable due to the intended use of differential regulation. Therefore, here only the V_{CE} feedback loop is used.

The feedback control of the V_{CE} is achieved by comparing the scaled feedback of the V_{CE}, $V_{FB} = \alpha V_{CE}$ obtained via a potential divider, with the V_{CE} reference signal V_{REF} and applying the

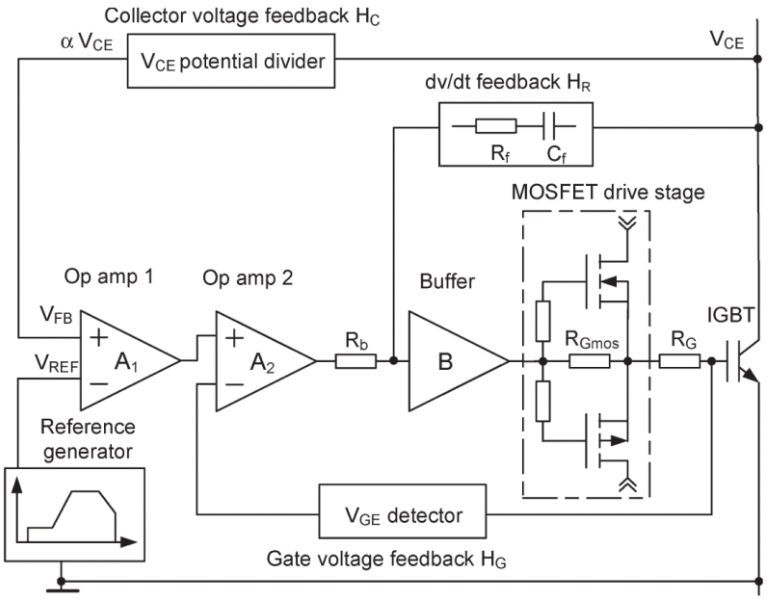


Figure 5.1: Basic control structure of the original CAVC [204].

processed and amplified error signal to the IGBT gate, which is an implementation of classic Proportional-Derivative (PD) control. This control structure can reduce the dependence of the control performance on the main plant, e.g. the IGBT [204].

5.1.2 Previous Implementations and Drawbacks

So far the most comprehensive use of the AVC scheme for regulating the V_{CE} sharing is reported in [180]. The circuit implementation of the AVC scheme in [180] is based on the AVC circuit configuration in [204], Figure 5.1.

The V_{CE} reference signal in [180] consists of three control stages. The first preconditioning stage features a low clamp to accommodate the timing difference in the initial discharging of the IGBT MOS gate from the on-state level to the V_{GE} controlled active region. The V_{CE} is expected to settle at a low level in this stage to improve the synchronisation of the V_{CE} after the initial gate discharging. In [180] the implementation results in a V_{CE} overshoot and a relatively high V_{CE} clamping level in this stage which cause undesirable losses.

The second control stage features a ramp in the V_{CE} reference signal that extends above the value for the average off-state V_{CE} of the IGBTs, which enables V_{CE} overshoot and load current commutation. In [180] this ramp is designed to control the V_{CE} through the V_{GE} controlled active region. In this stage the V_{CE} is expected to rise under the control of this ramp. To achieve such actively controlled V_{CE} rising, this ramp extends over a longer period than the V_{CE} rising time in hard-switched turn-off with a low gate resistance under the same load conditions. A drawback of such a ramp is a reduced $\mathrm{d}V_{CE}/\mathrm{d}t$ rate during the fast V_{CE} rising which increases the turn-off losses. Also, in such an implementation of the AVC scheme, the V_{CE} control performance of this ramp is weaker at low load currents [205], [206].

The third control stage features a temporarily lowered hard clamp in the V_{CE} reference signal, calibrated for the average off-state V_{CE} of the IGBTs and applied near the end of the tail time. The V_{CE} divergence accumulated after the V_{CE} overshoot is significantly reduced in this stage. This temporary clamp is removed after it is expected that the V_{CE} sharing will not diverge

to a significant extent afterwards. Before the temporary clamp, only the maximum V_{CE} is limited by an upper clamp which cannot effectively reduce the V_{CE} divergence. Hence, the V_{CE} divergence before the temporary clamp and the relatively high initial tail current of the high voltage Si IGBT cause a difference in the turn-off losses between the IGBTs.

In [180] the V_{CE} divergence is expected to be small and stable after processed by the AVC circuit and the V_{CE} reference signal. The experiment examples in [180] demonstrate that the V_{CE} divergence can be reduced to near zero after the temporary clamp in the V_{CE} reference signal and remain relatively stable afterwards, although the V_{CE} divergence in the tail time can still become significant before the temporary clamp.

A few factors are responsible for the underperforming of the AVC circuit and the V_{CE} reference signal in [180]. First, the AVC gate drives in [180] are subject to a triggering delay in the acquisition of the instruction signal for IGBT switching between the AVC gate drives. Digital IGBT gate drives based on FPGAs, e.g. the prototype AVC gate drives used in this thesis and in [180], enable the use of advanced control schemes. However, the synchronisation of the clock sources for the FPGAs is difficult between the gate drives isolated for the high voltage insulation requirements of the IGBTs in series. The triggering delay is therefore difficult to minimise and can be up to the full edge detection period of the FPGA, which is often an internal FPGA clock cycle. Even assuming complete control of the V_{CE}, since the V_{CE} reference signal in [180] apparently does not synchronise the peak of the V_{CE} overshoot, such a triggering delay can still cause a difference in the depletion progress by the initial tail time.

Regarding the V_{CE} control performance of the AVC scheme, due to the phase lag of the AVC loop [204], e.g. contributed by the propagation delay of the op-amps, the charging/discharging of the IGBT gate-emitter capacitance C_{GE}, and the internal ambipolar carrier transport, it is difficult to achieve high precision control of the V_{CE} in IGBT turn-off, even with well optimised AVC circuit parameters [204]. Even assuming matched instruction signal acquisition and AVC circuit performance, the V_{CE} control performance that is dependent on IGBT parameters [204] cannot ensure synchronised depletion progress during the turn-off. As discussed in Chapter 3, a small difference in the depletion progress can cause significant V_{CE} divergence in the tail time before the temporary clamp in [180] is applied.

5.2 Design and Implementation of Direct Active V_{CE} Sharing Regulation

The use of the AVC scheme here for direct active V_{CE} sharing regulation has been published to a limited extent by the thesis author as the first author in [185]. The experimental implementation of the direct active V_{CE} sharing regulation here attempts to demonstrate its design concept and key principles. Monitoring of circuit conditions, real-time automatic adjustments to the V_{CE} reference signal, and protection of the IGBTs switched in series are essential at product level, which are intended for future research.

5.2.1 Design Concept of the Direct Active V_{CE} Sharing Regulation

Considering the basic V_{CE} diverging mechanisms discussed in section 3.3, to compensate for the internal differences between the IGBTs that can cause the V_{CE} divergence in turn-off, a

universal approach is to adjust the proportions of the current components in the IGBT with a higher V_{CE}. Thus, the depletion process in the fast V_{CE}-I_C transient and the hole diffusion current in the undepleted part of the N base towards the depletion region in the tail time can be adjusted to suppress the original V_{CE} diverging mechanisms and mitigate the V_{CE} divergence. The intended adjustments to the proportions of the current components are achieved by introducing an electron current via the IGBT MOS channel controlled by the AVC scheme. With an adequate electron current via the MOS channel to counter the effects of the V_{CE} diverging factors, the original V_{CE} diverging mechanisms can be reversed to reduce the V_{CE} divergence.

To reduce the additional turn-off losses related to the V_{CE} sharing regulation, here the active V_{CE} sharing regulation is based on the strategy of differential V_{CE} sharing regulation, where the V_{CE} sharing regulation is only active on the IGBT with a higher V_{CE}. The direct V_{CE} sharing regulation is intended to regulate the V_{CE} sharing as it tends to diverge. This is to reduce the difference in the turn-off losses and mitigate the influence of the V_{CE} sharing regulation on the stability and the EMC of the power circuit. A redesigned preconditioning stage to mitigate the timing difference in the initial discharging of the IGBT MOS gate is also included. The mechanism and the implementation will be discussed further in the following sections.

5.2.2 Mechanism of the Differential V_{CE} Sharing Regulation

The differential V_{CE} sharing regulation here is triggered only on the IGBT with a higher V_{CE} when its V_{CE} exceeds a preset trajectory including a small safety margin. During the turn-off, for the IGBT with a higher V_{CE}, when the V_{CE} sharing regulation is triggered, its V_{GE} is raised above the V_{TH} by its AVC gate drive circuit, and an inversion layer in the MOS channel is formed to provide a small electron current for the depletion region. In the depletion region this electron current reduces the proportion of the hole current to the electron current compared with that in the other IGBT without an electron current via the MOS channel, which is assisted by the recombination of the electrons via the MOS channel with the drifting holes. Hence, in conjunction with the negative charges by those electrons, the positive net charge density and the electric field gradient in the depletion region are lower relative to the IGBT with a lower V_{CE}.

In the fast V_{CE}-I_C transient when high-level excess carriers exist in the undepleted part of the N base, the electrons via the MOS channel that reach the CSR supply some electrons to the ambipolar current in the CSR. Relative to the IGBT with a lower V_{CE}, this process results in lower transport of the excess electrons towards the P emitter and the excess holes towards the depletion region from the MOS gate side CSR boundary. Therefore, the difference in the expansion of the depletion region is mitigated, and with the relatively lower electric field gradient in the depletion region, the V_{CE} divergence is mitigated.

In the tail time when high-level excess electrons no longer exist in the undepleted part of the N base, the electrons via the MOS channel that reach the undepleted part of the N base reduce the proportion of the hole drift current in it towards the depletion region. This process is assisted by a higher hole diffusion current from the P emitter due to a higher electron current in the undepleted part of the N base. Consequently, further depletion in the N base in the IGBT with a higher V_{CE} that increases the V_{CE} divergence is mitigated. In conjunction with the lower

electric field gradient in the depletion region, the V_{CE} divergence is mitigated. With adequate electrons via the MOS channel reaching the undepleted part of the N base, the opposing diffusion-drift relation of the electrons at the depletion edge in the N base can be biased to diffusion, which recovers the depletion region from that depletion edge. In this process, the electron current via the MOS channel also results in increases in the hole diffusion current from the P emitter and the I_C. The increase in the hole diffusion current from the P emitter assists the redistribution of holes as the depletion region is being recovered. Meanwhile, since the I_C of the IGBT with a lower V_{CE} is increased, the original mechanism that causes the V_{CE} divergence is reversed and the V_{CE} divergence is reduced.

5.2.3 Implementation of the AVC Gate Drive Circuit

The experimental implementation of the AVC gate drive circuit here for the direct active regulation of the V_{CE} sharing is shown in Figure 5.2 with key parameters included. The IGBT V_{CE} is scaled down via a passive network R_{f2}-C_{f2}/R_{f1}-C_{f1} by a ratio of 101:1. The scaled V_{CE} feedback, V_{FB}, is compared with a V_{CE} reference signal, V_{REF}, and the difference is amplified by a gain of 10. This stage is achieved using a voltage source op-amp, Texas Instruments LM7171 indicated by LM7171_1. The next op-amp, a second Texas Instruments LM7171 indicated by LM7171_2, is configured as a voltage follower to enable high bandwidth driving for the next buffer stage. The LM7171_2 can also be configured to further increase the gain if required.

The output current of the op-amp stage is enhanced using a buffer, Texas Instruments BUF634, to drive a push-pull gate driving stage by BJTs, Diodes Inc. FZT851 (NPN) and Diodes Inc. FZT951 (PNP), to provide adequate driving current capabilities for the use of a low gate resistance. The push-pull BJTs replace the push-pull MOSFETs used in [204] as shown in Figure 5.1 to increase the output voltage range and enhance the response of the gate driving stage. This gate driving stage is more cost-effective compared with the use of multiple high-speed op-amps in parallel to provide the same driving current capabilities. The external gate resistance Rg_ext is 1 Ω. Further reducing the external gate resistance enhances the response of the AVC loop but starts to cause stability issues. In the AVC gate drive, the nominal power supply voltages for the gate driving stage are ±15 V, and the measured output voltage range of

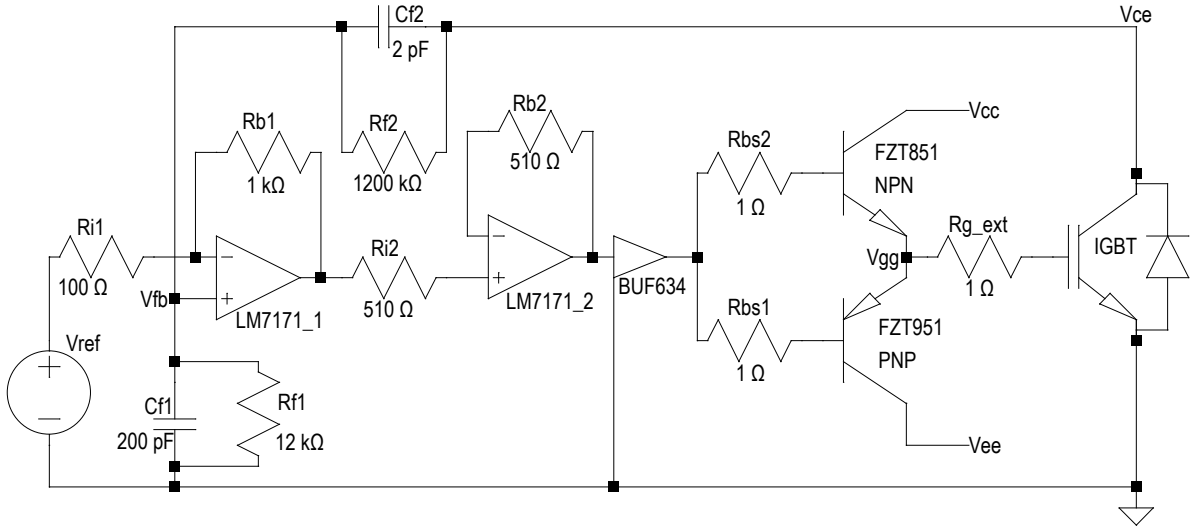


Figure 5.2: Implementation of the AVC circuit.

the AVC gate drive is approx. +13.3 V to -13.2 V. Such a range is reasonable considering the voltage drops of the forward biased PN junctions from the power supply to the output.

The ideal output voltage of the AVC gate drive, ignoring the PN junction voltage drops of the output BJTs, under quasi-static conditions can be described by:

$$V_{GG} = (V_{FB} - V_{REF})\frac{R_{b1}}{R_{i1}} + V_{FB} \qquad \text{Equation 5.1}$$

For calibrating the V_{CE} reference signal, it is convenient to write Equation 5.1 as:

$$V_{REF} = (V_{FB} - V_{GG})\frac{R_{i1}}{R_{b1}} + V_{FB} \qquad \text{Equation 5.2}$$

With the V_{CE} reference signal calibrated, when the V_{CE} exceeds the predicted trajectory plus a small safety margin, the V_{GG} is raised by the AVC circuit to increase the V_{GE} for introducing or increasing the electron current via the MOS channel, so that the V_{CE} divergence can be mitigated as discussed in section 5.2.2.

In the AVC gate drive, the V_{REF} is generated by an on-board FPGA and an 8-bit Digital-to-Analog Converter (DAC). The FPGA, Xilinx Spartan-3AN XC3S50AN, uses an independent on-board crystal as its clock source. Despite the same nominal frequency of the crystals, neither the frequency nor the phase of the clock sources in the AVC gate drives is synchronised. The instruction signal for an IGBT switching event is distributed to the AVC gate drives via optical fibres from a central signal generator due to the requirements of high voltage insulation.

The generation of the V_{REF} for IGBT turn-off and turn-on is triggered independently once a respective instruction signal is acquired by the FPGA. Due to the unsynchronised clock sources for the FPGAs, a relative jitter in the acquisition of an instruction signal exists between the FPGAs. In the experimental implementation here, the on-board FPGAs are operated at a nominal frequency of 50 MHz, which results in a signal acquisition jitter between the FPGAs of ±20 ns maximum. The maximum operational frequency of an FPGA depends on the physical layout and the performance of the logic blocks used in the FPGA for the logic programmed and the quality of the clock signal distributed to those logic blocks. With the essential control logic programmed in the FPGA here, the operating frequency of 50 MHz cannot be further increased without compromising reliability. Hence, the maximum signal acquisition jitter cannot be further reduced.

This signal acquisition jitter after processed through the FPGA and the DAC is converted into a timing jitter in the V_{REF}, which leads to a timing jitter in IGBT switching. As the generation of the V_{REF} for IGBT turn-off and turn-on is triggered independently, an early timing of turn-off may not lead to an early timing of the following turn-on.

5.2.4 Implementation of the V_{CE} Reference Signal

The implementation of the V_{CE} reference signal V_{REF} here is based on the strategy of differential V_{CE} sharing regulation, where the V_{CE} sharing regulation is only active on the IGBT with a higher V_{CE}. Hence, the calibration of the V_{CE} reference signal depends on IGBT characteristics, AVC gate drive parameters, and CCL parameters in the IGBT turn-off. These factors determine the average characteristics of the IGBT turn-off, e.g. the initial MOS gate discharging, the fast

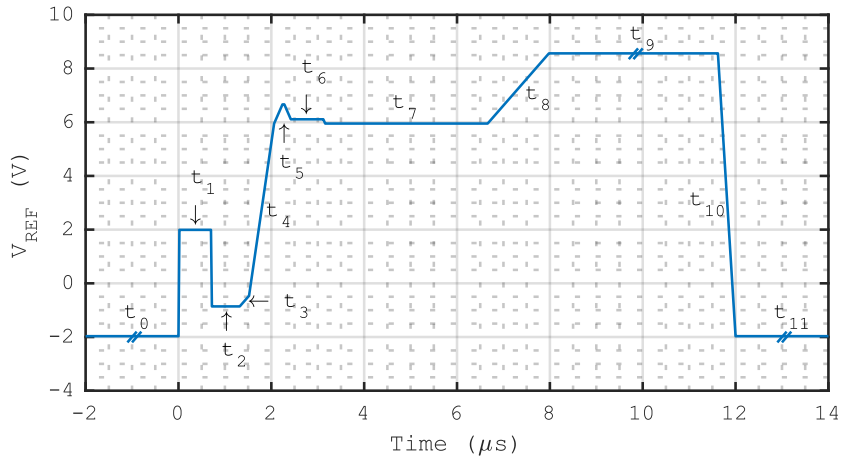


Figure 5.3: Redesigned reference signal for the direct active V_{CE} sharing regulation.

V_{CE} rising, the V_{CE} overshoot, and the tail current. These characteristics provide predictions of the average V_{CE} and I_C trajectories in the IGBT turn-off for calibrating the V_{CE} reference signal. Here, as only to demonstrate the key principles of the active V_{CE} sharing regulation, the V_{CE} reference signal is calibrated manually. The V_{CE} reference signals in this thesis are for typical operating conditions of modern FS IGBTs without punch-through of the depletion region to the N buffer. Automatic calibration of the V_{CE} reference signal and V_{CE} reference signals for other operating conditions are intended for future research.

The V_{CE} reference signal calibrated for the experiments in this chapter, Figure 5.3, uses three control stages by the segments t_1 to t_7 for all the IGBT turn-off stages with improvements upon the V_{CE} reference signal in [180]. In the V_{CE} reference signal here, the segment(s) t_1 to t_7 are for the turn-off, t_8 and t_9 are for the off-state, t_{10} is for the turn-on, and t_{11} and t_0 are for the on-state. The t_1 to t_9 are triggered by an IGBT turn-off instruction signal, and the t_{10}, t_{11}, and t_0 are triggered by an IGBT turn-on instruction signal. Since the IGBT turn-on is not part of the focus of this thesis, only a simple ramp is used for the t_{10}.

The timings and the voltages of the t_1 to t_8 and t_{10} shown in Figure 5.3 are the actual values calibrated for the experiments of the direct active V_{CE} sharing regulation in this chapter. The voltages of the t_0, t_9, and t_{11} shown in Figure 5.3 are also the actual values used, but the timings of the t_0, t_9, and t_{11} are controlled by the central signal generator and are longer in the actual experiments. The V_{CE} reference signal shown in Figure 5.3 is calibrated for demonstrating the key principles of the direct active V_{CE} sharing regulation in this chapter, which is not intended for industrial use.

The on-state driving in the t_{11} and t_0 is achieved by setting a negative plateau that saturates the AVC gate drive at its on-state driving voltage for $V_{FB} = 0$ V. Similarly, the off-state driving in the t_9 is achieved by setting a positive plateau that saturates the AVC gate drive at its off-state driving voltage for the V_{FB} of the predicted average off-state V_{CE}.

5.2.4.1 Low-Loss Preconditioning Stage

For the turn-off, the first control stage in the V_{CE} reference signal is a preconditioning stage that consists of two segments, the t_1 and t_2 as shown in Figure 5.3, designed to accommodate the timing difference in the initial discharging of the IGBT MOS gate from the on-state level to the

V_{GE} controlled active region. The general concept of the preconditioning stage here is similar to those in [204] and [180] with consideration of minimising the losses produced in the preconditioning stage.

The segment t_1 uses a positive plateau to set the gate driving output to its minimum negative voltage for shortening the initial gate discharging period. The segment t_2 uses a negative plateau calibrated to set the gate driving output to the V_{GE} that provides the minimum ($V_{GE} - V_{TH}$) required to operate the IGBT in the quasi-saturation region at the on-state load current. Ideally, the initial gate discharging in the t_1 shifts the operating point of the IGBT to the quasi-saturation region, but not into the V_{GE} controlled active region. Hence, the calibration of the t_1 and t_2 depends on the IGBT transfer characteristics, the gate drive circuit, and the on-state load current. The timing difference in the initial gate discharging between the IGBTs accumulated in the t_1 is mitigated in the t_2, where the synchronisation of the IGBTs in the quasi-saturation region can minimise the losses produced compared with those of the preconditioning stage in [180].

5.2.4.2 Differential V_{CE} Sharing Regulation in the Fast V_{CE}-I_C Transient

After the synchronisation in the t_2, for the fast V_{CE}-I_C transient the V_{CE} reference signal consists of three segments, the t_3 to t_5 as shown in Figure 5.3. To initiate the fast V_{CE}-I_C transient, the t_3 uses a slow rising ramp to drive the V_{GE} from the synchronisation level in the t_2 towards the V_{GE} controlled active region in a moderated manner. Such a slow ramp avoids saturating the op-amps in the AVC circuit or the driving stage and allows the V_{GE} to follow the V_{GG} more closely through the quasi-saturation region. With the preparation in the t_3, the following t_4 can drive the IGBTs rapidly through the V_{GE} controlled active region with a reduced timing difference.

For the fast V_{CE} rising, the t_4 uses a fast-rising ramp that is related to a linearised prediction of the average V_{CE} trajectory of the IGBTs in this turn-off stage. The V_{CE} reference signal in the t_4 is designed to benefit from the highly similar electric field gradients in the depletion regions of the IGBTs arising from the same I_C in this turn-off stage to assist the V_{CE} sharing regulation. Since the differential V_{CE} sharing regulation is only active on the IGBT with a higher V_{CE}, for the V_{CE} reference signal calibration a small safety margin is added to the predicted average V_{CE} trajectory to avoid instability caused by the phase lag of the AVC loop. The V_{CE} reference signal in the t_4 is designed to keep the V_{GE} between the V_{TH} and zero under evenly distributed V_{CE} sharing, which enables quick responses of the IGBT to the control loop.

For the V_{CE} overshoot, the t_5 uses a cap that closely traces the predicted V_{CE} overshoot with a reduced safety margin. In uncontrolled turn-off, the V_{CE} divergence often reaches a local maximum during the V_{CE} overshoot. The t_5 is designed to regulate this local maximum of the V_{CE} divergence and the difference in the depletion progress for improving the V_{CE} sharing in the tail time, although the actual effect varies depending on the V_{CE} diverging factors.

5.2.4.3 Differential V_{CE} Sharing Regulation in the Tail Time

In uncontrolled turn-off, the main V_{CE} divergence in terms of magnitude often develops in the tail time. Following the t_5, for the tail time the V_{CE} reference signal consists of two segments, the t_6 with a short clamp followed by the t_7 with a long and slightly lower clamp as shown in Figure 5.3.

For the early tail time, the short clamp in the t_6 is set to accommodate the slightly higher V_{CE} compared with the predicted average off-state V_{CE} due to the stray inductance in the CCL as the early tail current decays. In the t_6, due to the phase lag of the AVC loop, a clamp in the V_{CE} reference signal calibrated to the predicted average V_{CE} may cause V_{CE} undershoot during V_{CE} clamping, where the other IGBT in series may be forced into undesirable V_{CE} clamping. This situation in the worst-case scenario will cause V_{CE} oscillation and/or simultaneous V_{CE} clamping on both the IGBTs, where the I_C will rise undesirably. Hence, a small safety margin is included above the predicted average V_{CE} in the t_6. If the V_{CE} divergence is inadequate to quickly trigger the V_{CE} regulation in the t_6, the V_{GE} will be near the V_{TH} to reduce the response time of the IGBT in the following t_7.

For the late tail time, the long clamp in the t_7 regulates the V_{CE} sharing continuously towards the predicted average off-state V_{CE}. Since the internal differences between the IGBTs are reduced in the previous V_{CE} sharing regulation process, the t_6 and t_7 only needs to cover part of the tail time until the remaining differences between the IGBT devices after the V_{CE} sharing regulation would not upset the regulated V_{CE} sharing to a significant extent. Similar to the t_6, a small safety margin is included in the t_7 to avoid V_{CE} oscillation and/or simultaneous V_{CE} clamping on both the IGBTs. Hence, a slight but self-stabilising V_{CE} divergence may exist after the t_7 depending on the remaining differences between the IGBT devices.

For the following off-state, first in the t_8 a slow rising ramp gradually removes the previous clamp without producing a significant gate current. In the t_9, a plateau is set to saturate the driving stage of the AVC gate drive at the off-state driving voltage for a secure IGBT off-state.

5.3 Experiments of the Direct Active V_{CE} Sharing Regulation

5.3.1 Experiment Setup

The experiments of the direct active V_{CE} sharing regulation use a basic boost converter circuit as shown in Figure 5.4. In this circuit, two FS IGBTs in series are tested as the main switch using the double pulse method in [172], which enables testing power devices without high throughput power. The two IGBTs of the same model rated 1700 V and 650 A each are connected directly in series within a half-bridge module, Fuji Electric 2MBI650VXA-170E-50, without any snubber component attached except for the internal anti-parallel FWDs packaged in the same module.

The test rig for the experiments in this chapter is shown in Figure 5.5 and Figure 5.6. In this chapter, HS denotes the Higher electric potential Side (HS), and LS denotes the Lower electric potential Side (LS). The base signal generator provides a low frequency base signal to the double pulse signal generator, in which the base signal is converted into a double pulse signal. This double pulse signal is distributed to the AVC gate drives as the instruction signal for triggering V_{CE} reference signal generation.

In the experiment setup, for safety considerations, the average off-state V_{CE} of the IGBTs is set to approx. 600 V, only slightly higher than one third of the rated maximum V_{CE} of one IGBT. This is to ensure that in the case of a fault in an AVC gate drive where only one IGBT

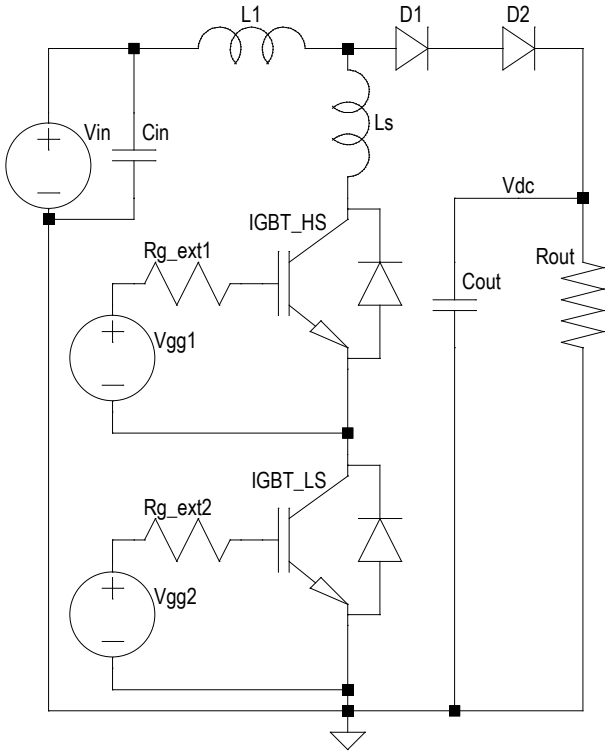


Figure 5.4: Boost converter circuit for the demonstration of the direct active V_{CE} sharing regulation.

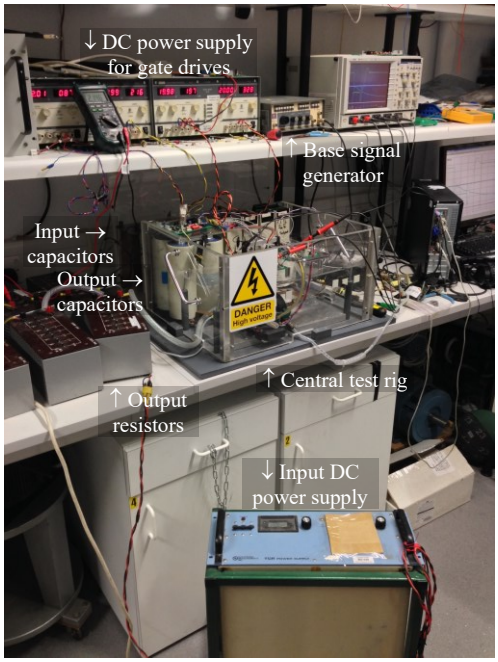


Figure 5.5: Test rig for the demonstration of the direct active V_{CE} sharing regulation.

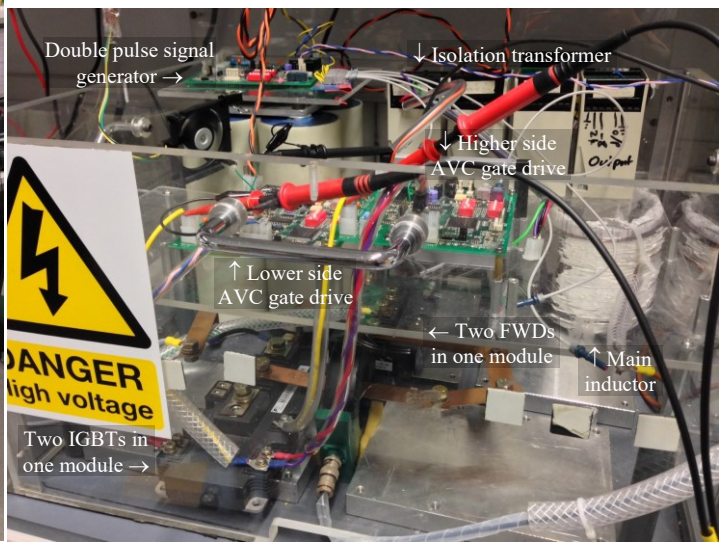


Figure 5.6: Central test rig for the demonstration of the direct active V_{CE} sharing regulation.

remains operational for switching, either IGBT can still remain within the RBSOA at a V_{DC} of approx. 1200 V. Limited by the specifications of the test rig available for the experiments, the IGBT load current for the IGBT turn-off is approx. 65 A.

5.3.2 V_{CE} Reference Signal Generated on the AVC Gate Drive

The measured V_{CE} reference signal generated by the FPGA and the DAC on the AVC gate drive under zero-input of the boost converter circuit is shown in Figure 5.7, and the segments for the turn-off V_{CE} sharing regulation is shown in Figure 5.8. The segments indicated in Figure 5.7 and Figure 5.8 correspond to those shown in Figure 5.3 and discussed in section 5.2.4. In a test

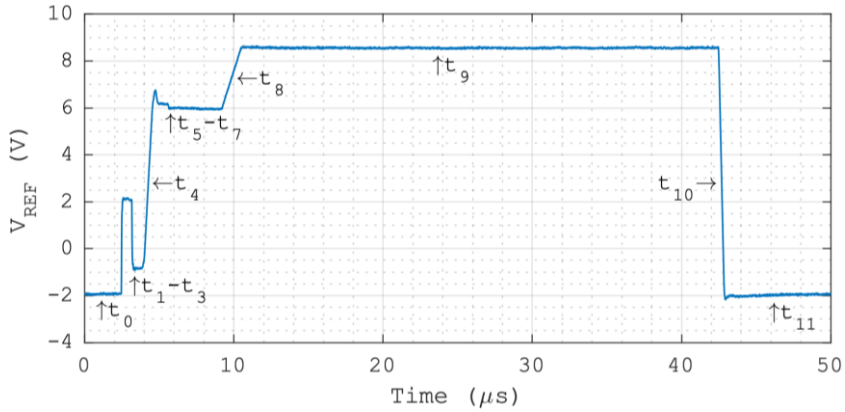


Figure 5.7: Redesigned reference signal for the demonstration of the direct active V_{CE} sharing regulation.

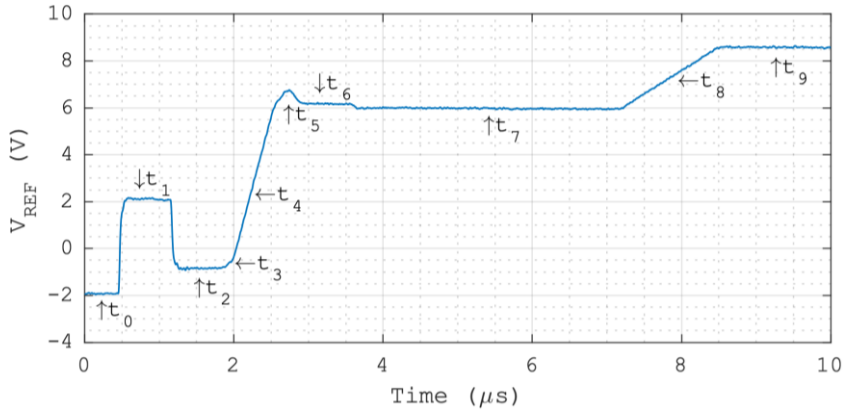


Figure 5.8: Segments of the redesigned reference signal for the direct turn-off V_{CE} sharing regulation.

cycle, excluding the preconditioning stage and the fast V_{CE}-I_C transient, the nominal IGBT off-state is approx. 37.5 µs, which is limited by the main inductor and the high conversion ratio of the boost converter circuit. The boost converter circuit is configured to operate in discontinuous mode at a high conversion ratio, which results in a considerable decrease in the main inductor current during the IGBT off-state in a test cycle. Hence, a considerable decrease in the IGBT load current is observed after the IGBT off-state.

The experiments here in each test group use the same V_{CE} reference signal and are sampled at different times during a continuous testing period with unchanged control of the circuit input conditions, unless specified otherwise. The features of the experiments are captured to an 8-bit resolution with a 2 ns sampling interval by a LeCroy LT344L oscilloscope.

5.3.3 V_{CE} Divergence in Uncontrolled IGBT Turn-Off

First for comparison, the V_{CE} divergence in uncontrolled IGBT turn-off, with the direct active V_{CE} sharing regulation disabled, is tested using hard-switched IGBT turn-off in the same test circuit. The hard-switched IGBT turn-off is emulated by the AVC gate drive using a step transition from the on-state level to the off-state level in the V_{CE} reference signal to sharply switch the AVC gate drive from its on-state driving voltage to its off-state driving voltage. Therefore, this emulated IGBT turn-off is effectively hard-switched and uncontrolled. For safety considerations, in this test of uncontrolled IGBT turn-off, the V_{DC} for the two IGBTs is 1000 V, and the IGBT load current to be switched at the IGBT turn-off is approx. 55 A. Due to the use of the AVC gate drives, the IGBT turn-off here is subject to the relative timing jitter between the AVC gate drives.

A typical example of the uncontrolled IGBT turn-off with large V_{CE} divergence is shown in Figure 5.9. As the IGBT package here only allows the I_C to be measured at the 'C' terminal of the IGBT package, the measured 'C' terminal current $I_{C,PKG}$ includes the current through the anti-parallel FWD inside the IGBT package, which are in off-state and without high-level excess carriers during the IGBT turn-off. Under these conditions, the current through the anti-parallel FWD is significantly smaller than the I_C of the IGBT. Therefore, during the IGBT turn-off, the measured $I_{C,PKG}$ is close to the I_C of the IGBT. The $V_{CE,Diff.}$ is defined as ($V_{CE,LS} - V_{CE,HS}$) here. As the turn-off and the turn-on of the IGBTs are triggered independently, the relative timing jitter between the AVC gate drives at the turn-off may change at the following turn-on and lead to an opposite V_{CE} diverging situation.

In this example, the V_{CE} divergence has a rapid but small increase at the beginning of the fast V_{CE} rising and continues to increase at a moderate rate as the total V_{CE} rises to the V_{DC}. The V_{CE} divergence decreases slightly during the V_{CE} overshoot as the $I_{C,PKG}$ falls rapidly. During the fast V_{CE}-I_C transient, the V_{CE} divergence remains small. During the tail time, the V_{CE} divergence increases again at a moderate rate in approx. the first 10 µs and continues to increase in the following 10 µs with a significantly lower increase rate. The total V_{CE} diverging period under the circuit conditions here exceeds 20 µs. Before the following IGBT turn-on, the $V_{CE,Diff.}$ reaches a maximum of approx. 320 V, 32% of the 1000 V V_{DC}, which would increase with the V_{DC} as discussed previously in section 4.2.5. The V_{CE} diverging situation in the following turn-on is not fully dependent on this turn-off event. At the following turn-on, the $V_{CE,LS}$ starts to fall first, causing the $V_{CE,HS}$ to rise temporarily and the $V_{CE,Diff.}$ to become negative during the turn-

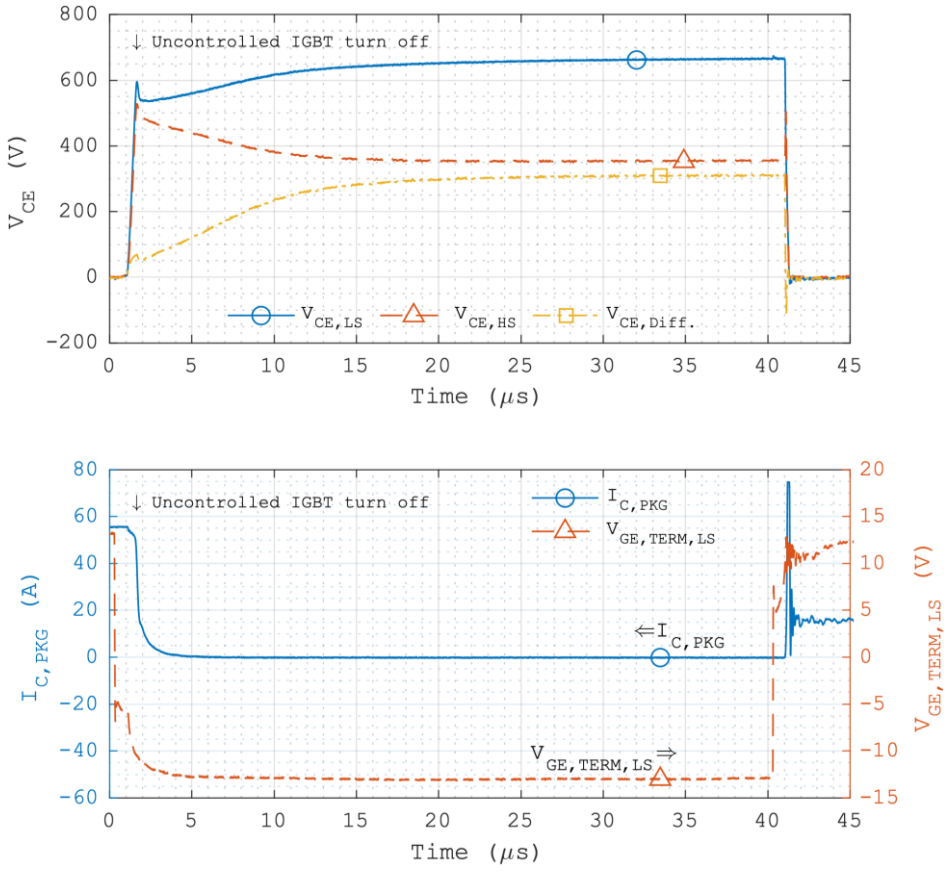


Figure 5.9: Uncontrolled turn-off of two IGBTs in series with large V_{CE} divergence.

on. A spike and oscillation in the $I_{C,PKG}$ are observed at the turn-on, which is caused by the reverse recovery current of the FWD branch in the CCL.

The $V_{GE,TERM,LS}$ refers to the gate-emitter voltage measured at the package terminals of the lower electric potential side IGBT. The internal gate resistance inside the IGBT package is 1.75 Ω, and the external gate resistance on the AVC gate drive is 1 Ω. The IGBT module used here only allows measurement at the package terminals, and the gate terminal in the gate driving path is between the internal gate resistance and the external gate resistance. Hence, the measured $V_{GE,TERM,LS}$ here is different from the V_{GE} of the IGBT chips.

The detailed features of the uncontrolled turn-off in Figure 5.9 is shown in Figure 5.10. A significant initial delay is observed between the V_{CE} trajectories at the beginning of the fast V_{CE} rising, after which the V_{CE} divergence continues to increase at a moderate rate as the total V_{CE} rises to the V_{DC}. As identified in Figure 5.9, the V_{CE} divergence decreases temporarily as the $I_{C,PKG}$ falls rapidly in the V_{CE} overshoot. This V_{CE} diverging feature is found in the previous simulation results that involve a delay in the IGBT MOS channel cut-off, e.g. the simulation of an IGBT gate driving delay shown in section 3.5.1.

Despite the difference between the terminal V_{GE} and the chip V_{GE} due to the internal gate resistance, as here the AVC gate drive output is quickly saturated at its off-state driving voltage, the terminal V_{GE} can be used to estimate the timings of the chip V_{GE} during the hard-switched turn-off. With given internal and external gate resistances, when the chip V_{GE} starts to fall at the end of the Miller plateau, the terminal V_{GE} starts to fall accordingly at the end of a similar

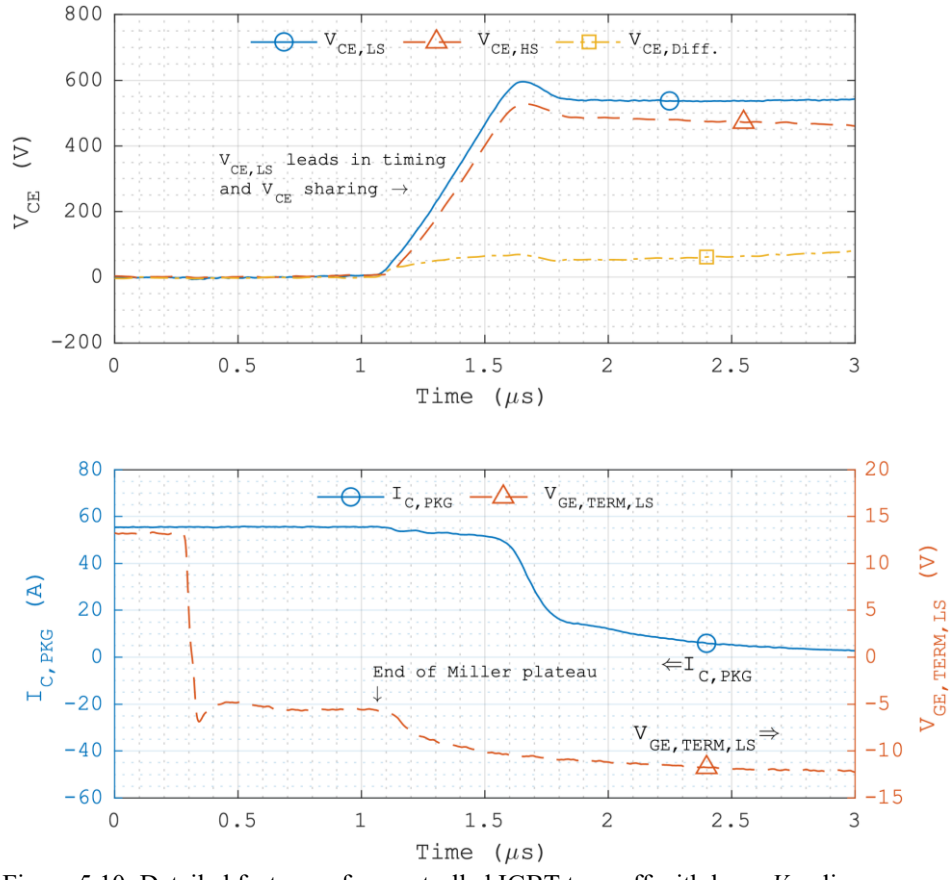


Figure 5.10: Detailed features of uncontrolled IGBT turn-off with large V_{CE} divergence.

plateau, which is aligned with the beginning of the fast V_{CE} rising, Figure 5.10. Hence, here the IGBT MOS channel is cut off very early in the fast V_{CE} rising due to the low gate resistance.

The relative timing jitter between the AVC gate drives in the V_{CE} reference signal for turn-off is shown in Figure 5.11 using colour graded persistence processed by the oscilloscope of 20 s of an edge in the turn-off V_{CE} reference signal. The red trace inside is the edge in the lower side V_{CE} reference signal used for triggering, which is positioned to cross the central intersection of the axes and is saturated at a red colour as it remains nearly unchanged. The blue/purple part is the distribution of the corresponding edge in the higher side V_{CE} reference signal. By measurement on the time axis at the zero-voltage level, the higher side V_{CE} reference signal is distributed between a 25 ns lead and a 15 ns lag relative to the lower side V_{CE} reference signal. This total range of 40 ns agrees with the relative timing jitter of ±20 ns maximum discussed in section 5.2.3. The 5 ns average offset in this distribution suggests a fixed 5 ns lead possibly in the transmission of the instruction signal regarding the higher side AVC gate drive.

While maintaining the respective optical fibres for the high and lower side IGBTs, exchanging only the two AVC gate drives produces a closely matched result of the relative timing jitter in the V_{CE} reference signal. While maintaining the respective AVC gate drives for the high and lower side IGBTs, exchanging only the optical fibres produces an opposite result of the relative timing jitter in the V_{CE} reference signal, where the lower side V_{CE} reference signal has an average 5 ns lead. This suggests that the components of the AVC gate drives do not have significant differences to affect the average offset of this relative timing jitter in the V_{CE} reference signal. Therefore, the average offset found in this relative timing jitter is caused by the optical fibres, possibly due to a difference in the light quality of the optical fibre output.

In Figure 5.10, the $V_{CE,HS}$ has a lower dV_{CE}/dt rate compared with that of the $V_{CE,LS}$ during the fast V_{CE} rising. The detailed features of a typical example of the uncontrolled turn-off with small V_{CE} divergence is shown in Figure 5.12, sampled at a different time during a continuous

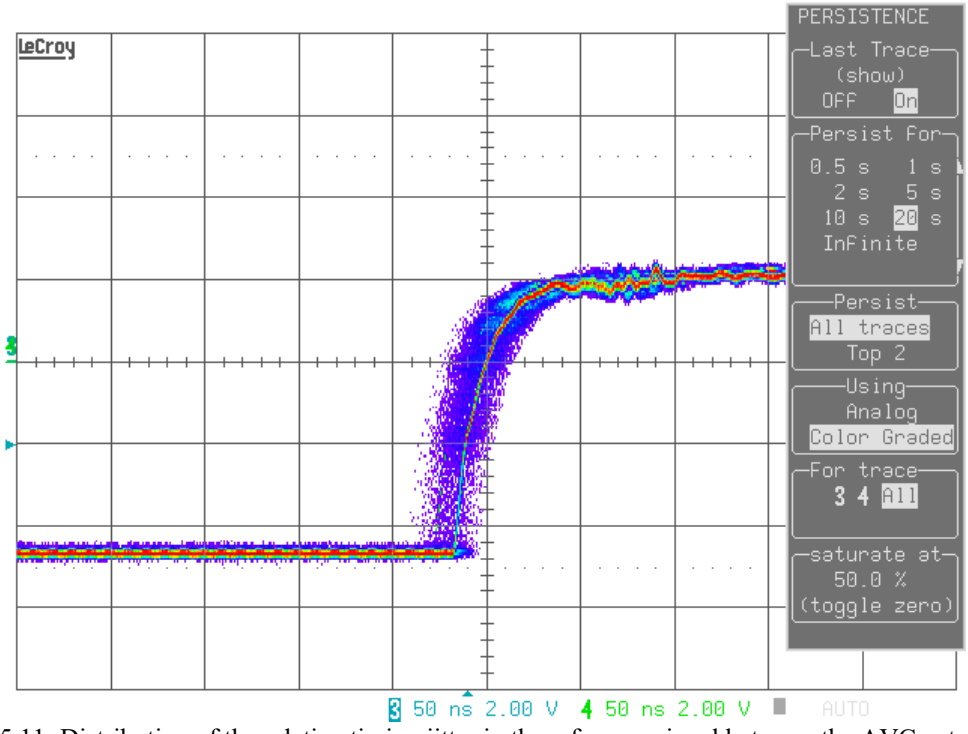


Figure 5.11: Distribution of the relative timing jitter in the reference signal between the AVC gate drives.

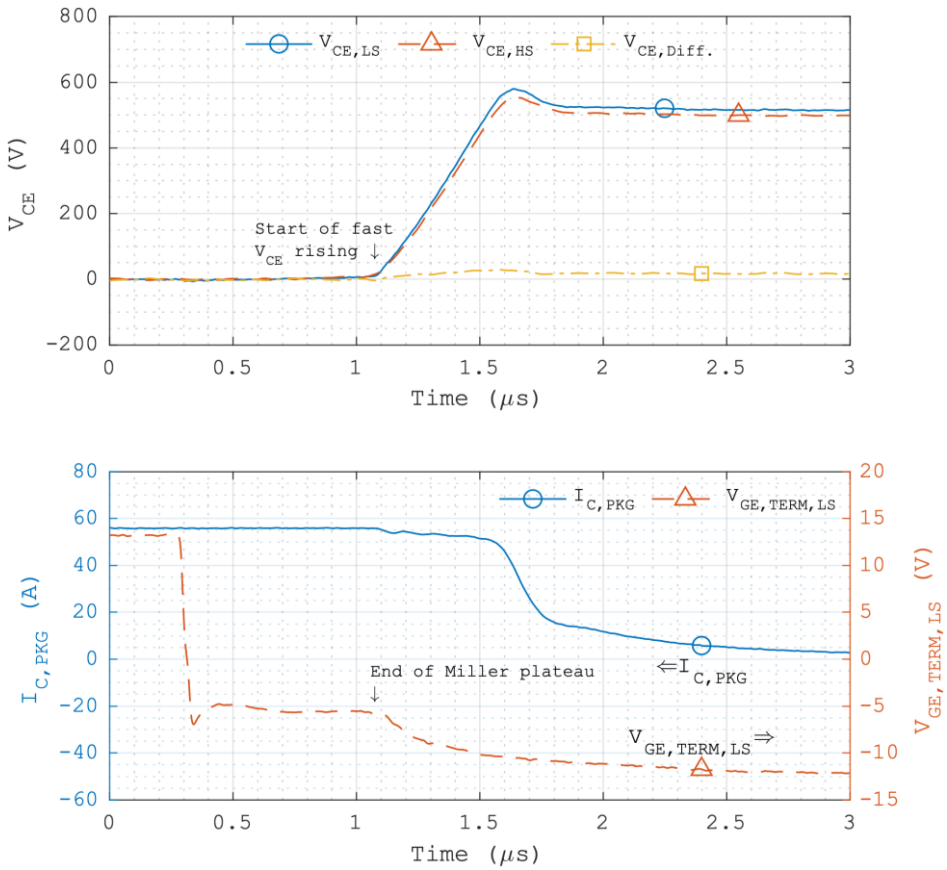


Figure 5.12: Detailed features of uncontrolled IGBT turn-off with small V_{CE} divergence.

testing period under unchanged circuit input conditions as those of the example shown in Figure 5.10. Despite a slight lead in the fast V_{CE} rising, the $V_{CE,HS}$ has a lower dV_{CE}/dt rate compared with that of the $V_{CE,LS}$ during the fast V_{CE} rising. This V_{CE} diverging feature is found in the previous simulation results that involve a difference in the on-state excess carrier concentration, e.g. the simulation of a higher P emitter doping profile in one IGBT shown in section 3.5.2.

5.3.4 Demonstration of the Direct Active V_{CE} Sharing Regulation in the Fast V_{CE}-I_C Transient

Figure 5.13 shows a typical example of the direct active V_{CE} sharing regulation in the preconditioning stage and the fast V_{CE}-I_C transient against strong V_{CE} diverging factors. The V_{DC} is 1200 V, and the IGBT load current to be switched at the IGBT turn-off is 65 A.

The preconditioning stage here avoids significant losses compared with those in the previous researches [178]–[181] while providing comparable synchronisation effects for the IGBTs. The duration of the t_1 used here is extended to emphasise the differences between the IGBTs and the synchronisation process in the following t_2. Therefore, temporary V_{CE} rises in both the IGBTs are observed as indicated in Figure 5.13, which can be mitigated by shortening the t_1 in the V_{CE} reference signal to further reduce losses. In this temporary V_{CE} rise, the lower side IGBT V_{CE} rises first with a higher magnitude, while the higher side IGBT V_{CE} rises later with a lower magnitude. This feature agrees with the lower side IGBT leading in the fast V_{CE} rising in the previous uncontrolled IGBT turn-off shown in Figure 5.10. The $V_{GE,TERM,LS}$ remains stable at approx. 8.75 V in the late t_2.

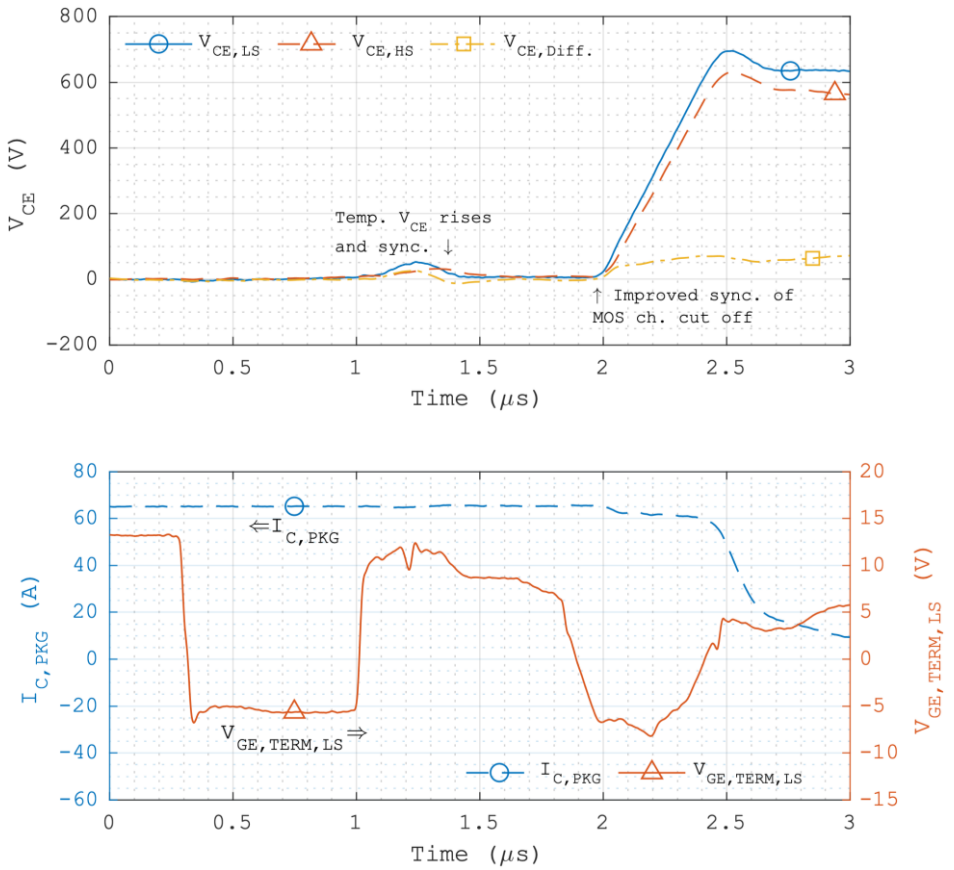


Figure 5.13: The direct active V_{CE} sharing regulation against strong V_{CE} diverging factors in the redesigned preconditioning stage and the fast V_{CE}-I_C transient.

From approx. 1.65 µs to 1.85 µs in Figure 5.13, a slow decrease in the $V_{GE,TERM,LS}$ is observed, which is related to the t_3 in the V_{CE} reference signal that prepares the IGBTs for the fast V_{CE} rising. Despite the differences in the temporary V_{CE} rise indicating some differences between the IGBTs, the timing consistency of the MOS channel cut-off indicated by the beginning of the fast V_{CE} rising is improved after the preconditioning stage compared with the uncontrolled turn-off result with strong V_{CE} diverging factors.

The V_{CE} divergence starts to increase at the beginning of the fast V_{CE} rising. Due to the integer limits in the FPGA programming to achieve the 20 ns clock cycle and the 8-bit DAC resolution, in the V_{CE} reference signal only a very few combinations of rising rates and durations are available for the fast V_{CE} rising considering the V_{CE} sharing regulation for the following V_{CE} overshoot. Consequently, with the safety margin in the V_{CE} reference signal, here the V_{CE} sharing regulation is not active during the fast V_{CE} rising. Although increases with the $V_{CE,Diff.}$ as expected, the $V_{GE,TERM,LS}$ remains below the V_{TH} during the fast V_{CE} rising. Further reducing the safety margin would cause the V_{CE} reference signal to force both the IGBTs undesirably into the V_{GE} controlled active region late in the fast V_{CE} rising under the circuit conditions here. A small decrease in the $V_{CE,Diff.}$ is observed in the V_{CE} overshoot. The $V_{CE,Diff.}$ starts to increase again at the beginning of the tail time before intervened by the active V_{CE} sharing regulation.

Figure 5.14 shows a typical example of the direct active V_{CE} sharing regulation in the preconditioning stage and the fast V_{CE}-I_C transient in an opposite V_{CE} diverging situation compared with that in the example shown in Figure 5.13. In the temporary V_{CE} rise, the lower side IGBT still leads with a higher magnitude, but the timing lead here is smaller compared with that shown

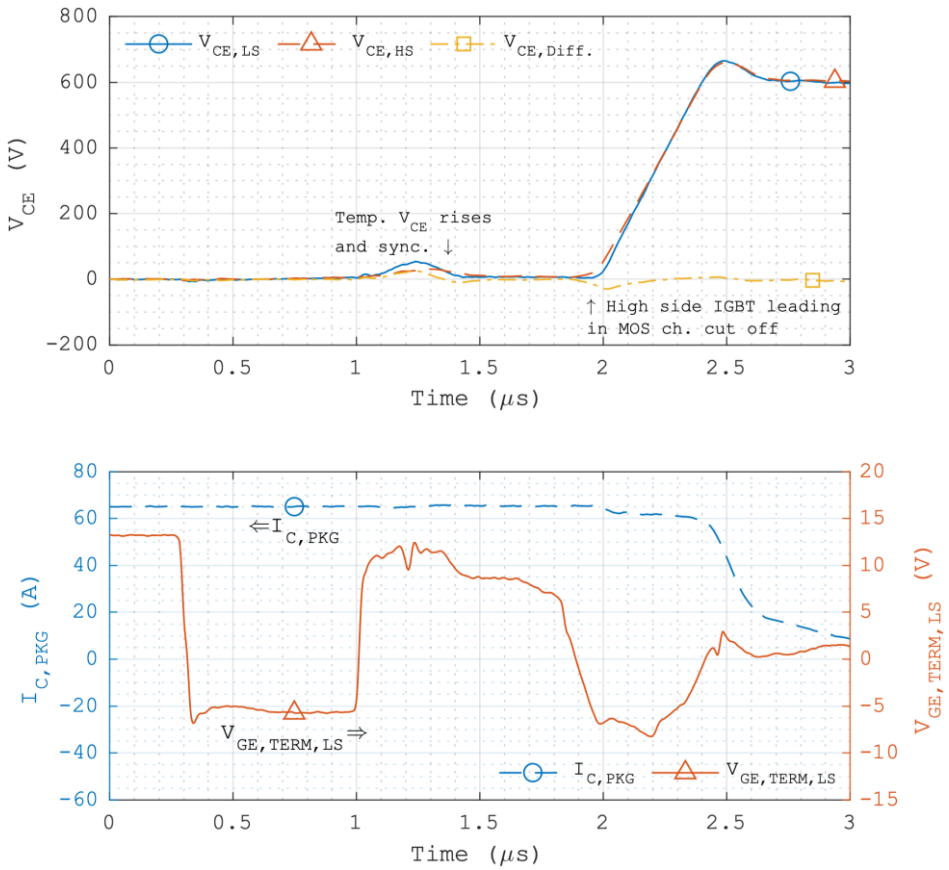


Figure 5.14: Preconditioning stage of direct active V_{CE} sharing regulation in an inverted V_{CE} diverging situation in fast V_{CE}-I_C transient.

in Figure 5.13. Also, the higher side IGBT has a timing lead at the beginning of the fast V_{CE} rising. Therefore, here the relative timing of the V_{CE} reference signal for the higher side IGBT shifted ahead compared with that shown in Figure 5.13. The higher side IGBT is still subject to a lower dV_{CE}/dt rate, which offsets its timing lead here in the beginning of the fast V_{CE} rising. The V_{CE} divergence decreases in the fast V_{CE} rising, and the V_{CE} sharing regulation is not active during the fast V_{CE} rising here due to the close V_{CE} sharing.

Summarising from the examples shown in Figure 5.13 and Figure 5.14, some effects of the fixed V_{CE} diverging factors can be mitigated by the redesigned preconditioning stage without producing significant losses. Both the operating frequency of the FPGA and the resolution of the DAC need to be increased to enhance the resolution and the precision of the V_{CE} reference signal for improving the adaptability of the V_{CE} reference signal to different IGBTs and circuit conditions. Also, synchronised clock sources for the FPGAs can significantly reduce the relative timing jitter in the V_{CE} reference signal to further improve the active V_{CE} sharing regulation.

5.3.5 Demonstration of the Direct Active V_{CE} Sharing Regulation in the Tail Time

Figure 5.15 shows the direct active V_{CE} sharing regulation in the tail time of the same example with strong V_{CE} diverging factors shown in Figure 5.13. After the V_{CE} overshoot, as the V_{CE} divergence increases in the tail time from approx. 2.7 µs, the $V_{GE,TERM,LS}$ is raised by the clamp in the t_6 of the V_{CE} reference signal. The $V_{GE,TERM,LS}$ starts to increase at 2.75 µs, and from 3 µs the V_{CE} divergence is limited to 73 V until the following t_7 of the V_{CE} reference signal, where the V_{CE} divergence is reduced.

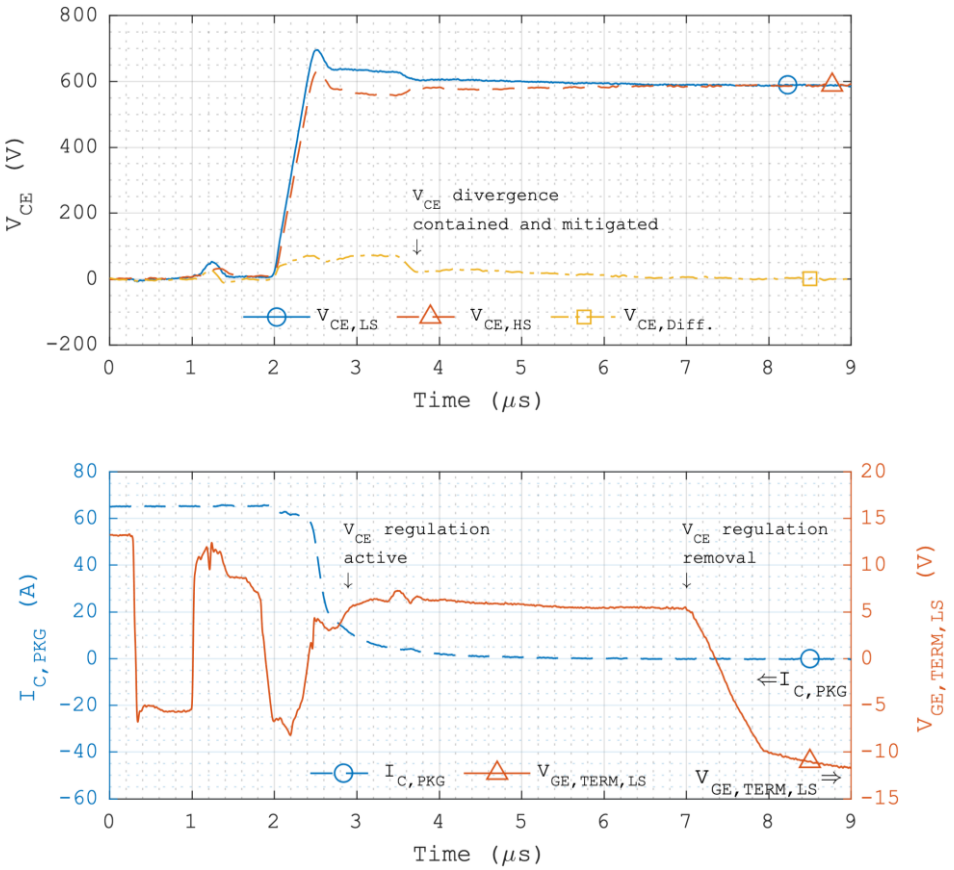


Figure 5.15: Direct active V_{CE} sharing regulation against strong V_{CE} diverging factors in tail time.

The small rise in the $V_{GE,TERM,LS}$ from 3.4 µs to 3.5 µs due to the lower clamp in the t_7 indicates the transition from the t_6 to the t_7. At 3.5 µs, the $V_{CE,LS}$ starts to decrease which significantly reduces the V_{CE} divergence, after which the $V_{GE,TERM,LS}$ falls back to the previous level with slight oscillation. In this process, the $I_{C,PKG}$ remains near level as the V_{CE} divergence decreases from 3.5 µs to 3.7 µs due to the MOS channel current in the lower side IGBT by the active V_{CE} sharing regulation.

In the rest of the t_7, the V_{CE} divergence is mitigated gradually, and the $V_{GE,TERM,LS}$ decreases slightly but remains above 5 V. This gradual V_{CE} sharing regulation process only requires a small MOS channel current and therefore the $V_{GE,TERM,LS}$ in this period is below the typical V_{TH} in the datasheet of 6.5 V at V_{CE} = 20 V, I_C = 650 mA, and 25 °C. For demonstration, here the t_6 and the following t_7 only cover the first 4.3 µs of the tail time, which is significantly shorter than the V_{CE} diverging period in the tail time of approx. 20 µs in a similar V_{CE} diverging situation shown in Figure 5.9. It is expected that under the circuit conditions here, after the t_7 the remaining differences between the IGBTs would not upset the regulated V_{CE} sharing to a significant extent. The removal of the V_{CE} sharing regulation is from 7 µs to 8 µs, indicated by the $V_{GE,TERM,LS}$ being driven towards the off-state driving voltage of the AVC gate drive.

Figure 5.16 shows a typical example of the direct active V_{CE} sharing regulation in the tail time against moderate V_{CE} diverging factors. Compared with the example shown in Figure 5.15 with strong V_{CE} diverging factors, here the V_{CE} divergence at the beginning of the fast V_{CE} rising at approx. 2 µs does not have a small and rapid initial increase, and the largest V_{CE} divergence reaches 50 V before mitigated in the t_7 of the V_{CE} reference signal. Also, here during the t_6, the

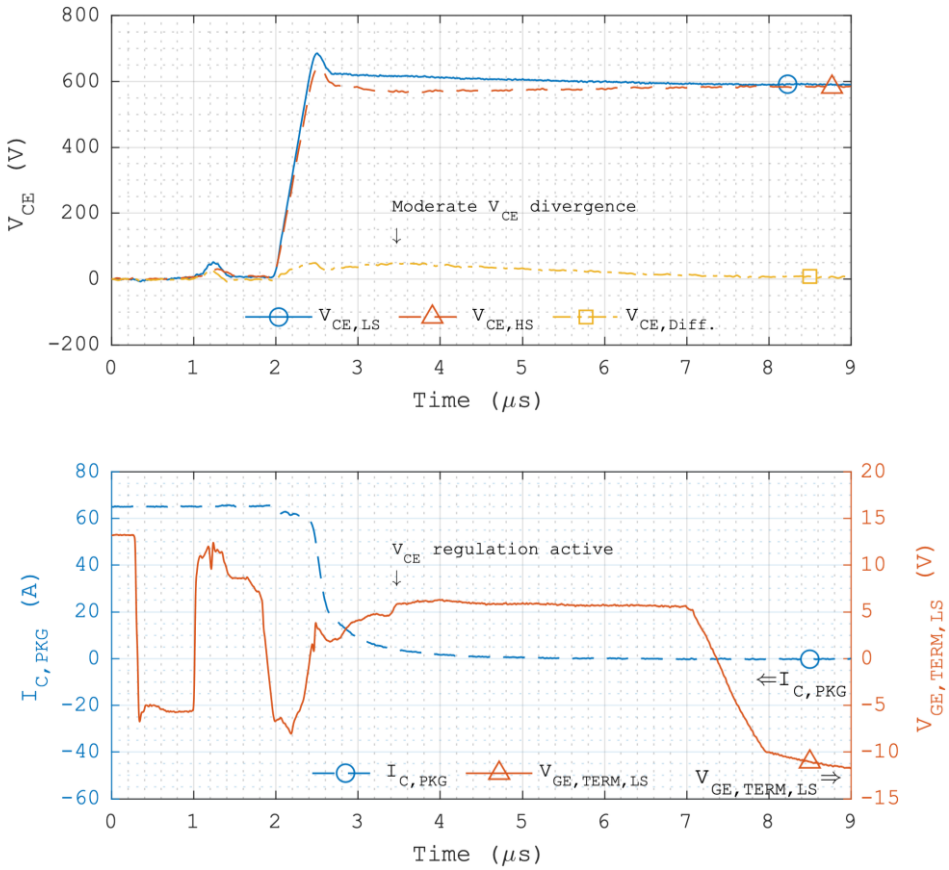


Figure 5.16: Direct active V_{CE} sharing regulation against moderate V_{CE} diverging factors.

$V_{GE,TERM,LS}$ remains below 5 V, indicating that the V_{CE} divergence is inadequate to quickly trigger the active V_{CE} sharing regulation.

In the t_7 as the clamp in the V_{CE} reference signal decreases, the $V_{GE,TERM,LS}$ increases and exceeds 5 V at 3.4 µs. From 3.6 µs the V_{CE} divergence is limited and mitigated gradually. The $V_{GE,TERM,LS}$ decreases slightly but remains above 5 V as the $V_{CE,Diff.}$ decreases. Similar to the previous example, such a gradual and steady V_{CE} sharing regulation process only requires a small MOS channel current, and therefore the $V_{GE,TERM,LS}$ in this period is below 6.5 V and the decay of the tail current remains steady in this process. The removal of the V_{CE} sharing regulation is from 7 µs to 8 µs, indicated by the $V_{GE,TERM,LS}$ being driven towards the off-state driving voltage of the AVC gate drive.

Figure 5.17 shows the direct active V_{CE} sharing regulation in the tail time of the same example shown in Figure 5.14 that features an opposite V_{CE} diverging situation compared with those in the examples shown in Figure 5.15 and Figure 5.16. Here, the V_{CE} divergence from the beginning of the fast V_{CE} rising at approx. 2 µs is basically of $V_{CE,LS} < V_{CE,HS}$, and therefore the differential active V_{CE} sharing regulation is triggered on the higher side IGBT. The higher side IGBT has a timing lead in the beginning of the fast V_{CE} rising at approx. 2 µs, despite a lag in the previous temporary V_{CE} rise from 1 µs to 1.5 µs in the preconditioning stage. The V_{CE} divergence decreases during the fast V_{CE} rising due to the lower $dV_{CE,HS}/dt$ rate of the higher side IGBT and fluctuates near zero during the V_{CE} overshoot. Limited by the specifications of the voltage probes available for the experiments, only the $V_{GE,TERM,LS}$ can be measured. In the fast

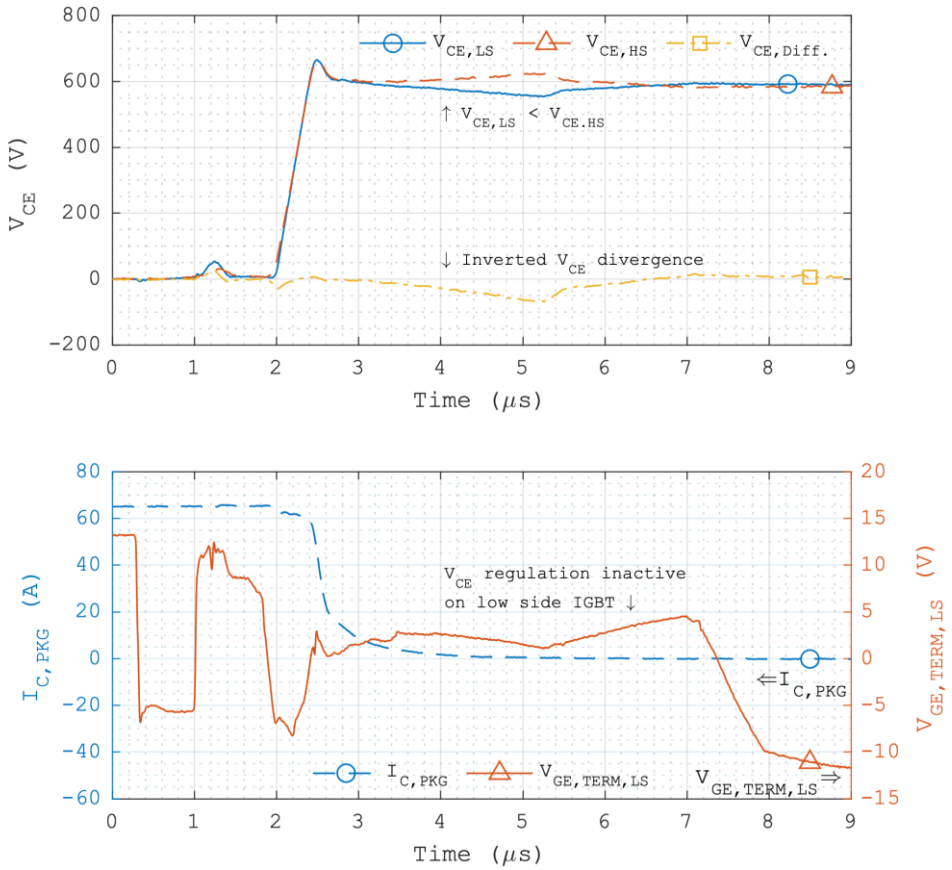


Figure 5.17: Direct active V_{CE} sharing regulation in an opposite V_{CE} diverging situation against strong V_{CE} diverging factors.

V_{CE}-I_C transient and the tail time, the $V_{GE,TERM,LS}$ remains below 5 V as the differential active V_{CE} sharing regulation is not triggered on the lower side IGBT.

In the tail time, the V_{CE} divergence of $V_{CE,LS} < V_{CE,HS}$ increases gradually at first. Due to the safety margin in the V_{CE} reference signal and the phase lag caused by charging/discharging the IGBT C_{GE}, here the active V_{CE} sharing regulation is not immediately effective on the higher side IGBT. The V_{CE} reference signal enters the t_7 at 3.4 µs, indicated by a slight increase in the $V_{GE,TERM,LS}$ as the clamp in the V_{CE} reference signal decreases. In the t_7, at first the $V_{GE,TERM,LS}$ is reduced as the $V_{CE,LS}$ decreases. The V_{CE} divergence reaches 68 V at 5.25 µs ($V_{CE,diff.}$ = -68 V as $V_{CE,LS} < V_{CE,HS}$) and then starts to decrease as the active V_{CE} sharing regulation becomes effective on the higher side IGBT. Consequently, the $V_{CE,LS}$ increases and the $V_{GE,TERM,LS}$ is raised but remains below 5 V.

Due to the phase lag of the AVC loop, slight over correction of the V_{CE} sharing is observed at 6.6 µs. Despite this over correction, the safety margin in the V_{CE} reference signal prevents the $V_{GE,TERM,LS}$ from exceeding 5 V and causing stability issues. The removal of the V_{CE} sharing regulation is from 7 µs to 8 µs, indicated by the $V_{GE,TERM,LS}$ being driven towards the off-state driving voltage of the AVC gate drive.

The three examples shown here are in three typical situations of the V_{CE} sharing regulation. In those examples, the direct active V_{CE} sharing regulation is effective with stable regulation processes, and oscillation is not observed during the removal of the V_{CE} sharing regulation. In the example shown in Figure 5.17, the phase lag caused by charging/discharging the IGBT C_{GE}

results in a lag in the V_{CE} sharing regulation process. Despite the slight over correction of the V_{CE} sharing, control instability is not observed due to the safety margin in the V_{CE} reference signal. The lag in the V_{CE} sharing regulation process can be reduced with a lower stray inductance in the gate driving path that ensures control stability when using a lower gate resistance and a higher gain in the AVC loop.

5.3.6 Long-Term Off-State V_{CE} Sharing after the Direct Active V_{CE} Sharing Regulation

For demonstration, here the t_6 and the following t_7 only cover the first 4.3 µs of the tail time, after which it is expected that under the circuit conditions here the remaining differences between the IGBTs would not upset the regulated V_{CE} sharing to a significant extent.

Figure 5.18 shows the long-term V_{CE} sharing in the IGBT off-state after the direct active V_{CE} sharing regulation of the same example shown in Figure 5.15 that features strong V_{CE} diverging factors. The IGBT off-state after the end of the V_{CE} sharing regulation as indicated in Figure 5.18 is approx. 33.3 µs from 7 µs to 40.3 µs.

At the end of the V_{CE} sharing regulation at 7 µs, the $V_{CE,Diff.}$ is reduced to near zero but not eliminated due to the safety margin in the V_{CE} reference signal. The $V_{CE,Diff.}$ is 4 V at 7 µs and decreases slightly afterwards. The $V_{CE,Diff.}$ reaches -4 V at 12 µs and decreases gradually to -9 V at the end of the IGBT off-state at 40.3 µs. This slight decrease of the $V_{CE,Diff.}$ is due to the small remaining differences between the IGBTs after the V_{CE} sharing regulation. As discussed previously in section 3.3.6, the long-term V_{CE} sharing in the IGBT off-state is self-stabilising,

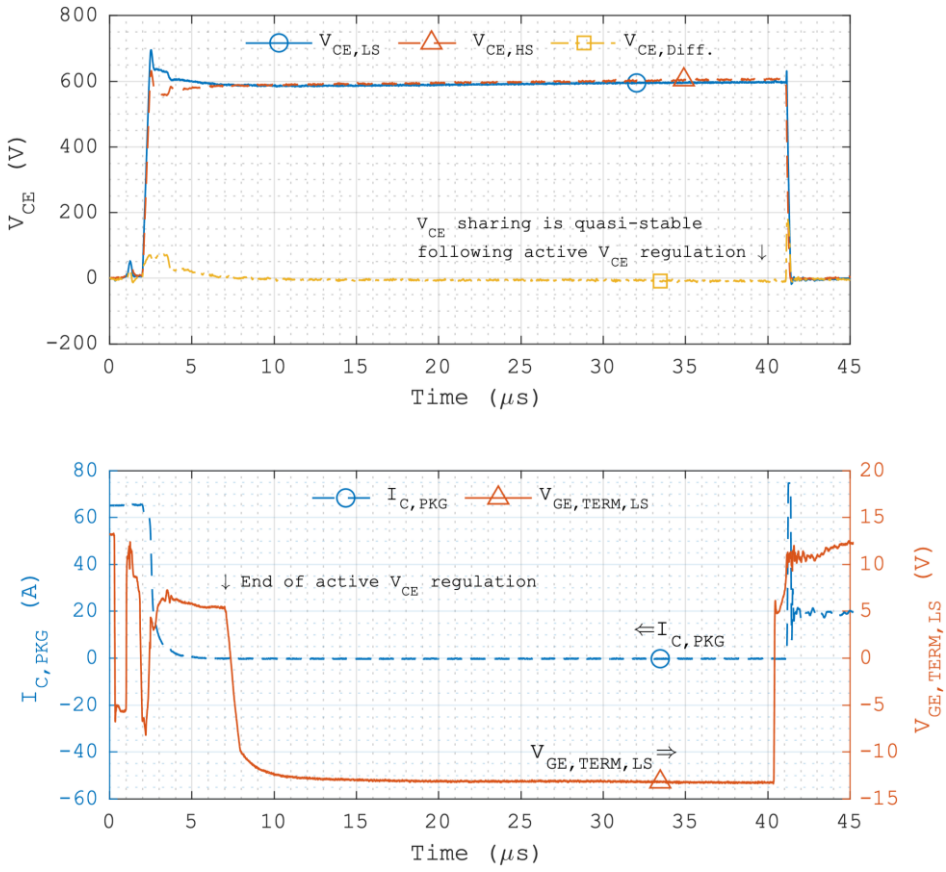


Figure 5.18: Long-term V_{CE} sharing in IGBT off-state following direct active V_{CE} sharing regulation against strong V_{CE} diverging factors.

although it may not reach an even distribution depending on the fixed differences between the IGBTs.

Here, the t_6 and the t_7 in the V_{CE} reference signal only cover the first 4.3 µs of the tail time. However, since the differences between the IGBTs are reduced during the V_{CE} sharing regulation process, this short regulation period compared with the V_{CE} diverging periods in the previous uncontrolled IGBT turn-off tests is still adequate to achieve quasi-static V_{CE} sharing in the following IGBT off-state. As discussed previously, the V_{CE} divergence in the following uncontrolled turn-on is not fully dependent on the V_{CE} diverging situation in this turn-off event and may be in an opposite V_{CE} diverging situation. Regarding the $I_{C,PKG}$, a spike followed by oscillation is observed in the following turn-on due to the reverse recovery current of the FWD branch in the CCL, which also causes simultaneous oscillation in the $V_{GE,TERM,LS}$.

Figure 5.19 shows the long-term V_{CE} sharing in the IGBT off-state after the direct active V_{CE} sharing regulation of the same example shown in Figure 5.16 that features moderate V_{CE} diverging factors. The initial V_{CE} divergence in the fast V_{CE}-I_C transient here is not as large as that in the example shown in Figure 5.18. At the end of the active V_{CE} sharing regulation at 7 µs, the V_{CE} divergence is reduced to near zero but not eliminated due to the safety margin in the V_{CE} reference signal. The $V_{CE,Diff.}$ is 11 V at 7 µs and decreases slightly afterwards. The $V_{CE,Diff.}$ reaches 3 V at 12 µs and decreases gradually to -1 V at the end of the following IGBT off-state at 40.3 µs. The long-term V_{CE} sharing here is also quasi-static and self-stabilising in the IGBT off-state after the V_{CE} sharing regulation.

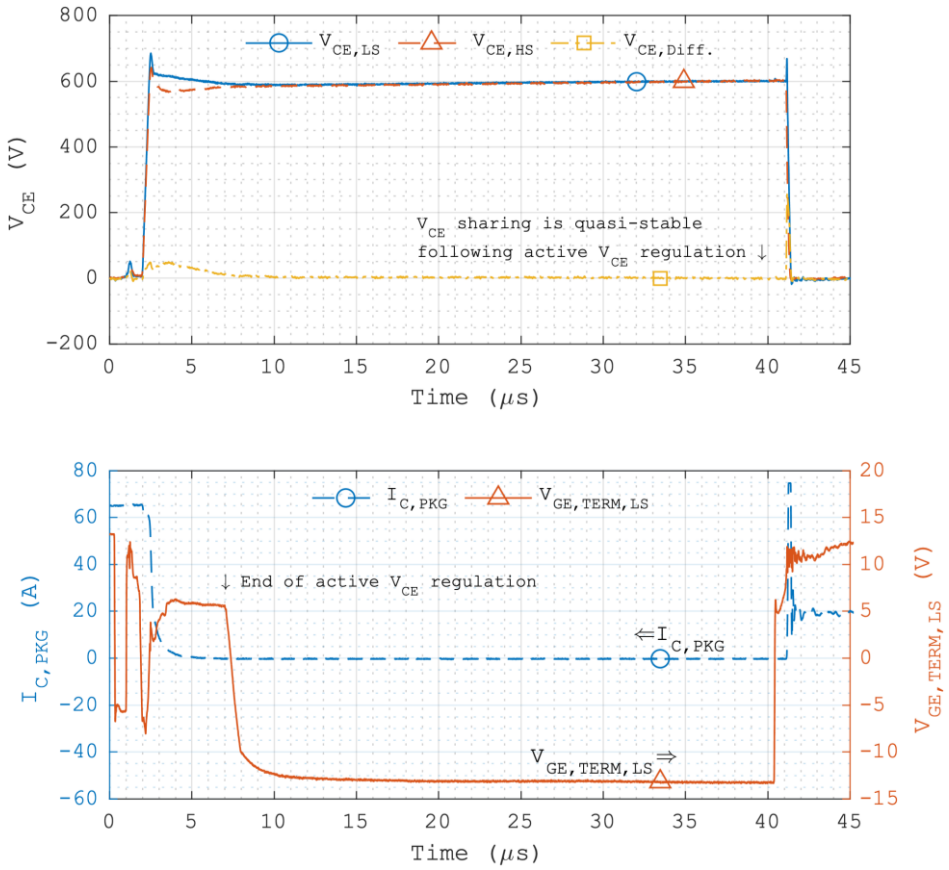


Figure 5.19: Long-term V_{CE} sharing in IGBT off-state following direct active V_{CE} sharing regulation against moderate V_{CE} diverging factors.

Figure 5.20 shows the long-term V_{CE} sharing in the IGBT off-state after the direct active V_{CE} sharing regulation of the same example shown in Figure 5.17 that features an opposite V_{CE} diverging situation compared with those in the examples shown in Figure 5.18 and Figure 5.19. Here, the V_{CE} divergence from the beginning of the fast V_{CE} rising at approx. 2 µs is basically of $V_{CE,LS} < V_{CE,HS}$, and therefore the differential active V_{CE} sharing regulation is triggered on the higher side IGBT. The lag caused by charging/discharging the IGBT C_{GE} delays the mitigation of the V_{CE} divergence and causes a slight over correction of the V_{CE} sharing. At the end of the active V_{CE} sharing regulation at 7 µs, the $V_{CE,Diff.}$ is 11 V due to the over correction and the phase lag of the AVC loop. Despite the triggering of the direct active V_{CE} sharing regulation on the higher side IGBT, the $V_{CE,Diff.}$ decreases slightly in the following IGBT off-state, similar to the examples shown in Figure 5.18 and Figure 5.19. The $V_{CE,Diff.}$ reaches -2 V at 12 µs and decreases gradually to -10 V at the end of the following IGBT off-state at 40.3 µs. The V_{CE} sharing here is quasi-static and self-stabilising in the IGBT off-state after the V_{CE} sharing regulation.

The three typical examples shown in this section all have similar slight decreases in the $V_{CE,Diff.}$ after the V_{CE} sharing regulation during the following IGBT off-state, regardless of the V_{CE} diverging situation and the IGBT on which the V_{CE} sharing regulation is triggered. Hence, those slight decreases in the $V_{CE,Diff.}$ after the V_{CE} sharing regulation are mainly caused by fixed differences between the IGBTs.

The $\Delta V_{CE,Diff.}$ after the V_{CE} sharing regulation is similar in the first two examples, in which the V_{CE} sharing regulation is triggered on the lower side IGBT, despite differences in the $V_{CE,Diff.}$ values. In the third and opposite V_{CE} diverging example, the $\Delta V_{CE,Diff.}$ after the V_{CE} sharing

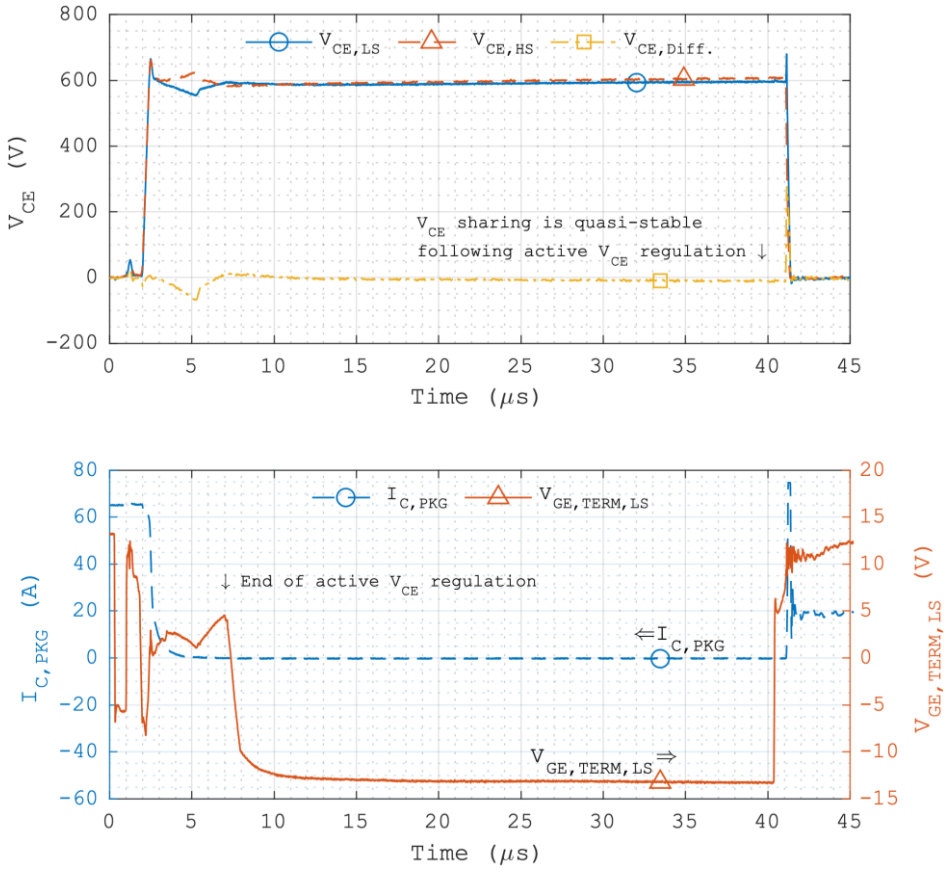


Figure 5.20: Long-term V_{CE} sharing in IGBT off-state following direct active V_{CE} sharing regulation against inverted V_{CE} divergence with strong V_{CE} diverging factors.

regulation is higher. Considering the V_{CE} sharing regulation process in the tail time, in the IGBT with a rising V_{CE} the depletion region expands into the previously undepleted part of the N base, where electrons are transported towards the P emitter, inducing additional hole diffusion from the P emitter. These additional holes reduce the tendency of the V_{CE} rising after the V_{CE} sharing regulation according to the discussion in section 3.3.3. Hence, the $\Delta V_{CE,Diff.}$ after the V_{CE} sharing regulation is higher in the third example, in which the lower side IGBT is with a rising V_{CE} in the V_{CE} sharing regulation process in the tail time.

In all the three typical examples shown, despite the relatively short V_{CE} sharing regulation period in the tail time, the V_{CE} sharing after the V_{CE} sharing regulation is quasi-static and apparently self-stabilising. However, evenly distributed V_{CE} sharing is not reached due to fixed differences between the IGBTs. Similar to the long-term off-state V_{CE} sharing after the direct active V_{CE} sharing regulation in Chapter 5, here the duration of the IGBT off-state after the V_{CE} sharing regulation in the test period is also insufficient for the V_{CE} sharing to reach a static distribution.

5.4 Summary of the Direct Active V_{CE} Sharing Regulation

The direct active V_{CE} sharing regulation via IGBT gate control is effective in the experiments. Due to the low-loss preconditioning stage and the differential V_{CE} sharing regulation that enables a high $\mathrm{d}V_{CE}/\mathrm{d}t$ rate in the fast V_{CE} rising, the additional losses caused by the V_{CE} sharing regulation are reduced compared with the previous relevant researches in [178]–[181]. In the tail time, as the differential V_{CE} sharing regulation here regulates the V_{CE} sharing as it tends to diverge, the extent of the V_{CE} divergence remains low in the turn-off, although not eliminated due to the essential small safety margin in the V_{CE} reference signal. The V_{CE} sharing after the V_{CE} sharing regulation is quasi-static with a self-stabilising trend.

However, the influence of the direct active V_{CE} sharing regulation on the reliability of the IGBT gate oxide requires further research. In an uncontrolled IGBT turn-off event, the IGBT gate oxide is only discharged once from the on-state to the off-state, which has a more predictable influence on the reliability of the IGBT gate oxide compared with that of the complicated and variable charging/discharging of the IGBT gate oxide in the direct active V_{CE} sharing regulation. The reliability prediction of the IGBTs under the direct active V_{CE} sharing regulation is difficult, which limits the use of the direct active V_{CE} sharing regulation in power electronic systems that require dependable reliability prediction of the IGBTs. This topic is intended for future research.

Chapter 6 External Active Voltage Control for Regulating the Voltage Sharing

6.1 External Active V_{CE} Sharing Regulation with SiC MOSFETs

6.1.1 Design Concept of the External Active V_{CE} Sharing Regulation

Following the discussions in section 5.2.1, another universal approach to compensate for the internal differences between the IGBTs that can cause the V_{CE} divergence in turn-off is to adjust the I_C of the IGBT with a higher V_{CE}. Thus, the depletion process in the fast V_{CE}-I_C transient and the hole diffusion current in the undepleted part of the N base towards the depletion region in the tail time can be adjusted to suppress the original V_{CE} diverging mechanisms and mitigate the V_{CE} divergence. The intended adjustments to the I_C are achieved by introducing a current via an auxiliary power semiconductor device in parallel to the IGBT controlled by the AVC scheme. With an adequate current via this auxiliary power semiconductor device to counter the effects of the V_{CE} diverging factors, the original V_{CE} diverging mechanisms can be reversed to reduce the V_{CE} divergence.

To reduce the additional IGBT turn-off losses related to the V_{CE} sharing regulation, the external active V_{CE} sharing regulation here is also based on the strategy of differential V_{CE} sharing regulation, where the V_{CE} sharing regulation is only active on the IGBT with a higher V_{CE}. The external active V_{CE} sharing regulation is also intended to regulate the V_{CE} sharing as it tends to diverge, so as to reduce the difference in the IGBT turn-off losses and mitigate the influence of the V_{CE} sharing regulation on the stability and the EMC of the power circuit.

Applying the V_{CE} sharing regulation via auxiliary power semiconductor devices in parallel diverts the extra stresses on the IGBT gate oxide related to the previous direct V_{CE} sharing regulation to the auxiliary power semiconductor devices. This topic is intended for future research.

The requirements for the auxiliary power semiconductor devices here include: (1) FET-type devices that enable the use of the AVC scheme and low-loss driving, (2) a high voltage rating that enables the device to withstand the high V_{CE} of the IGBT in parallel during the turn-off and the off-state, (3) the negative influence of the auxiliary power devices on the IGBT turn-off $\mathrm{d}V_{CE}/\mathrm{d}t$ rate is insignificant, and (4) a wide RBSOA of the auxiliary device that enables the use of a small active chip area of the auxiliary device to improve the control response under the AVC scheme and reduce the cost of the auxiliary devices.

Considering these requirements, Silicon Carbide (SiC) MOSFETs are suitable as the auxiliary power semiconductor devices for the intended external active V_{CE} sharing regulation. The gate driving of SiC MOSFETs is similar to that of Si IGBTs. Currently commercial SiC MOSFETs are available in voltage classes up to 1.7 kV, e.g. Wolfspeed C2M0045170P rated 1.7 kV and 72 A at 25 °C, which cover commercial Si IGBTs of up to 1.7 kV. Commercial SiC MOSFETs are also available in module packages for higher current ratings, e.g. Wolfspeed CAS300M17BM2 rated 1.7 kV and 325 A at 25 °C. The SiC MOSFET is a unipolar device that does not produce any tail current that can be found in typical Si IGBT turn-off. It also has a

very low leakage current in the off-state. Therefore, SiC MOSFETs have a very limited influence on the IGBT V_{CE} sharing after the intended external active V_{CE} sharing regulation.

The external active V_{CE} sharing regulation here only requires a small current via the auxiliary power semiconductor device for a short period during the IGBT turn-off, e.g. normally on a scale of 10-20 µs depending on the IGBT device and the operating conditions. Hence, the typical RBSOA of a SiC MOSFET enabled by the WBG characteristics of SiC and the robust SiC MOSFET structure including an avalanche capability enables the use of auxiliary SiC MOSFETs of small active chip areas to improve the control response and the cost-effectiveness.

Here, the auxiliary SiC MOSFETs only conduct the external active V_{CE} sharing regulation during the IGBT turn-off and are inactive during the rest of the IGBT switching cycle. Applications of similar circuits involving a Si IGBT and a SiC MOSFET are reported in [207], [208], however, their design concepts and operating principles are for reducing switching losses and are completely different from those of the external active V_{CE} sharing regulation here.

Since the approaches discussed in section 5.2.4.1 and 5.2.4.2 to mitigating the timing error in the initial discharging of the IGBT MOS gate can only be applied via IGBT gate control, the external active V_{CE} sharing regulation here is intended to operate in conjunction with the preconditioning stage of the direct active V_{CE} sharing regulation discussed in Chapter 5.

As discussed in section 5.2.3, here the V_{CE} reference signals generated on separate AVC gate drives are also subject to relative timing jitters due to the unsynchronised clock sources for the digital FPGAs on the AVC gate drives. If the intended external active V_{CE} sharing regulation is applied during the timing-critical fast V_{CE} rising of IGBT turn-off, such a relative timing jitter between the AVC gate drives for an IGBT and its auxiliary SiC MOSFET in parallel may cause undesirable shifting of the load current from the IGBT to its auxiliary SiC MOSFET of a much smaller current rating. For example, if the triggering of the IGBT gate drive is ahead of the triggering of the SiC MOSFET gate drive, the timing of the fast V_{CE} rising of the IGBT will be ahead of the related segments of the calibrated V_{CE} reference signal for the SiC MOSFET. In this case, false feedback of over-V_{CE} may occur in the AVC circuit for the SiC MOSFET and trigger the external active V_{CE} sharing regulation incorrectly. Part of the IGBT load current will be diverted to the SiC MOSFET, which in extreme cases can impose excessive and even critical stresses on the SiC MOSFET.

To avoid this situation, a safety margin needs to be included in the V_{CE} reference signal for the SiC MOSFET. However, considering the relative timing jitter of up to 20 ns and the FPGA programming limits under the experiment setup here, an adequate safety margin in the V_{CE} reference signal will significantly reduce the effectiveness of the external active V_{CE} sharing regulation during the fast V_{CE} rising. Hence, also for safety considerations, the external active V_{CE} sharing regulation under the experiment setup here will only be applied after the timing-critical fast V_{CE} rising of the IGBT from the peak V_{CE} overshoot. The detailed mechanism of the external active V_{CE} sharing regulation will be discussed in the following section.

6.1.2 Mechanism of the External Active V_{CE} Sharing Regulation

6.1.2.1 Internal Regulation Mechanism for the IGBTs

The differential V_{CE} sharing regulation here is also triggered only on the IGBT with a higher V_{CE} when its V_{CE} exceeds a preset trajectory including a small safety margin. During the IGBT turn-off, for the SiC MOSFET in parallel to the IGBT with a higher V_{CE}, when the V_{CE} sharing regulation is triggered, its V_{GS} is raised above the V_{TH} by its AVC gate drive circuit to enable a small drain current I_D to flow to the other IGBT-MOSFET pair with a lower IGBT V_{CE}. For the IGBT-MOSFET pair with a lower IGBT V_{CE}, as the differential V_{CE} sharing regulation is not triggered, the SiC MOSFET is inactive with an insignificant I_D compared with the I_C of the IGBT, regardless of the turn-off phase of the IGBT. This is because the SiC MOSFET has a much smaller active chip area and as a unipolar device is without high-level excess carriers. Hence, given the same total current of the IGBT-MOSFET pairs in series, the I_C of the IGBT with a higher V_{CE} under the external active V_{CE} sharing regulation is lower than the I_C of the IGBT with a lower V_{CE}. Here, between the IGBTs, the difference in the I_C is responsible for mitigating the V_{CE} divergence.

For the IGBT with a higher V_{CE}, under the external active V_{CE} sharing regulation, the lower I_C results in a lower total current in the undepleted part of the N base. When high-level excess carriers exist in the undepleted part of the N base, the lower I_C results in a lower ambipolar current in that region which requires a smaller number of electrons from the MOS gate side CSR boundary. Therefore, the number of holes from the MOS gate side CSR boundary transported into the depletion region is also smaller, which results in a lower electric field gradient in the depletion region. Hence, since the expansion of the depletion region and the electric field gradient in the depletion region are both lower, the V_{CE} divergence is mitigated.

When high-level excess carriers no longer exist in the undepleted part of the N base, the lower I_C results in a lower hole current in that region which leads to a lower requirement for the hole drift current in that region. Consequently, the number of holes transported into the depletion region and the tendency of further depletion in the N base are lower. Hence, since the electric field gradient in the depletion region and the tendency of further depletion in the N base are both lower, the V_{CE} divergence is mitigated. With an adequate current via the auxiliary SiC MOSFET, for the IGBT in parallel with a higher V_{CE}, its I_C can be lower to an extent that the opposing drift-diffusion relation of the electrons at the depletion edge in the N base is biased to diffusion, which recovers the depletion region from that depletion edge. In this process, the current via the auxiliary SiC MOSFET increases the I_C of the IGBT with a lower V_{CE} to reverse the original mechanism that causes the V_{CE} divergence. Hence, the V_{CE} divergence is reduced.

6.1.2.2 Internal Voltage Regulation Mechanism for Auxiliary SiC MOSFETs

The auxiliary SiC MOSFETs here are n-channel devices. In the forward-blocking state, the depletion region develops mainly in the N-drift region. Since SiC MOSFETs are unipolar devices, they do not produce any tail current that can be found in typical Si IGBT turn-off.

The auxiliary SiC MOSFET when conducting the external active V_{CE} sharing regulation is in the I_D saturation region and its V_{DS} is approximately equal to the V_{CE} of the IGBT in parallel.

In this process, relative to the other SiC MOSFET, the electrons via the MOS channel result in a lower electric field gradient in the depletion region in which the N-type dopants exhibit positive charges as they lost electrons. In the fast V_{CE}-I_C transient of the IGBT turn-off, part of the electrons via the MOS channel in this SiC MOSFET also adjust its own depletion process dynamically. Hence, its V_{DS} can change with the V_{CE} of the IGBT in parallel in the V_{CE} sharing regulation process.

When the V_{CE} of the IGBT in parallel is being reduced in the V_{CE} sharing regulation process, in this SiC MOSFET the electrons via the MOS channel bias the opposing drift-diffusion relation of the electrons at the depletion edge in the N base to diffusion, which recovers the depletion region from that depletion edge. Hence, the V_{DS} of this SiC MOSFET decreases with the V_{CE} of the IGBT in parallel. Meanwhile, a small part of the I_D via the active SiC MOSFET is distributed to the other inactive SiC MOSFET with a lower V_{DS}. Consequently, in the inactive SiC MOSFET the electron current in the undepleted part of the N-drift region increases, which leads to further depletion in the N-drift region. Hence, the V_{DS} of the inactive SiC MOSFET increases with the V_{CE} of the IGBT in parallel.

6.1.3 Implementation of the AVC Circuit and the V_{CE} Reference Signal

The experimental implementation of the external active V_{CE} sharing regulation here uses the same prototype AVC gate drives presented in Chapter 5 to control the auxiliary SiC MOSFETs. The AVC circuit of the AVC gate drives for the auxiliary SiC MOSFETs remains the same as presented in section 5.2.3 except that the external gate resistance Rg_ext is increased to 2.35 **Ω** to prevent oscillation in the gate driving path. The AVC gate drives for the IGBTs are set to perform uncontrolled turn-off. All the AVC gate drives are attached to the same central signal generator for switching instruction signals. Due to the signal acquisition jitter discussed in section 5.2.3, the relatively timing jitters between the AVC gate drives at an IGBT turn-off event may alter at the following IGBT turn-on event.

Following the discussion in section 6.1.1, for demonstration, here the V_{CE} reference signal for the auxiliary SiC MOSFETs is set to conduct the external active V_{CE} sharing regulation from the peak V_{CE} overshoot of the IGBT turn-off. The V_{CE} reference signal is also based on the strategy of differential V_{CE} sharing regulation using a predicted average V_{CE} trajectory and is calibrated manually using the same method in section 5.2.4 considering the conditions of the CCL and the characteristics of both the IGBT and the auxiliary SiC MOSFET. With the V_{CE} reference signal calibrated, when the V_{CE} of an IGBT exceeds the predicted trajectory plus a small safety margin, the gate driving voltage for the auxiliary SiC MOSFET in parallel to this IGBT is raised by the AVC circuit to introduce and/or adjust the I_D of the auxiliary SiC MOSFET, so that the V_{CE} divergence can be mitigated as discussed in section 6.1.2.

The V_{CE} reference signal for the auxiliary SiC MOSFET calibrated for the experiments in this chapter, Figure 6.1, uses two control stages by segments t_1 to t_5 for the part of IGBT turn-off from the peak V_{CE} overshoot to the tail time. In the V_{CE} reference signal, the segments t_1 to t_5 are for the IGBT turn-off, and the segments t_6, t_7, and t_0 are for the following IGBT off-state, turn-on, and on-state. The V_{CE} reference signal in the order of segment t_1 to t_7 and t_0 is triggered

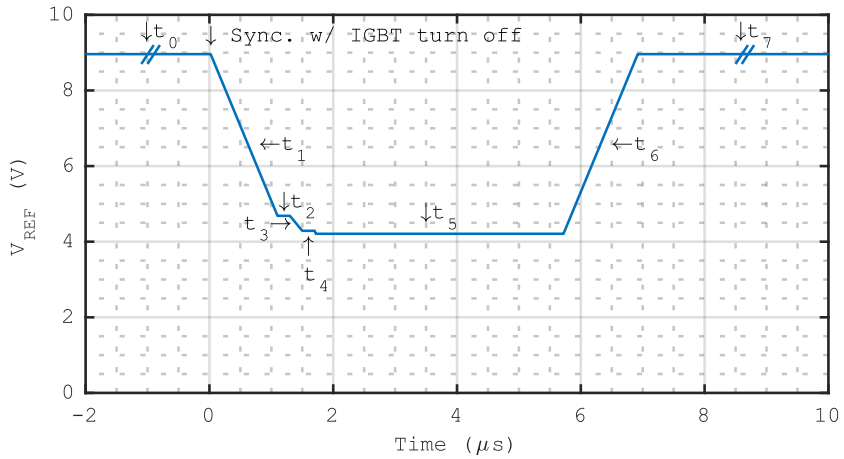


Figure 6.1: The reference signal for the auxiliary SiC MOSFETs.

by an IGBT turn-off instruction signal. Since the IGBT turn-on is not part of the focus of this thesis, the t_7 and t_0 are set to only maintain the auxiliary SiC MOSFET in the off-state.

The timings and the voltages of the t_1 to t_6 as shown in Figure 6.1 are the actual values calibrated for the auxiliary SiC MOSFETs in the experiments of the external active V_{CE} sharing regulation in this chapter. The voltages of the t_7 and t_0 as shown in Figure 6.1 are also the actual values used, but the timings of the t_7 and t_0 are controlled by the central signal generator and are longer in the actual experiments. The V_{CE} reference signal shown in Figure 6.1 is calibrated for demonstrating the key principles of the external active V_{CE} sharing regulation in this thesis, which is not intended for industrial use.

To maintain the auxiliary SiC MOSFET in the off-state outside the V_{CE} sharing regulation period, the t_7 and t_0 are set to a plateau higher than the scaled feedback of the predicted average off-state IGBT V_{CE} that saturates the AVC gate drive for the auxiliary SiC MOSFET at its off-state driving voltage.

After the acquisition of an IGBT turn-off instruction signal, as shown in Figure 6.1, the t_1 uses a slow ramp for the transition of the auxiliary SiC MOSFET from the off-state in the t_0 to conducting the external active V_{CE} sharing regulation in the t_2 from the peak IGBT V_{CE} overshoot. The duration of the t_1 is determined by the predicted time from the IGBT turn-off instruction signal to the beginning of the IGBT V_{CE} overshoot.

The t_2 and the t_3 are designed to trace the predicted IGBT V_{CE} overshoot from its peak. A small safety margin is included above the predicted V_{CE} to maintain the V_{GS} of the auxiliary SiC MOSFET below the V_{TH} in the case of evenly distributed V_{CE} sharing, similar to the V_{CE} reference signal in the direct active V_{CE} sharing regulation in Chapter 5.

Following the t_3, for the IGBT tail time the V_{CE} reference signal consists of two segments, the t_4 with a short clamp followed by the t_5 with a long and slightly lower clamp. For the early IGBT tail time, the short clamp in the t_4 is set to accommodate the slightly higher IGBT V_{CE} compared with the predicted average off-state V_{CE} due to the stray inductance in the CCL as the early IGBT tail current decays. Similar to the t_2 and the t_3, a small safety margin is included above the predicted average V_{CE} in the t_4 to avoid V_{CE} oscillation and/or simultaneous clamping of the V_{CE} on both the IGBTs, in which case the I_D of both the auxiliary SiC MOSFETs would

rise undesirably. If the V_{CE} divergence is inadequate to trigger the V_{CE} regulation in the t_4, the V_{GS} of the auxiliary SiC MOSFET will be near the V_{TH} to reduce the response time of the auxiliary SiC MOSFET in the following t_5, similar to the direct active V_{CE} sharing regulation in Chapter 5.

For the late IGBT tail time, the long clamp in the t_5 regulates the V_{CE} sharing continuously towards the predicted average off-state IGBT V_{CE}. Since the internal differences between the IGBTs are reduced in the previous V_{CE} sharing regulation process, the t_4 and t_5 only needs to cover part of the IGBT tail time until the remaining differences between the IGBT-MOSFET pairs would not upset the regulated V_{CE} sharing to a significant extent. Similar to the t_4, a small safety margin is included in the t_5 to avoid V_{CE} oscillation and/or simultaneous clamping of the V_{CE} on both the IGBTs. Hence, a slight but self-stabilising V_{CE} divergence may exist after the t_5 depending on the remaining differences between the IGBT-MOSFET pairs.

For the following IGBT off-state, turn-on, and on-state where the auxiliary SiC MOSFET is maintained in the off-state, first in the t_6 a slow rising ramp removes the previous clamp gradually. In the t_7, a plateau is set to saturate the AVC gate drive for the auxiliary SiC MOSFET at the off-state driving voltage for a secure off-state of the SiC MOSFET.

6.2 Experiments of the External Active V_{CE} Sharing Regulation

6.2.1 Experiment Setup

The experiments of the external active V_{CE} sharing regulation are based on the experiment setup and the test method used in Chapter 5, including the same IGBTs and boost converter circuit, with a few modifications as shown in Figure 6.2. Here, one SiC MOSFET controlled by an AVC gate drive is attached in parallel to each of the IGBTs in series, which remain as the main

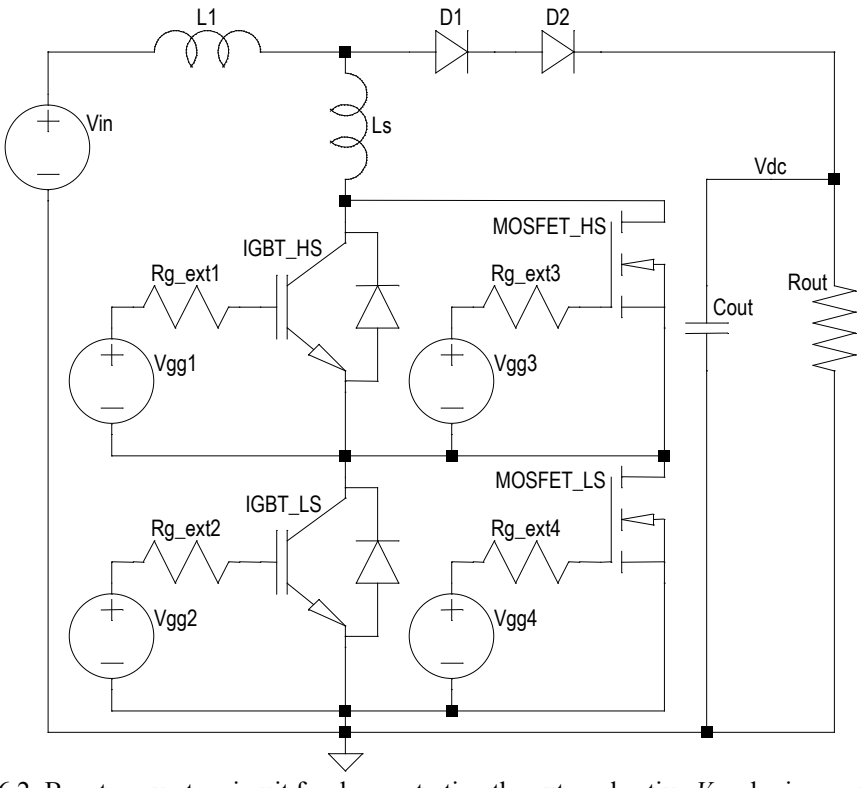


Figure 6.2: Boost converter circuit for demonstrating the external active V_{CE} sharing regulation.

switch of the boost converter circuit. Due to the availability of SiC MOSFETs at the time of the experiments, the SiC MOSFETs used here are Wolfspeed C2M0080120D, rated 1200 V and 36 A at 25 °C, with an internal gate resistance of 4.6 Ω. Limited by the voltage rating of the SiC MOSFETs, for the same safety considerations discussed in section 5.3.1, the V_{DC} here is reduced to approx. 800 V for an average off-state blocking voltage of approx. 400 V for the two IGBT-MOSFET pairs. As a result, the IGBT load current to be switched at the IGBT turn-off is reduced to approx. 45 A.

Figure 6.3 shows the layout of the AVC gate drives in the experiments of the external active V_{CE} sharing regulation. The AVC gate drives for the auxiliary SiC MOSFETs are positioned on the outer sides of the IGBT gate drives. Figure 6.4 shows the layout of the power devices in the experiments of the external active V_{CE} sharing regulation. The same experiment setup has the same parameter variations between the IGBTs and their respective gate drives. The uncontrolled turn-off of the IGBTs is also emulated by their AVC gate drives using step transitions in the V_{CE} reference signal for IGBT switching, which is subject to the same type of relative timing jitters between the AVC gate drives that can cause the V_{CE} divergence.

The measured V_{CE} reference signal generated by the FPGA and the DAC on the AVC gate drive for an auxiliary SiC MOSFET under zero-input of the boost converter circuit is shown in Figure 6.5. The segments indicated in Figure 6.5 correspond to those shown in Figure 6.1 and discussed in section 6.1.3. The short segment t_4 is not obvious in Figure 6.5 due to the 8-bit resolution of the oscilloscope. The full cycle of this V_{CE} reference signal is not shown, as outside the t_1 to t_6 the same plateau is used for the t_7 to t_0 to maintain the auxiliary SiC MOSFET in the off-state. Outside the V_{CE} sharing regulation period, the auxiliary SiC MOSFET remains in the off-state. Hence, the distribution of the thermal allowance of the auxiliary SiC MOSFET only needs to consider the losses in the V_{CE} sharing regulation period, which enables the cost-effective use of SiC MOSFETs of a low current rating.

In a test cycle, the nominal IGBT off-state is approx. 39 µs. Same as the experiments in Chapter 5, this is limited by the main inductor and the high conversion ratio of the boost converter circuit, which results in considerable decreases in the main inductor current during the IGBT off-state and the IGBT load current after the IGBT off-state.

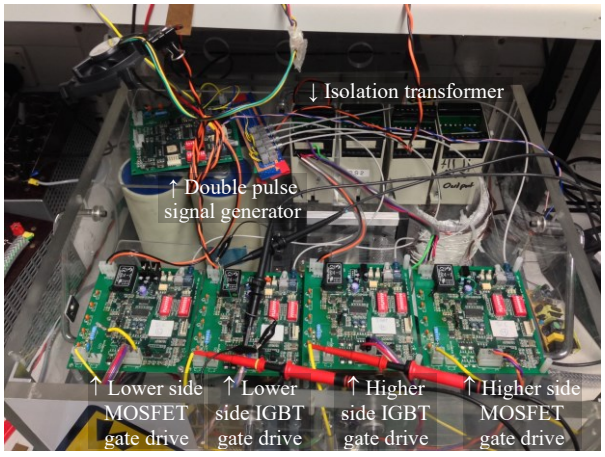


Figure 6.3: Physical layout of AVC gate drives.

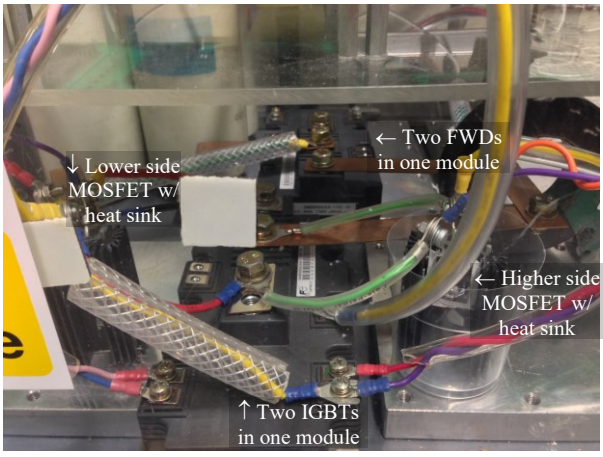


Figure 6.4: Physical layout of power devices.

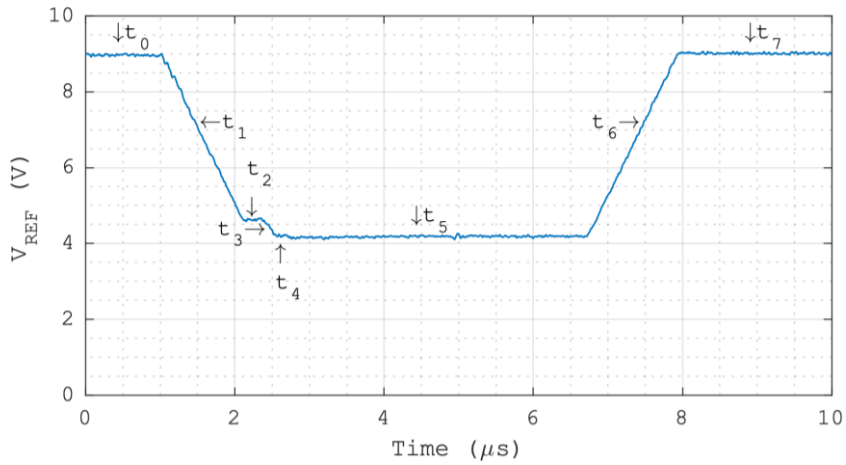


Figure 6.5: Boost converter circuit for demonstrating external active V_{CE} sharing regulation.

The experiments here in each test group use the same V_{CE} reference signal and are sampled at different times during a continuous testing period with unchanged control of the circuit input conditions, unless specified otherwise. The features of the experiments are also captured to an 8-bit resolution with a 2 ns sampling interval by the same LeCroy LT344L oscilloscope used in the experiments in Chapter 5.

6.2.2 V_{CE} Divergence in Uncontrolled IGBT Turn-off

First for comparison, the V_{CE} divergence in uncontrolled IGBT turn-off, with the external active V_{CE} sharing regulation disabled, is tested using hard-switched IGBT turn-off with the same test circuit. For the IGBTs, the hard-switched turn-off is also emulated using the same method in section 5.3.3 and is effectively uncontrolled. For the auxiliary SiC MOSFETs, the V_{CE} reference signal is set to the off-state level to saturate their AVC gate drives at the off-state driving voltage. Hence, the external active V_{CE} sharing regulation is effectively disabled. Similar to the uncontrolled IGBT turn-off test in section 5.3.3, here the V_{CE} divergence is also affected by the relative timing jitters between the AVC gate drives.

A typical example of the uncontrolled IGBT turn-off with large V_{CE} divergence is shown in Figure 6.6. The measured current I_{PAIR} includes the I_D of the auxiliary SiC MOSFET and the $I_{C,PKG}$ of the IGBT package that is close to the I_C of the IGBT. During this uncontrolled IGBT turn-off, since the unipolar SiC MOSFET of a low current rating without high-level excess carriers is in the off-state, the I_D is considerably smaller than the $I_{C,PKG}$. Hence, here the I_{PAIR} is close to the I_C of the IGBT. The $V_{CE,Diff.}$ is defined as the same ($V_{CE,LS} - V_{CE,HS}$). As the turn-off and the turn-on of the IGBTs are triggered independently, the relative timing jitters between the AVC gate drives at the turn-off may change at the following turn-on and lead to an opposite IGBT V_{CE} diverging situation.

In this example, the V_{CE} diverging features are similar to those in the IGBT-only uncontrolled turn-off test in section 5.3.3. Large V_{CE} divergence is observed in Figure 6.6, although compared with the results shown in Figure 5.9 in section 5.3.3 the V_{CE} divergence here is smaller but extends over a longer period at the reduced IGBT load current and DC voltage at the IGBT turn-off. Similar changes are also observed in the simulations in section 4.2.1 and 4.2.5 with similar reductions in the on-state J_C and the V_{DC}, respectively. The V_{CE} diverging period under the circuit conditions here exceeds 20 µs. Before the following IGBT turn-on, the $V_{CE,Diff.}$

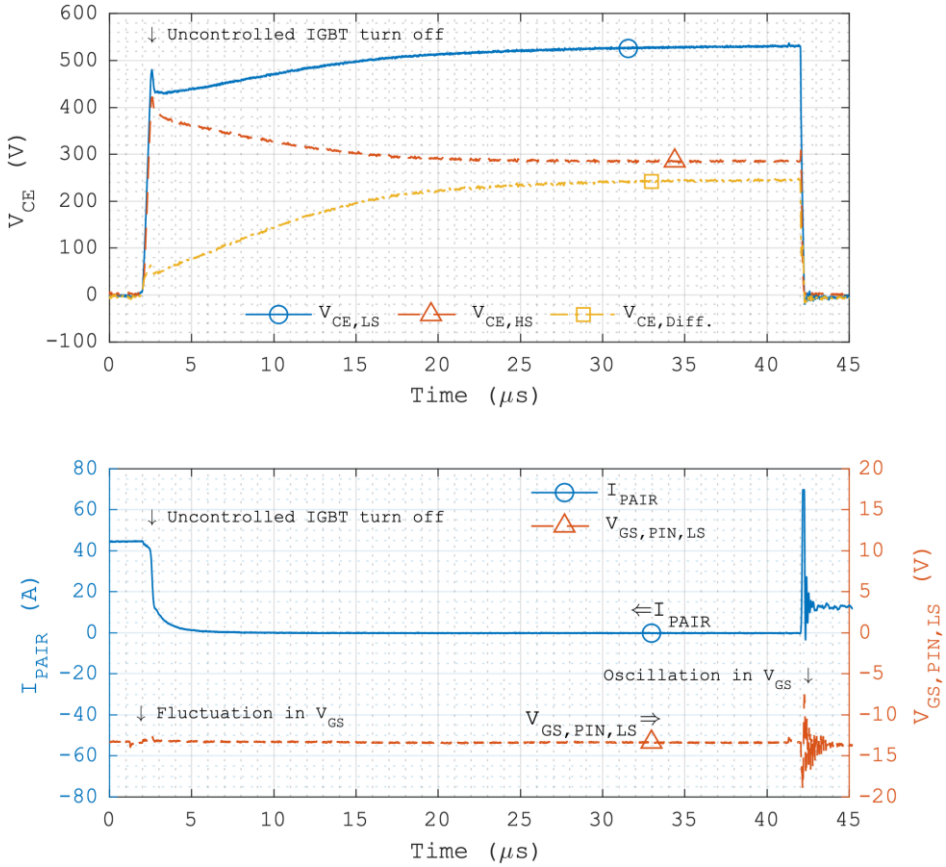


Figure 6.6: Uncontrolled turn-off of two IGBTs in series with large V_{CE} divergence and the external active V_{CE} sharing regulation disabled.

reaches a maximum of approx. 250 V, which is 31.25% of the 800 V V_{DC} and similar to that of 32% in the IGBT-only uncontrolled turn-off test in section 5.3.3, despite the reduced IGBT load current and DC voltage at the IGBT turn-off. Hence, the passive effects of the auxiliary SiC MOSFETs on the IGBT turn-off V_{CE} sharing are insignificant. Here, the passive characteristics of the SiC MOSFETs in the off-state are simply capacitive.

In the experiment results here, the $V_{GS,PIN,LS}$ refers to the gate-source voltage measured at the package pins of the lower electric potential side auxiliary SiC MOSFET. The internal gate resistance inside the MOSFET package is 4.6 Ω, and the external gate resistance on the MOSFET gate drive is 2.35 Ω. The MOSFET package here only allows the V_{GS} to be measured at the package pins, where the gate pin is between the internal gate resistance and the external gate resistance in the gate driving path. Hence, the measured V_{GS} here is different from the V_{GS} of the MOSFET chip.

The $V_{GS,PIN,LS}$ has slight oscillation during the fast V_{CE} rising at the IGBT turn-off as indicated in Figure 6.6 due to the gate-drain capacitance C_{GD}, the stray inductance in the gate driving path, and the gate resistance of the SiC MOSFET. At the following IGBT turn-on, the $V_{GS,PIN,LS}$ is subject to oscillation as indicated in Figure 6.6. The oscillation in the $V_{GS,PIN,LS}$ and the I_{PAIR} at the IGBT turn-on is caused by the reverse recovery current of the FWD branch in the CCL.

6.2.3 Demonstration of the External Active V_{CE} Sharing Regulation

To reveal the effects of the external active V_{CE} sharing regulation, the IGBTs are turned off in the same uncontrolled manner as in section 6.2.2. Figure 6.7 shows a typical example of the

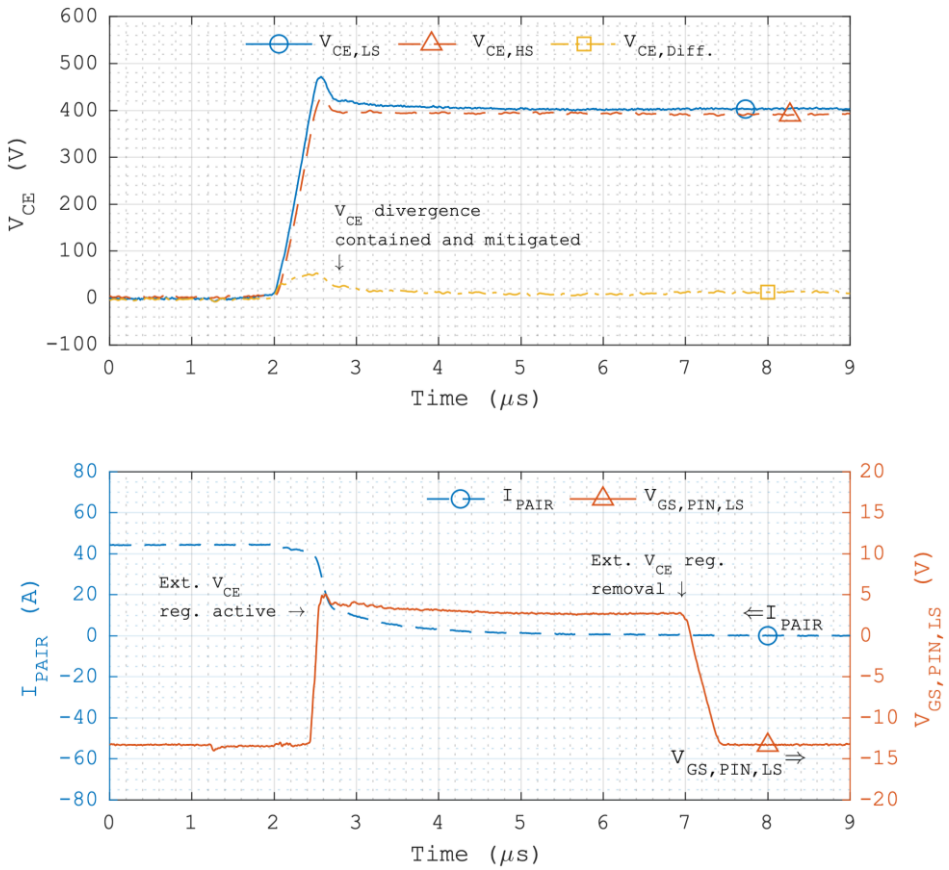


Figure 6.7: External active V_{CE} sharing regulation against strong V_{CE} diverging factors.

external active V_{CE} sharing regulation against strong V_{CE} diverging factors. Without any control of the IGBT V_{CE} applied until the peak V_{CE} overshoot, first a rapid but small V_{CE} divergence is observed at the beginning of the fast V_{CE} rising at 2 µs in Figure 6.7 mainly due to a relative timing jitter in IGBT gate driving. The $V_{CE,Diff.}$ defined as ($V_{CE,LS} - V_{CE,HS}$) here increases and reaches a maximum of approx. 53 V during the fast V_{CE}-I_C transient before mitigated by the external active V_{CE} sharing regulation. As discussed in section 6.1.1, in the demonstration here the external active V_{CE} sharing regulation is applied from the peak V_{CE} overshoot, which is from the segment t_4 of the V_{CE} reference signal.

At approx. 2.45 µs, slightly prior to the total V_{CE} reaching the V_{DC}, the $V_{GS,PIN,LS}$ starts to increase rapidly. At approx. 2.55 µs, the $V_{GS,PIN,LS}$ exceeds the typical V_{TH} in the datasheet of 2.6 V at $V_{DS} = V_{GS}$, $I_D = 5$ mA, and 25 °C, slightly prior to the peak $V_{CE,LS}$ overshoot. Afterwards a significant reduction in the $V_{CE,Diff.}$ is observed, although this reduction is also related to the simultaneous falling of the I_C as discussed previously in Chapter 3 and 4. Nevertheless, the more rapid and much larger decrease in the $V_{CE,LS}$ in its overshoot after the peak compared with that of the $V_{CE,HS}$ suggests effective and rapid V_{CE} sharing regulation. The changes in the $V_{GS,PIN,LS}$ during the rest of the t_4 of the V_{CE} reference signal are related to the simultaneous changes in the $V_{CE,LS}$. The $V_{GS,PIN,LS}$ reaches a maximum of approx. 5 V at approx. 2.6 µs. Afterwards the $V_{CE,Diff.}$ is controlled in the rest of the t_4.

The small rise in the $V_{GS,PIN,LS}$ at 2.9 µs indicates the transition from the t_4 to the t_5 of the V_{CE} reference signal due to the lower clamp level in the t_5, after which the $V_{CE,Diff.}$ starts to decrease gradually. In this process the $V_{GS,PIN,LS}$ decreases gradually to 2.7 V as the $V_{CE,Diff.}$

decreases. Similar to the example of the direct active V_{CE} sharing regulation shown in Figure 5.16 in Chapter 5, here the gradual and steady V_{CE} sharing regulation process only requires a small current via the auxiliary SiC MOSFET, and therefore late in the t_7 the $V_{GS,PIN,LS}$ is near the typical V_{TH} in the datasheet of 2.6 V at $V_{DS} = V_{GS}$, $I_D = 5$ mA, and 25 °C. Due to the safety margin in the V_{CE} reference signal, the V_{CE} divergence is not eliminated in the t_5. The removal of the V_{CE} sharing regulation is from approx. 6.95 µs to 7.45 µs, where the $V_{GS,PIN,LS}$ is driven towards the off-state driving voltage of the AVC gate drive.

Figure 6.8 shows a typical example of the external active V_{CE} sharing regulation against moderate V_{CE} diverging factors. The initial V_{CE} diverging features in this example are similar to those in the previous example shown in Figure 6.7. Here, the initial V_{CE} divergence at 2 µs in Figure 6.8 is smaller than that shown in Figure 6.7 due to a smaller relative timing jitter in IGBT gate driving. The $V_{CE,Diff.}$ increases and reaches a maximum of approx. 34 V during the fast V_{CE}-I_C transient before mitigated by the external active V_{CE} sharing regulation.

The V_{CE} sharing regulation features in this example are also similar to those shown in Figure 6.7. At approx. 2.45 µs, slightly prior to the total V_{CE} reaching the V_{DC}, the $V_{GS,PIN,LS}$ starts to increase rapidly. At approx. 2.55 µs, the $V_{GS,PIN,LS}$ exceeds the typical V_{TH} in the datasheet of 2.6 V at $V_{DS} = V_{GS}$, $I_D = 5$ mA, and 25 °C, slightly prior to the peak $V_{CE,LS}$ overshoot. Afterwards a significant reduction in the $V_{CE,Diff.}$ is observed. The more rapid and larger decrease in the $V_{CE,LS}$ in its overshoot after the peak compared with that of the $V_{CE,HS}$ also suggests effective and rapid V_{CE} sharing regulation. The changes in the $V_{GS,PIN,LS}$ during the rest of the t_4 of the V_{CE} reference signal are related to the simultaneous changes in the $V_{CE,LS}$. The $V_{GS,PIN,LS}$ reaches

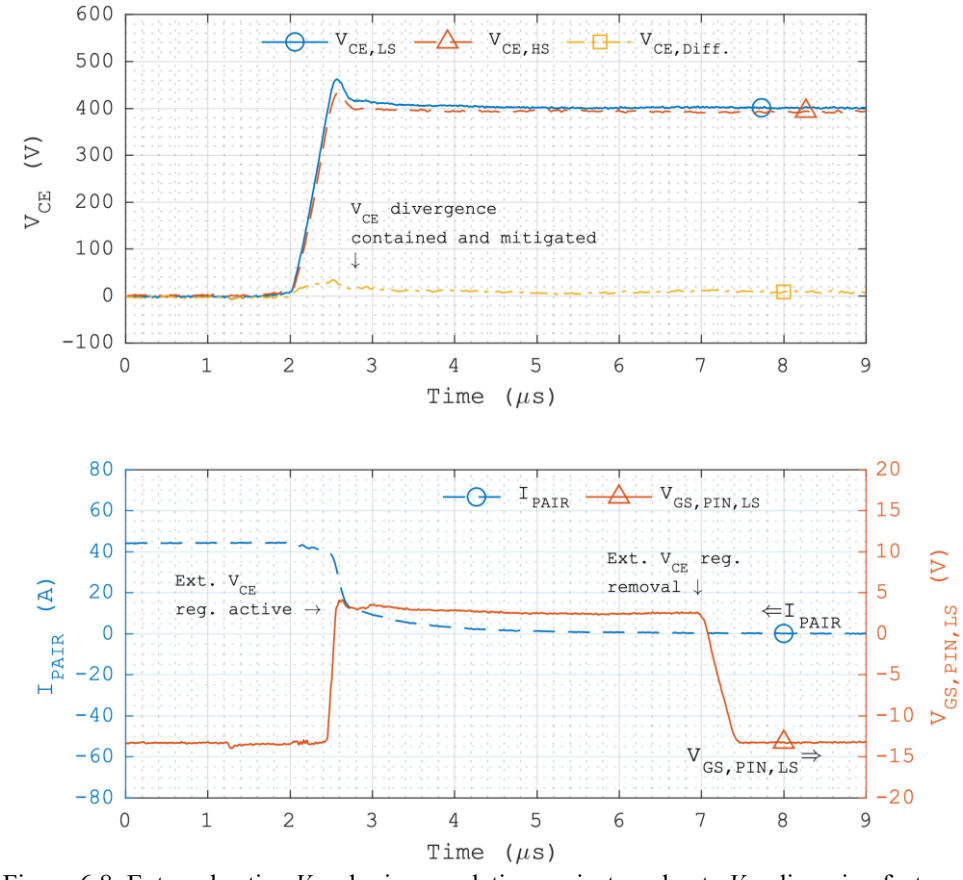


Figure 6.8: External active V_{CE} sharing regulation against moderate V_{CE} diverging factors.

a maximum of approx. 4 V at approx. 2.6 µs, which is lower than that shown in Figure 6.7 due to the smaller initial V_{CE} divergence. Afterwards the $V_{CE,Diff.}$ is controlled in the rest of the t_4.

The small rise in the $V_{GS,PIN,LS}$ at 2.9 µs indicates the transition from the t_4 to the t_5 of the V_{CE} reference signal due to the lower clamp level in the t_5, after which the $V_{CE,Diff.}$ starts to decrease gradually. In this process the $V_{GS,PIN,LS}$ decreases gradually to 2.55 V as the $V_{CE,Diff.}$ decreases. Same as the previous example shown in Figure 6.7, here the gradual and steady V_{CE} sharing regulation process only requires a small current via the auxiliary MOSFET, and therefore late in the t_7 the $V_{GS,PIN,LS}$ is also near the typical V_{TH} in the datasheet of 2.6 V at $V_{DS} = V_{GS}$, $I_D = 5$ mA, and 25 °C. Due to the safety margin in the V_{CE} reference signal, the V_{CE} divergence is not eliminated in the t_5. The removal of the V_{CE} sharing regulation is from approx. 6.95 µs to 7.45 µs, where the $V_{GS,PIN,LS}$ is driven towards the off-state driving voltage of the AVC gate drive.

As the IGBT gate drives are set to conduct uncontrolled turn-off, due to the fixed differences between the IGBTs, an example in which the higher side IGBT has higher V_{CE} sharing was not found in the testing period here. The external active V_{CE} sharing regulation is effective with stable V_{CE} sharing regulation processes in both the typical examples here with different V_{CE} diverging factors, and oscillation is not observed during the removal of the V_{CE} sharing regulation. Compared with the experiments of the direct active V_{CE} sharing regulation shown in Chapter 5, here the lag in the V_{CE} sharing regulation process is not as significant due to the considerably smaller C_{GS} of the auxiliary SiC MOSFET despite the higher gate resistance.

6.2.4 Long-Term Off-State V_{CE} Sharing after the External Active V_{CE} Sharing Regulation

For demonstration, here the t_4 and the following t_5 only cover the first 4.3 µs of the IGBT tail time, after which it is expected that under the circuit conditions here the remaining differences between the IGBT-MOSFET pairs would not upset the regulated V_{CE} sharing to a significant extent. The total duration of the t_4 and t_5 here is the same as that of the equivalent t_6 and t_7 in the demonstration of the direct active V_{CE} sharing regulation in Chapter 5.

Figure 6.9 shows the long-term V_{CE} sharing in the IGBT off-state after the external active V_{CE} sharing regulation of the same example shown in Figure 6.7 that features strong V_{CE} diverging factors. The IGBT off-state after the end of the V_{CE} sharing regulation as indicated in Figure 6.9 is approx. 34.3 µs from 7 µs to 41.3 µs.

At the end of the V_{CE} sharing regulation at 7 µs, the $V_{CE,Diff.}$ is reduced to 12 V from the highest 52 V but not to zero due to the safety margin in the V_{CE} reference signal. Afterwards, the $V_{CE,Diff.}$ is still approx. 12 V at 12 µs and then decreases gradually to 7 V at the end of the following IGBT off-state at 41.3 µs. This slight decrease in the $V_{CE,Diff.}$ is due to the small remaining differences between the IGBT-MOSFET pairs after the V_{CE} sharing regulation process. The t_4 and the t_5 in the V_{CE} reference signal only cover the first 4.3 µs of the IGBT tail time, but they are adequate for reducing the differences between the IGBTs to achieve quasi-static V_{CE} sharing in the following IGBT off-state. Since the basic principles regarding the long-term off-state voltage sharing discussed in section 3.3.6 are also applicable to SiC MOSFETs in series,

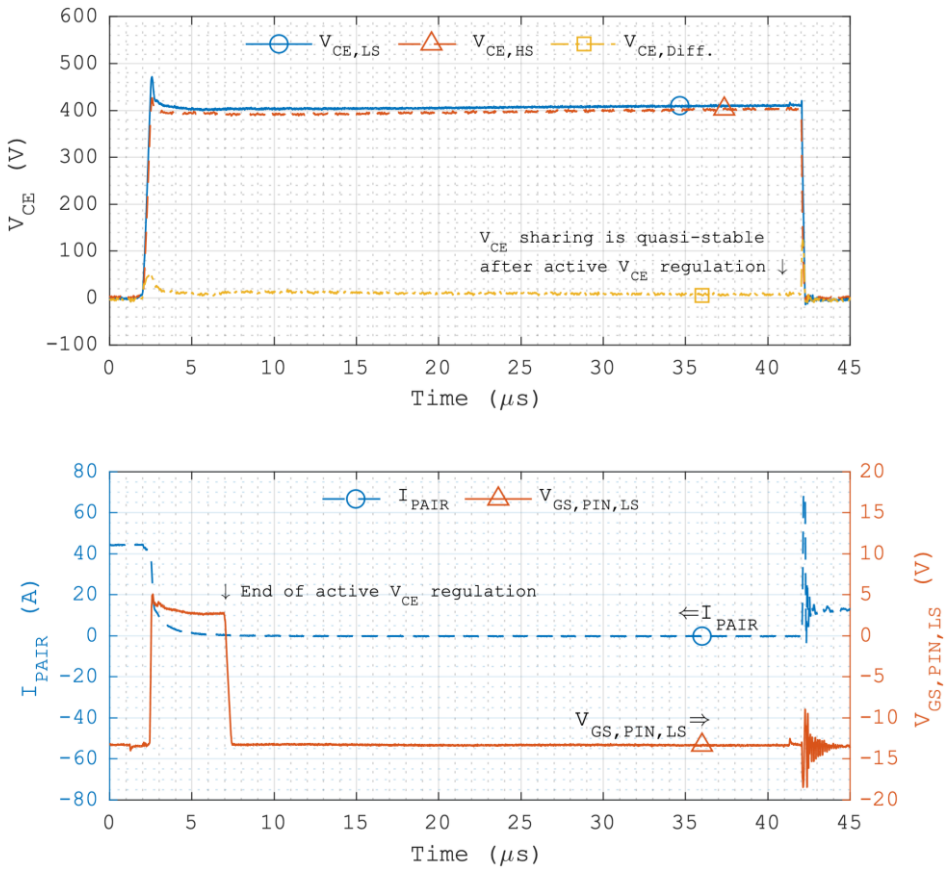


Figure 6.9: Long-term V_{CE} sharing in the IGBT off-state after the external active V_{CE} sharing regulation against strong V_{CE} diverging factors.

the long-term V_{CE} sharing in the IGBT off-state is also self-stabilising with the auxiliary SiC MOSFETs in parallel, although it may not reach an even distribution depending on the fixed differences between the IGBT-MOSFET pairs. The V_{CE} divergence in the following uncontrolled IGBT turn-on is not fully dependent on the V_{CE} diverging situation in this IGBT turn-off event. Regarding the I_{PAIR}, a spike followed by oscillation is observed in the following IGBT turn-on due to the reverse recovery current of the FWD branch in the CCL, which also causes simultaneous oscillation in the $V_{GS,PIN,LS}$.

Figure 6.10 shows the long-term V_{CE} sharing in the IGBT off-state after the external active V_{CE} sharing regulation of the same example shown in Figure 6.8 that features moderate V_{CE} diverging factors. The initial V_{CE} divergence in the fast V_{CE}-I_C transient here is not as large as that in the previous example shown in Figure 6.9, but the V_{CE} diverging features are similar. At the end of the V_{CE} sharing regulation at 7 µs, the $V_{CE,Diff.}$ is reduced to 12 V from the highest 34 V but not to zero due to the safety margin in the V_{CE} reference signal. Afterwards, the $V_{CE,Diff.}$ decreases to 6 V at 12 µs and continues to decrease gradually to -2 V at the end of the following IGBT off-state at 41.3 µs. This slight decrease in the $V_{CE,Diff.}$ is also due to the small remaining differences between the IGBT-MOSFET pairs after the V_{CE} sharing regulation process. Here, the long-term V_{CE} sharing is also quasi-static and self-stabilising in the following IGBT off-state.

The two typical examples shown in this section both have slight decreases in the $V_{CE,Diff.}$ after the V_{CE} sharing regulation during the following IGBT off-state. The general features of the long-term off-state V_{CE} sharing after the external active V_{CE} sharing regulation are similar

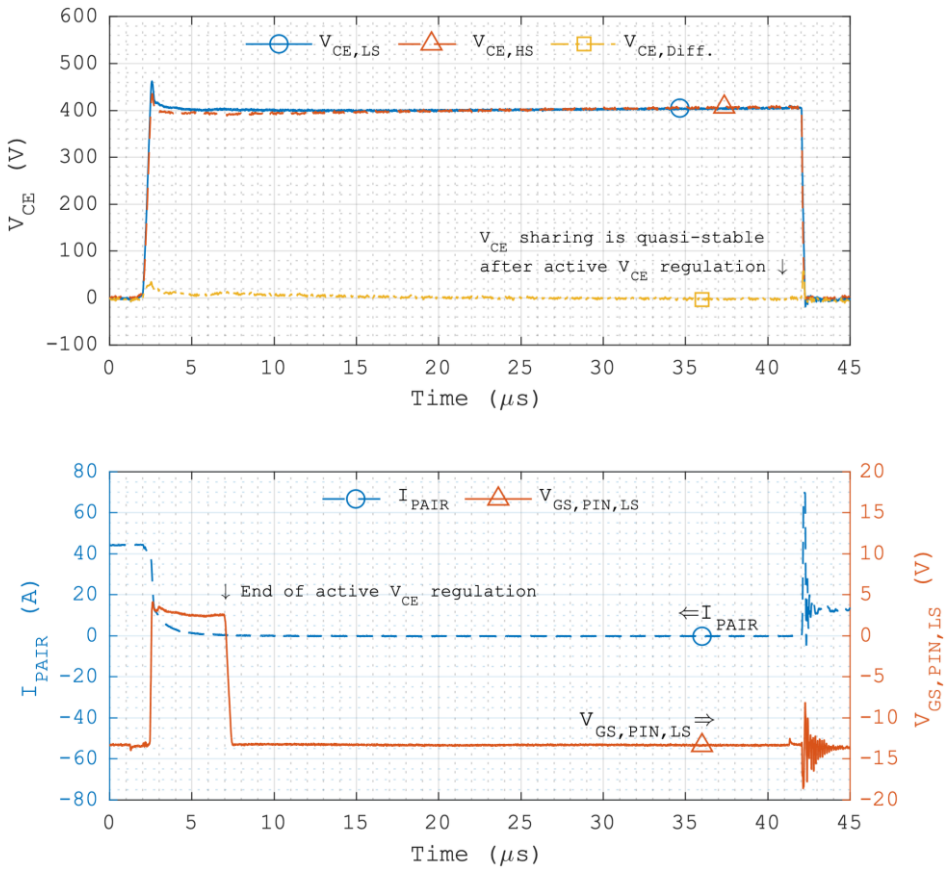


Figure 6.10: Long-term V_{CE} sharing in the IGBT off-state after the external active V_{CE} sharing regulation against moderate V_{CE} diverging factors.

compared with those after the direct active V_{CE} sharing regulation in Chapter 5. This suggests that those decreases in the $V_{CE,Diff.}$ after the V_{CE} sharing regulation are mainly caused by fixed differences between the IGBT-MOSFET pairs.

In both the typical examples shown here, despite the relatively short V_{CE} sharing regulation period in the IGBT tail time, the V_{CE} sharing after the V_{CE} sharing regulation is quasi-static and apparently self-stabilising as discussed previously. However, evenly distributed V_{CE} sharing is not reached due to fixed differences between the IGBTs. Considering the gradual decreases in the V_{CE} divergence in the uncontrolled IGBT off-state in the simulations shown in Chapter 3, here the duration of the IGBT off-state after the V_{CE} sharing regulation in the test period is insufficient for the V_{CE} sharing to reach a static distribution.

6.2.5 Thermal Utilisation of the Auxiliary SiC MOSFET

During the external active V_{CE} sharing regulation, the auxiliary SiC MOSFET is subject to high blocking voltages while providing a small current for the V_{CE} sharing regulation process. Despite the short V_{CE} sharing regulation period, the thermal utilisation of the auxiliary SiC MOSFET of a low current rating needs to be considered.

During the V_{CE} sharing regulation process, since $V_{DS} \gg (V_{GS} - V_{TH})$, the auxiliary SiC MOSFET operates under channel pinch-off conditions in the saturation region, where at a certain $(V_{GS} - V_{TH}) > 0$ the I_D is considered to be saturated as the V_{DS} increases. As the saturated drain current $I_{D,sat} \propto (V_{GS} - V_{TH})^2$, first the V_{GS} in the V_{CE} sharing regulation process is estimated. Considering the major circuit components in the gate driving path, the time constant of

the gate driving path is basically a RC time constant determined by the internal and the external gate resistances $R_{G,int}$ and $R_{G,ext}$, respectively, and the average gate-source capacitance $C_{iss,Avg}$ at high voltages estimated from the datasheet of the auxiliary SiC MOSFET, Figure 6.11 [209] (a):

$$\tau_{RgCg,Avg} = \left(R_{G,int} + R_{G,ext}\right)C_{iss,Avg} \approx (4.6\Omega + 2.35\Omega) \times 1090pF \approx 7.576ns \quad \text{Equation 6.1}$$

The $\tau_{RgCg,Avg}$ results in a RC settling time of approx. ($\tau_{RgCg,Avg} \times 5$) = 37.88 ns of the gate driving path within the controllable range of the AVC gate drive. Hence, considering the moderate slew rates of the $V_{GS,PIN,LS}$ within the V_{CE} sharing regulation period, the $V_{GS,PIN,LS}$ measured at the MOSFET package pins can be considered as the chip V_{GS} for estimating the thermal losses of the auxiliary SiC MOSFET during the V_{CE} sharing regulation period.

Therefore, in the typical example shown in Figure 6.9 featuring strong V_{CE} diverging factors, for the loss estimation it can be approximated that during the V_{CE} sharing regulation period the V_{GS} reaches 5 V rapidly and then decreases near exponentially to 2.7 V. According to the transfer characteristics of the auxiliary SiC MOSFET, Figure 6.11 [209] (b), at V_{GS} = 2.7 V the $I_{D,sat}$ is near zero. Therefore, as $I_{D,sat} \propto (V_{GS} - V_{TH})^2$, the I_D of the auxiliary SiC MOSFET during the V_{CE} sharing regulation period i_{VR} can be approximated as:

$$i_{VR} \approx i_{VR0} e^{-\frac{t_{VR}}{\tau_{VR}}} \quad \text{Equation 6.2}$$

where i_{VR0} is the initial value of the i_{VR}, t_{VR} is the relative time from the beginning of the V_{CE} sharing regulation period, τ_{VR} is the time constant in the exponential approximation of the decrease of the i_{VR} in the V_{CE} sharing regulation period. Considering the observed decrease of the

Figure of capacitance characteristics removed for copyright reasons. Copyright holder is Cree, Inc.

(a)

Figure of transfer characteristics removed for copyright reasons. Copyright holder is Cree, Inc.

(b)

Figure of power dissipation characteristics removed for copyright reasons. Copyright holder is Cree, Inc.

(c)

Figure of safe operating area removed for copyright reasons. Copyright holder is Cree, Inc.

(d)

Figure 6.11: Typical characteristics of the auxiliary SiC MOSFET from the datasheet [209]: (a) capacitances vs. V_{DS}, (b) transfer characteristics, (c) maximum dissipated power vs. case temperature, (d) safe operating area.

V_{GS} in the V_{CE} sharing regulation period T_{VR} of 4.6 µs, the τ_{VR} can be estimated at 1 µs. According to Figure 6.11 [209] (b), assuming the maximum operating junction temperature T_J = 150 °C where the $I_{D,sat}$ is the highest at a given V_{GS}, at the peak $V_{GS,PIN,LS}$ of 5 V considering its difference from the chip V_{GS} due to the internal gate resistance, the peak $I_{D,sat}$ is estimated at 2 A, which is the i_{VR0} here.

The thermal losses of the auxiliary SiC MOSFET in the V_{CE} sharing regulation process here can be approximated using Equation 6.2 as:

$$E_{VR} = \int_0^{T_{VR}} v_{DS} i_{VR}\, dt_{VR} \approx \int_0^{T_{VR}} \frac{1}{2} V_{DC} i_{VR0} e^{-\frac{t_{VR}}{\tau_{VR}}}\, dt_{VR} = \frac{1}{2} V_{DC} i_{VR0} \int_0^{T_{VR}} e^{-\frac{t_{VR}}{\tau_{VR}}}\, dt_{VR} \quad \text{Equation 6.3}$$
$$= \frac{1}{2} V_{DC} i_{VR0} \left(\tau_{VR} - \tau_{VR} e^{-\frac{T_{VR}}{\tau_{VR}}}\right) \approx \frac{1}{2} V_{DC} i_{VR0} \tau_{VR} = 400V \times 2A \times 1\mu s$$
$$= 800\mu J$$

Considering a high switching frequency f_{SW} of 10 kHz for typical 1700 V Si IGBTs, the dissipated power of the auxiliary SiC MOSFET related to the V_{CE} sharing regulation process here is:

$$P_{VR} = E_{VR} f_{SW} = 800\mu J \times 10kHz = 8W \quad \text{Equation 6.4}$$

Considering a high case temperature T_C of the auxiliary SiC MOSFET of 120 °C, the maximum dissipated power of the SiC MOSFET at T_C = 120 °C is approx. 45 W, Figure 6.11 [209] (c). Since the auxiliary SiC MOSFET here is only active in the V_{CE} sharing regulation period, under the high T_J and T_C assumed here, at a f_{SW} of 10 kHz a P_{VR} of 8 W is less than 20% of that 45 W thermal allowance. The V_{DS}-I_D trajectory of the auxiliary SiC MOSFET in this scenario assumed is inside the Safe Operating Area (SOA) in the datasheet of the SiC MOSFET, Figure 6.11 [209] (d). As the i_{VR0} is significantly lower than the rated I_D, the peak instant power of the auxiliary SiC MOSFET in the V_{CE} sharing regulation process is also considerably lower than that in a typical inductive turn-off event of the SiC MOSFET.

Depending on the V_{CE} diverging factors and the power circuit conditions, the dissipated power of the auxiliary SiC MOSFET in the V_{CE} sharing regulation process may increase. As shown in Figure 6.11 [209] (c), at lower case temperatures the maximum dissipated power increases to 80 W at 95 °C, 120 W at 70 °C, and 160 W at 45 °C. Improving the cooling conditions for the auxiliary SiC MOSFET can reduce the case temperature and increase the maximum dissipated power. This will assist the use of the external active V_{CE} sharing regulation in severe V_{CE} diverging situations and in the entire IGBT turn-off and turn-on.

6.3 Summary of the External Active V_{CE} Sharing Regulation

Here the external active V_{CE} sharing regulation via auxiliary SiC MOSFETs in parallel to the IGBTs is effective as demonstrated in the experiments. Due to the considerably smaller C_{GS} of the auxiliary SiC MOSFET of a low current rating, with the same feedback loop configuration of the AVC circuit, the response of the external active V_{CE} sharing regulation is improved compared with that of the direct active V_{CE} sharing regulation in Chapter 5. In the IGBT tail time, as the differential V_{CE} sharing regulation here regulates the V_{CE} sharing as it tends to diverge, the extent of the V_{CE} divergence remains low in the V_{CE} sharing regulation period, although not eliminated due to the small safety margin in the V_{CE} reference signal. The V_{CE} sharing after the V_{CE} sharing regulation is quasi-static and with a self-stabilising trend.

With a quick response of the auxiliary SiC MOSFET, the phase lag in the feedback loop of the AVC circuit can be reduced without compromising the control stability, which improves the control stability against mixed V_{CE} diverging features and enables the use of a simple and reliable controller. The external active V_{CE} sharing regulation is designed to operate in conjunction with the preconditioning stage of the direct active V_{CE} sharing regulation in Chapter 5. This preconditioning stage itself is essentially controlled discharging of the IGBT C_{GE} and has a predictable influence on the reliability of the IGBT gate oxide which is comparable with that in the equivalent stage of uncontrolled IGBT turn-off. The external active V_{CE} sharing regulation diverts the less predictable influence of the active V_{CE} sharing regulation on the gate oxide reliability from the critical load-carrying IGBTs to the auxiliary SiC MOSFETs. As the auxiliary SiC MOSFET is only required to provide a small current for a short V_{CE} sharing regulation period, the average dissipated power of the auxiliary SiC MOSFET in an IGBT switching cycle is low, which enables the use of SiC MOSFETs of a low current rating, provided that the cooling conditions are adequate and the SOA is not exceeded. Regarding the V_{CE} sharing regulation, enhancing the redundancy for the auxiliary SiC MOSFETs of a low current rating is less costly and more practical compared with that for the critical load-carrying IGBTs of a high current rating.

Chapter 7 Conclusions and Suggestions for Future Work

7.1 Conclusions

Electric energy conversion by power electronic systems is essential for today's electric power technologies. Modern FS IGBTs are popular in medium to high voltage power electronics, and the use of IGBTs in series connection is attractive in high voltage power electronic systems. However, evenly distributed V_{CE} sharing in uncontrolled turn-off of IGBTs in series is impractical to achieve. Hence, for the use of IGBTs in series, understanding, improving, and regulating the turn-off voltage sharing of IGBTs in series at IGBT device level are important.

The key V_{CE} diverging mechanisms are first discussed in the basic scenarios of the V_{CE} divergence in the fast V_{CE}-I_C transient and the tail time of hard-switched IGBT turn-off regarding the turn-off voltage sharing of modern FS IGBTs in direct series connection under typical inductive load conditions. These basic scenarios of the V_{CE} divergence are then used in different combinations to describe the individual V_{CE} divergence caused by seven V_{CE} diverging factors. To gain further insight into the V_{CE} divergence, an FEM trench-FS IGBT model is developed in Silvaco ATLAS and is calibrated towards an actual IGBT in terms of turn-off characteristics. Using this IGBT model, the simulations in Silvaco ATLAS MixedMode of two-in-series IGBT turn-off under uncontrolled, hard-switched, and inductive-load conditions with those seven V_{CE} diverging factors introduced individually are found to agree with the respective analyses of the seven V_{CE} diverging factors.

Based on the discussions of the key V_{CE} diverging mechanisms, six passive mitigation methods at IGBT device level are designed to improve the basis of the turn-off V_{CE} sharing via adjustments to IGBT operating conditions and internal parameters. The six passive mitigation methods are effective in the simulation tests. Appropriate application of some of these methods in combination is attractive as the individual drawbacks of these methods can be compensated for while maintaining or even improving the trade-off between the on-state losses and the turn-off losses. Due to the nature of passive approaches, the passive mitigation methods cannot regulate the V_{CE} sharing or considerably mitigate the V_{CE} divergence without significantly degrading the IGBT performance, where active voltage regulation methods are required. Nonetheless, the passive mitigation methods provide insights into the optimisation of IGBT operating conditions and internal parameters for improving the basis of the turn-off V_{CE} sharing.

Similarly, based on the discussions of the key V_{CE} diverging mechanisms, two active V_{CE} sharing regulation methods at IGBT device level are designed to regulate the turn-off V_{CE} sharing in the fast V_{CE}-I_C transient and the tail time in IGBT turn-off. The two active V_{CE} sharing regulation methods include a direct method via IGBT gate control and an external method via auxiliary SiC MOSFETs, both of which are based on the AVC scheme and the strategy of differential V_{CE} sharing regulation. The use of differential V_{CE} sharing regulation here aims to minimise the additional losses caused by the V_{CE} sharing regulation process and is based on hard-switched IGBT turn-off with a small gate resistance to achieve a high $\mathrm{d}V_{CE}/\mathrm{d}t$ rate in the fast V_{CE} rising.

The direct active V_{CE} sharing regulation is designed to reverse the mechanisms that cause the V_{CE} divergence directly via IGBT gate control. The low-loss preconditioning stage is redesigned from the implementations in the previous relevant researches to reduce the additional losses caused by the preconditioning stage. The differential V_{CE} sharing regulation aims to regulate the V_{CE} sharing as it tends to diverge for maintaining a low extent of the V_{CE} divergence. As the differences between the IGBTs related to the V_{CE} divergence are reduced in the V_{CE} sharing regulation process, the V_{CE} sharing regulation period is not required to cover the entire IGBT tail time for achieving quasi-static V_{CE} sharing in the following IGBT off-state.

The direct active V_{CE} sharing regulation is effective as demonstrated in the experiments. The V_{CE} sharing regulation process is stable, and the extent of the V_{CE} divergence remains low in the V_{CE} sharing regulation period. The short V_{CE} sharing regulation period in the tail time is adequate to achieve quasi-static V_{CE} sharing with a self-stabilising trend in the following IGBT off-state. The redesigned preconditioning stage and the differential V_{CE} sharing regulation strategy with hard-switched IGBT turn-off significantly reduce the additional losses and the EMI caused by the V_{CE} sharing regulation process, which enhances the practicality of the direct active V_{CE} sharing regulation.

The external active V_{CE} sharing regulation is designed to reverse the mechanisms that cause the V_{CE} divergence externally via auxiliary SiC MOSFETs, and is designed to operate in conjunction with the preconditioning stage in the direct active V_{CE} sharing regulation. The external active V_{CE} sharing regulation also aims to regulate the V_{CE} sharing as it tends to diverge for maintaining a low extent of the V_{CE} divergence. Same as the direct active V_{CE} sharing regulation, here the V_{CE} sharing regulation period is also not required to cover the entire IGBT tail time for achieving quasi-static V_{CE} sharing in the following IGBT off-state.

The external active V_{CE} sharing regulation is effective as demonstrated in the experiments. The V_{CE} sharing regulation process is stable, and the extent of the V_{CE} divergence remains low in the V_{CE} sharing regulation period. Same as the direct active V_{CE} sharing regulation, here the short V_{CE} sharing regulation period in the IGBT tail time is also adequate to achieve quasi-static V_{CE} sharing with a self-stabilising trend in the following IGBT off-state. With the auxiliary SiC MOSFET of a low current rating, the response of the V_{CE} sharing regulation is improved while maintaining a stable V_{CE} sharing regulation process, which enhances the practicality of the external active V_{CE} sharing regulation. Here the influence of the V_{CE} sharing regulation on the gate oxide reliability is diverted from the IGBTs to the auxiliary SiC MOSFETs. The average dissipated power of the auxiliary SiC MOSFET in an IGBT switching cycle is low, which enables the use of SiC MOSFETs of a low current rating under adequate cooling conditions. Regarding the V_{CE} sharing regulation, enhancing the redundancy for the auxiliary SiC MOSFETs of a low current rating is less costly and more practical compared with that for the IGBTs of a high current rating.

The passive mitigation methods and the active regulation methods here are practical and are applicable to the actual use of IGBTs operated in series connection. The potential improvements in the implementations of the two active V_{CE} sharing regulation methods are intended for the future work.

7.2 Suggestions for Future Work

7.2.1 Modelling and Advanced Optimisation in Simulation

The 2D IGBT model used in the simulations in Chapter 3 and 4 is adequate to study the basic principles of the V_{CE} divergence without consuming considerable computing resources. The discussions of the IGBT modelling in Chapter 3 suggest that simulation of the V_{CE} divergence of modern IGBTs can benefit from an IGBT model based on a 3D structure to reflect the modern trend in IGBT design. An IGBT model designed using fabrication data and/or processing simulation results is preferable. In addition, an extension of the theoretical study and an IGBT model including multiple IGBT cells with controlled parameter differences between them can provide further insights into the V_{CE} diverging mechanisms.

Here the IGBT model in the simulations uses a fixed mesh, which is robust but consumes more computing resources than an adaptive mesh. As the IGBT internal conditions change in turn-off, an adaptive mesh that tracks the steep gradients of the key internal variables and adjusts the mesh density appropriately can improve the trade-off between simulation accuracy and computing resource consumption, especially when using a 3D IGBT model with multiple cells.

The average operating conditions for the IGBTs in the simulations are in typical ranges. Studies of the V_{CE} divergence under abnormal IGBT operating conditions will be useful for the protection aspect of operating IGBTs in series connection. Also, the inclusion of external factors such as parasitic capacitances under high voltages in the CCL will contribute to a more comprehensive study of the V_{CE} divergence. The study of the V_{CE} sharing under other load conditions will be attractive for innovative IGBT based converters.

The discussion of the passive mitigation methods in Chapter 4 provides some insights into the optimisation of IGBT operating conditions and internal parameters for improving the basis of the V_{CE} sharing. Since changes in IGBT operating conditions and internal parameters also affect other IGBT performance aspects, advanced optimisation considering the basis of the V_{CE} sharing and the trade-off between switching and on-state performance aspects will be useful for improving the overall performance of operating IGBTs in series connection under given load conditions. An improved basis of the V_{CE} sharing reduces the requirements for the active V_{CE} sharing regulation. The simulation of the V_{CE} divergence can be developed to estimate the requirements for the active V_{CE} sharing regulation.

In addition, theoretical and simulation studies of the V_{CE} divergence in IGBT turn-on are essential for operating IGBTs in series connection.

7.2.2 Advancing the Active V_{CE} Sharing Regulation Methods

The two active V_{CE} sharing regulation methods discussed in Chapter 5 and 6 are effective, but their design concepts cannot be demonstrated to their full potential due to limits in the experimental implementations. Synchronised clock sources or a clock signal distribution system for the FPGAs on the AVC gate drives is useful to provide predictable timings of the V_{CE} reference signal. A high-performance FPGA and a high-performance DAC that can achieve V_{CE} reference

signal generation of high flexibility and high resolutions are essential for closely tracing the predicted average V_{CE} trajectory in the V_{CE} reference signal.

Automated V_{CE} reference signal generation is essential for the application of the active V_{CE} sharing regulation methods. For this, prediction of the average V_{CE} trajectory requires a fast IGBT model and fast load condition sensing. A communication system between the AVC gate drives and the central controller can be useful for obtaining load conditions. A high-performance FPGA is also required for fast prediction of the average V_{CE} trajectory.

Protection is critical for operating IGBTs in series connection. The protection will require studies of failure scenarios and protection strategies with implementations. Reliability prediction of the IGBTs and the auxiliary SiC MOSFETs will be required for the application of the active V_{CE} sharing regulation methods.

In addition, studies of the use of the active V_{CE} sharing regulation methods in IGBT turn-on are essential for operating IGBTs in series connection.

Bibliography

[1] J. Bardeen and W. H. Brattain, "The Transistor, A Semi-Conductor Triode," *Phys. Rev.*, vol. 74, no. 2, pp. 230–231, Jul. 1948.

[2] R. N. Hall, "Power Rectifiers and Transistors," *Proceedings of the IRE*, vol. 40, no. 11. pp. 1512–1518, 1952.

[3] X. She, A. Q. Huang, O. Lucia, and B. Ozpineci, "Review of Silicon Carbide Power Devices and Their Applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, Oct. 2017.

[4] E. A. Jones, F. F. Wang, and D. Costinett, "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 3, pp. 707–719, Sep. 2016.

[5] J. L. Moll, M. Tanenbaum, J. M. Goldey, and N. Holonyak, "P-N-P-N Transistor Switches," *Proceedings of the IRE*, vol. 44, no. 9. pp. 1174–1182, 1956.

[6] A. S. Grove, *Physics and Technology of Organic Semiconductor Devices*, vol. 1115. Wiley, 2010.

[7] E. D. Wolley, "Gate turn-off in p-n-p-n devices," *Electron Devices, IEEE Transactions on*, vol. ED-13, no. 7. pp. 590–597, 1966.

[8] P. K. Steimer, H. E. Gruning, J. Werninger, E. Carroll, S. Klaka, and S. Linder, "IGCT-a new emerging technology for high power, low cost inverters," *Industry Applications Conference, 1997. Thirty-Second IAS Annual Meeting, IAS '97., Conference Record of the 1997 IEEE*, vol. 2. pp. 1592–1599 vol.2, 1997.

[9] F. P. Heiman, "The silicon insulated-gate field-effect transistor," *Proceedings of the IEEE*, vol. 51, no. 9. pp. 1190–1202, 1963.

[10] D. A. Grant and J. Gowar, *Power MOSFETS: theory and applications*. Wiley, 1989.

[11] B. J. Baliga, M. S. Adler, P. V Gray, R. P. Love, and N. Zommer, "The insulated gate rectifier (IGR): A new power switching device," *Electron Devices Meeting, 1982 International*, vol. 28. pp. 264–267, 1982.

[12] M. F. Chang, G. C. Pifer, B. J. Baliga, M. S. Adler, and P. V Gray, "25 amp, 500 volt insulated gate transistors," *Electron Devices Meeting, 1983 International*, vol. 29. pp. 83–86, 1983.

[13] B. J. Baliga, "Fast-switching insulated gate transistors," *Electron Device Letters, IEEE*, vol. 4, no. 12. pp. 452–454, 1983.

[14] B. J. Baliga, M. S. Adler, R. P. Love, P. V Gray, and N. D. Zommer, "The insulated gate transistor: A new three-terminal MOS-controlled bipolar power device," *Electron Devices, IEEE Transactions on*, vol. 31, no. 6. pp. 821–828, 1984.

[15] J. P. Russell, A. M. Goodman, L. A. Goodman, and J. M. Neilson, "The COMFET - A new high conductance MOS-gated device," *Electron Device Letters, IEEE*, vol. 4, no. 3. pp. 63–65, 1983.

[16] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*, 1st ed. Springer, 2008.

[17] B. J. Baliga, *Advanced High Voltage Power Device Concepts*, 1st ed. New York, NY: Springer New York, 2012.

[18] C. Blake and C. Bull, "IGBT or MOSFET: Choose Wisely," *Int. Rectifier*, 2001.

[19] C. Ambarian and C. Chao, "WARP Speed IGBTs-switching at 100 to 150 kHz in power

converter applications," *Wescon/97. Conference Proceedings*. pp. 276–280, 1997.

[20] J. W. Slotboom and H. C. de Graaff, "Measurements of bandgap narrowing in Si bipolar transistors," *Solid State Electron.*, vol. 19, no. 10, pp. 857–862, Oct. 1976.

[21] M. A. Green, "Intrinsic concentration, effective densities of states, and effective mass in silicon," *J. Appl. Phys.*, vol. 67, no. 6, pp. 2944–2954, 1990.

[22] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. John Wiley & Sons, 2006.

[23] A. B. Sproul and M. A. Green, "Improved value for the silicon intrinsic carrier concentration from 275 to 375 K," *J. Appl. Phys.*, 1991.

[24] A. G. Chynoweth, "Ionization Rates for Electrons and Holes in Silicon," *Phys. Rev.*, vol. 109, no. 5, pp. 1537–1540, Mar. 1958.

[25] R. Van Overstraeten and H. De Man, "Measurement of the ionization rates in diffused silicon p-n junctions," *Solid State Electron.*, vol. 13, no. 5, pp. 583–608, May 1970.

[26] W. N. Grant, "Electron and hole ionization rates in epitaxial silicon at high electric fields," *Solid State Electron.*, 1973.

[27] W. Maes, K. De Meyer, and R. Van Overstraeten, "Impact ionization in silicon: A review and update," *Solid State Electron.*, 1990.

[28] D. B. M. Klaassen, "A unified mobility model for device simulation-I. Model equations and concentration dependence," *Solid State Electron.*, vol. 35, no. 7, pp. 953–959, Jul. 1992.

[29] D. B. M. Klaassen, "A unified mobility model for device simulation-II. Temperature dependence of carrier mobility and lifetime," *Solid State Electron.*, vol. 35, no. 7, pp. 961–967, Jul. 1992.

[30] D. M. Caughey and R. E. Thomas, "Carrier Mobilities in Silicon Empirically Related to Doping and Field," *Proc. IEEE*, 1967.

[31] C. Jacoboni, C. Canali, G. Ottaviani, and A. Alberigi Quaranta, "A review of some charge transport properties of silicon," *Solid State Electron.*, 1977.

[32] C. Canali, G. Majni, R. Minder, and G. Ottaviani, "Electron and Hole Drift Velocity Measurements in Silicon and Their Empirical Relation to Electric Field and Temperature," *IEEE Trans. Electron Devices*, 1975.

[33] K. K. Thornber, "Relation of drift velocity to low-field mobility and high-field saturation velocity," *J. Appl. Phys.*, 1980.

[34] G. Masetti, M. Severi, and S. Solmi, "Modeling of Carrier Mobility Against Carrier Concentration in Arsenic-, Phosphorus-, and Boron-Doped Silicon," *IEEE Trans. Electron Devices*, 1983.

[35] M. S. Adler and G. E. Possin, "Achieving Accuracy in Transistor and Thyristor Modeling," *IEEE Trans. Electron Devices*, 1981.

[36] A. R. Hefner and D. M. Diebolt, "An Experimentally Verified IGBT Model Implemented in the Saber Circuit Simulator," *IEEE Trans. Power Electron.*, 1994.

[37] P. A. Mawby, Z. R. Hu, M. S. Towers, M. J. Evans, and K. Board, "Recombination and Joule heating effects in GTO thyristors with spatially varying lifetimes," *IEE Proc. Circuits, Devices Syst.*, 1994.

[38] S. C. Sun and J. D. Plummer, "Electron Mobility in Inversion and Accumulation Layers on Thermally Oxidized Silicon Surfaces," *IEEE J. Solid-State Circuits*, 1980.

[39] C. Lombardi, S. Manzini, A. Saporito, and M. Vanzi, “A Physically Based Mobility Model for Numerical Simulation of Nonplanar Devices,” *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 7, no. 11, pp. 1164–1171, 1988.

[40] M. S. Adler, “Accurate calculations of the forward drop and power dissipation in thyristors,” *IEEE Trans. Electron Devices*, 1978.

[41] N. Iwamuro, A. Okamoto, S. Tagami, and H. Motoyama, “Numerical Analysis of Short-Circuit Safe Operating Area for p-Channel and n-Channel IGBT’s,” *IEEE Trans. Electron Devices*, vol. 38, no. 2, pp. 303–309, 1991.

[42] V. K. Khanna, “Carrier lifetimes and recombination-generation mechanisms in semiconductor device physics,” *Eur. J. Phys.*, 2004.

[43] D. K. Schröder, “Carrier lifetimes in silicon,” *IEEE Trans. Electron Devices*, 1997.

[44] W. Shockley and W. T. Read, “Statistics of the recombinations of holes and electrons,” *Phys. Rev.*, vol. 87, no. 5, pp. 835–842, Sep. 1952.

[45] R. N. Hall, “Electron-hole recombination in germanium,” *Phys. Rev.*, vol. 87, no. 2, p. 387, Jul. 1952.

[46] C. T. Sah, R. N. Noyce, and W. Shockley, “Carrier Generation and Recombination in P-N Junctions and P-N Junction Characteristics,” *Proc. IRE*, 1957.

[47] D. J. Roulston, N. D. Arora, and S. G. Chamberlain, “Modeling and Measurement of Minority-Carrier Lifetime versus Doping in Diffused Layers of n +-p Silicon Diodes,” *IEEE Trans. Electron Devices*, vol. 29, no. 2, pp. 284–291, Feb. 1982.

[48] J. G. Fossum and D. S. Lee, “A physical model for the dependence of carrier lifetime on doping density in nondegenerate silicon,” *Solid State Electron.*, vol. 25, no. 8, pp. 741–747, Aug. 1982.

[49] M. E. Law, E. Solley, M. Liang, and D. E. Burk, “Self-Consistent Model of Minority-Carrier Lifetime, Diffusion Length, and Mobility,” *IEEE Electron Device Lett.*, vol. 12, no. 8, pp. 401–403, Aug. 1991.

[50] L. Huldt, “Band-to-band auger recombination in indirect gap semiconductors,” *Phys. Status Solidi*, vol. 8, no. 1, pp. 173–187, Nov. 1971.

[51] J. Dziewior and W. Schmid, “Auger coefficients for highly doped and highly excited silicon,” *Appl. Phys. Lett.*, vol. 31, no. 5, p. 346, Oct. 1977.

[52] K. G. Svantesson and N. G. Nilsson, “Measurement of Auger recombination in silicon by laser excitation,” *Solid. State. Electron.*, vol. 21, no. 11–12, pp. 1603–1608, Nov. 1978.

[53] A. Haug, “Carrier density dependence of Auger recombination,” *Solid. State. Electron.*, vol. 21, no. 11–12, pp. 1281–1284, Nov. 1978.

[54] M. J. Kerr and A. Cuevas, “General parameterization of Auger recombination in crystalline silicon,” *J. Appl. Phys.*, 2002.

[55] A. Richter, S. W. Glunz, F. Werner, J. Schmidt, and A. Cuevas, “Improved quantitative description of Auger recombination in crystalline silicon,” *Phys. Rev. B - Condens. Matter Mater. Phys.*, 2012.

[56] L. Huldt, N. G. Nilsson, and K. G. Svantesson, “The temperature dependence of band-to-band Auger recombination in silicon,” *Appl. Phys. Lett.*, vol. 35, no. 10, pp. 776–777, Nov. 1979.

[57] R. A. Sinton and R. M. Swanson, “Recombination in Highly Injected Silicon,” *IEEE Trans. Electron Devices*, 1987.

[58] S. Selberherr, *Analysis and Simulation of Semiconductor Devices*. Vienna: Springer Vienna, 1984.

[59] N. Iwamuro and T. Laska, "IGBT History, State-of-the-Art, and Future Prospects," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 741–752, Mar. 2017.

[60] T. Laska, M. Münzer, F. Pfirsch, C. Schaeffer, and T. Schmidt, "The field stop IGBT (FS IGBT) - A new power device concept with a great improvement potential," in *IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2000, no. figure 2, pp. 355–358.

[61] K. Nakamura, S. Kusunoki, H. Nakamura, Y. Ishimura, Y. Tomomatsu, and T. Minato, "Advanced wide cell pitch CSTBTs having Light Punch-Through (LPT) structures," in *IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2002, pp. 277–280.

[62] M. Rahimo, A. Kopta, and S. Linder, "Novel enhanced-planar IGBT technology rated up to 6.5kV for lower losses and higher SOA capability," in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, 2006.

[63] W. M. Webster, "On the variation of junction-transistor current-amplification factor with emitter current," *Proc. IRE*, 1954.

[64] C. T. Kirk, "A Theory of Transistor Cutoff Frequency (Ft) Falloff at High Current Densities," *IRE Trans. Electron Devices*, vol. 9, no. 2, pp. 164–174, 1962.

[65] H. C. Poon, H. K. Gummel, and D. L. Scharfetter, "High Injection in Epitaxial Transistors," *IEEE Trans. Electron Devices*, vol. 16, no. 5, pp. 455–457, 1969.

[66] R. J. Whittier and D. A. Tremere, "Current Gain and Cutoff Frequency Falloff at High Currents," *IEEE Trans. Electron Devices*, vol. 16, no. 1, pp. 39–57, 1969.

[67] M. S. Mock, "Transport equations in heavily doped silicon, and the current gain of a bipolar transistor," *Solid State Electron.*, 1973.

[68] G. M. Kull, L. W. Nagel, S. W. Lee, P. Lloyd, E. J. Prendergast, and H. Dirks, "A Unified Circuit Model for Bipolar Transistors Including Quasi-Saturation Effects," *IEEE Trans. Electron Devices*, 1985.

[69] W. Shockley, "A unipolar 'field-effect' transistor," *Proc. IRE*, vol. 40, no. 11, pp. 1365–1376, 1952.

[70] T. Sakurai and A. R. Newton, "Alpha-Power Law MOSFET Model and its Applications to CMOS Inverter Delay and Other Formulas," *IEEE J. Solid-State Circuits*, vol. 25, no. 2, pp. 584–594, 1990.

[71] T. Sakurai and A. Richard Newton, "A Simple MOSFET Model for Circuit Analysis," *IEEE Trans. Electron Devices*, vol. 38, no. 4, pp. 887–894, 1991.

[72] L. VADASZ and A. S. GROVE, "Temperature Dependence of MOS Transistor Characteristics Below Saturation," *IEEE Trans. Electron Devices*, vol. ED-13, no. 12, pp. 863–866, 1966.

[73] T. Yamazaki, Y. Onozawa, M. Otsuki, N. Fujishima, and Y. Seki, "Advanced IGBT chip technology for industrial motor drive applications," *Power Electron. Conf. (IPEC), 2010 Int.*, pp. 783–789, 2010.

[74] Y. Onozawa, D. Ozaki, H. Nakano, T. Yamazaki, and N. Fujishima, "Development of the next generation 1700V trench-gate FS-IGBT," in *2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs*, 2011, pp. 52–55.

[75] T. Ogura, H. Ninomiya, K. Sugiyama, and T. Inoue, "Turn-off switching analysis

considering dynamic avalanche effect for low turn-off loss high-voltage IGBTs," *IEEE Trans. Electron Devices*, vol. 51, no. 4, pp. 629–635, Apr. 2004.

[76] A. R. Hefner and D. L. Blackburn, "An analytical model for the steady-state and transient characteristics of the power insulated-gate bipolar transistor," *Solid State Electron.*, 1988.

[77] W. Van Roosbroeck, "The transport of added current carriers in a homogeneous semiconductor," *Phys. Rev.*, 1953.

[78] A. Simon, "Ambipolar Diffusion in a Magnetic Field," *Plutonium Proj. Rec. Eq. Phys. Rev. Phys. Rev*, vol. 5, no. 93, pp. 197–201, 1955.

[79] F. E. Geiger and F. G. Cunningham, "Ambipolar Diffusion in Semiconductors," *Am. J. Phys.*, vol. 32, no. 5, pp. 336–342, May 1964.

[80] M. A. (Michael A. . Lieberman and A. J. Lichtenberg, *Principles of plasma discharges and materials processing*. Wiley-Interscience, 2005.

[81] M. J. Kushner, "DERIVATION OF AMBIPOLAR DIFFUSION COEFFICIENT AND AMBIPOLAR ELECTRIC FIELD," *Physical Processes in Plasmas*, 2012. [Online]. Available: http://uigelz.eecs.umich.edu/classes/pub/eecs517/handouts/derivation_ambipolar_diffusion_v02.pdf.

[82] A. Bryant *et al.*, "Investigation into IGBT dV/dt during turn-off and its temperature dependence," *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 3019–3031, Oct. 2011.

[83] T. Ogura, H. Ninomiya, K. Sugiyama, and T. Inoue, "4.5-kV injection-enhanced gate transistors (IEGTs) with high turn-off ruggedness," *IEEE Trans. Electron Devices*, vol. 51, no. 4, pp. 636–641, Apr. 2004.

[84] A. Kopta, M. Rahimo, U. Schlapbach, D. Schneider, E. Carroll, and S. Linder, "A 6.5kV IGBT module with very high Safe operating area," in *Conference Record - IAS Annual Meeting (IEEE Industry Applications Society)*, 2005, vol. 2, pp. 794–798.

[85] S. Machida, K. Ito, and Y. Yamashita, "Approaching the limit of switching loss reduction in Si-IGBTs," in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, 2014, pp. 107–110.

[86] Fuji Electric Co. Ltd., "FUJI IGBT MODULES APPLICATION MANUAL," 2017.

[87] P. Rose, D. Silber, A. Porst, and F. Pfirsch, "Investigations on the stability of dynamic avalanche in IGBTs," in *IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2002, pp. 165–168.

[88] "IGBT Modules Dynex Semiconductor, Lincoln, UK." [Online]. Available: http://www.dynexsemi.com/product-area/igbt-modules.

[89] "IGBT-Insulated Gate Bipolar Transistor and IGBTs Product Information." [Online]. Available: http://www.pwrx.com/summary/IGBT/IGBT.aspx.

[90] "MITSUBISHI ELECTRIC Semiconductors & Devices: Product Information | Power Modules [HVIGBT Modules/HVIPM]." [Online]. Available: http://www.mitsubishielectric.com/semiconductors/products/powermod/hvigbtmod/index.html.

[91] "Insulated Gate Bipolar Transistors (IGBTs) : Hitachi PDD." [Online]. Available: http://www.hitachi.eu/pdd/products/igbt/.

[92] "Insulated gate bipolar transistor (IGBT) and diode modules | ABB." [Online]. Available: http://new.abb.com/semiconductors/igbt-and-diode-modules.

[93] “IGBT Modules - Infineon Technologies.” [Online]. Available: http://www.infineon.com/cms/en/product/power/igbt/igbt-module/channel.html?channel=ff80808112ab681d0112ab69e66f0362.

[94] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, “A Survey of Wide Bandgap Power Semiconductor Devices,” *IEEE Transactions on Power Electronics*, vol. 29, no. 5. pp. 2155–2163, 2014.

[95] T. Fujihira, M. Otsuki, O. Ikawa, A. Nishiura, and N. Fujishima, “The State-of-The-Art and Future Trend of Power Semiconductor Devices,” *Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. pp. 1–8, 2015.

[96] S. Chowdhury and T. P. Chow, “Performance tradeoffs for ultra-high voltage (15 kV to 25 kV) 4H-SiC n-channel and p-channel IGBTs,” *2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*. pp. 75–78, 2016.

[97] K. Fukuda *et al.*, “Development of Ultrahigh-Voltage SiC Devices,” *IEEE Transactions on Electron Devices*, vol. 62, no. 2. pp. 396–404, 2015.

[98] K. Fukuda *et al.*, “Development of ultrahigh voltage SiC power devices,” *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*. pp. 3440–3446, 2014.

[99] X. Wang and J. A. Cooper, “High-Voltage n-Channel IGBTs on Free-Standing 4H-SiC Epilayers,” *IEEE Transactions on Electron Devices*, vol. 57, no. 2. pp. 511–515, 2010.

[100] Q. Zhang, M. Das, J. Sumakeris, R. Callanan, and A. Agarwal, “12-kV p-Channel IGBTs With Low On-Resistance in 4H-SiC,” *IEEE Electron Device Letters*, vol. 29, no. 9. pp. 1027–1029, 2008.

[101] S. Chowdhury, C. Hitchcock, Z. Stum, R. Dahal, I. B. Bhat, and T. P. Chow, “4H-SiC n-Channel Insulated Gate Bipolar Transistors on (0001) and (000-1) Oriented Free-Standing n− Substrates,” *IEEE Electron Device Letters*, vol. 37, no. 3. pp. 317–320, 2016.

[102] T. Kimoto, J. Suda, Y. Yonezawa, K. Asano, K. Fukuda, and H. Okumura, “Progress in ultrahigh-voltage SiC devices for future power infrastructure,” *2014 IEEE International Electron Devices Meeting*. pp. 2.5.1-2.5.4, 2014.

[103] “Siemens - HVDC Classic.” [Online]. Available: http://www.energy.siemens.com/hq/en/power-transmission/hvdc/hvdc-classic.htm.

[104] “HVDC Classic technology | ABB.” [Online]. Available: http://new.abb.com/systems/hvdc/hvdc-classic.

[105] “Siemens - HVDC PLUS (VSC Technology).” [Online]. Available: http://www.energy.siemens.com/hq/en/power-transmission/hvdc/hvdc-plus.htm.

[106] “HVDC Light technology | ABB.” [Online]. Available: http://new.abb.com/systems/hvdc/hvdc-light.

[107] “Medium Voltage Converters - Drive Technology - Siemens.” [Online]. Available: http://www.industry.siemens.com/drives/global/en/converter/mv-drives/Pages/medium-voltage-converters.aspx.

[108] “Medium voltage AC - ABB Drives.” [Online]. Available: http://new.abb.com/drives/medium-voltage-ac-drives.

[109] A. Hassanpoor, Y. J. Hafner, A. Nami, and K. Vinothkumar, “Cost-effective solutions for handling dc faults in VSC HVDC transmission,” in *2016 18th European Conference*

on Power Electronics and Applications, EPE 2016 ECCE Europe, 2016, pp. 1–7.

[110] K. Eriksson, T. Jonsson, and O. Tollerz, "Small scale transmission to AC networks by HVDC light," *12th Cepsi*, 1998.

[111] G. Asplund, K. Eriksson, and O. Tollerz, "HVDC light, a tool for electric power transmission to distant loads," *VI SEPOPE Conf. Salvador.*, 1998.

[112] L. Weimers, "HVDC light: a new technology for a better environment," *IEEE Power Eng. Rev.*, 1998.

[113] U. Axelsson, A. Holm, and C. Liljegren, "Gotland HVDC light transmission—world's first commercial small scale dc transmission," *CIRED*, 1999.

[114] R. Grünbaum and B. Halvarsson, "FACTS and HVDC light for power system interconnections," *Power Deliv.*, 1999.

[115] G. Asplund, "Application of HVDC Light to power system enhancement," in *2000 IEEE Power Engineering Society, Conference Proceedings*, 2000, vol. 4, pp. 2498–2503.

[116] K. Eriksson, "HVDC Light^{TM} and development of Voltage Source Converters," in *IEEE/PES T&D 2002 Latin American Conference*, 2002.

[117] K. Sharifabadi, L. Harnefors, H.-P. Nee, S. Norrga, and R. Teodorescu, *Design, Control and Application of Modular Multilevel Converters for HVDC Transmission Systems*. Chichester, UK: John Wiley & Sons, Ltd, 2016.

[118] ABB, "It's time to connect," 2013. [Online]. Available: https://library.e.abb.com/public/2742b98db321b5bfc1257b26003e7835/Pow0038 R7 LR.pdf.

[119] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," *Power Tech Conf.*, 2003.

[120] M. Glinka, "Prototype of multiphase modular-multilevel-converter with 2 MW power rating and 17-level-output-voltage," *Electron. Spec. Conf. 2004. PESC 04. ...*, 2004.

[121] H.-J. Knaak, "Modular multilevel converters and HVDC/FACTS: A success story," *Power Electron. Appl. (EPE 2011), Proc. 2011-14th Eur. Conf.*, no. Lcc, pp. 1–6, 2011.

[122] S. P. Teeuwsen, "Modeling the Trans Bay Cable Project as Voltage-Sourced Converter with Modular Multilevel Converter design," in *2011 IEEE Power and Energy Society General Meeting*, 2011, pp. 1–8.

[123] M. Davies, M. Dommaschk, J. Dorn, J. Lang, D. Retzmann, and D. Soerangr, "HVDC PLUS – Basics and Principle of Operation." [Online]. Available: http://www.energy.siemens.com/hq/pool/hq/power-transmission/HVDC/HVDC_Plus_Basic and Principals.pdf.

[124] M. M. C. Merlin *et al.*, "The alternate arm converter: A new hybrid multilevel converter with DC-fault blocking capability," *IEEE Trans. Power Deliv.*, vol. 29, no. 1, pp. 310–317, 2014.

[125] E. Solas, G. Abad, J. A. Barrena, S. Aurtenetxea, A. Carcar, and L. Zajac, "Modular Multilevel Converter With Different Submodule Concepts—Part I: Capacitor Voltage Balancing Method," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4525–4535, Oct. 2013.

[126] C. Davidson and D. Trainer, "Innovative concepts for hybrid multi-level converters for HVDC power transmission," *Ac dc Power Transm.*, 2010.

[127] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for HVDC applications: Review on converter cells and functionalities," *IEEE*

Transactions on Power Electronics, vol. 30, no. 1. pp. 18–36, Jan-2015.

[128] A. Nami, J. Liang, F. Dijkhuizen, and P. Lundberg, "Analysis of modular multilevel converters with DC short circuit fault blocking capability in bipolar HVDC transmission systems," in *2015 17th European Conference on Power Electronics and Applications, EPE-ECCE Europe 2015*, 2015, pp. 1–10.

[129] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "VSC-Based HVDC Power Transmission Systems: An Overview," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 592–602, Mar. 2009.

[130] A. Shukla and G. D. Demetriades, "A Survey on Hybrid Circuit-Breaker Topologies," *IEEE Trans. Power Deliv.*, vol. 30, no. 2, pp. 627–641, Apr. 2015.

[131] A. M. S. Atmadji and J. G. J. Sloot, "Hybrid switching: a review of current literature," in *Proceedings of EMPD '98. 1998 International Conference on Energy Management and Power Delivery (Cat. No.98EX137)*, vol. 2, pp. 683–688.

[132] P. van Gelder and J. A. Ferreira, "Zero volt switching hybrid DC circuit breakers," in *Conference Record of the 2000 IEEE Industry Applications Conference. Thirty-Fifth IAS Annual Meeting and World Conference on Industrial Applications of Electrical Energy (Cat. No.00CH37129)*, vol. 5, pp. 2923–2927.

[133] Y. Tang, J. L. Duarte, R. P. P. Smeets, T. E. Motoasca, and E. A. Lomonova, "Multi-stage DC hybrid switch with slow switching," in *IECON Proceedings (Industrial Electronics Conference)*, 2011, pp. 1462–1467.

[134] J. Magnusson, A. Bissai, G. Engdahl, J. A. Martinez, and L. Liljestrand, "Experimental study of the current commutation in hybrid DC-breakers," in *2015 3rd International Conference on Electric Power Equipment – Switching Technology (ICEPE-ST)*, 2015, pp. 506–511.

[135] A. Hassanpoor, J. Hafner, and B. Jacobson, "Technical Assessment of Load Commutation Switch in Hybrid HVDC Breaker," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5393–5400, Oct. 2015.

[136] E. Dong, Chen Yushuo, Y. Wang, J. Zhao, and J. Zou, "Experimental study of high-speed hybrid circuit breaker used in fast isolation of faulty power," in *2013 2nd International Conference on Electric Power Equipment - Switching Technology (ICEPE-ST)*, 2013, pp. 1–4.

[137] L. Liljestrand, L. Jonsson, M. Backman, and M. Riva, "A new hybrid medium voltage breaker for DC interruption or AC fault current limitation," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, 2016, pp. 1–10.

[138] F. Zhang *et al.*, "Voltage balancing optimization of series-connected IGBTs in solid-state breaker by using driving signal adjustment technique," in *2015 IEEE 2nd International Future Energy Electronics Conference (IFEEC)*, 2015, pp. 1–5.

[139] M. Callavik, A. Blomberg, and J. Häfner, "The hybrid HVDC breaker," *ABB Grid Syst. Tech.*, 2012.

[140] L. Feng *et al.*, "Development of a 10kV solid-state DC circuit breaker based on press-pack IGBT for VSC-HVDC system," in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, 2016, pp. 2371–2377.

[141] C. C. Davidson and D. R. Trainer, "Innovative concepts for hybrid multi-level converters for HVDC power transmission," in *9th IET International Conference on AC and DC Power Transmission (ACDC 2010)*, 2010, pp. O51–O51.

[142] M. M. C. Merlin, T. C. Green, P. D. Mitcheson, D. R. Trainer, D. R. Critchley, and R. W. Crookes, “A new hybrid multi-level voltage-source converter with DC fault blocking capability,” in *9th IET International Conference on AC and DC Power Transmission (ACDC 2010)*, 2010, pp. O56–O56.

[143] R. Marquardt, “Modular Multilevel Converter topologies with DC-Short circuit current limitation,” in *8th International Conference on Power Electronics - ECCE Asia*, 2011, pp. 1425–1431.

[144] D. Van Hertem, O. Gomis-Bellmunt, and J. Liang, *HVDC Grids: For Offshore and Supergrid of the Future*. Wiley, 2016.

[145] M. M. C. Merlin *et al.*, “The Extended Overlap Alternate Arm Converter: A Voltage Source Converter with DC Fault Ride-Through Capability and a Compact Design,” *IEEE Trans. Power Electron.*, pp. 1–1, 2017.

[146] B. Jacobson, P. Karlsson, G. Asplund, L. Harnefors, and T. Jonsson, “VSC-HVDC transmission with cascaded two-level converters,” in *Cigré session*, 2010, pp. 1–8.

[147] J.-F. C. J.-F. Chen, J.-N. L. J.-N. Lin, and T.-H. A. T.-H. Ai, “The techniques of the serial and paralleled IGBTs,” *Proc. 1996 IEEE IECON. 22nd Int. Conf. Ind. Electron. Control. Instrum.*, vol. 2, pp. 999–1004, 1996.

[148] G. Busatto, B. Cascone, L. Fratelli, and A. Luciano, “Series connection of IGBTs in hard-switching applications,” *Conf. Rec. 1998 IEEE Ind. Appl. Conf. Thirty-Third IAS Annu. Meet. (Cat. No.98CH36242)*, vol. 2, pp. 825–830, 1998.

[149] R. Roesner, H. J. Fellow, and K. R. S. Member, “Cellular Driverhubber S cherne for Series Connection of,” *2001 IEEE 32nd Annu. Power Electron. Spec. Conf. (IEEE Cat. No.01CH37230)*, vol. 2, pp. 637–641, 2001.

[150] F. V. Robinson and V. Hamidi, “Series connecting devices for high-voltage power conversion,” in *Proceedings of the Universities Power Engineering Conference*, 2007, pp. 1134–1139.

[151] T. C. Lim, B. W. Williams, and S. J. Finney, “Active snubber energy recovery circuit for series-connected IGBTs,” *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1879–1889, 2011.

[152] Beom-Seok Seo, Taeck-Kie Lee, and Dong-seok Hyun, “Synchronization on the points of turn-off time of series-connected power semiconductor devices using Miller effect,” in *Proceedings of the 1992 International Conference on Industrial Electronics, Control, Instrumentation, and Automation*, 1992, pp. 325–329.

[153] A. Consoli, S. Musumeci, G. Oriti, and A. Testa, “Active voltage balancement of series connected IGBTs,” in *IAS ’95. Conference Record of the 1995 IEEE Industry Applications Conference Thirtieth IAS Annual Meeting*, 1995, vol. 3, pp. 2752–2758.

[154] C. Gerster, P. Hofer, and N. Karrer, “Gate-control strategies for snubberless operation of series connected IGBTs,” in *PESC Record. 27th Annual IEEE Power Electronics Specialists Conference*, 1996, vol. 2, pp. 1739–1742.

[155] M. Bruckmann, R. Sommer, M. Fasching, and J. Sigg, “Series connection of high voltage IGBT modules,” *Conf. Rec. 1998 IEEE Ind. Appl. Conf. Thirty-Third IAS Annu. Meet. (Cat. No.98CH36242)*, vol. 2, pp. 1067–1072, 1998.

[156] S. Hong, V. Chitta, and D. A. Torrey, “Series connection of IGBT’s with active voltage balancing,” *IEEE Trans. Ind. Appl.*, vol. 35, no. 4, pp. 917–923, 1999.

[157] J. W. Baek, D. W. Yoo, and H. G. Kim, “High-voltage switch using series-connected IGBTs with simple auxiliary circuit,” *IEEE Trans. Ind. Appl.*, vol. 37, no. 6, pp. 1832–

1839, Nov. 2001.

[158] J. Saiz, M. Mermet, D. Frey, P. O. Jeannin, J. L. Schanen, and P. Muszicki, “Optimisation and integration of an active clamping circuit for IGBT series association,” *Conf. Rec. - IAS Annu. Meet. (IEEE Ind. Appl. Soc.*, vol. 2, pp. 1046–1051, 2001.

[159] D. Zhou and D. H. Braun, “A practical series connection technique for multiple IGBT devices,” in *PESC Record - IEEE Annual Power Electronics Specialists Conference*, 2001, vol. 4, pp. 2151–2155.

[160] A. Raciti, G. Belverde, A. Galluzzo, G. Greco, M. Melito, and S. Musumeci, “Control of the switching transients of IGBT series strings by high-performance drive units,” *IEEE Trans. Ind. Electron.*, vol. 48, no. 3, pp. 482–490, Jun. 2001.

[161] K. Sasagawa, Y. Abe, and K. Matsuse, “Voltage balancing method for IGBTs connected in series,” in *Conference Record of the 2002 IEEE Industry Applications Conference. 37th IAS Annual Meeting (Cat. No.02CH37344)*, 2002, vol. 4, pp. 2597–2602.

[162] S. Katoh, S. Ueda, H. Sakai, T. Ishida, and Y. Eguchi, “Active-gate-control for snubberless IGBTs connected in series,” in *2002 IEEE 33rd Annual IEEE Power Electronics Specialists Conference. Proceedings (Cat. No.02CH37289)*, 2002, vol. 2, pp. 609–613.

[163] H. Nakatake and A. Iwata, “Series connection of IGBTs used multilevel clamp circuit and turn off timing adjustment circuit,” in *Power Electronics Specialist Conference, 2003. PESC ’03. 2003 IEEE 34th Annual*, 2003, vol. 4, pp. 1910–1915 vol.4.

[164] A. Piazzesi and L. Meysenc, “Series connection of 3 . 3kV IGBTs with active voltage balancing,” *Electronics*, pp. 893–898, 2004.

[165] D. V. M. M. Krishna and V. Agarwal, “Active Gate Control of Series Connected IGBTs Using Positive Current Feedback Technique,” *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 52, no. 5, pp. 261–265, May 2005.

[166] C. Zhang, Y. Wei, Q. Jiang, and L. Tong, “Dynamic voltage balancing of series connected IGBTs using slope regulating and voltage clamping,” in *2010 IEEE Energy Conversion Congress and Exposition, ECCE 2010 - Proceedings*, 2010, pp. 4336–4340.

[167] S. Ji, T. Lu, Z. Zhao, H. Yu, and L. Yuan, “Series-Connected HV-IGBTs Using Active Voltage Balancing Control With Status Feedback Circuit,” *IEEE Transactions on Power Electronics*, vol. 30, no. 8. pp. 4165–4174, 2015.

[168] S. Ji, F. Wang, L. Tolbert, T. Lu, Z. Zhao, and H. Yu, “Active voltage balancing control for multi HV-IGBTs in series connection,” in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–6.

[169] P. R. Palmer and A. N. Githiari, “The series connection of IGBTs with optimised voltage sharing in the switching transient,” in *Proceedings of PESC ’95 - Power Electronics Specialist Conference*, 1995, vol. 1, pp. 44–49.

[170] P. R. Palmer, “A comparison of IGBT technologies for use in the series connection,” *6th Int. Conf. Power Electron. Var. Speed Drives*, vol. 1996, no. 429, pp. 236–241, 1996.

[171] P. R. Palmer and A. N. Githiari, “The series connection of IGBT’s with active voltage sharing,” *IEEE Trans. Power Electron.*, vol. 12, no. 4, pp. 637–644, Jul. 1997.

[172] A. N. Githiari and P. R. Palmer, “Analysis of IGBT modules connected in series,” *IEE Proc. Circuits, Devices Syst.*, vol. 145, no. 5, pp. 354–359, 1998.

[173] P. R. Palmer and M. S. Abu Khaizaran, “The series connection of IGBTs in a current source inverter,” *PESC Rec. - IEEE Annu. Power Electron. Spec. Conf.*, vol. 1, pp. 170–

175, 2001.

[174] Y. Wang, M. S. Abu Khaizaran, and P. R. Palmer, “Controlled switching of high voltage IGBTs in series,” in *Electron Devices and Solid-State Circuits, 2003 IEEE Conference on*, 2003, pp. 297–300.

[175] P. R. Palmer, Y. Wang, M. Abu-Khaizaran, and S. Finney, “Design of the active voltage controller for series IGBTs,” in *PESC Record - IEEE Annual Power Electronics Specialists Conference*, 2004, vol. 4, pp. 3248–3254.

[176] P. R. Palmer, H. S. Rajamani, and N. Dutton, “Experimental comparison of methods of employing IGBTs connected in series,” *IEE Proc. Electr. Power Appl.*, vol. 151, no. 5, pp. 576–582, 2004.

[177] A. T. Bryant, Y. Wang, S. J. Finney, P. R. Palmer, and T. C. Lim, “Numerical Optimization of an Active Voltage Controller for Series IGBTs,” in *IEEE 36th Conference on Power Electronics Specialists, 2005.*, 2005, pp. 2060–2065.

[178] W. He, P. R. Palmer, Z. Wang, and M. Snook, “Active Voltage Control on series connection of IGBTs and diode recovery optimization,” in *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, 2010, pp. 345–350.

[179] W. He, P. Palmer, X. Zhang, M. Snook, and Z. Wang, “IGBT series connection under Active Voltage Control,” in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, 2011, pp. 1–9.

[180] P. Palmer, W. He, X. Zhang, J. Zhang, and M. Snook, “IGBT series connection under Active Voltage Control with temporary clamp,” in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, 2012, pp. 465–470.

[181] T. C. Lim, B. W. Williams, S. J. Finney, and P. R. Palmer, “Series-Connected IGBTs Using Active Voltage Control Technique,” *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 4083–4103, Aug. 2013.

[182] J. Zhang, P. Palmer, X. Zhang, and W. He, “Analysis of an effective voltage sharing method for IGBTs connected in series,” in *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*, 2014, pp. 1261–1269.

[183] X. Zhang, X. Yang, J. Zhang, W. He, and P. R. Palmer, “Turn-off voltage sharing of field stop IGBTs in series connection,” in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 1959–1966.

[184] P. R. Palmer, J. Zhang, and X. Zhang, “SiC MOSFETs connected in series with active voltage control,” in *WiPDA 2015 - 3rd IEEE Workshop on Wide Bandgap Power Devices and Applications*, 2015, pp. 60–65.

[185] X. Zhang, J. Zhang, and P. R. Palmer, “Direct voltage balancing for series connected IGBTs,” in *ECCE 2016 - IEEE Energy Conversion Congress and Exposition, Proceedings*, 2016, pp. 1–6.

[186] X. Yang, J. Zhang, W. He, Z. Long, and P. R. Palmer, “Physical Investigation into Effective Voltage Balancing by Temporary Clamp Technique for the Series Connection of IGBTs,” *IEEE Trans. Power Electron.*, pp. 1–1, 2017.

[187] D. B. M. Klaassen, J. W. Slotboom, and H. C. de Graaff, “Unified apparent bandgap narrowing in n- and p-type silicon,” *Solid State Electron.*, vol. 35, no. 2, pp. 125–129, Feb. 1992.

[188] S. ichi Takagi and A. Toriumi, “Quantitative Understanding of Inversion-Layer Capacitance in Si MOSFET’s,” *IEEE Trans. Electron Devices*, vol. 42, no. 12, pp. 2125–2130, 1995.

[189] M. H. Andrews, A. H. Marshak, and R. Shrivastava, “The effect of position-dependent dielectric constant on the electric field and charge density in a p-n junction,” *J. Appl. Phys.*, vol. 52, no. 11, pp. 6783–6787, Nov. 1981.

[190] Fuji Electric Holdings Co. Ltd., “Release of New High-Power 2-in-1 IGBT Module Series Designed for Parallel Connections | Fuji Electric Global,” 2010. [Online]. Available: https://www.fujielectric.com/company/news/2010/10122801.html.

[191] Fuji Electric Co. Ltd., “Sixth-Generation V-Series IGBT Module Application Note,” 2011.

[192] F. Udrea, G. Deboy, and T. Fujihira, “Superjunction power devices, history, development, and future prospects,” *IEEE Trans. Electron Devices*, 2017.

[193] A. P. S. Hsieh *et al.*, “Field-stop layer optimization for 1200V FS IGBT operating at 200℃,” in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, 2014, pp. 115–118.

[194] M. N. Darwish, J. L. Lentz, M. R. Pinto, P. M. Zeitzoff, T. J. Krutsick, and H. H. Vuong, “An improved electron and hole mobility model for general purpose device simulation,” *IEEE Trans. Electron Devices*, vol. 44, no. 9, pp. 1529–1538, 1997.

[195] *Atlas User’s Manual*. Silvaco, Inc., 2014.

[196] R. Häcker and A. Hangleiter, “Intrinsic upper limits of the carrier lifetime in silicon,” *J. Appl. Phys.*, vol. 75, no. 11, pp. 7570–7572, Jun. 1994.

[197] J. W. Slotboom, “The pn-product in silicon,” *Solid State Electron.*, vol. 20, no. 4, pp. 279–283, Apr. 1977.

[198] J. W. Slotboom and H. C. De Graaff, “Bandgap Narrowing in Silicon Bipolar Transistors,” *IEEE Trans. Electron Devices*, vol. 24, no. 8, pp. 1123–1125, Aug. 1977.

[199] P. Mars, “Temperature dependence of avalanche breakdown voltage in p—n junctions†,” *Int. J. Electron.*, vol. 32, no. 1, pp. 23–37, Jan. 1972.

[200] G. K. Wachutka, “Rigorous Thermodynamic Treatment of Heat Generation and Conduction in Semiconductor Device Modeling,” *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 9, no. 11, pp. 1141–1149, 1990.

[201] V. Palankovski, R. Schultheis, and S. Selberherr, “Simulation of power heterojunction bipolar transistors on gallium arsenide,” *IEEE Trans. Electron Devices*, vol. 48, no. 6, pp. 1264–1269, Jun. 2001.

[202] T. Van Nguyen, P. O. Jeannin, E. Vagnon, D. Frey, and J. C. Crebier, “Series connection of IGBTs with self-powering technique and 3-D topology,” *IEEE Trans. Ind. Appl.*, vol. 47, no. 4, pp. 1844–1852, Jul. 2011.

[203] P. R. Palmer and H. S. Rajamani, “Active voltage control of IGBTs for high power applications,” *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 894–901, 2004.

[204] Y. Wang, P. R. Palmer, A. T. Bryant, S. J. Finney, M. S. Abu-Khaizaran, and G. Li, “An Analysis of High-Power IGBT Switching Under Cascade Active Voltage Control,” *Industry Applications, IEEE Transactions on*, vol. 45, no. 2. pp. 861–870, 2009.

[205] X. Yang and P. R. Palmer, “Optimised IGBT turn-off under active voltage control in PEBB applications,” *2013 15th Eur. Conf. Power Electron. Appl. EPE 2013*, pp. 1–10, 2013.

[206] P. R. Palmer, X. Yang, X. Zhang, J. Zhang, and P. R. Palmer, “Predictive optimisation of high-power IGBT switching under Active Voltage Control,” in *Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE*, 2013, pp. 1169–1174.

[207] M. Rahimo *et al.*, “Characterization of a Silicon IGBT and Silicon Carbide MOSFET Cross-switch hybrid,” *IEEE Trans. Power Electron.*, 2015.

[208] X. Song, A. Q. Huang, M. C. Lee, and C. Peng, “High voltage Si/SiC hybrid switch: An ideal next step for SiC,” in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, 2015.

[209] Cree Inc., “C2M0080120D Datasheet Rev. C, 10-2015.” Cree Inc., pp. 1–10, 2015.