A Physics-based IGBT Model with Terminal Capacitance Correction

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Abstract

IGBT terminal capacitances play an important role in IGBT switching transients. The terminal capacitance modelling, particularly Miller capacitance modelling, is a difficult task due to their operating-point-dependent characteristics. Previously, for the planar gate IGBT, the Miller capacitance's voltage dependency is modelled by considering the depletion region growth pattern. For modern trench gate design, however, there is no similar dynamic process available. Also, its current dependency needs to be taken account of. This paper presents an improved IGBT physics-based model with proper terminal capacitance correction. By comparison of experimental and simulation results, the proposed model works brilliantly for different types of IGBTs (including the state-of-art trench-gate field-stop type) over a wide range of operating conditions.

1 Introduction

The modelling and simulation technology has become increasingly important to reduce development cycles and costs, and achieve optimal designs of power electronics systems [1]. It is more essential to the revolutionary PEBB (Power Electronic Building Block) based power electronic systems [2]. Power semiconductor device models that aim at simulating their switching transients require satisfactory performance under different operating conditions (voltages, currents, and temperatures). More importantly, it needs to achieve good accuracy of voltage and current switching waveforms in order to estimate switching losses, predict EMI [3], and optimise gate drive design [4-5]. Accordingly, physics-based models become reasonable solutions with desired accuracy, especially in the system simulation [2]. However, a trade-off has to be made between simulation speed and accuracy.

Although the most accurate simulation can be carried out effectively by using the device simulator involving finite difference analysis, obtaining IGBT designs is difficulty for power engineers, and its simulation time is substantial and its compatibility with other levels of simulation is poor. The most important part of modelling bipolar devices such as IGBT is the carrier storage phenomenon. There have been several models that applied the ambipolar diffusion equation to depict the excess carrier dynamics with different analytic solutions [6-8]. Therefore, the simulation speed is improved. But the problem remains that the

semiconductor manufacturers do not officially disclose all the detailed physics parameters of semiconductor devices and some of them are unable to measure. Thus, designers of power conversion engineering have to extract or estimate a few physical parameters of targeted power devices, and then adjust or optimise the parameters in accordance with measured waveforms.

However, the number of IGBT physical parameters is much larger than that of a power diode model. This complicates the parameter extraction and optimisation of an IGBT model. Previously, with switching loss errors between simulation and experimental results set as cost function, the Hooke and Jeeves search method is applied on five main IGBT physical parameters and two external circuit parameters to get an optimum set of their values [9]. The search time is annoyingly substantial. Also, the previous IGBT model takes account of the varying Miller capacitances C_{GC} with respect to the growth of depletion layer in the planar gate structure [6, 9]. However, C_{GC} has also been found to be current-dependent [1, 6] and IGBT physical parameters to calculate C_{GC} like the distance between adjacent p-wells l_M and the radius of the cell R (Figure 3) are seldom revealed. Furthermore, for trench gate, there is so far no proper similar physical modelling to calculate C_{GC}. It should be noted that the switching transient is considerably affected by IGBT terminal capacitances. Therefore, the terminal capacitances in the previous model are still deviated. Based on those inaccurate terminal capacitances, the search algorithm for optimal IGBT physical parameters is unable to provide accurate results. As a consequence, the inaccurate physical parameters extracted will generate inaccurate terminal capacitances in the simulation, which cause worse deviations to the physical parameters during parameter optimisation. This vicious circle would prevent any advanced algorithm from searching the optimal set of parameters. Therefore, in previous papers to achieve matching of simulation and experimental waveforms, efforts have to be made to implement the parameter optimisation at each operating condition [9].

This paper applied the IGBT model developed by Palmer and Bryant [6, 9, 10] with further terminal capacitance correction. The initial parameter estimation is improved based on the manufacturer data. Furthermore, an improved IGBT parameter optimisation process is proposed. Therefore, accurate physical parameters can be extracted and the simulation model can work at different operating conditions without the need for algorithm-based parameter optimisation techniques. Furthermore, the simulation speed is greatly increased.

2 IGBT Physical Model

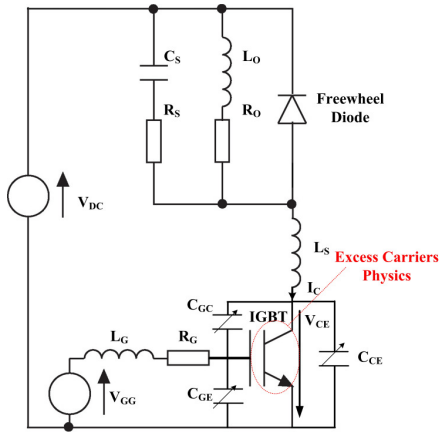


Figure 1: IGBT model configuration and test circuit with inductive load (R_0, L_0: load; R_S , C_S : snubber; L_S : stray inductance; L_G : gate inductance; and R_G : gate resistance).

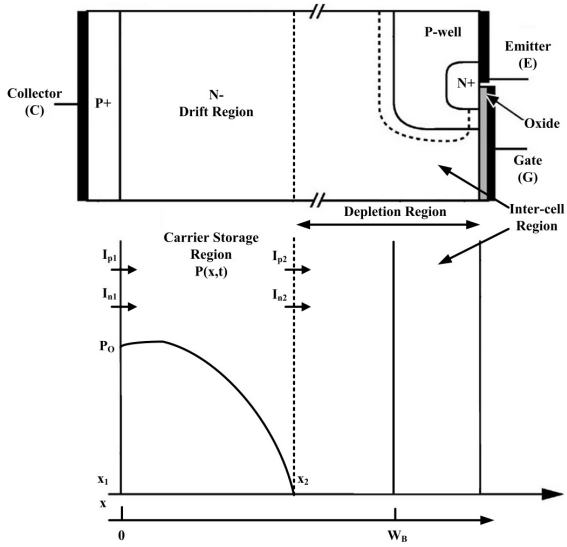


Figure 2: Structure of a planar NPT IGBT and undeleted drift-region carrier profile showing boundary currents.

Most power electronic circuits can be reduced to a standard chopper cell for device simulation purposes. So the chopper cell is selected as the simulation circuit as shown in Figure 1 with a diode snubber (small R_S and C_S) to improve simulation convergence [9]. The model in this paper is mainly consisted of a physics-based model involving C_{GC} correction while variation in C_{CE} is assumed to be sufficiently accurately modelled by excess carrier physical modelling. Correction for C_{GC} is necessary due to their influence on the gate circuit [1].

2.1 Fourier-based-solution IGBT model

The behaviour of conductivity modulated devices heavily depends on the excess carrier distribution in the wide lightly doped drift region. In most power devices, the charge profile has a 1-D form over most of its volume [8]. Thus, a 1-D solution is adequate for the device bulk. The structure of a planar NPT IGBT and its simplified carrier profile are shown in Figure 2. Regardless of the detailed structure of a particular IGBT (NPT/NP/FS or Trench/Planar), under high-level injection conditions, the carrier's dynamics in the base is governed by the ambipolar diffusion equation (ADE):

$$D\frac{\partial^2 P(x,t)}{\partial^2 x}=\frac{P(x,t)}{\tau_{HL}}+\frac{\partial P(x,t)}{\partial t} \qquad (1)$$

where D is the ambipolar diffusivity, $P(x,t)$ is the concentration of excess carrier and τ_{HL} is the ambipolar carrier lifetime.

The Fourier-series approach developed in [6-7], [9], and [10] can be implemented in the circuit simulator like Ltspice, Pspice and Matlab. It is now briefly described. The second-order partial differential equation (1) is converted into a set of ordinary differential equations. The Fourier-series solution for the carrier distribution is

$$P(x,t)=P_0(x,t)+\sum_{k=1}^{\infty}P_k(t)\cos[\frac{k\pi(x-x_1)}{(x-x_2)}] \qquad (2).$$

The boundary conditions are given by the gradients of the carrier distribution, f(t) and g(t), at the boundaries of the N- drift region (x_1 and x_2) as shown in Figure 2, which can be expressed as a function of the hole and electron currents at x_1 and x_2

$$f(x) = [\frac{\partial P(x,t)}{\partial t}]_{x_1} = \frac{1}{2qA}[\frac{I_{n1}}{D_n} - \frac{I_{p1}}{D_p}]$$
$$g(x) = [\frac{\partial P(x,t)}{\partial t}]_{x_2} = \frac{1}{2qA}[\frac{I_{n2}}{D_n} - \frac{I_{p2}}{D_p}] \qquad (3)$$

where A is the active cross sectional area of the device, D_n and D_p, the electron and hole diffusion coefficients, I_{n1} and I_{p1}, the electron and hole currents at $x=x_1$, and I_{n2} and I_{p2}, the electron and hole currents $x=x_2$. Clearly, the solution's accuracy now depends solely upon developing appropriate boundary conditions. Therefore, in order to establish boundary conditions, hole and electron currents at the edges of the drift region are needed. Figure 2 defines some of the relevant variables used in the analysis for NPT IGBT. Since by current continuity

$$I_C = I_{n1} + I_{p1} = I_{n2} + I_{p2} \qquad (4),$$

where the switching current I_C is known, it is sufficient to find each current component at the boundaries. At the right side of the n- drift region, W_B, the electron current I_{n2} is the MOS channel current. So the hole current can be obtained by equation (4). At the left side of the N- drift region, different equations are used for the NPT and FS/PT according to their structures. For the FS/PT, I_{p1} can be written as

$$I_{p1} = \frac{qAD_{PH}}{L_{PH}\sinh(\frac{W_H}{L_{PH}})}[P_{H0} - P_{PH}\cosh(\frac{W_H}{L_{PH}})] + I_{QH} \qquad (5)$$

where L_{PH} and D_{PH} are the diffusion length and mobility of the hole carrier in the FS/PT buffer layer. W_H is the layer length. P_{PH} and P_{H0} are the hole densities at the P+ side and N- side of the FS buffer. I_{QH} is the charge control current. For NPT (no FS Buffer),

$$I_{P1} = qAh_pP^2{}_0 \qquad (6)$$

where h_p is the hole recombination rate and P_0 is the excess carrier density at the collector side.

2.2 Terminal Capacitance Modelling

The three IGBT terminal capacitances are all voltage-dependent and change with the depletion region width [12]. C_{CE}, C_{GC} and C_{GE} vary with V_{CE}, V_{GC} and V_{GE} respectively. The displacement currents flow through the terminal capacitances of C_{CE} and C_{GC}. At the right side of the N- drift region, Figure 2, $x=x_2$, these two current components comprise of the hole boundary current that affect the carrier storage in the N- drift region. Normally, manufacturers will provide the terminal capacitances information in the datasheet in terms of input capacitance $C_{iss}=C_{GC}+C_{GE}$, output capacitance $C_{oss}=C_{GC}+C_{CE}$, reverse transfer

capacitance C_{rss}=C_{GC}. But they are measured under the condition that V_{GE}=0 and lower V_{CE} values, so these values cannot represent the actual capacitances appearing during IGBT switching. Although improved measurements can be done by LCR meter via some well-designed methods, but the work is intensive and its range is limited to only tens of voltages while the operating voltage of an IGBT can vary from tens to thousands [12]. In a normal PWM converter, a large range of operating currents will also make the measurement approach unattractive.

In the previously published IGBT model [9], the gate capacitance C_{GE} is assumed to be constant. As C_{GE} variation's sensitivity to voltage is very low, this assumption is able to provide very accurate results [1,10-12]. The charge extraction capacitance C_O represented by modelling the dynamic excess carrier physics. For the calculation of C_{GC} during switching in the previous model, mainly the voltage dependency is considered. In [1], it points out that C_{GC} has the characteristics of current dependency as well as voltage dependency. Therefore, under some conditions, there could be significant deviations in the modelling of C_{GC}. Therefore, previously to achieve satisfactory simulation results, we have to optimise the doping coefficient N_B, along with other related physical parameters, at each voltage/current eventually finding a best fit. Using the switching loss errors between simulated and experimental results as cost function, the time-consuming parameter optimisation might offer acceptable simulated switching losses. But from [9], the agreement between simulated voltage/current waveforms and the experimental waveforms is still limited under some conditions. The parameters, such as N- region doping N_B and geometry should be constant, but the parameter extraction sometimes makes them change between different operating conditions.

The phenomenon of C_{GC} varying with current is reported to relate with the effective doping concentration N_{eff} in the depletion layer [1]

$$N_{eff} = N_B + \frac{I_{p2}}{qv_{\partial sat}A} - \frac{I_{n2}}{qv_{\partial sat}A} \qquad (7)$$

where v_{sat} is the saturated drift velocity. It can be seen that N_{eff} is closely dependent on the hole and electron component currents at the MOS end. In the previous model, N_{eff} cannot be modified by the hole and electron currents to avoid extra loops in the model creating a convergence issue [9]. The width of the depletion region, W_d, can be described by with the voltage applied to the depletion region V_d

$$W_d = \sqrt{\frac{2\varepsilon_{si}V_d}{qN_{eff}}} \qquad (8).$$

Thud, the depletion region C_{dep} under the gate is represented by

$$C_{dep} = \frac{\varepsilon_{si}a_iA}{W_d} \qquad (9).$$

C_{GC} is comprised of the gate oxide capacitance C_{OX} in series with the depletion capacitance C_{dep}. Thus,

$$C_{GC} = \frac{C_{OX} A a_i C_{dep}}{C_{OX} A a_i + C_{dep}} \qquad (10).$$

Previously in [7, 17], C_{dep} has been modelling in the planar gate structure as shown in Figure 3 by analysing its simulation results from Silvaco ATLAS. For trench gate IGBTs, the growth of the depletion region will follow a similar pattern, for both devices, as soon as the collector voltage has risen above a few tens of voltages [16]. However, the effect on the capacitances will be quite different early in the switching process, due to the different orientation of the MOS channel and the behaviour of the stored charge under the gate. Therefore, we concluded that the important Miller capacitance C_{GC} is difficult to model properly and a correction method is needed in order to obtain accurate capacitance values.

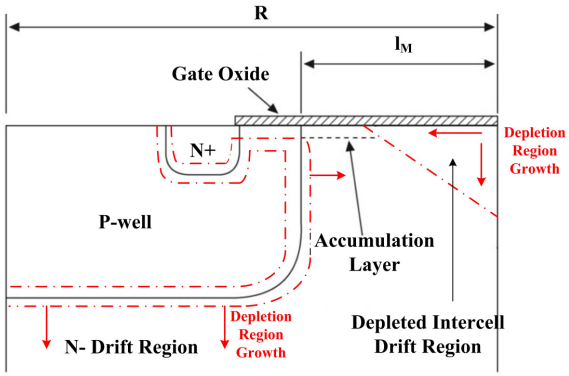


Figure 3: 2-D Arrangement of the gate accumulation and depletion layers during planar gate IGBT turn-off.

3 Parameter Extraction and Validation of the IGBT Model

In order to validate the proposed approach, the experimental switching behaviours of different IGBT structures listed in Table I are compared by simulation results. The experiment measurements of voltage and current waveforms are measured by a high-voltage probe, PMK PHV 641-L, and Pearson current monitor (Model 110). The waveforms are captured using a digital oscilloscope (working at 500 MHz) and transferred to the host computer.

3.1 Parameter Extraction

The initial IGBT parameters estimation is based on the method proposed in [9-10]. In the case of parameterization, the initial parameter set is crucial. With a good initial estimate, a simple direct search, without additional heuristics, might be enough to obtain an optimal set of parameter values. In addition, the search time can be kept low. It has been shown that the initial estimation method can provide reasonable MOS Gate and Geometry parameters (Group 1 in Table II) for a variety of IGBTs with different structures made by different manufactures. Most parameters of Group 1 can be derived from the datasheet provided by the manufacturers. For other parameters, their initial estimation can be further improved. The N- doping N_B and

region width W_B, Group 2, can be estimated by the empirical equations from [9, 10]. As W_B sometimes might be revealed in the manufacturer manuals or magazines [14], the parameter for optimisation is the doping coefficient N_B. Also, N_B has a reasonably limited range, normally $6\times10^{13}-2\times10^{14}cm^{-3}$. The further optimisation is made by comparing the simulated dV_{CE}/dt with the experimental one. According to paper [11], the full expression of dV_{CE}/dt can be written as

$$\frac{dV_{CE}}{dt}=\frac{V_{GE(ON)}-V_{GG(OFF)}}{R_G C_{gc}+\frac{C_o}{g_m}} \qquad (11)$$

$V_{GE(ON)}$,the constant plateau voltage in the voltage rise dependent on the current; $V_{GG(OFF)}$ is the off-state gate voltage; R_G is the gate resistor; g_m is the transconductance of MOS channel. The accuracy of the initial estimated for N_B can be checked by the simulated dV_{CE}/dt at turn-off. As C_{GC} collapses when entering the fast rise of V_{CE}, the C_{GC} time constant in Equation (11) is of a similar magnitude to the C_O/g_m time constant. Therefore, N_B will have an impact on dV_{CE}/dt at this point. Clearly reasonable value of N_B will lead to a better simulated dV_{CE}/dt and then, the group 3 parameters can be optimised by referring to the tail current as the decay rate of current is set by the lifetime. Empirical values of lifetime from different structures (FS/NPT) help the parameter optimisation as well. It is of great interest to point out that modern FS IGBT has increased the bulk resistivity so the FS-buffer reaching through voltage would be normally higher than the safe operating voltage [13]. As a result, a small tail current can still be observed. So the N- drift region lifetime in FS IGBT might be estimated by the similar method of NPT IGBT. The extracted parameters are given in Table II. For IGBT C and D, similar parameters can be obtained.

Table I: Experimental IGBT Device list

IGBT	Structure	Rating	Model	Manufacturer
A	Planar NPT	1700V/400A	SKM400GA173D	SEMIKRON
B	Trench FS	1700V/400A	2MBI400U4H-170	Fuji
C	Trench FS	1700V/650A	2MBI650VXA-170E-50	Fuji
D	Trench FS	1200V/900A	2MBI900VXA-120P-50	Fuji

Table II: IGBT Model Parameter list

Part	Symbol	Description	IGBT A	IGBT B	Group
MOS Gate	$V_{th}(V)$	MOS threshold voltage	5.5	6.5	1
	$K_{pl}(A/V^2)$	MOS transconductance coefficient	35	15	
	λ	Short-channel parameter	0.08	0.05	
	$C_{GE}(nF)$	Gate-emitter capacitance	50	40	
	$C_{OX}(nF)$	Oxide capacitance	16	12	

Geometry	$A(cm^2)$	Effective die area	6	4	
	a_i	Ratio of inter-cell to total die area	0.45	0.667	
Collector Side	$W_B(cm)$	N drift region width	270e-3	170e-3	2
	$N_B(cm^{-3})$	Doping concentration of N drift region	6e13	8e13	
	$\tau_{HL}(\mu s)$	Carrier high-level lifetime in N drift region	15	0.9	3
	$h_p(cm^4 s^{-1})$	Hole recombination coefficient in emitter (NPT)	80e-13	100e-13	
	$N_H(cm^{-3})$	Doping concentration of N buffer layer (FS)		1e16	
	$W_H(cm)$	Width of N+ buffer layer (FS)		4e-4	
	$\tau_{BF}(\mu s)$	Carrier lifetime in N buffer layer (FS)		0.2	

3.2 Proposed Terminal Capacitance Correction

In this paper, C_{GC} is corrected by considering the effective doping N_{eff}. From Equation (8)-(10), the original values, C_{GCO}, are multiplied by the correction coefficients K_{CGC} and the square root of load current I_L

$$C_{GC} = K_{CGC}\sqrt{I_L}C_{GCO} \qquad (12).$$

With a set of reasonable physical parameters, as chosen above, the further parameter optimisation at different operating conditions can concentrate on K_{CGC}. Due to the very limited variation range of C_{GE} [1,10], changing C_{GE} has very limited effects on the voltage/current waveforms. K_{CGC} is mainly used to correct the simulated turn-off delay while C_{GE} can be slightly corrected for gate waveform correction. The further optimisation of K_{CGC} can be made by two different ways. One is "by eye"; that is, adjust the two parameters according to a salient point, like IGBT turn-off delay time or V_{CE} peak time. Another is to search the two values by an advanced search algorithm to find the minimum value of cost function mentioned in [9]. As the total number of variables is only two in this case, the simulation/optimisation time is greatly shortened. In this paper, the first method is used to show that the proposed model is very easy to set up and can achieve high accuracy.

3.3 Temperature Dependent Parameters

The extracted parameters in Table II are for normal room temperature 27°C (300 K). Textbook equations can be used to depict the variation of the temperature-dependent parameter as following:

$$\tau_{HL} = 5\times10^{-7}(\frac{T+273}{300})^{1.5},$$
$$\mu_n = 1400(\frac{T+273}{300})^{2.5},$$
$$\mu_p = 450(\frac{T+273}{300})^{2.5}, \quad (13).$$
$$n_i = 3.88\times10^{16}(T+273)^{1.5} \Big/ \exp(\frac{7000}{T+273})$$

There are two other IGBT parameters also affected by the temperatures. They are the MOS gate threshold voltage and MOS channel transconductance. They can be approximated by

$$V_{th} = V_{th0} - 9\times10^{-3}(T - T_a) \quad (14),$$

where V_{tho} is the device threshold voltage at T_a= 27°C.

$$K_p = K_{p0}(\frac{T_a+273}{T+273})^{0.8} \quad (15)$$

where K_{p0} is the transconductance at 27°C [6].

3.3 Results

In order to avoid the effects brought by the external circuit, the validation experiments are performed under a simple hard switching environment of a clamped inductive load test. The original model was validated under resistive load tests in [1, 10] with a high degree of accuracy. The comparisons between the experimental and simulated results for various IGBTs at turn-off are shown in Figure 4. For IGBT A, the proposed model accurately simulates voltage and current waveforms so that the simulated switching losses are almost identical to that of experimental measurements (Figure 4(a)). For IGBT B, the simulated results are promising, Figure 4(b). The proposed model simulates nicely the delay of V_{CE} and the tail current but there is a slight error in the overshoot of V_{CE} waveform, which leads to the early drop of I_C. However, the switching losses are still simulated well. For the latest IGBT C, it was tested at 800V/100A (Figure 4(d)) and 900/50 A (Figure 4(c)) respectively. The results are also quite satisfactory in the switching losses profile but there are still some slight deviations in the V_{CE} overshoots and the tail currents. For the IGBT D, similar results are observed in Figure 4 (e) and (f) when compared with Figure 4 (c) and (d). From Figures 5 to 6, it can be seen that at different currents, the simulation results are still very close to the experiments'. For IGBT A, the differences between the simulation and experiment results are tiny while the errors become slightly increased for IGBT B. In Figure 7, C_{GC} values corrections are shown for IGBT A turn-off at 800V/100A. In the previous model, C_{GC} almost stay constant without dependency on the current if not adjusting related physical parameters. The C_{GC} values from datasheet are very small compared with the simulated results.

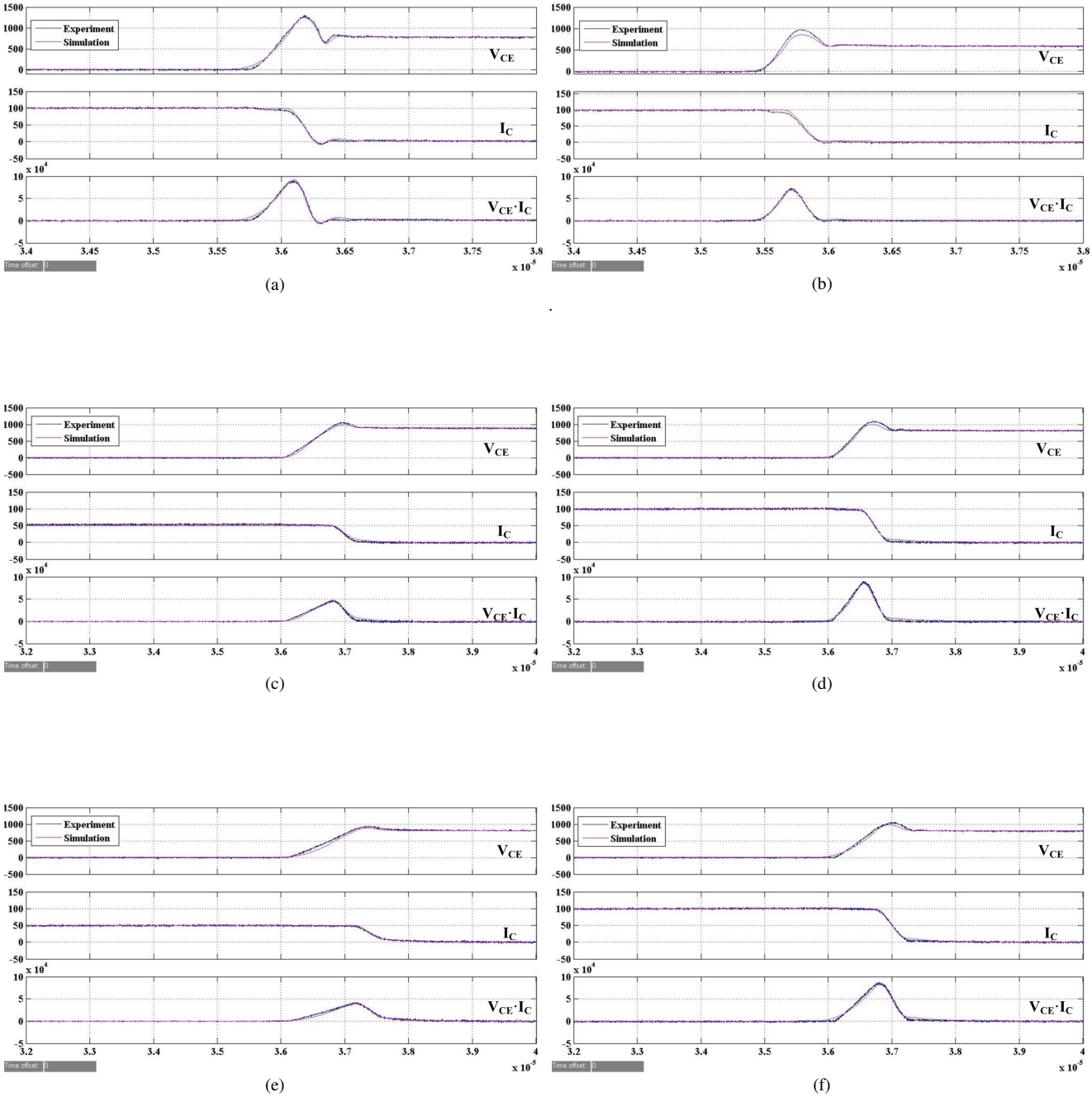


Figure 4: Turn-off Comparisons between the experimental data and simulation results: (a) IGBT **A** at 800V/100A; (b) IGBT **B** at 600V/100A; (c) IGBT **C** at 900V/50A; (d) IGBT **C** at 800V/100A; (e) IGBT **D** at 800V/50A; (f) IGBT **D** at 800V/100A.

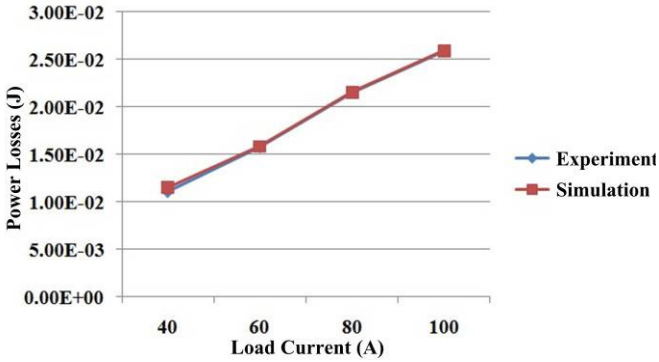


Figure 5: IGBT A comparison between the experimental switching losses and simulation.

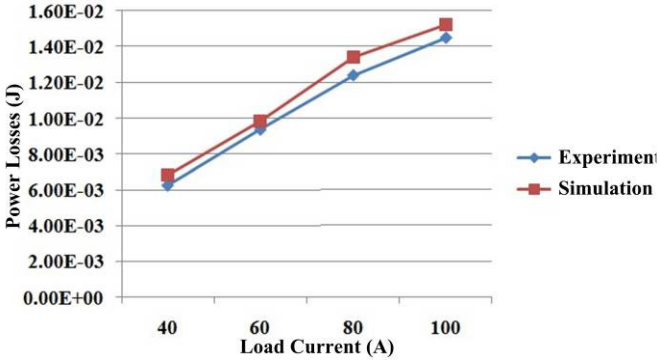


Figure 6: IGBT B comparison between the experimental switching losses and simulation.

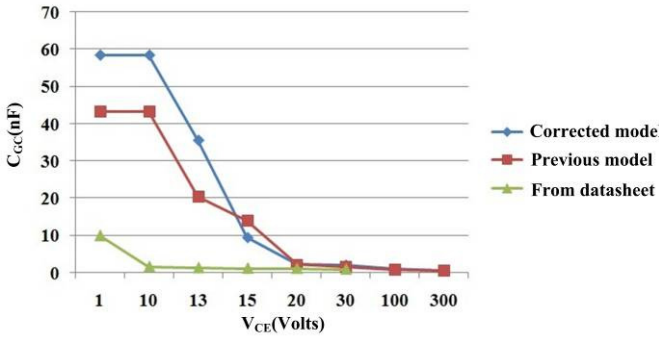
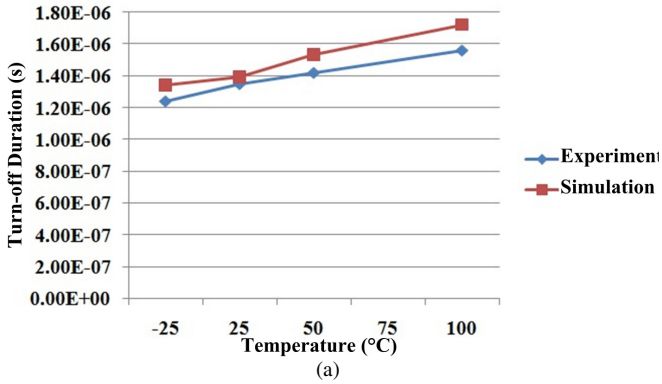
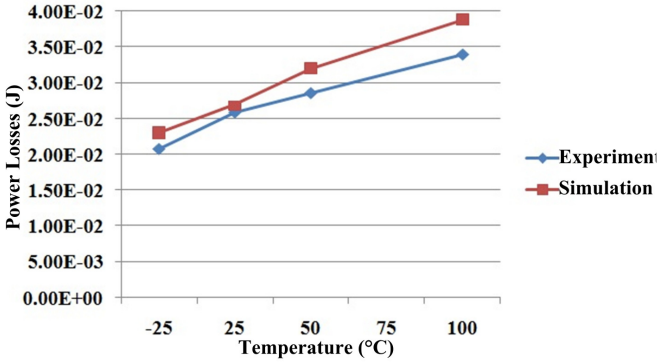


Figure 7: IGBT A C_{GC} vs. V_{CE} under a load current of 100A.

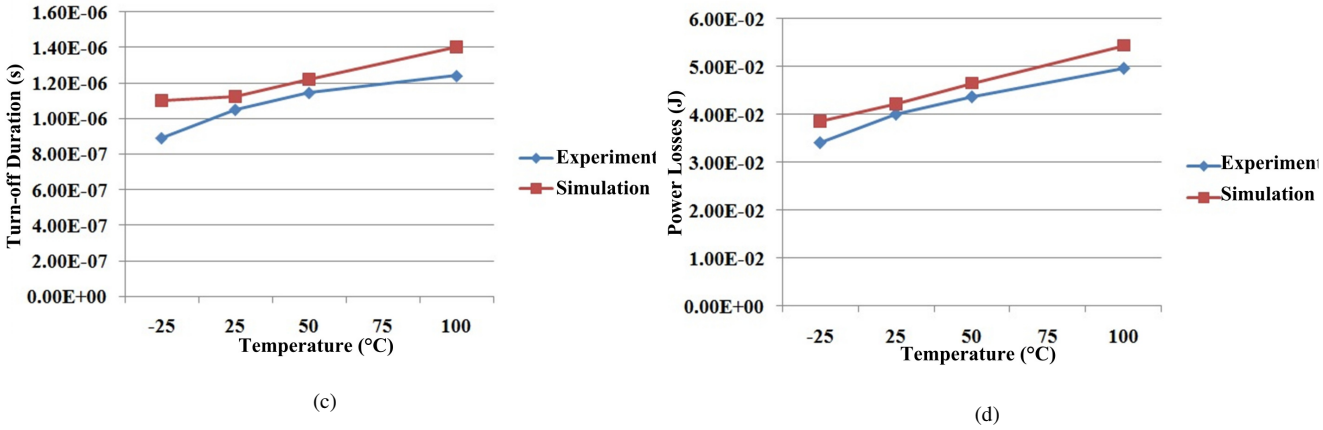
The variations with temperature of IGBT characteristics as obtained in the experiment and simulated Matlab are presented in the following graph, Figure 8. Two operating conditions are selected for IGBT C: one is at 900V/50A and another 800V/100A. There is no algorithm-base parameter optimisation process involved. The physical temperature-sensitive parameters are all calculated by Equations (13)-(15) above. The proposed approach as it shows produced a useful set of results.



(a)



(b)



(c) (d)

Figure 8: IGBT C comparison between the experimental and simulation results at different temperatures: (a) turn-off time at 900V/50A; (b) turn-off losses at 900V/50A; (c) turn-off time at 800V/100A; (d) turn-off losses at 800V/100A.

4 Discussion

In previous research [9-10], the IGBT main physical parameters are optimised over a range of operating conditions in order to produce a set of parameters which provide accurate simulation results. In the absence of details from manufacturers, this process can be time-consuming. The optimisation techniques rely on finding the minimum of the cost function. However, it has been found that multiple combinations of the physical parameters that can produce minimum switching loss errors between simulation and experiment, and can even provide voltage and current waveforms that are close to the experimental waveforms. This reduces confidence in the set of parameters produces. The stochastic searches such as simulated annealing and genetic algorithms are believed to find the global minimum more effectively by introducing random parameter variation [9]. However, with a large number of parameters that need to be optimised at the same time, the optimisation process is still slow and the resulting parameters may still be unlike those of actual geometry. The terminal capacitances, particularly Miller capacitance have a significant effect on the switching performance. Addressing the issue of the capacitances by adding 2D modelling features and current dependencies into N_{eff} creates simulation issues as mentioned above and the need for yet more parameters known only to the manufacturer. However, addressing the main issue with a correction factor gives the parameterisation process another degree of freedom, with just one parameter, but allows the process to then obtain good results with a single convincing set of parameters. Clearly knowledge of the device structure, particularly for trench gate devices, could be attractive to those wishing to perform simulation, but the effect of small changes is quite dramatic [17] and should be considered as a part of the design that remains confidential. The terminal capacitances found in Silvaco ATLAS [6] and measurements [11] that they are varying in more involved manner even than that given by the more than simply with the depletion layer width.

However, some physical parameters are not actually treated as secrets and are in fact publicised. For example, the width of 1200V 5th and 6th FS IGBT N- drift region is provided in [14]. Therefore, based on these known parameters, a whole set of reasonable parameters can be obtained. And here, the parameter optimisation at different operating conditions is mainly transferred to the optimal values of correction factors, mainly K_{CGC}. Therefore, the optimisation process is much simplified and more importantly, the search process for the optimal IGBT physical parameter can be more accurate and reasonable. The charge behaviour in the bulk of the device is shown in Figure 9. The model indirectly develops the charge capacitance C_O using the carrier physics to control the sweeping out of the stored charge. The inferred values of C_O/g_m are dynamically changing. However, it is clear that the effect of C_{GC} is diminished when the voltage starts to rise rapidly, as the dV_{CE}/dt is held back by the C_O/g_m term, Equation 11. Thus, the proposed model for C_{GC} does not adversely influence the charge profiles during the fast rise in voltage. The observed ripple in the charge, Figure 9, at around 36 μs is an artefact due to the truncation of the Fourier series solution at order eight. The total quantity of charge under the curve in the N- drift region is unaffected and therefore, the terminal voltage/current waveforms are unaffected [6].

The proposed model has been proven to be effective under different currents, voltages and temperatures. Capacitance corrections could be made for different temperatures (K_{CGC} slightly lower at lower temperatures, slightly high at high temperatures.). However, it was found that this was not necessary, noting that the effect of the correction is early in the formation of the depletion region. With the advance of power device techniques, the IGBT has been pushed to work at around 175 °C [15]. Such a temperature range in Silicon for an IGBT requires the use of a detailed physics-based model to take account of a large range of working conditions. The proposed improved model can produce nice simulation results with promising accuracy while the parameter optimisation has been much simplified.

Given the good results above, it has to be admitted that with the advance of IGBT design [13], 3-D IGBT design should be considered as shown in Figure 10. The improved IGBT structure from Fuji greatly improved the voltage drop and IGBT switching behaviour [14]. The proposed 1-D model will simulate the 3-D IGBT design with some deviations. The 3-D wide distribution of electrons leads to the improved excess carrier profile. There is a high charge concentration on the trench gate side and an accumulation layer of electrons under the gate, Figure 10. Therefore, the Miller capacitance becomes larger than those in previous generations of IGBTs, which can be seen from the V-series IGBT datasheet. Therefore, an improved solution is possibly to take into account the 2-D dimensional effects, following the work in [16]. Adding the C_{GC} correction factor as above will assist in capturing the behaviour without resort to further complexity, again avoiding use of the manufacturer's geometric design.

Finally, for the IGBT turn-on, the result is shown in Figure 11. The difficulty in modelling IGBT turn-on is compounded by the need to model the freewheel diode, and improving the turn-on process involves diode parameter optimisation. However,

the current in the IGBT increases rapidly while the diode is on, and the value of C_{GC} develops appropriately. Figure 11 shows that the proposed approach still gives a high degree of confidence in the result even without optimising the diode parameters. A further correction may be developed for turn on [1].

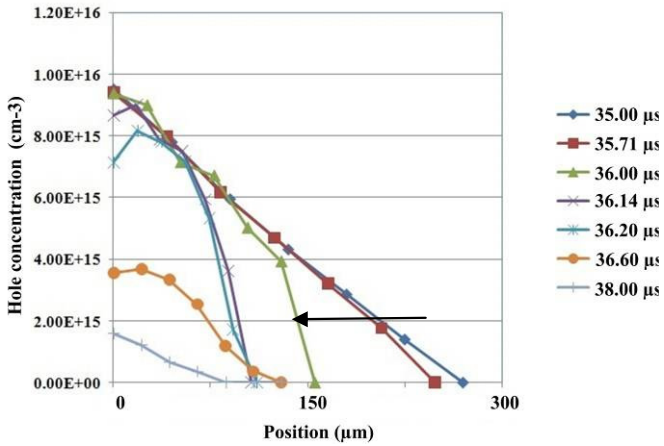


Figure 9: IGBT A Charge profiles during turn-off.

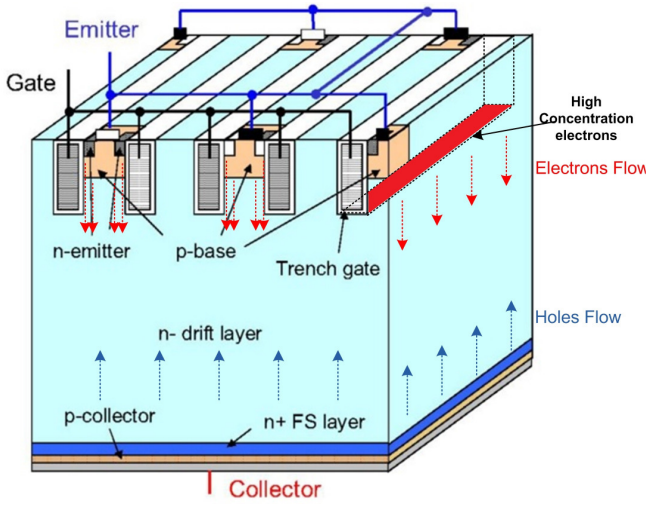


Figure 10: 3D excess carriers flow inside the latest 1200V Fuji IGBT model.

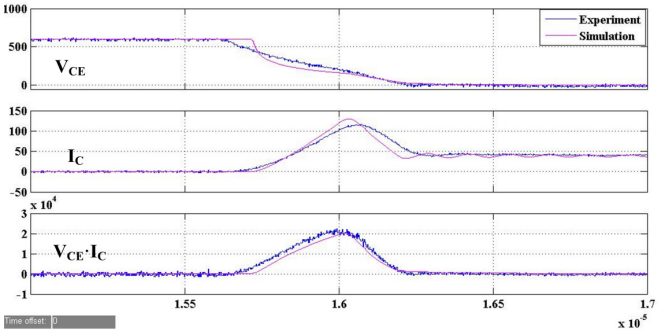


Figure 11: IGBT B Comparison between the experimental data and simulation during turn-on at 600V/40A.

5 Conclusion

This paper presented an improved IGBT physical model with terminal capacitance correction. The proposed model avoided the requirement of IGBT geometrical information on modelling the Miller capacitance. In the proposed model, the terminal capacitances C_{GC}' current-dependency is taken into account. The correction on C_{GC} is made mainly based on the load currents. It has been shown that for different types of IGBTs, the simulated waveforms are in excellent agreement with the experimentally measured over a wide operating range. With such an improved physical model, a reasonable IGBT physical

parameter can be obtained without the need of a time-consuming parameter optimisation process. The optimisation does mainly concentrate on the correction of terminal capacitances; therefore, the process can be very fast and effective.

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