Novel Digital Radio over Fibre for 4G-LTE

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***Abstract*— Digital radio over fibre (RoF) technology has been suggested as a promising solution to replace conventional analogue RoF technology for multi-service in-building wireless coverage. However in conventional digital RoF, digitisation leads to high data rates which in turn results in high capital expenditure (CAPEX) and operational expenditure (OPEX). This paper investigates a novel methodology to transmit efficiently a digitised radio service over an optical link to provide wireless coverage. We demonstrate a digital processing technique that is able to compress the digitised 20MHz bandwidth Long Term Evolution (LTE) data stream to a much lower level than in a conventional link without impairing its radio performance.**

Keywords*— *Radio over Fibre (RoF), Digitisation, Data Rate, Data Compression, Digital Signal Processing, Long Term Evolution (LTE), In-building Wireless, Distributed Antenna System (DAS), Error Value Magnitude (EVM), Dynamic Range

I. INTRODUCTION

Radio over fibre (RoF) technology has long been suggested as a promising solution to meet the increasing demand for larger transmission bandwidth, multi-service capability and cost-effectiveness of wireless access networks. A traditional analogue RoF system shown on *Fig. 1 (a)* is able to carry multiple bands of wireless services over a single-fibre link in a service agnostic manner **[1]** and is typically used in buildings [**2**]. This type of system directly transmits RF signals over optical fibre without demodulation. Therefore, it simplifies the system architecture for antenna remoting applications where large-area coverage is required.

However, the RF performance of such an analogue RoF system is highly dependent on the transmission distance and linearity of the analogue optical link whereas a digital RoF approach shown on *Fig 1 (b)* is able to achieve a fixed RF performance until error-free transmission is no longer possible **[3]**. Furthermore, analogue RoF requires a dedicated infrastructure to be built because, unlike widely-adopted and standardised digital communication components, the optoelectronic modules required in a RoF system have to be specifically designed to support wideband analogue signal and optimised for high carrier frequencies. There is also a trend of converging all communication services, including TV, mobile services and Ethernet data onto a single network infrastructure. Something that can be readily achieved for wireless services using digital RoF. For these reasons, operators and mobile equipment vendors are in favour of digital RoF solutions and so common public radio interface (CPRI) and open base station architecture initiative (OBSAI) standards have been developed to enable a common and flexible digital radio transmission interface.

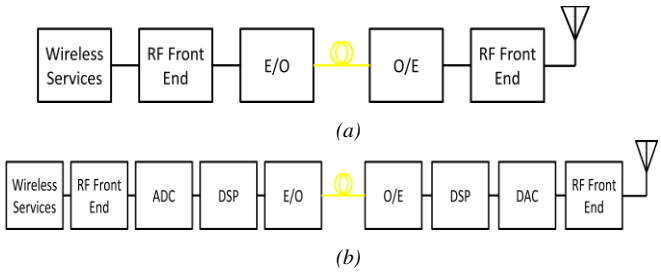

Fig 1. (a) Analogue RoF system (b) Digital RoF system

A typical digital distributed antenna system (DAS) approach using digital RoF technology is shown in *Fig. 2*. Multiple wireless services from base stations (BS) or access points (AP) housed at a central location, typically basement of a building, are digitally distributed over optical fibre links. This system aims to use off-the-shelf digital components and existing in-building infrastructure for wireless coverage. However, the digitisation process normally results in high digital transmission data rate which require expensive digital transceiver modules with high power consumption. Studies **[4][5][6]** have shown a higher capital expenditure (CAPEX) and operational expenditure (OPEX) for digital RoF system compared with analogue RoF as a result of the high line rate and additional hardware required, especially for the latest mobile standards such as Long Term Evolution (LTE) and LTE-Advanced (LTE-A).

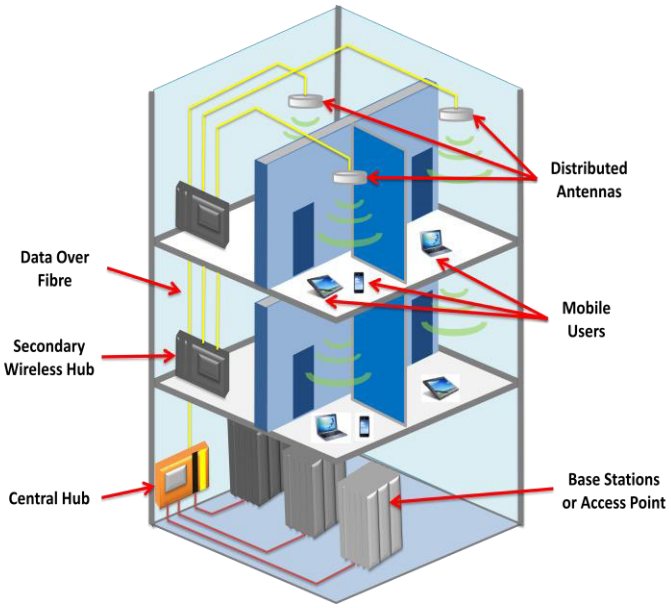

Fig. 2 In-building Digital DAS

To address this issue, a low bit rate digital RoF system using an offline processing data compression algorithm is proposed in [**7**]. With compression, 3G wide-band code division multiple access (WCDMA) service is able to be digitally transmitted over low-cost twisted pair cables for signal coverage in real time **[8]**. In this paper, we demonstrate a real-time service-agnostic digital RoF system which is able to transmit wireless information at a much lower aggregate data rate as well as maintaining the radio performance. The system is implemented on a field programmable gate array (FPGA) platform. Transmission of LTE signals are reported as these are of great interest currently.

II. Theory and System Proposal

A. *Data Rate of Digitised LTE*

Compared with legacy standards, LTE is challenging for digital RoF systems due to its wide channel bandwidth (up to 20MHz) and the use of multiple input multiple output (MIMO) technology. In order to maintain the signal integrity of LTE, the analogue-to-digital converter (ADC) has to meet the sampling and quantisation requirement. A tradeoff between the ADC quantisation bit and sampling rate has been discussed in [**7**]. The sampling requirement is defined by the Nyquist theorem which states that the sample rate has to be greater than twice of the highest frequency component of the input signal. In practice, the actual sampling rate has to be more than the Nyquist rate to tolerate the roll-off of filters. In CPRI, when digitising the signal at baseband the sampling rate is 30.72MHz for 20MHz bandwidth LTE [**9**]. This is derived from the bandwidth used by 2048 subcarriers in the orthogonal frequency division multiple access (OFDMA) process with a 15kHz bandwidth for each subcarrier. In practice, only 1200 subcarriers are defined in 3rd generation partner project (3GPP) TS 36.101 for the case of 20MHz bandwidth including a 2MHz guard band **[10]**. This leaves a large spectral redundancy during digitisation.

From the quantisation perspective, a 16-bit resolution for each baseband in-phase (I) and quadrature (Q) channel is typically required to achieve an adequate dynamic range and satisfactory error value magnitude (EVM) which measures the modulation accuracy of a wireless signal **[4]**. Thus, a digital RoF link will typically require at least 983.04Mbps (30.72MHz × 32- bit) capacity to transmit a single 20MHz LTE channel. CPRI also introduces control words which further increases the overhead. To utilise commercially available transceiver modules, a 1.25Gbps link has to be built to transmit single 20MHz-LTE band in this case. The need for high capacity links is further increased when MIMO is used as each MIMO antenna added will require an additional 1.25Gbps capacity. The CAPEX increases dramatically when higher order MIMO technology is deployed. Furthermore, carrier aggregation (CA) has been specified by the LTE-A standard. The goal is to aggregate multiple LTE frequency bands in order to achieve even higher user bandwidth.

B. *System Proposal*

To deal with the issue of high digital bit rate requirements for in-building wireless coverage in this work, a digital DAS is proposed as shown in *Fig. 3.* The system is composed of a central DAS module and a remote module. Multiple wireless services generated from a BS or AP are fed into the central DAS module where an RF front end module converts them to intermediate frequencies (IF) and automatic gain control (AGC) is applied. The signals are then digitised by ADC and processed using an FPGA. The signal processing consists of four major stages – digital down conversion (DDC), data compression, packetisation and transceiver interface. In the remote module, the received digital data is recovered by the FPGA and DAC. At the far end, they are retransmitted through remote distributed antennas for signal coverage.

As described, a core part of the system is the digital signal processing technique on the FPGA to transport wireless services at a lower bit rate without losing radio performance and the signal agnostic feature. In this system, an initial filtering stage in DDC is used to remove the spectral redundancy at baseband. Then there is a data compression

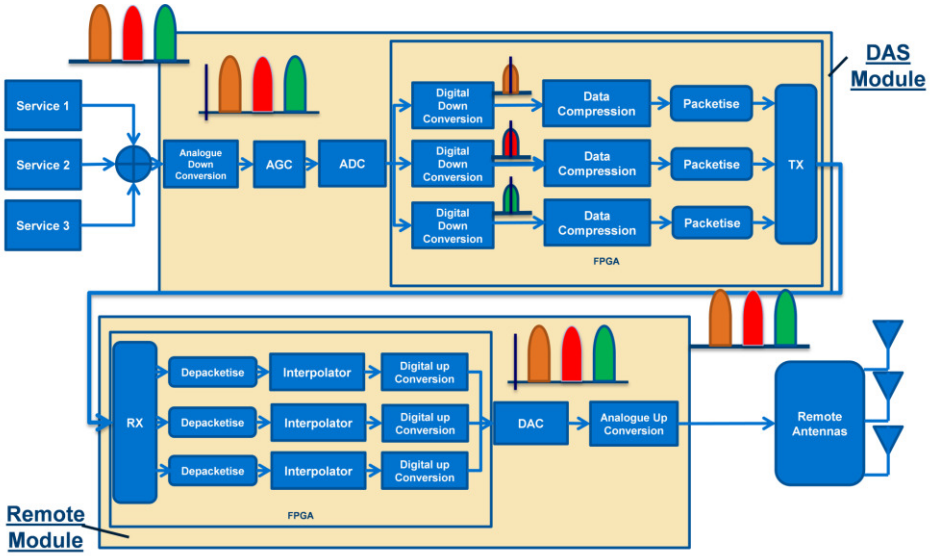

Fig. 3 Multi-service Digital RoF System Proposal

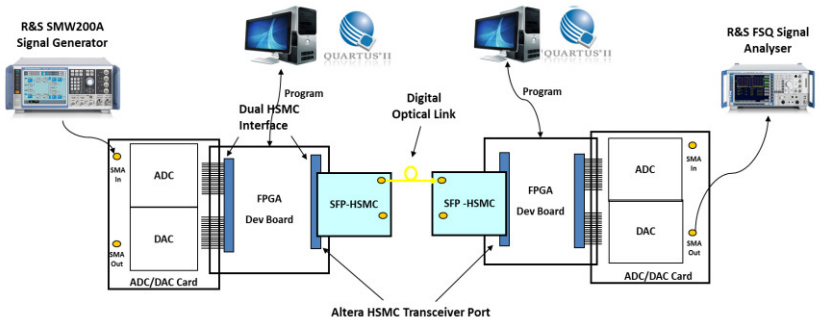

Fig. 4 Experimental Setup

stage which is composed of both sampling and quantisation compression to minimise the data rate required by the link. Due to the unknown input power level at uplink, a large dynamic range is required for the system. The 3GPP has specified an EVM requirement of less than 8% for LTE signal modulated by 64 quadrature amplitude modulation (64-QAM) [**10**]. In the next sections, a report is made of the dynamic range supported by the system which is evaluated by varying the input power level and measuring the EVM value. A dynamic range analysis is also carried out in this paper to illustrate the performance of the system.

III. Experimental Setup And Results

A. *Experimental Setup*

The experimental setup is illustrated on *Fig. 4.* An LTE test signal with 20MHz bandwidth defined by LTE test model 3.1 [**11**] is generated from Rhode and Schwarz (R&S) SMW200A signal generator. The sampling clock of the digitiser is set to 125 Mega samples per second (Msps). To ensure best image rejection, the IF signal is tuned to the centre frequency of the first Nyquist Zone, which is 31.25MHz before digitisation. In practice, an additional RF front end is installed to perform RF/IF conversion.

A 14-bit ADC and DAC pair with 125 Msps sampling rate are used to perform analogue to digital (A/D) and digital to analogue (D/A) conversions. Each of the input/output pins of the converters is interfaced with Terasic's DE4 FPGA development boards through low voltage differential signalling (LVDS) on high speed mezzanine card (HSMC) ports. The DE4 is based on Altera's Stratix IV GX FPGA which is composed of 230K logic elements (LEs) and transceiver blocks supporting multi-standard high speed digital interface [**12**]. A transceiver interface card is connected to the DE4 to interface the FPGA with commercially available transceiver modules. Small form factor pluggable (SFP) modules are among the most commonly used optical digital interface in the market. A SFP-HSMC provides 8 optical or electrical SFP transceiver I/O channels which give users the flexibility to choose different cabling types. In this experiment, two 1.25Gbps optical SFP modules are installed on the transmitting and receiving side of the link, connected by a two-metre single-mode optical fibre.

To test the signal performance, the DAC output streams are supplied to an R&S FSQ signal analyser with 4G LTE testing options. EVM values are measured.

B. *Digital Signal Processing*

The digital signal processing on the two FPGAs is graphically illustrated in *Fig. 5*. The digitisation process generates an oversampled IF data. Oversampling improves the signal-to-quantisation-noise ratio (SQNR) of digitisation according to the following equation:

$$SQNR = 6.02B + 4.77 - 10log\eta + 10log(\frac{Fs}{2*BW}) \qquad (1)$$

where B is the ADC quantisation bit, η is the peak to average ratio, Fs is the sampling rate and BW is the signal bandwidth. From this equation, the quantisation noise level is determined by both quantisation resolution and sampling rate. One bit increase of resolution will improve the SQNR by roughly 6dB and every doubling of sampling rates adds approximately 3dB to the total SQNR. Commercial ADCs have worse SQNR than this theoretical value. In this experiment, the 14-bit and 125 Msps ADC has a ~75dB SQNR for the digitised IF input. Ideally a 16-bit ADC is used to give a better performance. The purpose of using a larger quantisation bit width is to ensure that high input power will not be saturated and low input power will not fall below the sensitivity level. The front end AGC is able to set the signal level within a certain range, but the dynamic range requirement is still high for the rest of the system

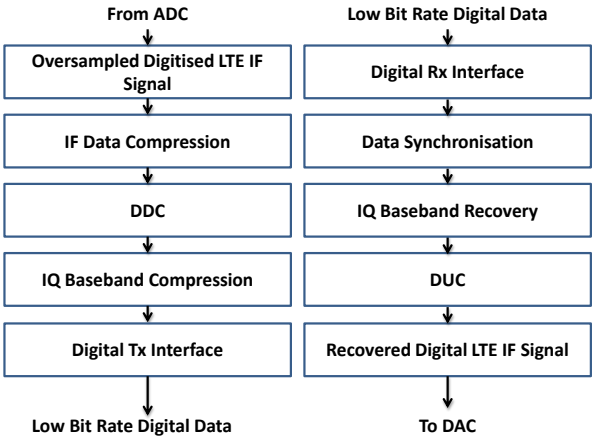

Fig. 5 Digital Processing Algorithm

An IF compression method is designed to make sure the signal quality does not degrade when reducing the sampling rate and quantisation resolution. This process continuously trains the signal to learn optimum compression parameters. After this stage, the 14-bit input is compressed to an 8-bit data stream. A fixed training length has to be carefully considered to avoid any error occurred during the real-time processing. A lower bit number not only reduces the overall transmission bit rate, but also eases the need for larger FPGA resources. 8-bit arithmetical computation is carried out in DDC and DUC on the FPGAs until the signal is recovered back to 14-bit format.

In the DDC, the signal is down converted from a 31.25MHz IF to baseband. Each IQ component is filtered by a carefully designed finite impulse response (FIR) filter to remove the spectral redundancy. Due to multiplication in mixing and filtering processes which increases the IQ bit width, another self-training loop is used to remove the redundant bits generated during the processes. Sampling compression is performed by decimation of the IQ data stream and re-sampling at a lower clock rate. Ideally a 20MHz clock rate is used to sample the filtered signal. This experiment re-samples the signal at 25MHz to avoid clock jittering caused by fractional down sampling. Thus, the data rate after compression is 400Mbps (8×25×2 Mbps) for the 8-bit IQ data which is then coded by 8b/10b coding scheme with K28.5 (10'b0101111100) as a control word for word alignment and serially transmitted through the optical transceiver.

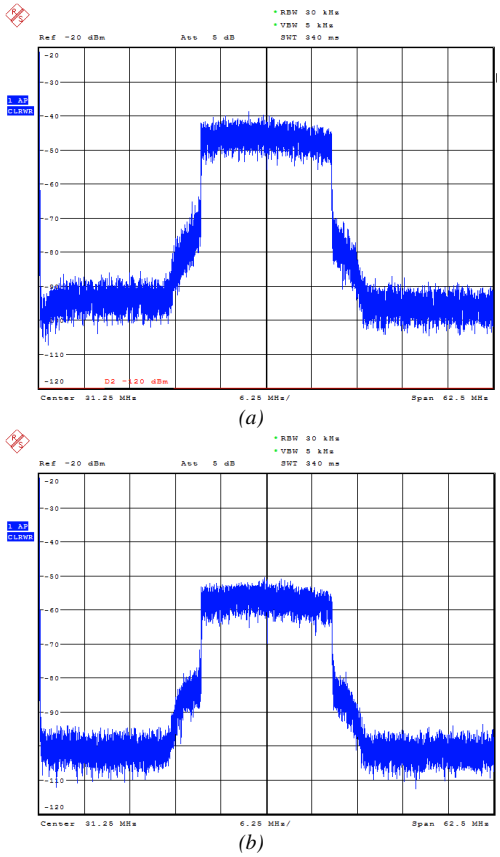

Fig. 6. Spectrum of Experimental Output for (a) Input Power at -10dBm and (b) Input Power at -40dBm

At the receiver FPGA, data synchronisation is performed by built-in FPGA circuitry. An IQ baseband recovery method is used to compensate the sampling rate of the compressed data and IQ channels are restored before digital up conversion (DUC). Unlike in DDC, DUC firstly filters the signal using a matched FIR filter and then reassembles the signal into its IF format. At the output of the DUC, the 14-bit data is reconstructed according to the bit width compressed. *Fig. 6* shows the output spectrum displayed at R&S FSQ signal analyser for input at -10dBm and input at -40dBm.

An utilisation report generated from Altera's Quartus II software is shown on *Fig. 7*. Only 15% of the total logic resource is used for a full-duplex processing on both FPGAs. In this case, a single FPGA is therefore able to process at least 6 channels of radio input simultaneously. Research on FPGA code optimisation is ongoing to further reduce the resource utilisation.

Family	Stratix IV
Device	EP4SGX230KF40C2
Timing Models	Final
Logic utilization	15 %
Combinational ALUTs	16,841 / 182,400 (9 %)
Memory ALUTs	106 / 91,200 (< 1 %)
Dedicated logic registers	22,384 / 182,400 (12 %)
Total registers	22384
Total pins	372 / 888 (42 %)
Total virtual pins	0
Total block memory bits	2,949,120 / 14,625,792 (20 %)
DSP block 18-bit elements	14 / 1,288 (1 %)
Total GXB Receiver Channel PCS	1 / 24 (4 %)
Total GXB Receiver Channel PMA	1 / 36 (3 %)
Total GXB Transmitter Channel PCS	1 / 24 (4 %)
Total GXB Transmitter Channel PMA	1 / 36 (3 %)
Total PLLs	1 / 8 (13 %)
Total DLLs	0 / 4 (0 %)

Fig. 7 FPGA Unitisation for Full Duplex Processing

C. Experimental Results

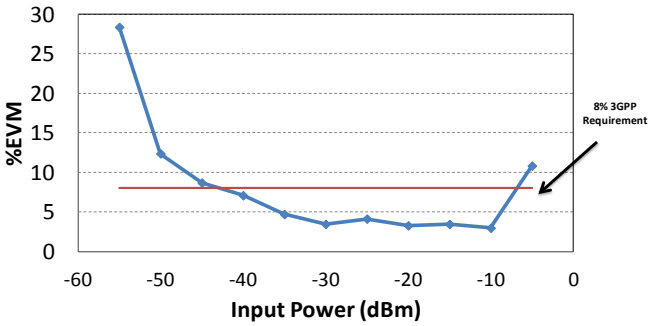

Fig. 8 EVM Performance of Compressed LTE Transmission

An EVM test is carried out to analyse the dynamic range supported by the system. 64QAM has been defined as the highest-order modulation format in LTE and its EVM requirement is 8%. This experiment is conducted according to this highest requirement to ensure the system is fully compatible with the standard. *Fig. 8* indicates the EVM performance against different input power levels to the ADC at a real-time compressed data rate of 400Mbps. The lowest EVM with a value of 2.96% occurs at -10dBm because that the self-training algorithm limits maximum ADC input to match the 8-bit quantisation range. In practice, the system input power can

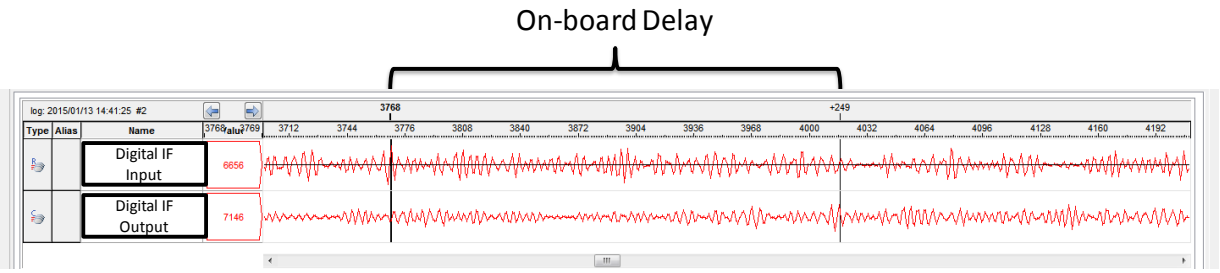

Fig. 9. On-board Latency of the Digital Signal Processing

be adjusted in a front end AGC to allow higher input to the system. The EVM values are maintained at a level less than 5% over a 25dB range, and then start to increase with reducing input power. A 30-35dB dynamic range is demonstrated in the figure below the 8% EVM requirement. Note that this dynamic range is measured at the input before ADC. In practice front end AGC circuitry would be able to further increase the range. A commercial AGC with 40dB variable gain is able to add another 40dB to the total range supported by the system.

Another issue of concern for practical implementation of indoor LTE coverage is the system latency. A large delay in signal processing and transceiver will degrade the quality of service (QoS) for a wireless signal. LTE has a stringent latency requirement compared with legacy mobile standards. Industrial in-building wireless vendors typically allow of the delay of less than 10µs in DAS for LTE coverage. Most delay in our system occurs during the digital signal processing. Altera's SignalTap II signal analyser allows users to monitor and analyse the on-board signalling during real-time processing on the FPGA. A single FPGA external loopback test is performed to measure the total latency on both transmitting and receiving FPGAs. The digital IF after digitisation and digital IF after complete signal reconstruction are captured and displayed as shown on *Fig. 9*. As seen, the same digital IF pattern as input is observed after 249 samples at the digital IF output. Since the system is clocked at 125 Msps, the total latency can be calculated as 1.992µs. This gives a sufficient latency budget for signal propagation in the link and RF front end.

D. Link Efficiency

The experiment has shown that the compressed LTE method is able to transmit a single 20MHz LTE channel at a date rate of 400Mbps. Further sampling redundancy can be removed if the clock rate is tuned to 20MHz. At this clock speed, a data rate of 320Mbps can be achieved. Therefore, a single 1.25Gbps transceiver link is able to support up to three 20MHz LTE channels. If MIMO is used, one 2x2 MIMO and a single-antenna LTE services can be carried together in a link with the same capacity. A table of comparison for total spectral bandwidth supported in conventional CPRI and compressed LTE schemes is shown on *Table 1*. Link efficiency is 3-time higher for the compressed LTE than conventional system defined in CPRI.

	Conventional CPRI	Compressed LTE
Total Bandwidth Supported using 1.25Gbps Transceiver	Single 20MHz LTE band	Up to 3 x 20MHz LTE bands
Total Bandwidth Supported using 6.25Gbps Transceiver	80MHz -100MHz	Up to 300MHz

Table 1. Comparison of Bandwidth Supported by CPRI and the Compressed LTE using Commercial Transceivers Modules

IV. CONCLUSION

Compared with a conventional analogue RoF system, the digital RoF transmission is able to mitigate the negative effect of radio performance deterioration and need for dedicated infrastructure. For these reasons, many industrial wireless vendors adopt the digital DAS for in-building coverage. However, some studies have pointed out the increased CAPEX and OPEX of conventional digital DAS due to the large data rates generated. This paper demonstrates a new form of digital RoF system that is able to compress and transport a digitised LTE service for wireless coverage.

We develop and discuss a new compression algorithm that is able to achieve 3 times higher spectral efficiency than industrial digital approach, such as CPRI. With compression, a 30-35dB input dynamic range before the ADC is demonstrated in a 64QAM 20MHz LTE test. A final system dynamic range could reach above 70dB if a front end AGC is used. The paper also investigates the latency caused by the digital signal processing. It has been shown that the delay is less than 2µs on the FPGA boards to transmit and receive. We believe that this digital RoF system will significantly benefit in-building wireless coverage, particularly with increasing bandwidth and capacity requirements in future mobile standards.

ACKNOWLEDGMENT

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